AiP31032
Dot Matrix LCD Controller/Driver

Product Specification

Specification Revision History:

Version	Data	Description
2017-09-A1	2017-09	New
2019-08-A2	2019-08	Replace the new template
2022-05-A3	2022-03	Modify the instruction code (D4) of internal OSC frequency in the 5.17.2、Instruction table at “Extension mode”

1、General Description

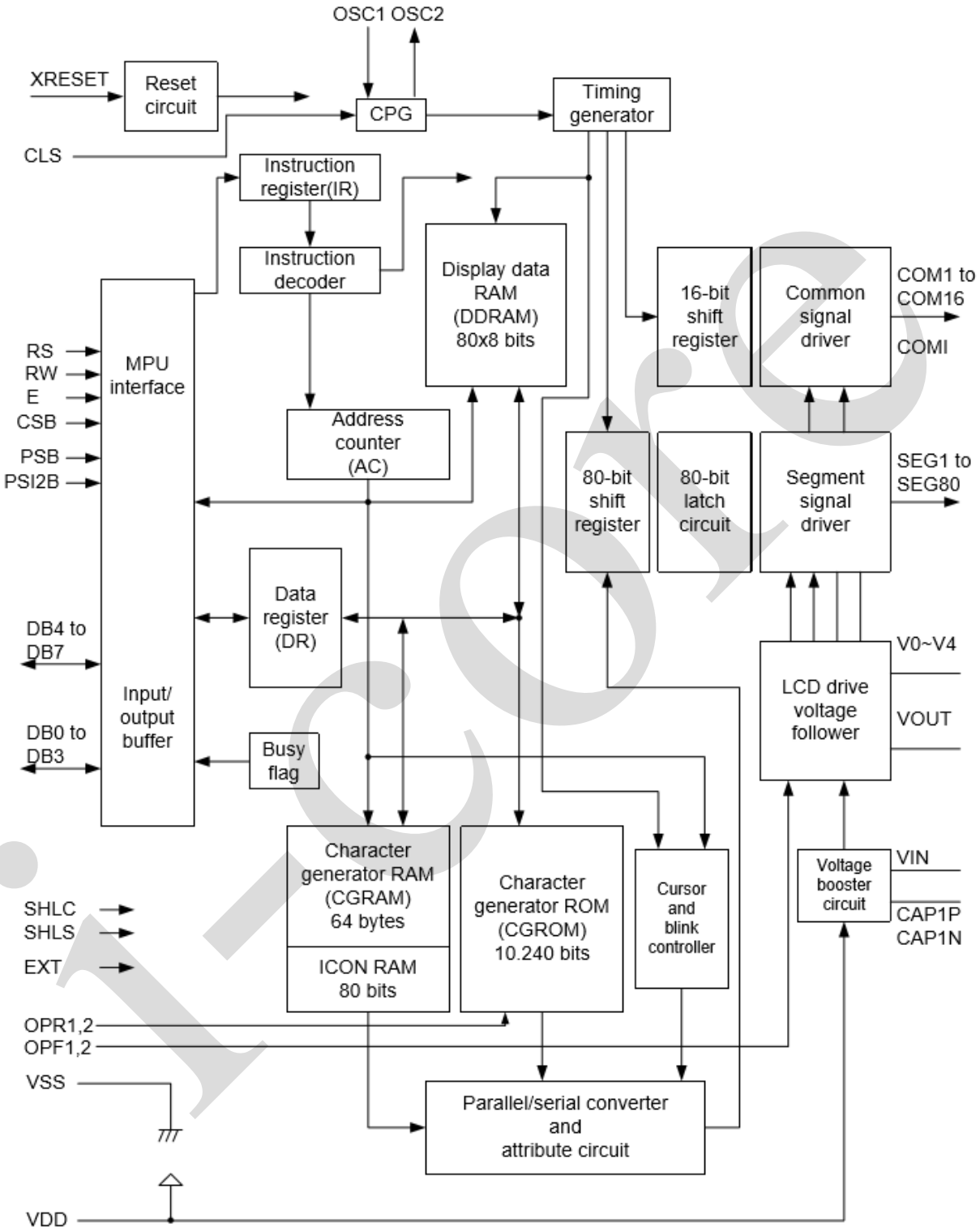
The AiP31032 dot-matrix liquid crystal display controller can display alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4/8-bit with 6800-series or 8080-series, 4-line serial interface and I^2C-bus interface. Since all the functions such as display RAM, character generator ROM/RAM and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be used with this controller/driver. The AiP31032 dot-matrix LCD driver does not need extra cascaded drivers.

Features:

- 5×8 dot matrix possible
- Low power operation support: 2.7 to 5.5V
- Range of LCD driver power: 3.0 to 7.0V
- 4-bit, 8-bit, serial MPU or 400kbits/s fast I^2C-bus interface are available
- 80×8-bit display RAM (80 characters max.)
- 10,240-bit character generator ROM for a total of 256 character fonts (max)
- 64×8-bit character generator RAM (max)
- 16-common×80-segment and 1-common×80-segment ICON liquid crystal display driver
- 16×5–bit ICON RAM (max)
- Wide range of instruction functions: Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift, double height font
- Automatic reset circuit that initializes the controller/driver after power on and external reset pin
- Built-in voltage booster and follower circuit (low power consumption)
- Internal oscillator (Frequency=540kHz) and external clock
- Instruction compatible to AiP31066 and AiP31068
- Multi-selectable for CGRAM/CGROM size
- Com/Seg direction selectable
- Available in COG type

2、Block Diagram And Pin Description

2.1、Block Diagram



2.2、Pin Description

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Interfaced with</th><th>Function</th></tr>
<tr><td>XRESET</td><td>1</td><td>I</td><td>MPU</td><td>External reset pin. Only if the power on reset used, the XRESET pin must be fixed to VDD.
Low active.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Select registers.
0: Instruction register (for write)
Busy flag & address counter (for read)
1: Data register (for write and read)</td></tr>
<tr><td>R/W</td><td>1</td><td>I</td><td>MPU</td><td>Select read or write (In parallel mode).
0: Write 1: Read</td></tr>
<tr><td>E</td><td>1</td><td>I</td><td>MPU</td><td>Starts data read/write.
(“E” must connect to “VDD” when serial interface is selected.)</td></tr>
<tr><td>CSB</td><td>1</td><td>I</td><td>MPU</td><td>Chip select in parallel mode and serial interface (Low active).When the CSB in falling edge state (in serial interface), the shift register and the clock counter are reset.</td></tr>
<tr><td rowspan="2">DB4 to DB7</td><td rowspan="2">4</td><td rowspan="2">I/O</td><td rowspan="2">MPU</td><td>Four high order bi-directional data bus pins. Used for data transfer and receive between the MPU and the AiP31032. DB7 can be used as a busy flag. In serial interface mode DB7 is SI (input data), DB6 is SCL (serial clock).</td></tr>
<tr><td>In I^2C interface DB7 (SDA) is input data and DB6 (SCL) is clock input.
SDA and SCL must connect to I^2C bus (I^2C bus is to connect a resister between SDA/SCL and the power of I^2C bus).</td></tr>
<tr><td>DB0 to DB3</td><td>4</td><td>I/O</td><td>MPU</td><td>Four low order bi-directional data bus pins. Used for data transfer and receive between the MPU and the AiP31032. These pins are not used during 4-bit operation.</td></tr>
<tr><td>EXT</td><td>1</td><td>I</td><td>ITO option</td><td>Extension instruction select:
0: enable extension instruction (add contrast/ICON/double height font/ extension instruction)
1: disable extension instruction (without 5×11dot font)</td></tr>
<tr><td>PSB</td><td>1</td><td>I</td><td>MPU</td><td>Interface selection
0: serial mode (“E” must connect to “VDD” when serial mode is selected.)
1: parallel mode(4/8 bit) In I^2C interface PSB must connect to VDD</td></tr>
<tr><td>PSI2B</td><td>1</td><td>I</td><td>ITO option</td><td>
<table>
<tr><th>PSB</th><th>PSI2B</th><th>Interface</th></tr>
<tr><td>0</td><td>0</td><td>X</td></tr>
<tr><td>0</td><td>1</td><td>SI4</td></tr>
<tr><td>1</td><td>0</td><td>SI2(I^2C)</td></tr>
<tr><td>1</td><td>1</td><td>Parallel68</td></tr>
</table>
</td></tr>
<tr><td>OPR1
OPR2</td><td>2</td><td>I</td><td>ITO option</td><td>Character generator select:：
<table>
<tr><th>OPR1</th><th>OPR2</th><th>CGROM</th><th>CGRAM</th></tr>
<tr><td>0</td><td>0</td><td>240</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>250</td><td>6</td></tr>
<tr><td>1</td><td>0</td><td>248</td><td>8</td></tr>
<tr><td>1</td><td>1</td><td>256</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>SHLC</td><td>1</td><td>I</td><td>ITO option</td><td>Common signals direction select:
0: Com1~16←Row address 15~0 (Invert)
1: Com1~16←Row address 0~15 (Normal)</td></tr>
</table>

<table>
<tr><td>SHLS</td><td>1</td><td>I</td><td>ITO option</td><td>Segment signals direction select:
0: Seg1~80←Column address 79~0(Invert)
1: Seg1~80←Column address 0~79(Normal)</td></tr>
<tr><td>COM1 to COM16</td><td>16</td><td>O</td><td>LCD</td><td>Common signals that are not used are changed to non-selection waveform. COM9 to COM16 are non-selection waveforms at 1/8 or 1/9 duty factor</td></tr>
<tr><td>COMI</td><td>2</td><td>O</td><td>LCD</td><td>ICON Common signals</td></tr>
<tr><td>SEG1 to SEG80</td><td>80</td><td>O</td><td>LCD</td><td>Segment signals</td></tr>
<tr><td>OPF1
OPF2</td><td>2</td><td>I</td><td>ITO option</td><td>The built-in voltage follower circuit selection
<table>
<tr><th>OPF1</th><th>OPF2</th><th>Bias select</th></tr>
<tr><td>0</td><td>0</td><td>Built-in voltage follower(EXT=0)</td></tr>
<tr><td>0</td><td>1</td><td>Built-in bias resistor(3.3kΩ) ±30%</td></tr>
<tr><td>1</td><td>0</td><td>Built-in bias resistor(9.6kΩ) ±30%</td></tr>
<tr><td>1</td><td>1</td><td>External bias resistor select</td></tr>
</table></td></tr>
<tr><td>CAP1P</td><td>1</td><td>-</td><td>Power supply</td><td rowspan="2">For voltage booster circuit(VDD-VSS) External capacitor about 0.1uF~4.7uF</td></tr>
<tr><td>CAP1N</td><td>1</td><td>-</td><td>Power supply</td></tr>
<tr><td>VIN</td><td>1</td><td>-</td><td>Power supply</td><td>Input the voltage to booster</td></tr>
<tr><td>VOUT</td><td>1</td><td>-</td><td>Power supply</td><td>DC/DC voltage converter. Connect a capacitor between this terminal and VIN when the built-in booster is used.</td></tr>
<tr><td>V0 toV4</td><td>5</td><td>-</td><td>Power supply</td><td>Power supply for LCD drive V0-GND =7V (Max)
Built-in/external Voltage follower circuit</td></tr>
<tr><td>VDD
VSS</td><td>2</td><td>-</td><td>Power supply</td><td>VDD: 2.7V to 5.5V, GND: 0V</td></tr>
<tr><td>CLS</td><td>1</td><td>I</td><td>ITO option</td><td>Internal/External oscillation select
0:external clock
1:internal oscillation</td></tr>
<tr><td>OSC1
OSC2</td><td>2</td><td>I/O</td><td>Oscillation</td><td>When the pin input is an external clock, it must be input to OSC1.</td></tr>
<tr><td>TEST1,2</td><td>2</td><td>I/O</td><td>Test pin</td><td>TEST1, 2 must connect to VDD.</td></tr>
</table>

2.3、EXT option pin difference table

	Normal mode（EXT=1）	Extension mode（EXT=0）
Booster	Always OFF.	ON/OFF control by instruction.
Bias (V0~V4)	Can’t use the follower circuit. Only use external resistor or internal resistor(1/5 bias).	Follower or internal/external resistor selectable.
Contrast adjust	Control by external VR.	Control by instruction with follower Control by external VR with internal/ external resistor.
ICON RAM	Can’t be used.	RAM size has 80 bit width (S1~S80).
Instruction	Control normal instruction similar to AiP31066.	Control extension instruction for low power consumption.
Double height font	Only 5×8 font.	Can set 5×8 or 5×16 font.
OSC frequency adjust	Only adjust by external clock.	Can set OSC frequency by instruction set.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, All voltage referenced to GND, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Power Supply Voltage	VDD	-0.3~6.0	V
LCD Supply Voltage	V_{LCD}	7.0-VSS~-0.3+GND	V
Input Voltage	V_{IN}	-0.3~VDD+0.3	V
Operating Temperature	T_{amb}	-30~+85	℃
Storage Temperature	T_{stg}	-65~+150	℃

3.2、Electrical Characteristics

3.2.1、DC Characteristics 1

(T_{amb}=25℃, VDD=2.7V~4.5V.)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	-	2.7	-	4.5	V
LCD Voltage	V_{LCD}	V0-GND	2.7	-	7.0	V
Power Supply Current	I_{CC}	VDD=3.0V (Use internal booster/follower circuit)	-	160	230	uA
Input High Voltage (Except OSC1)	V_{IH1}	-	1.9	-	VDD	V
Input Low Voltage (Except OSC1)	V_{IL1}	-	-0.3	-	0.8	V
Input High Voltage (OSC1)	V_{IH2}	-	0.7VDD	-	VDD	V
Input Low Voltage (OSC1)	V_{IL2}	-	-	-	0.2VDD	V
Output High Voltage (DB0 - DB7)	V_{OH1}	I_{OH}=-1mA	0.75VDD	-	-	V
Output Low Voltage (DB0 - DB7)	V_{OL1}	I_{OL}=1mA	-	-	0.8	V
Output High Voltage (Except DB0 - DB7)	V_{OH2}	I_{OH}=-0.04mA	0.8VDD	-	VDD	V
Output Low Voltage (Except DB0 - DB7)	V_{OL2}	I_{OL}=0.04mA	-	-	0.2VDD	V
Common Resistance	R_{COM}	V_{LCD}=4V, I_d=0.05mA	-	2	20	kΩ
Segment Resistance	R_{SEG}	V_{LCD}=4V, I_d=0.05mA	-	2	30	kΩ
Input Leakage Current	I_{LEAK}	$V_{IN=}$0V~VDD	-1	-	1	uA
Pull Up MOS Current	I_{PUP}	VDD=3V	20	30	40	uA
Oscillation frequency	f_{OSC}	VDD=3V, 1/17duty	350	540	1100	kHz

3.2.2 DC Characteristics 2

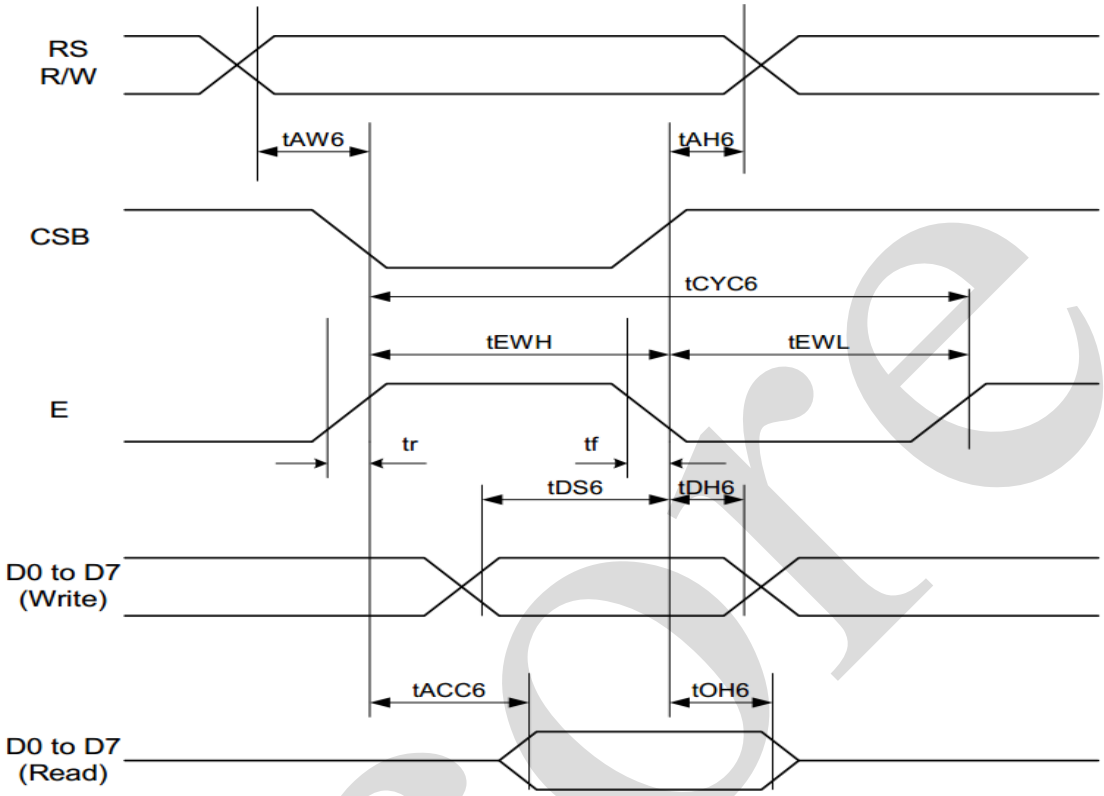
(Unless otherwise specified, T_{amb}=25℃, VDD=4.5~5.5V)

Characteristic	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	-	4.5	-	5.5	V
LCD Voltage	V_{LCD}	V0-GND	2.7	-	7.0	V
Power Supply Current	I_{CC}	VDD=5.0V (Use internal booster/follower circuit)	-	240	340	uA
Input High Voltage (Except OSC1)	V_{IH1}	-	2.7	-	VDD	V
Input Low Voltage (Except OSC1)	V_{IL1}	-	-0.3	-	0.8	V
Input High Voltage (OSC1)	V_{IH2}	-	0.7VDD	-	VDD	V
Input Low Voltage (OSC1)	V_{IL2}	-	-	-	1.0	V
Output High Voltage (DB0 - DB7)	V_{OH1}	I_{OH}=-1mA	3.8	-	VDD	V
Output Low Voltage (DB0 - DB7)	V_{OL1}	I_{OL}=1mA	-	-	0.8	V
Output High Voltage (Except DB0 - DB7)	V_{OH2}	I_{OH}=-0.04mA	0.8VDD	-	VDD	V
Output Low Voltage (Except DB0 - DB7)	V_{OL2}	I_{OL}=0.04mA	-	-	0.2VDD	V
Common Resistance	R_{COM}	V_{LCD}=4V, I_d=0.05mA	-	2	20	kΩ
Segment Resistance	R_{SEG}	V_{LCD}=4V, I_d=0.05mA	-	2	30	kΩ
Input Leakage Current	I_{LEAK}	$V_{IN=}$0V~VDD	-1	-	1	uA
Pull Up MOS Current	I_{PUP}	VDD = 5V	65	95	125	uA
Oscillation frequency	f_{OSC}	VDD=5V, 1/17duty	350	540	1100	kHz

4、Testing Circuit

4.1、AC Characteristics

4.1.1、6800 Interface

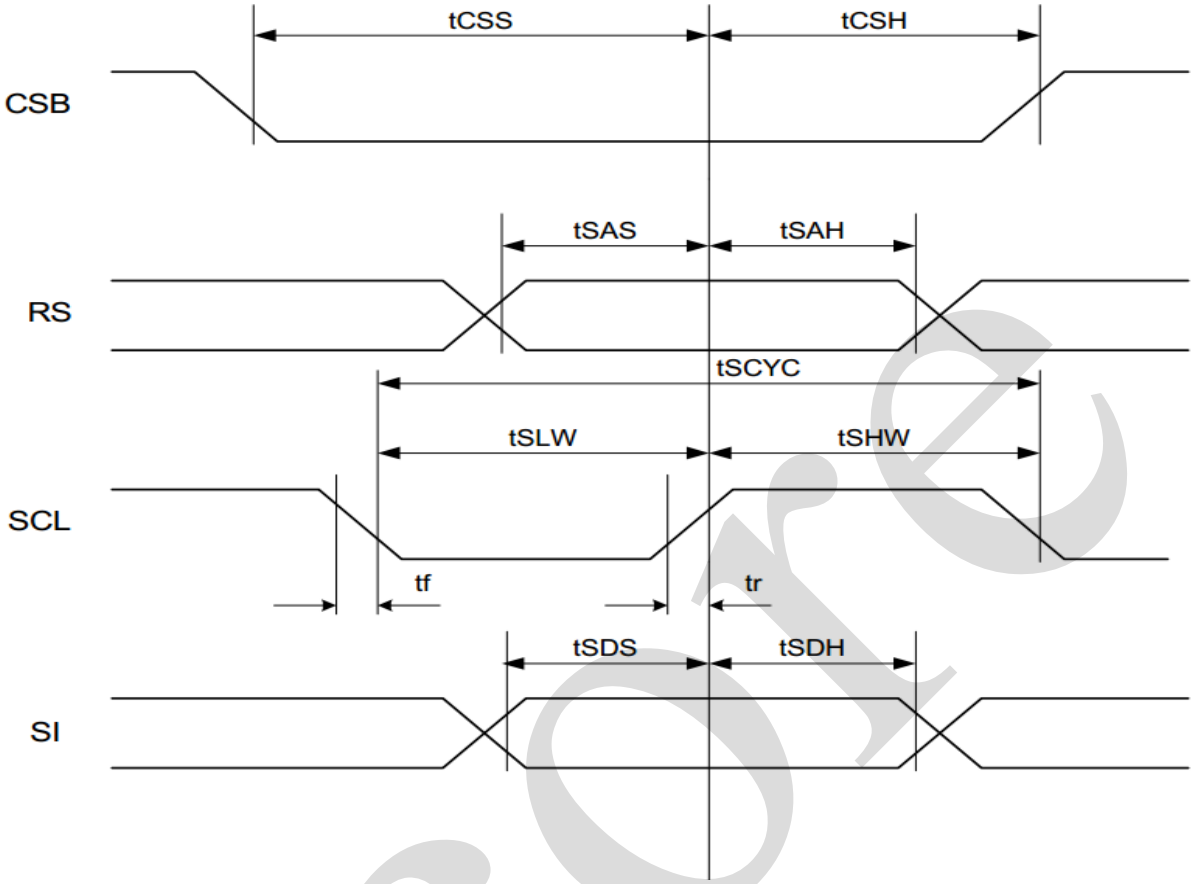


(T_{amb}=25℃)

Item	Signal	Symbol	Condition	VDD=2.7~4.5V		VDD=4.5~5.5V		Unit
				Min.	Max.	Min.	Max.	
Address hold time	RS	tAH6	-	20	-	20	-	ns
Address setup time	RS	tAH6	-	20	-	20	-	ns
System cycle time	RS	tCYC6	-	400	-	280	-	ns
Data setup time	D0~D7	tDS6	-	100	-	80	-	ns
Data hold time	D0~D7	tDH6	-	40	-	20	-	ns
Access time	D0~D7	tACC6	C_L=100pF	-	500	-	400	ns
Output disable time	D0~D7	tOH6		300	-	150	-	ns
Enable Rise/Fall time	E	tr, tf	-	-	20	-	20	ns
Enable H pulse time	E	tEWH	-	200	-	120	-	ns
Enable L pulse time	E	tEWL	-	150	-	130	-	ns

Note: All timing is specified using 20% and 80% of VDD as the reference.

4.1.2、Serial Interface

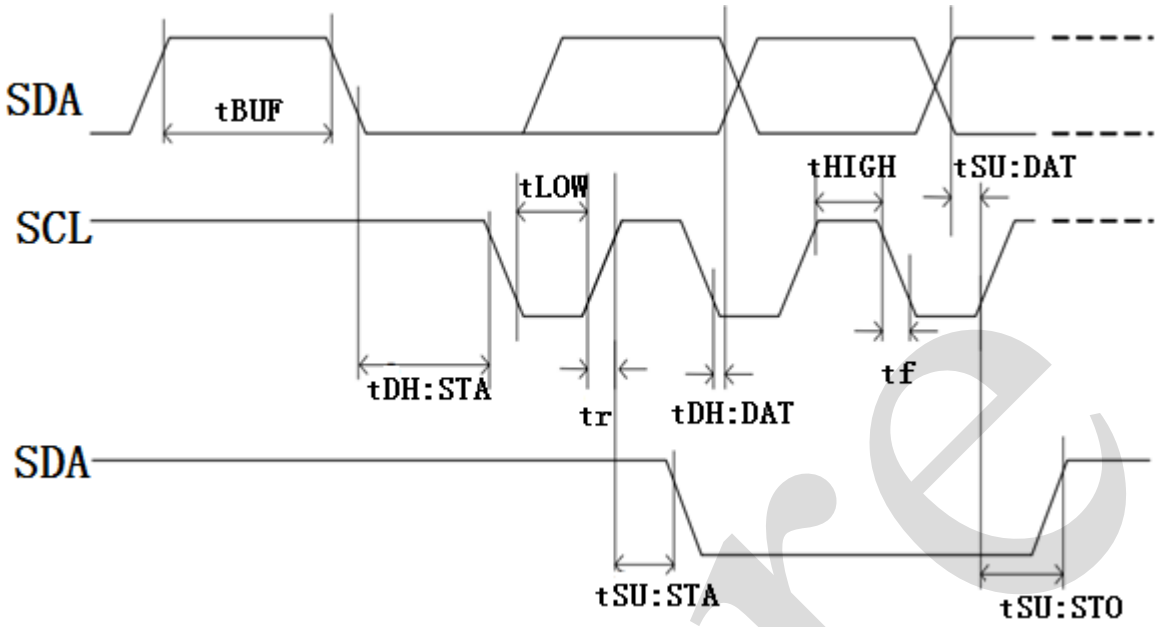


(T_{amb}=25℃)

Item	Signal	Symbol	Condition	VDD=2.7~4.5V		VDD=4.5~5.5V		Unit
				Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	200	-	100	-	ns
SCL “H” pulse width		tSHW		20	-	20	-	ns
SCL “L” pulse width		tSLW		160	-	120	-	ns
SCL Rise/Fall time		tr, tf	-	-	20	-	20	ns
Address setup time	RS	tSAS	-	10	-	10	-	ns
Address hold time		tSAH		250	-	150	-	ns
Data setup time	SI	tSDS	-	10	-	10	-	ns
Data hold time		tSDH		10	-	20	-	ns
CS-SCL time	CS	tCSS	-	20	-	20	-	ns
		tCSH		350	-	200	-	ns

Note: All timing is specified using 20% and 80% of VDD as the standard.

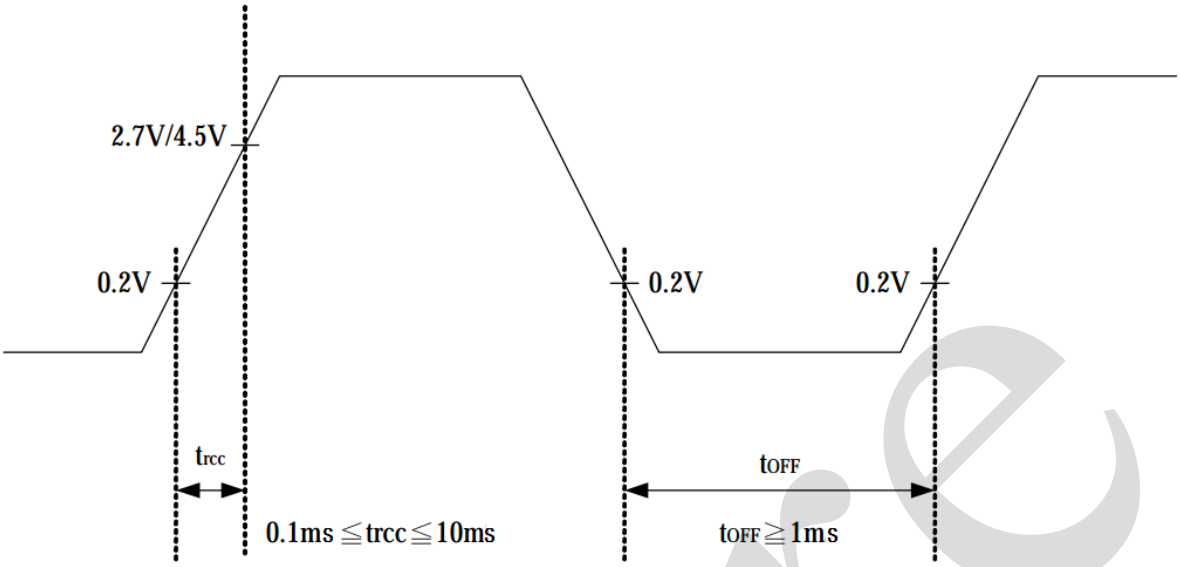
4.1.3、I²C interface



(T_{amb}=25℃)

Item	Signal	Symbol	Condition	VDD=2.7~4.5V		VDD=4.5~5.5V		Unit
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	fSCLK	-	DC	400	DC	400	kHz
SCL clock low period		tLOW		1.3	-	1.3	-	us
SCL clock high period		tHIGH		0.6	-	0.6	-	us
Data set-up time	SI	tSU:DAT	-	180	-	100	-	ns
Data hold time		tDH:DAT		0	0.9	0	0.9	us
SCL, SDA rise time	SCL, SDA	tr	-	20+0.1 Cb	300	20+0.1 Cb	300	ns
SCL, SDA fall time		tf		20+0.1 Cb	300	20+0.1 Cb	300	ns
Capacitive load represent by each bus line	-	Cb	-	-	400	-	400	pF
Setup time for a repeated START condition	SI	tSU:STA	-	0.6	-	0.6	-	us
Start condition hold time		tDH:STA		0.6	-	0.6	-	us
Setup time for STOP condition	-	tSU:STO	-	0.6	-	0.6	-	us
Bus free time between a Stop and START condition	SCL	tBUF	-	1.3	-	1.3	-	us

4.1.4、Internal Power Supply Reset



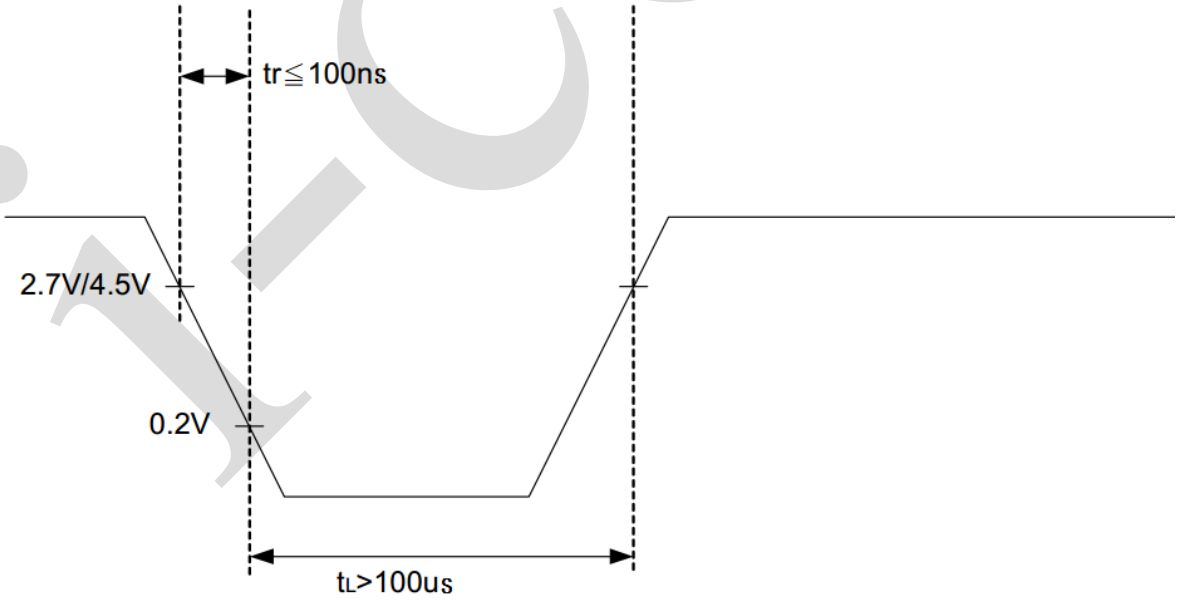
Notes:

[1] t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.

[2] Specified at 4.5V for 5V operation, and at 2.7V for 3V operation.

[3] If 2.7V/4.5V is not reached during 3V/5V operation, internal reset circuit will not operate normally.

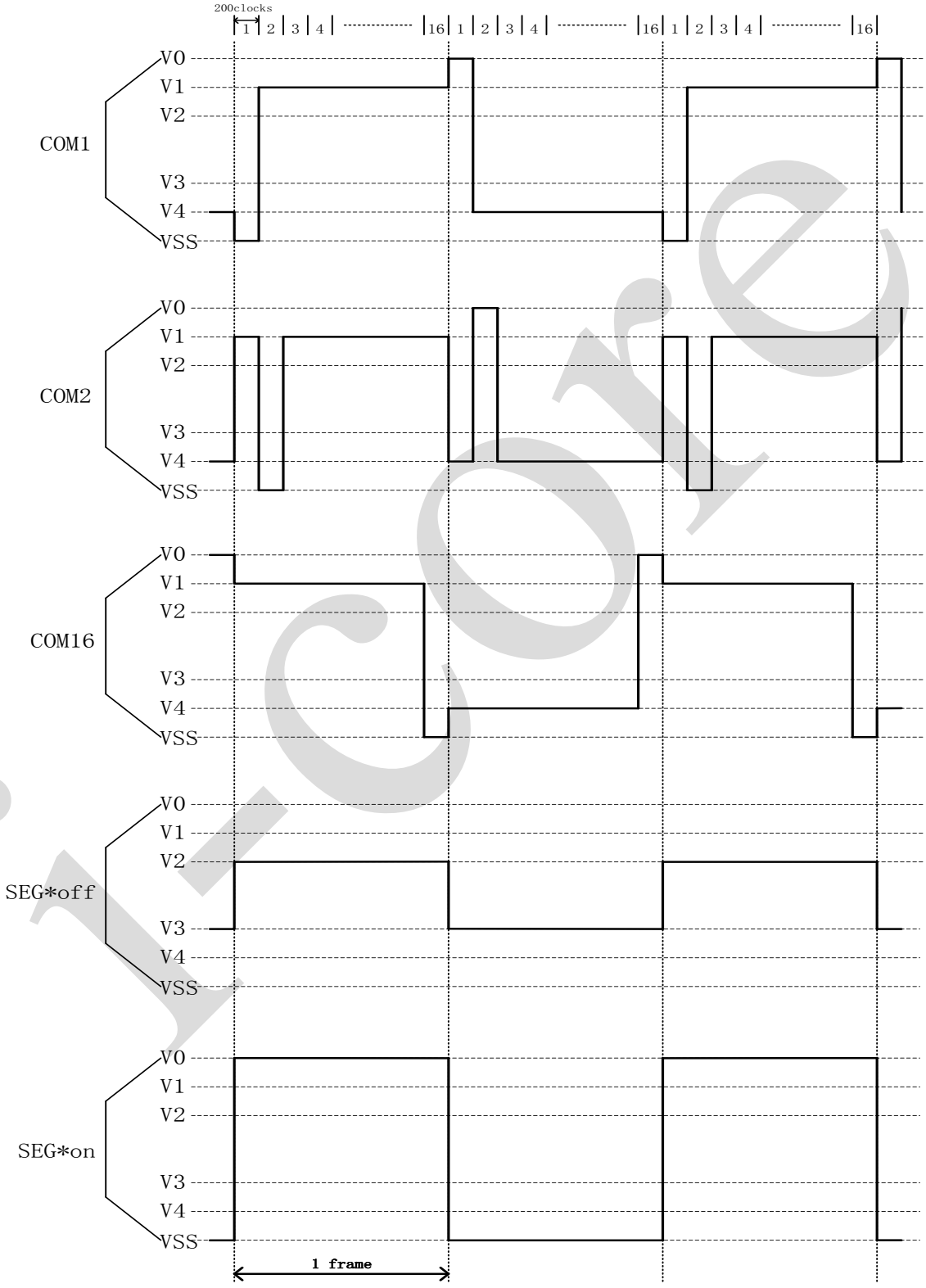
4.1.5、Hardware reset(XRESET)



4.2、LCD Frame Frequency

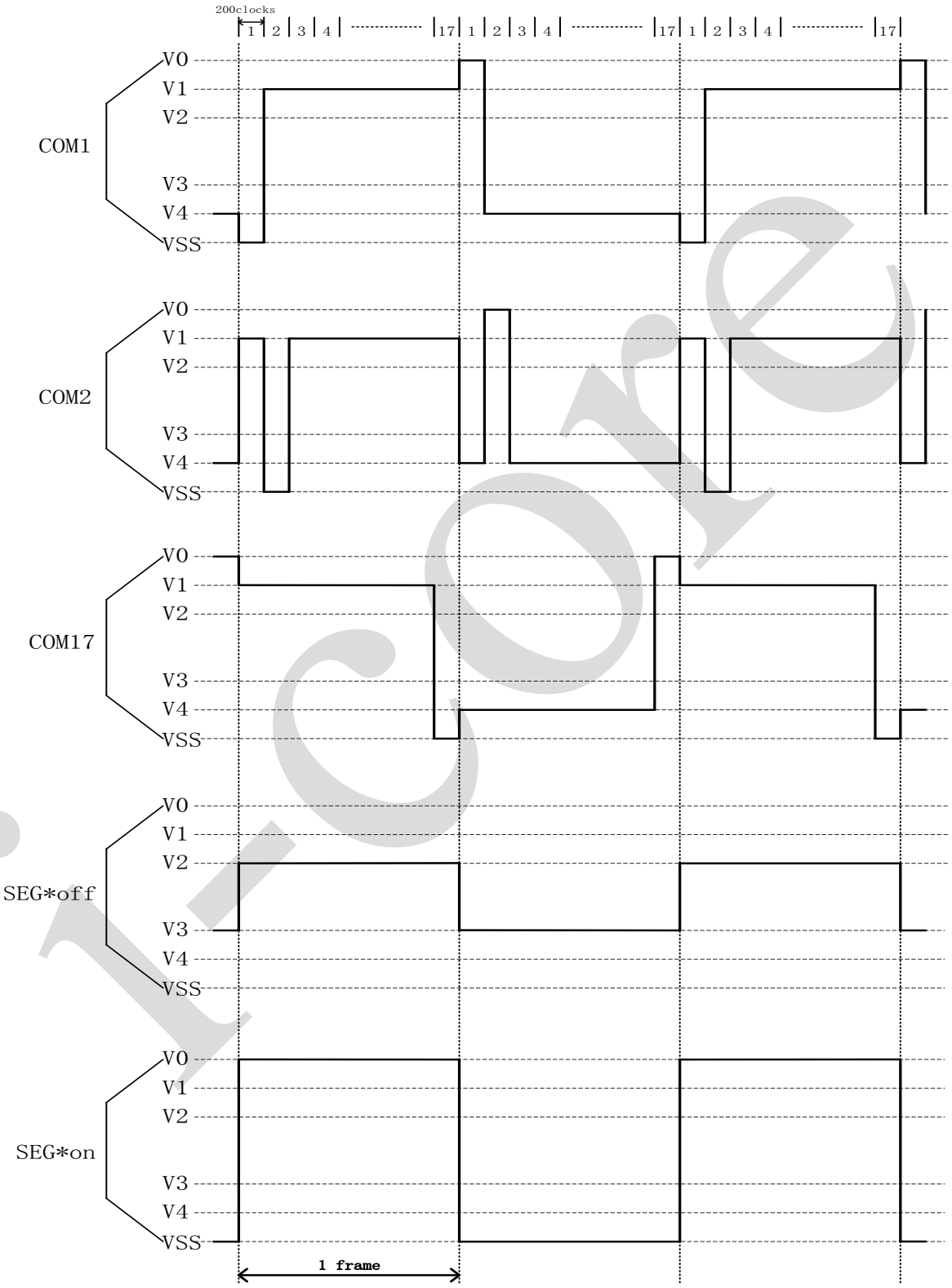
4.2.1、1/16 Duty(normal mode)

Assume the oscillation frequency is 540kHz, 1 clock cycle time = 1.85us, 1/16 duty, 1/5 bias, 1 frame =1.85us ×200 ×16 = 5.92ms=168.9Hz (SHLC and SHLS connect to High).



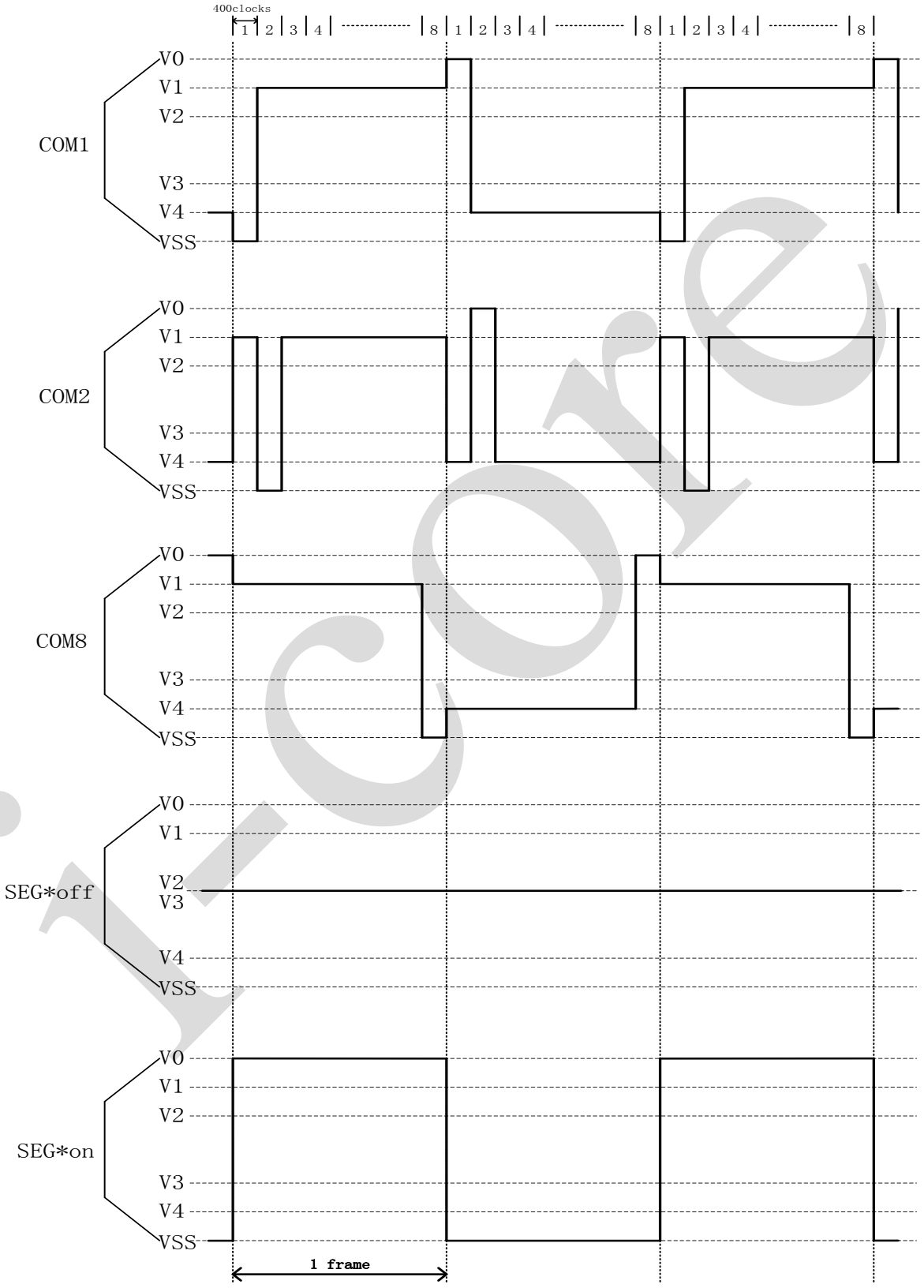
4.2.2、1/17 Duty(Extension mode)

Assume the oscillation frequency is 540kHz, 1 clock cycle time = 1.85us, 1/17 duty, 1/5 bias, 1 frame =1.85us ×200 ×17 = 6.29ms=159Hz (SHLC and SHLS connect to High).



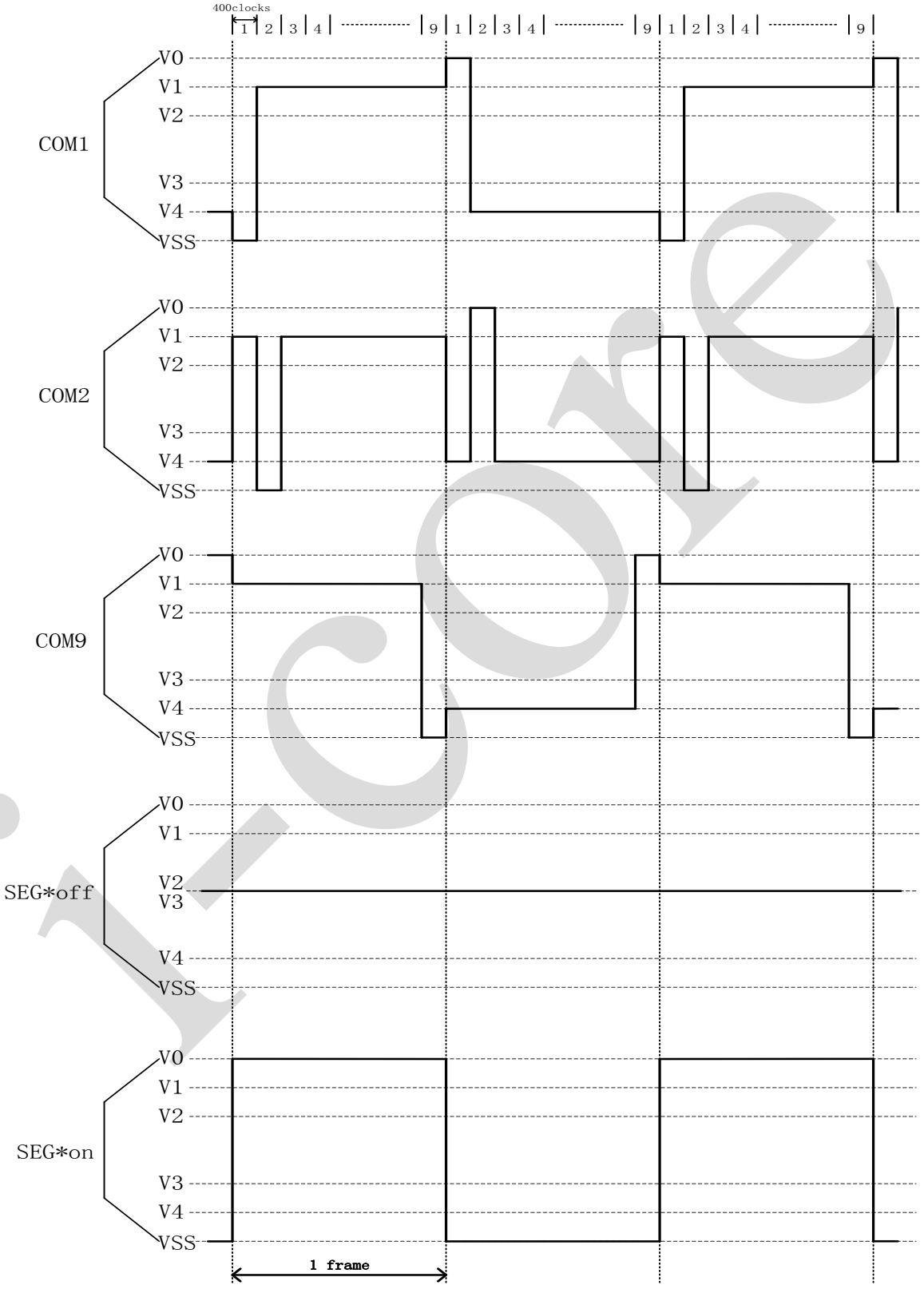
4.2.3、1/8 Duty(Normal mode)

Assume the oscillation frequency is 540kHz, 1 clock cycle time = 1.85us, 1/8 duty, 1/4 bias, 1 frame = 1.85us ×400 ×8 = 5.92ms =168.9Hz (SHLC and SHLS connect to High).



4.2.4、1/9 Duty(Extension mode)

Assume the oscillation frequency is 540kHz, 1 clock cycle time = 1.85us, 1/9 duty, 1/4 bias, 1 frame = 1.85us ×400 ×9 = 6.66ms =150Hz (SHLC and SHLS connect to High).



5、Function Description

5.1、System Interface

This chip has all four kinds of interface type with MPU: 4-bit bus, 8-bit bus, serial and fast I^2C interface. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR); the other is instruction register (IR).

The data register (DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM/ICON RAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

Using RS input pin to select command or data in 4-bit/8-bit bus mode.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
L	H	Read Busy Flag(DB7) and address counter (DB0 ~ DB6)
H	L	Data Write operation (MPU writes data into DR)
H	H	Data Read operation (MPU reads data from DR)

5.2、I^2C interface

It just only could write Data or Instruction to AiP31032 by the IIC Interface.

It could not read Data or Instruction from AiP31032 (except Acknowledge signal).

SCL: serial clock input

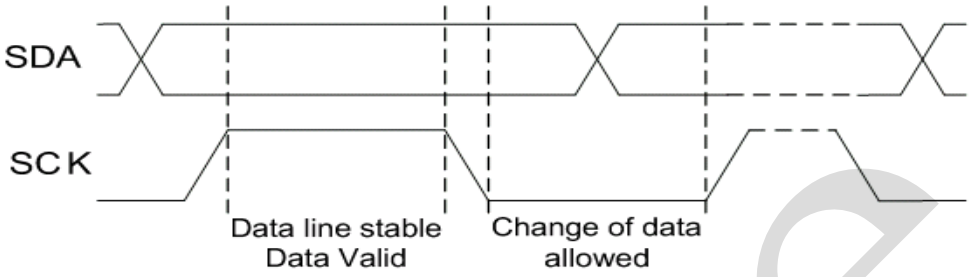
SDA: serial data input

Slaver address could only set to 0111110, no other slaver address could be set.

The I^2C interface send RAM data and executes the commands sent via the I^2C Interface. It could send data bit to the RAM. The I^2C Interface is two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

5.3、Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal.



5.4、Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in following figure.

5.5、System Configuration

[1] The system configuration is illustrated in following figure. Transmitter: the device, which sends the data to the bus.

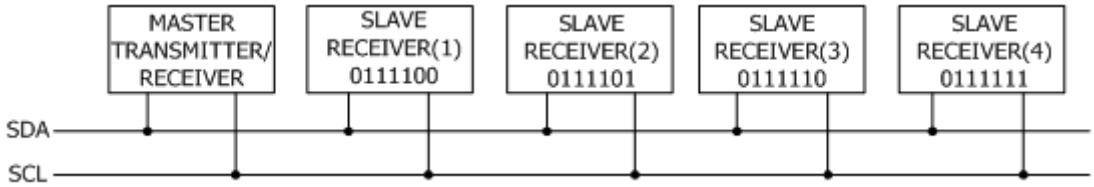
[2] Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.

[3] Slave: the device addressed by a master.

[4] Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.

[5] Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

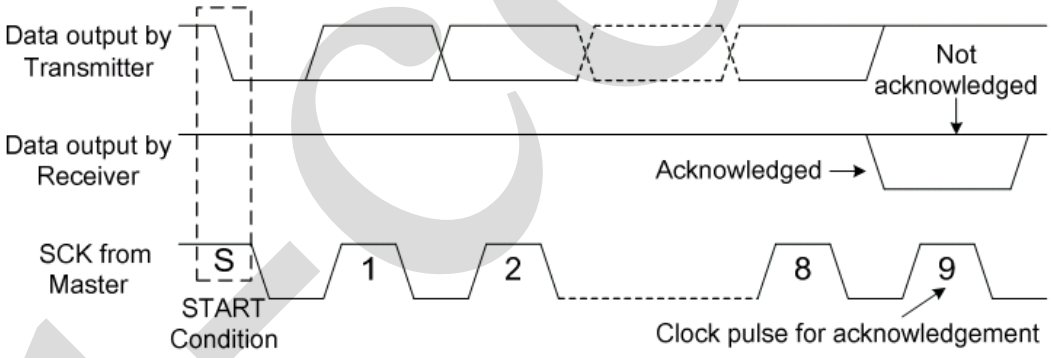
[6] Synchronization: procedure to synchronize the clock signals of two or more devices.



5.6、Acknowledge

Acknowledge is not Busy Flag in I²C interface.

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

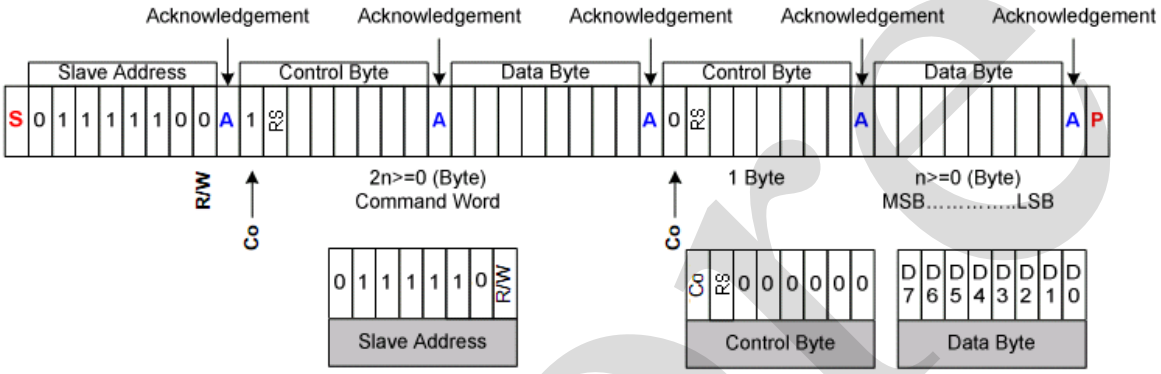


5.7、I²C Interface protocol

The AiP31032 supports command, data write addressed slaves on the bus. Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Only one 7-bit slave addresses (0111110) is reserved for the AiP31032. The R/W is assigned to 0 for Write only.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and RS, plus a data byte. The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the RS bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on

the bus also acknowledge the control and data bytes. After the last control byte, depending on the RS bit setting; either a series of display data bytes or command data bytes may follow. If the RS bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended AiP31032 device. If the RS bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I^2C INTERFACE-bus master issues a STOP condition (P).



Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received

During write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register (IR).

The data register (DR) is used as temporary data storage place for being written into DDRAM/CGRAM/ICON RAM, target RAM is selected by RAM address setting instruction. Each internal operation, writing into RAM, is done automatically. So to speak, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/ICON RAM automatically.

The Instruction register (IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input in I^2C interface.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
H	L	Data Write operation (MPU writes data into DR)

5.8、Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

5.9、Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM/ICON RAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM/ICON RAM, AC is automatically increased (decreased) by 1. When RS = “Low” and R/W = “High”, AC can be read through DB0 ~ DB6 ports.

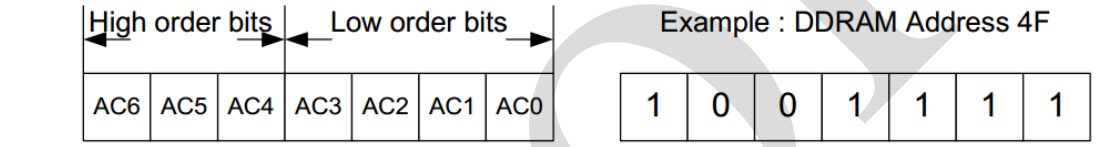
5.10、Display Data RAM (DDRAM)

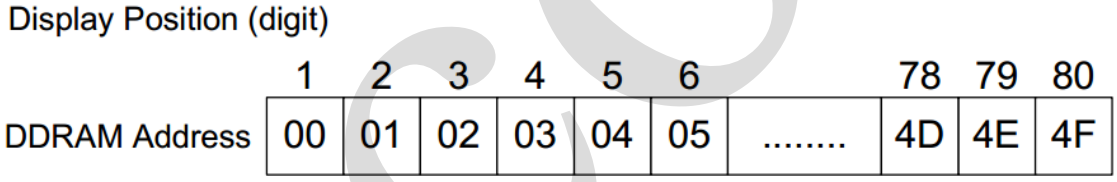
Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 × 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 7 for the relationships between DDRAM addresses and positions on the liquid crystal display.

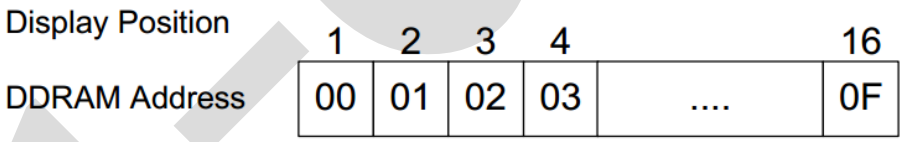
The DDRAM address (ADD) is set in the address counter (AC) as hexadecimal.

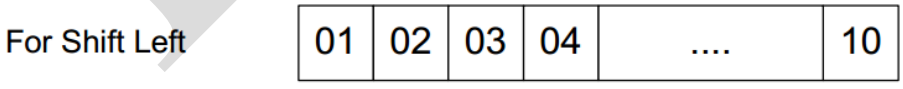
5.10.1、1-line display (N = 0)

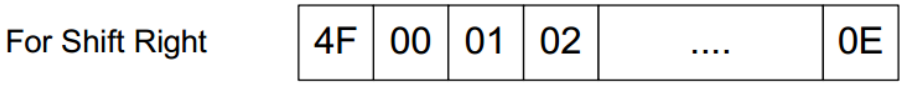
When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the AiP31032, 16 characters are displayed. When the display shift operation is performed, the DDRAM address shifts.











5.10.2、2-line display (N=1)

Case 1: When the number of display characters is less than 40*2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive.

Display Position

	1	2	3	4	5	6		38	39	40
DDRAM Address (hexadecimal)	00	01	02	03	04	05	.....	25	26	27
	40	41	42	43	44	45	.....	65	66	67

Case 2: For a 16-character.2-line display. When display shift operation is performed, the DDRAM address shifts.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
For Shift Left	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
For Shift Right	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

5.11、Character Generator ROM (CGROM)

The character generator ROM generates 5×8 dot character patterns from 8-bit character codes. It can generate 240/250/248/256 5×8 dot character patterns (select by OPR1/2 ITO pin). User-defined character patterns are also available by mask-programmed ROM.

5.12、Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 5×8 dots, eight character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of code table (refer to appendix) to show the character patterns stored in CGRAM.

See Table 4 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

5.13、ICON RAM

In the ICON RAM, the user can rewrite icon pattern by program. There are totally 80 dots for icon can be written. See ICON RAM map，for the relationship between ICON RAM address and data and the display patterns.

5.14、Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area. (In I^2C interface the reading function is invalid.)

5.15、LCD Driver Circuit

LCD Driver circuit has 17 common and 80 segment signals for LCD driving. Data from CGRAM/CGROM/ICON is transferred to 80 bit segment latch serially, and then it is stored to 80 bit shift latch. When each common is selected by 17 bit common register, segment data also output through segment driver from 80 bit segment latch.

5.16、Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Character Code (DDRAM data)									CGRAM address							CGRAM Data							
D7	D6	D5	D4	D3	D2	D1	D0		A5	A4	A3	A2	A1	A0		P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	×	0	0	0		0	0	0	0	0	0		×	×	×	0	1	1	1	0
												0	0	1					0	0	1	0	0
												0	1	0					0	0	1	0	0
												0	1	1					0	0	1	0	0
												1	0	0					0	0	1	0	0
												1	0	1					0	0	1	0	0
												1	1	0					0	1	1	1	0
												1	1	1					0	0	0	0	0
0	0	0	0	×	0	0	1		0	0	1	0	0	0		×	×	×	0	1	1	1	0
												0	0	1					1	0	0	0	1
												0	1	0					1	0	0	0	0
												0	1	1					1	0	0	0	0
												1	0	0					1	0	0	0	0
												1	0	1					1	0	0	0	1
												1	1	0					0	1	1	1	0
												1	1	1					0	0	0	0	0
				*							*							*					
				*							*							*					
				*							*							*					
				*							*							*					
0	0	0	0	×	1	1	1		1	1	1	0	0	0		×	×	×	1	1	1	1	1
												0	0	1					1	0	0	0	0
												0	1	0					1	0	0	0	0
												0	1	1					1	1	1	1	0
												1	0	0					1	0	0	0	0
												1	0	1					1	0	0	0	0
												1	1	0					1	1	1	1	1
												1	1	1					0	0	0	0	0

When SHLS=1, ICON RAM map refer below table

ICON address	ICON RAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S1	S2	S3	S4	S5
01H	-	-	-	S6	S7	S8	S9	S10
02H	-	-	-	S11	S12	S13	S14	S15
03H	-	-	-	S16	S17	S18	S19	S20
04H	-	-	-	S21	S22	S23	S24	S25
05H	-	-	-	S26	S27	S28	S29	S30
06H	-	-	-	S31	S32	S33	S34	S35
07H	-	-	-	S36	S37	S38	S39	S40
08H	-	-	-	S41	S42	S43	S44	S45
09H	-	-	-	S46	S47	S48	S49	S50
0AH	-	-	-	S51	S52	S53	S54	S55
0BH	-	-	-	S56	S57	S58	S59	S60
0CH	-	-	-	S61	S62	S63	S64	S65
0DH	-	-	-	S66	S67	S68	S69	S70
0EH	-	-	-	S71	S72	S73	S74	S75
0FH	-	-	-	S76	S77	S78	S79	S80

When SHLS=0, ICON RAM map refer below table

ICON address	ICON RAM bits							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	-	-	S80	S79	S78	S77	S76
01H	-	-	-	S75	S74	S73	S72	S71
02H	-	-	-	S70	S69	S68	S67	S66
03H	-	-	-	S65	S64	S63	S62	S61
04H	-	-	-	S60	S59	S58	S57	S56
05H	-	-	-	S55	S54	S53	S52	S51
06H	-	-	-	S50	S49	S48	S47	S46
07H	-	-	-	S45	S44	S43	S42	S41
08H	-	-	-	S40	S39	S38	S37	S36
09H	-	-	-	S35	S34	S33	S32	S31
0AH	-	-	-	S30	S29	S28	S27	S26
0BH	-	-	-	S25	S24	S23	S22	S21
0CH	-	-	-	S20	S19	S18	S17	S16
0DH	-	-	-	S15	S14	S13	S12	S11
0EH	-	-	-	S10	S9	S8	S7	S6
0FH	-	-	-	S5	S4	S3	S2	S1

5.17、Instructions

Instruction table at “Normal mode”

(When “EXT” option pin connect to VDD, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0		380 kHz	540 kHz	700 kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	×	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1: entire display on C=1: cursor on B=1: cursor position on	26.3 us	18.5 us	14.3 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	×	×	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	×	×	×	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us

Be sure the AiP31032 is not in the busy state (BF = 0) before sending an instruction from the MPU to the AiP31032. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

5.17.2、Instruction table at "Extension mode"

(When "EXT" option pin connect to GND, the instruction set follow below table)

Instruction	Instruction Code										Description	Instruction Execution Time		
	RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0		380 kHz	540 kHz	700 kHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	×	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM(DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM(DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note:* this bit is for test command, and must always set to "0".

Instruction table 0(IS=0)													
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	×	×	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us
Instruction table 1(IS=1)													
Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC 3	AC 2	AC 1	AC 0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/ contrast set	0	0	0	1	0	1	I_{ON}	B_{ON}	C5	C4	Ion: ICON display on/off B_{ON}: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	F_{ON}	Rab 2	Rab 1	Rab 0	F_{ON}: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us

5.18、Instruction Description

5.18.1、Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = “1”).

5.18.2、Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

5.18.3、Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

Increment / decrement of DDRAM address (cursor or blink)

When I/D = “High”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D = “Low”, cursor/blink moves to left and DDRAM address is decreased by 1.

CGRAM operates the same as DDRAM, when read from or write to CGRAM.

S: Shift of entire display

When DDRAM read (CGRAM read/write) operation or S = “Low”, shift of entire display is not performed. If S = “High” and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = “1”: shift left, I/D = “0”: shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

5.18.4、Display ON/OFF

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D = “High”, entire display is turned on.

When D = “Low”, display is turned off, but display data is remained in DDRAM.

C: Cursor ON/OFF control bit

When C = “High”, cursor is turned on.

When C = “Low”, cursor is disappeared in current display, but I/D register remains its data.

B: Cursor Blink ON/OFF control bit

When B = “High”, cursor blink is on, that performs alternate between all the high data and display character at the cursor position.

When B = “Low”, blink is off.

5.18.5、Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

S/C: Screen/Cursor select bit

When S/C=“High”, Screen is controlled by R/L bit.

When S/C=“Low”, Cursor is controlled by R/L bit.

R/L: Right/Left

When R/L=“High”, set direction to right.

When R/L=“Low”, set direction to left.

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

5.18.6、Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	DH	0	IS

DL: Interface data length control bit

When DL = “High”, it means 8-bit bus mode with MPU.

When DL = “Low”, it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.

When in 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit

When N = “High”, 2-line display mode is set.

When N = “Low”, it means 1-line display mode.

DH: Double height font type control bit

When DH = “High” and N= “Low”, display font is selected to double height mode (5×16 dot), RAM address can only use 00H~27H.

When DH= “High” and N= “High”, it is forbidden.

When DH = “Low”, display font is normal (5×8 dot).

N	DH	EXT option pin connect to high		EXT option pin connect to low	
		Display Lines	Character Font	Display Lines	Character Font
L	L	1	5×8	1	5×8
L	H	1	5×8	1	5×16
H	L	2	5×8	2	5×8
H	H	2	5×8	Forbidden	

IS: Normal/Extension instruction select

When IS=“High”, extension instruction be selected (refer extension instruction table)

When IS=“Low”, normal instruction be selected (refer normal instruction table)

5.18.7、Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

5.18.8、Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction makes DDRAM data available from MPU. When 1-line display mode (N=0), DDRAM address is from “00H” to “4FH”. In 2-line display mode (N=1), DDRAM address in the 1st line is from “00H” to “27H”, and DDRAM address in the 2nd line is from “40H” to “67H”.

5.18.9、Read Busy Flag and Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

When BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

5.18.10、Write Data to CGRAM,DDRAM or ICON RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to CGRAM, DDRAM or ICON RAM The selection of RAM from DDRAM, CGRAM or ICON RAM, is set by the previous address set instruction: DDRAM address set, CGRAM address set, ICON RAM address set. RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

5.18.11、Read Data from CGRAM,DDRAM or ICON RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/ICON RAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. (Read data must be “set address” before this instruction).

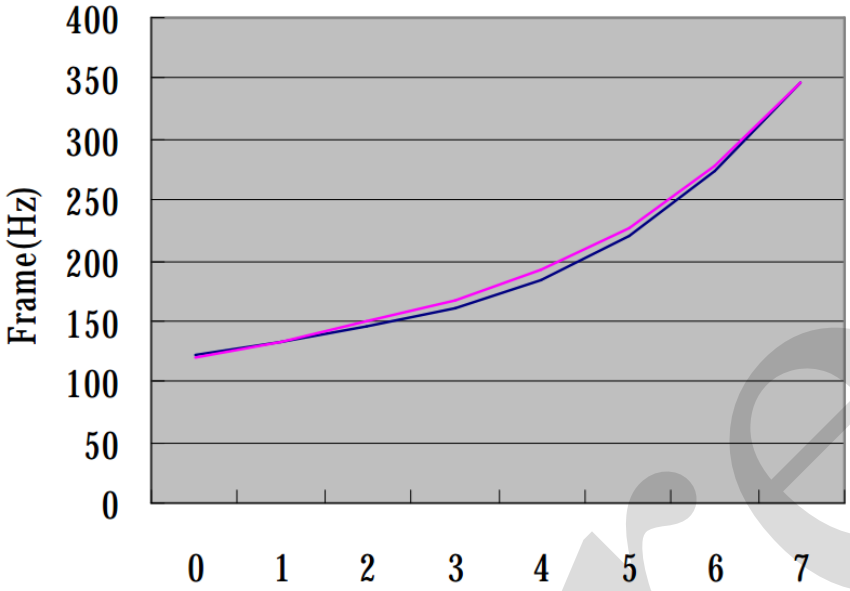
5.18.12、Bias selection/Internal OSC frequency adjust

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	BS	F2	F1	F0

BS: bias selection
When BS=”High”, the bias will be 1/4
When BS=”Low”, the bias will be 1/5
BS will be invalid when external bias resistors are used (OPF1=1, OPF2=1).

F2, F1, F0: Internal OSC frequency adjust
When CLS connect to high, that instruction can adjust OSC and Frame frequency.

Internal frequency adjust			Frame frequency (Hz) (2 line mode)	
F2	F1	F0	VDD=3V	VDD=5V
0	0	0	122	120
0	0	1	131	133
0	1	0	144	149
0	1	1	161	167
1	0	0	183	192
1	0	1	221	227
1	1	0	274	277
1	1	1	347	347



5.18.13、Set ICON RAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	AC3	AC2	AC1	AC0

This instruction makes ICON data available from MPU. When IS=1 at Extension mode, The ICON RAM address is from “00H” to “0FH”.

5.18.14、Power/ICON control/Contrast set(high byte)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	I_{ON}	B_{ON}	C5	C4

I_{ON}: Set ICON display on/off
When Ion = “High”, ICON display on.
When Ion = “Low”, ICON display off.

B_{ON}: switch booster circuit
B_{ON} can only be set when internal follower is used (OPF1=0, OPF2=0).
When B_{ON} = “High”, booster circuit is turn on.
When B_{ON} = “Low”, booster circuit is turn off.

C5, C4: Contrast set (high byte)
C5, C4, C3, C2, C1, C0 can only be set when internal follower is used (OPF1=0, OPF2=0). They can more precisely adjust the input reference voltage of V0 generator. The details please refer to the supply voltage for LCD driver.

5.18.15、Follower control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	F_{ON}	Rab2	Rab1	Rab0

F_{ON}: Switch follower circuit

F_{ON} can only be set when internal follower is used (OPF1=0, OPF2=0).

When F_{ON} = “High”, internal follower circuit is turn on.

When F_{ON} = “Low”, internal follower circuit is turn off.

Rab2, Rab1, Rab0: V0 generator amplified ratio

Rab2, Rab1, Rab0 can only be set when internal follower is used (OPF1=0, OPF2=0). They can adjust the amplified ratio of V0 generator. The details please refer to the supply voltage for LCD driver.

5.18.16、Contrast set(low byte)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	C3	C2	C1	C0

C3, C2, C1, C0: Contrast set (low byte)

C5, C4, C3, C2, C1, C0 can only be set when internal follower is used (OPF1=0, OPF2=0). They can more precisely adjust the input reference voltage of V0 generator. The details please refer to the supply voltage for LCD driver.

5.19、Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the AiP31032 when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state (BF = 1) until the initialization ends. The busy state lasts for 40 ms after VDD rises to stable.

[1] Display clear

[2] Function set:

DL=1; 8-bit interface data

N=0; 1-line display

DH=0; normal 5×8 font

IS=0; use instruction table 0

[3] Display on/off control:

D=0; Display off

C=0; Cursor off

B=0; Blinking off

[4] Entry mode set:

I/D=1; Increment by 1

S=0; No shift

[5] Internal OSC frequency

(F2, F1, F0) = (1, 0, 0)

[6] ICON control

I_{ON}=0; ICON off

[7] Power control

BS=0; 1/5bias

B_{ON}=0; booster off

F_{ON}=0; follower off

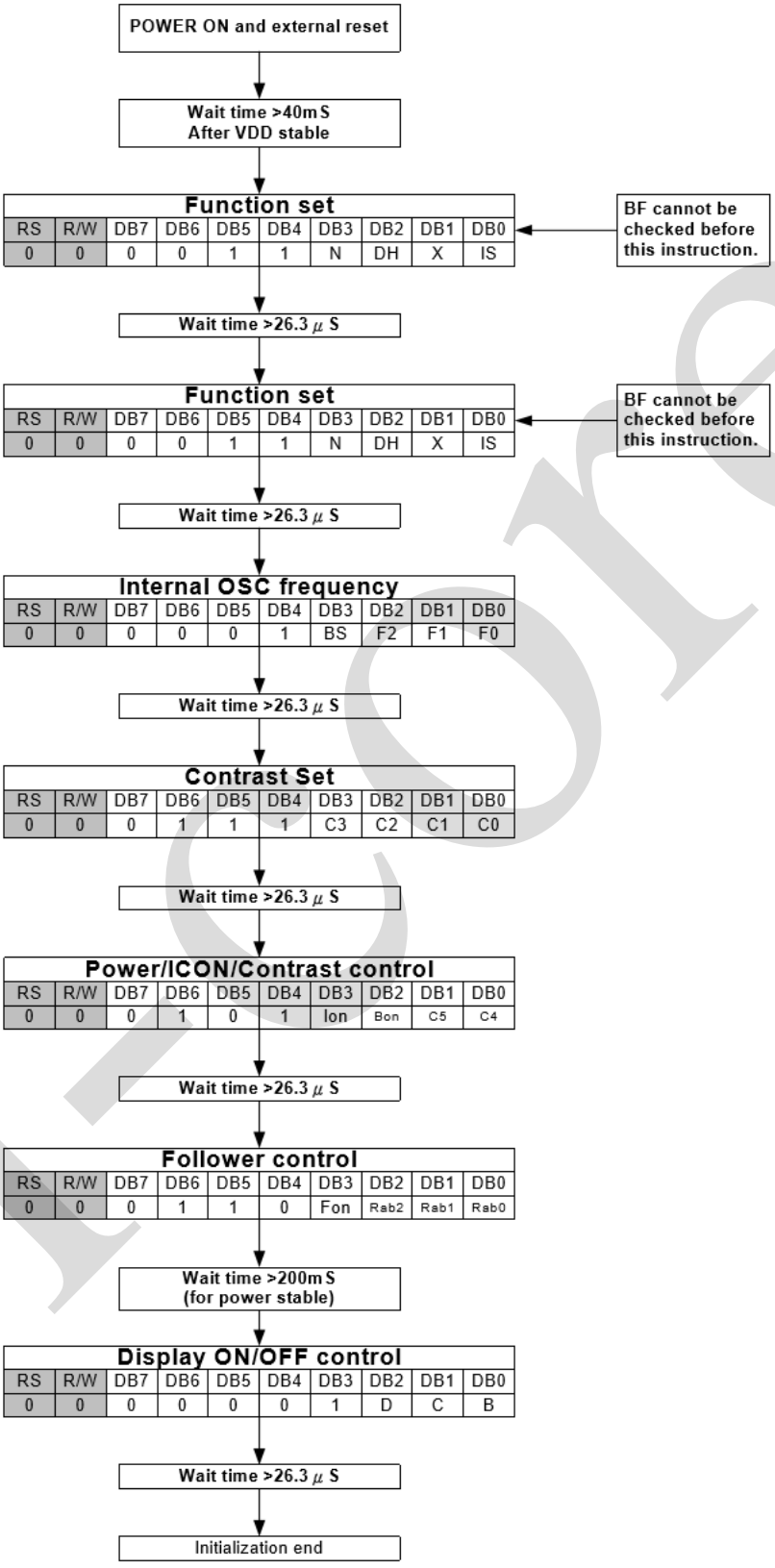
(C5, C4, C3, C2, C1, C0) = (1, 0, 0, 0, 0, 0)

(Rab2, Rab1, Rab0) = (0, 1, 0)

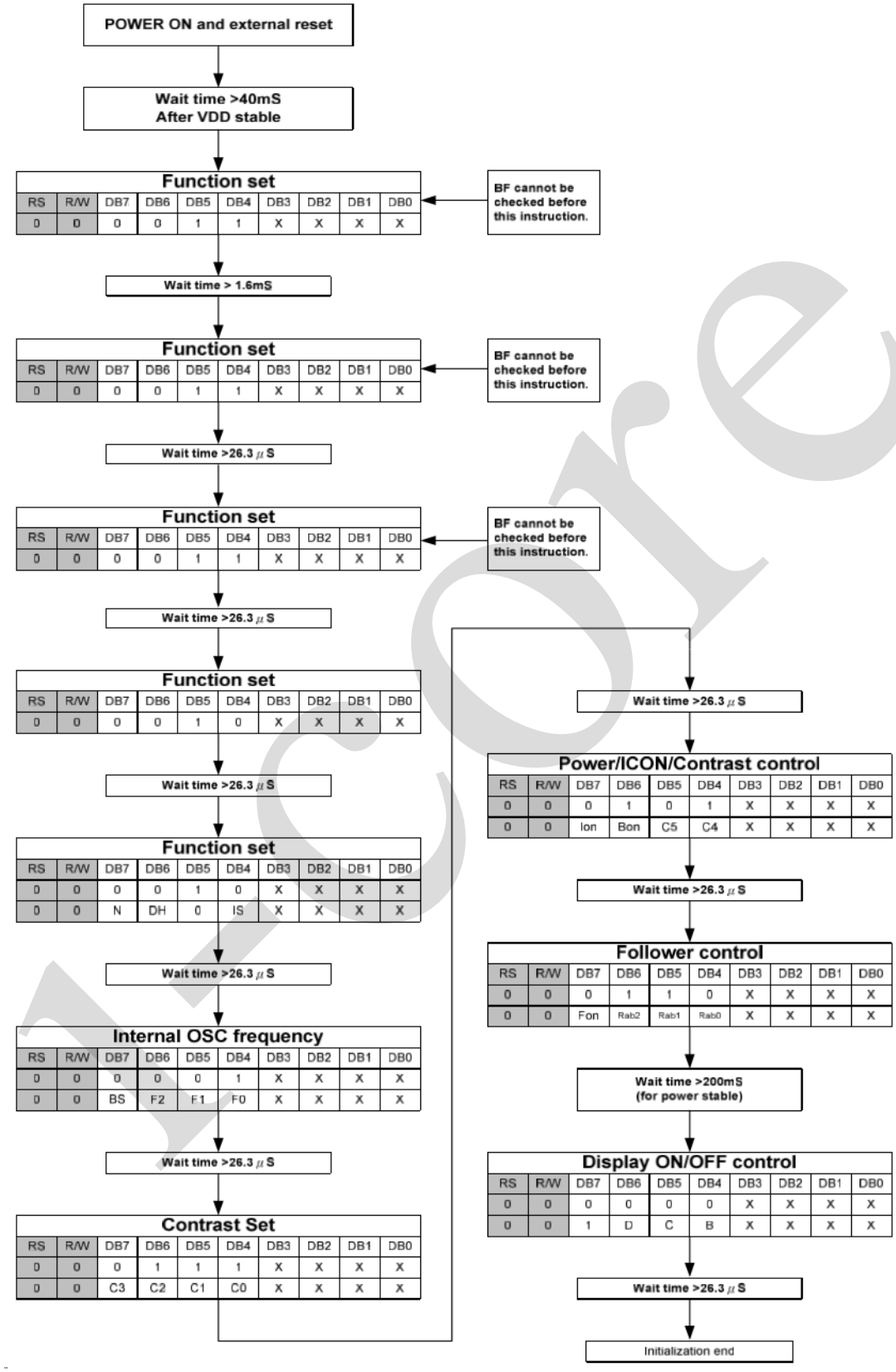
Note: If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the AiP31032. When internal Reset Circuit not operate, AiP31032 can be reset by XRESET pin from MPU control signal.

5.20、Initializing by Instruction

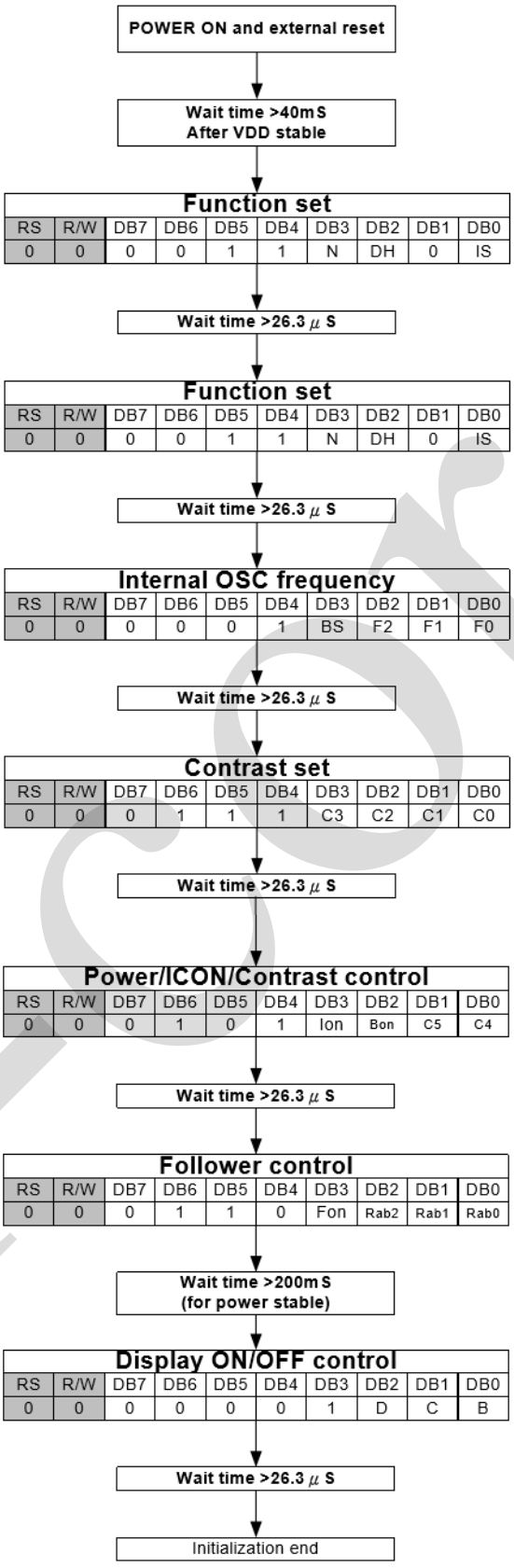
5.20.1、8-bit Interface (fosc=380kHz)



5.20.2、4-bit Interface (fosc=380kHz)



5.20.3、Serial interface & IIC interface (fosc=380kHz)



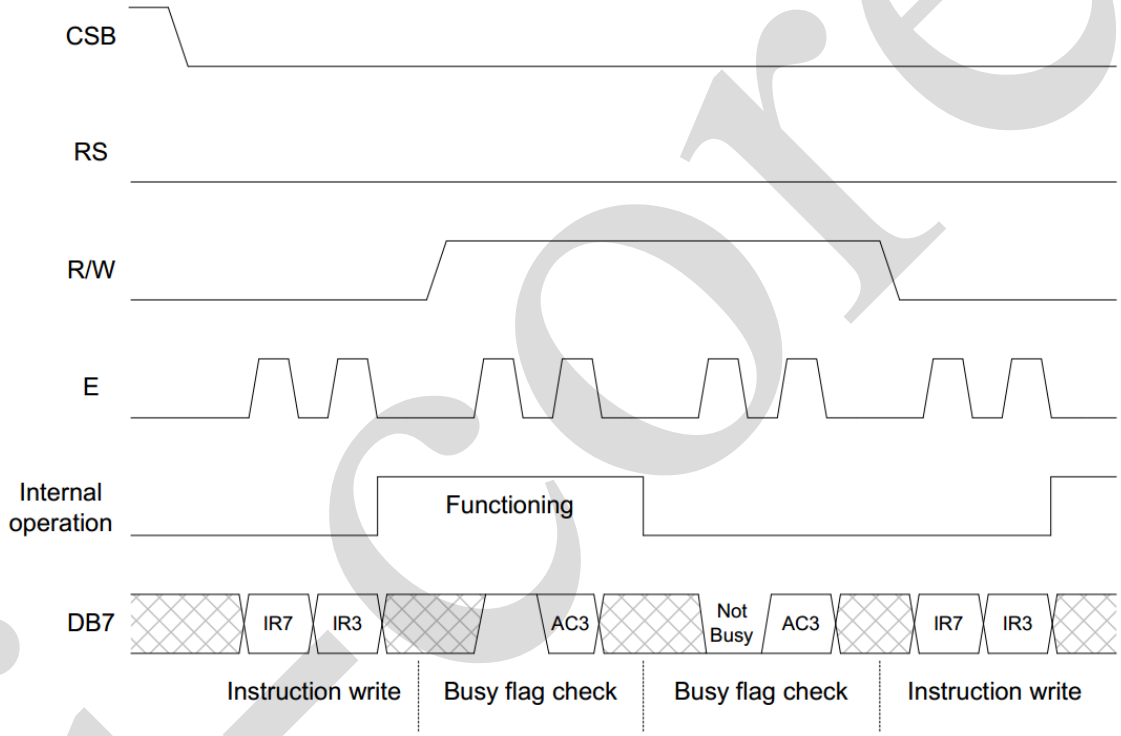
5.21、Interfacing to the MPU

The AiP31032 can send data in two 4-bit operations/one 8-bit operation, serial 1 bit operation or fast I^2C operation, thus allowing interfacing with 4-bit, 8-bit or I^2C MPU.

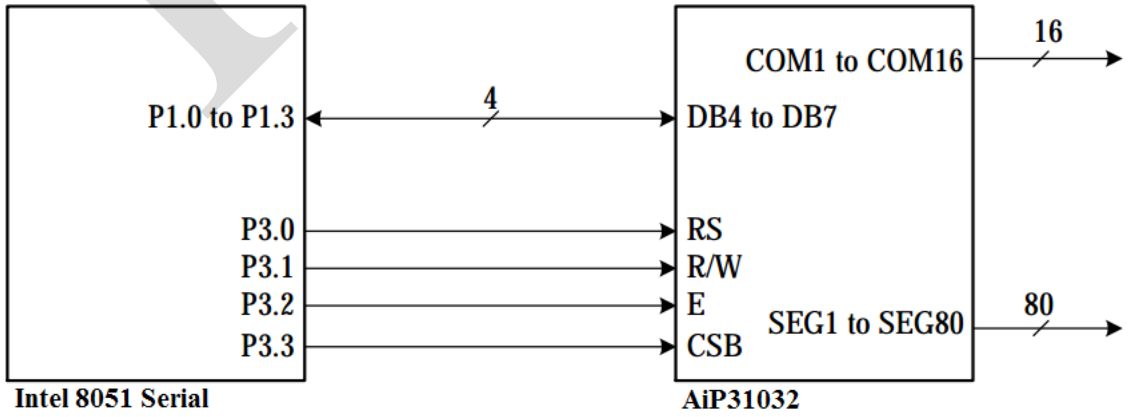
5.21.1、For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.

Bus lines DB0 to DB3 are disabled. The data transfer between the AiP31032 and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

Example of busy flag check timing sequence

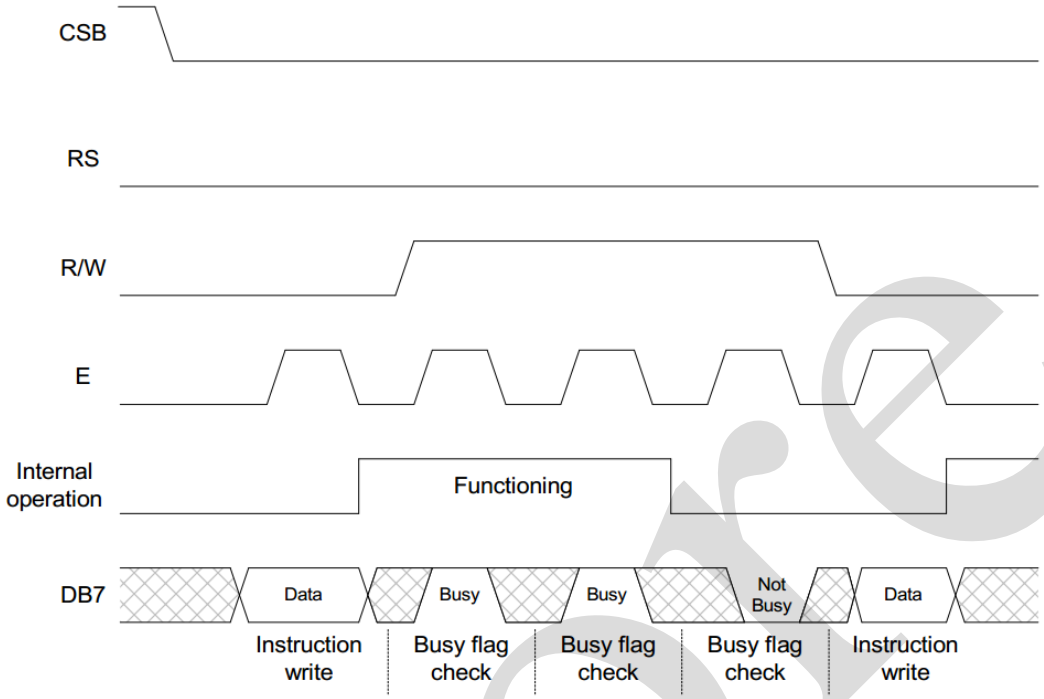


Intel 8051 interface (4 Bit)

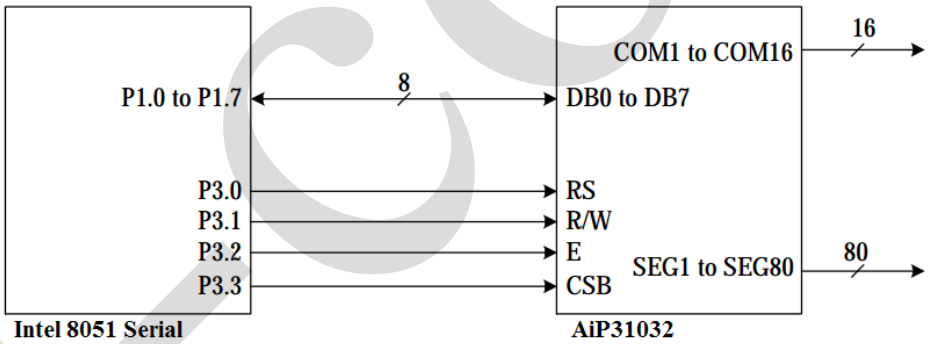


5.21.2、For 8-bit interface data, all eight bus lines (DB0 to DB7) are used

Example of busy flag check timing sequence

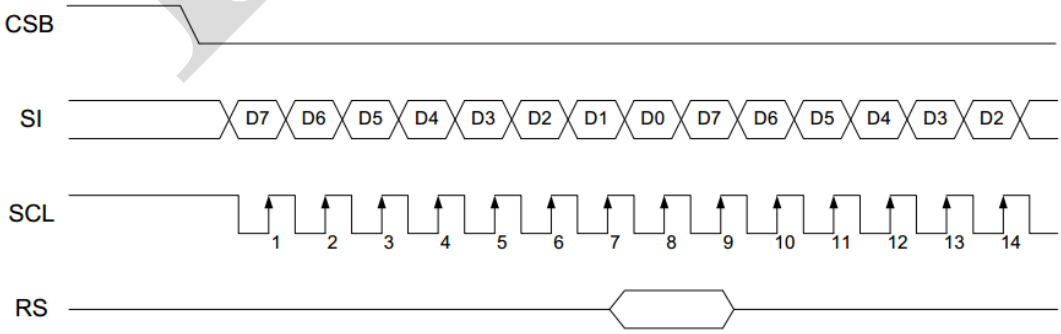


Intel 8051 interface (8 Bit)



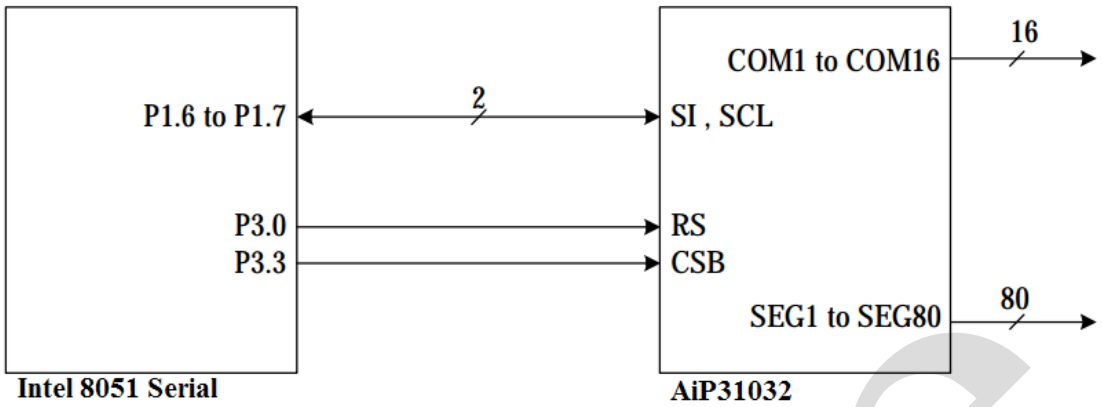
5.21.3、For serial interface data, only two bus lines (DB6 to DB7) are used

Example of timing sequence



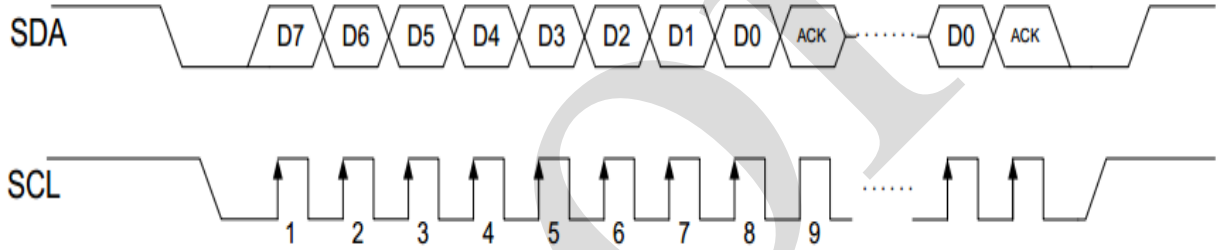
Note: The falling edge must cause on CSB before the serial clock (SCL) active.

Intel 8051 interface (Serial)

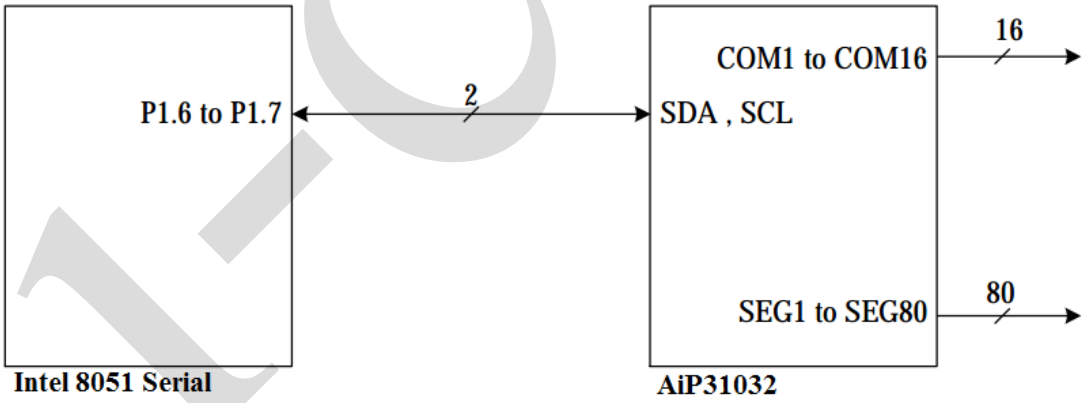


5.21.4、For I²C interface data, only two bus lines (DB6 to DB7) are used

Example of timing sequence

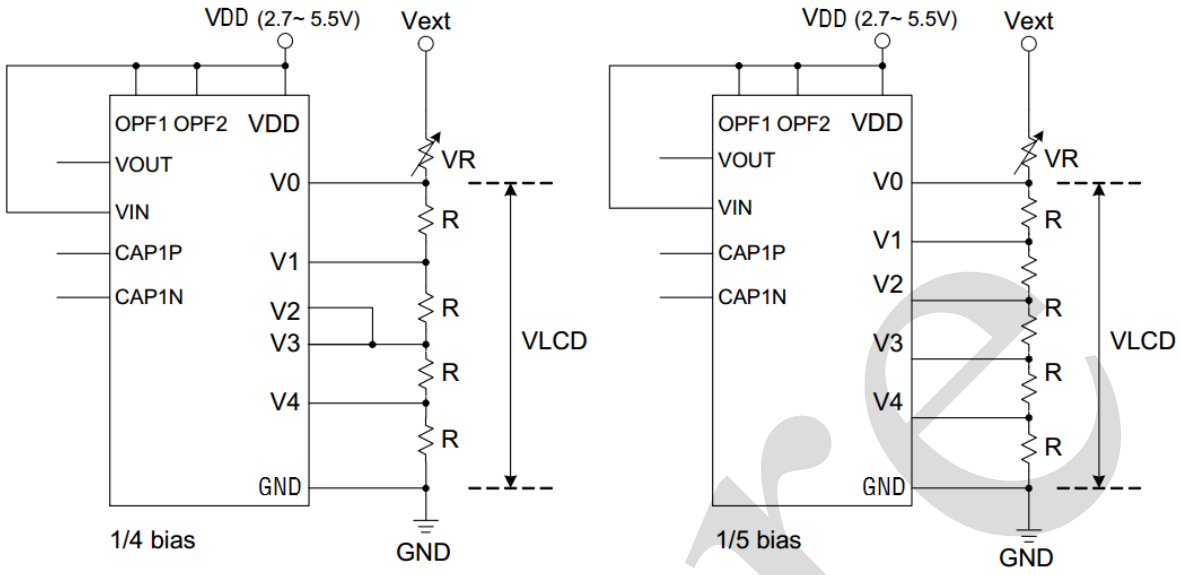


Intel 8051 interface(I²C)

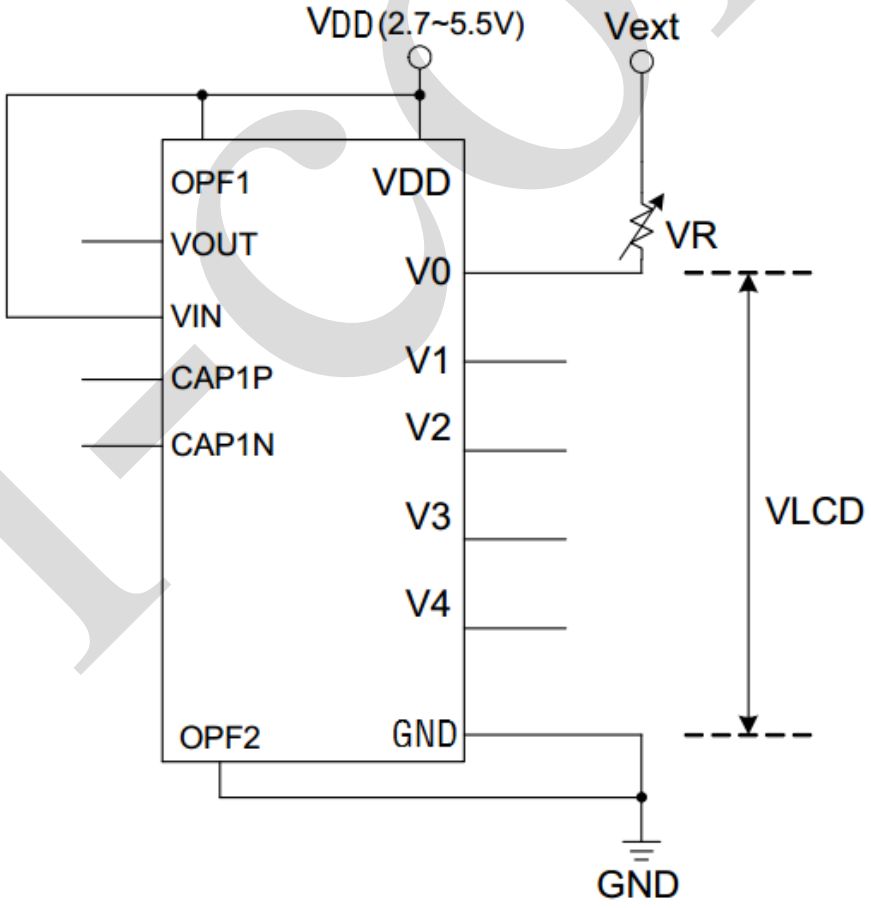


5.22、Supply Voltage for LCD Drive

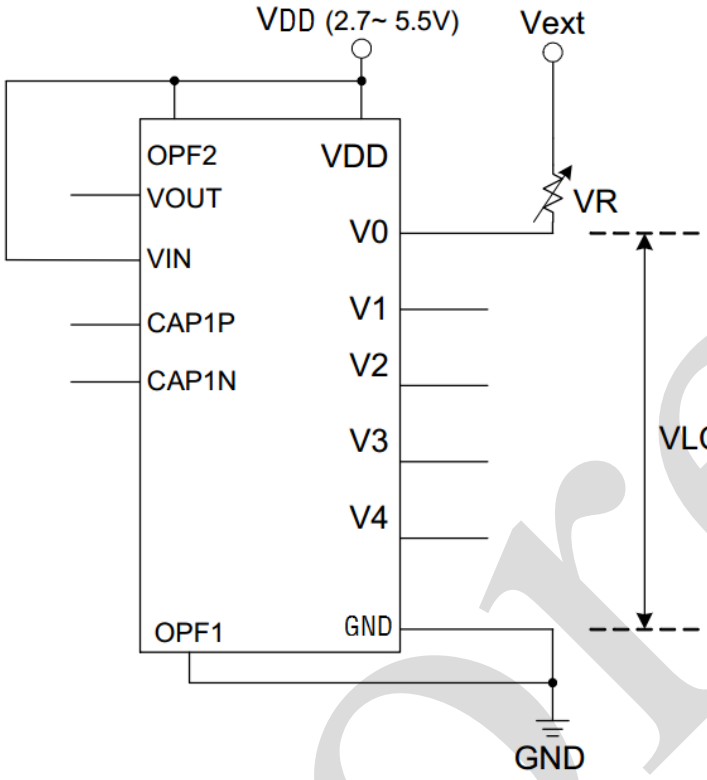
5.22.1、When external bias resistors are used (OPF1=1, OPF2=1)



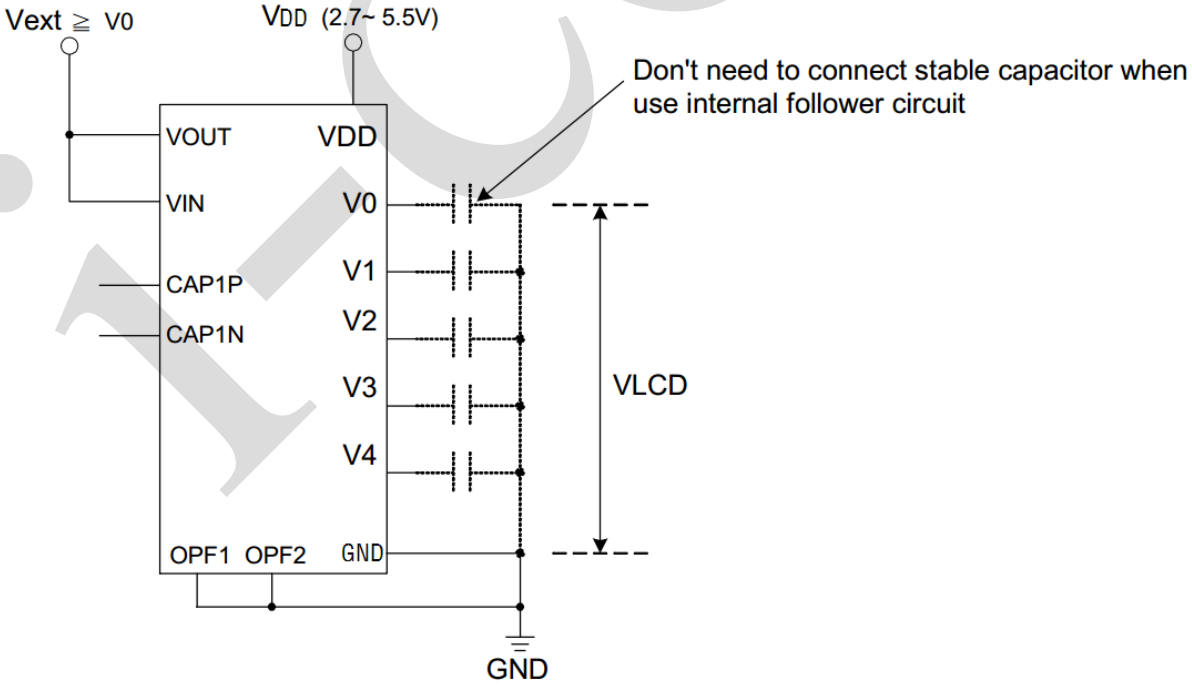
5.22.2、When built-in bias resistors(9.6kΩ) are used (OPF1=1, OPF2=0)



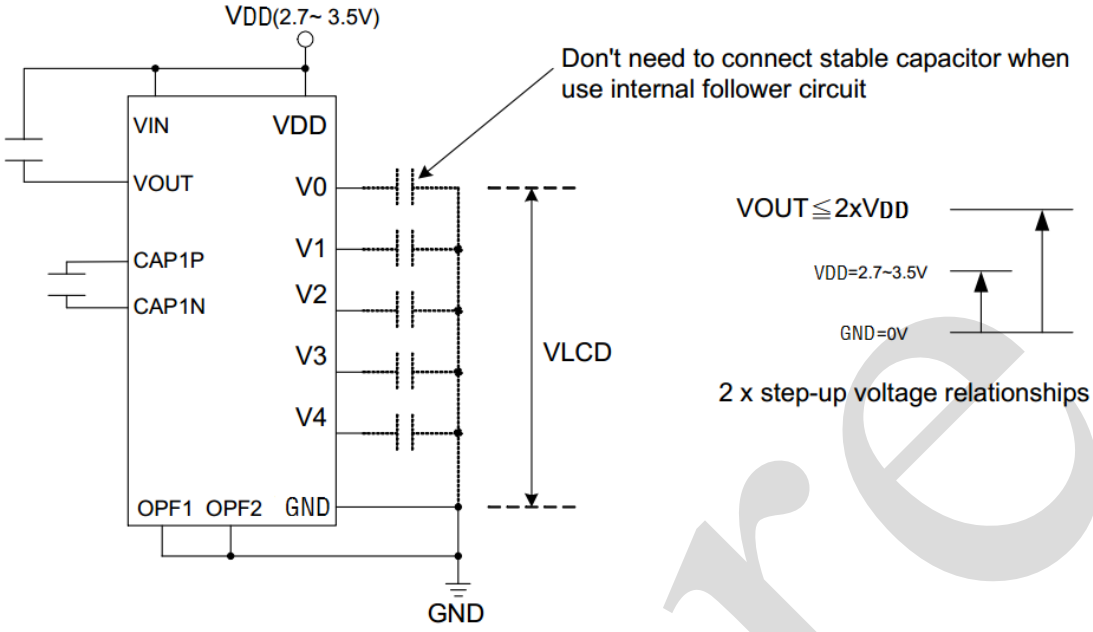
5.22.3、When built-in bias resistors(3.3kΩ) are used (OPF1=0, OPF2=1)



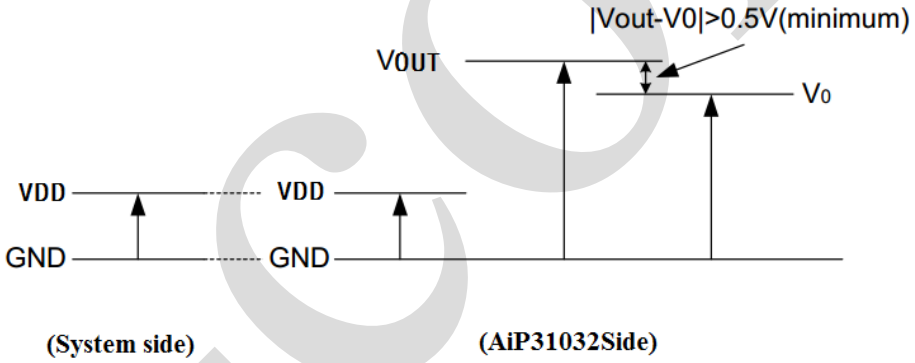
5.22.4、When built-in voltage followers with external VOUT are used (OPF1=0, OPF2=0 and instruction setting B_{ON}=0, F_{ON}=1)



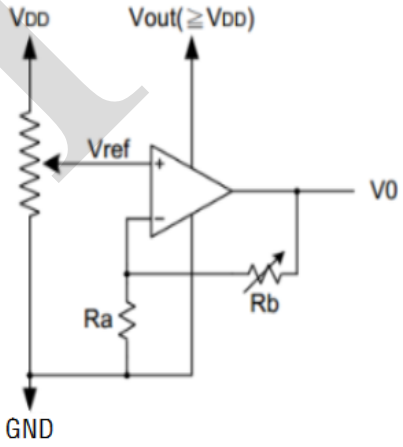
5.22.5、When built-in booster and voltage followers are used (OPF1=0, OPF2=0)



Note: Ensure V0 level stable, that must let |VOUT-V0| over 0.5V (if panel size over 4.5”, the |VOUT-V0| propose over 0.8V).



V0 voltage follower value calculation

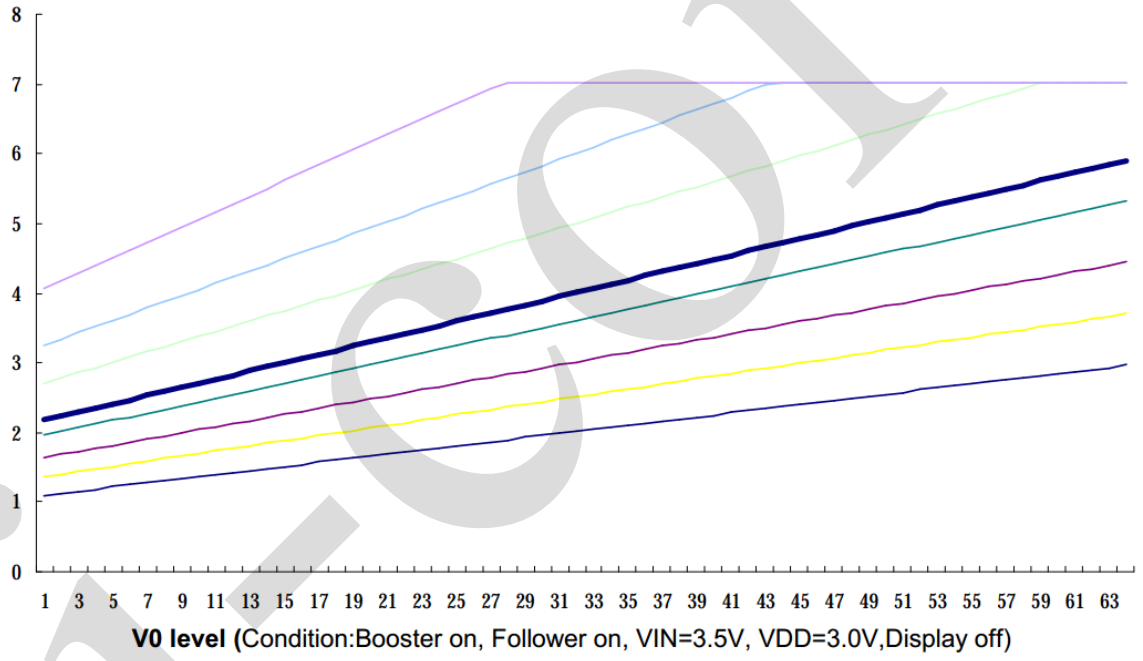


$$V0=(1+\frac{Rb}{Ra})*Vref$$

$$While\ Vref=VDD*(\frac{\alpha+36}{100})$$

C5	C4	C3	C2	C1	C0	α
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			. .			. .
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Rab2	Rab1	Rab0	1+Rb/Ra
0	0	0	1
0	0	1	1.25
0	1	0	1.5
0	1	1	1.8
1	0	0	2
1	0	1	2.5
1	1	0	3
1	1	1	3.75



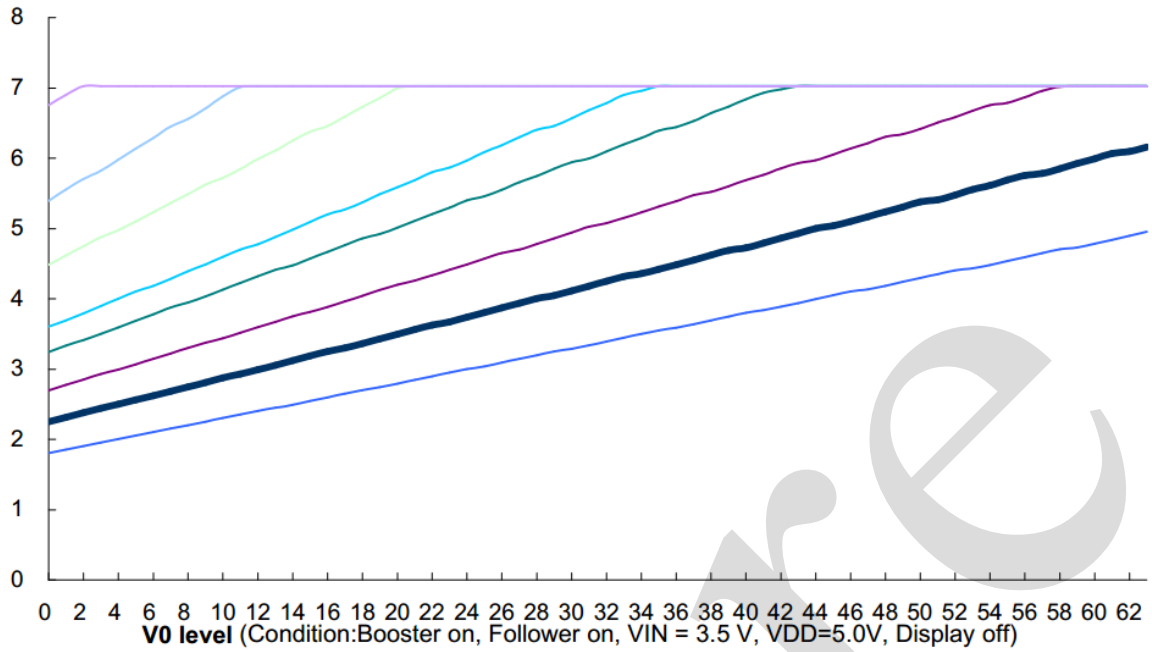
The recommended curve: follower=04H.

Notes:

[1] VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ GND must be maintained.

[2] If the calculation value of V0 is higher than VOUT, the real V0 value will saturate to VOUT.

[3] Internal built-in booster can only be used when OPF1=0, OPF2=0.



The recommended curve: follower=01H.

Notes:

[1] VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ GND must be maintained.

[2] If the calculation value of V0 is higher than VOUT, the real V0 value will saturate to VOUT.

[3] Internal built-in booster can only be used when OPF1=0, OPF2=0.

6、Typical Application Circuit And Application Note

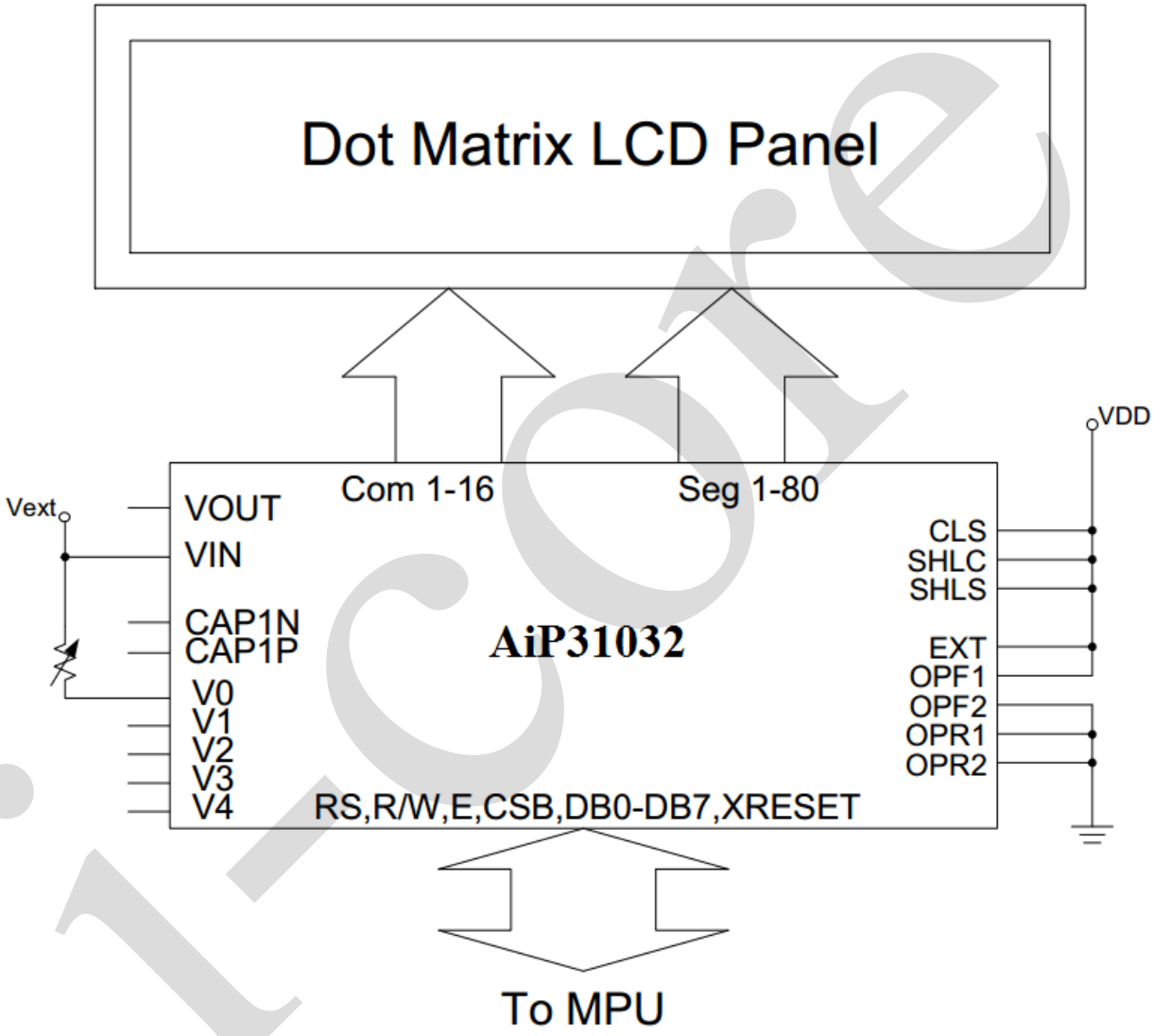
6.1、Application Circuit1（normal mode）

Use internal resistor (9.6kΩ) and contrast adjust with external VR.

Booster always off.

Has 240 character of CGROM and 8 characters of CGRAM.

Internal oscillator.



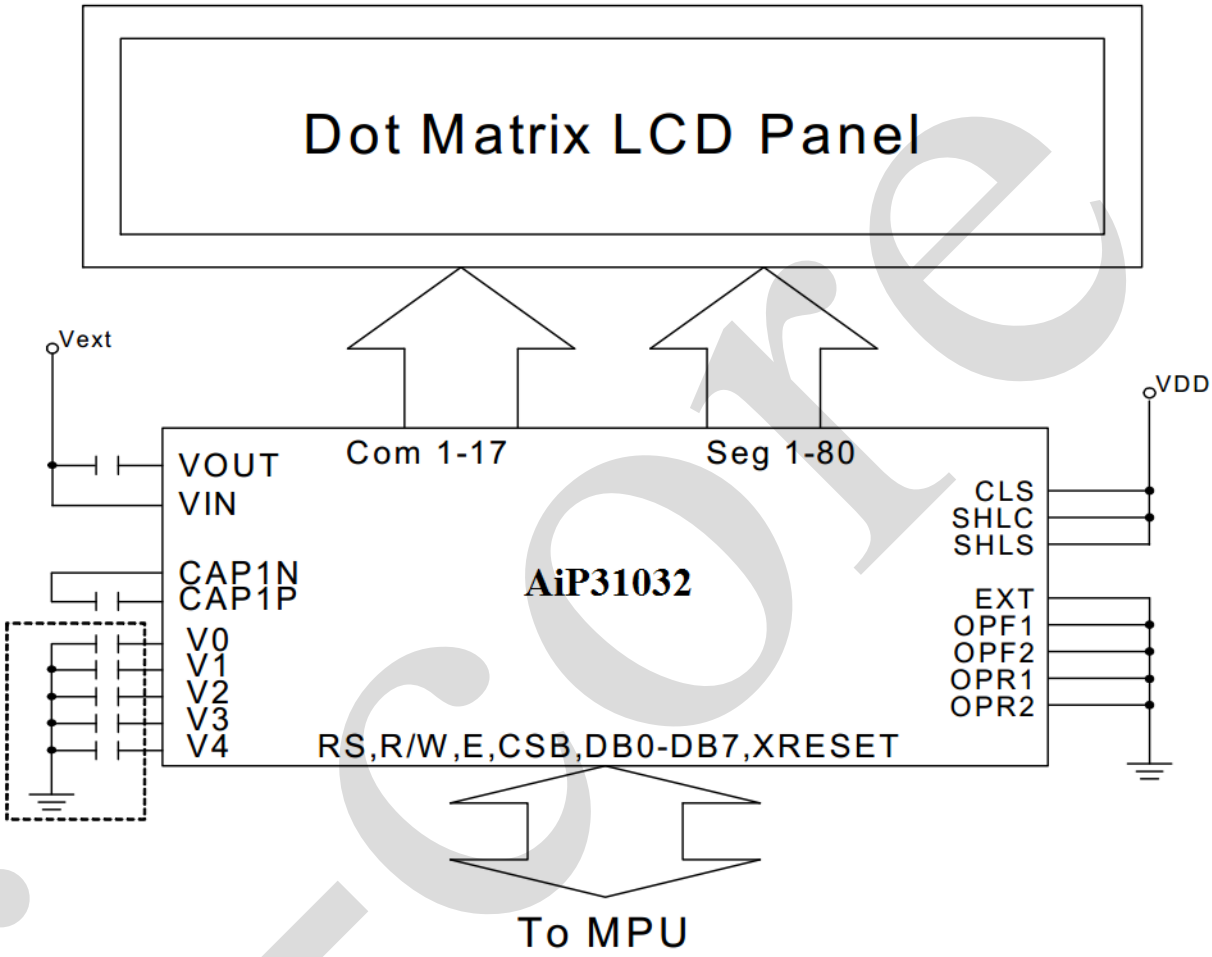
6.2、Application Circuit2（Extension mode）

Use internal follower circuit.

Booster has 2 times pump.

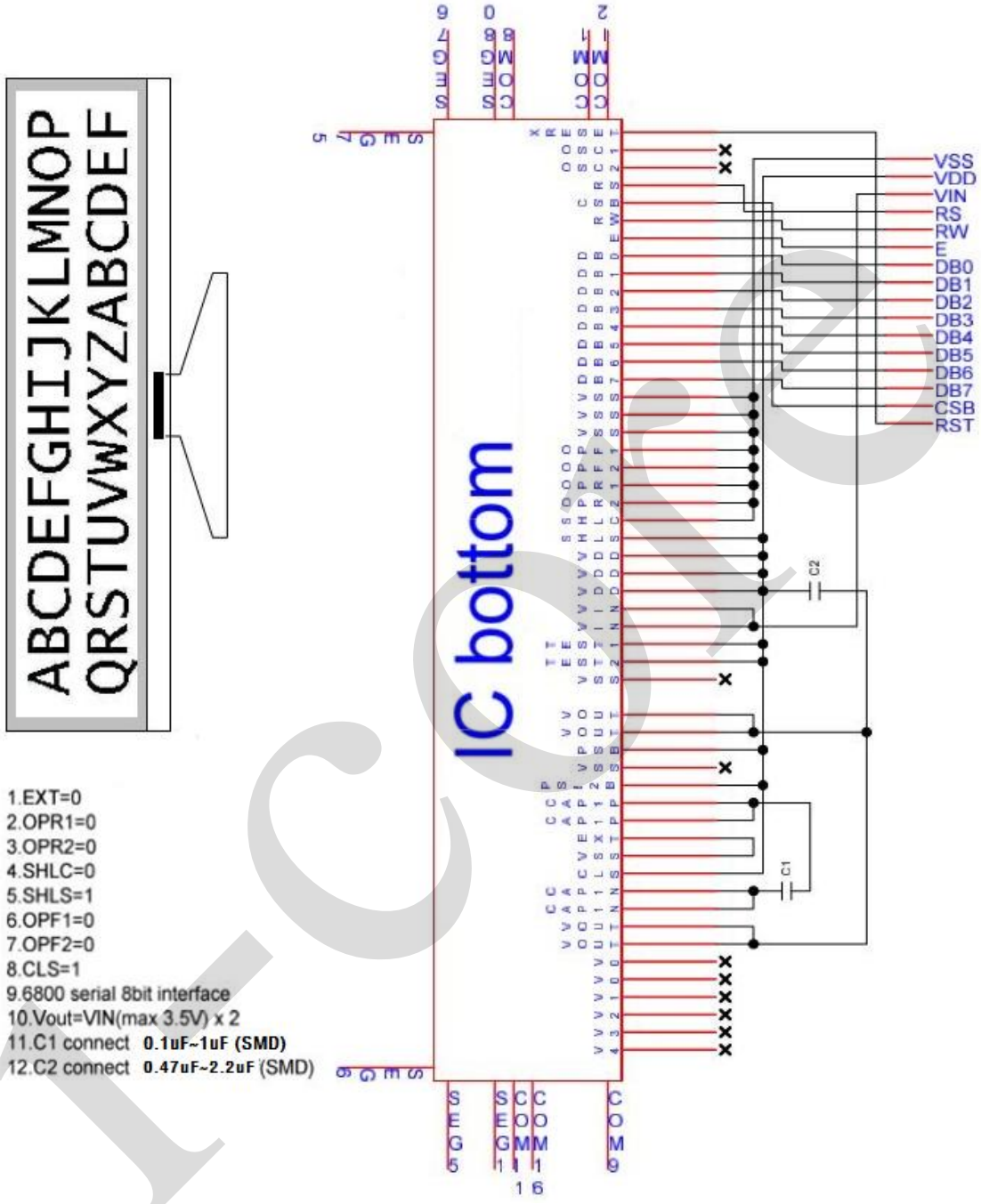
Has 240 character of CGROM and 8 characters of CGRAM.

Internal oscillator.

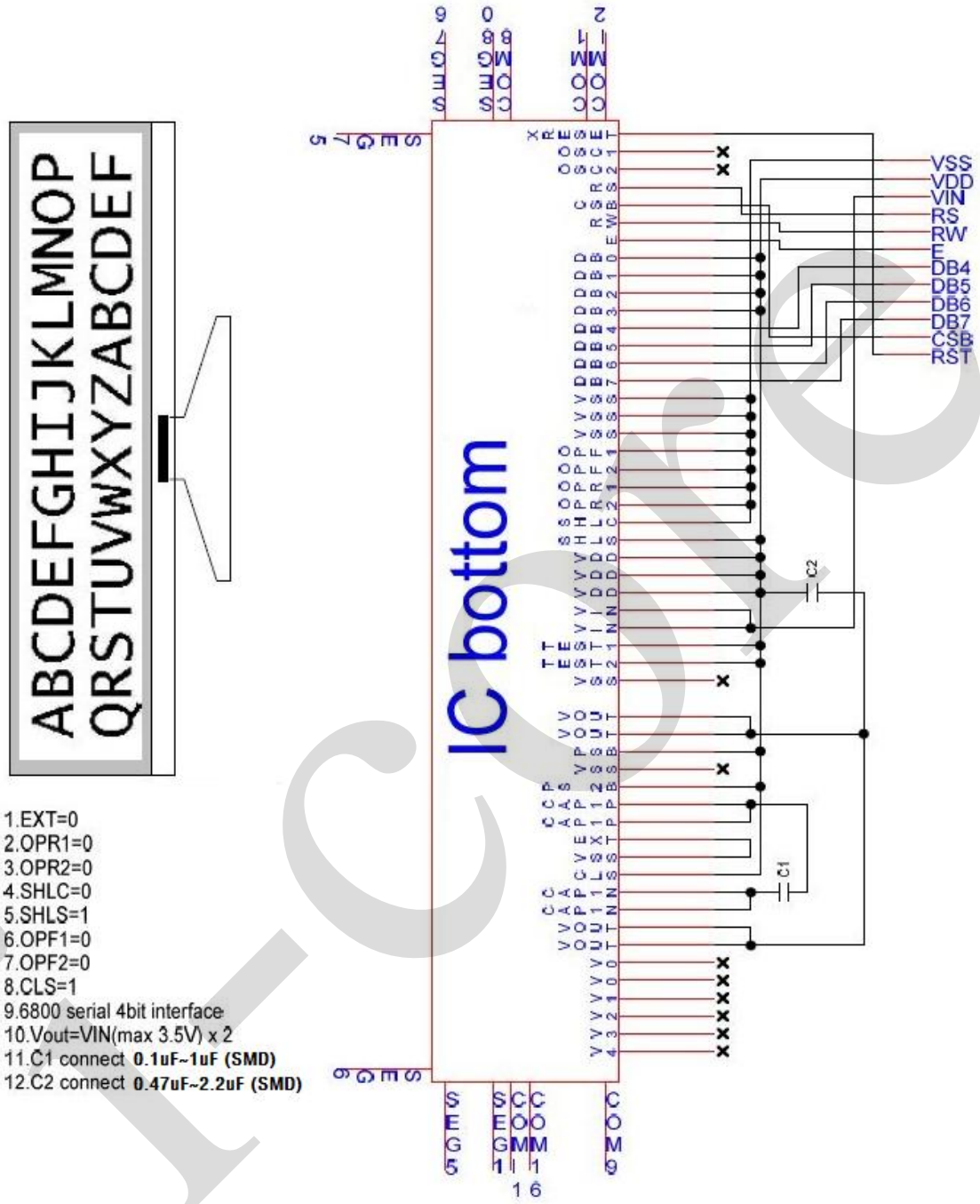


Note: When the heavy load is applied, the dotted line part could be added.

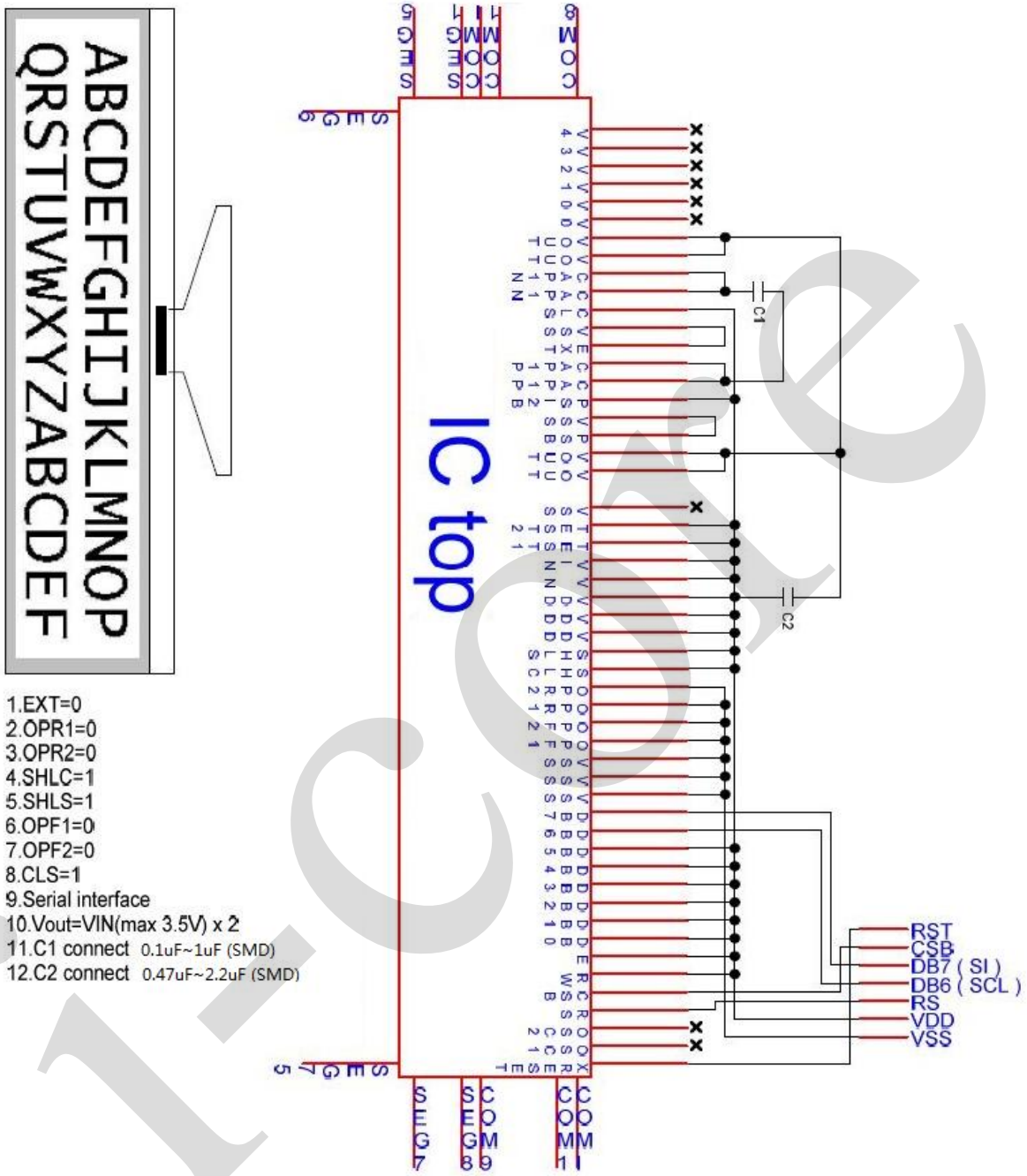
6.3、6800 serial 8bit parallel interface



6.4、6800 parallel 4bit interface

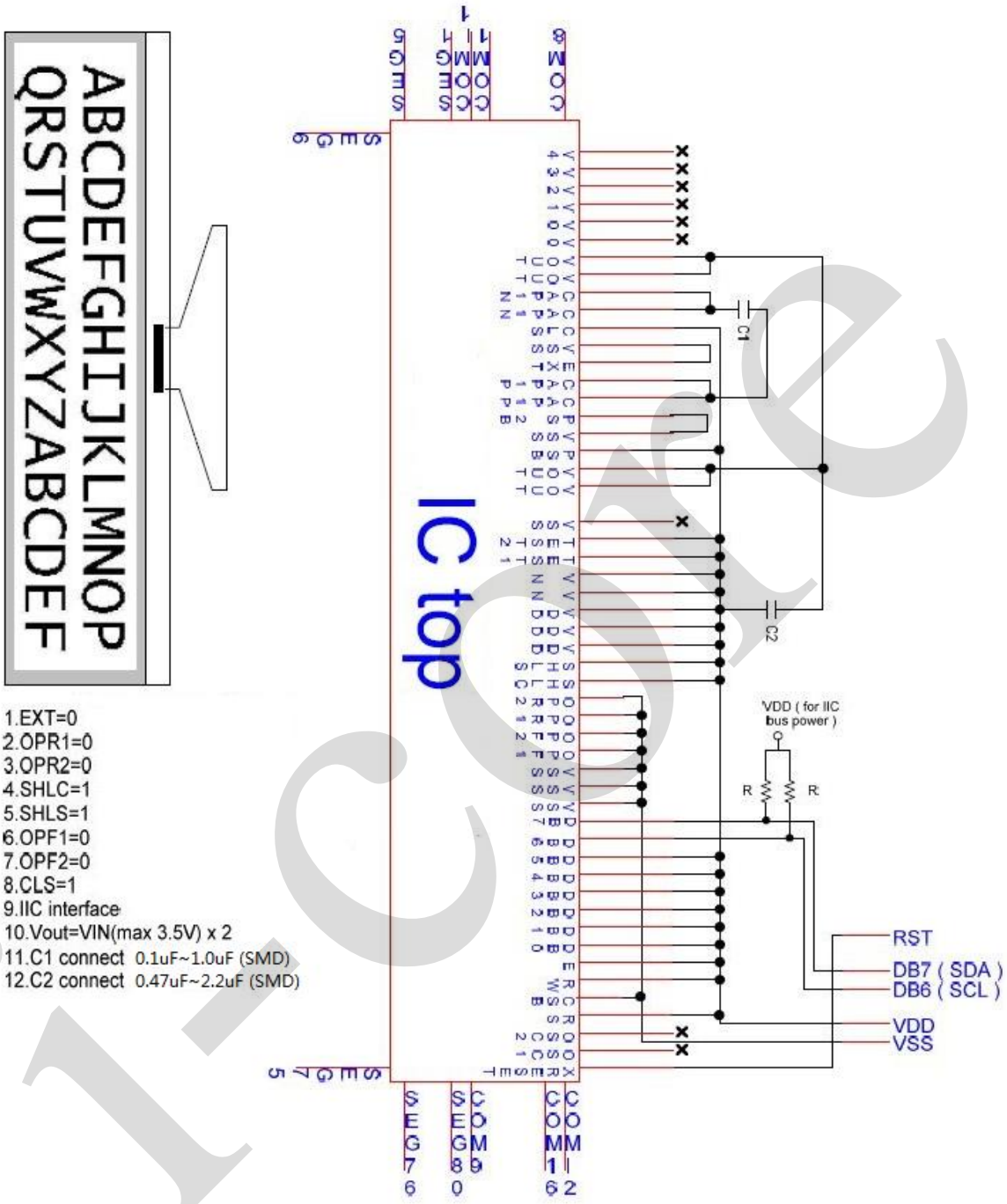


6.5、Serial Interface



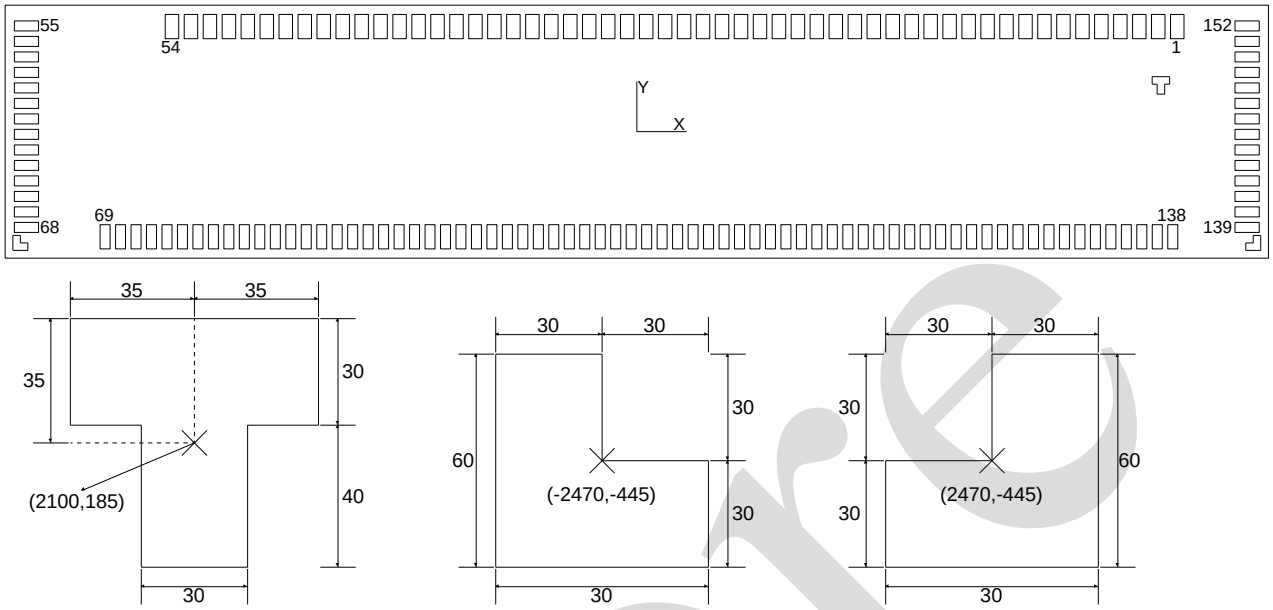
1.EXT=0
2.OPR1=0
3.OPR2=0
4.SHLC=1
5.SHLS=1
6.OPF1=0
7.OPF2=0
8.CLS=1
9.Serial interface
10.Vout=VIN(max 3.5V) x 2
11.C1 connect 0.1uF~1uF (SMD)
12.C2 connect 0.47uF~2.2uF (SMD)

6.6、I²C interface



7、Pad Diagram And Pad Location

7.1、Pad Diagram



Chip Size: 5062 × 1012um

Chip Thickness: 480um

Bump Pitch: 62um (min)

Bump Height: 9um (typ)

Bump Size:

Pad No.1~54：54um×97um

Pad No.55~68，139~152：97um×40um

Pad No.69~138：40um×97um

7.2、PAD location

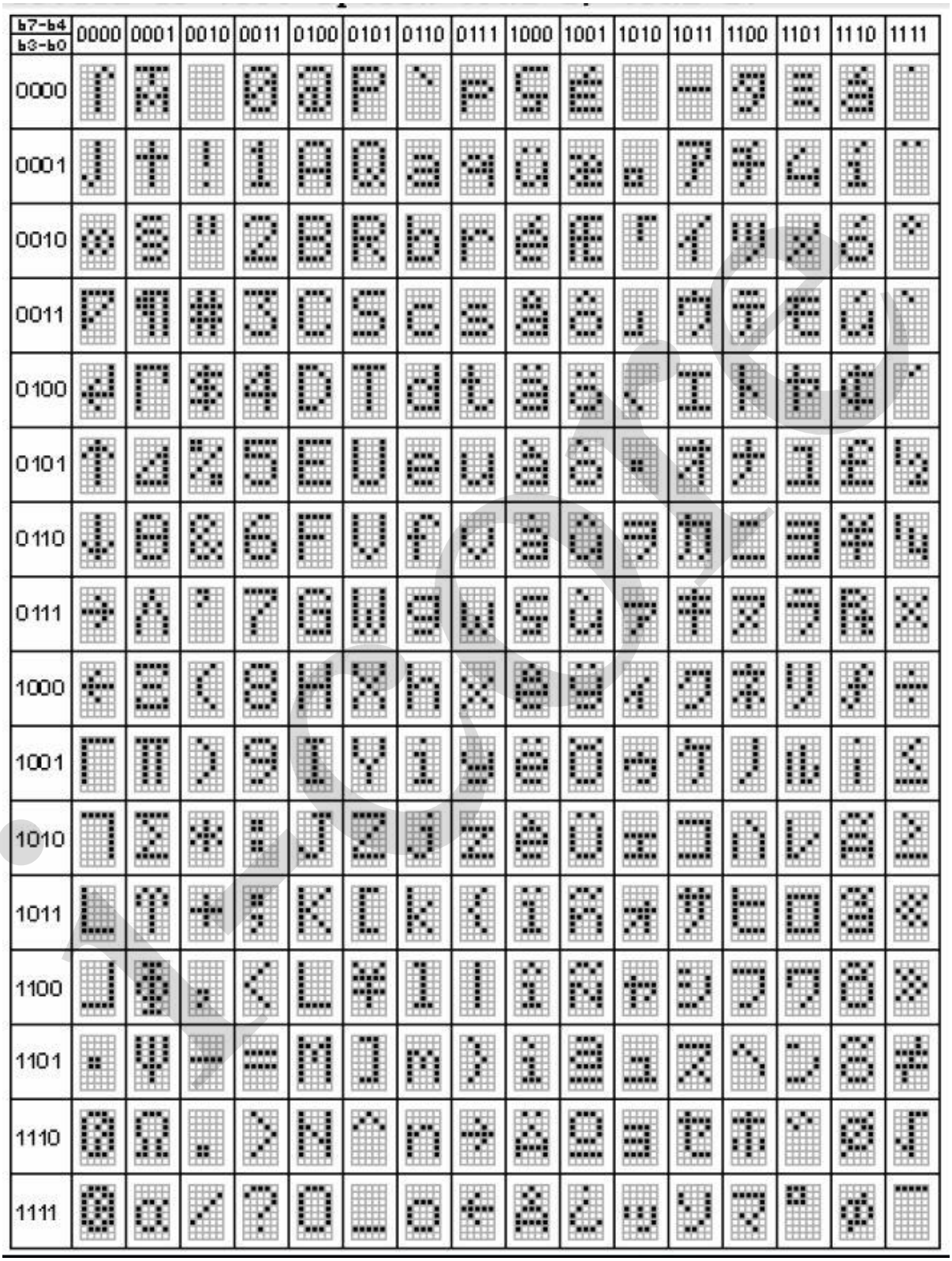
Pad No.	Function	X	Y	Pad No.	Function	X	Y
1	XRESET	2165.5	420.5	**77**	SEG[14]	-1634.5	-420.5
2	OSC1	2089.5	420.5	**78**	SEG[15]	-1572.5	-420.5
3	OSC2	2013.5	420.5	**79**	SEG[16]	-1510.5	-420.5
4	RS	1937.5	420.5	**80**	SEG[17]	-1448.5	-420.5
5	CSB	1861.5	420.5	**81**	SEG[18]	-1386.5	-420.5
6	RW	1785.5	420.5	**82**	SEG[19]	-1324.5	-420.5
7	E	1709.5	420.5	**83**	SEG[20]	-1262.5	-420.5
8	DB0	1633.5	420.5	**84**	SEG[21]	-1200.5	-420.5
9	DB1	1557.5	420.5	**85**	SEG[22]	-1138.5	-420.5
10	DB2	1481.5	420.5	**86**	SEG[23]	-1076.5	-420.5
11	DB3	1405.5	420.5	**87**	SEG[24]	-1014.5	-420.5
12	DB4	1329.5	420.5	**88**	SEG[25]	-952.5	-420.5
13	DB5	1253.5	420.5	**89**	SEG[26]	-890.5	-420.5
14	DB6	1177.5	420.5	**90**	SEG[27]	-828.5	-420.5
15	DB7	1101.5	420.5	**91**	SEG[28]	-766.5	-420.5
16	GND	1025.5	420.5	**92**	SEG[29]	-704.5	-420.5
17	GND	949.5	420.5	**93**	SEG[30]	-642.5	-420.5
18	GND	873.5	420.5	**94**	SEG[31]	-580.5	-420.5
19	OPF1	797.5	420.5	**95**	SEG[32]	-518.5	-420.5
20	OPF2	721.5	420.5	**96**	SEG[33]	-456.5	-420.5
21	OPR1	645.5	420.5	**97**	SEG[34]	-394.5	-420.5
22	OPR2	569.5	420.5	**98**	SEG[35]	-332.5	-420.5
23	SHLC	493.5	420.5	**99**	SEG[36]	-270.5	-420.5
24	SHLS	417.5	420.5	**100**	SEG[37]	-208.5	-420.5
25	VDD	341.5	420.5	**101**	SEG[38]	-146.5	-420.5
26	VDD	265.5	420.5	**102**	SEG[39]	-84.5	-420.5
27	VDD	189.5	420.5	**103**	SEG[40]	-22.5	-420.5
28	VIN	113.5	420.5	**104**	SEG[41]	39.5	-420.5
29	VIN	37.5	420.5	**105**	SEG[42]	101.5	-420.5
30	TEST1	-38.5	420.5	**106**	SEG[43]	163.5	-420.5
31	TEST2	-114.5	420.5	**107**	SEG[44]	225.5	-420.5
32	GND	-190.5	420.5	**108**	SEG[45]	287.5	-420.5
33	NC1	-266.5	420.5	**109**	SEG[46]	349.5	-420.5
34	VOUT	-342.5	420.5	**110**	SEG[47]	411.5	-420.5
35	VOUT	-418.5	420.5	**111**	SEG[48]	473.5	-420.5
36	PSB	-494.5	420.5	**112**	SEG[49]	535.5	-420.5
37	GND	-570.5	420.5	**113**	SEG[50]	597.5	-420.5
38	PSI2B	-646.5	420.5	**114**	SEG[51]	659.5	-420.5
39	CAP1P	-722.5	420.5	**115**	SEG[52]	721.5	-420.5

40	CAP1P	-798.5	420.5	**116**	SEG[53]	783.5	-420.5
41	EXT	-874.5	420.5	**117**	SEG[54]	845.5	-420.5
42	GND	-950.5	420.5	**118**	SEG[55]	907.5	-420.5
43	CLS	-1026.5	420.5	**119**	SEG[56]	969.5	-420.5
44	CAP1N	-1102.5	420.5	**120**	SEG[57]	1031.5	-420.5
45	CAP1N	-1178.5	420.5	**121**	SEG[58]	1093.5	-420.5
46	VOUT	-1254.5	420.5	**122**	SEG[59]	1155.5	-420.5
47	VOUT	-1330.5	420.5	**123**	SEG[60]	1217.5	-420.5
48	V0	-1406.5	420.5	**124**	SEG[61]	1279.5	-420.5
49	V0	-1482.5	420.5	**125**	SEG[62]	1341.5	-420.5
50	V1	-1558.5	420.5	**126**	SEG[63]	1403.5	-420.5
51	V2	-1634.5	420.5	**127**	SEG[64]	1465.5	-420.5
52	V3	-1710.5	420.5	**128**	SEG[65]	1527.5	-420.5
53	V4	-1786.5	420.5	**129**	SEG[66]	1589.5	-420.5
54	NC	-1862.5	420.5	**130**	SEG[67]	1651.5	-420.5
55	COM[8]	-2445.5	423	**131**	SEG[68]	1713.5	-420.5
56	COM[7]	-2445.5	361	**132**	SEG[69]	1775.5	-420.5
57	COM[6]	-2445.5	299	**133**	SEG[70]	1837.5	-420.5
58	COM[5]	-2445.5	237	**134**	SEG[71]	1899.5	-420.5
59	COM[4]	-2445.5	175	**135**	SEG[72]	1961.5	-420.5
60	COM[3]	-2445.5	113	**136**	SEG[73]	2023.5	-420.5
61	COM[2]	-2445.5	51	**137**	SEG[74]	2085.5	-420.5
62	COM[1]	-2445.5	-11	**138**	SEG[75]	2147.5	-420.5
63	COMI1	-2445.5	-73	**139**	SEG[76]	2445.5	-383
64	SEG[1]	-2445.5	-135	**140**	SEG[77]	2445.5	-321
65	SEG[2]	-2445.5	-197	**141**	SEG[78]	2445.5	-259
66	SEG[3]	-2445.5	-259	**142**	SEG[79]	2445.5	-197
67	SEG[4]	-2445.5	-321	**143**	SEG[80]	2445.5	-135
68	SEG[5]	-2445.5	-383	**144**	COM[9]	2445.5	-73
69	SEG[6]	-2130.5	-420.5	**145**	COM[10]	2445.5	-11
70	SEG[7]	-2068.5	-420.5	**146**	COM[11]	2445.5	51
71	SEG[8]	-2006.5	-420.5	**147**	COM[12]	2445.5	113
72	SEG[9]	-1944.5	-420.5	**148**	COM[13]	2445.5	175
73	SEG[10]	-1882.5	-420.5	**149**	COM[14]	2445.5	237
74	SEG[11]	-1820.5	-420.5	**150**	COM[15]	2445.5	299
75	SEG[12]	-1758.5	-420.5	**151**	COM[16]	2445.5	361
76	SEG[13]	-1696.5	-420.5	**152**	COMI2	2445.5	423

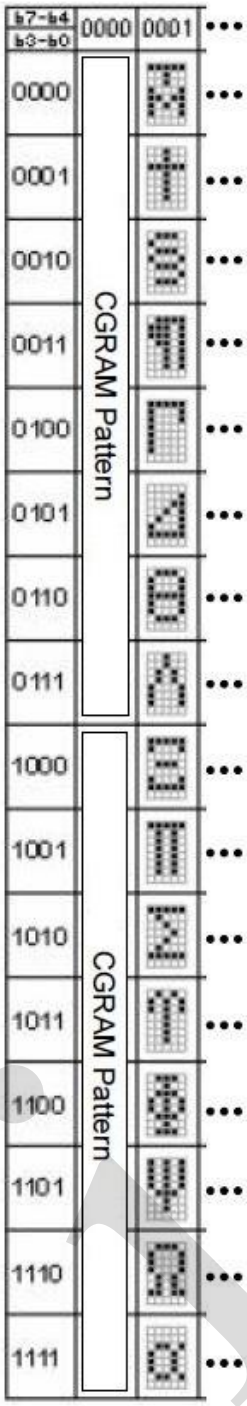
Unit：um

8、Character Pattern

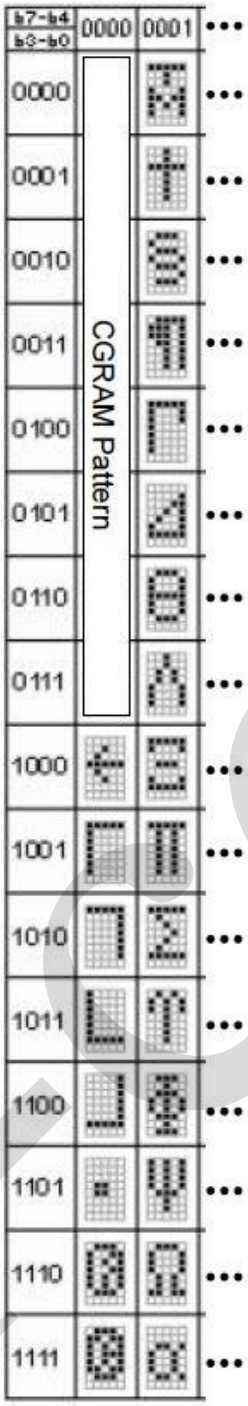
8.1、OPR1=1, OPR2, English/Japan/European



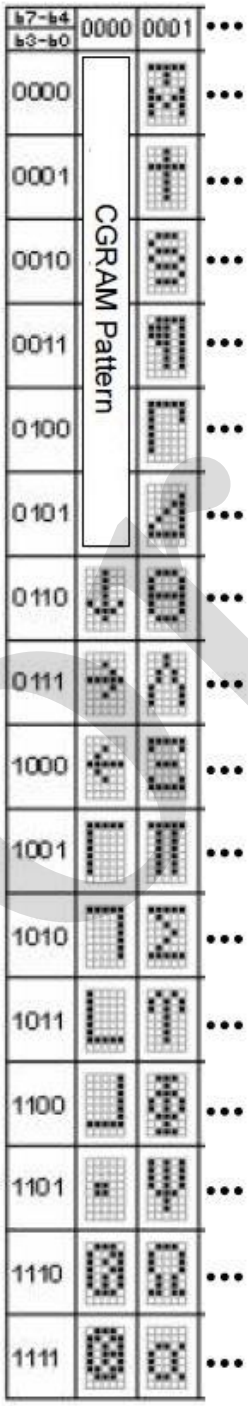
8.2、Select display pattern CGRAM



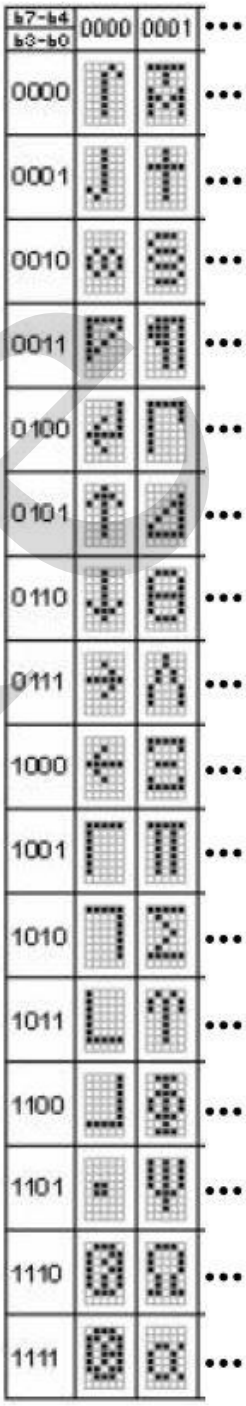
OPR2\OPR1=(0, 0)



OPR2\OPR1=(0, 1)



OPR2\OPR1=(1, 0)



OPR2\OPR1=(1, 1)

9、Statements And Notes

9.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

9.2、Notion

Recommended carefully reading this information before the use of this product；

The information in this document are subject to change without notice；

This information is using to the reference only, the company is not responsible for any loss；

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.