

Sitronix

ST7529A

32 Gray Scale Dot Matrix LCD Controller/Driver

1. INTRODUCTION

The ST7529A is a driver & controller LSI for 32 gray scale graphic dot-matrix liquid crystal display systems. It generates 255 Segment and 160 Common driver circuits. This chip is connected directly to a microprocessor, accepts Serial Peripheral Interface (SPI), 8-bit parallel display data and stores in an on-chip display data RAM. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver Output Circuits

- 255 segment outputs / 160 common outputs
- Maximum resolution is 255 x 160

Applicable Duty Ratios

- Various partial display
- Partial window moving & data scrolling

Microprocessor Interface

- 8bit parallel bi-directional interface with 6800-series or 8080-series
- 4-line serial interface (write only)
- 9 bit 3-line serial interface (write only)

On-chip Display Data RAM

- Capacity: 160 x 255 x 5bit = 204000bits (Max)

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x10)
- Voltage regulator
- Voltage follower
- (LCD bias: 1/9, 1/10, 1/11, 1/12, 1/13, 1/14)

Operating Voltage Range

- Supply voltage
(VDD, VDD1, VDD2, VDD3, VDD4): 2.4 to 3.3V
- LCD driving voltage (Vop = V0-XV0): 7.0 to 18.0V

Temperature Gradient Coefficient

- -0.130%/°C

LCD driving voltage (OTP)

- To store contrast adjustment value for better display

Package Type

- Application for COG

ST7529A	6800, 8080, 4-Line, 3-Line interface	
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3. Pad Arrangement

Chip Size :

10500um x 725um ($\pm 50\mu\text{m}$)

Pad pitch :

Com, Seg pad pitch:

Pad No113~552: 25 μm

IO pad pad pitch:

Pad No1~46, 50~97, 128~130: 80 μm

Pad No46~47, 49~50: 60 μm

Pad No47~49: 40 μm

Pad No97~98, 127~128: 79 μm

Pad No98~105, 110~127: 78 μm

Pad No105~106, 109~110: 84 μm

Pad No106~109: 90 μm

Pad size :

Com, Seg pad size:

Pad No131~138, 545~552 : 111 μm (X) x 14 μm (Y)

Pad No139~544 : 14 μm (X) x 111 μm (Y)

IO pad pad size:

Pad No1~46, 50~97, 128~130: 62 μm (X) x 63 μm (Y)

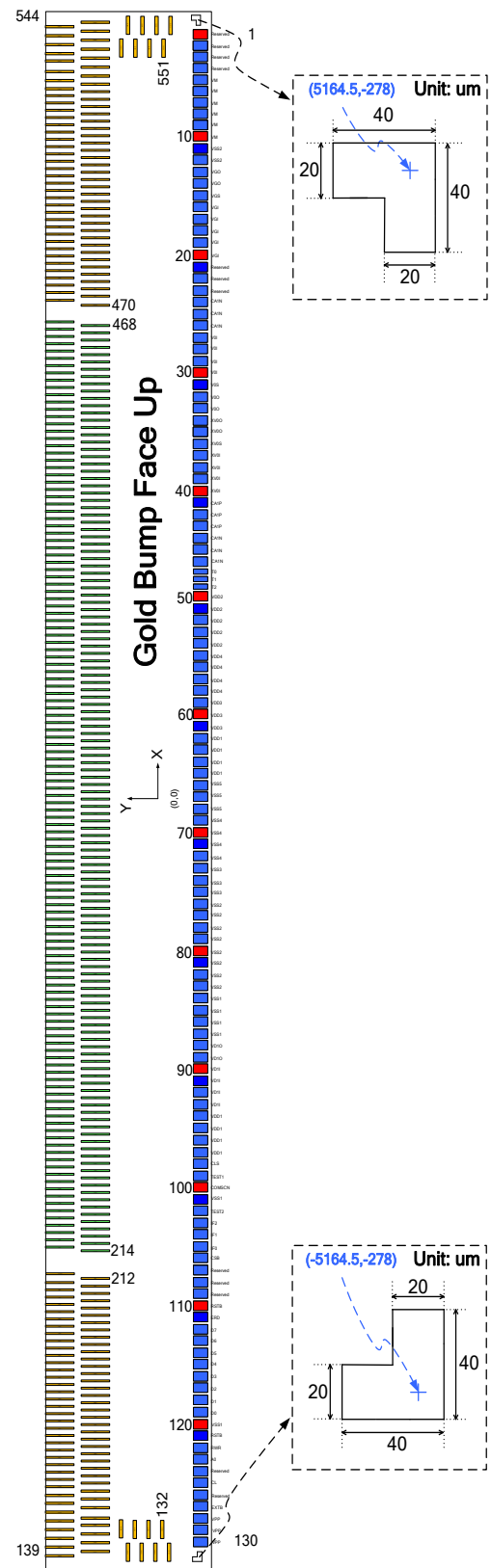
Pad No98~105, 110~127: 60 μm (X) x 63 μm (Y)

Pad No47~49: 22 μm (X) x 63 μm (Y)

Pad No106~109: 72 μm (X) x 63 μm (Y)

Bump Height: 15 μm

Chip Thickness: 480 μm



4. Pad Center Coordinates

PAD No.	PIN NAME	X	Y
1	Reserved	5094	-273.5
2	Reserved	5014	-273.5
3	Reserved	4934	-273.5
4	Reserved	4854	-273.5
5	VM	4774	-273.5
6	VM	4694	-273.5
7	VM	4614	-273.5
8	VM	4534	-273.5
9	VM	4454	-273.5
10	VM	4374	-273.5
11	VSS2	4294	-273.5
12	VSS2	4214	-273.5
13	VGO	4134	-273.5
14	VGO	4054	-273.5
15	VGS	3974	-273.5
16	VGI	3894	-273.5
17	VGI	3814	-273.5
18	VGI	3734	-273.5
19	VGI	3654	-273.5
20	VGI	3574	-273.5
21	Reserved	3494	-273.5
22	Reserved	3414	-273.5
23	Reserved	3334	-273.5
24	CA1N	3254	-273.5
25	CA1N	3174	-273.5
26	CA1N	3094	-273.5
27	V0I	3014	-273.5
28	V0I	2934	-273.5
29	V0I	2854	-273.5
30	V0I	2774	-273.5
31	V0S	2694	-273.5
32	V0O	2614	-273.5
33	V0O	2534	-273.5
34	XV0O	2454	-273.5
35	XV0O	2374	-273.5
36	XV0S	2294	-273.5

PAD No.	PIN NAME	X	Y
37	XV0I	2214	-273.5
38	XV0I	2134	-273.5
39	XV0I	2054	-273.5
40	XV0I	1974	-273.5
41	CA1P	1894	-273.5
42	CA1P	1814	-273.5
43	CA1P	1734	-273.5
44	CA1N	1654	-273.5
45	CA1N	1574	-273.5
46	CA1N	1494	-273.5
47	T0	1434	-273.5
48	T1	1394	-273.5
49	T2	1354	-273.5
50	VDD2	1294	-273.5
51	VDD2	1214	-273.5
52	VDD2	1134	-273.5
53	VDD2	1054	-273.5
54	VDD2	974	-273.5
55	VDD4	894	-273.5
56	VDD4	814	-273.5
57	VDD4	734	-273.5
58	VDD4	654	-273.5
59	VDD3	574	-273.5
60	VDD3	494	-273.5
61	VDD3	414	-273.5
62	VDD1	334	-273.5
63	VDD1	254	-273.5
64	VDD1	174	-273.5
65	VDD1	94	-273.5
66	VSS5	14	-273.5
67	VSS5	-66	-273.5
68	VSS5	-146	-273.5
69	VSS4	-226	-273.5
70	VSS4	-306	-273.5
71	VSS4	-386	-273.5
72	VSS4	-466	-273.5

PAD No.	PIN NAME	X	Y
73	VSS3	-546	-273.5
74	VSS3	-626	-273.5
75	VSS3	-706	-273.5
76	VSS2	-786	-273.5
77	VSS2	-866	-273.5
78	VSS2	-946	-273.5
79	VSS2	-1026	-273.5
80	VSS2	-1106	-273.5
81	VSS2	-1186	-273.5
82	VSS2	-1266	-273.5
83	VSS2	-1346	-273.5
84	VSS1	-1426	-273.5
85	VSS1	-1506	-273.5
86	VSS1	-1586	-273.5
87	VSS1	-1666	-273.5
88	VD1O	-1746	-273.5
89	VD1O	-1826	-273.5
90	VD1I	-1906	-273.5
91	VD1I	-1986	-273.5
92	VD1I	-2066	-273.5
93	VD1I	-2146	-273.5
94	VDD1	-2226	-273.5
95	VDD1	-2306	-273.5
96	VDD1	-2386	-273.5
97	VDD1	-2466	-273.5
98	CLS	-2545	-273.5
99	TEST1	-2623	-273.5
100	COMSCN	-2701	-273.5
101	VSS1	-2779	-273.5
102	TEST2	-2857	-273.5
103	IF2	-2935	-273.5
104	IF1	-3013	-273.5
105	IF0	-3091	-273.5
106	CSB	-3175	-273.5
107	Reserved	-3265	-273.5
108	Reserved	-3355	-273.5
109	Reserved	-3445	-273.5

PAD No.	PIN NAME	X	Y
110	RSTB	-3529	-273.5
111	ERD	-3607	-273.5
112	D7	-3685	-273.5
13	D6	-3763	-273.5
114	D5	-3841	-273.5
115	D4	-3919	-273.5
116	D3	-3997	-273.5
117	D2	-4075	-273.5
118	D1	-4153	-273.5
119	D0	-4231	-273.5
120	VSS1	-4309	-273.5
121	RSTB	-4387	-273.5
122	RWR	-4465	-273.5
123	A0	-4543	-273.5
124	Reserved	-4621	-273.5
125	CL	-4699	-273.5
126	Reserved	-4777	-273.5
127	EXTB	-4855	-273.5
128	VPP	-4934	-273.5
129	VPP	-5014	-273.5
130	VPP	-5094	-273.5
131	Reserved	-5136	-186
132	Reserved	-5005	-161
133	COM159	-5136	-136
134	COM157	-5005	-111
135	COM155	-5136	-86
136	COM153	-5005	-61
137	COM151	-5136	-36
138	COM149	-5005	-11
139	COM147	-5157.5	249.5
140	COM145	-5132.5	118.5
141	COM143	-5107.5	249.5
142	COM141	-5082.5	118.5
143	COM139	-5057.5	249.5
144	COM137	-5032.5	118.5
145	COM135	-5007.5	249.5
146	COM133	-4982.5	118.5

PAD No.	PIN NAME	X	Y
147	COM131	-4957.5	249.5
148	COM129	-4932.5	118.5
149	COM127	-4907.5	249.5
150	COM125	-4882.5	118.5
151	COM123	-4857.5	249.5
152	COM121	-4832.5	118.5
153	COM119	-4807.5	249.5
154	COM117	-4782.5	118.5
155	COM115	-4757.5	249.5
156	COM113	-4732.5	118.5
157	COM111	-4707.5	249.5
158	COM109	-4682.5	118.5
159	COM107	-4657.5	249.5
160	COM105	-4632.5	118.5
161	COM103	-4607.5	249.5
162	COM101	-4582.5	118.5
163	COM99	-4557.5	249.5
164	COM97	-4532.5	118.5
165	COM95	-4507.5	249.5
166	COM93	-4482.5	118.5
167	COM91	-4457.5	249.5
168	COM89	-4432.5	118.5
169	COM87	-4407.5	249.5
170	COM85	-4382.5	118.5
171	COM83	-4357.5	249.5
172	COM81	-4332.5	118.5
173	COM79	-4307.5	249.5
174	COM77	-4282.5	118.5
175	COM75	-4257.5	249.5
176	COM73	-4232.5	118.5
177	COM71	-4207.5	249.5
178	COM69	-4182.5	118.5
179	COM67	-4157.5	249.5
180	COM65	-4132.5	118.5
181	COM63	-4107.5	249.5
182	COM61	-4082.5	118.5
183	COM59	-4057.5	249.5

PAD No.	PIN NAME	X	Y
184	COM57	-4032.5	118.5
185	COM55	-4007.5	249.5
186	COM53	-3982.5	118.5
187	COM51	-3957.5	249.5
188	COM49	-3932.5	118.5
189	COM47	-3907.5	249.5
190	COM45	-3882.5	118.5
191	COM43	-3857.5	249.5
192	COM41	-3832.5	118.5
193	COM39	-3807.5	249.5
194	COM37	-3782.5	118.5
195	COM35	-3757.5	249.5
196	COM33	-3732.5	118.5
197	COM31	-3707.5	249.5
198	COM29	-3682.5	118.5
199	COM27	-3657.5	249.5
200	COM25	-3632.5	118.5
201	COM23	-3607.5	249.5
202	COM21	-3582.5	118.5
203	COM19	-3557.5	249.5
204	COM17	-3532.5	118.5
205	COM15	-3507.5	249.5
206	COM13	-3482.5	118.5
207	COM11	-3457.5	249.5
208	COM9	-3432.5	118.5
209	COM7	-3407.5	249.5
210	COM5	-3382.5	118.5
211	COM3	-3357.5	249.5
212	COM1	-3332.5	118.5
213	Reserved	-3307.5	249.5
214	Reserved	-3187.5	118.5
215	SEG0	-3162.5	249.5
216	SEG1	-3137.5	118.5
217	SEG2	-3112.5	249.5
218	SEG3	-3087.5	118.5
219	SEG4	-3062.5	249.5
220	SEG5	-3037.5	118.5

PAD No.	PIN NAME	X	Y
221	SEG6	-3012.5	249.5
222	SEG7	-2987.5	118.5
223	SEG8	-2962.5	249.5
224	SEG9	-2937.5	118.5
225	SEG10	-2912.5	249.5
226	SEG11	-2887.5	118.5
227	SEG12	-2862.5	249.5
228	SEG13	-2837.5	118.5
229	SEG14	-2812.5	249.5
230	SEG15	-2787.5	118.5
231	SEG16	-2762.5	249.5
232	SEG17	-2737.5	118.5
233	SEG18	-2712.5	249.5
234	SEG19	-2687.5	118.5
235	SEG20	-2662.5	249.5
236	SEG21	-2637.5	118.5
237	SEG22	-2612.5	249.5
238	SEG23	-2587.5	118.5
239	SEG24	-2562.5	249.5
240	SEG25	-2537.5	118.5
241	SEG26	-2512.5	249.5
242	SEG27	-2487.5	118.5
243	SEG28	-2462.5	249.5
244	SEG29	-2437.5	118.5
245	SEG30	-2412.5	249.5
246	SEG31	-2387.5	118.5
247	SEG32	-2362.5	249.5
248	SEG33	-2337.5	118.5
249	SEG34	-2312.5	249.5
250	SEG35	-2287.5	118.5
251	SEG36	-2262.5	249.5
252	SEG37	-2237.5	118.5
253	SEG38	-2212.5	249.5
254	SEG39	-2187.5	118.5
255	SEG40	-2162.5	249.5
256	SEG41	-2137.5	118.5
257	SEG42	-2112.5	249.5

PAD No.	PIN NAME	X	Y
258	SEG43	-2087.5	118.5
259	SEG44	-2062.5	249.5
260	SEG45	-2037.5	118.5
261	SEG46	-2012.5	249.5
262	SEG47	-1987.5	118.5
263	SEG48	-1962.5	249.5
264	SEG49	-1937.5	118.5
265	SEG50	-1912.5	249.5
266	SEG51	-1887.5	118.5
267	SEG52	-1862.5	249.5
268	SEG53	-1837.5	118.5
269	SEG54	-1812.5	249.5
270	SEG55	-1787.5	118.5
271	SEG56	-1762.5	249.5
272	SEG57	-1737.5	118.5
273	SEG58	-1712.5	249.5
274	SEG59	-1687.5	118.5
275	SEG60	-1662.5	249.5
276	SEG61	-1637.5	118.5
277	SEG62	-1612.5	249.5
278	SEG63	-1587.5	118.5
279	SEG64	-1562.5	249.5
280	SEG65	-1537.5	118.5
281	SEG66	-1512.5	249.5
282	SEG67	-1487.5	118.5
283	SEG68	-1462.5	249.5
284	SEG69	-1437.5	118.5
285	SEG70	-1412.5	249.5
286	SEG71	-1387.5	118.5
287	SEG72	-1362.5	249.5
288	SEG73	-1337.5	118.5
289	SEG74	-1312.5	249.5
290	SEG75	-1287.5	118.5
291	SEG76	-1262.5	249.5
292	SEG77	-1237.5	118.5
293	SEG78	-1212.5	249.5
294	SEG79	-1187.5	118.5

PAD No.	PIN NAME	X	Y
295	SEG80	-1162.5	249.5
296	SEG81	-1137.5	118.5
297	SEG82	-1112.5	249.5
298	SEG83	-1087.5	118.5
299	SEG84	-1062.5	249.5
300	SEG85	-1037.5	118.5
301	SEG86	-1012.5	249.5
302	SEG87	-987.5	118.5
303	SEG88	-962.5	249.5
304	SEG89	-937.5	118.5
305	SEG90	-912.5	249.5
306	SEG91	-887.5	118.5
307	SEG92	-862.5	249.5
308	SEG93	-837.5	118.5
309	SEG94	-812.5	249.5
310	SEG95	-787.5	118.5
311	SEG96	-762.5	249.5
312	SEG97	-737.5	118.5
313	SEG98	-712.5	249.5
314	SEG99	-687.5	118.5
315	SEG100	-662.5	249.5
316	SEG101	-637.5	118.5
317	SEG102	-612.5	249.5
318	SEG103	-587.5	118.5
319	SEG104	-562.5	249.5
320	SEG105	-537.5	118.5
321	SEG106	-512.5	249.5
322	SEG107	-487.5	118.5
323	SEG108	-462.5	249.5
324	SEG109	-437.5	118.5
325	SEG110	-412.5	249.5
326	SEG111	-387.5	118.5
327	SEG112	-362.5	249.5
328	SEG113	-337.5	118.5
329	SEG114	-312.5	249.5
330	SEG115	-287.5	118.5
331	SEG116	-262.5	249.5

PAD No.	PIN NAME	X	Y
332	SEG117	-237.5	118.5
333	SEG118	-212.5	249.5
334	SEG119	-187.5	118.5
335	SEG120	-162.5	249.5
336	SEG121	-137.5	118.5
337	SEG122	-112.5	249.5
338	SEG123	-87.5	118.5
339	SEG124	-62.5	249.5
340	SEG125	-37.5	118.5
341	SEG126	-12.5	249.5
342	SEG127	12.5	118.5
343	SEG128	37.5	249.5
344	SEG129	62.5	118.5
345	SEG130	87.5	249.5
346	SEG131	112.5	118.5
347	SEG132	137.5	249.5
348	SEG133	162.5	118.5
349	SEG134	187.5	249.5
350	SEG135	212.5	118.5
351	SEG136	237.5	249.5
352	SEG137	262.5	118.5
353	SEG138	287.5	249.5
354	SEG139	312.5	118.5
355	SEG140	337.5	249.5
356	SEG141	362.5	118.5
357	SEG142	387.5	249.5
358	SEG143	412.5	118.5
359	SEG144	437.5	249.5
360	SEG145	462.5	118.5
361	SEG146	487.5	249.5
362	SEG147	512.5	118.5
363	SEG148	537.5	249.5
364	SEG149	562.5	118.5
365	SEG150	587.5	249.5
366	SEG151	612.5	118.5
367	SEG152	637.5	249.5
368	SEG153	662.5	118.5

PAD No.	PIN NAME	X	Y
369	SEG154	687.5	249.5
370	SEG155	712.5	118.5
371	SEG156	737.5	249.5
372	SEG157	762.5	118.5
373	SEG158	787.5	249.5
374	SEG159	812.5	118.5
375	SEG160	837.5	249.5
376	SEG161	862.5	118.5
377	SEG162	887.5	249.5
378	SEG163	912.5	118.5
379	SEG164	937.5	249.5
380	SEG165	962.5	118.5
381	SEG166	987.5	249.5
382	SEG167	1012.5	118.5
383	SEG168	1037.5	249.5
384	SEG169	1062.5	118.5
385	SEG170	1087.5	249.5
386	SEG171	1112.5	118.5
387	SEG172	1137.5	249.5
388	SEG173	1162.5	118.5
389	SEG174	1187.5	249.5
390	SEG175	1212.5	118.5
391	SEG176	1237.5	249.5
392	SEG177	1262.5	118.5
393	SEG178	1287.5	249.5
394	SEG179	1312.5	118.5
395	SEG180	1337.5	249.5
396	SEG181	1362.5	118.5
397	SEG182	1387.5	249.5
398	SEG183	1412.5	118.5
399	SEG184	1437.5	249.5
400	SEG185	1462.5	118.5
401	SEG186	1487.5	249.5
402	SEG187	1512.5	118.5
403	SEG188	1537.5	249.5
404	SEG189	1562.5	118.5
405	SEG190	1587.5	249.5

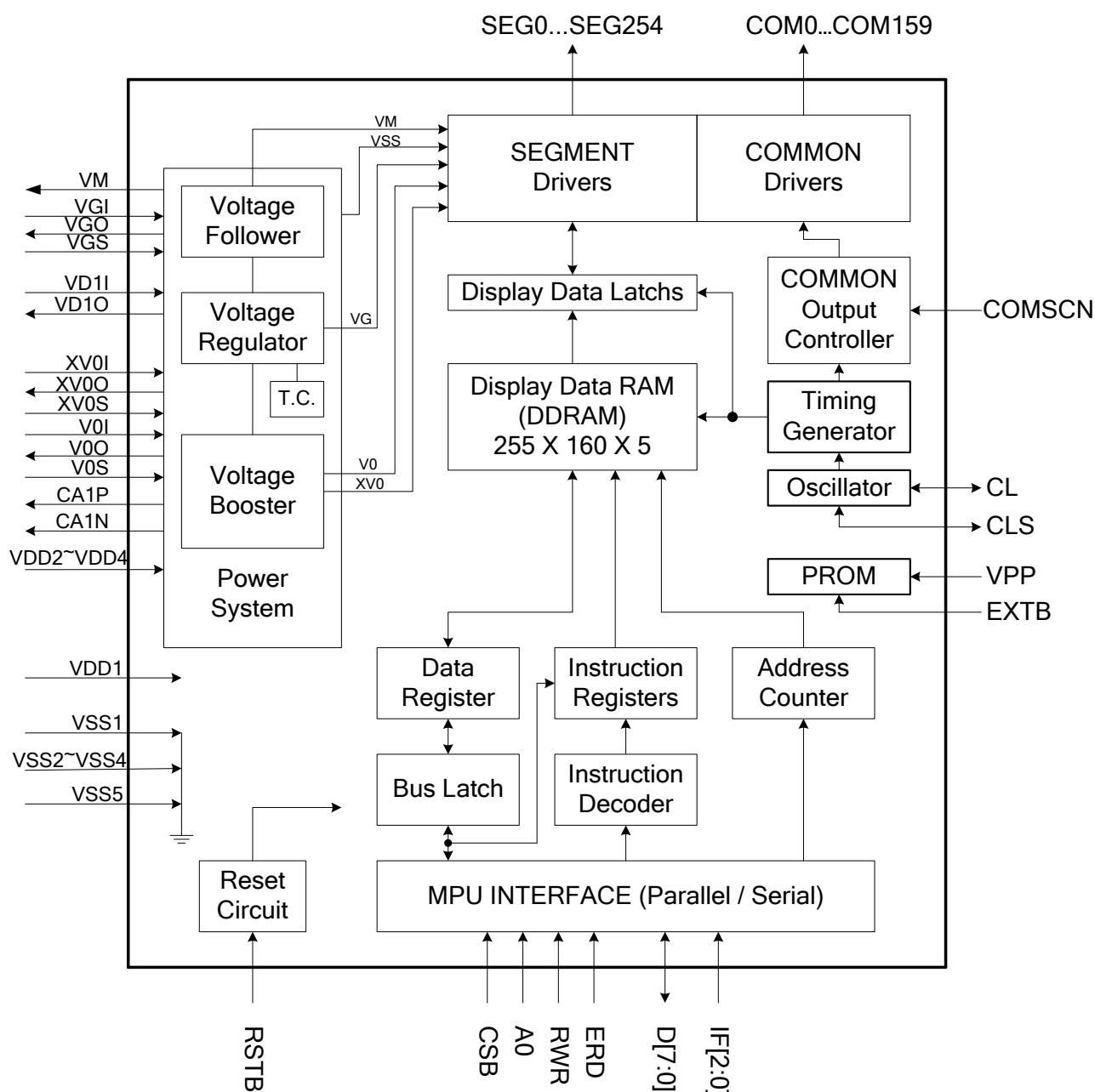
PAD No.	PIN NAME	X	Y
406	SEG191	1612.5	118.5
407	SEG192	1637.5	249.5
408	SEG193	1662.5	118.5
409	SEG194	1687.5	249.5
410	SEG195	1712.5	118.5
411	SEG196	1737.5	249.5
412	SEG197	1762.5	118.5
413	SEG198	1787.5	249.5
414	SEG199	1812.5	118.5
415	SEG200	1837.5	249.5
416	SEG201	1862.5	118.5
417	SEG202	1887.5	249.5
418	SEG203	1912.5	118.5
419	SEG204	1937.5	249.5
420	SEG205	1962.5	118.5
421	SEG206	1987.5	249.5
422	SEG207	2012.5	118.5
423	SEG208	2037.5	249.5
424	SEG209	2062.5	118.5
425	SEG210	2087.5	249.5
426	SEG211	2112.5	118.5
427	SEG212	2137.5	249.5
428	SEG213	2162.5	118.5
429	SEG214	2187.5	249.5
430	SEG215	2212.5	118.5
431	SEG216	2237.5	249.5
432	SEG217	2262.5	118.5
433	SEG218	2287.5	249.5
434	SEG219	2312.5	118.5
435	SEG220	2337.5	249.5
436	SEG221	2362.5	118.5
437	SEG222	2387.5	249.5
438	SEG223	2412.5	118.5
439	SEG224	2437.5	249.5
440	SEG225	2462.5	118.5
441	SEG226	2487.5	249.5
442	SEG227	2512.5	118.5

PAD No.	PIN NAME	X	Y
443	SEG228	2537.5	249.5
444	SEG229	2562.5	118.5
445	SEG230	2587.5	249.5
446	SEG231	2612.5	118.5
447	SEG232	2637.5	249.5
448	SEG233	2662.5	118.5
449	SEG234	2687.5	249.5
450	SEG235	2712.5	118.5
451	SEG236	2737.5	249.5
452	SEG237	2762.5	118.5
453	SEG238	2787.5	249.5
454	SEG239	2812.5	118.5
455	SEG240	2837.5	249.5
456	SEG241	2862.5	118.5
457	SEG242	2887.5	249.5
458	SEG243	2912.5	118.5
459	SEG244	2937.5	249.5
460	SEG245	2962.5	118.5
461	SEG246	2987.5	249.5
462	SEG247	3012.5	118.5
463	SEG248	3037.5	249.5
464	SEG249	3062.5	118.5
465	SEG250	3087.5	249.5
466	SEG251	3112.5	118.5
467	SEG252	3137.5	249.5
468	SEG253	3162.5	118.5
469	SEG254	3187.5	249.5
470	Reserved	3307.5	118.5
471	COM0	3332.5	249.5
472	COM2	3357.5	118.5
473	COM4	3382.5	249.5
474	COM6	3407.5	118.5
475	COM8	3432.5	249.5
476	COM10	3457.5	118.5
477	COM12	3482.5	249.5
478	COM14	3507.5	118.5
479	COM16	3532.5	249.5

PAD No.	PIN NAME	X	Y
480	COM18	3557.5	118.5
481	COM20	3582.5	249.5
482	COM22	3607.5	118.5
483	COM24	3632.5	249.5
484	COM26	3657.5	118.5
485	COM28	3682.5	249.5
486	COM30	3707.5	118.5
487	COM32	3732.5	249.5
488	COM34	3757.5	118.5
489	COM36	3782.5	249.5
490	COM38	3807.5	118.5
491	COM40	3832.5	249.5
492	COM42	3857.5	118.5
493	COM44	3882.5	249.5
494	COM46	3907.5	118.5
495	COM48	3932.5	249.5
496	COM50	3957.5	118.5
497	COM52	3982.5	249.5
498	COM54	4007.5	118.5
499	COM56	4032.5	249.5
500	COM58	4057.5	118.5
501	COM60	4082.5	249.5
502	COM62	4107.5	118.5
503	COM64	4132.5	249.5
504	COM66	4157.5	118.5
505	COM68	4182.5	249.5
506	COM70	4207.5	118.5
507	COM72	4232.5	249.5
508	COM74	4257.5	118.5
509	COM76	4282.5	249.5
510	COM78	4307.5	118.5
511	COM80	4332.5	249.5
512	COM82	4357.5	118.5
513	COM84	4382.5	249.5
514	COM86	4407.5	118.5
515	COM88	4432.5	249.5
516	COM90	4457.5	118.5

PAD No.	PIN NAME	X	Y
517	COM92	4482.5	249.5
518	COM94	4507.5	118.5
519	COM96	4532.5	249.5
520	COM98	4557.5	118.5
521	COM100	4582.5	249.5
522	COM102	4607.5	118.5
523	COM104	4632.5	249.5
524	COM106	4657.5	118.5
525	COM108	4682.5	249.5
526	COM110	4707.5	118.5
527	COM112	4732.5	249.5
528	COM114	4757.5	118.5
529	COM116	4782.5	249.5
530	COM118	4807.5	118.5
531	COM120	4832.5	249.5
532	COM122	4857.5	118.5
533	COM124	4882.5	249.5
534	COM126	4907.5	118.5
535	COM128	4932.5	249.5
536	COM130	4957.5	118.5
537	COM132	4982.5	249.5
538	COM134	5007.5	118.5
539	COM136	5032.5	249.5
540	COM138	5057.5	118.5
541	COM140	5082.5	249.5
542	COM142	5107.5	118.5
543	COM144	5132.5	249.5
544	COM146	5157.5	118.5
545	COM148	5005	-11
546	COM150	5136	-36
547	COM152	5005	-61
548	COM154	5136	-86
549	COM156	5005	-111
550	COM158	5136	-136
551	Reserved	5005	-161
552	Reserved	5136	-186

5. BLOCK DIAGRAM



6. PIN DESCRIPTION

6.1 POWER SUPPLY

Name	I/O	Description						
VDD1	Supply	Power supply for logic circuit						
VDD2	Supply	Power supply for Booster Circuit						
VDD3 VDD4	Supply	Power supply for LCD						
VSS1 VSS2 VSS3 VSS4 VSS5	Supply	Ground. Ground system should be connected together.						
VD1I VD1O	Supply	VD1I is the power source of digital circuits. VD1O is the VD1 output. VD1I and VD1O should be connected together.						
CA1P CA1N	O	DC/DC voltage converter. Connect a capacitor between CA1P and CA1N.						
V0O V0I V0S	Supply	Positive operating voltage of COM-drivers. V0O is the output of the positive Vop generator. V0I is the positive Vop supply of LCD drivers. V0S is the sensor of the positive Vop generator. V0O, V0I & V0S should be connected together by ITO.						
XV0O XV0I XV0S	Supply	Negative operating voltage of COM-drivers. XV0O is the output of the negative Vop generator. XV0I is the negative Vop supply of LCD drivers. XV0S is the sensor of the negative Vop generator. XV0O, XV0I & XV0S should be connected together by ITO.						
VGO VGI VGS VM	Power	VG is the power of SEG-drivers. VM is the non-select voltage level of COM-drivers. VGO is the output of the VG regulator. VGI is the supply of SEG-drivers. VGS is the sensor of the VG regulator. VGO, VGI & VGS should be connected together by ITO. VM is the I/O pin of LCD bias supply voltage. Be sure the relationships (as shown below) among the LCD driving voltages: $V0 \geq VG \geq VM \geq VSS \geq XV0$; $VG \geq VM \geq 0.9V$; $VDD2 \geq VG \geq 1.8V$ When this IC is operating, VG and VM are generated according to the bias setting shown below: <table border="1"> <thead> <tr> <th>LCD Bias</th><th>VG</th><th>VM</th></tr> </thead> <tbody> <tr> <td>1/N Bias</td><td>$(2/N) \times V0$</td><td>$(1/N) \times V0$</td></tr> </tbody> </table> Note: N = 9~14	LCD Bias	VG	VM	1/N Bias	$(2/N) \times V0$	$(1/N) \times V0$
LCD Bias	VG	VM						
1/N Bias	$(2/N) \times V0$	$(1/N) \times V0$						

6.2 LCD DRIVER SUPPLY

Name	I/O	Description
CLS	I	When using internal clock oscillator, connect CLS to VDD. When using external clock oscillator, connect CLS to VSS.
CL	I/O	When using internal clock oscillator, it is the output of oscillator. When using external clock oscillator, it is the input of oscillator.

6.3 TEST

Name	I/O	Description
T0-T2	Test	Reserved for test only. T0 can be floating or connected to VSS1. T1-T2 must be floating.
TEST1-TEST2	Test	TEST1, TEST2 must be fixed to VDD1. This pin is reserved for internal setting.
Reserved	Test	Reserved for test only, recommend setting to floating.

6.4 MICROPROCESSOR INTERFACE

Name	I/O	Description																				
RSTB	I	Reset input pin When RSTB is “L”, initialization is executed.																				
CSB	I	Chip select input pins Data/instruction I/O is enabled only when CSB is "L". When chip select is non-active, DB0 to DB7 may be high impedance.																				
IF[2:0]	I	Parallel / Serial data input select input <table><tr><th>IF0</th><th>IF1</th><th>IF2</th><th>MPU interface type</th></tr><tr><td>H</td><td>H</td><td>L</td><td>80 series 8-bit parallel</td></tr><tr><td>L</td><td>H</td><td>H</td><td>68 series 8-bit parallel</td></tr><tr><td>L</td><td>L</td><td>H</td><td>9-bit serial (3 line)</td></tr><tr><td>L</td><td>L</td><td>L</td><td>8-bit serial (4 line)</td></tr></table>	IF0	IF1	IF2	MPU interface type	H	H	L	80 series 8-bit parallel	L	H	H	68 series 8-bit parallel	L	L	H	9-bit serial (3 line)	L	L	L	8-bit serial (4 line)
IF0	IF1	IF2	MPU interface type																			
H	H	L	80 series 8-bit parallel																			
L	H	H	68 series 8-bit parallel																			
L	L	H	9-bit serial (3 line)																			
L	L	L	8-bit serial (4 line)																			
A0	I	Register select input pin A0 = "H": DB0 to DB7 or SI are display data A0 = "L": DB0 to DB7 or SI are control data There is no A0 pin in 3-Line SPI interface. A0 should be fixed to “H” by VDD1.																				
RWR	I	Read / Write execution control pin <table><tr><th>MPU type</th><th>RWR</th><th>Description</th></tr><tr><td>6800-series</td><td>RW</td><td>Read / Write control input pin RW = “H” : read RW = “L” : write</td></tr><tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr></table> This pin is not used in serial interfaces and should be connected to VDD1.	MPU type	RWR	Description	6800-series	RW	Read / Write control input pin RW = “H” : read RW = “L” : write	8080-series	/WR	Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WR signal.											
MPU type	RWR	Description																				
6800-series	RW	Read / Write control input pin RW = “H” : read RW = “L” : write																				
8080-series	/WR	Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WR signal.																				
ERD	I	Read / Write execution control pin <table><tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr><tr><td>6800-series</td><td>E</td><td>Read / Write control input pin RW = “H”: When E is “H”, DB0 to DB7 are in an output status. RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr><tr><td>8080-series</td><td>/RD</td><td>Read enable clock input pin When /RD is “L”, DB0 to DB7 are in an output status.</td></tr></table> This pin is not used in serial interfaces and should be connected to VDD1.	MPU Type	ERD	Description	6800-series	E	Read / Write control input pin RW = “H”: When E is “H”, DB0 to DB7 are in an output status. RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.	8080-series	/RD	Read enable clock input pin When /RD is “L”, DB0 to DB7 are in an output status.											
MPU Type	ERD	Description																				
6800-series	E	Read / Write control input pin RW = “H”: When E is “H”, DB0 to DB7 are in an output status. RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.																				
8080-series	/RD	Read enable clock input pin When /RD is “L”, DB0 to DB7 are in an output status.																				

D7 to D0	I/O	When using 8-bit parallel interface: 8080 or 6800 mode 8 bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor. When CSB is "H", D[7:0] are high impedance.
	I/O	When using serial interface : 4-line SPI or 3-line SPI mode D[0:3] : fix to "H" by VDD1. D[4:6] : serial input/output data (SDA). D[7] : serial input clock (SCL). <u>D4 to D6 must be connected together (SDA)</u> When CSB is "H", D[7:0] are high impedance.

NOTE:

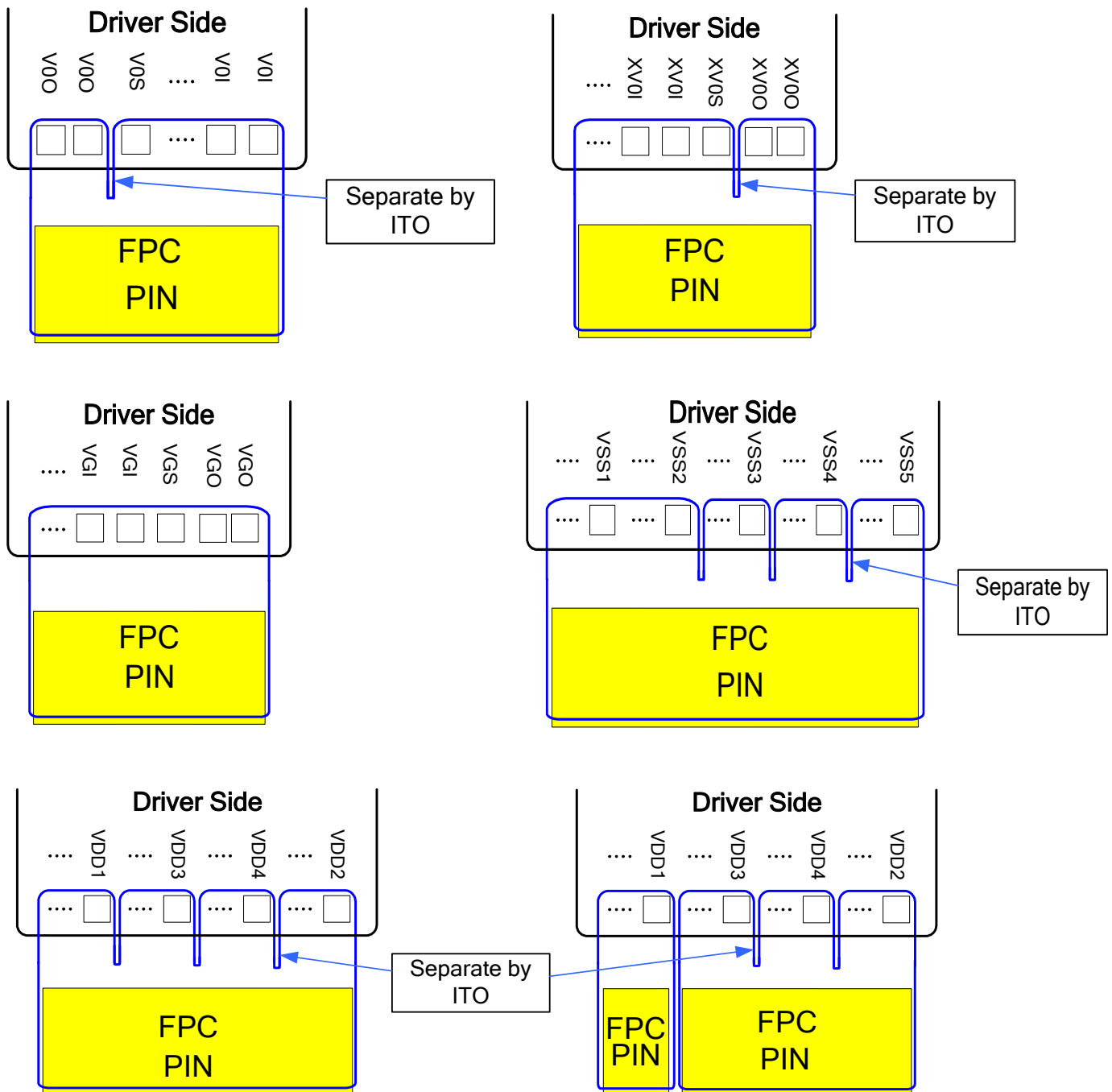
Microprocessor interface pins should not be floating in any operation mode.

6.5 LCD DRIVER OUTPUTS

Name	I/O	Description																										
SEG0 to SEG254	O	LCD segment driver outputs The display data and the M signal control the output voltage of segment driver. <table><tr><th rowspan="2">Display data</th><th rowspan="2">M (Internal)</th><th colspan="2">Segment driver output voltage</th></tr><tr><th>Normal display</th><th>Reverse display</th></tr><tr><td>H</td><td>H</td><td>VG</td><td>VSS</td></tr><tr><td>H</td><td>L</td><td>VSS</td><td>VG</td></tr><tr><td>L</td><td>H</td><td>VSS</td><td>VG</td></tr><tr><td>L</td><td>L</td><td>VG</td><td>VSS</td></tr><tr><td colspan="2">Power save mode</td><td>VSS</td><td>VSS</td></tr></table>	Display data	M (Internal)	Segment driver output voltage		Normal display	Reverse display	H	H	VG	VSS	H	L	VSS	VG	L	H	VSS	VG	L	L	VG	VSS	Power save mode		VSS	VSS
Display data	M (Internal)	Segment driver output voltage																										
		Normal display	Reverse display																									
H	H	VG	VSS																									
H	L	VSS	VG																									
L	H	VSS	VG																									
L	L	VG	VSS																									
Power save mode		VSS	VSS																									
COM0 to COM159	O	LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver. <table><tr><th>Scan data</th><th>M (Internal)</th><th>Common driver output voltage</th></tr><tr><td>H</td><td>H</td><td>XV0</td></tr><tr><td>H</td><td>L</td><td>V0</td></tr><tr><td>L</td><td>H</td><td>VM</td></tr><tr><td>L</td><td>L</td><td>VM</td></tr><tr><td colspan="2">Power save mode</td><td>VSS</td></tr></table>	Scan data	M (Internal)	Common driver output voltage	H	H	XV0	H	L	V0	L	H	VM	L	L	VM	Power save mode		VSS								
Scan data	M (Internal)	Common driver output voltage																										
H	H	XV0																										
H	L	V0																										
L	H	VM																										
L	L	VM																										
Power save mode		VSS																										
COMSCN	I	Set scan direction of COM. 1. COMSCN="L"; COM0→COMX; IC is placed under the module. FPC COMSCN=L <table><tr><th>IC COM Pad Name</th><th>Module COM Display Direction</th></tr><tr><td>COM0</td><td>COM0</td></tr><tr><td>COMX</td><td>↓ COMX</td></tr></table> 2. COMSCN="H"; COMX→COM0; IC is placed below the module. COMSCN=H FPC <table><tr><th>IC COM Pad Name</th><th>Module COM Display Direction</th></tr><tr><td>COMX</td><td>COM0</td></tr><tr><td>COM0</td><td>↓ COMX</td></tr></table> Note: COMX is determined by the DUTY setting.	IC COM Pad Name	Module COM Display Direction	COM0	COM0	COMX	↓ COMX	IC COM Pad Name	Module COM Display Direction	COMX	COM0	COM0	↓ COMX														
IC COM Pad Name	Module COM Display Direction																											
COM0	COM0																											
COMX	↓ COMX																											
IC COM Pad Name	Module COM Display Direction																											
COMX	COM0																											
COM0	↓ COMX																											

6.6 ITO Layout Guide

For V0, XV0, VG, VDD and VSS- The ITO layout suggestion is shown as below:



Single VDD: VDDI and VDDA together

Dual VDD: VDDI and VDDA separately

6.7 For VPP

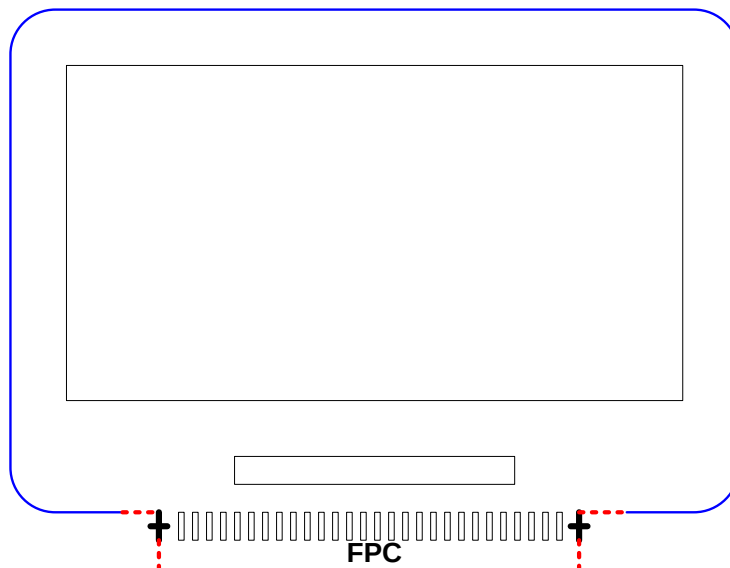
This is the power source for programming the internal OTP. If the ITO resistance is too high, the operation current will cause the voltage drop while programming OTP. Please try to keep the ITO resistance as low as possible.

6.8 Enhance ESD performance for COG application

1. Increase RSTB resistance:



2. Add ESD protection ring



Note: Please short the ESD protection ring to VSS of external device

7. FUNCTIONAL DESCRIPTION

7.1 MICROPROCESSOR INTERFACE

Chip Select Input

The CSB pin is for chip selection. The ST7529A can function with an MPU when CSB is "L". In case of serial interface, the internal shift register and the counter are reset.

7.1.1 Selecting Parallel / Serial Interface

ST7529A has seven types of interface with an MPU, which are four parallel and three serial interfaces. This parallel or serial interface is determined by IF pin as shown in table 7.1.1.

Table 7.1.1 Parallel / Serial Interface Mode

IF0	IF1	IF2	Interface type	CSB	A0	/RD(E)	/WR(R/W)	D7 to D0
H	H	L	80 serial 8-bit parallel	CSB	A0	/RD	/WR	D7 to D0
L	H	H	68 serial 8-bit parallel	CSB	A0	E	R/W	D7 to D0
L	L	H	9-bit SPI mode (3 line)	CSB	--	--	--	D[7]= SCL, D[4:6]=SDA, D[0:3]= ---
L	L	L	8-bit SPI mode (4 line)	CSB	A0	--	--	D[7]= SCL, D[4:6]=SDA, D[0:3]= ---

Note: The un-used pins are marked as "---" and should be fixed to "H" by VDD1.

7.1.2 8bit Parallel Interface

The ST7529A identifies the type of the data bus signals according to the combination of A0, /RD (E) and /WR (W/R) as shown in table 7.1.2.

Table 7.1.2 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	R/W	E	/RD	/WR	
H	H	H	L	H	Display data read out
H	L	H	H	L	Display data write
L	H	H	L	H	Register status read
L	L	H	H	L	Writes to internal register (instruction)

Relation between Data Bus and Gradation Data

ST7529A offers the 3bytes 3pixels(3B3P) mode to display 32 gray scale data.

3B3P 32 Gray Scale Display

8-bit mode

D7	D6	D5	D4	D3	D2	D1	D0	
P0	P0	P0	P0	P0	X	X	X	1st write
P1	P1	P1	P1	P1	X	X	X	2nd write
P2	P2	P2	P2	P2	X	X	X	3rd write

A single pixel of data is read after the third write operation as shown, and it is written in the display RAM.

"X" are dummy bits, which are ignored for display.

7.1.3 8-bit (4 line) and 9-bit (3 line) Serial Interface

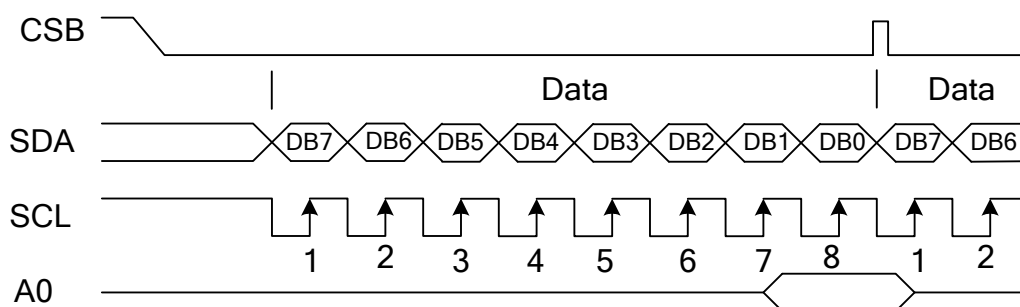
The 8-bit serial interface uses four pins CSB, SDA, SCL, and A0 to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins CSB, SDA and SCL for the same purpose.

Data read is not available in the serial interface. The entered data must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.

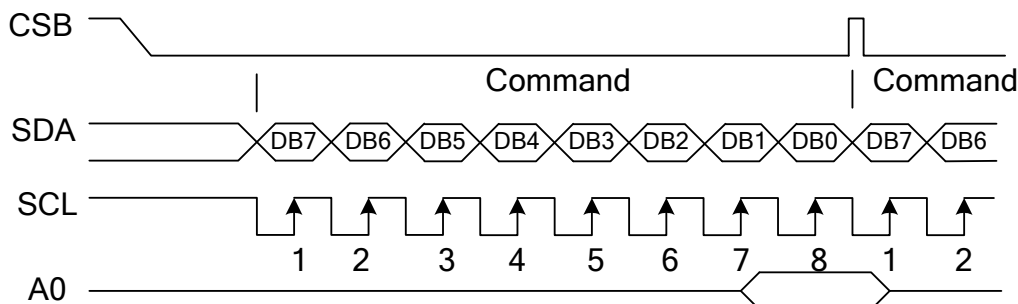
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode at every gradation.

(1) 8-bit serial interface (4 line)

When entering data (parameters): A0= HIGH at the rising edge of the 8th SCL.

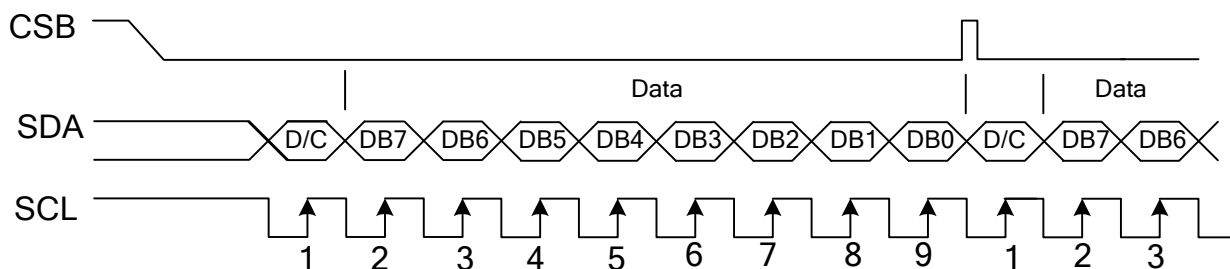


When entering command: A0= LOW at the rising edge of the 8th SCL

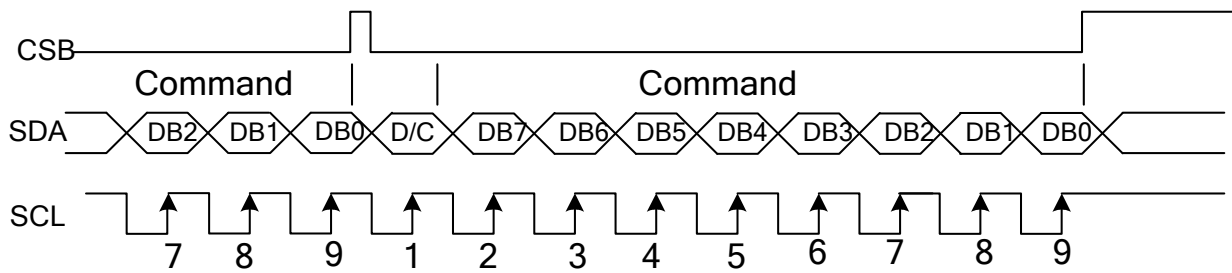


(2) 9-bit serial interface (3 line)

When entering data (parameters): SDA= HIGH at the rising edge of the 1st SCL.



When entering command: SDA= LOW at the rising edge of the 1st SCL.



- If CSB is set to HIGH while the 8 bits from D7 to D0 are entered, the data concerned is invalid. Before entering succeeding sets of data, you must correctly input the data concerned again.
- In order to avoid data transfer error due to incoming noise, it is recommended to set CSB at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
- When executing the command RAMWR, set CSB to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

7.2 ACCESS TO DDRAM AND INTERNAL REGISTERS

Since ST7529A access from MPU by pipeline processing via the bus holder attached to the internal that requires only the cycle time but no waiting time, it can achieves high-speed data transfer.

For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle start. When MPU reads data from the DDRAM, the first read cycle is dummy and the data read in the dummy cycle is held by the bus holder, and then it read from the bus holder to the system bus in the succeeding read cycle. Fig. 7.2.1 illustrates these relations.

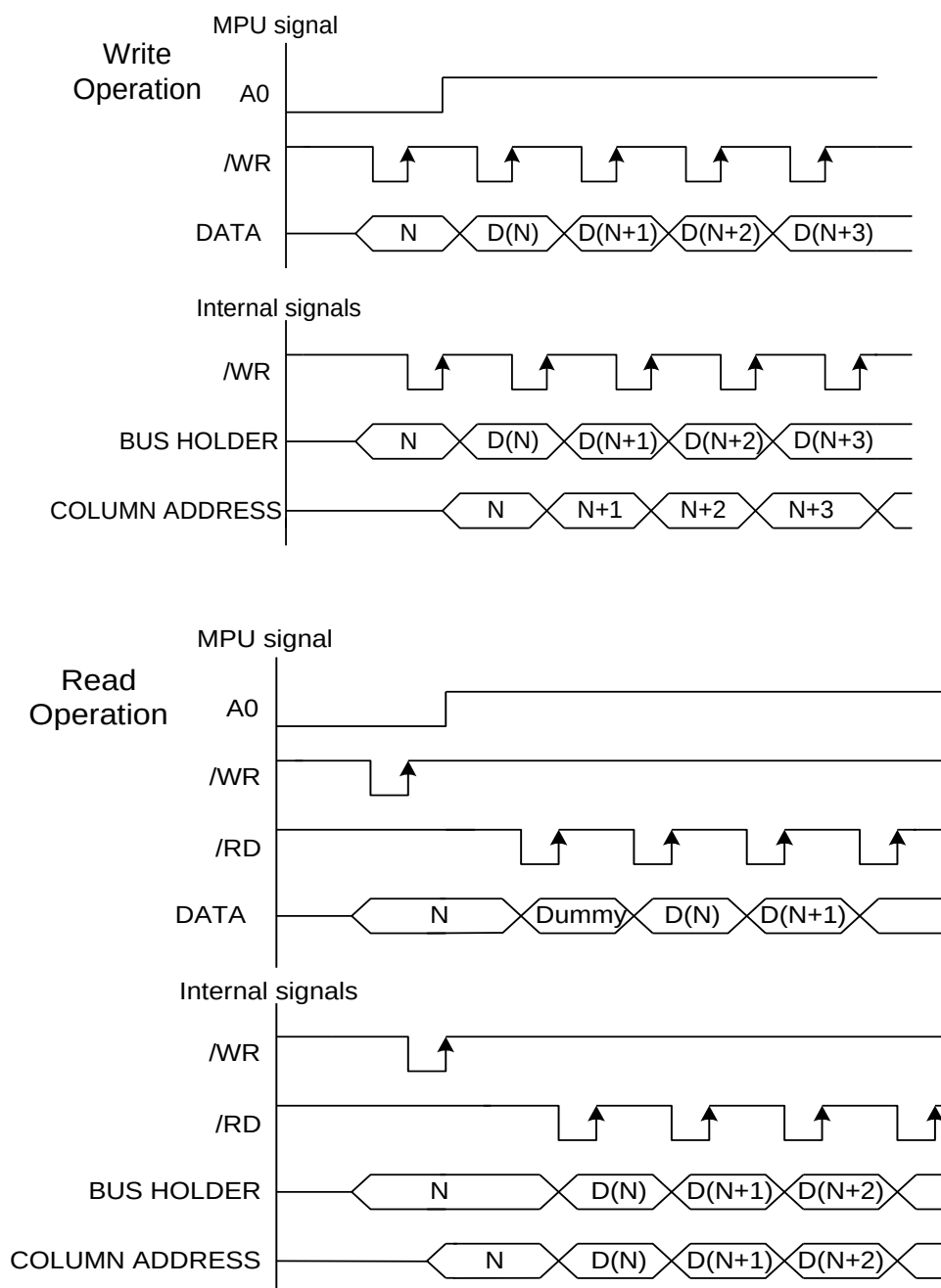


Fig 7.2.1

7.3 DISPLAY DATA RAM (DDRAM)

7.3.1 DDRAM

It is 160 X 255 X 5 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the LINE address and column address.

The RAM on ST7529A is separated to a block per 4 lines to allow the display system to process data on the block basis.

The reading and writing RAM operations of MPU are performed via the I/O buffer circuit. Reading of the RAM for the liquid crystal drive is controlled from another separate circuit.

Refer to the following memory map for the RAM configuration.

32 Gray Scale Display

Memory Map (3B3P, 8-bit mode)

			Column									
LCD read direction	CI = 0		0			1				84		
	CI = 1		84			83				0		
	Pixel		P0	P1	P2	P3	P4	P5		P252	P253	P254
	Data Line											
			D7'1,0 D6'1,0 D5'1,0 D4'1,0 D3'1,0	D7'2,0 D6'2,0 D5'2,0 D4'2,0 D3'2,0	D7'3,0 D6'3,0 D5'3,0 D4'3,0 D3'3,0	D7'1,1 D6'1,1 D5'1,1 D4'1,1 D3'1,1	D7'2,1 D6'2,1 D5'2,1 D4'2,1 D3'2,1	D7'3,1 D6'3,1 D5'3,1 D4'3,1 D3'3,1		D7'1,84 D6'1,84 D5'1,84 D4'1,84 D3'1,84	D7'2,84 D6'2,84 D5'2,84 D4'2,84 D3'2,84	D7'3,84 D6'3,84 D5'3,84 D4'3,84 D3'3,84
Block	LI = 0	LI = 1										
0	0	159										
	1	158										
	2	157										
	3	156										
1	4	155										
	5	154										
	6	153										
	7	152										
2	8	151										
	9	150										
38	152	7										
	153	6										
	154	5										
	155	4										
39	156	3										
	157	2										
	158	1										
	159	0										
SEGout			0	1	2	3	4	5		252	253	254

7.3.2 Line Address Control Circuit

This circuit is to control the address in the line direction when MPU accesses the DDRAM or read the DDRAM to display image on the LCD.

You can specify a range of the line address with line address set command. When the line-direction scan is specified with DATACTRL command and the address are increased from the start up to the end line, the column address is increased by 1 and the line address returns to the start line.

The DDRAM supports up to 160 lines, and thus the total line becomes 160.

In the READ operation, as the end line is reached, the column address is automatically increased by 1 and the line address returns to the start line.

Users may inverse the correspondence between the DDRAM address and common output via the address normal/inverse parameter of DATACTRL command.

7.3.3 Column Address Control Circuit

This circuit is to control the address in the column direction when MPU accesses the DDRAM. You can specify a range of the column address with column address set command. When the column-direction scan is specified with DATACTRL command and the address are increased from the start up to the end line, the line address is increased by 1 and the column address returns to the start column.

In the READ operation, the column address is also automatically increased by 1 and returns to the start line as the end column is reached.

Just like the line address control circuit, users may inverse the correspondence between the DDRAM column address and segment output via the column address normal/inverse parameter of DATACTRL command. This arrangement makes the chip layout on the LCD module flexible.

7.3.4 I/O Buffer Circuit

It is the bi-directional buffer when MPU reads or writes the DDRAM. Since the READ or WRITE operation of MPU to DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.5 Block Address Circuit

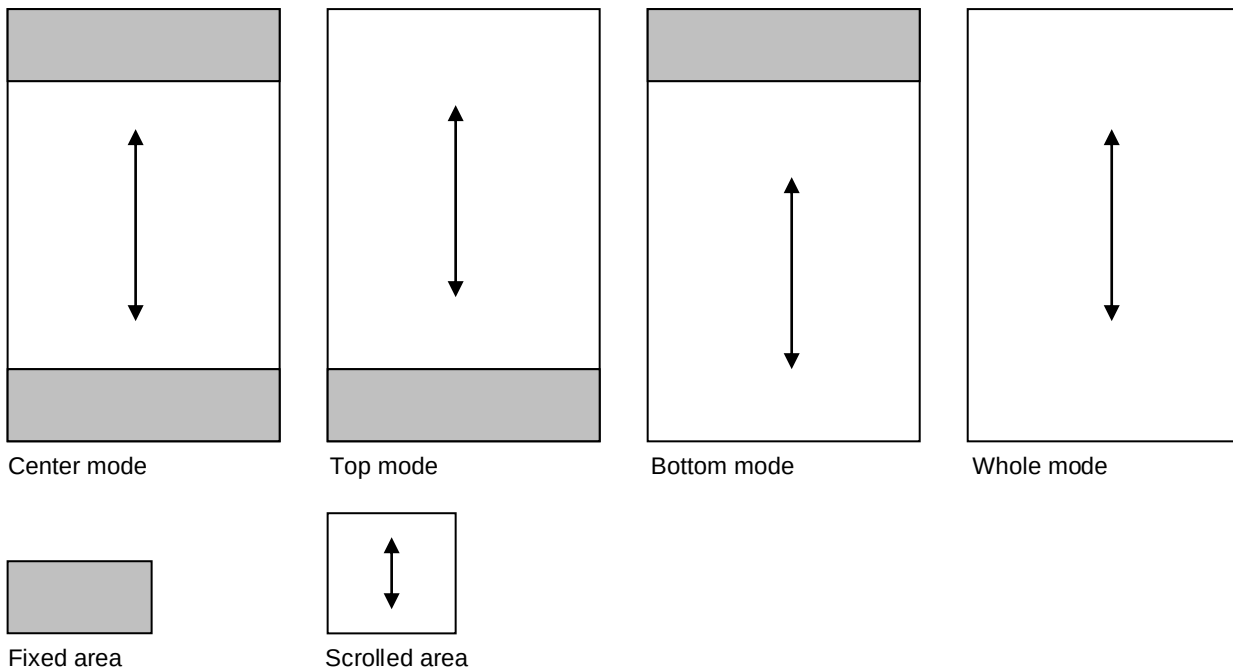
The circuit associates lines on DDRAM with COM output. ST7529A processes signals for the liquid crystal display on 4-line basis. Thus, when specifying a specific area in the area of scroll display or partial display, you must designate it in block.

7.3.6 Display Data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

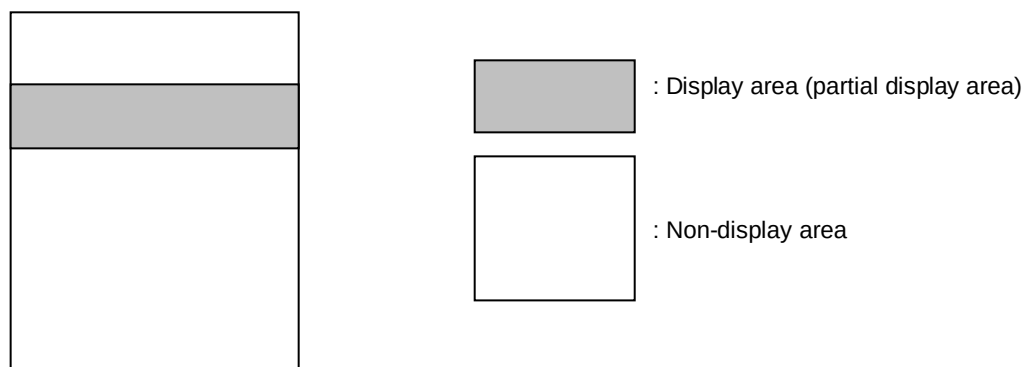
7.4 Area Scroll Display

The user may scroll the display screen partially in any one of the following four scroll patterns via AREA SCROLL SET and SCROLL START SET commands.



7.5 Partial Display

The user may turn on the partial display (division by line) of the screen via PARTIAL IN command. This mode consumes less current than the whole screen display and is suitable for the equipment in the standby state.



If the partial display region is out of the maximum display range, it will be no operation.

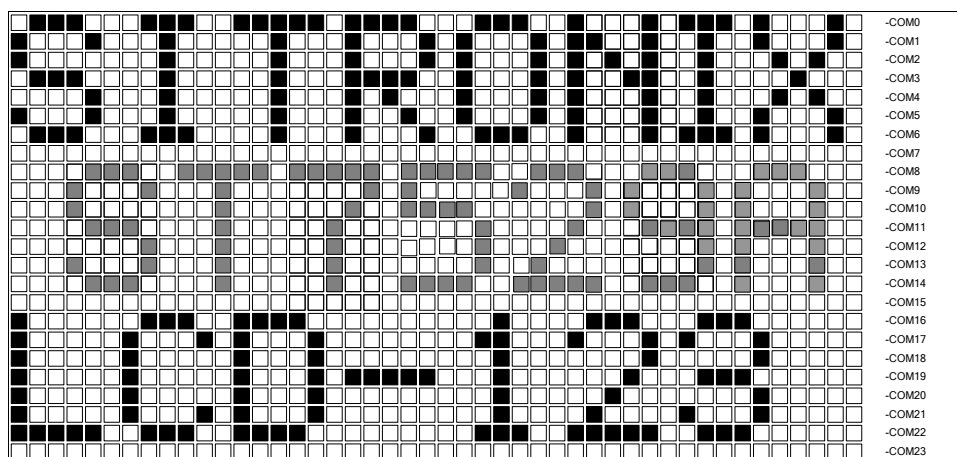


Figure 7.5.1.Reference Example for Partial Display

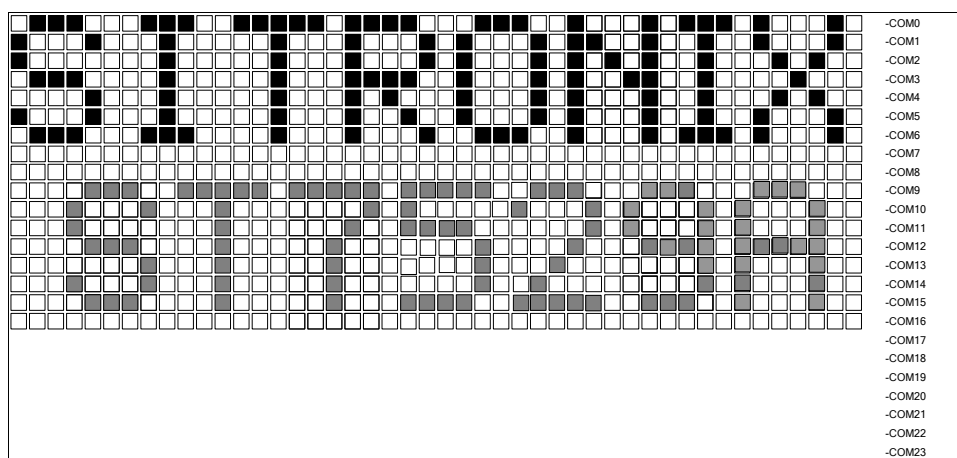


Figure 7.5.2.Partial Display

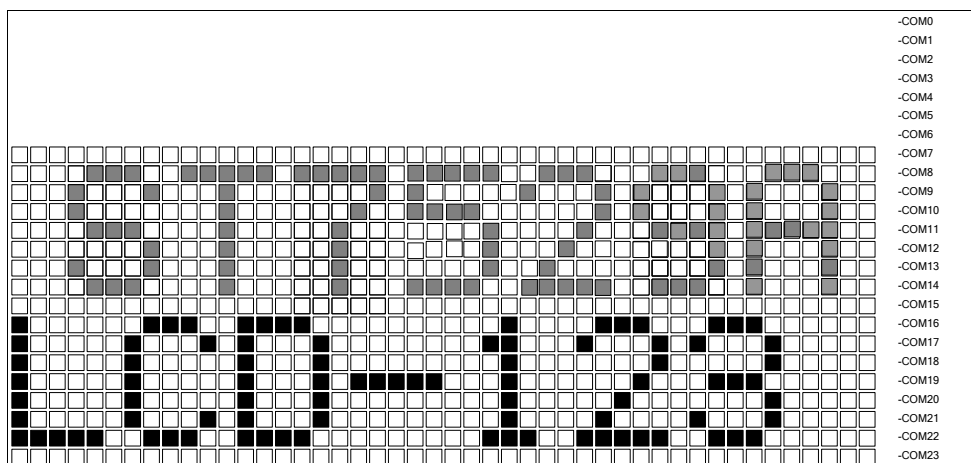


Figure 7.5.3.Moving Display

7.6 Partial Display Application with COMSCN

The relation between display output and different COMSCN setting is shown below. **The partial duty layout must be connected from COM0 to COMx (partial duty).** The following example illustrates partial duty equal to 64 duties. For related setting on COMSCN please refer to Section 6.2 Driver Output Pins.

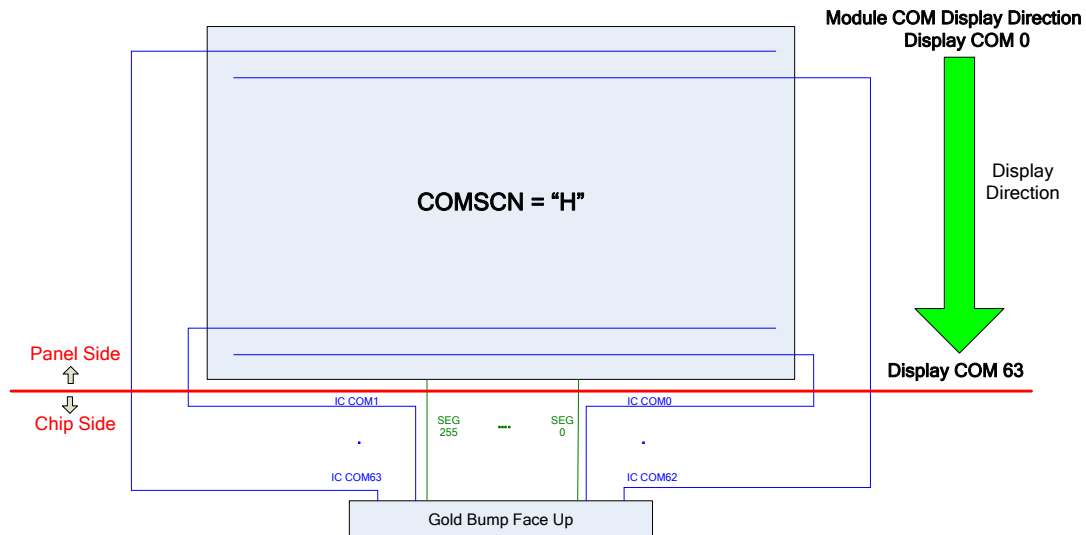


Figure 7.6.1.64 duty and COMSCN = H

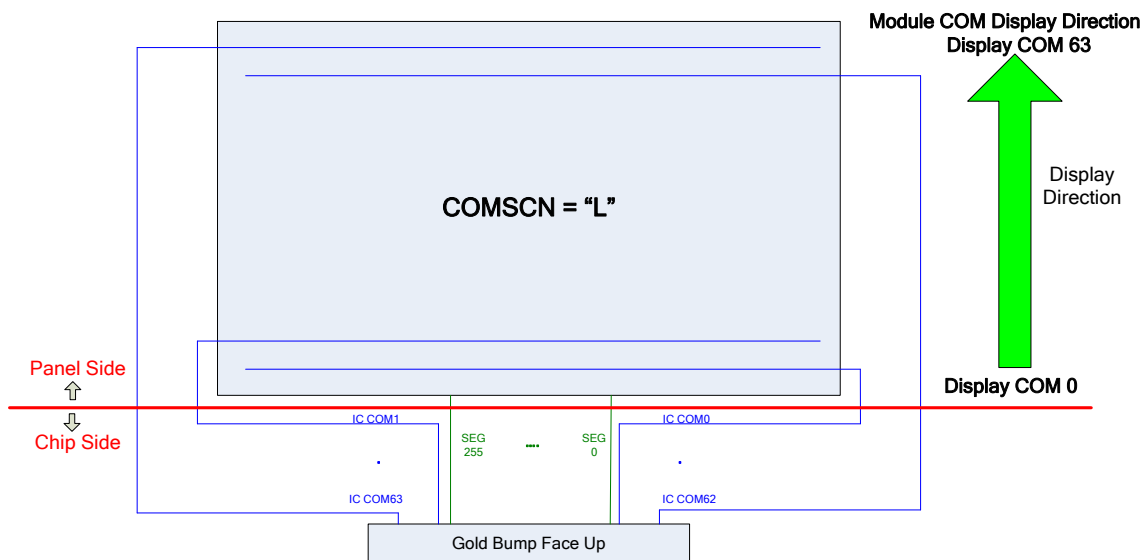


Figure 7.6.2.64 duty and COMSCN = L

7.7 Gray-Scale Display

ST7529A incorporates a 2 FRC & 31 PWM function circuit to display a 32 gray-scale display.

7.8 Oscillation Circuit

This is an on-chip oscillator without external resistor. When the internal oscillator is used, this pin must connect to VDD; when the external oscillator is used, this pin could be an input pin. This oscillator signal is used in the voltage converter and display timing generation circuit.

7.9 Display Timing Generator Circuit

This circuit generates some signals for displaying on LCD. The display clock, CL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 160-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the MPU. The display clock generates an LCD AC signal (M) which enables the LCD driver to make an AC drive waveform. It also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the M by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 7.9.1.

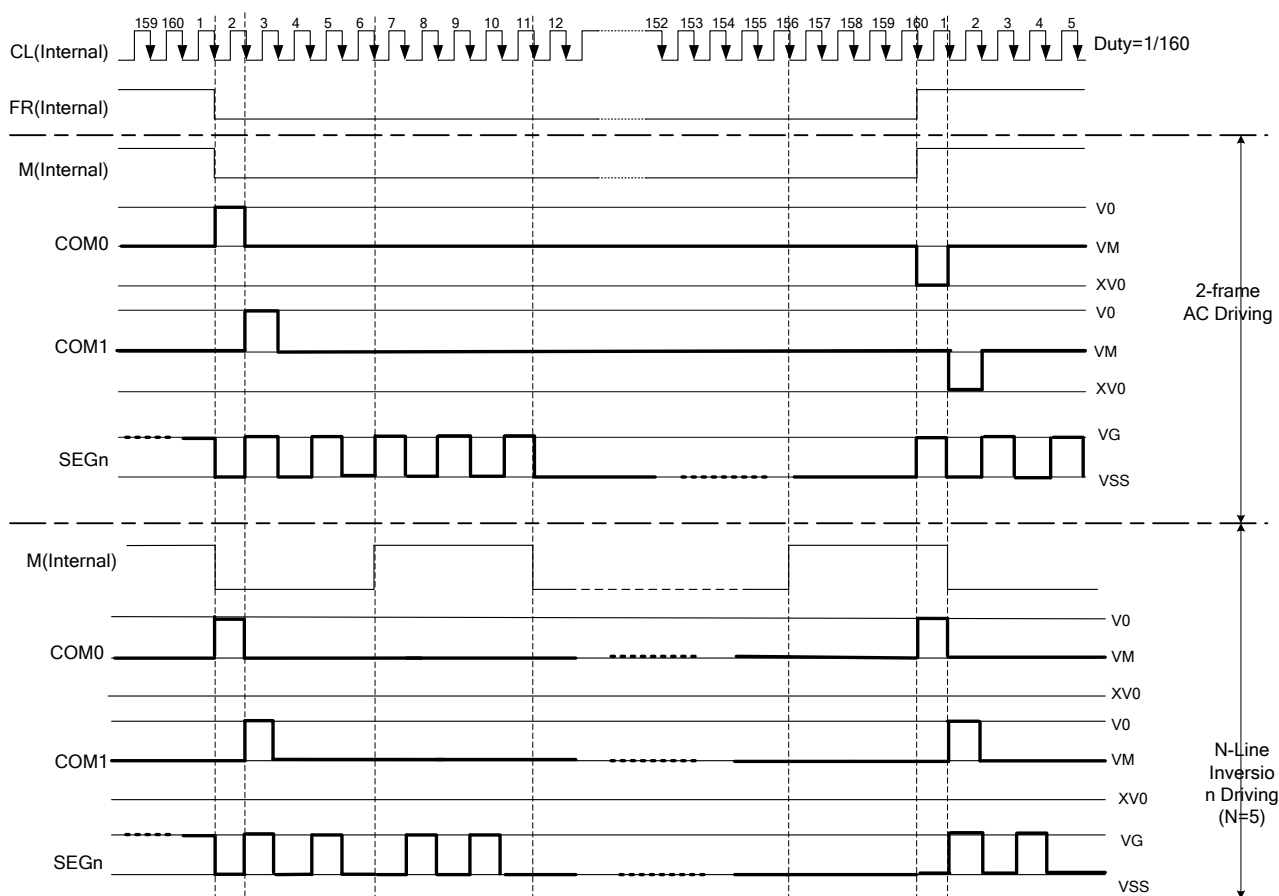
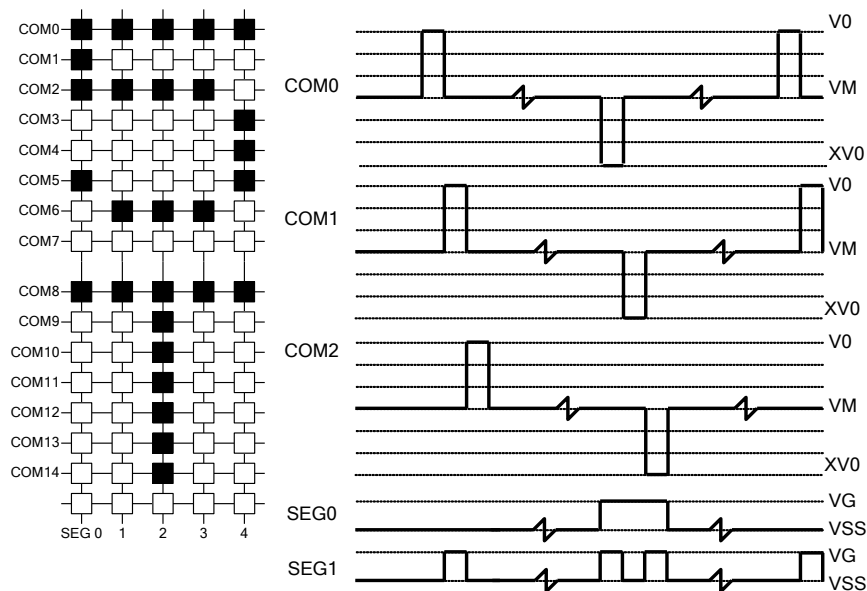


Figure 7.9.1 2-frame AC Driving Waveform (Duty Ratio: 1/160)

7.10 Liquid Crystal drive Circuit

This driver circuit is configured by 160-channel common drivers and 255-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and M signal.



7.11.1 Liquid Crystal Driver Power Circuits

The recommended external power components need only three capacitors. The detailed values of these three capacitors are determined by panel size and loading.

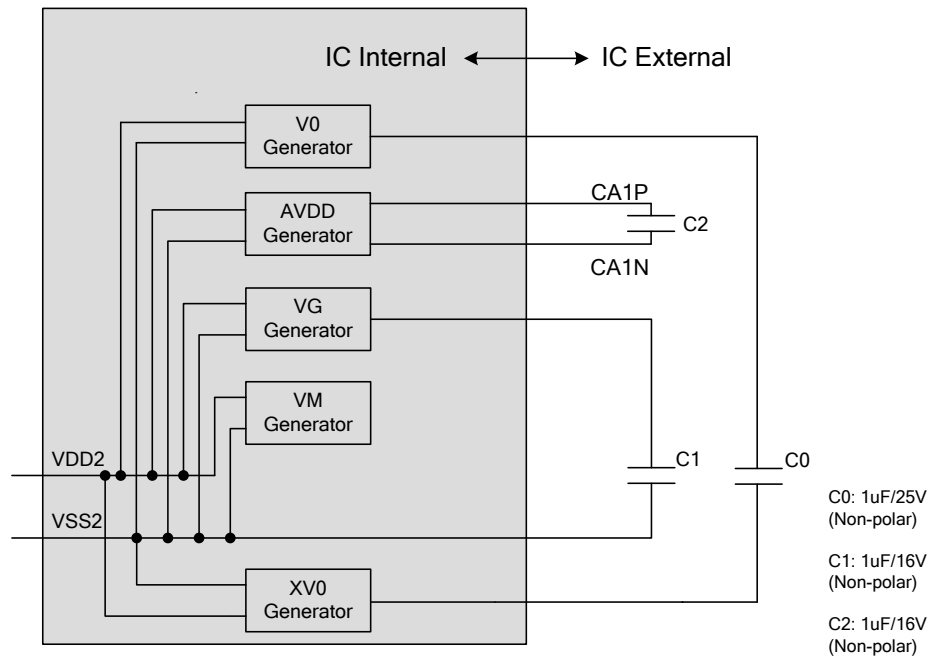


Fig. 7.11.1 Internal Power Supply Circuit

Note:

1. C0: 1uF/25V~2.2uF/25V (Default 1uF/25V)
2. C1: 1uF/16V~2.2uF/16V (Default 1uF/16V)
3. C2: 1uF/16V~2.2uF/16V (Default 1uF/16V)

7.11.2 Voltage Regulator Circuits

SET V_{OP} (SETVOP)

The set V_{OP} function is to program the optimum LCD supply voltage V₀.

SETVOP

Reset state of VPR[8:0] is 257_{DEC} = 13.88V.

The V₀ value is programmed via the VPR[8:0] register.

$$V_0 = a + (VPR[8:6]VPR[5:0]) \times b$$

Ex: VPR[5:0]=000001, VPR[8:6]=100

→ VPR[8:0]=100000001

→ 3.6+257×0.04=13.88

where a is a fixed constant value 3.6, b is a fixed constant value 0.04, VPR[8:0] is the programmed V₀ value with programming range from 85 to 360 (55_{HEX} to 168_{HEX}), and VPR[5:0] is the set contrast value which can be set via the interface and is in two's complement format.(See command VOLUP & VOLDOWN)

The VPR[8:0] value must be in the V₀ programming range as given in Fig.7.11.2. Evaluating equation (1), values outside the programming range indicated in Fig.7.11.2 may result.

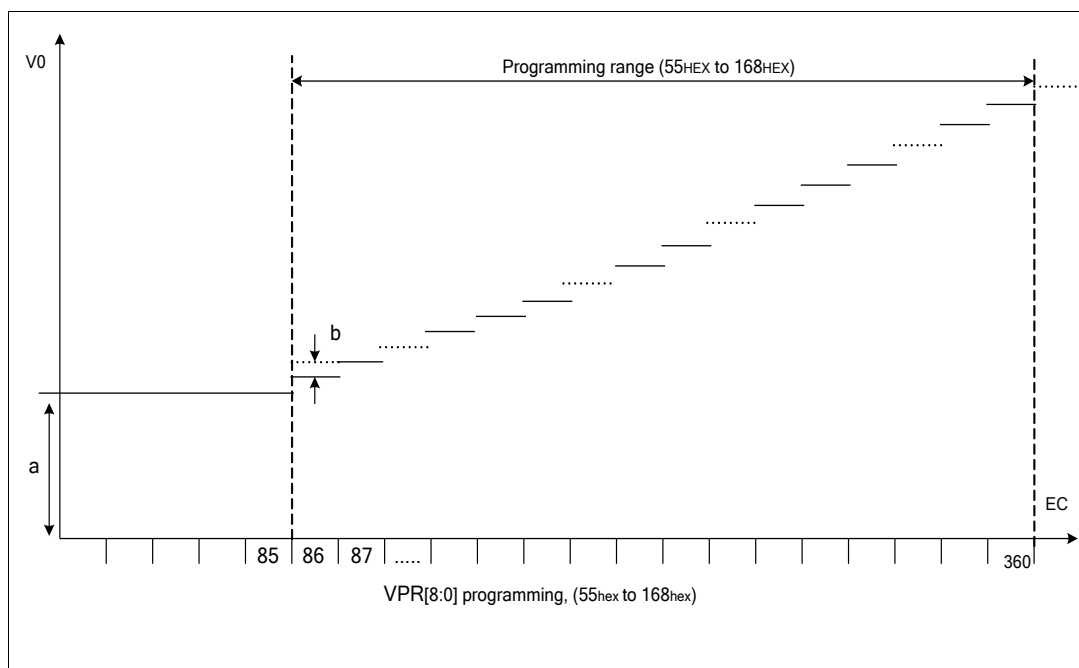


Fig. 7.11.2 V₀ programming range

Although the programming range for the internally generated V₀ allows values above the maximum allowed V₀, the customer has to ensure setting the V_{PR} register and selecting the temperature compensation under all condition and including all tolerances that the maximum allowed V₀ (18V) will never be exceeded.

V0 Restriction

Because VG should larger than 1.8V, V0 value should be higher than $\frac{1.8 \times \text{Bias}}{2} \text{ (V)}$ and lower than 18V. V0 value outside the available range is undefined. User has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that V0 voltage remains in the range.

RESET CIRCUIT
When Power is Turned On

Input power (VDD1~VDD4)



Be sure to apply POWER-ON RESET (RSTB = LOW)


<Display Setting>

Display control (DISCTRL)

Setting clock dividing ratio:

Duty setting:

Setting reverse rotation number of line:

Common scan direction (COMSCN)

Setting scan direction:



Oscillation ON (OSCON)



Sleep-out (SLIPOUT)


<Power Supply Setting>

Electronic volume control (VOLCTRL)

Setting volume value :

Setting built-in resistance value:

Power control (PWRCTR)

Setting operation of power supply circuit:


<Display Setting 2>

Normal rotation of display (DISNOR)/Inversion of display (DISINV): Normal rotation of display

Partial-in (PTLIN)/Partial-out (PTLOUT)

Setting fix area:

Area scroll set (ASSET)

Setting area scroll region:

Setting area scroll type:

Scroll start set (SCSTART)

Setting scroll start address:


<Display Setting 3>

Data control (DATCTRL)

Setting normal rotation/inversion of line address:

Setting normal rotation/inversion of column address:

<<State after resetting>>

2 dividing

1/4

11H reverse rotations

COM0 -> COM79, COM80-> COM159

Oscillation OFF

Sleep-in

<<State after resetting>>

0

0 (3.95)

All OFF

<<State after resetting>>

Partial-out

0

0

Full-screen scroll

0

<<State after resetting>>

Normal rotation

Normal rotation

Setting direction of address scanner:

Column direction



<RAM Setting>

<<State after resetting>>

Line address set (LASET)

Setting start line address:

0

Setting end line address:

0

Column address set (CASET)

Setting start column address:

0

Setting end column address:

0



<RAM Write>

<<State after resetting>>

Memory write command (RAMWR)

Writing displayed data: Repeat as many as the number needed and exit by entering other command.



<Waiting (approximately 100ms)>

Wait until the power supply voltage has stabilized.

Enter the command of power supply control first, and then wait at least 100ms before entering the display ON command when the built-in power supply circuit operates.

If you do not wait, an unexpected display may appear on the liquid crystal panel.



DISPLAY ON (DISON):

DISPLAY OFF

*1: When the IC is in SLEEP IN state, the liquid crystal drive power supply, the boosting power output, and GND pin are connected together, therefore, the SLEEP OUT command must be entered to cancel the SLEEP state prior to turning on the built-in circuit.

(Note) If changes are unnecessary after resetting, command input is unnecessary.

8. COMMANDS

8.1 Command table

Ext=0 or Ext=1 or Ext=2

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	Ext 0	0	1	0	0	0	1	1	0	0	0	0	Ext=0 Set	30	None
2	Ext 1	0	1	0	0	0	1	1	0	0	0	1	Ext=1 Set	31	None
3	Ext 2	0	1	0	0	0	1	1	1	0	0	1	Ext=2 Set	39	None

Ext=0

Index	Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	DISON	0	1	0	1	0	1	0	1	1	1	1	Display On	AF	None
2	DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display Off	AE	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	1	Normal Display	A7	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	0	Inverse Display	A6	None
5	DISCTRL	0	1	0	1	1	0	0	1	0	1	0	Display Control	CA	3 bytes
6	SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep In	95	None
7	SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep Out	94	None
8	LASET	0	1	0	0	1	1	1	0	1	0	1	Line Address Set	75	2 bytes
9	CASET	0	1	0	0	0	0	1	0	1	0	1	Column Address Set	15	2 bytes
10	DATSDR	0	1	0	1	0	1	1	1	1	0	0	Data Scan Direction	BC	1 byte
11	RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to Memory	5C	Data
12	RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from Memory	5D	Data
13	PTLIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2 bytes
14	PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None
15	RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read and Modify Write	E0	None
16	RMWOUT	0	1	0	1	1	1	0	1	1	1	0	RMW end	EE	None
17	ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area Scroll Set	AA	4 bytes
18	SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll Start Set	AB	1 byte
19	OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal OSC on	D1	None
20	OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal OSC off	D2	None
21	PWRCTRL	0	1	0	0	0	1	0	0	0	0	0	Power Control	20	1 byte
22	VOLCTRL	0	1	0	1	0	0	0	0	0	0	1	EC control	81	2 bytes
23	VOLUP	0	1	0	1	1	0	1	0	1	1	0	EC increase 1	D6	None
24	VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	EC decrease 1	D7	None
25	RESERVED	0	1	0	1	0	0	0	0	0	1	0	Not Use	82	0
26	EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	READ Register1	7C	None

27	EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	READ Register2	7D	None
28	NOP	0	1	0	0	0	1	0	0	1	0	1	NOP Instruction	25	None
29	STREAD	0	0	1	Read Data								Status Read		

Ext=1

<i>Index</i>	<i>Command</i>	<i>A0</i>	<i>RD</i>	<i>WR</i>	<i>D7</i>	<i>D6</i>	<i>D5</i>	<i>D4</i>	<i>D3</i>	<i>D2</i>	<i>D1</i>	<i>D0</i>	<i>Function</i>	<i>Hex</i>	<i>Parameter</i>
1	Gray 1 Set	0	1	0	0	0	1	0	0	0	0	0	FRAME 1 Gray PWM Set	20	16 bytes
2	Gray 2 Set	0	1	0	0	0	1	0	0	0	0	1	FRAME 2 Gray PWM Set	21	16 bytes
3	ANASET	0	1	0	0	0	1	1	0	0	1	0	Analog Circuit Set	32	3 bytes
4	XARD	0	1	0	1	1	0	1	0	1	1	1	OTP Auto Read	D7	1 byte
5	XWRDC	0	1	0	1	1	1	0	0	0	0	0	OTP WR/RD Control	E0	1 byte
6	XCTRL	0	1	0	1	1	1	0	0	0	0	1	OTP Control Out	E1	None
7	XWR	0	1	0	1	1	1	0	0	0	1	0	OTP Write	E2	None
8	XRD	0	1	0	1	1	1	0	0	0	1	1	OTP Read	E3	None
9	XSC	0	1	0	1	1	1	0	0	1	0	0	OTP Selection Control	E4	1 byte
10	XPS	0	1	0	1	1	1	0	0	1	0	1	OTP Programming Setting	E5	1 byte

Ext=2

<i>Index</i>	<i>Command</i>	<i>A0</i>	<i>RD</i>	<i>WR</i>	<i>D7</i>	<i>D6</i>	<i>D5</i>	<i>D4</i>	<i>D3</i>	<i>D2</i>	<i>D1</i>	<i>D0</i>	<i>Function</i>	<i>Hex</i>	<i>Parameter</i>
1	EOTP	0	1	0	1	1	0	1	0	1	1	0	Enable OTP	D6	1 byte

EXT= "0" or "1" or "2"

(1) Extension instruction 0 (EXT0) - Parameter Byte: None (30H)

Use the "EXT=0" command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	0

(2) Extension instruction 1 (EXT1) - Parameter Byte: None (31H)

Use the "EXT=1" command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	0	0	0	1

(3) Extension instruction 2 (EXT2) - Parameter Byte: None (39H)

Use the "EXT=2" command table

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	1	1	0	0	1

EXT= "0"

(1) Display ON (DISON) - Parameter Byte: None (AFH)

It is to turn the display on. When the display is turned on, segment and common outputs are generated at the level corresponding to the display data and display timing. As long as the sleep mode is selected, the display cannot be turned on. Thus, whenever using this command, the sleep mode must be cancelled first.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) - Parameter Byte: None (AEH)

It is to forcibly turn the display off. As long as the display is turned off, every segment and common outputs are forced to VSS level.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) - Parameter Byte: None (A7H)

It is to normally highlight the display area without modifying contents of the display data RAM.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(4) Inverse display (DISINV) - Parameter Byte: None (A6H)

It is to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(5) Display control (DISCTRL) - Parameter Byte: 3 (CAH)

This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Do not change this command while the display is turned on.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	
Parameter Byte 1 (PB1)	1	1	0	*	*	*	0	0	CLD	0	0	CL dividing ratio, F1 and F2 drive pattern.
Parameter Byte 2 (PB2)	1	1	0	*	*	DT5	DT4	DT3	DT2	DT1	DT0	Drive duty

PB1 specifies the CL dividing ratio.

CLD: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

CLD=0: not divide, CLD=1: 2 divisions.

PB2 specifies the duty of the module on block basis. Initial: 00H

$(\text{Numbers of display lines})/4-1 = DT5 \times 2^5 + DT4 \times 2^4 + DT3 \times 2^3 + DT2 \times 2^2 + DT1 \times 2^1 + DT0 \times 2^0$

For example, 1/128 duty $\rightarrow 128/4-1=31 \rightarrow (DT5, DT4, DT3, DT2, DT1, DT0) = (0, 1, 1, 1, 1, 1)$

(6) Sleep in (SLPIN) - Parameter Byte: None (95H)

This command is to enter the SLEEP MODE.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

(7) Sleep out (SLPOUT) - Parameter Byte: None (94H)

This command is to exit the SLEEP MODE.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(8) Line address set (LASET) - Parameter Byte: 2 (75H)

This command is to specify the line address area when MPU makes access to the display data RAM. As the addresses are increased from the start to the end line in the line-direction scan, the column address is increased by 1 and the line address return to the start line. Note that the start and end line must be a pair. Moreover, the relation "start line < end line" must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	—
Parameter Byte 1 (PB1)	1	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	Start Line
Parameter Byte 2 (PB2)	1	1	0	EL7	EL6	EL5	EL4	EL3	EL2	EL1	EL0	End Line

Note: The range of line address is 0 ~ 159.

(9) Column address set (CASET) - Parameter Byte: 2 (15H)

This command is to specify the column address area when MPU makes access to the display data RAM. As the addresses are increased from the start to the end column in the column-direction scan, the line address is incremented by 1 and the column address is returned to the start column. Note that the start and end line must be a pair. Moreover, the relation “start column < end column” must be maintained.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	—
Parameter Byte 1 (PB1)	1	1	0	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Start Column
Parameter Byte 2 (PB2)	1	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	End Column

Note: The range of column address is 0 ~ 84.

(10) Data scan direction (DATSDR) - Parameter Byte: 1 (BCH)

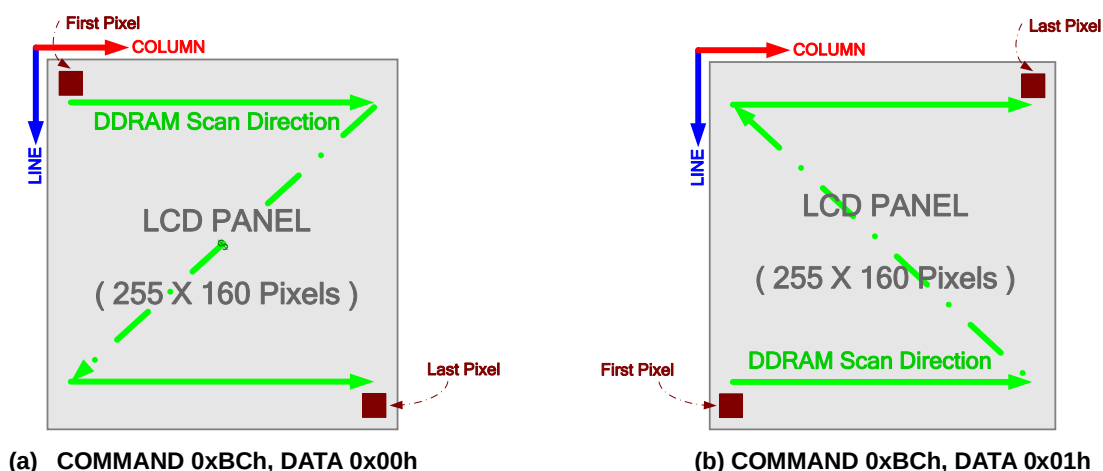
This command is to setup various parameters in the operations of display data stored on the built-in RAM by MPU.

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	—
Parameter Byte 1 (PB1)	1	1	0	*	*	*	*	*	0	CI	LI	Normal/inverse display of address and address scan direction.

This command is to specify the normal/inverse display of the line and column address and the address scanning direction.

LI: Normal/inverse direction of the line address. LI =0: Normal, LI =1: Inverse

CI: Normal/reverse direction of the column address. CI =0: Normal, CI =1: Reverse



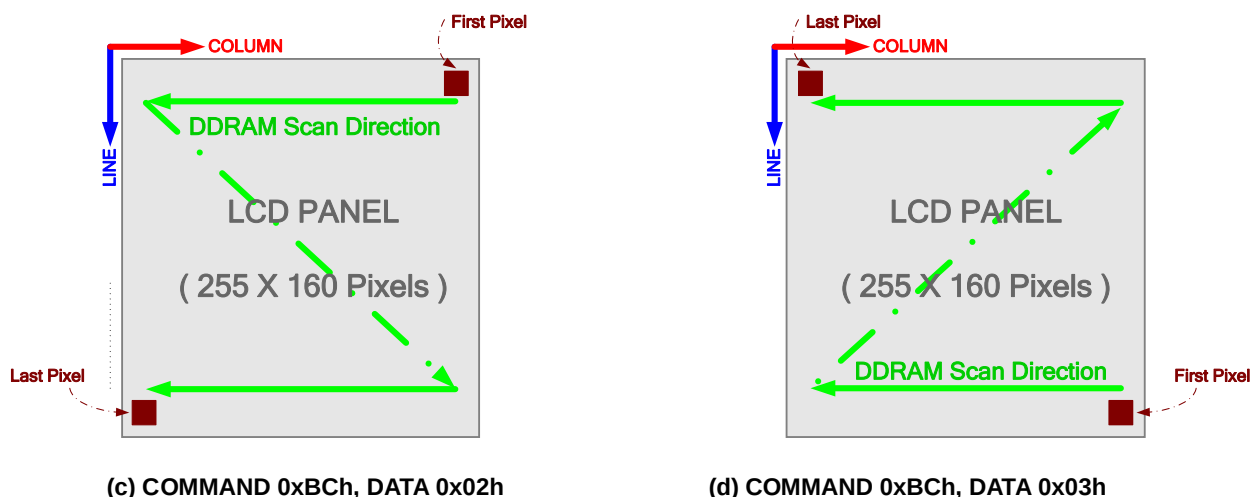


Figure 8.1.1 Different RAM accessing setup under COMMAND 0xBCh

- (a) DATA 0x00h (CI=0, LI=0)
- (b) DATA 0x01h (CI=0, LI=1)
- (c) DATA 0x02h (CI=1, LI=0)
- (d) DATA 0x03h (CI=1, LI=1)

(11) Memory write (RAMWR) - Parameter Byte: Numbers of data written (5CH)

This command turns on the data entry mode when MPU writes data to the display memory. This command will always sets the line and column address at the start address while executed. The following parameter byte rewrites contents of the display data RAM and increases the line or column address automatically. The write mode is automatically cancelled if any other command is entered.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	—
Parameter Byte 1 (PB1)	1	1	0	Data to be written							Data to be written	

(12) Memory read (RAMRD) - Parameter Byte: Numbers of data read (5DH)

This command turns on the data read mode when MPU read data from the display memory. This command will always sets the line and column address at the start address while executed. The contents of the display data RAM will be read in the following parameter byte and increases the line or column address automatically. The data read mode is automatically cancelled if any other command is entered.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	--
Parameter Byte 1 (PB1)	1	0	1	Data to be read							Data to be read	

(13) Partial in (PTLIN) - Parameter Byte: 2 (A8H)

This command is to specify the partial display area. It will turn on partial display of the screen (dividing screen by lines) to save power. Since ST7529A processes the liquid crystal display signal on 4-line basis (block basis), the display and no-display areas are also specified on 4-bit line (block basis).

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	--
Parameter Byte 1 (PB1)	1	1	0	*	*	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	Start block address
Parameter Byte 2 (PB2)	1	1	0	*	*	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	End block address

Only the address of the display block can be specified for the partial display. Do not specify an address not to be displayed when scrolled.

(14) Partial out (PTLOUT) - Parameter Byte: none (A9H)

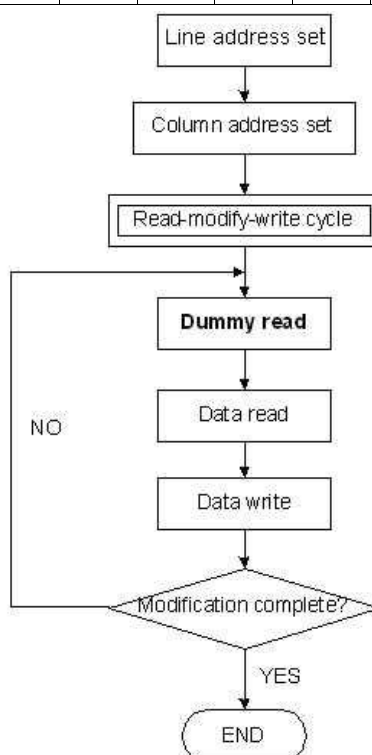
This command is to exit the PARTIAL DISPLAY MODE.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

(15) Read modify write in (RMWIN) - Parameter Byte: none (E0H)

This command is used along with the (8) line address set command (LASET), (9) column address set command (CASET), and (16) read modify write out command (RMWOUT). This function is for frequently modified data on a specific area, such as blinking cursor. First, set a specific display area using the column and line address commands. Then, execute this command to set the column and line addresses as the start address of the specific area. When this operation is complete, the column and line address will not be modified by the display data read command. It is increased only when the display data write command is executed. You can cancel this mode by entering the read modify write out or any other command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0



(16) Read modify write out (RMWOUT) - Parameter Byte: none (EEH)

This command cancels the read modify write mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

(17) Read modify write out (RMWOUT) - Parameter Byte: none (EEH)Area scroll set (ASCSET) - Parameter Byte: 4 (AAH)

It is to scroll only the specified portion of the screen (dividing the screen by lines). This command specifies the scrolling type of area, fixed area and scrolled area.

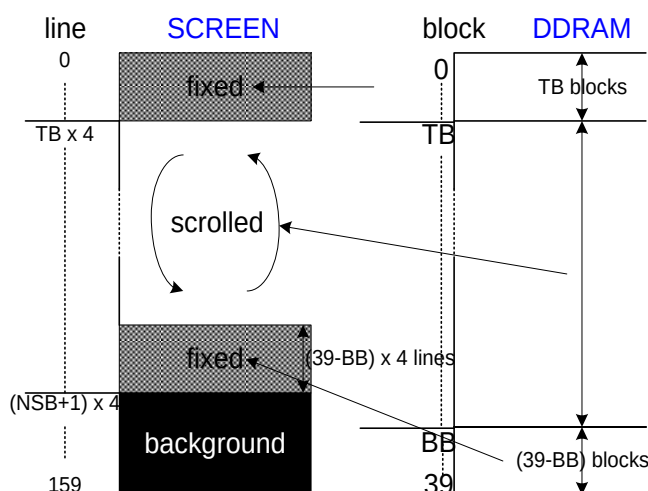
	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	--
Parameter Byte 1 (PB1)	1	1	0	*	*	TB5	TB4	TB3	TB2	TB1	TB0	Top block address
Parameter Byte 2 (PB2)	1	1	0	*	*	BB5	BB4	BB3	BB2	BB1	BB0	Bottom block address
Parameter Byte 3 (PB3)	1	1	0	*	*	NSB5	NSB4	NSB3	NSB2	NSB1	NSB0	Number of specified blocks
Parameter Byte 4 (PB4)	1	1	0	*	*	*	*	*	*	SCM1	SCM0	Area scroll mode

PB4: It is used to specify the scrolling mode.

SCM1	SCM0	Scrolling Mode	Settings		
			Top block address (TB)	Bottom block address (BB)	Number of specified blocks (NSB)
0	0	Center mode	Top(fixed area) height = Top address	Bottom(fixed area) height = 39-Bottom address	Bottom start address = Specified number
0	1	Top mode	0	Bottom(fixed area) height = 39-Bottom address	Bottom start address = Specified number
1	0	Bottom mode	Top(fixed area) height = Top address	39	39
1	1	Whole mode	0	39	39

Since ST7529A processes the liquid crystal display signals on the four-line basis (block basis), fixed and scrolled areas are also specified on the four-line basis (block basis).

DDRAM address of the top fixed area is set in the block address increasing direction starting with the 0th block. DDRAM address of the bottom fixed area is set in the block address decreasing direction starting with 39st block. The DDRAM address of other blocks fixed areas are assigned to the scrolled + background areas.



PB1 is to specify the top block address of the scrolled +

background areas. Specify the 0th block for the top screen scroll or whole screen scroll.

PB2 specifies the bottom address of the scroll + background areas. Specify the 39th block for the bottom or whole screen scroll. The relation that top block address < bottom block address must be maintained.

PB3 specifies a specific number of blocks {Numbers of (Top fixed area + Scroll area) block-1}. In the case of the bottom scroll or whole screen scroll, the value is identical with PB2.

The user can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

(18) Scroll start address set (SCSTART) - Parameter Byte: 1 (ABH)

This command is to specify which line address of DDRAM to be the start line content shown on screen. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	--
Parameter Byte 1 (PB1)	1	1	0	*	*	SB5	SB4	SB3	SB2	SB1	SB0	Start block address

Note : Don't repeat "Area scroll set(AAH)" instruction when "Scroll start address set" is executed.

(19) Internal oscillation on (OSCON) - Parameter Byte: none (D1H)

This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit CLS = HIGH.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(20) Internal oscillation off (OSCOFF) - Parameter Byte: none (D2H)

It turns off the internal oscillation circuit. The circuit is also turned off in the reset mode.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(21) Power control set (PWRCTRL) - Parameter Byte: 1 (20H)

This command is used to turn on or off the Booster circuit, voltage regulator circuit, and reference voltage.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	--
Parameter Byte 1 (PB1)	1	1	0	*	*	*	0	VB	0	VF	VR	LCD drive power

VR turns on/off the reference voltage generation circuit. VR = "1": ON, VR = "0": OFF

VF turns on/off the circuit voltage follower. VF = "1": ON, VF = "0": OFF

VB: It turns on or off the Booster. VB = "1": ON, VB = "0": OFF

(22) Electronic volume control (VOLCTRL) - Parameter Byte: 2 (81H)

The command is used to program the optimum LCD supply voltage Vo. Refer to 7.11.2.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	--
Parameter Byte 1 (PB1)	1	1	0	*	*	VPR5	VPR4	VPR3	VPR2	VPR1	VPR0	VPR[5:0]
Parameter Byte 2 (PB2)	1	1	0	*	*	*	*	*	VPR8	VPR7	VPR6	VPR[8:6]

With the VOLUP and VOLDOWN command the VOP voltage and therewith the contrast of the LCD can be adjusted.

(23) Increment electronic control (VOLUP) - Parameter Byte: none (D6H)

This command increments electronic control offset value of voltage regulator (Vop) circuit by 1. Each step is 0.04V.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the electronic control value to 111111, the control value is set to 000000 after this command has been executed.

(24) Decrement electronic control (VOLDOWN) - Parameter Byte: none (D7H)

This command decrements electronic control offset value of voltage regulator (Vop) circuit by 1. Each step is 0.04V.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the electronic control value to 000000, the control value is set to 111111 after this command has been executed.

(25) Reserved (82H)

Do not use this command.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	0	0	0	1	0

(26) Read Register 1 (EPSRRD1) Command: 1 Parameter Byte: none (7CH)

Execute the EPSRRD1 and STREAD (Status Read) commands in succession to read the Electronic Control value.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Execute the Status Read command immediately after this command and execute the NOP command after the STREAD (Status Read) command.

(27) Read Register 2 (EPSRRD2) Command: 1 Parameter Byte: none (7DH)

Execute the EPSRRD2 and STREAD (Status Read) commands in succession to read the built-in resistance ratio.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Execute the Status Read command immediately after this command and execute the NOP(Reset) command after the STREAD (Status Read) command.

(28) Non-operating (NOP) - Parameter Byte: none (25H)

This command does not affect the operation but has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and so on.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

(29) Status read (STREAD) - Parameter Byte: none

The command is to read the internal condition of the IC. One status can be displayed depending on the setting status after reset or after NOP operation.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	Status data							

D7: Area scroll mode Refer to SCM1 (ASCSET)

D6: Area scroll mode Refer to SCM0 (ASCSET)

D5: RMW on/off 0 : Out 1 : In

D4: Scan direction 0 : Column 1 : Line

D3: Display ON/OFF 0 : OFF 1 : ON

D2: OTP access 0: OutAccess 1: InAccess

D1: Display normal/inverse 0 : Inverse 1 : Normal

D0: Partial display 0 : OFF 1 : ON

EXT="1"

The ST7529A applies 16-gray level and 2 FRC to achieve 32-gray scale display. Every gray level is in the strength controlled by 31-PWM (5-bit). The following 2 commands are to set the gray scale value.

(1) Set Gray 1 value (Gray 1 set) - Parameter Byte: 16 (20H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Gray1 Set	0	1	0	0	0	1	0	0	0	0	0	ODD FRAME Gray PWM Set
Parameter Byte 1 (PB1)	1	1	0	*	*	*	G0F14	G0F13	G0F12	G0F11	G0F10	Set Gray level 0 at odd frames
Parameter Byte 2 (PB2)	1	1	0	*	*	*	G1F14	G1F13	G1F12	G1F11	G1F10	Set Gray level 1 at odd frames
Parameter Byte 14 (PB14)	1	1	0	*	*	*	G13F14	G13F13	G13F12	G13F11	G13F10	Set Gray level 13 at odd frames
Parameter Byte 16 (PB16)	1	1	0	*	*	*	G15F14	G15F13	G15F12	G15F11	G15F10	Set Gray level 15 at odd frames

(2) Set Gray 2 value (Gray 2 set) - Parameter Byte: 16 (21H)

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Gray1 Set	0	1	0	0	0	1	0	0	0	0	1	EVEN FRAME Gray PWM Set
Parameter Byte 1 (PB1)	1	1	0	*	*	*	G0F24	G0F23	G0F22	G0F21	G0F20	Set Gray level 0 at even frames
Parameter Byte 2 (PB2)	1	1	0	*	*	*	G1F24	G1F23	G1F22	G1F21	G1F20	Set Gray level 1 at even frames
Parameter Byte 14 (PB14)	1	1	0	*	*	*	G13F24	G13F23	G13F22	G13F21	G13F20	Set Gray level 13 at even frames
Parameter Byte 16 (PB16)	1	1	0	*	*	*	G15F24	G15F23	G15F22	G15F21	G15F20	Set Gray level 15 at even frames

(3) Analog circuit set (ANASET) – Parameter Byte: 3 (32H)

	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	1	0	0	1	0	—
Parameter Byte 1 (PB1)	1	1	0	*	*	*	*	*	FR2	FR1	FR0	Frame Rate Adjustment
Parameter Byte 2 (PB2)	1	1	0	*	*	*	*	*	*	BE1	BE0	Booster Efficiency Set
Parameter Byte 3 (PB3)	1	1	0	*	*	*	*	*	BS2	BS1	BS0	Bias setting

PB1: Frame rate adjustment

FR2	FR1	FR0	Frame Rate (Hz)
0	0	0	76 (default)
0	0	1	80
0	1	0	90.5
0	1	1	95.5
1	0	0	105
1	0	1	135.5
1	1	0	144.5
1	1	1	153

The frame rate table is used for only 160 duty, If the number of duty is changed, the frame rate will be different also.

PB2: Booster Efficiency set

BE1	BE0	Frequency on booster capacitors
0	0	Level1
0	1	Level2 (Default)
1	0	Level3
1	1	Level4

PB3: Select LCD bias ratio of the voltage required for driving the LCD.

BS2	BS1	BS0	LCD bias
0	0	0	1/14
0	0	1	1/13
0	1	0	1/12
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9

(4) OTP Auto Read (XARD) - Parameter Byte: 1 (D7H)

This instruction is used to set status of OTP auto read to enable or disable.

XARD=0; Enable Auto Read (Default)

XARD=1; Disable Auto Read

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1
Parameter Byte 1 (PB1)	1	1	0	1	0	0	XARD	1	1	1	1

(5) OTP WR/RD Control (XWRDC) - Parameter Byte: 1 (E0H)

This instruction is used to set status of OTP that write to OTP or read from OTP.

WR/RD=0; Enable OTP Read (Default)

WR/RD =1; Disable OTP Read

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0
Parameter Byte 1 (PB1)	1	1	0	0	0	WR/RD	0	0	0	0	0

(6) OTP Control Out (XCTRL) - Parameter Byte: None (E1H)

This instruction is used to cancel the OTP control.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	1

(7) OTP Write (XWR) - Parameter Byte: None (E2H)

This instruction is used to trigger OTP programming procedure.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	1	0

(8) OTP Read (XRD) - Parameter Byte: None (E3H)

This instruction is used to trigger OTP programming procedure.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	1	1

(9) OTP Selection Control (XCS) - Parameter Byte: 1 (E4H)

This instruction is used to define OTP selection control.

Ctrl =0; Enable OTP Selection (Default)

Ctrl =1; Disable OTP Selection

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	1	0	0
Parameter Byte 1 (PB1)	1	1	0	1	Ctrl	0	1	1	0	0	1

(10) OTP Programming Setting (XPS) - Parameter Byte: 1 (E5H)

This instruction is used to set OTP write timing.

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	1	0	1
Parameter Byte 1 (PB1)	1	1	0	0	0	0	0	1	1	1	1

EXT= " 2 "
(1) Enable OTP (EOTP) - Parameter Byte: 1 (D6H)

This instruction is used to disable/enable OTP programming.

EOTP =0; Disable OTP (Default)

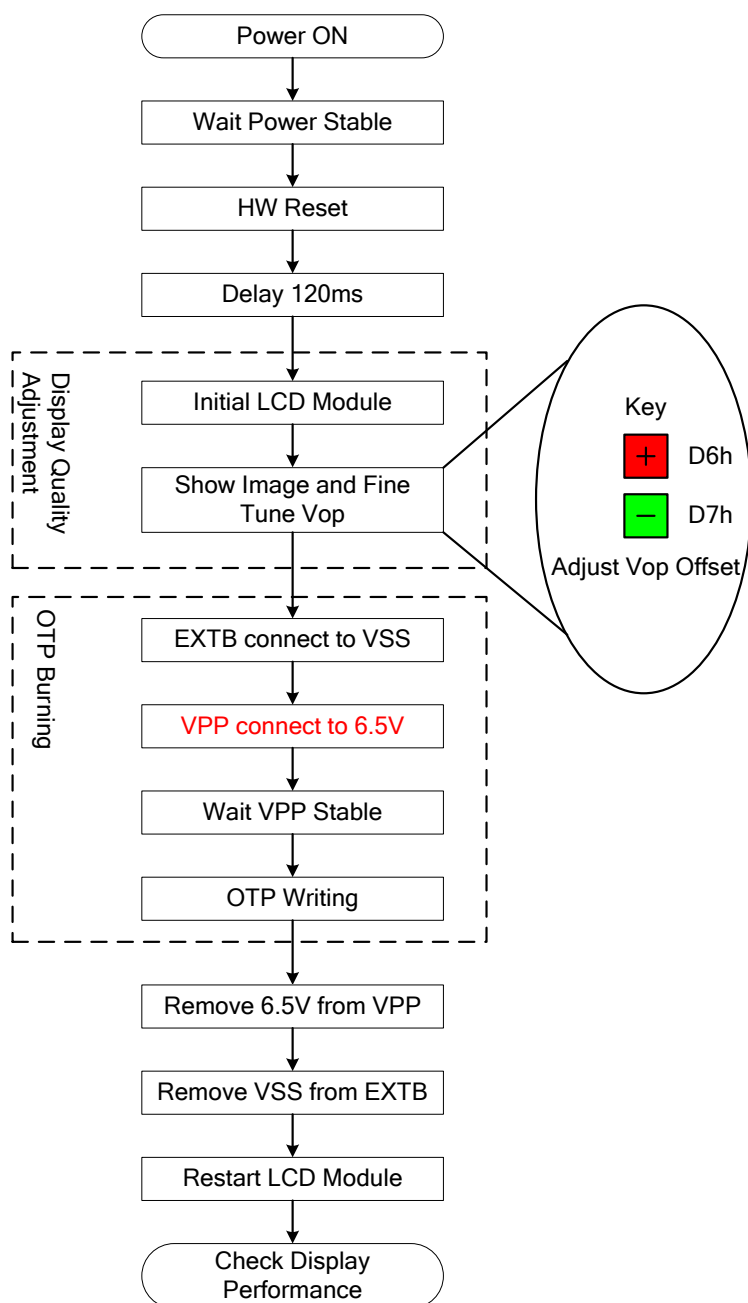
EOTP =1; Enable OTP

	A0	RD	RW	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0
Parameter Byte 1 (PB1)	1	1	0	0	0	0	EOTP	0	0	0	0

8.2 Referential Instruction Setup Flow

8.2.1 OTP Burning Flow

The ST7529A provide the Write and Read function to write the Electronic Control value into and read them from the built-in OTP. Using the Write and Read functions, you can store these values appropriate to each LCD panel. This function is very convenient for user in setting from some different panel's voltage. But using this function must attention the setting procedure. Please see the following diagram.



Note:

In this section “+” and “-” key button, please execute command D6h to increase one step at Vop and execute command D7h to decrease one step at Vop.

Vop Fine Tune Operation

```
void Vop_Fine_Tune( void )
{
    Disp_Image();                // Display the image
    Write( COMMAND, 0x0030 );    // Ext = 0
    Write( COMMAND, 0x00AF );    // Display ON
    Write( COMMAND, 0x00D6 );    // Fine tuning Vop to adjust display quality
    or
    Write( COMMAND, 0x00D7 );

}
```

OTP Write Operation

```
void OTP_Write( void )
{
    Write( COMMAND, 0x0030 );    // Ext = 0
    Write( COMMAND, 0x00AE );    // Display OFF
    Delay( 50ms );              // Delay 50ms

    Write( COMMAND, 0x0039 );    // Ext = 2
    Write( COMMAND, 0x00D6 );    // Enable OTP
    Write( DATA, 0x0010 );
    Write( COMMAND, 0x0031 );    // Ext = 1
    Write( COMMAND, 0x00E4 );    // OTP Selection Control
    Write( DATA, 0x0099 );
    Write( COMMAND, 0x00E5 );    // OTP Programming Setting
    Write( DATA, 0x000F );
    Write( COMMAND, 0x00E0 );    // OTP WR/RD Control
    Write( DATA, 0x0020 );
    Delay( 100ms );             // Waite for OTP Operation ( 100ms )
    Write( COMMAND, 0x00E2 );    // OTP Write
    Delay( 100ms );             // Waite for OTP Operation ( 100ms )
    Write( COMMAND, 0x00E1 );    // OTP Control Out
    Write( COMMAND, 0x0030 );    // Ext = 0

}
```

8.2.2 Initializing with the Built-in Power Supply Circuits

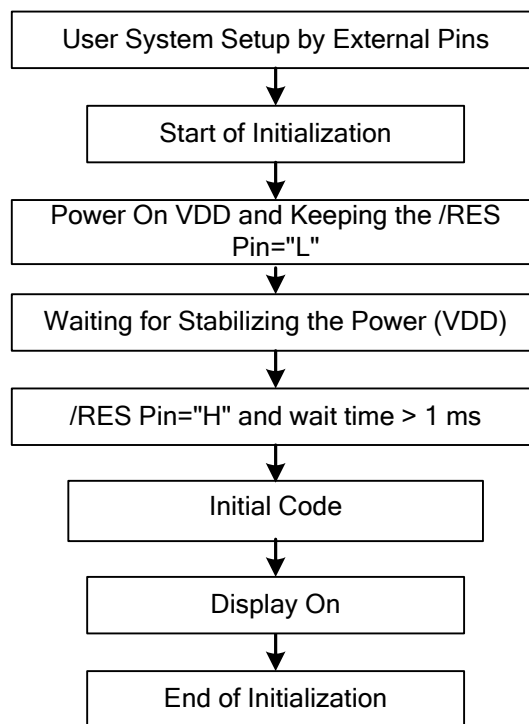
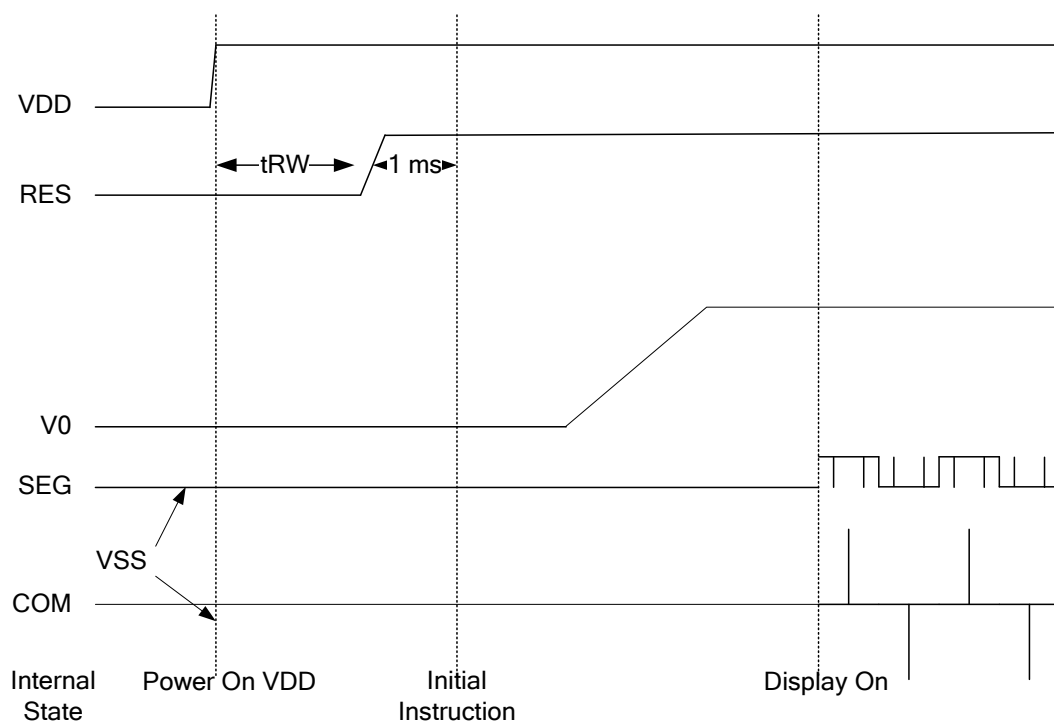


Figure 8.2.2.1 Initializing with the Built-in Power Supply Circuits

When Power-ON (VDDI/VDDA goes from low to high), please follow the sequence shown below. If not, some unpredictable result may occur.



8.2.3 Initial code for 160 duty

```
void ST7529A_Init( void )
```

{	
Write(COMMAND, 0x0030);	//Ext = 0
Write(COMMAND, 0x0094);	//Sleep Out
Write(COMMAND, 0x00D1);	//OSC On
Write(COMMAND, 0x0020);	//Power Control Set
Write(DATA, 0x0008);	//Booster Must Be On First
Delay(1ms);	
Write(COMMAND, 0x0020);	//Power Control Set
Write(DATA, 0x000B);	//Booster, Regulator, Follower ON
Write(COMMAND, 0x0081);	//Electronic Control
Write(DATA, 0x0004);	//Vop=14.0V
Write(DATA, 0x0004);	
Write(COMMAND, 0x00CA);	//Display Control
Write(DATA, 0x0000);	//CL=X1
Write(DATA, 0x0027);	//Duty=160
Write(DATA, 0x0000);	//FR Inverse-Set Value
Write(COMMAND, 0x00A7);	// Normal Display
Write(COMMAND, 0x00BC);	//Data Scan Direction
Write(DATA, 0x0000);	//Normal
Write(COMMAND, 0x0075);	//Line Address Set
Write(DATA, 0x0000);	//Start Line=0
Write(DATA, 0x009F);	//End Line =159
Write(COMMAND, 0x0015);	//Column Address Set
Write(DATA, 0x0000);	//Start Column=0
Write(DATA, 0x0054);	//End Column =84
Write(COMMAND, 0x0031);	//Ext = 1
Write(COMMAND, 0x0032);	//Analog Circuit Set
Write(DATA, 0x0000);	//Frame Rate =000 (Default)
Write(DATA, 0x0001);	//Booster Efficiency=01(Default)
Write(DATA, 0x0000);	//Bias=1/14
Write(COMMAND, 0x0030);	//Ext = 0
Write(COMMAND, 0x00AF);	//Display On
}	

NOTE:

1. Microprocessor interface pins should not be floating in any operation mode.

8.2.4 Data Displaying

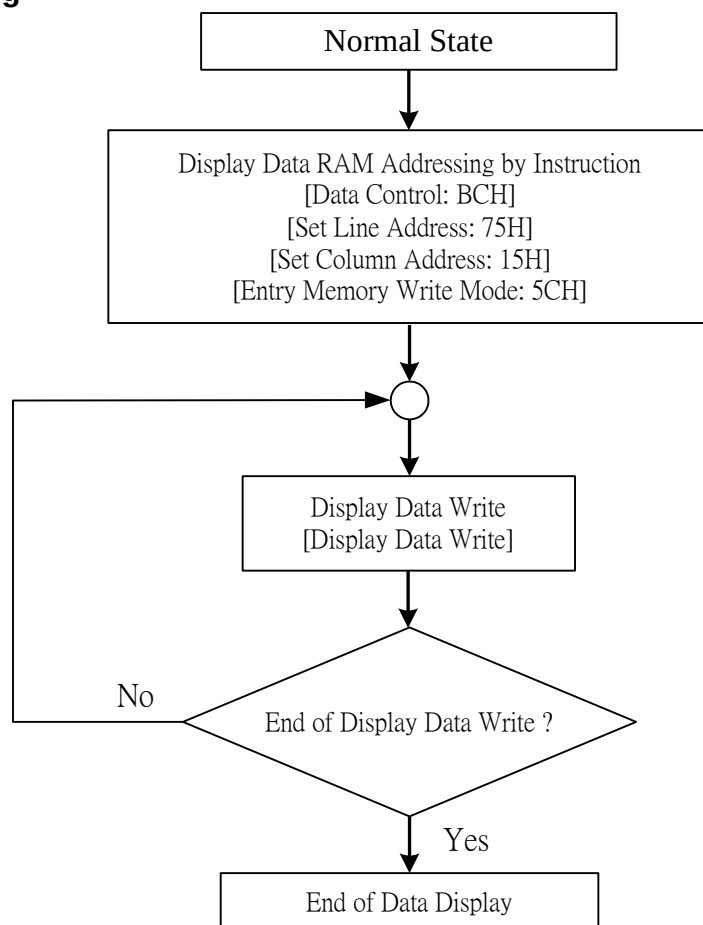


Figure 8.2.4.1 Data Displaying

Example : Display for 255X160

```

void Display( char *pattern )
{
    unsigned char i, j;

    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x0015 );           // Column address set
    Write( DATA, 0x0000 );              // From column0 to column254
    Write( DATA, 0x0054 );
    Write( COMMAND, 0x0075 );           // Page address set
    Write( DATA, 0x0000 );              // From line0 to line159
    Write( DATA, 0x009F );
    Write( COMMAND, 0x005C )            // Entry Memory Write Mode
    for( j = 0; j < 160 ; j++ )
        For( i = 0 ; i < 85 ; i++ )
            Write( DATA, pattern[j * 160 + i] ); // Display Data Write
}
  
```

8.2.5 Partial Display In/Out

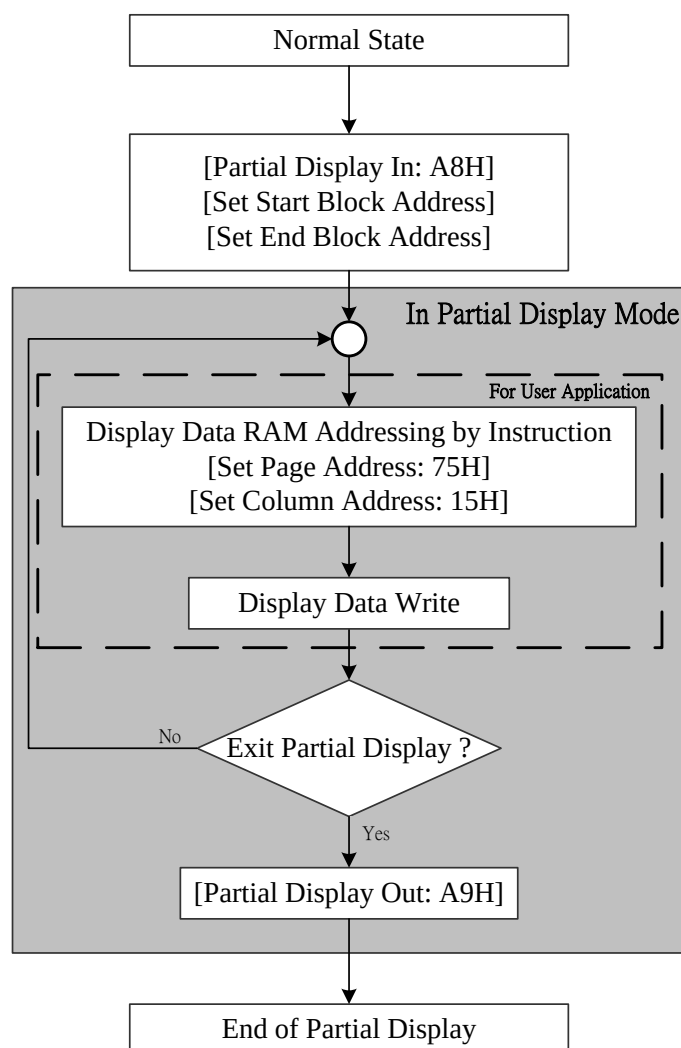


Figure 8.2.5.1 Partial Display In/Out

Example : Partial Display In/Out Operation

void PartialIn(unsigned char start_block, unsigned char end_block)

```

{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00A8 );           // Partial Display In Function
    Write( DATA, start_block );        // Start Block
    Write( DATA, end_block );          // End Block
}
  
```

void PartialOut(void)

```

{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00A9 );           // Partial Display Out Function
}
  
```

```
extern unsigned char *display_pattern;
void main()
{
    PartialIn( 11, 18 );           // entry partial display mode

    Windowing( 0, 11*4, 84, 18*4 ); // set the page and column range
    PartialDisplay( display_pattern ); // Fill the data into partial display area
    .
    .
    .
    PartialOut();                 // Out of partial display mode
}
```

8.2.6 Scroll Display

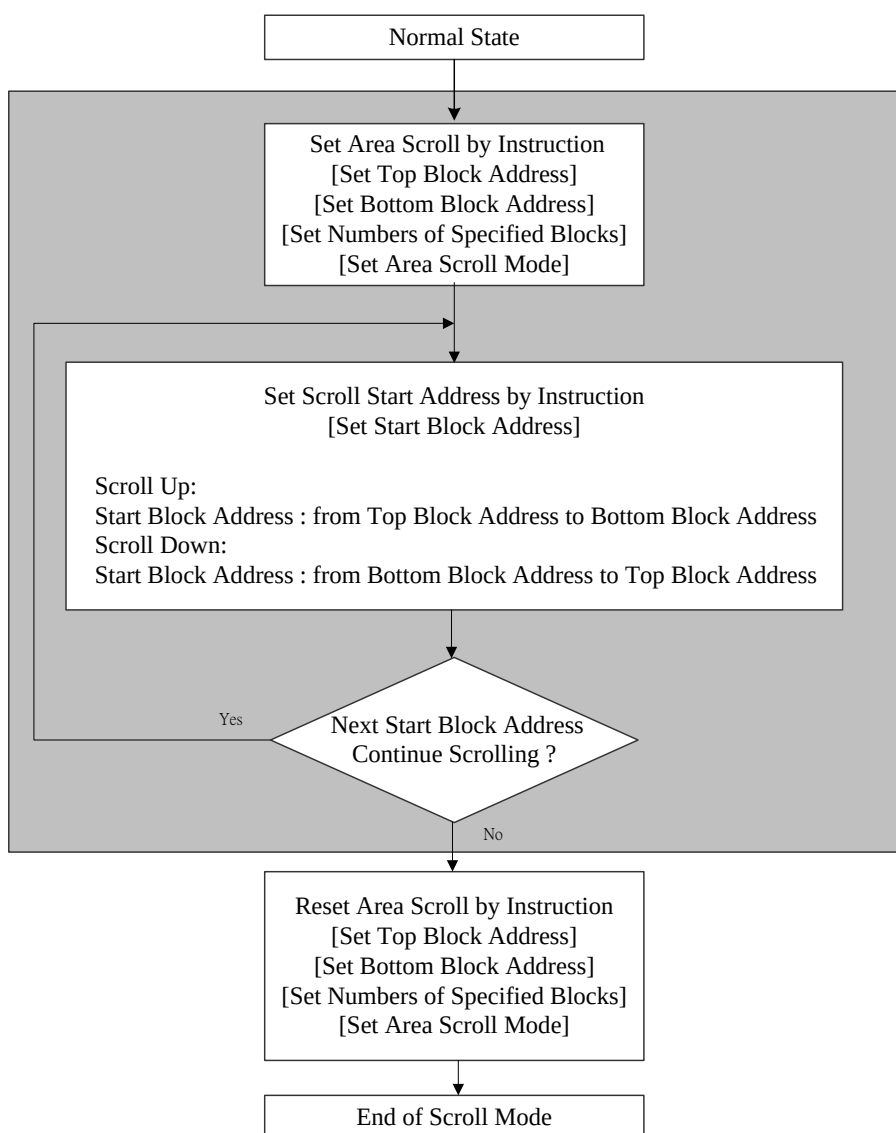


Figure 8.2.6.1 Scroll Display

Example : Screen Scroll Operation

```
void CenterScreenScroll( void )
```

```
{  
  
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA );          // Partial Display In Function  
    Write( DATA, 0x000A );            // Top_Block=10  
    Write( DATA, 0x0014 );            // Bottom_Block=20  
    Write( DATA, 0x0014 );            // Number of Specified Blocks=Bottom_Block=20  
    Write( DATA, 0x0000 );            // Area Scroll Type=Center Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down  
  
}
```

```
void TopScreenScroll( void )
```

```
{  
  
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA );          // Partial Display In Function  
    Write( DATA, 0x0000 );            // Top_Block=0  
    Write( DATA, 0x0014 );            // Bottom_Block=20  
    Write( DATA, 0x0014 );            // Number of Specified Blocks=Bottom_Block=20  
    Write( DATA, 0x0001 );            // Area Scroll Type=Top Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down  
  
}
```

```
void BottomScreenScroll( void )
```

```
{  
  
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA );          // Partial Display In Function  
    Write( DATA, 0x000A );            // Top_Block=10  
    Write( DATA, 0x0019 );            // Bottom_Block=25  
    Write( DATA, 0x0019 );            // Number of Specified Blocks=Bottom_Block=25  
    Write( DATA, 0x0002 );            // Area Scroll Type=Bottom Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down  
  
}
```

```
void WholeScreenScroll( void )
```

```
{  
  
    Write( COMMAND, 0x0030 );           // Ext = 0  
    Write( COMMAND, 0x00AA );          // Partial Display In Function  
    Write( DATA, 0x0000 );            // Top_Block=0  
    Write( DATA, 0x0019 );            // Bottom_Block=25  
    Write( DATA, 0x0019 );            // Number of Specified Blocks=Bottom_Block=25  
    Write( DATA, 0x0003 );            // Area Scroll Type=Whole Screen Scroll  
  
    ScrollUp() or ScrollDown();         // Scroll Up or Scroll Down  
  
}
```

```
void ScrollUp( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block);          // Start Block Address=Top_Block
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block +1 );       // Start Block Address= Top_Block+1
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block +2 );       // Start Block Address= Top_Block +2
    Delay();                           // Delay
    .....
    .....
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block );       // Start Block Address= Bottom_Block
    Delay();                           // Delay
}

void ScrollDown( void )
{
    Write( COMMAND, 0x0030 );           // Ext = 0
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block);        // Start Block Address= Bottom_Block
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block -1 );    // Start Block Address= Bottom_Block -1
    Delay();                           // Delay

    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Bottom_Block -2 );    // Start Block Address= Bottom_Block -2
    Delay();                           // Delay
    .....
    .....
    Write( COMMAND, 0x00AB);           // Scroll Start Set
    Write( DATA, Top_Block );          // Start Block Address= Top_Block
    Delay();                           // Delay
}
```

8.2.7 Read-Modify-Write Cycle

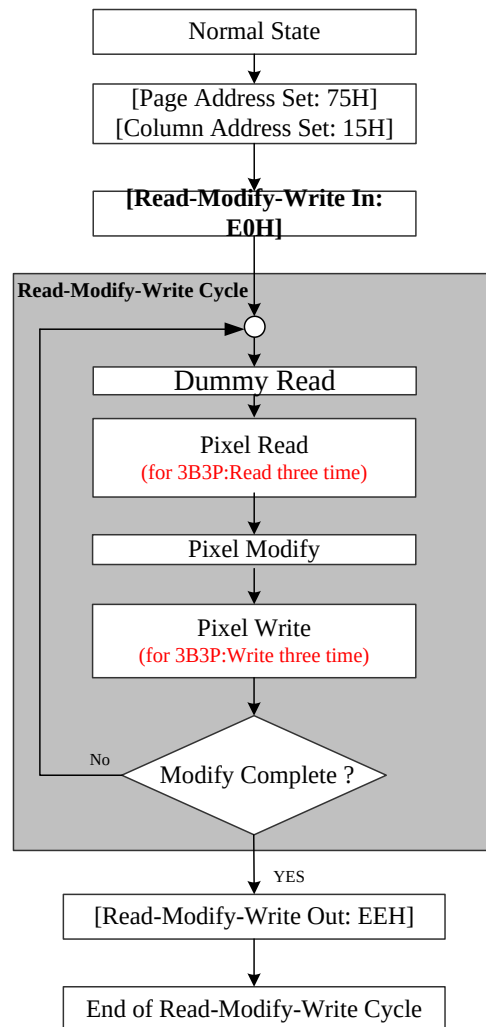


Figure 8.2.7.1 Read-Write-Modify Cycle

Example : Read-Write-Modify Cycle

```

void ReadModifyWriteIn( void )
{
    Write( COMMAND, 0x0030 );    // Ext = 0
    Write( COMMAND, 0x00E0 );    // Entry the Read-Modify-Write mode
}

void ReadModifyWriteOut( void )
{
    Write( COMMAND, 0x0030 );    // Ext = 0
    Write( COMMAND, 0x00EE );    // Out of partial display mode
}
  
```

```
extern unsigned char *display_pattern;
void main() (For 3B3P 32Gray Scale Display)
{
    unsigned pixel1,pixel2,pixel3, i;

    Windowing( 11, 31, 80, 50 );           // set the page and column range

    ReadModifyWriteIn();                   // entry the Read-Modify-Write mode

    for( i = 0 ; i < 1000 ; i++ )
    {
        Read( DATA );                     // For dummy read
        Pixel1= Read( DATA );             // Pixel read
        Pixel2= Read( DATA );             // Pixel read
        Pixel3= Read( DATA );             // Pixel read
        Pixel1 = pixel1 & 0x07FF;          // Pixel modify
        Pixel2 = pixel2 & 0x07FF;          // Pixel modify
        Pixel3 = pixel3 & 0x07FF;          // Pixel modify
        Write( DATA, pixel1 );
        Write( DATA, pixel2 );
        Write( DATA, pixel3 );
    }

    ReadModifyWriteOut();                  // Out of Read-Modify-Write mode
}
```

8.2.8 Display On / OFF

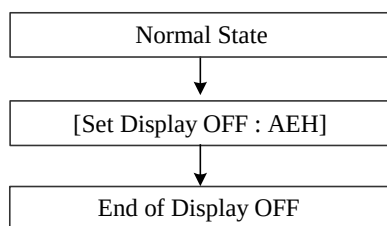


Figure 8.2.8.1 Display Off

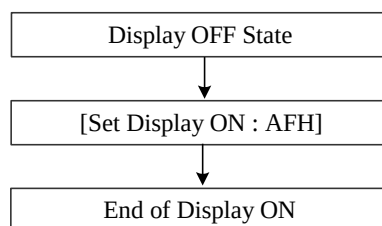


Figure 8.2.8.2 Display On

Example : Display OFF Operation

```
void DisplayOff( void )
```

```
{
```

Write(COMMAND, 0x0030);	// Ext = 0
Write(COMMAND, 0x00AE);	// Display Off

```
}
```

Example : Display ON Operation

```
void DisplayOn( void )
```

```
{
```

Write(COMMAND, 0x0030);	// Ext = 0
Write(COMMAND, 0x00AF);	// Display On

```
}
```

8.2.9 Power OFF sequence with Build-in power circuit:

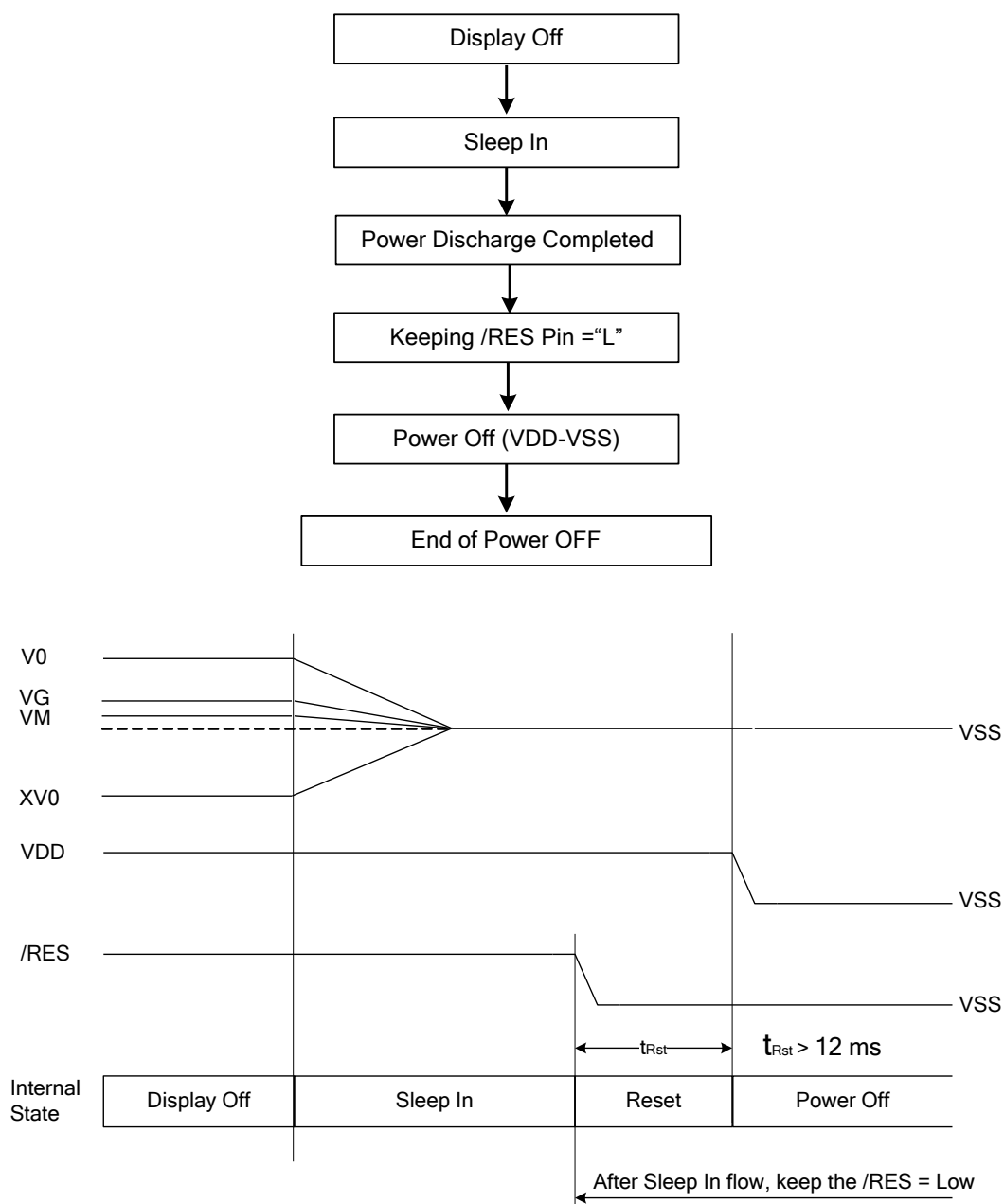


Figure 8.2.9.1 Power off

Note : The sequence is that users must set the VDD to low after keeping the /RES=low time longer than 12ms.

9. LIMITING VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Power Supply Voltage	VDDI (VDD1)	-0.5 ~ +4.0	V
Power supply voltage	VDDA (VDD2, VDD3, VDD4)	-0.5 ~ +4.0	V
Power supply voltage (VDD standard)	V0-XV0	-0.5 ~ +19	V
Power supply voltage (VDD standard)	VG	-0.3 ~ VDDA+0.3	V
Power supply voltage (VDD standard)	VM	-0.3 ~ VDDA+0.3	V
Input voltage	VIN	-0.5 to VDDI+0.5	V
Operating temperature(Die)	TOPR	-30 to +85	°C
Storage temperature(Die)	TSTR	-40 to +125	°C

Note:

1. All voltages are respect to VSS unless otherwise noted (VSS1=VSS2=VSS3=VSS4=VSS5).
2. Insure the voltage levels of VLCDIN, V0, VG, VM, VSS and XV0 always match the correct relation while operating:
VLCDIN > V0 ≥ VG > VM > VSS ≥ XV0
3. Stresses exceed the ranges listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
4. Parameters are valid in operating temperature range unless otherwise specified.
5. Interface input voltage range cannot exceed the maximum limitation of digital power supply voltage. $V_{in} \leq 3.6V$.

10. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

11. DC CHARACTERISTICS

$T_a = -30^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Item	Symbol	Condition	Rating			Units	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage (1)	VDD1	-	2.4	-	3.3	V	VDD1*1
Operating Voltage (2)	VDD2 VDD3 VDD4	(Relative to VSS)	2.4	-	3.3	V	VDD2 VDD3 VDD4
High-level Input Voltage	VIH	-	0.7 VDD	-	VDD	V	*2
Low-level Input Voltage	VIL	-	VSS	-	0.3 VDD	V	*2
High-level Output Current	IOH	VDD=2.7V VOH = 2.2V	0.5	-	-	mA	*3
Low-level Output Current	IOL	VDD=2.7V VOL = 0.5V	-	-	-0.5	mA	*3
Input leakage current	ILI	VIN = VDD or VSS	-1.0	-	1.0	μA	*4
Liquid Crystal Driver ON Resistance	RON	$T_a = 25^{\circ}\text{C}$ (Relative To VSS) V0 = 14.0V VDD = 2.7V	-	1.4	2.0	K Ω	SEgN COMn *5
Power supply voltage	V0-XV0		7	-	18	V	V0-XV0
Frame Frequency	fFRAME	1/160duty $T_a=25^{\circ}\text{C}$ VDD=2.7V CLD=0	-	78	160	Hz	SEgN

*** Recommended LCD V_{OP} voltage is 12V~14V .**

Dynamic Consumption Current: During Display, with the Internal Power Supply ON.

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern (checkerboard)	ISS	VDD = 2.8 V, V0-XV0 = 16.0 V Booster = 10x Bias = 1/12 Duty = 1/160 Bare chip Cap = 1.0uF	-	460	600	μA	*6
Power Down	ISS	Ta = 25°C	-	-	10	μA	-

Notes to the DC characteristics

1. The maximum possible V0-XV0 voltage that may be generated is dependent on voltage, temperature and (display) load, and internal clock
2. Power-down mode. During power down all static currents are switched off.

References for items marked with *

- *1. While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
- *2. The A0, D0 to D3, D4 to D6 (SDA), D7 (SCL), /RD(E), /WR(R/W), CSB, CL, RSTB .
- *3. The D0 to D7 and CL.
- *4. The A0,/RD (E), /WR(R/W), CSB, CLS, CL, RSTB, IF0 to IF2
- *5. These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (VG, and VM). These are specified for the operating voltage range.
RON = 0.1 V / ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)
- *6. It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

ST7529A I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
V0I, V0O, V0S, XV0I, XV0O, XV0S, VGI, VGO, VGS, VM, CA1P, CA1N	<100Ω
VPP, VDD1~VDD4, VSS1~VSS5	<50Ω
A0, ERD, RWR, CSB, D[7:0], (SPI.SDA), (SPI.SCL)	<700Ω
RSTB	1~3KΩ
IF[2:0], COMSCN, CLS, EXTB, T0 TEST1, TEST2	<1KΩ
CL, T[2:1], Reserved	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM159 is equal, and so is it of SEG0 ~ SEG254.
2. These limitations include the bottleneck of ITO layout.
3. Refer to the application note for "ITO Layout Guide".

12. AC CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

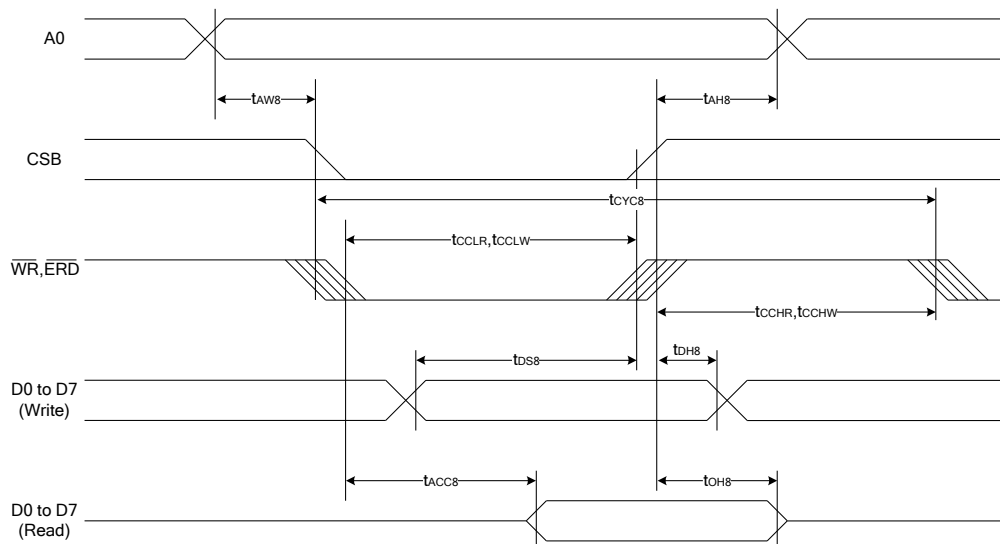


Figure 39.

(VDD = 3.3V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8	-	40	-	ns
Address setup time		tAW8	-	20	-	
System cycle time	WR	tCYC8	-	380	-	
Enable L pulse width (WRITE)		tCCLW	-	80	-	
Enable H pulse width (WRITE)		tCCHW	-	300	-	
Enable L pulse width (READ)	RD	tCCLR	-	230	-	
Enable H pulse width (READ)		tCCHR	-	500	-	
WRITE Data setup time	D0 to D7	tDS8	-	250	-	
WRITE Address hold time		tDH8	-	20	-	
READ access time		tACC8	CL = 100 pF	-	40	
READ Output disable time		tOH8	CL = 100 pF	-	30	

(VDD = 2.7 V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8	-	60	-	ns
Address setup time		tAW8	-	30	-	
System cycle time	WR	tCYC8	-	520	-	
Enable L pulse width (WRITE)		tCCLW	-	100	-	
Enable H pulse width (WRITE)		tCCHW	-	420	-	
Enable L pulse width (READ)	RD	tCCLR	-	350	-	
Enable H pulse width (READ)		tCCHR	-	650	-	
WRITE Data setup time	D0 to D7	tDS8	-	450	-	
WRITE Address hold time		tDH8	-	40	-	
READ access time		tACC8	CL = 100 pF	-	40	
READ Output disable time		tOH8	CL = 100 pF	-	30	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr + tf) \leq (tCYC8 - tCCLW - tCCHW)$ for $(tr + tf) \leq (tCYC8 - tCCLR - tCCHR)$ are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CSB being "L" and WR and RD being at the "L" level.

System Bus Read/Write Characteristics 1 (For the 6800 Series MPU)

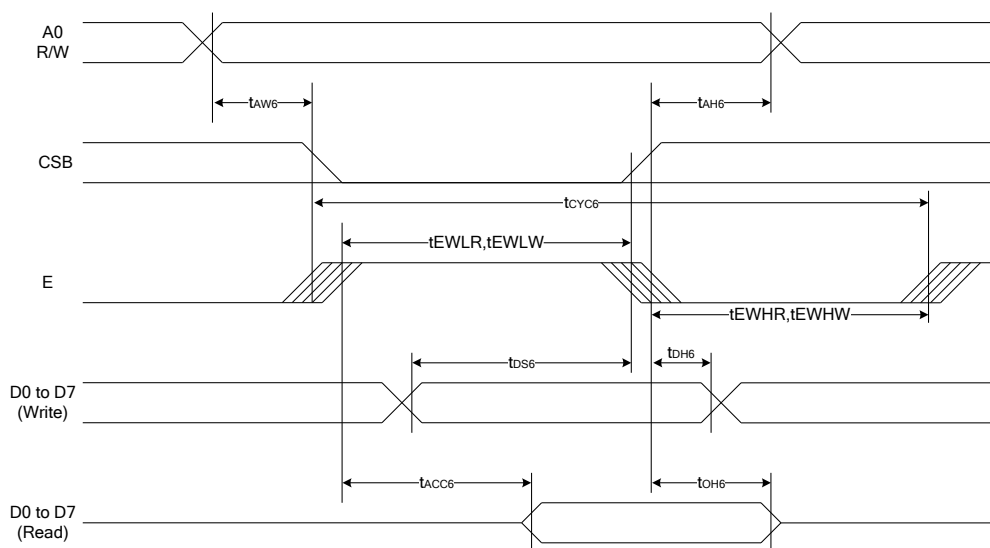


Figure 40.

(VDD = 3.3 V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6	-	20	-	ns
Address setup time		tAW6	-	20	-	
System cycle time	E	tCYC6	-	470	-	
Enable L pulse width (WRITE)		tEWLW	-	330	-	
Enable H pulse width (WRITE)		tEWHW	-	140	-	
Enable L pulse width (READ)		tEWLR	-	500	-	
Enable H pulse width (READ)	E	tEWHR	-	230	-	
WRITE Data setup time	D0 to D7	tDS6	-	240	-	
WRITE Address hold time		tDH6	-	230	-	
READ access time		tACC6	CL = 100 pF	-	40	
READ Output disable time		tOH6	CL = 100 pF	-	30	

(VDD = 2.7V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6	-	40	-	ns
Address setup time		tAW6	-	30	-	
System cycle time	E	tCYC6	-	650	-	
Enable L pulse width (WRITE)		tEWLW	-	420	-	
Enable H pulse width (WRITE)		tEWHW	-	230	-	
Enable L pulse width (READ)	E	tEWLR	-	650	-	
Enable H pulse width (READ)		tEWHR	-	350	-	
WRITE Data setup time	D0 to D7	tDS6	-	360	-	
WRITE Address hold time		tDH6	-	290	-	
READ access time		tACC6	CL = 100 pF	-	40	
READ Output disable time		tOH6	CL = 100 pF	-	30	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(tr + tf) \leq (tCYC6 - tEWLW - tEWHW)$ for $(tr + tf) \leq (tCYC6 - tEWLR - tEWHR)$ are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CSB being "L" and E.

SERIAL INTERFACE (4-Line Interface)

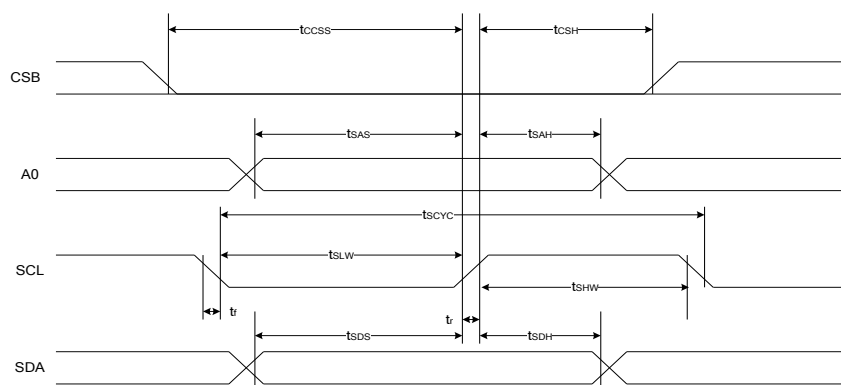


Fig 41.

(VDD=3.3V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	130	-	ns
SCL "H" pulse width		tSHW	-	80	-	
SCL "L" pulse width		tSLW	-	50	-	
Address setup time	A0	tSAS	-	40	-	
Address hold time		tSAH	-	30	-	
Data setup time	SDA	tSDS	-	40	-	
Data hold time		tSDH	-	30	-	
CS-SCL time	CSB	tCSS	-	20	-	
CS-SCL time		tCSH	-	60	-	

(VDD=2.7V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	150	-	ns
SCL "H" pulse width		tSHW	-	100	-	
SCL "L" pulse width		tSLW	-	50	-	
Address setup time	A0	tSAS	-	50	-	
Address hold time		tSAH	-	40	-	
Data setup time	SDA	tSDS	-	50	-	
Data hold time		tSDH	-	40	-	
CS-SCL time	CSB	tCSS	-	30	-	
CS-SCL time		tCSH	-	80	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

SERIAL INTERFACE (3-Line Interface)

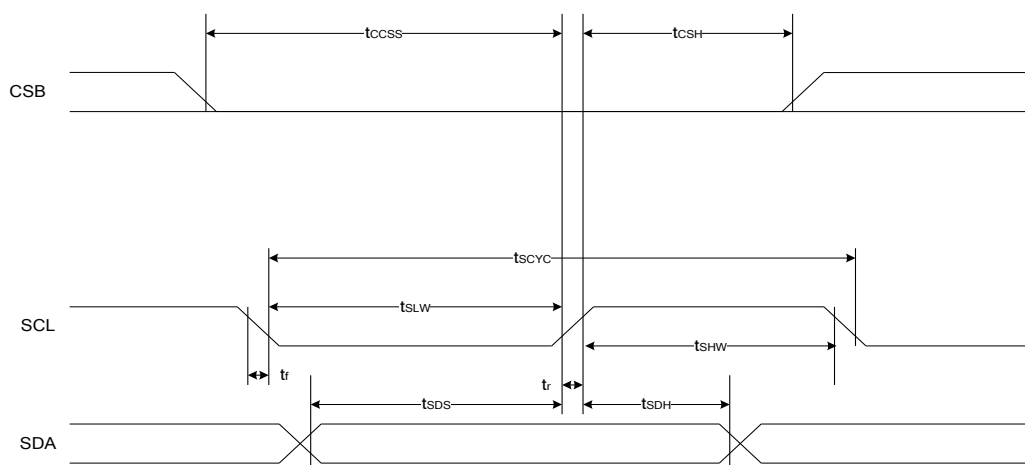


Fig 42.

(V_{DD}=3.3V, Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	130	-	ns
SCL "H" pulse width		tSHW	-	80	-	
SCL "L" pulse width		tSLW	-	50	-	
Data setup time	SI	tSDS	-	40	-	
Data hold time		tSDH	-	30	-	
CS-SCL time	CSB	tCSS	-	20	-	
CS-SCL time		tCSH	-	60	-	

(V_{DD}=2.7V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	tSCYC	-	150	-	ns
SCL "H" pulse width		tSHW	-	100	-	
SCL "L" pulse width		tSLW	-	50	-	
Data setup time	SI	tSDS	-	50	-	
Data hold time		tSDH	-	40	-	
CS-SCL time	CSB	tCSS	-	30	-	
CS-SCL time		tCSH	-	80	-	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

13. RESET TIMING

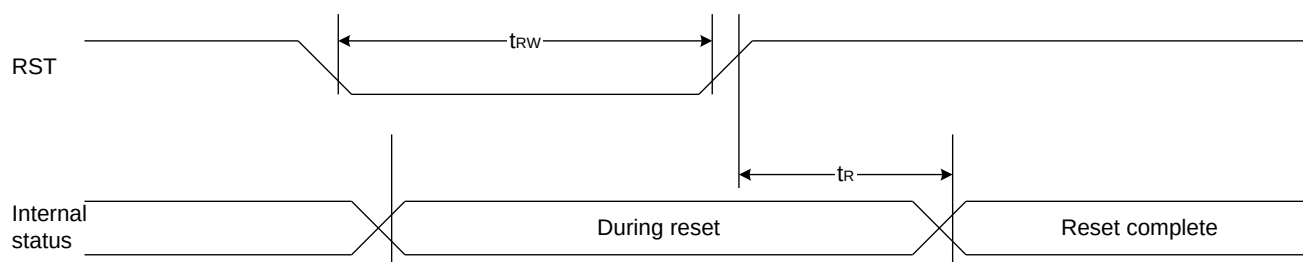


Fig 43.

(VDD = 3.3V, Ta = 25°C, Die)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR	-	-	-	1	ms
Reset "L" pulse width	RSTB	tRW	-	1	-	-	ms

(VDD = 2.7V, Ta = 25°C, Die)

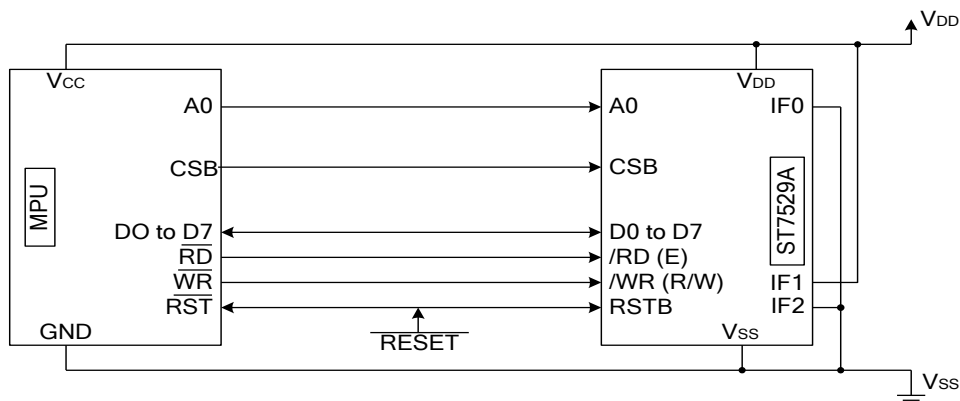
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR	-	-	-	1.5	ms
Reset "L" pulse width	RSTB	tRW	-	1.5	-	-	ms

14. THE MPU INTERFACE (REFERENCE EXAMPLES)

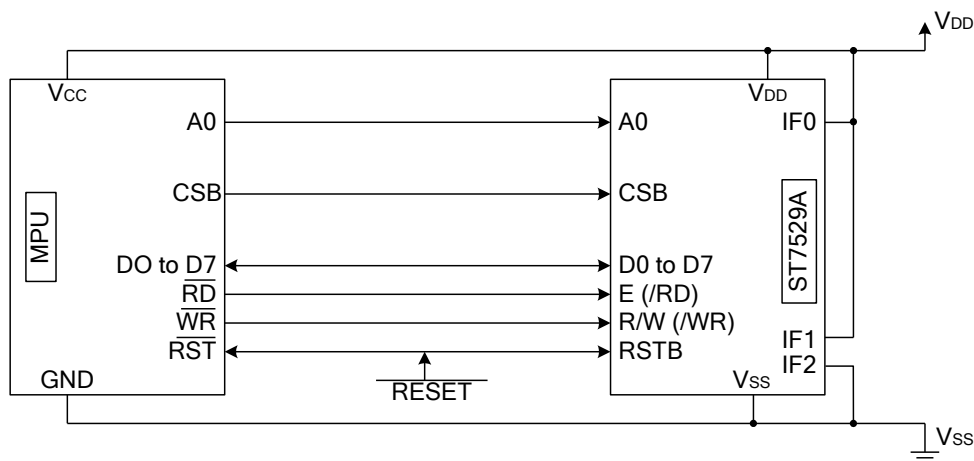
The ST7529A Series can be connected to either 8080 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the ST7529A series chips with fewer signal lines.

The display area can be enlarged by using multiple ST7529A Series chips. When this is done, the chip select signal can be used to select the individual lcs to access.

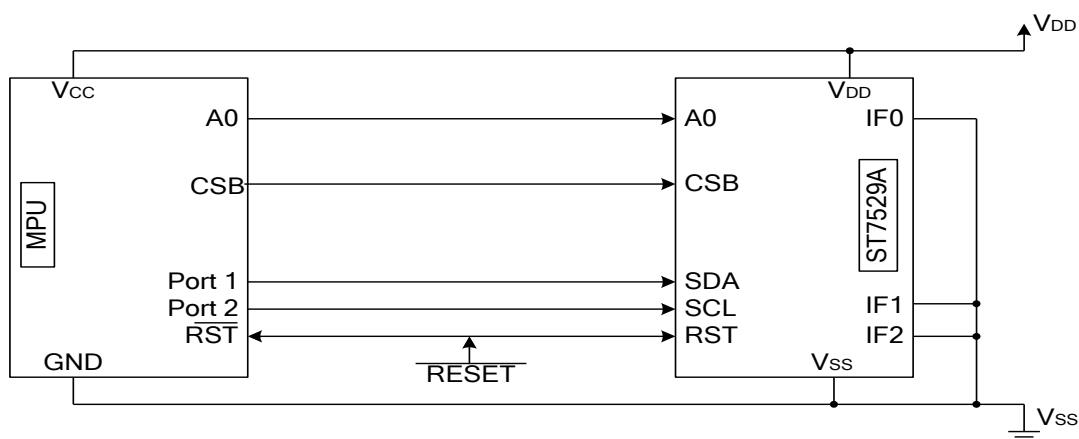
(1) 6800 Series MPUs(8 bit)



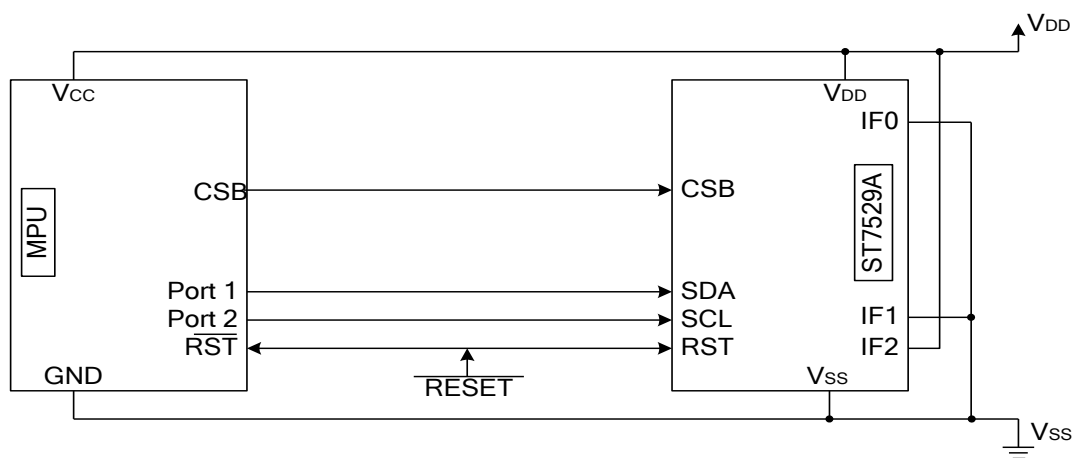
(2) 8080 Series MPUs(8 bit)



(3) Using the Serial Interface (4-line interface)

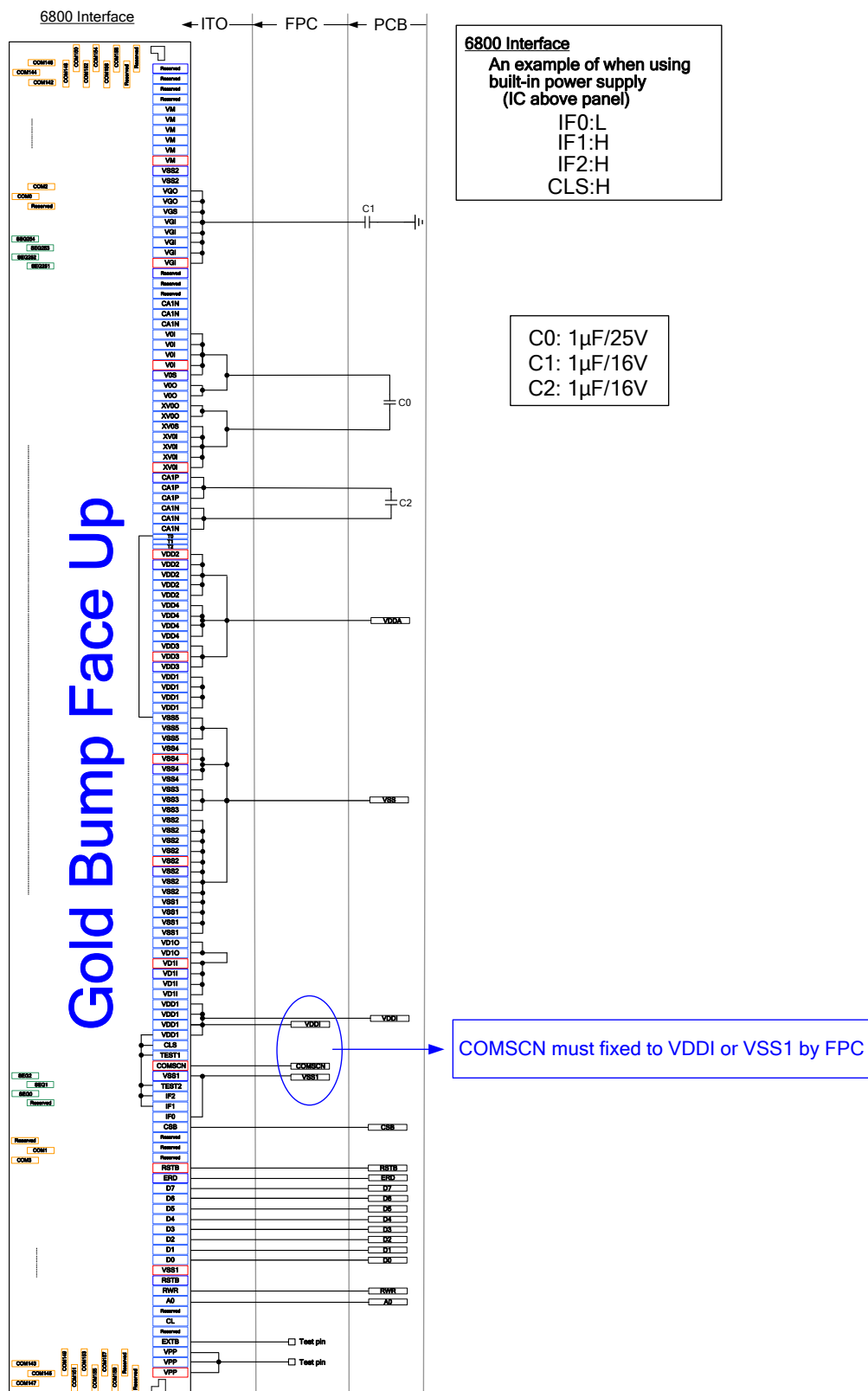


(3) Using the Serial Interface (3-line interface)



15. Application circuit

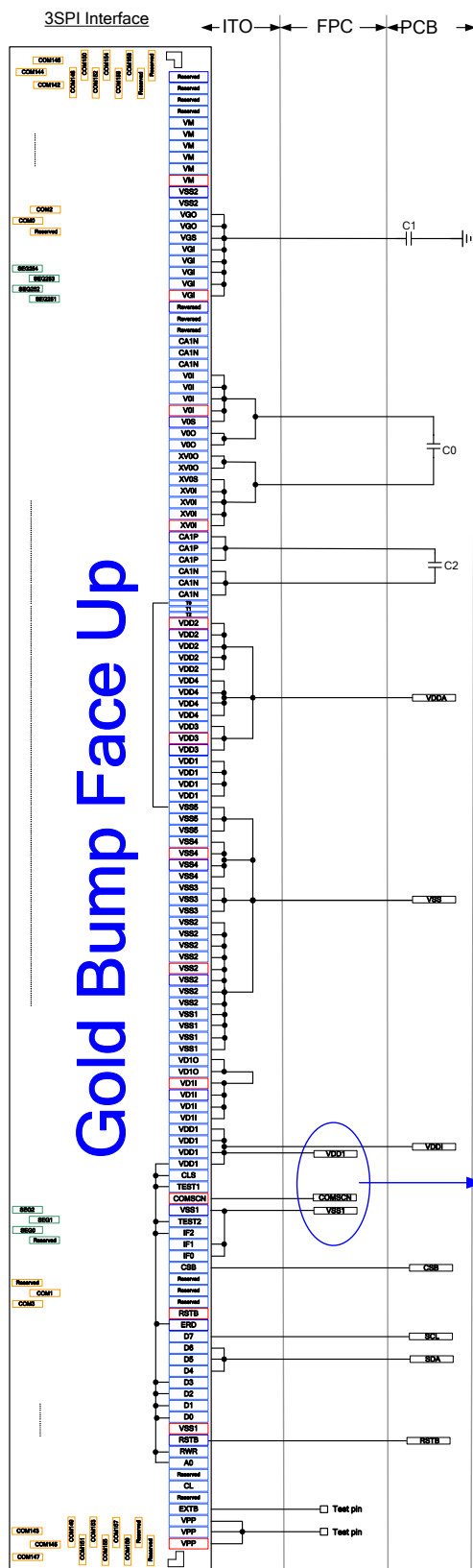
6800 Interface



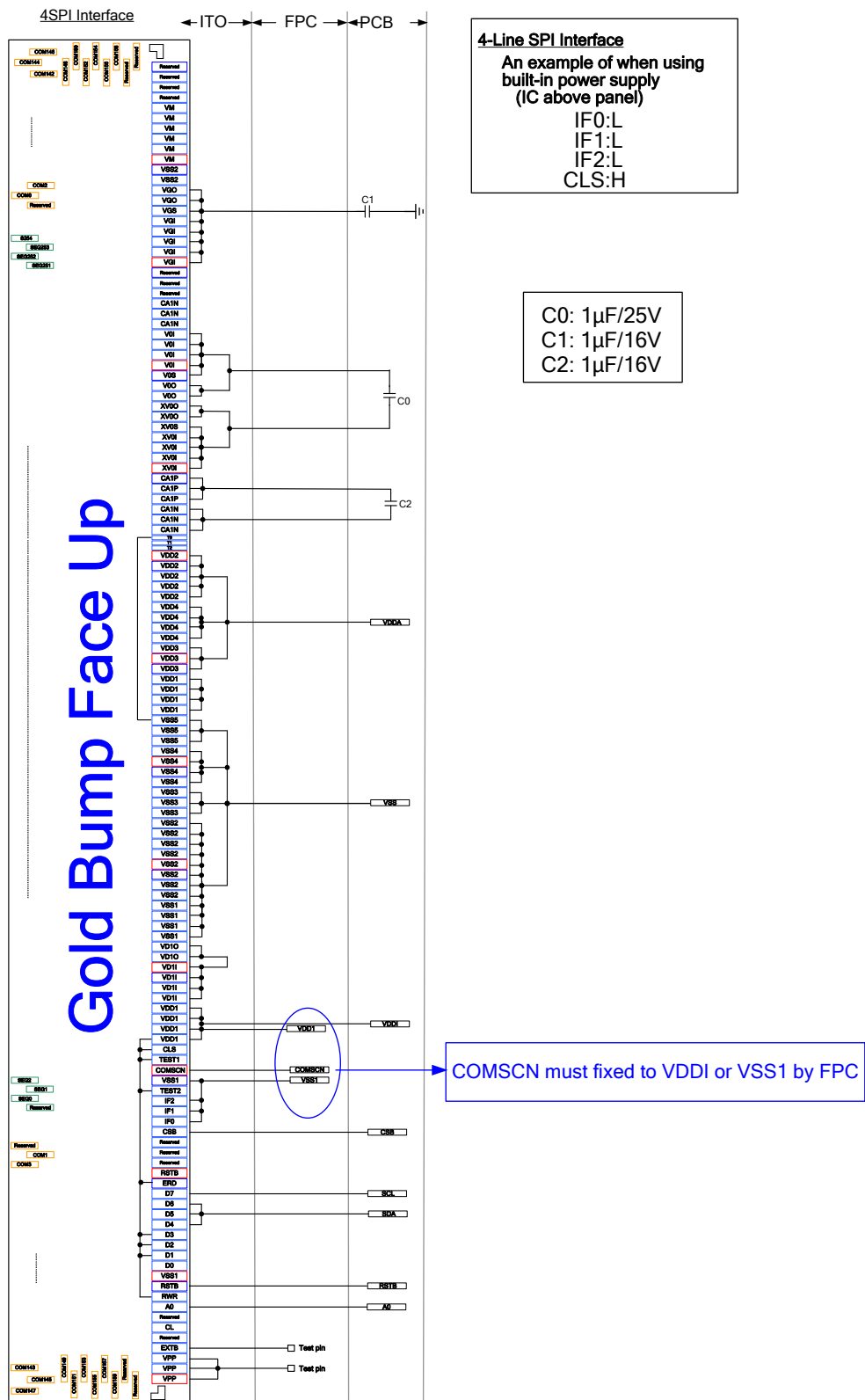
8080 Interface



ST7529A / Serial - 3 Line



ST7529A / Serial - 4 Line



ST7529A Series Specification Revision History		
Version	Date	Description
1.0	2021/06/11	Release version
1.0.a	2021/11/08	Modify ITO Layout Guide