

VFD Driver/Controller IC with Character RAM**PT6302**

DESCRIPTION

PT6302 is a dot matrix VFD Driver/Controller IC utilizing CMOS Technology specially designed to display characters, numerals, and symbols. PT6302 provides 35 dot matrix plus 2 additional segment drivers and 16 grid drivers. 248 types of character data (CGROM), 8 types of character data (CGRAM), 16 display digits x 2 bits symbol data, 16 display digits x 8 bits register for character data display and 2 general output bits for static operation are provided. Pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

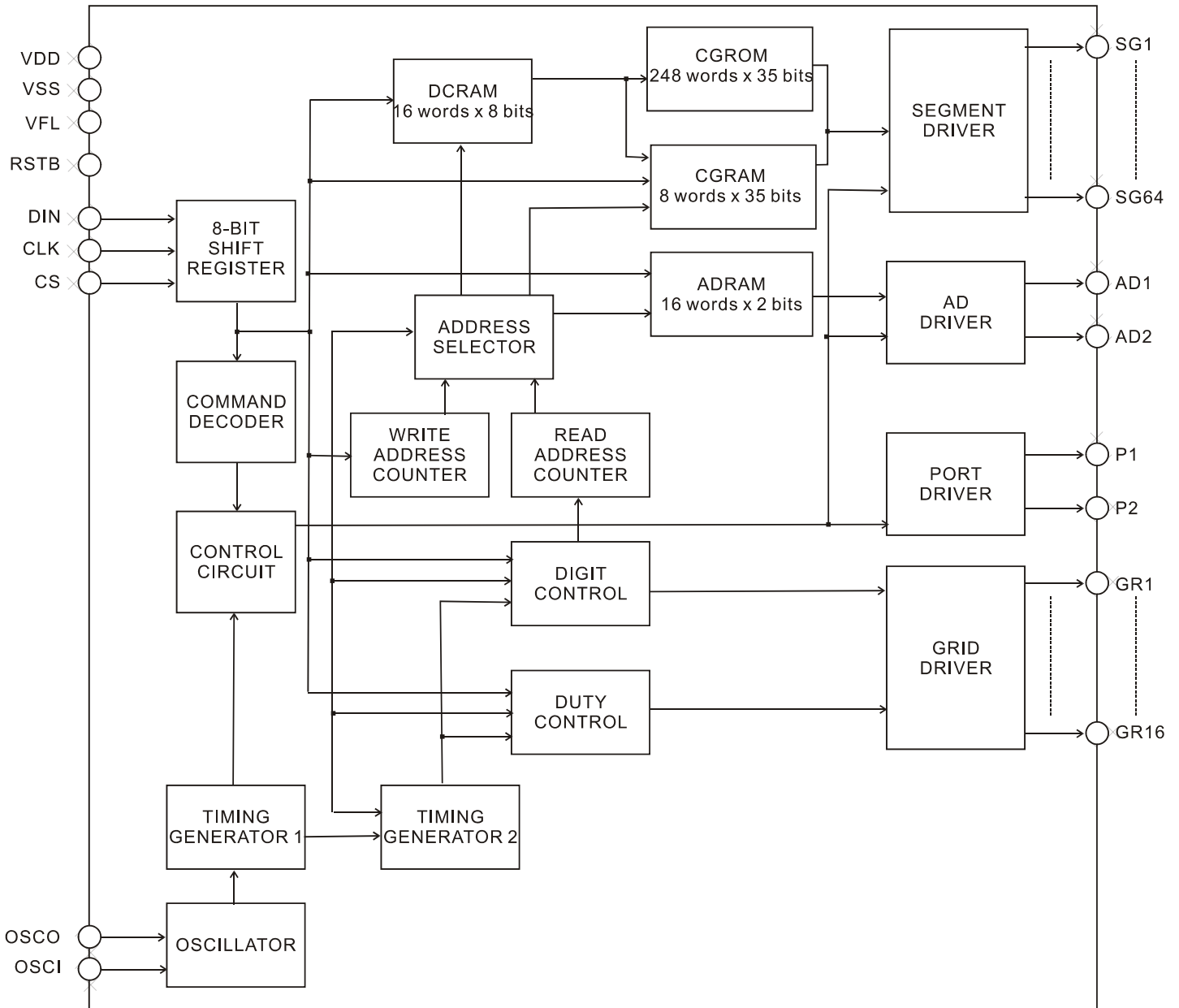
- CMOS Technology
- Logic Power Supply: $VDD = 3.3\text{ V} \pm 10\%$ or $5.0\text{ V} \pm 10\%$
- VFD Drive Power Supply: $VEE = -20\text{V to } -30\text{V}$
- Built-in Oscillation Circuit (External RC)
- One-Byte Instruction Execution (not including Data Write to RAM)
- Microcontroller Interface
- Display Contents:
 - Character Generator ROM (CGROM): 5x7 Dots (248 Character Data Types)
 - Character Generator RAM (CGRAM): 5x7 Dots (8 Character Data Types)
 - Additional Data RAM (ADRAM): 16 Display Digits x 2 Bits (Symbol Data)
 - Data Control RAM (DCRAM): 16 Display Digits x 8 Bits (Character Data Display Register)
 - General Output Port: 2 Bits (Static Operation)
- Display Control Function:
 - Display Digits : 9 to 16 Digits
 - Display Duty (Contrast Adjustment) : 8 stages
 - All Display Lights : ON/OFF Mode

APPLICATIONS

- Microcontroller Peripheral Device
- Audio/Video Equipment

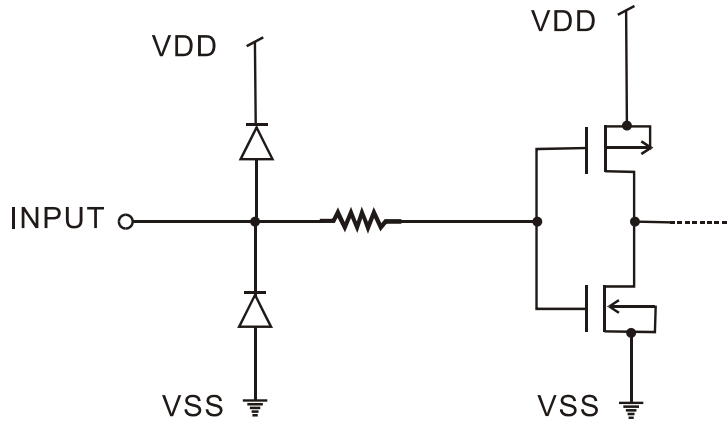
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BLOCK DIAGRAM

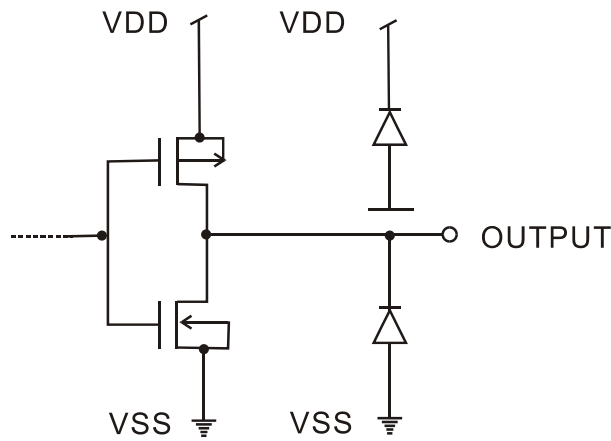


INPUT & OUTPUT CONFIGURATION

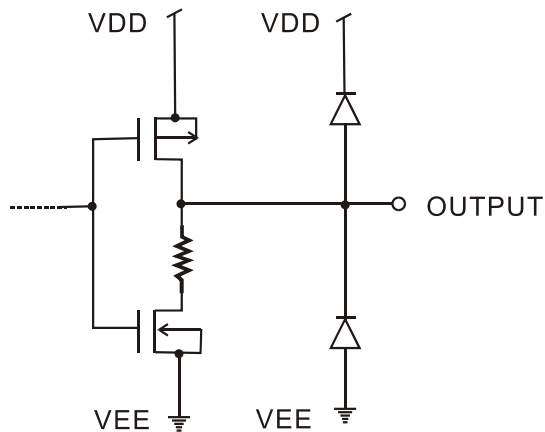
- Logic Input Pins



- Logic Output Pins



- Driver Output Pins



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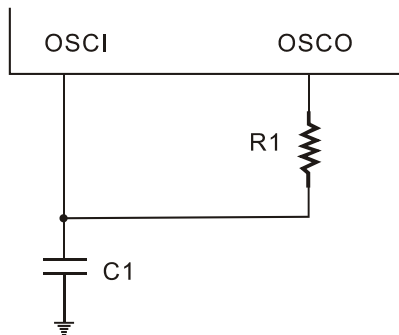
PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			LQFP	SSOP
SG5 to SG35 SG4 to SG1	O	Segment Driver Output Pin	1 ~ 31 64 ~ 61	9 ~ 39 8 ~ 5
GR1 to GR16	O	Grid Driver Output Pin	32 ~ 47	40 ~ 55
VEE	-	Power Supply	48	56
VSS	-	Ground Pin	49	57
OSCI	I	Oscillator Input Pin	50	58
OSCO	O	Oscillator Output Pin	51	59
RSTB	I	Reset Input Pin When this pin is set to "LOW", all functions are initialized.	52	60
CSB	I	Chip Select Input Pin When this pin is set to "High" Level, the serial data transfer is disabled.	53	61
CLKB	I	Shift Clock Input Pin The serial data is shifted at the rising edge of CLKB.	54	62
DIN	I	Serial Data Input Pin	55	63
VDD	-	Positive Power Supply	56	64
P1 to P2	O	General Purpose Output Pin	57 ~ 58	1 ~ 2
AD2 to AD1	O	Segment Driver Output Pin	59 ~ 60	3 ~ 4

FUNCTIONAL DESCRIPTION

OSCILLATION CIRCUIT

An oscillation circuit may be constructed by connecting external Resistor (R1) and Capacitor (C1) between the oscillator pins -- OSCO and OSCI. The RC time constant depends on the value of VDD voltage used. The target oscillation frequency is 2MHz. Please refer to the diagram below.

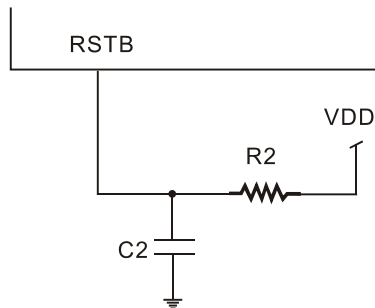


RESET FUNCTION

The Reset Function is enabled when the RSTB Pin is set to "Low" Level. All functions are initialized. The initial status of the various functions is given below:

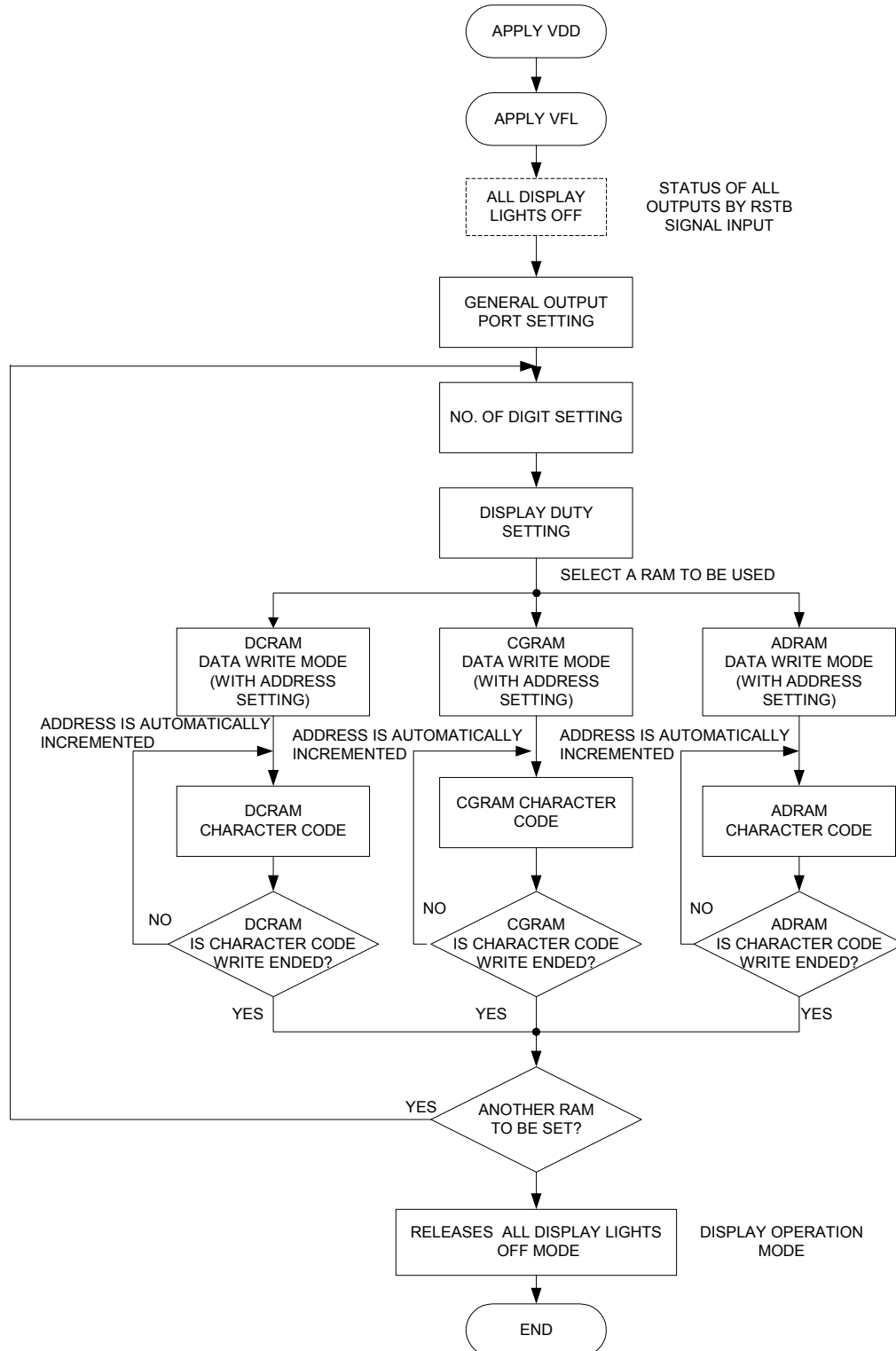
- | | | | |
|----|----------------------|---|--|
| 1. | Address of each RAM | : | Address "00"H |
| 2. | Data of each RAM | : | All contents are undefined. |
| 3. | General Output Ports | : | All General Output Ports are set to "LOW". |
| 4. | Display Digit | : | 16 Digits |
| 5. | Contrast Adjustment | : | 8/16 |
| 6. | All Display Lights | : | OFF Mode |
| 7. | Segment Output | : | All Segment Outputs are set to "LOW". |
| 8. | AD Output | : | All AD Outputs are set to "LOW". |

The RSTB Pin may be connected to either the microcontroller or an external Resistor and capacitor. For an external RC connection, please refer to the diagram below.



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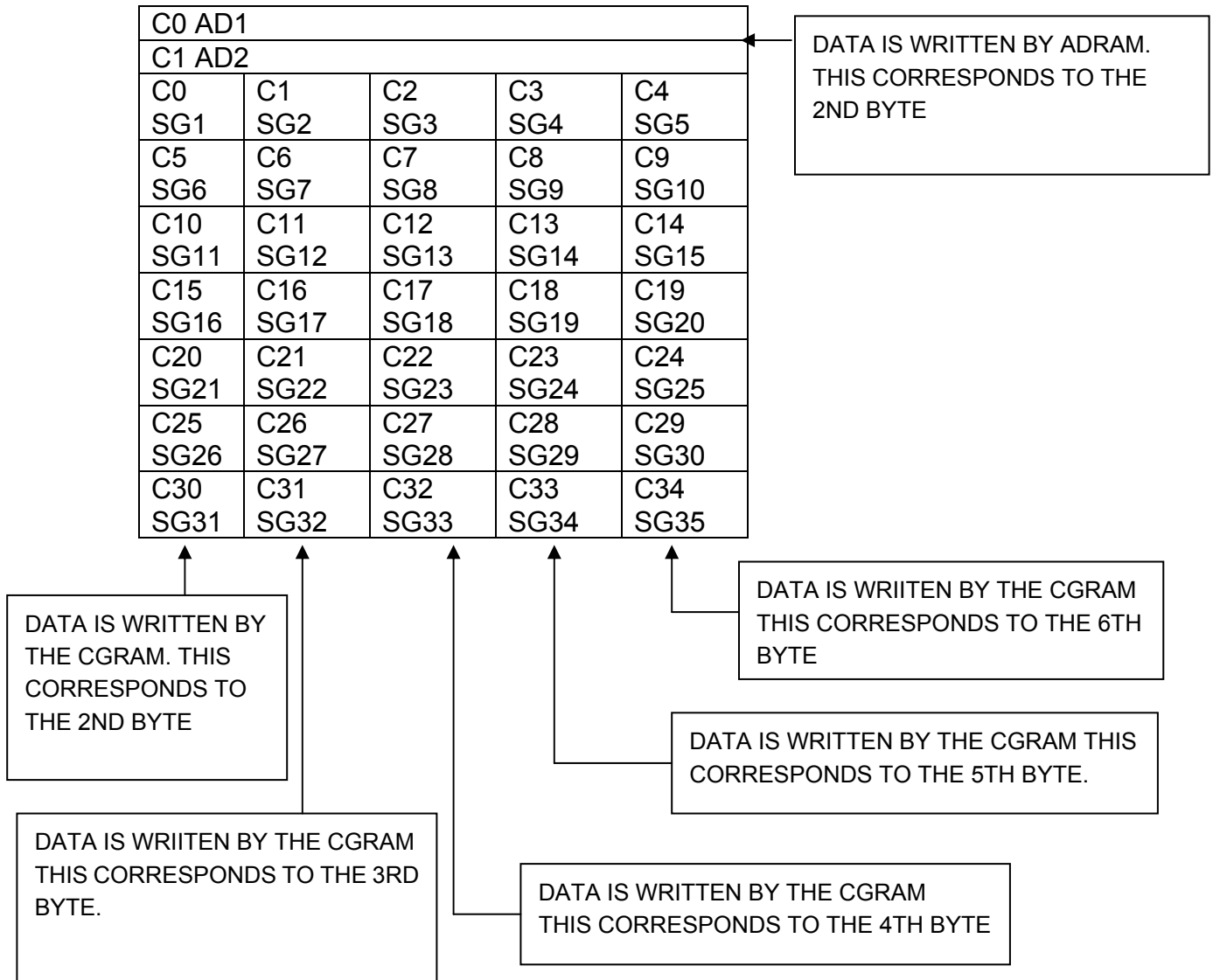
After reset, the PT6302 must be set according to the Initial Setting Flowchart shown below.



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RELATIONSHIP BETWEEN SEGMENT DRIVERS SGN AND ADN (ONE DIGIT)

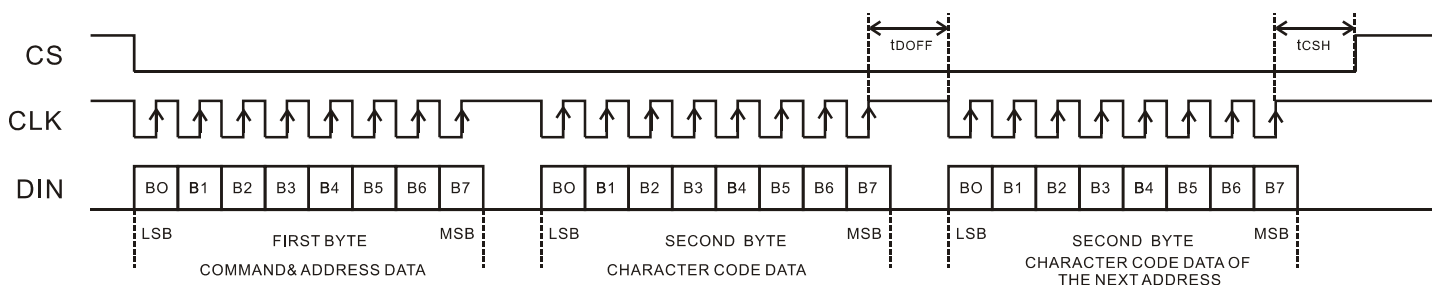
The following diagram best describes the relationship between the Segment Drivers -- SGN and ADn.



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DATA TRANSFER

The Display Control Command and the data are written by an 8-bit serial data transfer. Please refer to the Write Timing Diagram below.



Note: When data is written into the RAM (DCRAM, ADRAM, CGRAM) in a continuous manner, the address are automatically incremented. Therefore it is not necessary to specify the first byte of the 2nd and later bytes when writing the RAM data.

When the CSB pin is set to "LOW" Level, data transfer operation is enabled. 8 bits of data are sequentially inputted into the DIN Pin (LSB first). The shift register reads the data at the rising edge of the shift clock. The data is then inputted into the CLKB Pin. The internal load signals are automatically generated and the data is written to each register and RAM. Thus, it is not necessary to input load signals externally.

When the CSB Pin is set to "HIGH" Level, the data transfer operation is disabled. The data input when the CSB Pin changes from "HIGH" to "LOW" is recognized in 8-bit units.

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COMMANDS

The following are the list of commands issued by PT6302. When data is written into the RAM (DCRAM, CGRAM, or ADRAM) in a continuous manner, the addresses are automatically incremented internally. It is therefore not necessary to specify the first byte.

NO.	COMMAND	FIRST BYTE								SECOND BYTE								
		LSB	FIRST BYTE							MSB	LSB	SECOND BYTE						
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM DATA WRITE	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM DATA WRITE	X0	X1	X2	*	0	1	0	0	C0	C5	C10	C15	C20	C25	C30	*	2ND BYTE
										C1	C6	C11	C16	C21	C26	C31	*	3RD BYTE
										C2	C7	C12	C17	C22	C27	C32	*	4TH BYTE
										C3	C8	C13	C18	C23	C28	C33	*	5TH BYTE
		C4	C9	C14	C19	C24	C29	C34	*								*	6TH BYTE
3	ADRAM DATA WRITE	X0	X1	X2	X3	1	1	0	0	C0	C1	*	*	*	*	*	*	
4	GENERAL OUTPUT PORT SET	P1	P2	*	*	0	0	1	0									
5	DISPLAY DUTY SET	D0	D1	D2	*	1	0	1	0									
6	NO. OF DIGITS SET	K0	K1	K2	*	0	1	1	0									
7	ALL LIGHTS ON/OFF	L	H	*	*	1	1	1	0									
	TEST MODE	0	0	0	*	0	0	0	1									

Note:

1. The Test Mode is not a user function, but an IC internal function
2. * = Not Relevant
3. Xn = RAM Address Bit, n = 0 to 3
4. Cn = RAM Character Code Bit, n = 0 to 34
5. Pn = General Output Port Status Bit, n = 1 to 2
6. Dn = Display Duty Bit, n = 0 to 2
7. Kn = Number of Digits Bit, n = 0 to 2
8. H = All Lights ON
9. L = All Lights OFF

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DATA CONTROL RAM (DCRAM) DATA WRITE COMMAND

The DCRAM Data Write Command is used to specify the address of the DCRAM and writes the character code of the CGROM and CGRAM. The DCRAM consists of 4 address bits which are used to store the CGRAM & CGROM character codes. The character codes specified by the DCRAM is converted to a 5 x 7 dot matrix character pattern via the CGROM and CGRAM. The DCRAM can store up to 16 characters. The DCRAM Data Write Command Format is shown below.

1st Byte (1st)	LSB				MSB				DCRAM Data Write Mode is selected and the DCRAM Address is specified. (i.e. DCRAM Address = 0H)
	B0	B1	B2	B3	B4	B5	B6	B7	
	X0	X1	X2	X3	1	0	0	0	

2nd Byte (2nd)	LSB				MSB				CGROM & CGRAM Character Codes are specified. (They are written into the DCRAM Address 0H)
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C1	C2	C3	C4	C5	C6	C7	

During a continuous data write operation from one DCRAM Address to the next, it is not necessary to specify the DCRAM address since they are automatically incremented; however, the character code must be specified. Please refer to the information below.

2nd Byte (3rd)	LSB				MSB				Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 1H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C1	C2	C3	C4	C5	C6	C7	

2nd Byte (4th)	LSB				MSB				Character Code of CGRAM & CGROM are specified and written into the DCRAM Address 2H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C1	C2	C3	C4	C5	C6	C7	

⋮

2nd Byte (17th)	LSB				MSB				Character Code of CGRAM & CGROM are specified and written into the DCRAM Address FH.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C1	C2	C3	C4	C5	C6	C7	

2nd Byte (18th)	LSB				MSB				Character Code of CGRAM & CGROM are specified and rewritten into the DCRAM Address 0 H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C1	C2	C3	C4	C5	C6	C7	

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where: X0 (LSB) to X3 (MSB): DCRAM Address Bits (16 Characters)
 C0 (LSB) to C7 (MSB): CGROM & CGRAM Character Code Bits (256 Characters)

Please refer to the table below for the GRID position and DCRAM Address setting relationship.

Hex	X0	X1	X2	X3	GRID Position
0	0	0	0	0	GR1
1	1	0	0	0	GR2
2	0	1	0	0	GR3
3	1	1	0	0	GR4
4	0	0	1	0	GR5
5	1	0	1	0	GR6
6	0	1	1	0	GR7
7	1	1	1	0	GR8
8	0	0	0	1	GR9
9	1	0	0	1	GR10
A	0	1	0	1	GR11
B	1	1	0	1	GR12
C	0	0	1	1	GR13
D	1	0	1	1	GR14
E	0	1	1	1	GR15
F	1	1	1	1	GR16

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CGRAM DATA WRITE COMMAND

The Character Generator RAM (CGRAM) Data Write Command is used to specify the CGRAM address (00H to 07H) and write the character pattern data. It consists of 3 address bits which is used to store the 5 x 7 dot matrix character patterns. The CGRAM can store up to 8 types of character patterns which may be displayed by specifying the Character Code (DCRAM Address). The CGRAM Data Write Command Format is given below.

1st Byte (1st)	LSB				MSB				CGRAM Data Write Mode is selected and the CGRAM Address is specified (i.e. CGRAM Address = 00H).
	B0	B1	B2	B3	B4	B5	B6	B7	
	X0	X1	X2	*	0	1	0	0	

2nd Byte (2nd)	LSB				MSB				1st Column Data is specified and rewritten into the CGRAM Address 00H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C5	C10	C15	C20	C25	C30	*	

3rd Byte (3rd)	LSB				MSB				2nd Column Data is specified and rewritten into the CGRAM Address 00H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C1	C6	C11	C16	C21	C26	C31	*	

4th Byte (4th)	LSB				MSB				3rd Column Data is specified and rewritten into the CGRAM Address 00H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C2	C7	C12	C17	C22	C27	C32	*	

5th Byte (5th)	LSB				MSB				4th Column Data is specified and rewritten into the CGRAM Address 00H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C3	C8	C13	C18	C23	C28	C33	*	

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6th Byte (6th)	LSB				MSB				5th Column Data is specified and rewritten into the CGRAM Address 00H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C4	C9	C14	C19	C24	C29	C34	*	

During a continuous data write operation from one CGRAM Address to the next, it is not necessary to specify the CGRAM address since they are automatically incremented; however, the character pattern data must be specified. The 2nd to the 6th character pattern data byte are considered as one data item, therefore 300ns is sufficient value for parameter tDOFF between bytes. Please refer to the information below.

2nd Byte (7th)	LSB				MSB				1st Column Data is specified and rewritten into the CGRAM Address 01H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C0	C5	C10	C15	C20	C25	C30	*	

⋮

6th Byte (11th)	LSB				MSB				5th Column Data is specified and rewritten into the CGRAM Address 01H.
	B0	B1	B2	B3	B4	B5	B6	B7	
	C4	C9	C14	C19	C24	C29	C34	*	

where:

- X0 (LSB) to X2 (MSB) : CGRAM Address Bits (8 Characters)
- C0 (LSB) to C34 (MSB): Character Pattern Data Bits (35 outputs/digit)

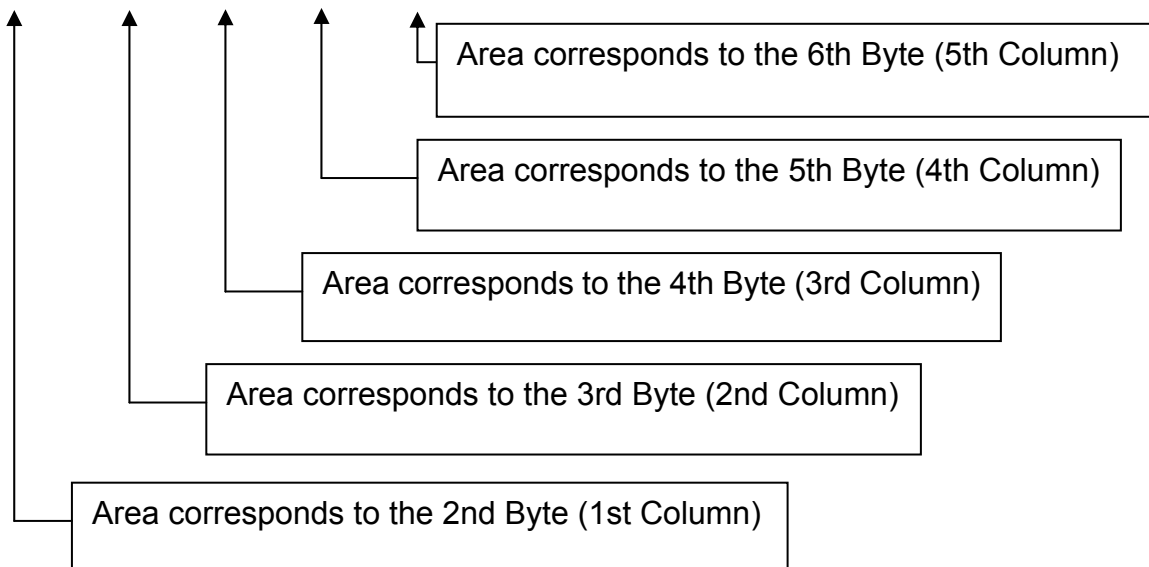
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Please refer below for the CGROM Address and CGRAM Address Setting relationship.

HEX	X0	X1	X2	CGROM Address
00	0	0	0	RAM00(00000000B)
01	1	0	0	RAM01(00000001B)
02	0	1	0	RAM02(00000010B)
03	1	1	0	RAM03(00000011B)
04	0	0	1	RAM04(00000100B)
05	1	0	1	RAM05(00000101B)
06	0	1	1	RAM06(00000110B)
07	1	1	1	RAM07(00000111B)

The CGROM and CGRAM output area placement is given in the table below.

C0	C1	C2	C3	C4
C5	C6	C7	C8	C9
C10	C11	C12	C13	C14
C15	C16	C17	C18	C19
C20	C21	C22	C23	C24
C25	C26	C27	C28	C29
C30	C31	C32	C33	C34



The Character Generator ROM (CGROM) consists of 8 CGROM Address bits generating 5 x 7 dot matrix character patterns. It can store up to a maximum of 248 types of character patterns.

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ADRAM DATA WRITE COMMAND

The Additional Data RAM (ADRAM) consists of 4 address bits used to store the symbol data. It can store up to 2 types of symbol patterns per digit. The symbol data specified by the ADRAM is directly outputted. The terminals to which the ADRAM data are outputted may be used as a cursor. The ADRAM command format is given below.

	LSB				MSB				
1st Byte (1st)	B0	B1	B2	B3	B4	B5	B6	B7	ADRAM Data Write Mode is selected and the ADRAM address is specified. (i.e. ADRAM Address = 0H)
	X0	X1	X2	X3	1	1	0	0	

	LSB				MSB				
2nd Byte (2nd)	B0	B1	B2	B3	B4	B5	B6	B7	Symbol Data is specified and written into the ADRAM Address 0H.
	C0	C1	*	*	*	*	*	*	

During a continuous data write operation from one ADRAM Address to the next, it is not necessary to specify the ADRAM address since they are automatically incremented; however, the symbol data must be specified. Please refer to the information below.

	LSB				MSB				
2nd Byte (3rd)	B0	B1	B2	B3	B4	B5	B6	B7	Symbol Data is specified and written into the ADRAM Address 1H.
	C0	C1	*	*	*	*	*	*	

	LSB				MSB				
2nd Byte (4th)	B0	B1	B2	B3	B4	B5	B6	B7	Symbol Data is specified and written into the ADRAM Address 2H.
	C0	C1	*	*	*	*	*	*	

⋮

	LSB				MSB				
2nd Byte (17th)	B0	B1	B2	B3	B4	B5	B6	B7	Symbol Data is specified and written into the ADRAM Address FH.
	C0	C1	*	*	*	*	*	*	

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	LSB				MSB				
2nd Byte (18th)	B0	B1	B2	B3	B4	B5	B6	B7	Symbol Data is specified and rewritten into the ADRAM Address 0H.
	C0	C1	*	*	*	*	*	*	

where: X0 (LSB) to X3 (MSB): ADRAM Address Bits (16 Characters)
 C0 (LSB) to C1 (MSB): Symbol Data Bits (2 Symbol Data per Digit)

Please refer to the table below for the GRID and ADRAM Address relationship.

HEX	X0	X1	X2	X3	GRID Position
0	0	0	0	0	GR1
1	1	0	0	0	GR2
2	0	1	0	0	GR3
3	1	1	1	0	GR4
4	0	0	1	0	GR5
5	1	0	1	0	GR6
6	0	1	1	0	GR7
7	1	1	1	0	GR8
8	0	0	0	1	GR9
9	1	0	0	1	GR10
A	0	1	0	1	GR11
B	1	1	0	1	GR12
C	0	0	1	1	GR13
D	1	0	1	1	GR14
E	0	1	1	1	GR15
F	1	1	1	1	GR16

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GENERAL OUTPUT PORT SET COMMAND

The General Output Port Set Command is used to specify the general output port status. The general output port is used to control other input/output devices as well as turn on the LED Display. When the general output port is set to "HIGH", the output is equivalent to the VDD voltage. When the general output port is set to "LOW" Level, the output becomes ground potential. The command format is given below.

	LSB				MSB				
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	A General Output Port is selected and the output status is specified.
	P1	P2	*	*	0	0	1	0	

where: P1, P2 : General Output Port * = Not Relevant

The following table shows the data setting in relation to the Status of the General Output Port

P1	P2	General Output Port Display Status
0	0	P1="LOW", P2="LOW" (see note 1)
1	0	P1="HIGH", P2="LOW"
0	1	P1="LOW", P2="HIGH"
1	1	P1="HIGH", P2="HIGH"

Note:

1. The state when the power is applied or when the RSTB is inputted.

DISPLAY DUTY SET COMMAND

The Display Duty Set Command is used to write the display duty value to the duty cycle register. Using a 3-bit data, the display duty adjusts the contrast in 8 stages. When the power is turned ON or when the RSTB signal is inputted, the duty cycle register value is set to "0". It is advisable to always execute this command before turning on the display, after which the desired duty value may be set. The command format is given below.

	LSB				MSB				
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	Display Duty Set Mode is selected and the duty value is specified.
	D0	D1	D2	*	1	0	1	0	

where: D0 (LSB) to D2 (MSB) : Display Duty Data Bits (8 stages)
 * = Not Relevant

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The Relationship between the Setup Data and the Controlled GRID Duty is given in the table below.

HEX	D2	D1	D0	GRID Duty
0	0	0	0	8/16
1	0	0	1	9/16
2	0	1	0	10/16
3	0	1	1	11/16
4	1	0	0	12/16
5	1	0	1	13/16
6	1	1	0	14/16
7	1	1	1	15/16

The state when the Power is turned ON or when the RSTB signal is inputted

NUMBER OF DIGITS SET COMMAND

The Number of Digits Set Command is used to write the number of display digits into the display digit register. Using a 3-bit data, the Number of Digits Set Command can display 9 to 16 digits. When the power is turned ON or when the RSTB signal is inputted, the value is set to "0". It is advisable to always execute this command before the turning on the display. The command format is given below.

1st Byte	LSB			MSB				
	B0	B1	B2	B3	B4	B5	B6	B7
	K0	K1	K2	*	0	1	1	0

The Number of Digits Set Mode is selected and the number of digit value is specified.

The table below shows the relationship between the setup data and the controlled GR.

HEX	K2	K1	K0	Number of Digits of GR
0	0	0	0	GR1 ~ GR16
1	0	0	1	GR1 ~ GR9
2	0	1	0	GR1 ~ GR10
3	0	1	1	GR1 ~ GR11
4	1	0	0	GR1 ~ GR 12
5	1	0	1	GR1~ GR13
6	1	1	0	GR1~ GR14
7	1	1	1	GR1~ GR15

The state when the Power is turned ON or when the RSTB signal is inputted.

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DISPLAY LIGHT SET COMMAND

The Display Light Set Command is used to turn all display lights ON or OFF. All Display Lights ON Mode is primarily used for testing the display. The All Display Light OFF Mode is used for the blinking display and to prevent any malfunction when the power is turned ON.. The general output port cannot be controlled by this command. The command format is given below.

	LSB				MSB				
1st Byte	B0	B1	B2	B3	B4	B5	B6	B7	The Display Light Set Command is selected.
	L	H	*	*	1	1	1	0	

where: L = All Display Lights are turned OFF
 H = All Display Lights are turned ON
 * = Not Relevant

The table below shows the SG and AD Display Status in relation to the Display Light Set Command data.

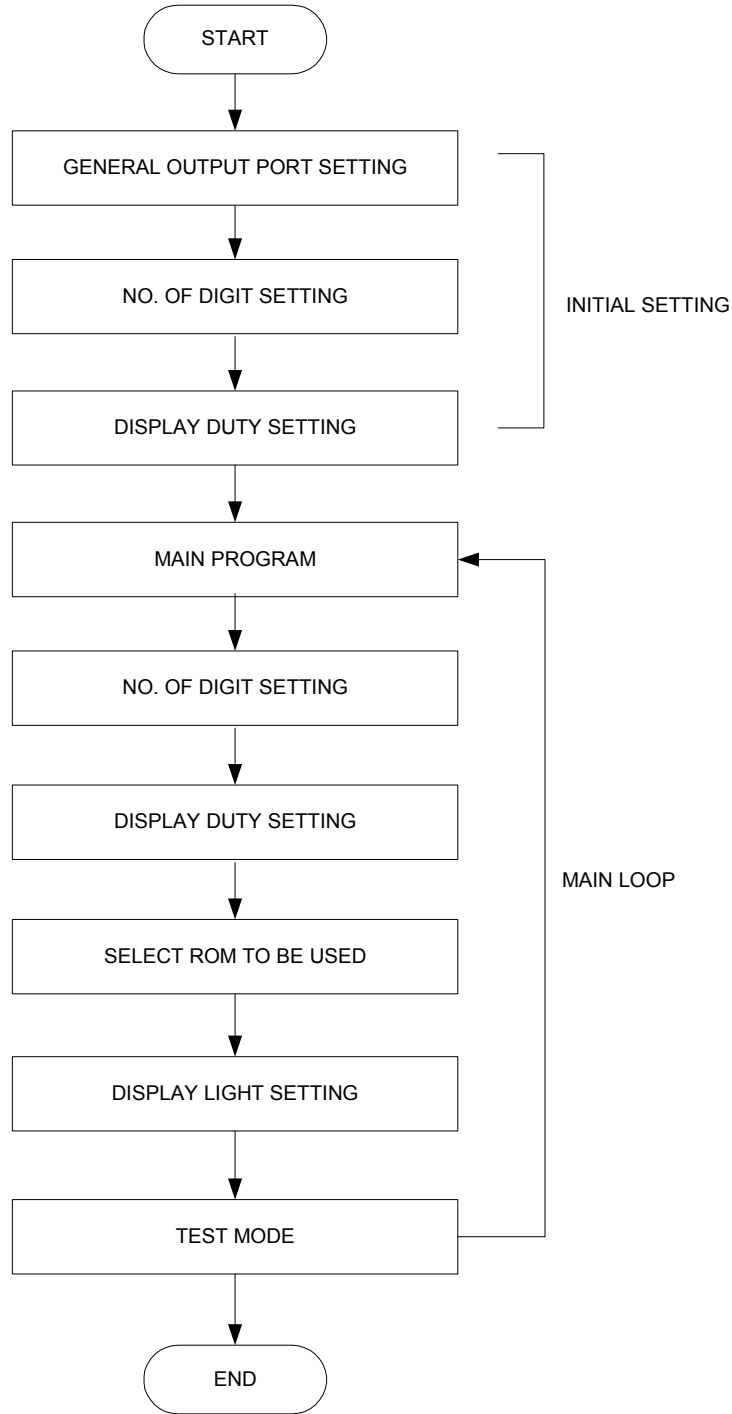
L	H	SG and AD Display State
0	0	Normal Display Mode
1	0	All Outputs ="LOW"
0	1	All Output ="HIGH"
1	1	All Outputs = "HIGH"

The state when the power is applied or when the RSTB signal is inputted

All Display Light ON Mode has the first priority.

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RECOMMENDED SOFTWARE FLOWCHART



- Notes:
1. Display light active mode (ex. 0111XX00B)
 2. Test mode OFF (ex. 1000X000B)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage 1	V_{DD}	-	-0.3 to 6.5	V
Supply Voltage 2	V_{EE}	-	-30 to $V_{DD} + 0.3$	V
Input Voltage	V_{IN}	-	-0.3 to $V_{DD} + 0.3$	V
Power Dissipation	P_D	$T_a \leq 25^\circ\text{C}$	541	mW
Output Current 1	I_{O1}	GR1 to GR16	-40 to 0	mA
Output Current 2	I_{O2}	AD1 to AD2	-20 to 0	mA
Output Current 3	I_{O3}	SG1 to SG35	-10 to 0	mA
Output Current 4	I_{O4}	P1 to P2	-4.0 to 4.0	mA
Operating Temperature	T_{opr}	-	-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-	-65 to +150	$^\circ\text{C}$

VFD Driver/Controller IC with Character RAM
PT6302

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage 1	V_{DD}		4.5	5.0	5.5	V
			3.0	3.3	3.6	V
Supply Voltage 2	V_{EE}	Power Supply Voltage=5V	-30	-	-20	V
		Power Supply Voltage=3.3V	-30	-	-20	V
High Level Input Voltage	V_{IH}	Power Supply Voltage=5V All input pins except OSC1.	$0.7V_{DD}$	-	-	V
		Power Supply Voltage=3.3V All input pins except OSC1.	$0.8V_{DD}$	-	-	V
Low Level Input Voltage	V_{IL}	Power Supply Voltage=5V All input pins except OSC1.	-	-	$0.3V_{DD}$	V
		Power Supply Voltage=3.3V All input pins except OSC1.	-	-	$0.2V_{DD}$	V
CLKB Frequency	f_c	Power Supply Voltage=5V	-	-	1.0	MHz
		Power Supply Voltage=3.3V	-	-	1.0	MHz
Oscillation Frequency	f_{osc}	Power Supply Voltage=5V R1=3.3 kOhms, C1=47pF	1.5	2.0	2.5	MHz
		Power Supply Voltage=3.3V R1=3.3 kOhms, C1=39pF	1.5	2.0	2.5	MHz
Frame Frequency	f_{FR}	Power Supply Voltage=5V DIGIT= 1 to 16, R1=3.3KOhms, C1=47pF	183	244	305	Hz
		Power Supply Voltage=3.3V DIGIT= 1 to 16, R1=3.3 kOhms, C1=39pF	183	244	305	Hz
RSTB Input Time	t_{RSON}	Power Supply Voltage=5V R2=1.0 kOhms, C2=0.1uF	0	-	200	μs
		Power Supply Voltage=3.3V R2=1.0 kOhms, C2=0.1uF	0	-	200	μs
Operating Temperature	T_{opr}	Power Supply Voltage=5V	-40	-	85	$^{\circ}C$
		Power Supply Voltage=3.3V	-40	-	85	$^{\circ}C$

VFD Driver/Controller IC with Character RAM
PT6302

DC ELECTRICAL CHARACTERISTICS

 (Unless otherwise specified, $V_{EE} = -30V$, $T_a = -40$ to $+85^\circ C$)

Parameter	Symbol	Condition	Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$V_{DD} = 5.0 \pm 10\%$ CSB, CLKB, DIN, RSTB	$0.7V_{DD}$	-	V
		$V_{DD} = 3.3 \pm 10\%$ CSB, CLKB, DIN, RSTB	$0.8V_{DD}$	-	V
Low Level Input Voltage	V_{IL}	$V_{DD} = 5.0 \pm 10\%$ CSB, CLKB, DIN, RSTB	-	$0.3V_{DD}$	V
		$V_{DD} = 3.3 \pm 10\%$ CSB, CLKB, DIN, RSTB	-	$0.2V_{DD}$	V
High Level Input Current	I_{IH}	$V_{DD} = 5.0 \pm 10\%$ CSB, CLKB, DIN, RSTB $V_{IH} = V_{DD}$	-1.0	1.0	μA
		$V_{DD} = 3.3 \pm 10\%$ CSB, CLKB, DIN, RSTB $V_{IH} = V_{DD}$	-1.0	1.0	μA
Low Level Input Current	I_{IL}	$V_{DD} = 5.0 \pm 10\%$ CSB, CLKB, DIN, RSTB $V_{IL} = 0V$	-1.0	1.0	μA
		$V_{DD} = 3.3 \pm 10\%$ CSB, CLKB, DIN, RSTB $V_{IL} = 0V$	-1.0	1.0	μA
High Level Output Voltage 1	V_{OH1}	$V_{DD} = 5.0 \pm 10\%$ GR1 to GR16 $I_{OH} = -30mA$	$V_{DD} - 1.5$	-	V
		$V_{DD} = 3.3 \pm 10\%$ GR1 to GR16 $I_{OH} = -30mA$	$V_{DD} - 1.5$	-	V

VFD Driver/Controller IC with Character RAM
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Parameter	Symbol	Condition	Min.	Max.	Unit
High Level Output Voltage 2	V_{OH2}	$V_{DD}=5.0\pm 10\%$ AD1 to AD2, $I_{OH}=-15\text{mA}$	$V_{DD}-1.5$	-	V
		$V_{DD}=3.3\pm 10\%$ AD1 to AD2, $I_{OH}=-15\text{mA}$	$V_{DD}-1.5$	-	V
High Level Output Voltage 3	V_{OH3}	$V_{DD}=5.0\pm 10\%$ SG1 to SG35, $I_{OH}=-6\text{mA}$	$V_{DD}-1.5$	-	V
		$V_{DD}=3.3\pm 10\%$ SG1 to SG35, $I_{OH}=-6\text{mA}$	$V_{DD}-1.5$	-	V
High Level Output Voltage 4	V_{OH4}	$V_{DD}=5.0\pm 10\%$ P1 to P2, $I_{OH}=-5\text{mA}$	$V_{DD}-1.0$	-	V
		$V_{DD}=3.3\pm 10\%$ P1 to P2, $I_{OH}=-2.5\text{mA}$	$V_{DD}-1.0$	-	V
Low Level Output Voltage 1	V_{OL1}	$V_{DD}=5.0\pm 10\%$ GR1 to GR16, AD1 to AD2, SG1 to SG35	-	$V_{EE}+1.0$	V
		$V_{DD}=3.3\pm 10\%$ GR1 to GR16, AD1 to AD2, SG1 to SG35		$V_{EE}+1.0$	V
Low Level Output Voltage	V_{OL2}	$V_{DD}=5.0\pm 10\%$ P1, P2, $I_{OL}=15\text{mA}$	-	1.0	V
		$V_{DD}=3.3\pm 10\%$ P1, P2, $I_{OL}=7.5\text{mA}$	-	1.0	V
Current Consumption 1	I_{DD1}	$V_{DD}=5.0\pm 10\%$ V_{DD} , fosc=2MHz, No Load Duty 15/16, DIGIT 1 to 16 All outputs lights ON	-	4	mA
		$V_{DD}=3.3\pm 10\%$ V_{DD} , fosc=2MHz, No Load Duty 15/16, DIGIT 1 to 16 All outputs lights ON	-	3	mA
Current Consumption 2	I_{DD2}	$V_{DD}=5.0\pm 10\%$ V_{DD} , fosc=2MHz, No Load Duty 8/16, DIGIT 1 to 9 All outputs lights OFF	-	3	mA
		$V_{DD}=3.3\pm 10\%$ V_{DD} , fosc=2MHz, No Load Duty 8/16, DIGIT 1 to 9 All outputs lights OFF	-	2	mA

VFD Driver/Controller IC with Character RAM
PT6302

AC CHARACTERISTICS

 (Unless otherwise specified, $V_{EE} = -30V$, $T_a = -40$ to $+85^{\circ}C$)

Parameter	Symbol	Condition	Min.	Max.	Unit
CLKB Cycle Time	fc	VDD = 5.0V + 10%	-	1.0	μs
		VDD = 3.3V + 10%	-	1.0	μs
CLKB Pulse Width	tCW	VDD = 5.0V + 10%	300	-	ns
		VDD = 3.3V + 10%	300	-	ns
DIN Setup Time	tDS	VDD = 5.0V + 10%	300	-	ns
		VDD = 3.3V + 10%	300	-	ns
DIN Hold Time	tDH	VDD = 5.0V + 10%	300	-	ns
		VDD = 3.3V + 10%	300	-	ns
CSB Setup Time	tCSS	VDD = 5.0V + 10%	300	-	ns
		VDD = 3.3V + 10%	300	-	ns
CSB Hold Time	tCSH	VDD = 5.0V + 10% R1=3.3kOhms, C1=47pF	16	-	μs
		VDD = 3.3V + 10% R1=3.3kOhms, C1=39pF	16	-	μs
CSB Wait Time	tCSW	VDD = 5.0V + 10%	300	-	ns
		VDD = 3.3V + 10%	300	-	ns
Data Processing Time	tDOFF	VDD = 5.0V + 10% R1=3.3kOhms, C1=47pF	8	-	μs
		VDD = 3.3V + 10% R1=3.3kOhms, C1=39pF	8	-	μs
RSTB Pulse Width	tWRSTB	VDD = 5.0V + 10% When the RSTB Signal is externally inputted from the microcontroller.	300	-	ns
		VDD = 3.3V + 10% When the RSTB Signal is externally inputted from the microcontroller.	300	-	ns

VFD Driver/Controller IC with Character RAM
PT6302

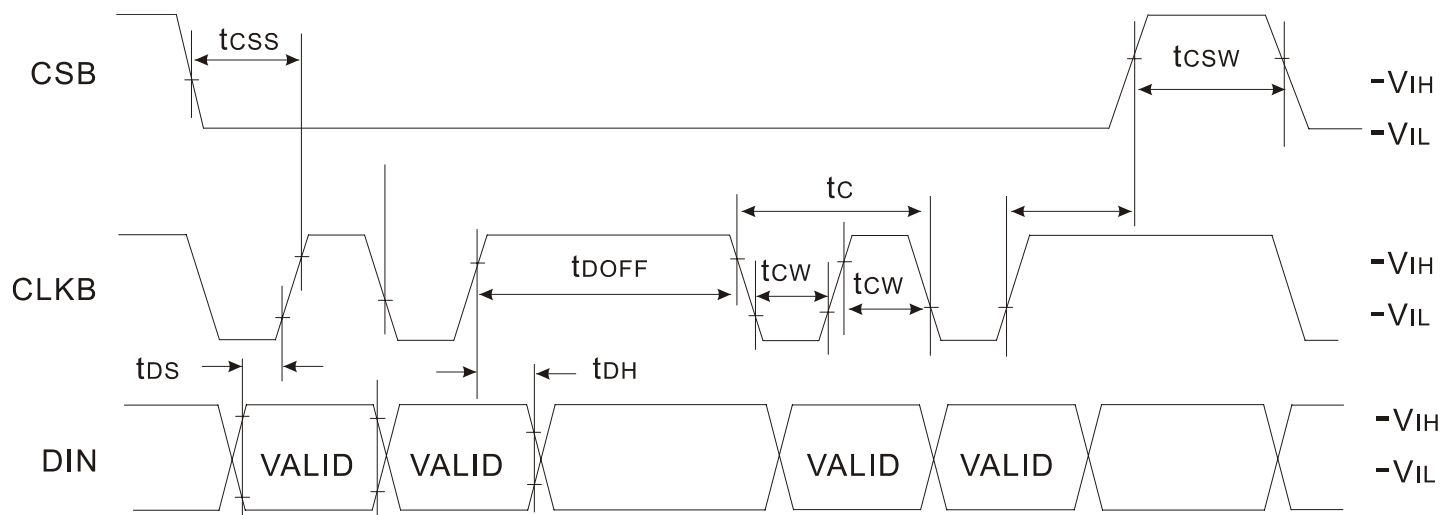
Parameter	Symbol	Condition	Min.	Max.	Unit
DIN Wait Time	tRSOFF	VDD = 5.0V + 10%	300	-	ns
		VDD = 3.3V + 10%	300	-	ns
All Outputs Slew Rate	tR	VDD = 5.0V + 10% Ci=100pF, tR=20% to 80%	-	4.0	μs
		VDD = 3.3V + 10% Ci=100pF, tR=20% to 80%	-	4.0	μs
	tF	VDD = 5.0V + 10% Ci=100pF, tF=80% to 20%	-	4.0	μs
		VDD = 3.3V + 10% Ci=100pF, tF=80% to 20%	-	4.0	μs
VDD Rise Time	tPRZ	VDD = 5.0V + 10% Mounted in the Unit	-	100	μs
		VDD = 3.3V + 10% Mounted in the Unit	-	100	μs
VDD Off Time	tPOF	VDD=0V Mounted in the Unit	5.0	-	ms

VFD Driver/Controller IC with Character RAM **PT6302**

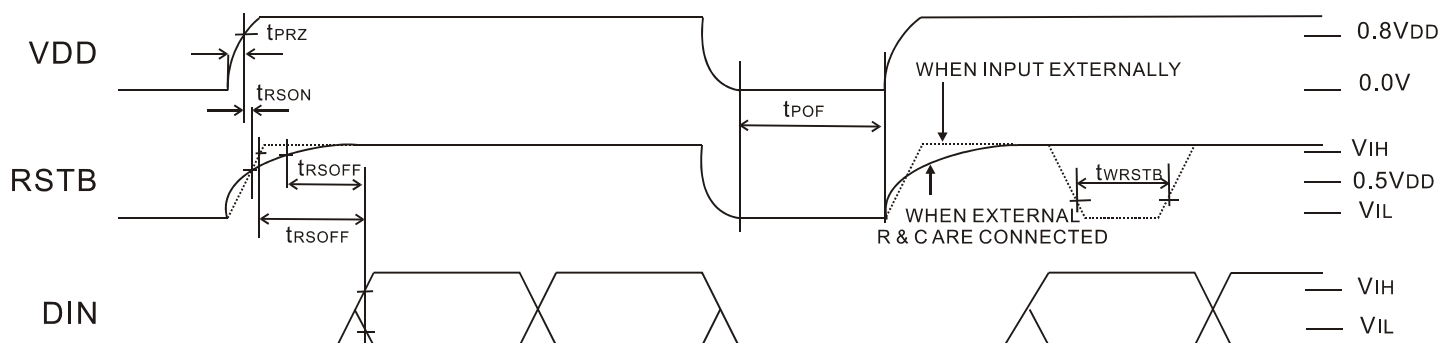
TIMING CHARACTERISTICS

Parameter	Symbol	VDD=3.3V ± 10%	VDD=5.0 ± 10%
High Level Input Voltage	V _{IH}	0.8V _{DD}	0.7V _{DD}
Low Level Input Voltage	V _{IL}	0.2V _{DD}	0.3V _{DD}

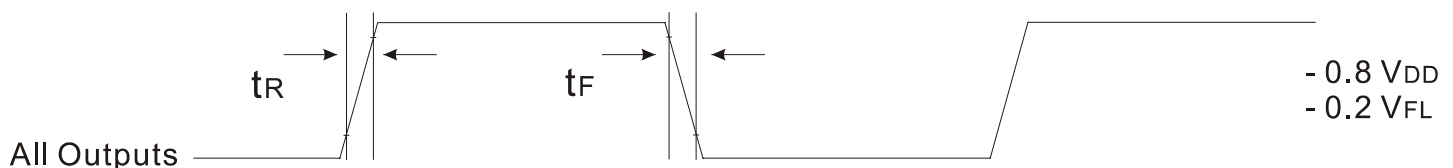
DATA TIMING



RESET (RSTB) TIMING

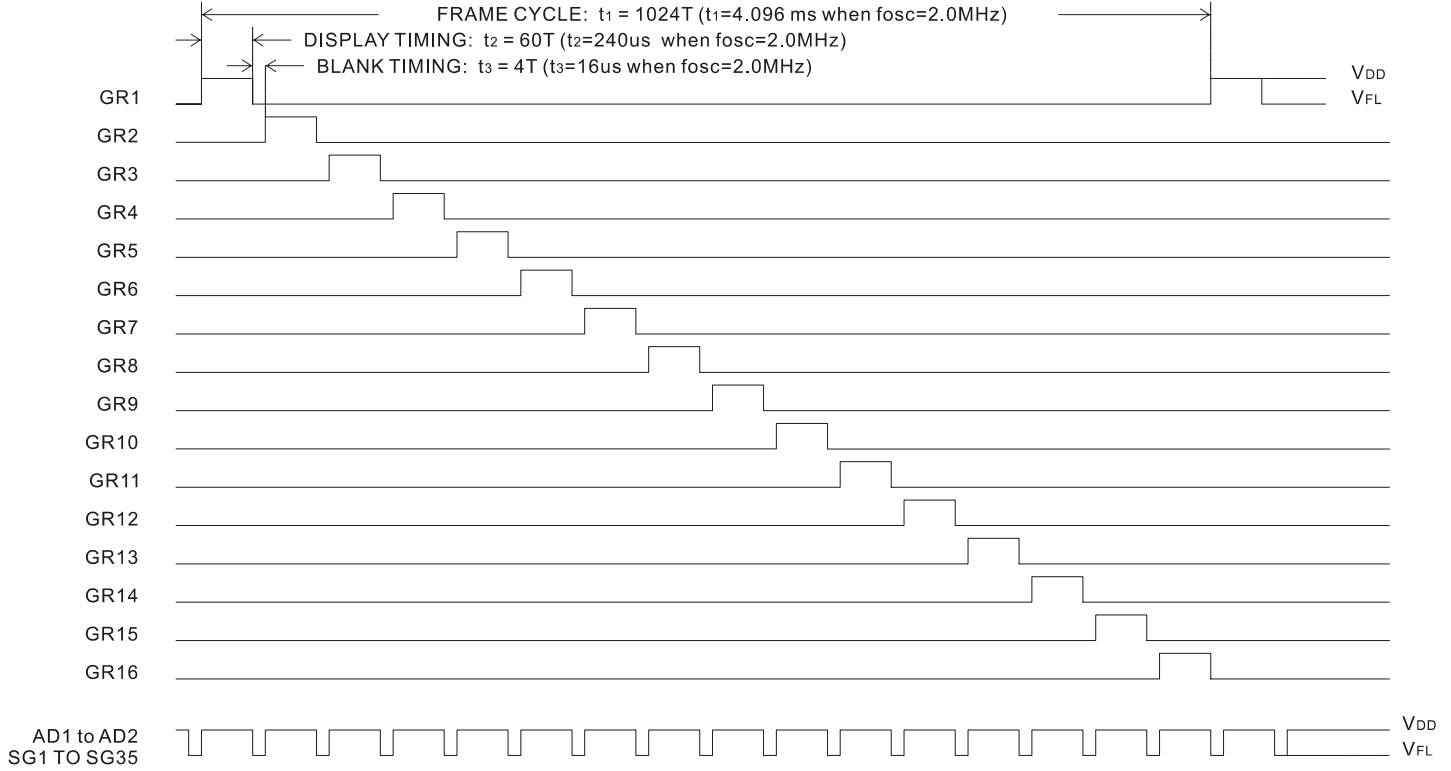


OUTPUT TIMING



VFD Driver/Controller IC with Character RAM **PT6302**

DIGIT OUTPUT TIMING (16-DIGIT DISPLAY, DUTY= 15/16)

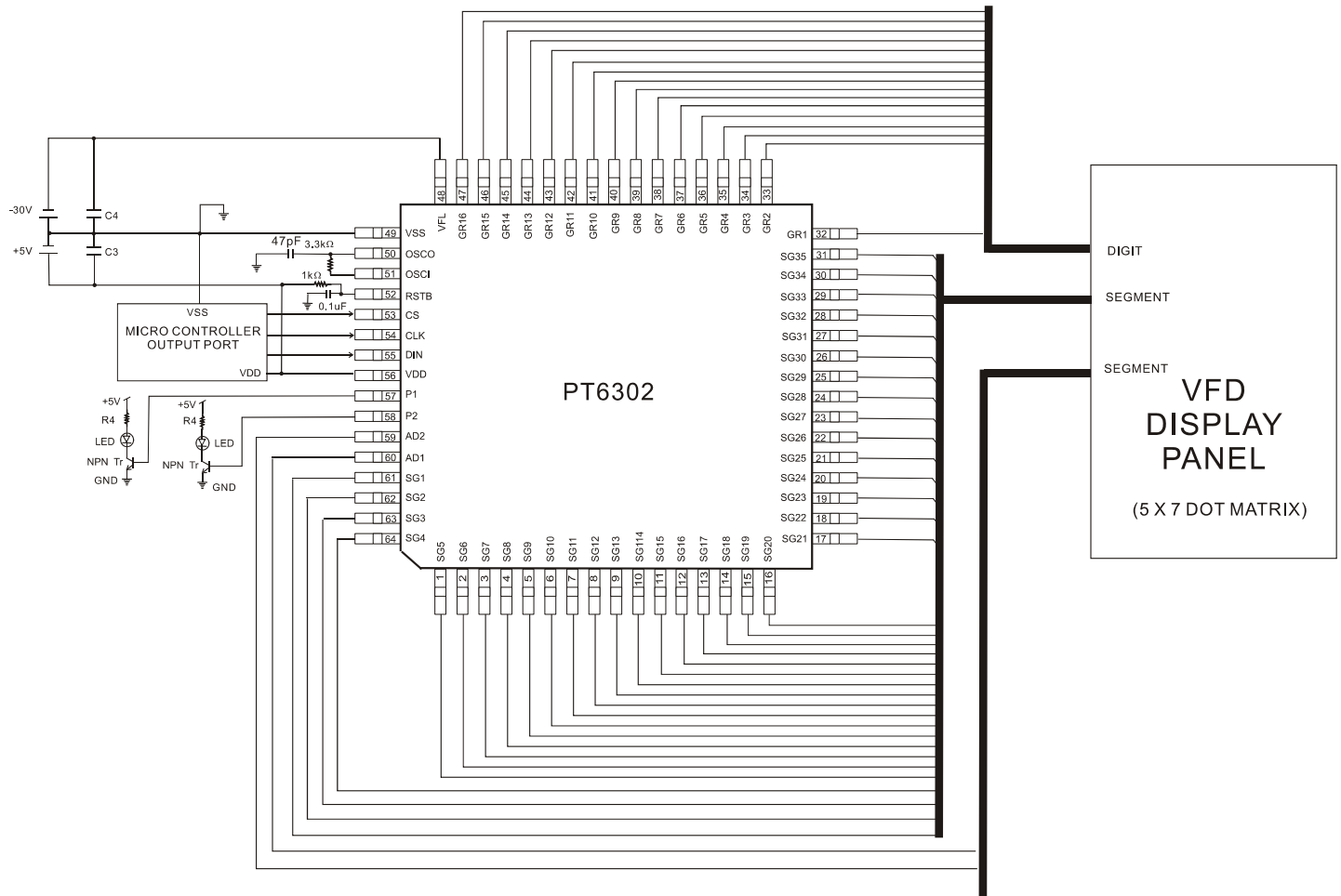


where: $T=8/f_{osc}$

VFD Driver/Controller IC with Character RAM

PT6302

APPLICATION CIRCUIT



PT6302-001 CHARACTER FONT TABLE

MSB \ LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 RAM0	一		0	0	P											
1 RAM1	P	!	1	A	Q	a	q	手	山	十						
2 RAM2	千	"	2	B	R	b	r	ウ	人	中						
3 RAM3	口	#	3	C	S	c	s	テ	毛	毛						
4 RAM4	工	\$	4	O	T	d	t	ト	尸	天						
5 RAM5	才	%	5	E	U	e	u	十	工	羊						
6 RAM6	力	&	6	F	V	f	v	二	日	十						
7 RAM7	井	'	7	G	W	w	ワ	ウ	三	十						
8	十	0	8	H	X	h	x	卒	人	十						
9	古	1	9	I	Y	y	ウ	人	山	十						
A	五	口	*	:	J	j	z	山	山	山						
B	才	才	+	:	K	k	山	山	山	山						
C	才	山	.	<	L	l	山	山	山	山						
D	山	又	-	=	M	m	山	山	山	山						
E	山	山	.	>	N	n	山	山	山	山						
F	山	山	/	?	O	山	山	山	山	山						

PT6302-002 CHARACTER FONT TABLE

MSB \ LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0	□	□	0	1	2	3	4	5	6	7	8	9	0	1	2
0001	RAM1	□	!	T	A	Q	a	q	×	○	。	ア	キ	△	□	□
0010	RAM2	□	"	2	B	R	b	r	●	□	「	イ	ウ	又	□	□
0011	RAM3	□	#	3	C	S	c	s	!	□	」	ウ	テ	モ	□	□
0100	RAM4	□	\$	4	D	T	d	t	\	□	√	エ	ト	巾	□	□
0101	RAM5	□	%	5	E	U	e	u	×	□	•	オ	ト	工	□	□
0110	RAM6	□	&	6	F	V	f	v	÷	□	ヨ	カ	ニ	ヨ	□	□
0111	RAM7	□	'	7	G	W	g	w	†	□	ア	キ	又	ウ	□	□
1000		□	(8	H	X	h	x	+	□	イ	夕	幸	製	□	□
1001		□)	9	I	Y	i	y	!	□	ウ	夕	人	ル	□	□
1010		□	.	*	:	J	Z	j	z	□	エ	コ	白	ル	□	□
1011		□	+	;	<	K	L	k	l	□	オ	サ	白	口	□	□
1100		□	,	<	<	羊	1	1	△	□	カ	ウ	フ	ウ	□	□
1101		□	-	=	冂	I	m	ノ	ノ	□	ユ	又	ウ	ウ	□	□
1110		□	.	<	N	ˆ	n	一	田	□	ヨ	セ	市	"	□	□
1111		□	/	?	0	□	□	■	田	□	ウ	ウ	又	□	□	□

PT6302-003 CHARACTER FONT TABLE

MSB \ LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
0000	RAM0																
0001	RAM1																
0010	RAM2																
0011	RAM3																
0100	RAM4																
0101	RAM5																
0110	RAM6																
0111	RAM7																
1000																	
1001																	
1010																	
1011																	
1100																	
1101																	
1110																	
1111																	

PT6302-004 CHARACTER FONT TABLE

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		—		0	0	P		P	0	3		°	Δ	Δ	Δ	Δ
1		7	!	1	A	Q	a	9	7	4	i	±	Δ	Δ	Δ	Δ
2				2	B	R	b	r	U	X	φ	2	Δ	Δ	Δ	Δ
3				3	C	S	c	s	T	E	E	3	Δ	Δ	Δ	Δ
4				4	D	T	d	t								
5				5	E	U	e	u								
6				6	F	V	f	v								
7				7	G	W	w									
8				8	H	X	h	x								
9				9	I	Y	y									
A				A	J	Z	j	z								
B				B	K	L	k	l								
C				C	L	N	l	n								
D				D	M	I	m	i								
E				E	N	^	n									
F				F	O	_	o									

PT6302-005 CHARACTER FONT TABLE

MSB b7 b6 b5 b4 LSB	0				1				1				1			
	b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	CG RAM0	α	β	θ	ρ	ε	φ	ε	θ	β	υ	δ	δ	δ	δ
0001	1	CG RAM1	β	!	1	A	Q	a	7	0	æ	1	Π	4	θ	±
0010	2	CG RAM2	Π	"	2	B	R	b	r	ε	θ	Δ	U	ε	δ	ε
0011	3	CG RAM3	π	#	3	C	S	c	s	θ	θ	θ	θ	θ	θ	θ
0100	4	CG RAM4	ε	\$	4	D	T	d	t	θ	θ	θ	θ	θ	θ	θ
0101	5	CG RAM5	θ	%	5	E	U	e	u	θ	θ	θ	θ	θ	θ	θ
0110	6	CG RAM6	θ	&	6	F	V	f	v	θ	θ	θ	θ	θ	θ	θ
0111	7	CG RAM7	π	'	7	G	W	w	g	θ	θ	θ	θ	θ	θ	θ
1000	8		ε	ε	0	H	X	h	x	θ	θ	θ	θ	θ	θ	θ
1001	9		ε	θ)	9	I	Y	i	y	θ	θ	θ	θ	θ	θ
1010	A		ε	θ	*	:	J	Z	j	z	θ	θ	θ	θ	θ	θ
1011	B		ε	θ	+	ε	K	Q	k	q	θ	θ	θ	θ	θ	θ
1100	C		ε	θ	,	<	L	\	l	ε	θ	θ	θ	θ	θ	θ
1101	D		ε	θ	-	ε	M	Q	m	q	θ	θ	θ	θ	θ	θ
1110	E		ε	θ	.	>	N	^	n	^	θ	θ	θ	θ	θ	θ
1111	F		ε	θ	/	?	O	Q	o	q	θ	θ	θ	θ	θ	θ

PT6302-006 CHARACTER FONT TABLE

D3 D2 D1 D0	D7	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	D6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	
	D5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	
	D4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 0 0 0	0	RAM0	—	SP	0	P	Q	R	S	T	U	V	W	X	Y	Z	
0 0 0 1	1	RAM1	!	"	#	\$	%	&	'	()	*	+	,	-	=	
0 0 1 0	2	RAM2	1	2	3	4	5	6	7	8	9	:	;	<	=	?	
0 0 1 1	3	RAM3	A	B	C	D	E	F	G	H	I	J	K	L	M	N	
0 1 0 0	4	RAM4	a	b	c	d	e	f	g	h	i	j	k	l	m	n	
0 1 0 1	5	RAM5	o	p	q	r	s	t	u	v	w	x	y	z	{	}	
0 1 1 0	6	RAM6	[\]	^	_	`	{		}	~	?	@	A	B	
0 1 1 1	7	RAM7	!	"	#	\$	%	&	'	()	*	+	,	-	=	
1 0 0 0	8		0	1	2	3	4	5	6	7	8	9	:	;	<	=	
1 0 0 1	9		A	B	C	D	E	F	G	H	I	J	K	L	M	N	
1 0 1 0	A		a	b	c	d	e	f	g	h	i	j	k	l	m	n	
1 0 1 1	B		o	p	q	r	s	t	u	v	w	x	y	z	{	}	
1 1 0 0	C		[\]	^	_	`	{		}	~	?	@	A	B	
1 1 0 1	D		!	"	#	\$	%	&	'	()	*	+	,	-	=	
1 1 1 0	E		0	1	2	3	4	5	6	7	8	9	:	;	<	=	
1 1 1 1	F		A	B	C	D	E	F	G	H	I	J	K	L	M	N	

PT6302-007 CHARACTER FONT TABLE

MSB \ LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011
0000	RAM0			0	1	2	3	4	5	6	7	8
0001	RAM1		!	A	Q	a	q	8	3	0		
0010	RAM2		"	2	R	r	e	0				
0011	RAM3		#	3	S	s	e	0				
0100	RAM4		4	T	t	i	i	0				
0101	RAM5		5	U	u	i	i	0				
0110	RAM6		6	V	v	0	0					
0111	RAM7		7	W	w	0	0					
1000			8	H	h	x	0	0				
1001			9	I	y	0	0					
1010			*	J	j	0	0					
1011			+	K	k	0	0					
1100			,	L	l	S	S					
1101			=	M	m	0	0					
1110			.	N	n	i	i					
1111			/	? 0	0	0	0					

ORDERING INFORMATION

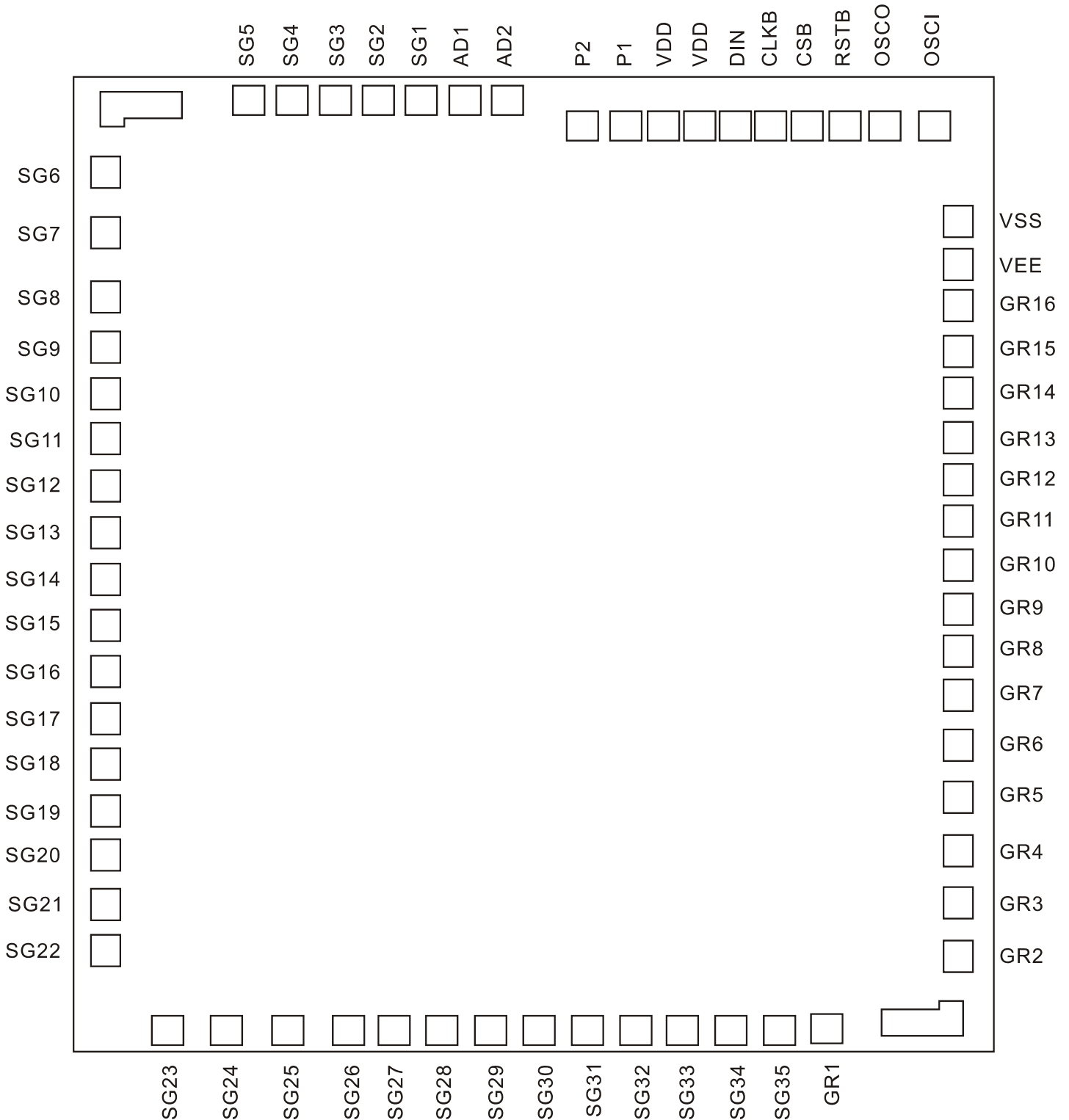
Order Part Number	Package Type	Top Code
PT6302LQ-001	64-pin LQFP	PT6302LQ-001
PT6302-R-001	64-pin SSOP	PT6302-R-001
PT6302LQ-002	64-pin LQFP	PT6302LQ-002
PT6302-R-002	64-pin SSOP	PT6302-R-002
PT6302-R-003	64-pin, SSOP	PT6302-R-003
PT6302LQ-003	64-pin, LQFP	PT6302LQ-003
PT6302-003-H	CIG	-
PT6302-R-004	64-pin, SSOP	PT6302-R-004
PT6302LQ-004	64-pin, LQFP	PT6302LQ-004
PT6302-R-005	64-pin, SSOP	PT6302-R-005
PT6302LQ-005	64-pin, LQFP	PT6302LQ-005
PT6302-R-006	64-pin, SSOP	PT6302-R-006
PT6302LQ-006	64-pin, LQFP	PT6302LQ-006
PT6302-007-H	CIG	-
PT6302LQ-001 (L)	64-pin LQFP	PT6302LQ-001
PT6302-R-001(L)	64-pin SSOP	PT6302-R-001
PT6302LQ-002 (L)	64-pin LQFP	PT6302LQ-002
PT6302-R-002 (L)	64-pin SSOP	PT6302-R-002
PT6302-R-003 (L)	64-pin, SSOP	PT6302-R-003
PT6302LQ-003 (L)	64-pin, LQFP	PT6302LQ-003
PT6302-R-004 (L)	64-pin, SSOP	PT6302-R-004
PT6302LQ-004 (L)	64-pin, LQFP	PT6302LQ-004
PT6302-R-005 (L)	64-pin, SSOP	PT6302-R-005
PT6302LQ-005 (L)	64-pin, LQFP	PT6302LQ-005
PT6302-R-006 (L)	64-pin, SSOP	PT6302-R-006
PT6302LQ-006 (L)	64-pin, LQFP	PT6302LQ-006

Notes:

1. (L) = Lead Free
2. The Lead Free mark is put in front of the date code.

VFD Driver/Controller IC with Character RAM **PT6302**

PAD CONFIGURATION



VFD Driver/Controller IC with Character RAM
PT6302

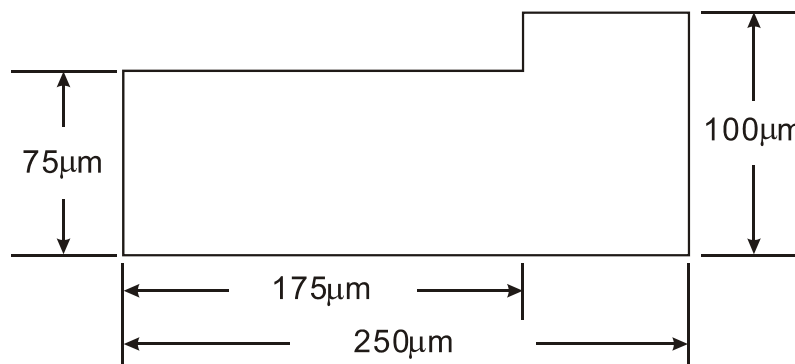
PAD LOCATION

Pad No.	Pad Name	Location
1	SG5	[478.600, 2852.100]
2	SG6	[50.000, 2637.500]
3	SG7	[50.000, 2447.500]
4	SG8	[50.000, 2257.500]
5	SG9	[50.000, 2107.500]
6	SG10	[50.000, 1967.500]
7	SG11	[50.000, 1827.500]
8	SG12	[50.000, 1687.500]
9	SG13	[50.000, 1547.500]
10	SG14	[50.000, 1407.500]
11	SG15	[50.000, 1267.500]
12	SG16	[50.000, 1127.500]
13	SG17	[50.000, 987.500]
14	SG18	[50.000, 847.500]
15	SG19	[50.000, 707.500]
16	SG20	[50.000, 567.500]
17	SG21	[50.000, 427.500]
18	SG22	[50.000, 287.500]
19	SG23	[233.800, 50.000]
20	SG24	[413.800, 50.000]
21	SG25	[593.800, 50.000]
22	SG26	[773.800, 50.000]
23	SG27	[918.800, 50.000]
24	SG28	[1063.800, 50.000]
25	SG29	[1208.800, 50.000]
26	SG30	[1353.800, 50.000]
27	SG31	[1498.800, 50.000]
28	SG32	[1643.800, 50.000]
29	SG33	[1788.800, 50.000]
30	SG34	[1933.800, 50.000]
31	SG35	[2078.800, 50.000]
32	GR1	[2223.800, 50.000]
33	GR2	[2615.800, 267.200]
34	GR3	[2615.800, 427.200]
35	GR4	[2615.800, 587.200]
36	GR5	[2615.800, 747.200]
37	GR6	[2615.800, 907.200]
38	GR7	[2615.800, 1057.200]
39	GR8	[2615.800, 1187.200]

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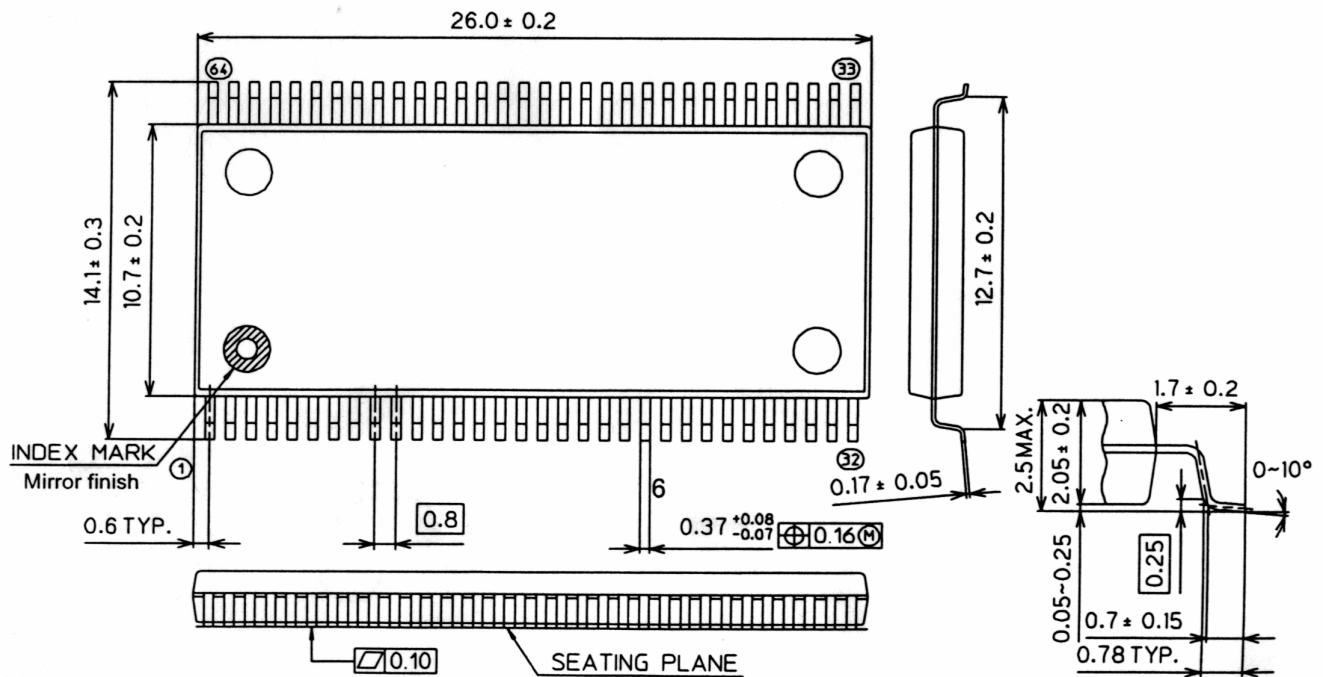
Pad No.	Pad Name	Location
40	GR9	[2615.800, 1317.200]
41	GR10	[2615.800, 1447.200]
42	GR11	[2615.800, 1577.200]
43	GR12	[2615.800, 1707.200]
44	GR13	[2615.800, 1837.200]
45	GR14	[2615.800, 1967.200]
46	GR15	[2615.800, 2097.200]
47	GR16	[2615.800, 2227.200]
48	VEE	[2615.800, 2357.200]
49	VSS	[2615.800, 2487.200]
50	OSCI	[2543.700, 2772.300]
51	OSCO	[2395.900, 2772.300]
52	RSTB	[2277.900, 2772.300]
53	CSB	[2167.900, 2772.300]
54	CLKB	[2057.900, 2772.300]
55	DIN	[1947.900, 2772.300]
56	VDD	[1837.900, 2772.300]
56	VDD	[1727.900, 2772.300]
57	P1	[1615.300, 2772.300]
58	P2	[1490.100, 2772.300]
59	AD2	[1258.600, 2852.100]
60	AD1	[1128.600, 2852.100]
61	SG1	[998.600, 2852.100]
62	SG2	[868.600, 2852.100]
63	SG3	[738.600, 2852.100]
64	SG4	[608.600, 2852.100]

ALIGNMENT MARK DIMENSION



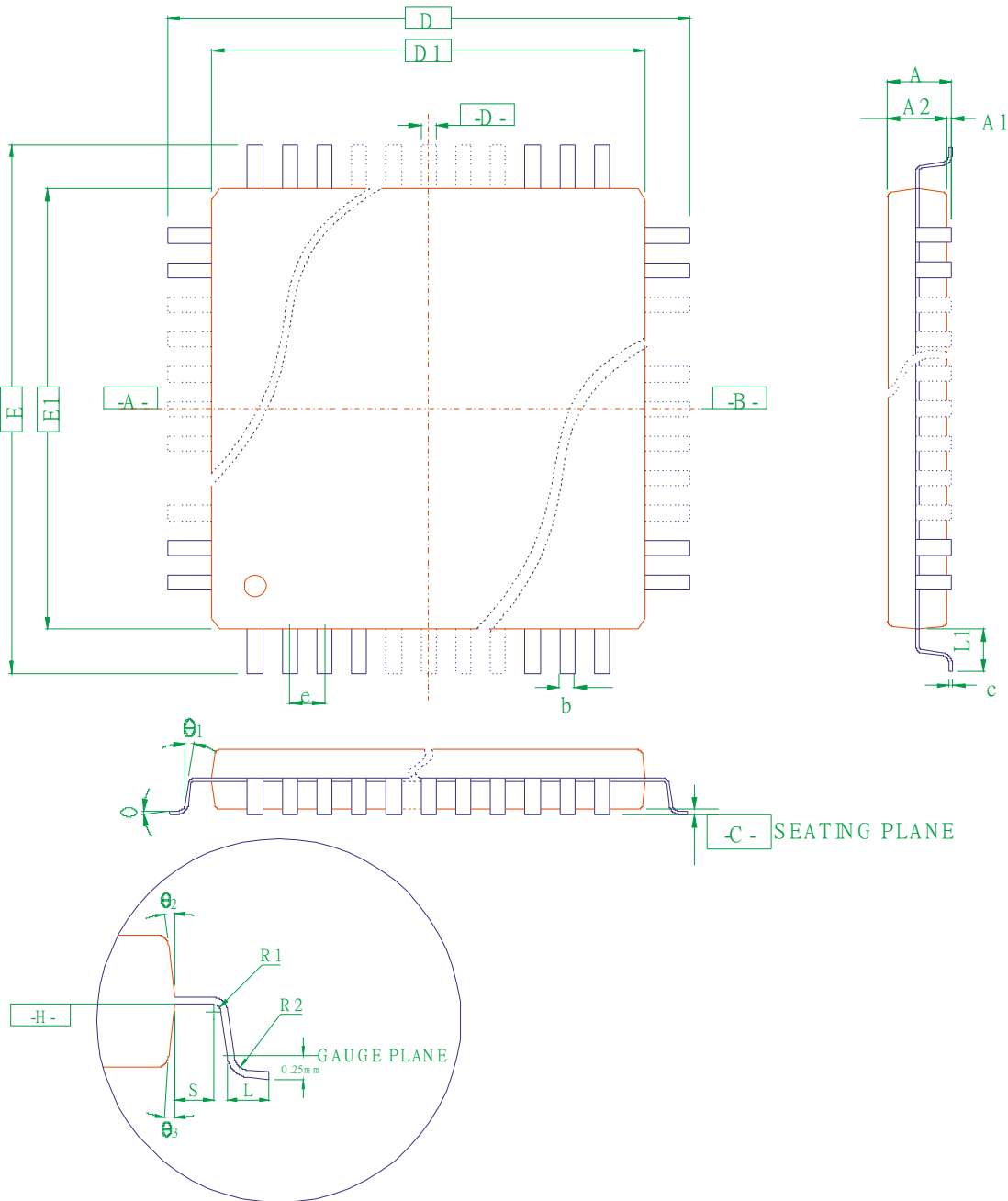
PACKAGE INFORMATION

64 PINS, SSOP PACKAGE



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64 PINS, LQFP PACKAGE
(BODY SIZE: 14MM X 14MM, PITCH: 0.8MM, THK BODY: 1.40MM)



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Symbol	Min.	Typ.	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	16.00 BSC		
D1	14.00 BSC		
e	0.80 BSC		
E	16.00 BSC		
E1	14.00 BSC		
θ	0°	3.5°	7°
$\theta 1$	0°	-	-
$\theta 2$	11°	12°	13°
$\theta 3$	11°	12°	13°
C	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994
2. The top package body size may be smaller than the bottom package size by as much as 0.15mm.
3. Datum A-B and D to be determined at the datum plane H.
4. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Controlling Dimension: MILLIMETER
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius or the foot. Minimum space between the protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm PITCH Package.
7. These dimensions apply to the flat section of the lead between 0.10mm and 0.25mm from the lead tip.
8. A1 is defined as the distance from the seating plane to the lowest point on the package body.
9. Details of pin 1 identifier are optional but must be located within the zone identified.
10. Dimension D2 and E2 show the minimum allowed for the optional exposed heat slug. The maximum allowed is equal to the package body size (D1 and E1). However, the size of the exposed heat slug is variable depending on the device function (die size). End users should verify the actual size or either top or bottom exposed thermal pad for specific device application.
11. Refer to JEDEC MS-026 Variation BEB.

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