HIGH-VOLTAGE DIGITAL-SIGNAL IC

UCi7702

240-Output LCD SEG/COM Driver

MP Specifications **May 18, 2017**

ULTRACHIP

The Coolest Source Driver, Ever!

Table of Content

UCi7702

240-Output LCD SEG/COM Driver

INTRODUCTION

UCi7702c is a 240-bit output SEG/COM driver LSI, suitable for driving the large scale dot matrix LCD panels used by PDA's, personal computers and work stations for example. Through the use of SST (Super Slim TCP) technology, it is ideal for substantially decreasing the size of the frame section of the LCD module.

UCi7702c is good as both a SEG driver and a COM driver. A low power consuming, high-precision LCD panel display can be assembled using the UCi7702c. In SEG mode, the data input is selected 4-bit parallel input mode or as 8-bit parallel input mode by a mode pin (MD). In COM mode, the data input/output pins are bi-directional and the four data shift directions are pin-selectable.

FEATURE HIGHLIGHTS

(SEG mode)

- Shift Clock frequency :
  – 20 MHz (Max.) (V_{DD} = 5V ± 10%)
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode pin (MD)
- Automatic transfer function with an enable signal
- Automatic counting function when in the chip select mode, causes the internal clock to be stopped by automatically counting 240 bits of input data

(COM mode)

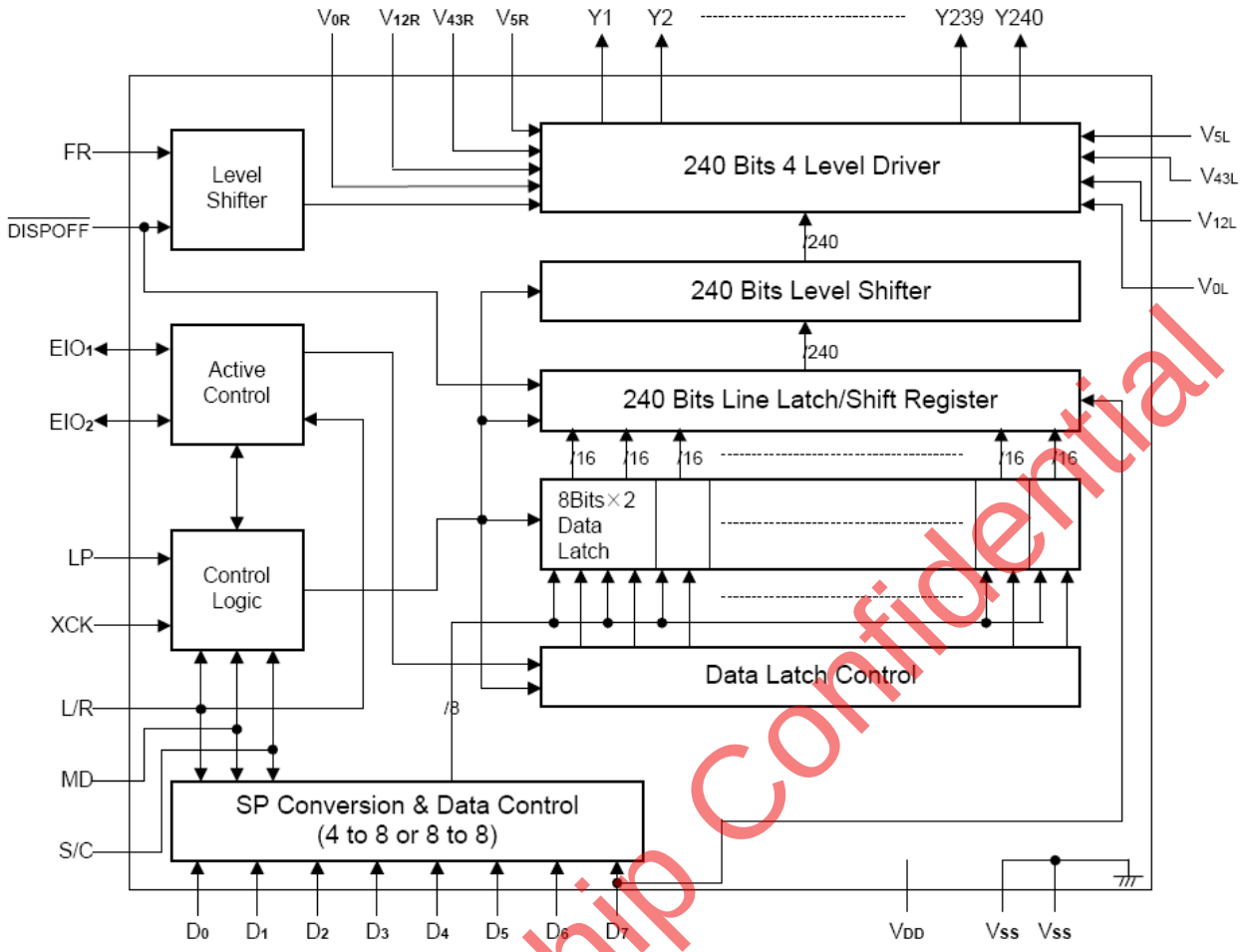
- Shift clock frequency: 4.0MHz (Max.)
- Built-in 240-bit bi-directional shift register (divisible into 120-bit x 2)
- 4 pin-selectable shift directions available in single mode (240-bit shift register) or dual mode (120-bit shift register x 2)
  1. Y1 → Y240 (Single mode)
  2. Y240 → Y1 (Single mode)
  3. Y1 → Y120, Y121 → Y240 (Dual mode)
  4. Y240 → Y121, Y120 → Y1 (Dual mode)

(Both SEG mode and COM mode)

- Supply voltage for LCD drive: 15.0 to 42.0V
- Number of LCD driver outputs: 240
- Low output impedance
- Low power consumption
- Supply voltage for the logic system: +2.5 to +5.5V
- COMs process
- Package: 272-pin TCP (Tape Carrier Package)
- Not designed or rated as radiation hardened

Remark: Contact UltraChip for a visual inspection document of COG (03-DOC-131) or Film (03-DOC-214).

BLOCK DIAGRAM



Level Shifter The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

Active Control In the case of segment mode, controls the selection or deselection of the chip. Following a LP signal input, and after the select signal is input, a select signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the ship is deselected. In the case of common mode, controls the input/output data of bidirectional pins.

Control Logic It controls the operation of each block. In the case of the segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 240 bits of data are read in, and the chip is deselected. In the case of the common mode, it controls the direction of the data shift.

SP Conversion & Data Control In the case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

4-Level Driver It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V0, V12, V43, Vss) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

Data Latch Control In the case of the segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

Line Latch / Shift Register In the case of the segment mode, all 240 bits which have been read into the data latch, are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block. In the case of the common mode, shifts data from the data input pin on to the falling edge of the LP signal.

Data Latch In the case of the segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control 240 bits of data are read in 30 sets of 8 bits.

ORDERING INFORMATION

Part Number	Description
UCi7702cGAA	Bump on Chip Tray
UCi7702cTAA	TCP Form
UCi7702cTDA	TCP Form

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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CAUTIONS CONCERNING STORAGE

1. When storing the product, it is recommended that it be left in its shipping package.
   After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
2. Storage conditions :

Storage state	Storage conditions
Unopened (less than 90 days)	Temperature: 5 to 30°C; humidity: 80%RH or less
After seal of broken (less than 30 days)	Room temperature, dry nitrogen atmosphere

3. Don't store in a location exposed to corrosive gas or excessive dust.
4. Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
5. Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
6. Deterioration of the plating may occur after long-term storage, so special care is required.
   It is recommended that the products be inspected before use.

CONTACT DETAILS

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PIN DESCRIPTION

: Number of Pads

<table>
<tr><th>Pin Name (Pad Name)</th><th>Type</th><th>#</th><th>Description</th></tr>
<tr><td>VDD</td><td>PWR</td><td>3</td><td>Power supply pin for the logic system (+2.5 to +5.5V)</td></tr>
<tr><td>Vss</td><td>GND</td><td>12</td><td>Ground (0V).</td></tr>
<tr><td>V0R, V0L (V0)
V12R, V12L (V12)
V43R, V43L (V34)
V5R, V5L (V5)</td><td>PWR</td><td>1, 1
1, 1
1, 1
1, 1</td><td>Bias power supply pin for LCD driver voltage.
Normally, the bias voltages are set by a resistor divider.
Ensure that voltages are set such that Vss ≤ V5 < V34 < V12 < V0.
To reduce the differences between the output waveforms of the LCD driver output pins Y1 and Y240, connect externally V0R and V0L, V12R and V12L, V43R and V43L, respectively.</td></tr>
<tr><td>D7 ~ D0 (DI7~DI0)</td><td>I</td><td>8</td><td>For COM mode
Data input for Dual mode. According to the data shift direction of the data shift register, data can be input starting from the 81st bit.
<table>
<tr><th></th><th>D7</th><th>D6~D0</th></tr>
<tr><td>Single mode</td><td>won't be pulled down</td><td rowspan="2">Not used. Connect to VDD or Vss to avoid floating.</td></tr>
<tr><td>Dual mode</td><td>will be pulled down</td></tr>
</table>
For SEG mode
Input for Display data
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>4-bit mode</td><td colspan="4">Connect to VDD or Vss</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td></tr>
<tr><td>8-bit mode</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td></tr>
</table></td></tr>
<tr><td>XCK</td><td>I</td><td>1</td><td>For COM mode
Not used. Pull down and connect to Vss or leave it open.
For SEG mode
Clock input for display data. Data are read on the falling edge of clock pulse.</td></tr>
<tr><td>LP</td><td>I</td><td>1</td><td>For COM mode
Shift clock input for bi-directional shift register. Data are shifted at the falling edge of clock pulse.
For SEG mode
Latch pulse input for display data. Data are latched on the falling edge of clock pulse.</td></tr>
<tr><td>L/R</td><td>I</td><td>1</td><td>Shift direction (Left / Right) selection for reading display data.
When L/R is set to “L” (Vss level), data are read sequentially from Y240 to Y1.
When L/R is set to “H” (VDD level), data are read sequentially from Y1 to Y240.</td></tr>
<tr><td>$\overline{\text{DISPOFF}}$
(/DISPOFF)</td><td>I</td><td>1</td><td>Control for output of non-select level. The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit.
When set to “L”, the LCD drive output pins (Y1~Y240) are set to level V5 and the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of $\overline{\text{DISPOFF}}$. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs non-select level (V12 or V34), then outputs the contents of the data latch on the next falling edge of the LP. At that time, if $\overline{\text{DISPOFF}}$ removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly.</td></tr>
<tr><td>FR</td><td>I</td><td>1</td><td>AC-converting signal input for LCD driver waveform. The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. Normally it inputs a frame inversion signal. The LCD drive output pins' output voltage level can be set using the line latch output signal and the FR signal.</td></tr>
</table>

<table>
<tr><th>Pin Name (Pad Name)</th><th>Type</th><th>#</th><th>Description</th></tr>
<tr><td>MD</td><td>I</td><td>1</td><td>Single or Dual (or 4-bit or 8-bit) Mode selection.
For COM mode
When MD is set to “L”, Single mode is selected.
When MD is set to “H”, Dual mode is selected.

For SEG mode
When MD is set to “L”, 8-bit parallel input mode is selected.
When MD is set to “H”, 4-bit parallel input mode is selected.</td></tr>
<tr><td>S/C</td><td>I</td><td>1</td><td>SEG mode / COM mode selection.
When S/C is set to “L”, COM mode is selected.
When S/C is set to “H”, SEG mode is selected.</td></tr>
<tr><td>EIO1, EIO2</td><td>I/O</td><td>1, 1</td><td>For COM mode
Data input / output for the bi-directional shift register.
<table>
<tr><td></td><td>EIO2</td><td>EIO1</td></tr>
<tr><td>L/R=”L”</td><td>used as input. pulled down.</td><td>used as output</td></tr>
<tr><td>L/R=”H”</td><td>used as output</td><td>used as input. pulled down</td></tr>
</table>
For SEG mode
Input / output for chip select.
<table>
<tr><td></td><td>EIO2</td><td>EIO1</td></tr>
<tr><td>L/R=”L”</td><td>used as input</td><td>used as output</td></tr>
<tr><td>L/R=”H”</td><td>used as output</td><td>used as input</td></tr>
</table>
During output, it’s set to "H" while LP • XCK is "H" and after 240 bits of data have been read, it’s set to "L" for one cycle (from one falling edge to its next falling edge of XCK), after which it returns to "H".
During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is deselected after 240 bits of data have been read.</td></tr>
<tr><td>Y240 ~ Y1</td><td>O</td><td>240</td><td>LCD driver output.
Corresponding directly to each bit of the data latch, one level (V0, V12, V34, or V5) is selected and output.</td></tr>
<tr><td>Dummy</td><td></td><td>52</td><td>No connection.</td></tr>
</table>

S/C	MD
L: COM mode	L : SINGLE mode
	H: DUAL mode
H: SEG mode	L: 8-bit mode
	H: 4-bit mode

S/C	L/R		
L: COM mode	L: Data shifted Y240 → Y1,	EIO2 for input,	EIO1 for output
	H: Data shifted Y1 → Y240,	EIO2 for output,	EIO1 for input
H: SEG mode	L: Data shifted Y240 → Y1,	EIO2 for input,	EIO1 for output
	H: Data shifted Y1 → Y240,	EIO2 for output,	EIO1 for input

FUNCTIONAL OPERATIONS

1. LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

1.1. Segment Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y1 ~ Y240)
L	L	H	V43
L	H	H	V5
H	L	H	V12
H	H	H	V0
X	X	L	V5

Remark:
VSS ≤ V5 < V43 < V12 <V0,
H: VDD (+2.5 to +5.5V),
L: VSS (0V),
X: Don't care

1.2. Common Mode

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level (Y1 ~ Y240)
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	V5
X	X	L	V5

Remark:
VSS ≤ V5 < V43 < V12 < V0,
H: VDD (+2.5 to +5.5V),
L: Vss (0V),
X: Don't care

Note:
1. There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which assigned by specification for each power pin.
2. That time "Don't care" should be fixed to "H" or "L", avoiding floating.

2. Relationship between the Display Data and Driver Output Pins

2.1. SEG Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					60clock	59clock	58clcok	…	3clock	2clock	1clock
H	L	Output	Input	D0	Y1	Y5	Y9	…	Y229	Y233	Y237
				D1	Y2	Y6	Y10	…	Y230	Y234	Y238
				D2	Y3	Y7	Y11	…	Y231	Y235	Y239
				D3	Y4	Y8	Y12	…	Y232	Y236	Y240
H	H	Input	Output	D0	Y240	Y236	Y232	…	Y12	Y8	Y4
				D1	Y239	Y235	Y231	…	Y11	Y7	Y3
				D2	Y238	Y234	Y230	…	Y10	Y6	Y2
				D3	Y237	Y233	Y229	…	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					30clock	29clock	28clcok	…	3clock	2clock	1clock
L	L	Output	Input	D0	Y1	Y9	Y17	…	Y217	Y225	Y233
				D1	Y2	Y10	Y18	…	Y218	Y226	Y234
				D2	Y3	Y11	Y19	…	Y219	Y227	Y235
				D3	Y4	Y12	Y20	…	Y220	Y228	Y236
				D4	Y5	Y13	Y21	…	Y221	Y229	Y237
				D5	Y6	Y14	Y22	…	Y222	Y230	Y238
				D6	Y7	Y15	Y23	…	Y223	Y231	Y239
				D7	Y8	Y16	Y24	…	Y224	Y232	Y240
L	H	Input	Output	D0	Y240	Y232	Y224	…	Y24	Y16	Y8
				D1	Y239	Y231	Y223	…	Y23	Y15	Y7
				D2	Y238	Y230	Y222	…	Y22	Y14	Y6
				D3	Y237	Y229	Y221	…	Y21	Y13	Y5
				D4	Y236	Y228	Y220	…	Y20	Y12	Y4
				D5	Y235	Y227	Y219	…	Y19	Y11	Y3
				D6	Y234	Y226	Y218	…	Y18	Y10	Y2
				D7	Y233	Y225	Y217	…	Y17	Y9	Y1

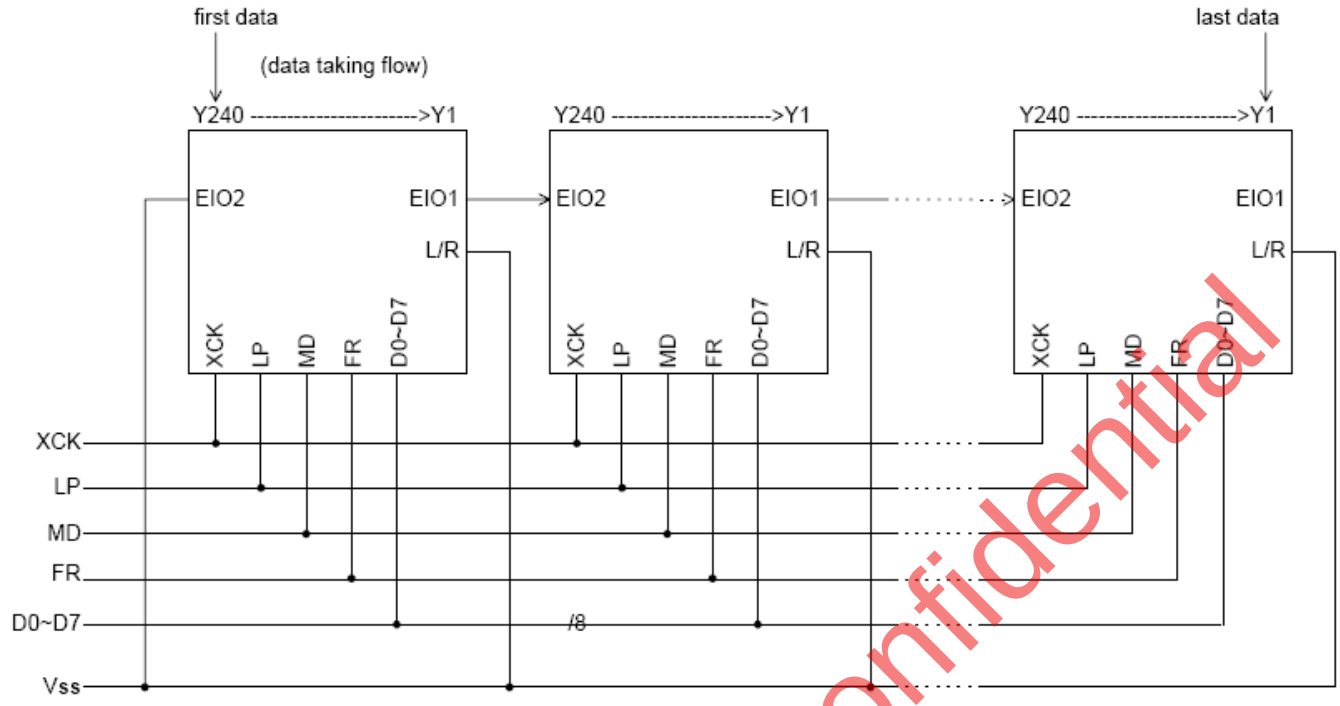
2.2. COM Mode

MD	L/R	Data Transfer Direction	EIO1	EIO2	D7
L (Single)	L (shift to left)	Y240 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y240	Input	Output	X
H (Dual)	L (shift to left)	Y240 to Y121, Y120 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y120, Y121 to Y240	Input	Output	Input

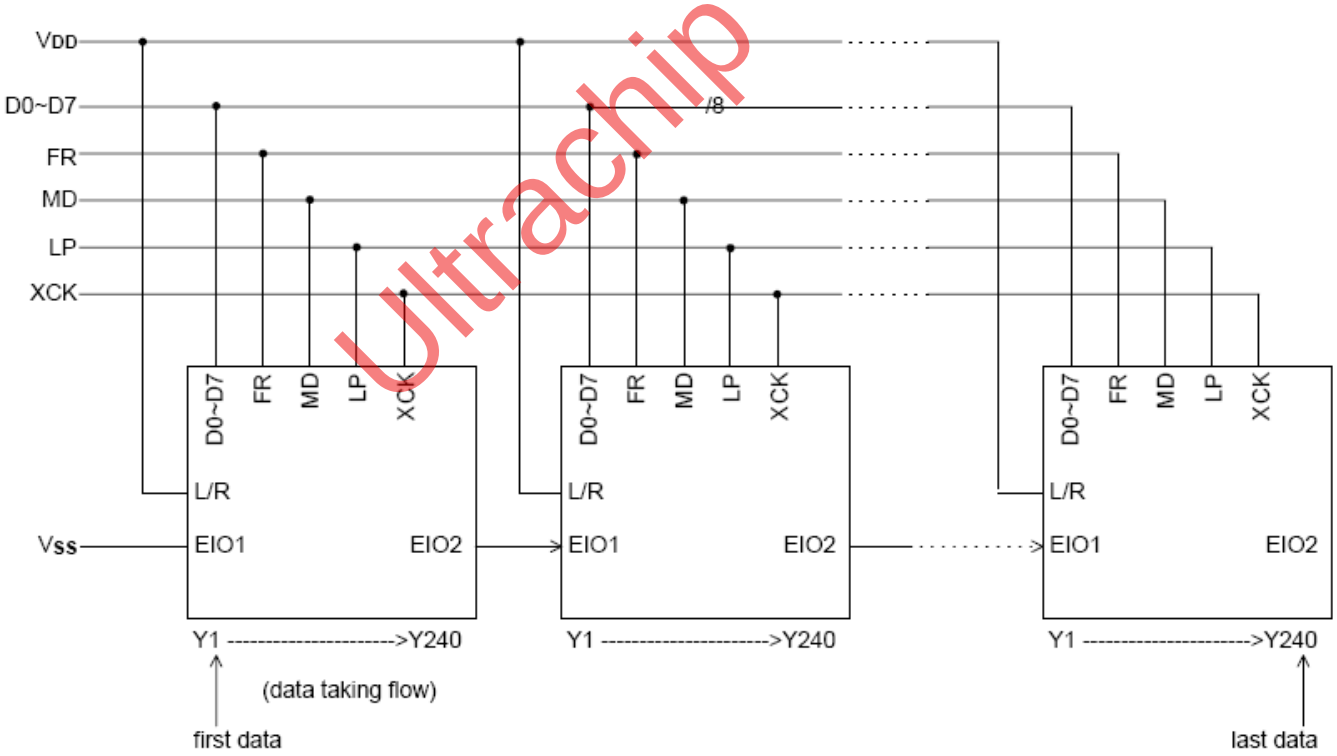
Remark:
L: Vss (0V),
H: VDD (+2.5V to +5.5V),
X: Don't care. Should be fixed to "H" or "L", avoiding floating.

3. Connection Examples of SEG Drivers

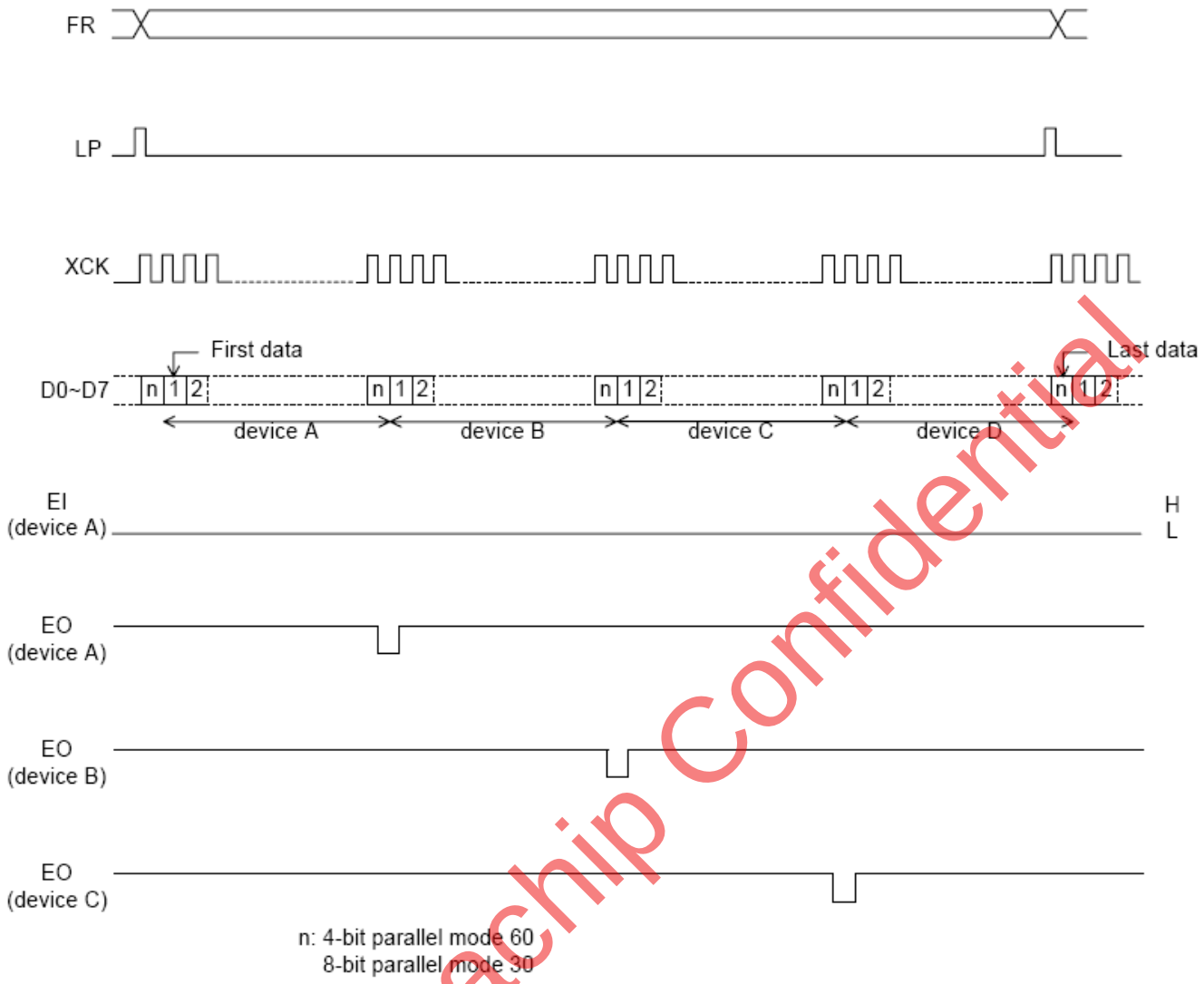
3.1. Case of L/R = "L"



3.2. Case of L/R = "H"

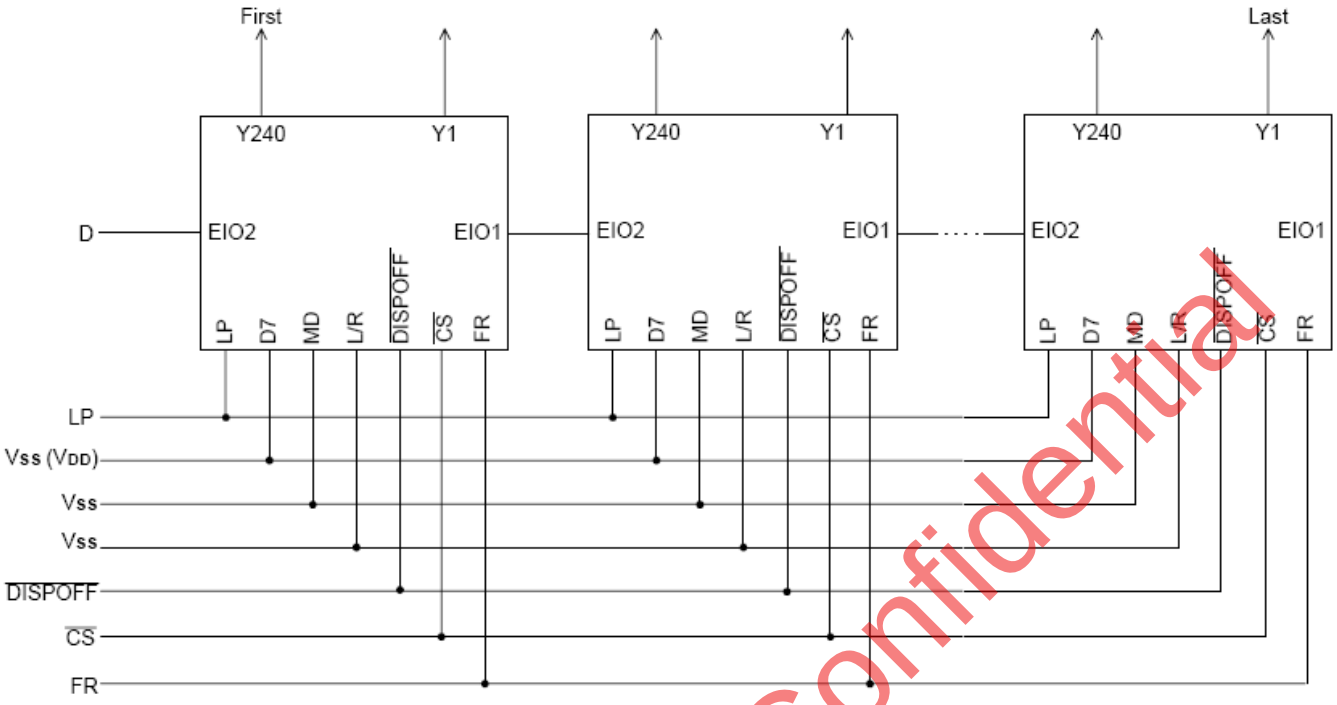


4. Timing Waveform of 4-Device Cascade Connection of SEG Drivers

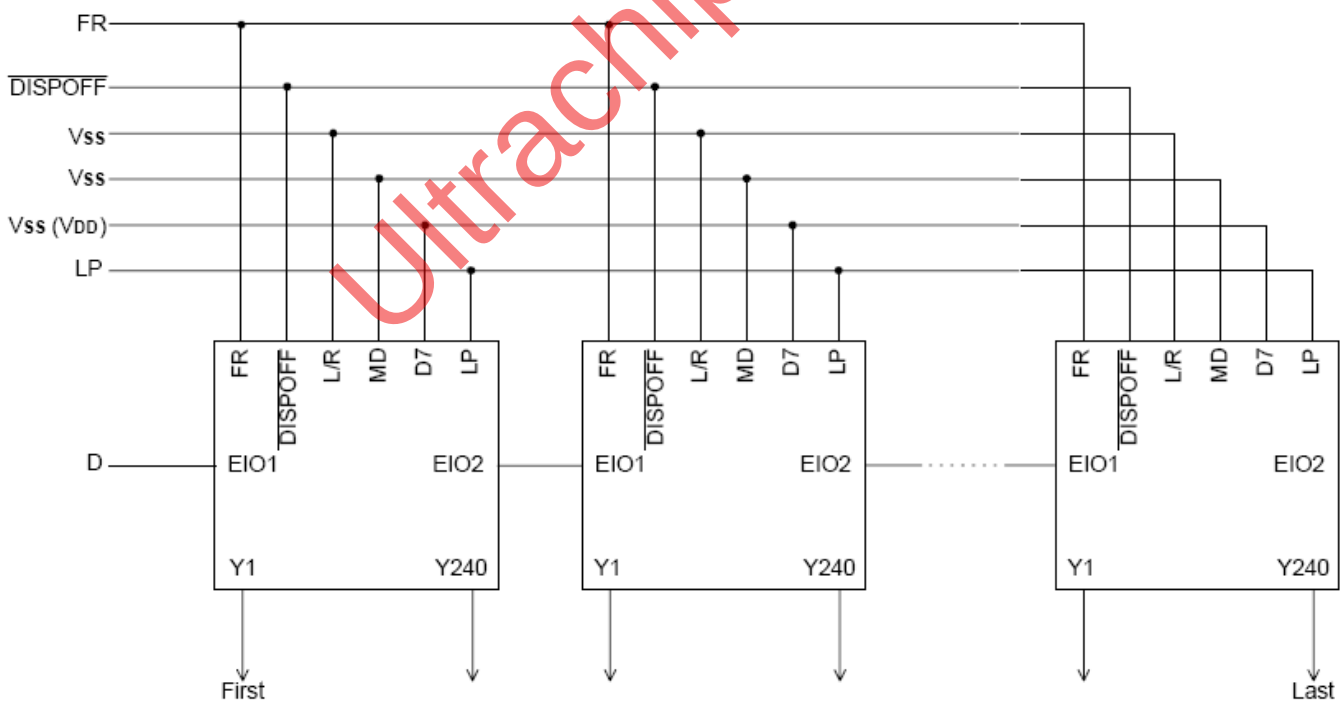


5. Connection Examples for COM Drivers

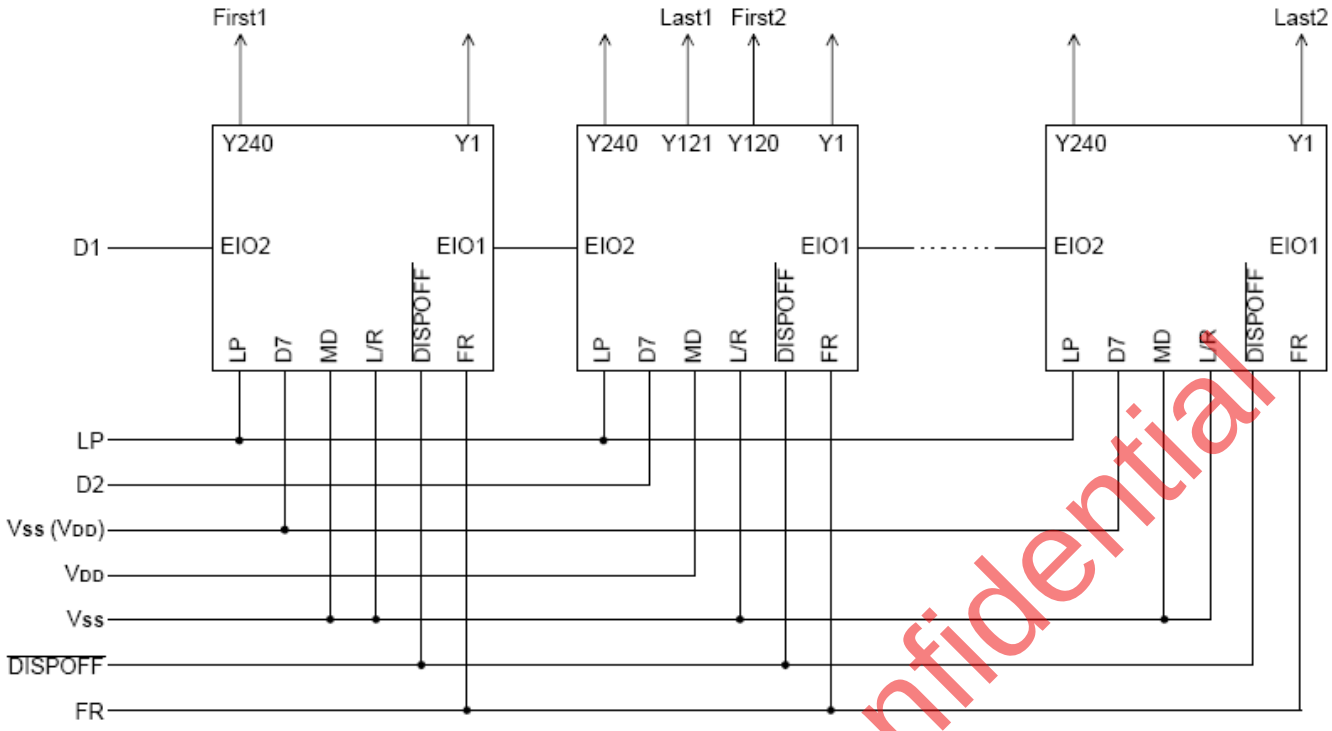
5.1. Single Mode (MD="L") **with L/R = "L"** (Data shifted Y240 → Y1, EIO2: input, EIO1: output)



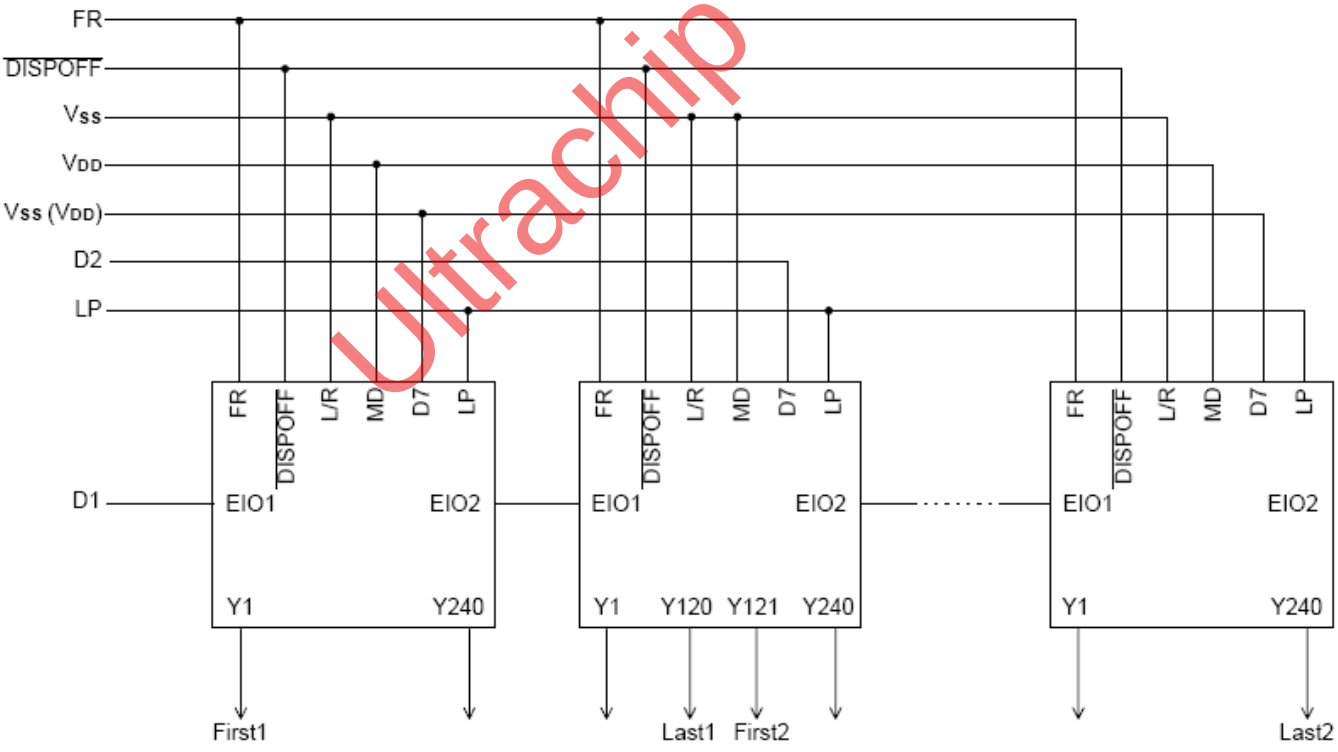
5.2. Single Mode (MD="L") **with L/R = "H"** (Data shifted Y1 → Y240, EIO2: output, EIO1: input)



5.3. Dual Mode (MD="H") **with L/R = "L"** (Data shifted Y240 → Y1, EIO2: input, EIO1: output)



5.4. Dual Mode (MD="H") **with L/R = "H"** (Data shifted Y1 → Y240, EIO2: output, EIO1: input)



6. Precaution

Be careful when connecting or disconnecting the power. This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

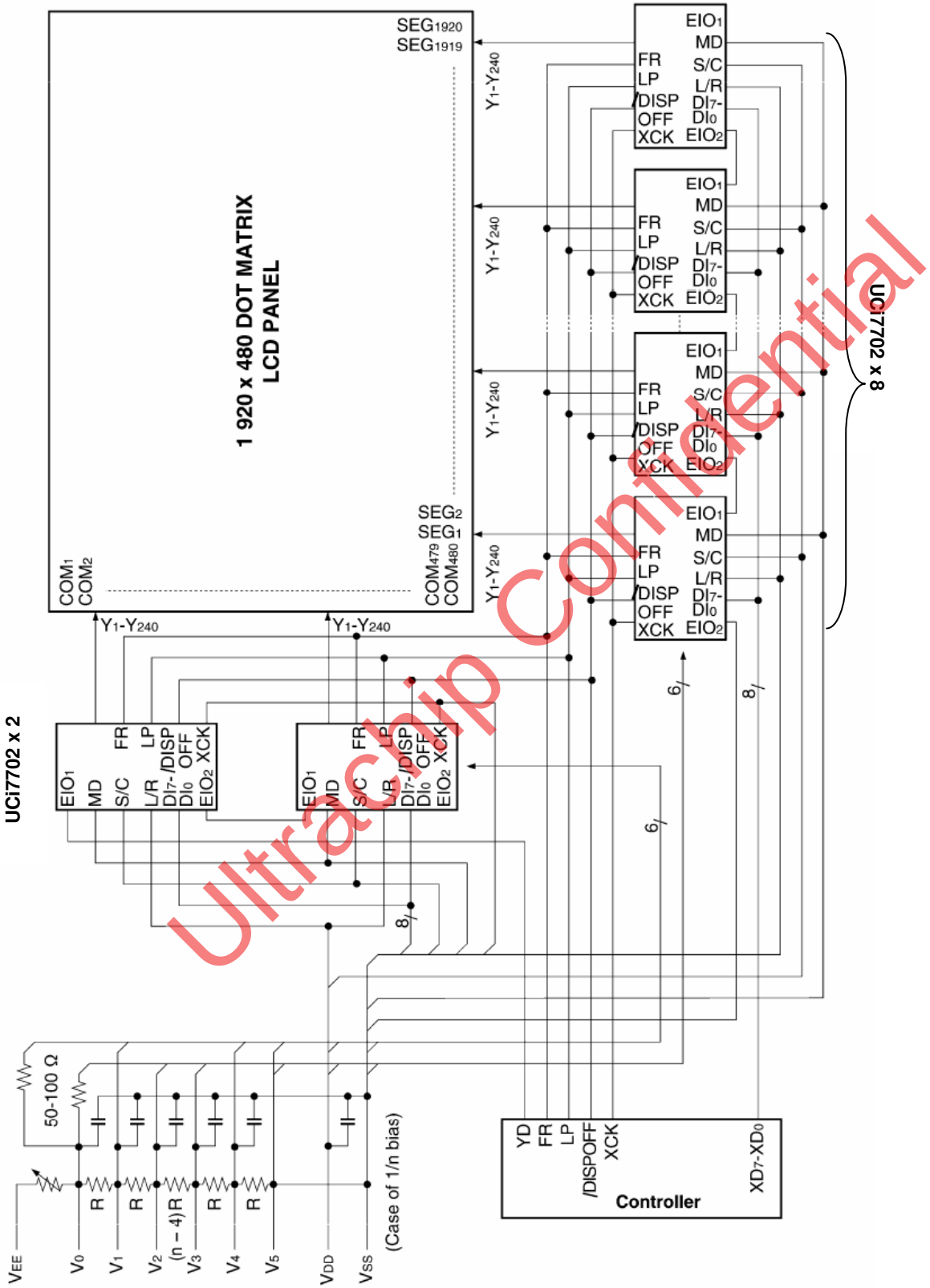
The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100Ω) or fuse to the LCD driver power V0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ cancels the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level VSS on the DISPOFF function. After that, disconnect the logic system power after disconnecting the LCD driver power.

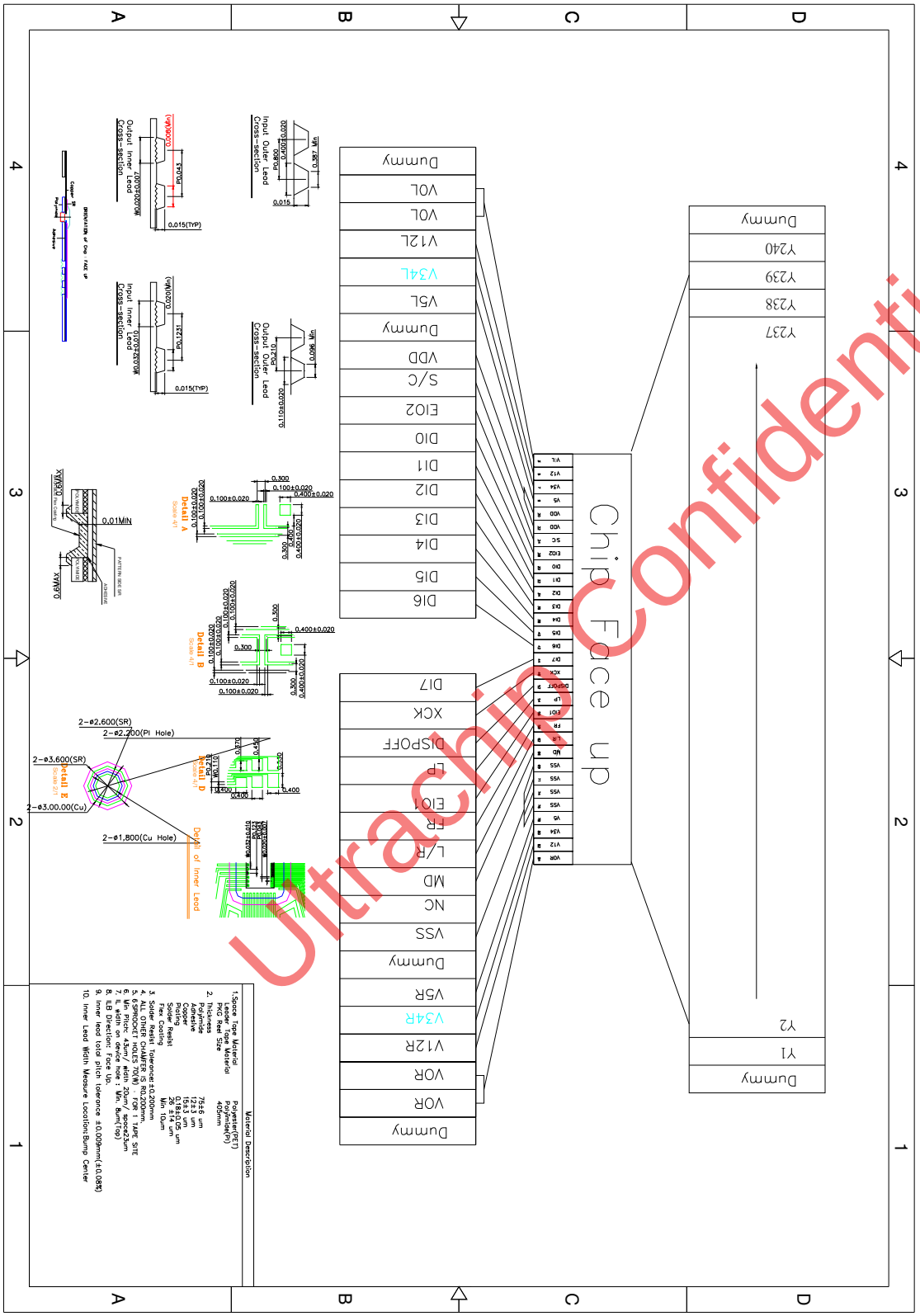
When connecting the power supply, follow the recommended sequence shown.

REFERENCE APPLICATION CIRCUIT



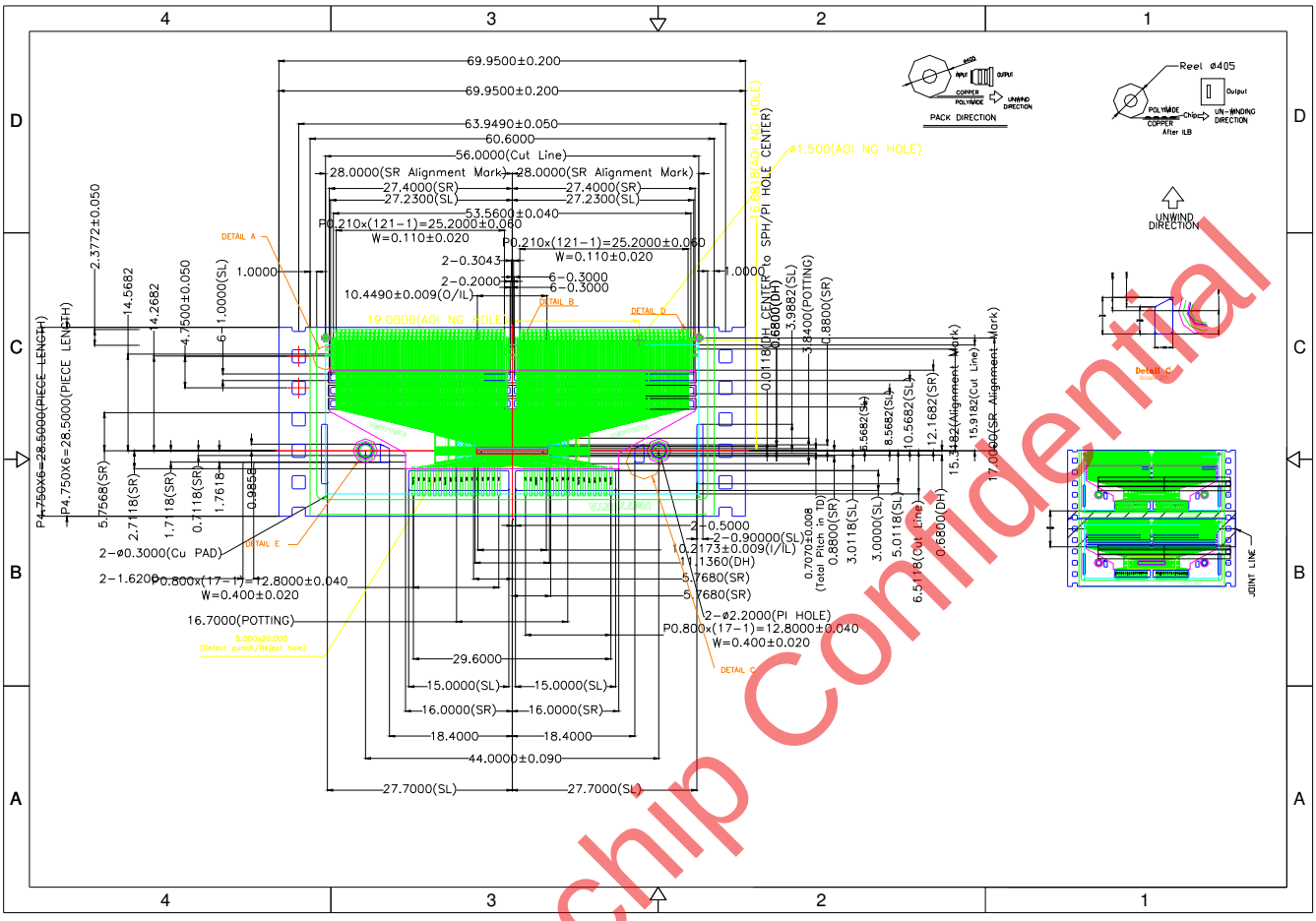
TCP PIN LAYOUT

(For part number: UCi7702cTAA)

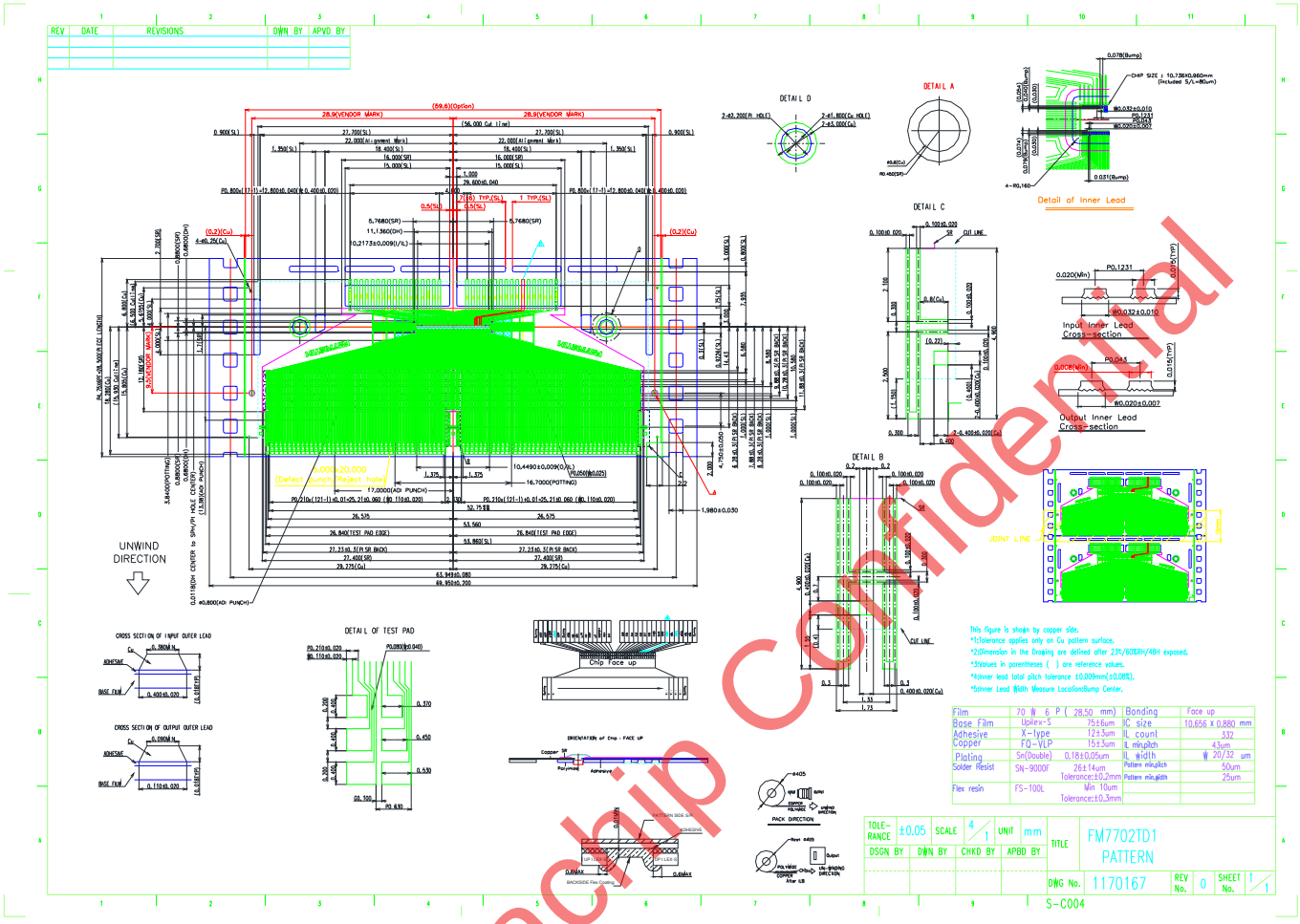


EXTERNAL VIEW OF TCP PINS

(For part number: UCi7702cTAA)



(For part number: UCi7702cTDA)



ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Signal	Item	Rating
V_{DD}	DC Supply Voltage	–0.3V ~ +7.0V
V_0	DC Supply Voltage	–0.3V ~ +45V
V_{IN}	Input Voltage	–0.3V ~ V_{DD}+0.3V
T_{OPR}	Operating Ambient temperature	–30°C ~ +85°C
T_{STG}	Storage temperature	–45°C ~ +125°C

Remark: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

SEG Mode (VSS = V5 = 0V, V_{DD} = 2.5 - 5.5V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.5	-	5.5	V	
Operating Voltage	V0	15	-	42	V	
Input high voltage	VIH	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins
Input low voltage	VIL	-	-	0.2 V_{DD}	V	
Output high voltage	VOH	V_{DD} - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA
Output low voltage	VOL	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA
Input leakage current 1	IIH	-	-	+1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, VI = V_{DD}
Input leakage current 2	IIL	-	-	-1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, VI = VSS
Output resistance	RON	-	1.5	2.0	kΩ	V0 = +42V; Y1 - Y240 pins, | ΔVON| = 0.5V
		-	2.0	2.5		V0 = +20.0V; Y1 - Y240 pins, | ΔVON| = 0.5V
Stand-by current	ISB	-	-	10	μA	Vss pin, See Note 1
Consumed current (1) (Deselection)	IDD1	-	-	2.0	mA	V_{DD} pin, See Note 2
Consumed current (2) (Selection)	IDD2	-	-	12	mA	V_{DD} pin, See Note 3
Consumed current	I0	-	-	1.5	mA	V0 pin, See Note 4

Note:
1. V_{DD} = +5.0V, V0 = +42V, VI = VSS
2. V_{DD} = +5.0V, V0 = +42V, fXCK = 20MHz, No-load, EI = V_{DD}
   The input data is turned over by the data taking clock (4-bit parallel input mode)
3. V_{DD} = +5.0V, V0 = +42V, fXCK = 20MHz, No-load. EI = VSS
   The input data is turned over by the data taking clock (4-bit parallel input mode)
4. V_{DD} = +5.0V, V0 = +42V, fXCK = 20MHz, fLP = 41.6kHz, fFR = 80 Hz, No-load
   The input data is turned over by the data taking clock (4-bit parallel-input mode)

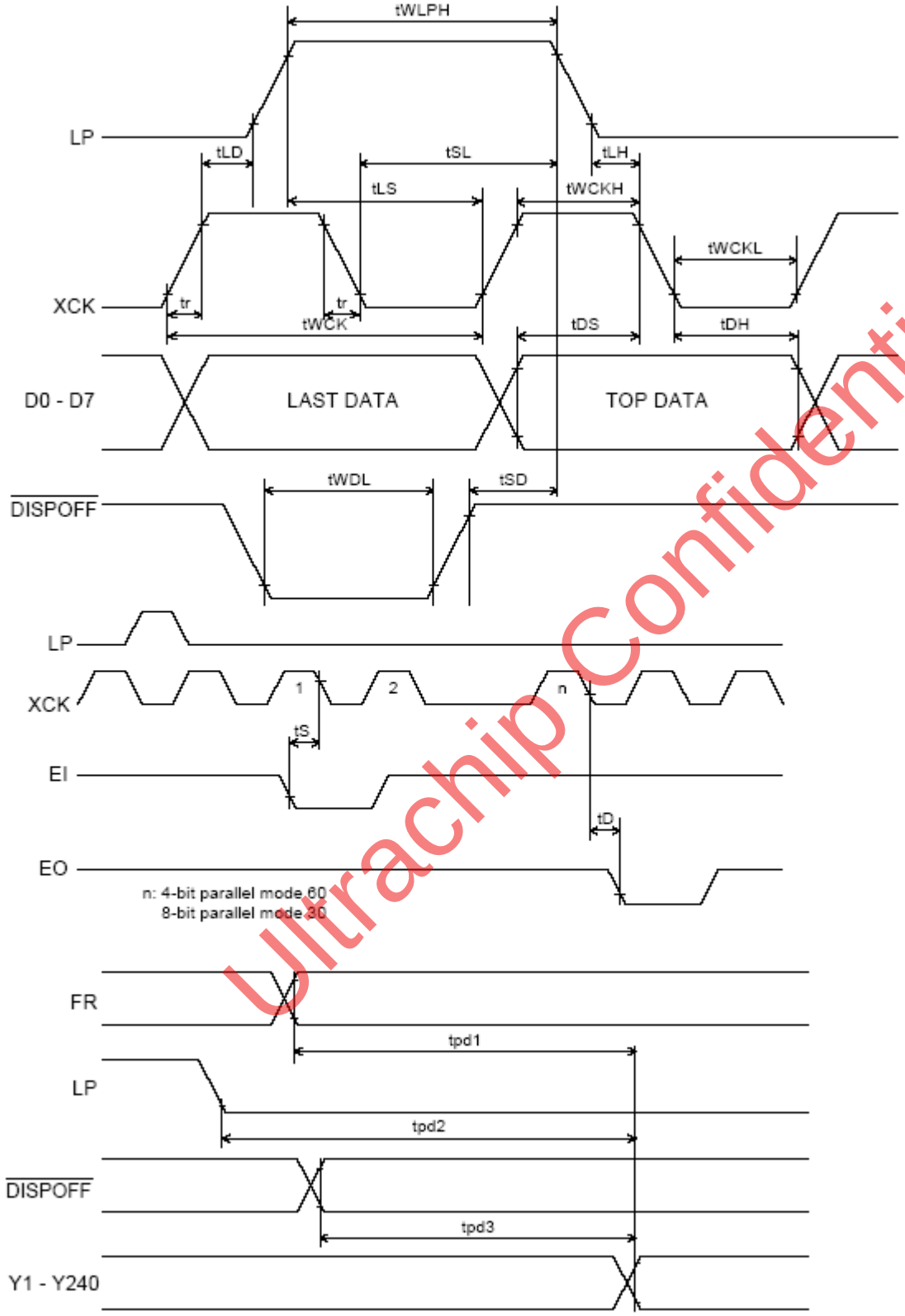
COM Mode (Vss = V5 = 0V, V_{DD} = 2.5 - 5.5V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.5	-	5.5	V	
Operating Voltage	V0	15	-	42	V	
Input high voltage	VIH	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins
Input low voltage	VIL	-	-	0.2 V_{DD}	V	
Output high voltage	VOH	V_{DD} - 0.4	-	-	V	EIO1, EIO2 pins, IOH = -0.4mA
Output low voltage	VOL	-	-	+0.4	V	EIO1, EIO2 pins, IOL = +0.4mA
Input leakage current 1	IIH	-	-	+10.0	μA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, VI = V_{DD}
Input leakage current 2	IIL	-	-	-10.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, VI = VSS
Output resistance	RON	-	15	2.0	kΩ	V0 = +42V; Y1 ~ Y240 pins, | ΔVON| = 0.5V
		-	2.0	2.5		V0 = +20.0V; Y1 ~ Y240 pins, | ΔVON| = 0.5V
Stand-by current	ISB	-	-	75	μA	VSS pin, Note 1
Consumed current (1)	IDD	-	-	120	μA	V_{DD} pin, Note 2
Consumed current (2)	I0	-	-	240	μA	V0 pin, Note 2

Note:
1. V_{DD} = +5.0V, V0 = +42V, fLP = 0 - 41.6kHz
2. V_{DD} = +5.0V, V0 = +42V, fLP = 41.6KHz, fFR = 80Hz, case of 1/480 duty operation, No-load

AC CHARACTERISTICS

Timing Characteristics of SEG Mode



SEG Mode 1

(VSS = V5 = 0V, V_{DD} = 4.5 - 5.5V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWCK	50	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	tWCKH	15	-		ns	
Shift clock "L" pulse width	tWCKL	15	-		ns	
Data setup time	tDS	10	-		ns	
Data hold time	tDH	12	-		ns	
Latch pulse "H" pulse width	tWLPH	15	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	30	-		ns	
Latch pulse rise to Shift clock rise time	tLS	25	-		ns	
Latch pulse fall to Shift clock rise time	tLH	25	-		ns	
Input signal rise time	tr		-	50	ns	Note 2
Input signal fall time	tf		-	50	ns	Note 2
Enable setup time	tS	10	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-		µs	
Output delay time (1)	tD		-	30	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2		-	1.2	µs	CL = 15pF
Output delay time (3)	tpd3		-	1.2	µs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (Tck - tWCKII - twckl)/2 is the maximum in the case of high speed operation.

SEG Mode 2

(VSS = V5 = 0V, V_{DD} = 3.0 - 4.5V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWCK	66	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	tWCKH	23	-		ns	
Shift clock "L" pulse width	tWCKL	23	-		ns	
Data setup time	tDS	15	-		ns	
Data hole time	tDH	23	-		ns	
Latch pulse "H" pulse width	tWLPH	30	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	50	-		ns	
Latch pulse rise to Shift clock rise time	tLS	30	-		ns	
Latch pulse fall to Shift clock fall time	tLH	30	-		ns	
Input signal rise time	tr		-	50	ns	Note 2
Input signal fall time	tf		-	50	ns	Note 2
Enable setup time	tS	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-		µs	
Output delay time (1)	tD		-	41	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2		-	1.2	µs	CL = 15pF
Output delay time (3)	tpd3		-	1.2	µs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (tCK - tWCKII - tWCKL)/2 is the maximum in the case of high speed operation.

SEG Mode 3

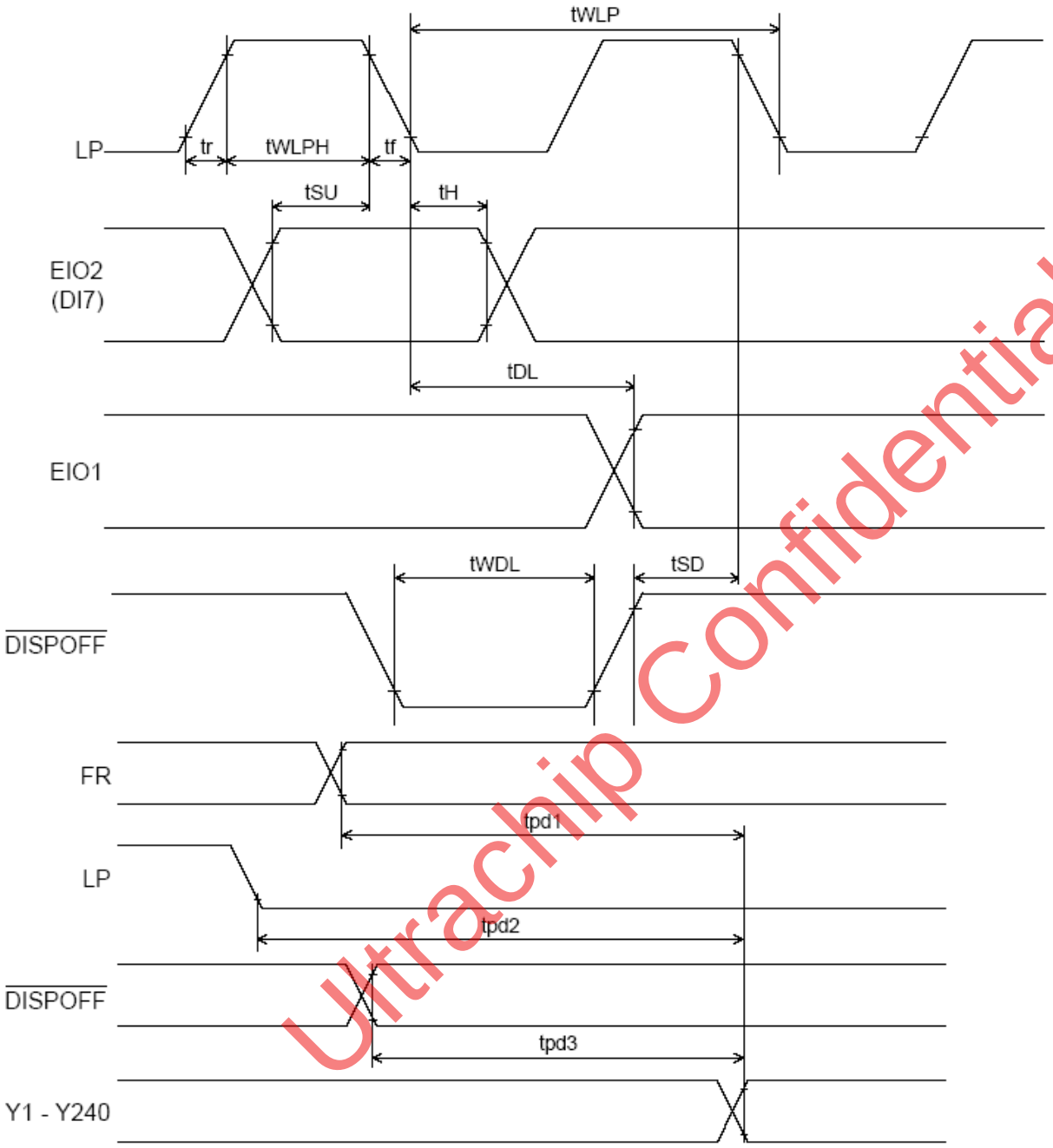
(VSS = V5 = 0V, V_{DD} = 2.5 - 3.0V, V0 = 15 to 42V, and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWCK	82	-		ns	tr, tf ≦ 10ns, Note 1
Shift clock "H" pulse width	tWCKH	28	-		ns	
Shift clock "L" pulse width	tWCKL	28	-		ns	
Data setup time	tDS	20	-		ns	
Data hole time	tDH	23	-		ns	
Latch pulse "H" pulse width	tWLPH	30	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	65	-		ns	
Latch pulse rise to Shift clock rise time	tLS	30	-		ns	
Latch pulse fall to Shift clock fall time	tLH	30	-		ns	
Input signal rise time	tr		-	50	ns	Note 2
Input signal fall time	tf		-	50	ns	Note 2
Enable setup time	tS	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-		μs	
Output delay time (1)	tD		-	57	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2		-	1.2	μs	CL = 15pF
Output delay time (3)	tpd3		-	1.2	μs	CL = 15pF

Note:

1. Take the cascade connection into consideration.
2. (tCK - tWCKII - tWCKL)/2 is the maximum in the case of high speed operation.

Timing Characteristics of COM Mode



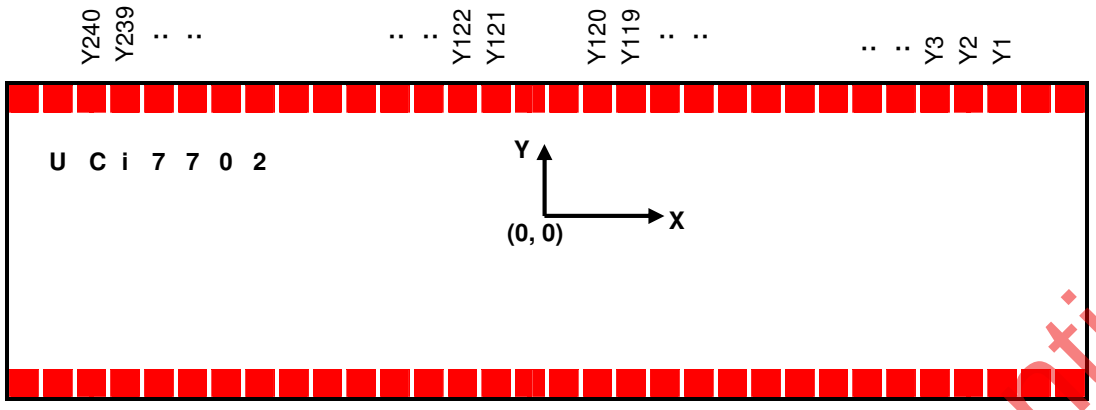
COM Mode

(VSS = V5 = 0V, V_{DD} = 2.5 - 5.5V, V0 = 15 to 42V and TA = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWLP	250	-	-	ns	tr, tf ≦ 20ns
Shift clock "H" pulse width	tWLPH	15	-	-	ns	V_{DD} = +5.0V ± 10%
		30	-	-	ns	V_{DD} = +2.5 - +4.5V
Data setup time	tSU	30	-	-	ns	
Data hole time	tH	50	-	-	ns	
Input signal rise time	tr		-	50	ns	
Input signal fall time	tf		-	50	ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-	-	ns	
$\overline{\text{DISPOFF}}$ enable pulse width	tWDL	1.2	-	-	µs	
Output delay time (1)	tDL	-	-	200	ns	CL = 15pF
Output delay time (2)	tpd1, tpd2	-	-	1.2	µs	CL = 15pF
Output delay time (3)	tpd3	-	-	1.2	µs	CL = 15pF

PHYSICAL DIMENSIONS

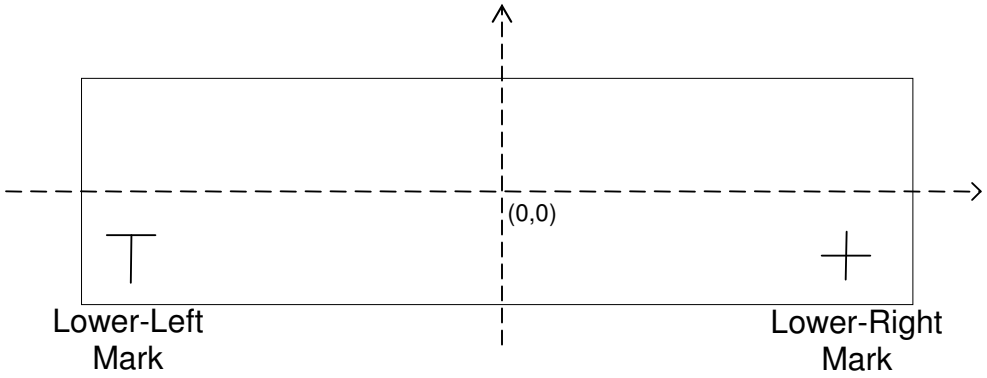
Circuit / Bump View:



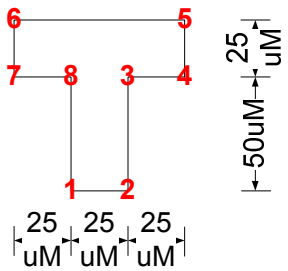
Die / Bump Information:

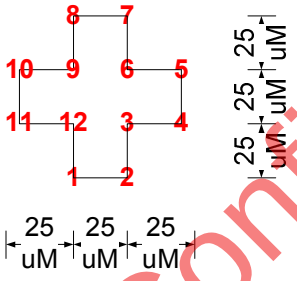
Die Size:	(10696 µM ± 40 µM) x (920 µM ± 40 µM)	**Bump Pitch:**	43 µM
Die Thickness:	508 µM ± 20 µM	**Bump Gap:**	12 µM
	(D_{MAX} – D_{MIN}) within die ⩽ 2 µM	**Bump Area:**	2449 μM^2
Bump Height:	15 µM ± 3 µM	**Coordinate origin:**	Chip center
	(H_{MAX} – H_{MIN}) within die ⩽ 2 µM	**Pad reference:**	Pad center
Bump Size:	31 µM x 79 µM (Typical)		

ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:





COORDINATES:

	Lower-Left Mark (T)		Lower-Right Mark (+)	
	X	Y	X	Y
1	-4628.8	-318.6	4601.2	-318.6
2	-4603.8	-318.6	4626.2	-318.6
3	-4603.8	-268.6	4626.2	-293.6
4	-4578.8	-268.6	4651.2	-293.6
5	-4578.8	-243.6	4651.2	-268.6
6	-4653.8	-243.6	4626.2	-268.6
7	-4653.8	-268.6	4626.2	-243.6
8	-4628.8	-268.6	4601.2	-243.6
9	--	--	4601.2	-268.6
10	--	--	4576.2	-268.6
11	--	--	4576.2	-293.6
12	--	--	4601.2	-293.6

PAD COORDINATES

No	Name	X	Y	W	H
1	DUMMY	-5231.8	-378	77.6	40
2	DUMMY	-5108.7	-378	77.6	40
3	V0	-4985.6	-378	77.6	40
4	DUMMY	-4862.5	-378	77.6	40
5	V12	-4739.4	-378	77.6	40
6	DUMMY	-4616.3	-378	77.6	40
7	V34	-4493.2	-378	77.6	40
8	DUMMY	-4370.1	-378	77.6	40
9	V5	-4247	-378	77.6	40
10	DUMMY	-4123.9	-378	77.6	40
11	VSS	-4000.8	-378	77.6	40
12	DUMMY	-3877.7	-378	77.6	40
13	VSS	-3754.6	-378	77.6	40
14	DUMMY	-3631.5	-378	77.6	40
15	DUMMY	-3508.4	-378	77.6	40
16	VSS	-3385.3	-378	77.6	40
17	DUMMY	-3262.2	-378	77.6	40
18	VSS	-3139.1	-378	77.6	40
19	DUMMY	-3016	-378	77.6	40
20	VDD	-2892.9	-378	77.6	40
21	DUMMY	-2769.8	-378	77.6	40
22	VDD	-2646.7	-378	77.6	40
23	DUMMY	-2523.6	-378	77.6	40
24	S/C	-2400.5	-378	77.6	40
25	DUMMY	-2277.4	-378	77.6	40
26	VSS	-2154.3	-378	77.6	40
27	DUMMY	-2031.2	-378	77.6	40
28	EIO2	-1908.1	-378	77.6	40
29	DUMMY	-1785	-378	77.6	40
30	DI0	-1661.9	-378	77.6	40
31	DUMMY	-1538.8	-378	77.6	40
32	DI1	-1415.7	-378	77.6	40
33	DUMMY	-1292.6	-378	77.6	40
34	DI2	-1169.5	-378	77.6	40
35	DUMMY	-1046.4	-378	77.6	40
36	DI3	-923.3	-378	77.6	40
37	DUMMY	-800.2	-378	77.6	40
38	DI4	-677.1	-378	77.6	40
39	DUMMY	-554	-378	77.6	40
40	DI5	-430.9	-378	77.6	40
41	DUMMY	-307.8	-378	77.6	40
42	DI6	-184.7	-378	77.6	40
43	DUMMY	-61.6	-378	77.6	40
44	DI7	61.5	-378	77.6	40
45	DUMMY	184.6	-378	77.6	40
46	VSS	307.7	-378	77.6	40
47	DUMMY	430.8	-378	77.6	40
48	XCK	553.9	-378	77.6	40
49	DUMMY	677	-378	77.6	40
50	VSS	800.1	-378	77.6	40
51	DUMMY	923.2	-378	77.6	40
52	/DISPOFF	1046.3	-378	77.6	40
53	DUMMY	1169.4	-378	77.6	40
54	LP	1292.5	-378	77.6	40
55	DUMMY	1415.6	-378	77.6	40
56	EIO1	1538.7	-378	77.6	40
57	DUMMY	1661.8	-378	77.6	40
58	FR	1784.9	-378	77.6	40

No	Name	X	Y	W	H
59	DUMMY	1908	-378	77.6	40
60	VSS	2031.1	-378	77.6	40
61	DUMMY	2154.2	-378	77.6	40
62	L/R	2277.3	-378	77.6	40
63	DUMMY	2400.4	-378	77.6	40
64	VDD	2523.5	-378	77.6	40
65	DUMMY	2646.6	-378	77.6	40
66	MD	2769.7	-378	77.6	40
67	DUMMY	2892.8	-378	77.6	40
68	DUMMY	3015.9	-378	77.6	40
69	VSS	3139	-378	77.6	40
70	DUMMY	3262.1	-378	77.6	40
71	VSS	3385.2	-378	77.6	40
72	DUMMY	3508.3	-378	77.6	40
73	DUMMY	3631.4	-378	77.6	40
74	VSS	3754.5	-378	77.6	40
75	DUMMY	3877.6	-378	77.6	40
76	VSS	4000.7	-378	77.6	40
77	DUMMY	4123.8	-378	77.6	40
78	V5	4246.9	-378	77.6	40
79	DUMMY	4370	-378	77.6	40
80	V34	4493.1	-378	77.6	40
81	DUMMY	4616.2	-378	77.6	40
82	V12	4739.3	-378	77.6	40
83	DUMMY	4862.4	-378	77.6	40
84	V0	4985.5	-378	77.6	40
85	DUMMY	5108.6	-378	77.6	40
86	DUMMY	5231.7	-378	77.6	40
87	DUMMY	5267.5	386.5	31	79
88	DUMMY	5224.5	386.5	31	79
89	Y1	5181.5	386.5	31	79
90	Y2	5138.5	386.5	31	79
91	Y3	5095.5	386.5	31	79
92	Y4	5052.5	386.5	31	79
93	Y5	5009.5	386.5	31	79
94	Y6	4966.5	386.5	31	79
95	Y7	4923.5	386.5	31	79
96	Y8	4880.5	386.5	31	79
97	Y9	4837.5	386.5	31	79
98	Y10	4794.5	386.5	31	79
99	Y11	4751.5	386.5	31	79
100	Y12	4708.5	386.5	31	79
101	Y13	4665.5	386.5	31	79
102	Y14	4622.5	386.5	31	79
103	Y15	4579.5	386.5	31	79
104	Y16	4536.5	386.5	31	79
105	Y17	4493.5	386.5	31	79
106	Y18	4450.5	386.5	31	79
107	Y19	4407.5	386.5	31	79
108	Y20	4364.5	386.5	31	79
109	Y21	4321.5	386.5	31	79
110	Y22	4278.5	386.5	31	79
111	Y23	4235.5	386.5	31	79
112	Y24	4192.5	386.5	31	79
113	Y25	4149.5	386.5	31	79
114	Y26	4106.5	386.5	31	79
115	Y27	4063.5	386.5	31	79
116	Y28	4020.5	386.5	31	79

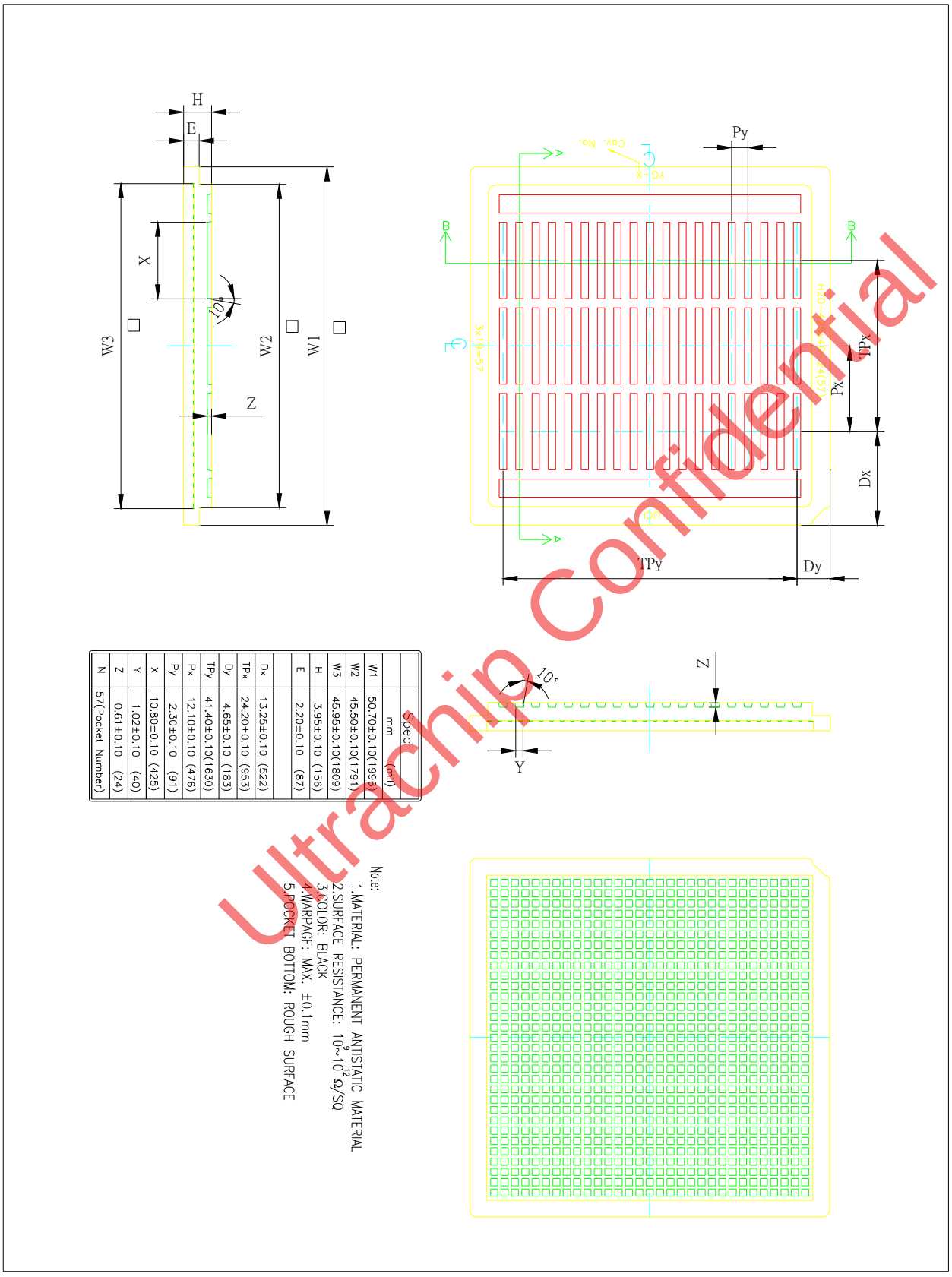
No	Name	X	Y	W	H
117	Y29	3977.5	386.5	31	79
118	Y30	3934.5	386.5	31	79
119	Y31	3891.5	386.5	31	79
120	Y32	3848.5	386.5	31	79
121	Y33	3805.5	386.5	31	79
122	Y34	3762.5	386.5	31	79
123	Y35	3719.5	386.5	31	79
124	Y36	3676.5	386.5	31	79
125	Y37	3633.5	386.5	31	79
126	Y38	3590.5	386.5	31	79
127	Y39	3547.5	386.5	31	79
128	Y40	3504.5	386.5	31	79
129	Y41	3461.5	386.5	31	79
130	Y42	3418.5	386.5	31	79
131	Y43	3375.5	386.5	31	79
132	Y44	3332.5	386.5	31	79
133	Y45	3289.5	386.5	31	79
134	Y46	3246.5	386.5	31	79
135	Y47	3203.5	386.5	31	79
136	Y48	3160.5	386.5	31	79
137	Y49	3117.5	386.5	31	79
138	Y50	3074.5	386.5	31	79
139	Y51	3031.5	386.5	31	79
140	Y52	2988.5	386.5	31	79
141	Y53	2945.5	386.5	31	79
142	Y54	2902.5	386.5	31	79
143	Y55	2859.5	386.5	31	79
144	Y56	2816.5	386.5	31	79
145	Y57	2773.5	386.5	31	79
146	Y58	2730.5	386.5	31	79
147	Y59	2687.5	386.5	31	79
148	Y60	2644.5	386.5	31	79
149	Y61	2601.5	386.5	31	79
150	Y62	2558.5	386.5	31	79
151	Y63	2515.5	386.5	31	79
152	Y64	2472.5	386.5	31	79
153	Y65	2429.5	386.5	31	79
154	Y66	2386.5	386.5	31	79
155	Y67	2343.5	386.5	31	79
156	Y68	2300.5	386.5	31	79
157	Y69	2257.5	386.5	31	79
158	Y70	2214.5	386.5	31	79
159	Y71	2171.5	386.5	31	79
160	Y72	2128.5	386.5	31	79
161	Y73	2085.5	386.5	31	79
162	Y74	2042.5	386.5	31	79
163	Y75	1999.5	386.5	31	79
164	Y76	1956.5	386.5	31	79
165	Y77	1913.5	386.5	31	79
166	Y78	1870.5	386.5	31	79
167	Y79	1827.5	386.5	31	79
168	Y80	1784.5	386.5	31	79
169	Y81	1741.5	386.5	31	79
170	Y82	1698.5	386.5	31	79
171	Y83	1655.5	386.5	31	79
172	Y84	1612.5	386.5	31	79
173	Y85	1569.5	386.5	31	79
174	Y86	1526.5	386.5	31	79
175	Y87	1483.5	386.5	31	79
176	Y88	1440.5	386.5	31	79

No	Name	X	Y	W	H
177	Y89	1397.5	386.5	31	79
178	Y90	1354.5	386.5	31	79
179	Y91	1311.5	386.5	31	79
180	Y92	1268.5	386.5	31	79
181	Y93	1225.5	386.5	31	79
182	Y94	1182.5	386.5	31	79
183	Y95	1139.5	386.5	31	79
184	Y96	1096.5	386.5	31	79
185	Y97	1053.5	386.5	31	79
186	Y98	1010.5	386.5	31	79
187	Y99	967.5	386.5	31	79
188	Y100	924.5	386.5	31	79
189	Y101	881.5	386.5	31	79
190	Y102	838.5	386.5	31	79
191	Y103	795.5	386.5	31	79
192	Y104	752.5	386.5	31	79
193	Y105	709.5	386.5	31	79
194	Y106	666.5	386.5	31	79
195	Y107	623.5	386.5	31	79
196	Y108	580.5	386.5	31	79
197	Y109	537.5	386.5	31	79
198	Y110	494.5	386.5	31	79
199	Y111	451.5	386.5	31	79
200	Y112	408.5	386.5	31	79
201	Y113	365.5	386.5	31	79
202	Y114	322.5	386.5	31	79
203	Y115	279.5	386.5	31	79
204	Y116	236.5	386.5	31	79
205	Y117	193.5	386.5	31	79
206	Y118	150.5	386.5	31	79
207	Y119	107.5	386.5	31	79
208	Y120	64.5	386.5	31	79
209	DUMMY	21.5	386.5	31	79
210	DUMMY	-21.5	386.5	31	79
211	Y121	-64.5	386.5	31	79
212	Y122	-107.5	386.5	31	79
213	Y123	-150.5	386.5	31	79
214	Y124	-193.5	386.5	31	79
215	Y125	-236.5	386.5	31	79
216	Y126	-279.5	386.5	31	79
217	Y127	-322.5	386.5	31	79
218	Y128	-365.5	386.5	31	79
219	Y129	-408.5	386.5	31	79
220	Y130	-451.5	386.5	31	79
221	Y131	-494.5	386.5	31	79
222	Y132	-537.5	386.5	31	79
223	Y133	-580.5	386.5	31	79
224	Y134	-623.5	386.5	31	79
225	Y135	-666.5	386.5	31	79
226	Y136	-709.5	386.5	31	79
227	Y137	-752.5	386.5	31	79
228	Y138	-795.5	386.5	31	79
229	Y139	-838.5	386.5	31	79
230	Y140	-881.5	386.5	31	79
231	Y141	-924.5	386.5	31	79
232	Y142	-967.5	386.5	31	79
233	Y143	-1010.5	386.5	31	79
234	Y144	-1053.5	386.5	31	79
235	Y145	-1096.5	386.5	31	79
236	Y146	-1139.5	386.5	31	79

No	Name	X	Y	W	H
237	Y147	-1182.5	386.5	31	79
238	Y148	-1225.5	386.5	31	79
239	Y149	-1268.5	386.5	31	79
240	Y150	-1311.5	386.5	31	79
241	Y151	-1354.5	386.5	31	79
242	Y152	-1397.5	386.5	31	79
243	Y153	-1440.5	386.5	31	79
244	Y154	-1483.5	386.5	31	79
245	Y155	-1526.5	386.5	31	79
246	Y156	-1569.5	386.5	31	79
247	Y157	-1612.5	386.5	31	79
248	Y158	-1655.5	386.5	31	79
249	Y159	-1698.5	386.5	31	79
250	Y160	-1741.5	386.5	31	79
251	Y161	-1784.5	386.5	31	79
252	Y162	-1827.5	386.5	31	79
253	Y163	-1870.5	386.5	31	79
254	Y164	-1913.5	386.5	31	79
255	Y165	-1956.5	386.5	31	79
256	Y166	-1999.5	386.5	31	79
257	Y167	-2042.5	386.5	31	79
258	Y168	-2085.5	386.5	31	79
259	Y169	-2128.5	386.5	31	79
260	Y170	-2171.5	386.5	31	79
261	Y171	-2214.5	386.5	31	79
262	Y172	-2257.5	386.5	31	79
263	Y173	-2300.5	386.5	31	79
264	Y174	-2343.5	386.5	31	79
265	Y175	-2386.5	386.5	31	79
266	Y176	-2429.5	386.5	31	79
267	Y177	-2472.5	386.5	31	79
268	Y178	-2515.5	386.5	31	79
269	Y179	-2558.5	386.5	31	79
270	Y180	-2601.5	386.5	31	79
271	Y181	-2644.5	386.5	31	79
272	Y182	-2687.5	386.5	31	79
273	Y183	-2730.5	386.5	31	79
274	Y184	-2773.5	386.5	31	79
275	Y185	-2816.5	386.5	31	79
276	Y186	-2859.5	386.5	31	79
277	Y187	-2902.5	386.5	31	79
278	Y188	-2945.5	386.5	31	79
279	Y189	-2988.5	386.5	31	79
280	Y190	-3031.5	386.5	31	79
281	Y191	-3074.5	386.5	31	79
282	Y192	-3117.5	386.5	31	79
283	Y193	-3160.5	386.5	31	79
284	Y194	-3203.5	386.5	31	79
285	Y195	-3246.5	386.5	31	79
286	Y196	-3289.5	386.5	31	79
287	Y197	-3332.5	386.5	31	79
288	Y198	-3375.5	386.5	31	79
289	Y199	-3418.5	386.5	31	79
290	Y200	-3461.5	386.5	31	79
291	Y201	-3504.5	386.5	31	79
292	Y202	-3547.5	386.5	31	79
293	Y203	-3590.5	386.5	31	79
294	Y204	-3633.5	386.5	31	79
295	Y205	-3676.5	386.5	31	79
296	Y206	-3719.5	386.5	31	79

No	Name	X	Y	W	H
297	Y207	-3762.5	386.5	31	79
298	Y208	-3805.5	386.5	31	79
299	Y209	-3848.5	386.5	31	79
300	Y210	-3891.5	386.5	31	79
301	Y211	-3934.5	386.5	31	79
302	Y212	-3977.5	386.5	31	79
303	Y213	-4020.5	386.5	31	79
304	Y214	-4063.5	386.5	31	79
305	Y215	-4106.5	386.5	31	79
306	Y216	-4149.5	386.5	31	79
307	Y217	-4192.5	386.5	31	79
308	Y218	-4235.5	386.5	31	79
309	Y219	-4278.5	386.5	31	79
310	Y220	-4321.5	386.5	31	79
311	Y221	-4364.5	386.5	31	79
312	Y222	-4407.5	386.5	31	79
313	Y223	-4450.5	386.5	31	79
314	Y224	-4493.5	386.5	31	79
315	Y225	-4536.5	386.5	31	79
316	Y226	-4579.5	386.5	31	79
317	Y227	-4622.5	386.5	31	79
318	Y228	-4665.5	386.5	31	79
319	Y229	-4708.5	386.5	31	79
320	Y230	-4751.5	386.5	31	79
321	Y231	-4794.5	386.5	31	79
322	Y232	-4837.5	386.5	31	79
323	Y233	-4880.5	386.5	31	79
324	Y234	-4923.5	386.5	31	79
325	Y235	-4966.5	386.5	31	79
326	Y236	-5009.5	386.5	31	79
327	Y237	-5052.5	386.5	31	79
328	Y238	-5095.5	386.5	31	79
329	Y239	-5138.5	386.5	31	79
330	Y240	-5181.5	386.5	31	79
331	DUMMY	-5224.5	386.5	31	79
332	DUMMY	-5267.5	386.5	31	79

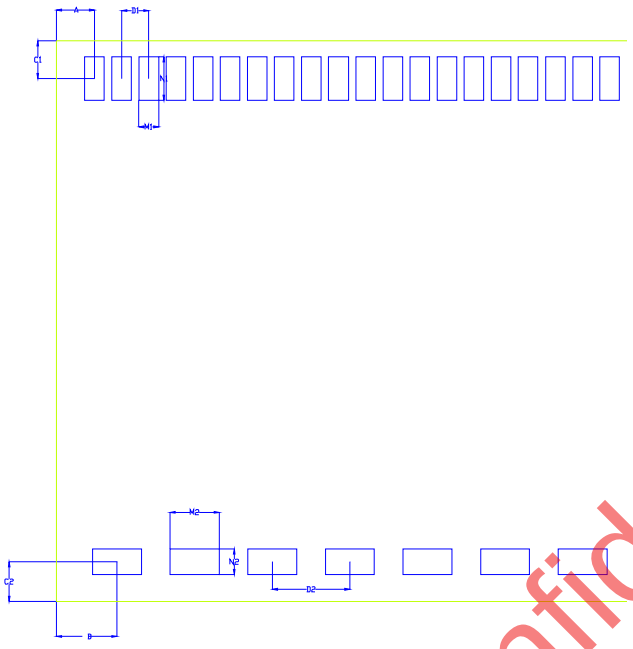
TRAY INFORMATION



	Spec	
	mm	(mil)
W1	50.70±0.10	(1996)
W2	45.50±0.10	(1791)
W3	45.95±0.10	(1809)
H	3.95±0.10	(156)
E	2.20±0.10	(87)
Dx	13.25±0.10	(522)
TPx	24.20±0.10	(953)
Dy	4.65±0.10	(183)
TPy	41.40±0.10	(1630)
Px	12.10±0.10	(476)
Py	2.30±0.10	(91)
X	10.80±0.10	(425)
Y	1.02±0.10	(40)
Z	0.61±0.10	(24)
N	57(Pocket Number)	

Note:
1.MATERIAL: PERMANENT ANTISTATIC MATERIAL
2.SURFACE RESISTANCE: 10^9~10^{12} Ω/SQ
3.COLOR: BLACK
4.WARPAGE: MAX. ±0.1mm
5.POCKET BOTTOM: ROUGH SURFACE

PACKAGE INFORMATION



Chip Outline Dimensions

Symbol	Dimensions in μm
A1	60.5
C1	59
D1	43
M1	31
N1	68

Symbol	Dimensions in μm
B	96.2
C2	62
D2	123.1
M2	77.6
N2	40

REVISION HISTORY

Revision	Content	Date
0.6	First Release	Oct. 14, 2011
1.0	Tray drawing presents.	Apr. 3, 2012
1.2	Part numbers are modified.	Oct. 14, 2015
1.3	A TCP drawing and its related part number are provided.	Mar. 23, 2015
1.4	One more part number is added.	May 4, 2017
1.41	The visual inspection documents are updated.	May 18, 2017
	The TCP drawing for part number "UCi7702cTDA" is updated.	
	The AC, DC sections are updated.	