TOMATO LSI Inc.

LCD driver IC

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VER 0.2

TL0324S

65COM / 132SEG DRIVER & CONTROLLER
FOR STN LCD

TOMATO LSI Inc.

1. INTRODUCTION

The TL0324S is a driver and controller LSI for graphic dot-matrix liquid crystal display systems.
It contains 65 common and 132 segment driver circuits.
This chip is connected directly to a microprocessor (MPU), accepts serial or 8-bit parallel display data and stores in an on-chip Display Data RAM (DDRAM) of 65 x 132 bits.
It provides a high-flexible display section due to one to one correspondences between on-chip DDRAM bits and LCD panel pixels.
And it performs DDRAM read / write operation with no externally operating clock to minimize power consumption.
In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver output circuits

-. 65 common outputs / 132 segment outputs

On-chip display data RAM (DDRAM)

-. Capacity: 65 x 132=8,580 bits
-. RAM bit data “1”: a dot of display is illuminated.
-. RAM bit data “0”: a dot of display is not illuminated.

Multi-chip operation

-. Master and slave mode available

Applicable duty-ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/9 or 1/7	65 x 132
1/55	1/8 or 1/6	55 x 132
1/49	1/8 or 1/6	49 x 132
1/33	1/6 or 1/5	33 x 132

Microprocessor (MPU) interface

-. 8-bit parallel bi-directional interface with 6800-series or 8080-series
-. Serial interface (write operation only)

Various Function set

-. Display ON/OFF, set initial display line, set page address, set column address, read status, write / read display data, select segment driver output, reverse display ON/OFF, entire display ON/OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for V0 voltage regulation, electronic volume, set static indicator state.
-. H/W and S/W reset available
-. Static drive circuit equipped internally for indicators with 4 flashing modes

Built-in analog circuits

-. On-chip Oscillator circuit for display clock (external clock can also be used)
-. High performance voltage converter
(with booster ratios of x2, x3, x4 and x5, where the step-up reference voltage can be used externally)
-. High accuracy voltage regulator (temperature coefficient: -0.05%/°C or external input)
-. Electronic contrast control function (64 steps)
-. Vref = 2.1V ± 3% (V0 voltage adjustment voltage)
-. High performance voltage follower
(V1 to V4 voltage divider resistors and OP-Amp for increasing drive capacity)

Operating voltage range

-. Supply voltage (VDD): 2.4V to 3.6V
-. LCD driving voltage (VLCD = V0 -VSS): 4.5V to 15.0V

Low power consumption

-. Operating power: 40μA (Typ)
(V_{DD} = 3V, x4 boosting [VCI is V_{DD}], V0 = 11V, internal power supply ON, display OFF and normal mode is selected)
-. Standby power: 10μA Max. (during power save [standby] mode)

Operating Temperatures

-. Wide range of operating temperatures : -40°C to 85°C

CMOS Process

Package type

-. Gold bumped chip and TCP available

3. BLOCK DIAGRAM

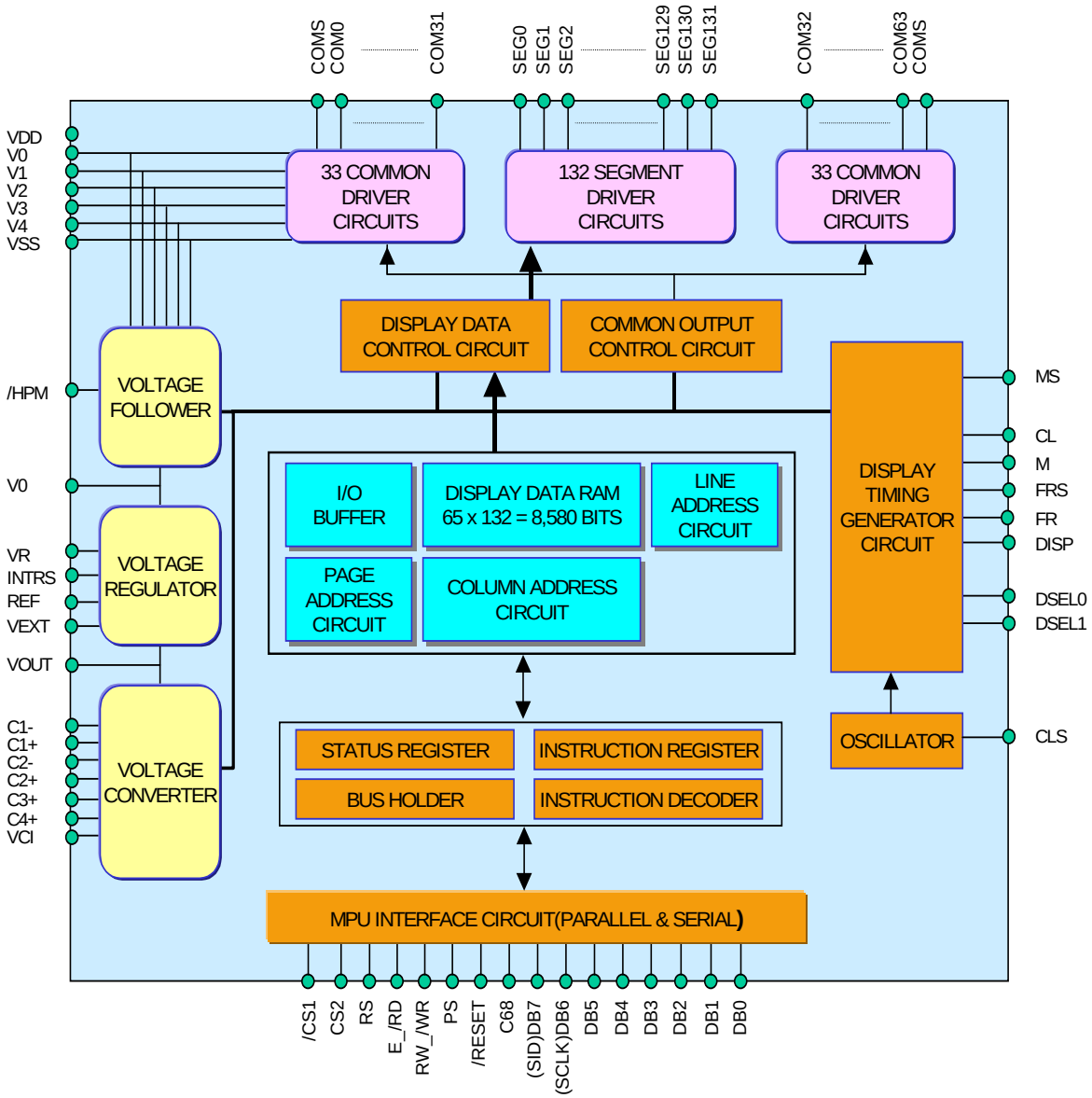

Figure 3-1. block diagram

4. PIN DESCRIPTION

Table 4-1. Pin description

<table>
<tr><td colspan="3">Power supply</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>VDD</td><td rowspan="2">Power supply</td><td>Shared with the MPU power supply terminal VCC.</td></tr>
<tr><td>VSS</td><td>This is a 0V terminal connected to the system GND.
Main VSS pad (PAD No. 43,44,45,46 and 47) have to be connected</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>The voltage is determined by the LCD pixel impedance-converted for application by an operational amplifier.
Voltage have the following relationship: V0 ≥V1≥V2≥V3≥V4≥VSS(GND)
When the on-chip power circuit is active, these voltages are generated according to the state of LCD bias, as shown in the table below.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 bias</td><td>(8/9) x V0</td><td>(7/9) x V0</td><td>(2/9) x V0</td><td>(1/9) x V0</td></tr>
<tr><td>1/8 bias</td><td>(7/8) x V0</td><td>(6/8) x V0</td><td>(2/8) x V0</td><td>(1/8) x V0</td></tr>
<tr><td>1/7 bias</td><td>(6/7) x V0</td><td>(5/7) x V0</td><td>(2/7) x V0</td><td>(1/7) x V0</td></tr>
<tr><td>1/6 bias</td><td>(5/6) x V0</td><td>(4/6) x V0</td><td>(2/6) x V0</td><td>(1/6) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD driver power supply</td></tr>
<tr><td>C1+</td><td rowspan="6">O</td><td>Capacitor1+ positive connection pin for the voltage converter</td></tr>
<tr><td>C1-</td><td>Capacitor1- negative connection pin for voltage converter</td></tr>
<tr><td>C2+</td><td>Capacitor2+ positive connect ion pin for voltage converter</td></tr>
<tr><td>C2-</td><td>Capacitor2- negative connection pin for voltage converter</td></tr>
<tr><td>C3+</td><td>Capacitor3+ positive connection pin for voltage converter</td></tr>
<tr><td>C4+</td><td>Capacitor4+ positive connection pin for voltage converter</td></tr>
<tr><td>V_{OUT}</td><td>I/O</td><td>Voltage converter input / output pin
Connect this pin to VSS through capacitor.</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin. It is valid only when using external resistors.(INTRS=”L”)</td></tr>
<tr><td>VCI</td><td>I</td><td>This is the reference voltage for the voltage converter circuit for the LCD drive.
Whether internal voltage converter use or not use, this pin should be fixed.
The voltage should have the following range: 2.4V ≤ VCI ≤ 3.6V</td></tr>
<tr><td>VEXT</td><td>I</td><td>This is the externally input reference voltage (VREF) for the internal voltage regulator.
It is valid only when external VREF is used (REF = “L”).
When using internal VREF, this pin is Open</td></tr>
<tr><td>REF</td><td>I</td><td>Select the external VREF voltage via VEXT pin
-REF = “L”: using the external VREF
-REF = “H”: using the internal VREF</td></tr>
</table>

Table 4-1. Pin description (continued)

<table>
<tr><th colspan="3">System control</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master/slave mode select input. Master makes some signals for display, and slave receives them. This for display synchronization.
MS =”H”: Master mode
MS =”L”: Slave mode
<table>
<tr><th>MS</th><th>CLS</th><th>OSC Circuit</th><th>Power Supply</th><th>CL</th><th>M</th><th>FRS, FR</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>-</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enables / disable select pin.
CLS = “H”: Enable
CLS = ”L”: Disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin. When TL0324S is used in master/slave mode(multi-chip), the CL pin must be connected to each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input / output pin.
When TL0324S is used in master/slave mode(multi-chip), the M pin must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output. This pin is used together with the FR pin.</td></tr>
<tr><td>FR</td><td>O</td><td>Static driver common output. This pin is used together with the FRS pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input/output.
When TL0324S is used in master/slave mode (multi-chip), the DISP pin must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistor selects pin.
This pin selects the resistor for adjusting V0 voltage level and is available only in master mode.
INTRS = “H”: using built-in resistors.
INTRS = “L”: not using built-in resistors.
V0 voltage is controlled by VR pin with external resistive divider.</td></tr>
<tr><td>/HPM</td><td>I</td><td>Power control pin of the power supply circuits for LCD driver
- /HPM = “H”: normal mode
- /HPM = “L”: high power mode
This pin is valid only in master operation.</td></tr>
<tr><td>DSEL1 , DSEL0</td><td>I</td><td>The LCD driver duty ratio depends on the following table.(Duty Selection)
<table>
<tr><th>DSEL1</th><th>DSEL0</th><th>DUTY RATIO</th></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L</td><td>1/55</td></tr>
<tr><td>H</td><td>H</td><td>1/65</td></tr>
</table></td></tr>
</table>

Table 4-1. Pin description (continued)

<table>
<tr><th colspan="3">MPU interface</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>/RESET</td><td>I</td><td>Hardware reset input pin.
When /RESET is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel/Serial select input pin.
<table>
<tr><th>PS</th><th>Operating mode</th><th>Chip select</th><th>Data/ Instruction</th><th>Data I/O</th><th>Read/ Write</th><th>Serial</th></tr>
<tr><td>H</td><td>Parallel</td><td>/CS1, CS2</td><td>RS</td><td>DB7 to DB0</td><td>E_/RD, RW_/WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>/CS1, CS2</td><td>RS</td><td>DB7 (SID)</td><td>Write only</td><td>DB6 (SCLK)</td></tr>
</table>
When PS= “L”, DB5 to DB0 are high impedance.
E_/RD and RW_/WR are fixed to either “H” or “L”.
With serial data input, RAM display data reading is not supported.</td></tr>
<tr><td>C68</td><td>I</td><td>This pin is the MPU interface switch terminal.
C68 = “H”: 6800 series MPU interface
C68 = “L”: 8080 series MPU interface</td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>Chip select input pin.
Data input/output is enables only when /CS1 is low and CS2 is high.
When chip select is non-active, DB7 to DB0 will be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin.
RS = “H”: The data on DB7 to DB0 is used the display data.
RS = “L”: The data on DB7 to DB0 is used the control data.</td></tr>
<tr><td>RW_/WR</td><td>I</td><td>When interfacing to a 6800-series MPU, read/write is enabled at;
RW_/WR = “H”: read
RW_/WR = “L”: write
When interfacing to an 8080-series MPU, RW_/WR is enabled at low.
The signals on the data bus are latched at the rising edge of the RW_/WR signal.</td></tr>
<tr><td>E_/RD</td><td>I</td><td>When interfacing to a 6800-series MPU: Active High.
This pin is used as an enable clock input pin of the 6800-series MPU.
When interfacing to a 8080-series MPU: Active Low.
This pin is connected to the RD signal of the 8080-series MPU. While this signal is Low, TL0324S data bus output is enabled.</td></tr>
<tr><td>DB7
To
DB0</td><td>I/O</td><td>8-bit bi-directional data bus.
It is connected to the standard 8-bit microprocessor data bus.
In case of serial interface,(PS = ”L”)
DB7: Serial input data(SID)
DB6: Serial input clock(SCLK)
DB5 to DB0 : High impedance
When chip select is not active, DB7 to DB0 will be high impedance.</td></tr>
<tr><td>NC1
NC0</td><td>I/O</td><td>These are set to Open.</td></tr>
<tr><td>TEST15
to
TEST0</td><td>I/O</td><td>These are pins for IC chip testing.
These are set to Open.</td></tr>
</table>

Table 4-1. Pin description (continued)

<table>
<tr><th colspan="3">LCD driver output</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>LCD driver output for segment.
The display data and the FR signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">FR</th><th colspan="2">Segment output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM63</td><td>O</td><td>LCD driver output for common.
The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>FR</th><th>Common output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common signal output for the icons. The output signals of two pins are the same.
When this signal is not used, should be left open. In multi-chip(master/slave) mode, all COMS pin on both master and slave units are the same signal.</td></tr>
</table>

Note: -. DUMMY, TEST0 ~ TEST15, NC0, NC1: The pins should be opened (floated).

5. FUNCTIONAL DESCRIPTION

5-1. MICROPROCESSOR INTERFACE

a. Chip select input

There are /CS1 and CS2 pins for chip selection.

The TL0324S can interface with an MPU only when /CS1 is “L” and CS2 is “H”.

When these pins are set to any other combination, RS, E_/RD, and RW_/WR inputs are disabled and DB7 to DB0 are to be high impedance.

And, in case of serial interface, the internal shift register and the counter are reset.

b. Interface

TL0324S has three types of interface with an MPU, which are one serial and two parallel interfaces.

This parallel or serial interface is determined by PS pin as shown in table 5-1.

Table 5-1. Parallel / Serial interface mode

PS	Type	/CS1	CS2	C68	Interface mode
H	Parallel	/CS1	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	/CS1	CS2	X*	Serial MPU mode

* X : Don't care

c. Parallel interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 5-2.

The type of data transfer is determined by signals at RS, E_/RD, and RW_/WR as shown in table 5-3.

Table 5-2. Microprocessor selection for parallel interface

C68	/CS1	CS2	RS	E_/RD	RW_/WR	DB7 to DB0	MPU
H	/CS1	CS2	RS	E	RW	DB7 to DB0	6800-series
L	/CS1	CS2	RS	/RD	/WR	DB7 to DB0	8080-series

Table 5-3. Parallel data transfer

Common	6800-series		8080-series		Description
RS	E_/RD (E)	RW_/WR (RW)	E_/RD (/RD)	RW_/WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register(instruction)

d. Serial interface (PS = "L")

When the TL0324S is active and serial interface has been selected, the serial data (DB7) and the serial clock (DB6) inputs are enabled.

And TL0324S is not active, the internal 8-bit shift register and the 3-bit counter are reset.

The serial data can be read on the rising edge of the serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock.

The serial data input is display data when RS is high and control data when RS is low.

Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

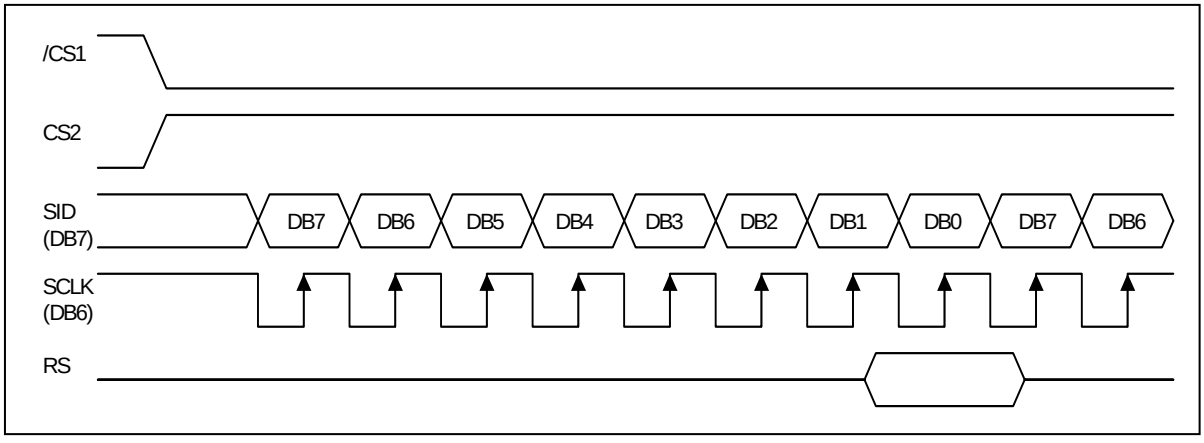

Figure 5-1. Serial interface timing

e. Busy flag

The busy flag indicates whether the TL0324S is operating or not.

When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction.

If the cycle time is correct, the MPU needs not to check this flag before each instruction, which improves the MPU performance.

f. Data accessing

The TL0324S uses bus holder and internal data bus for data read and data write with the MPU.

When writing data from the MPU to on-chip RAM, the data is automatically transferred from the bus holder to the on-chip RAM as shown in figure 5-2. When the MPU reads data from on-chip RAM, the first data read cycle stores the data in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5-3. This means the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data. Therefore, a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed.

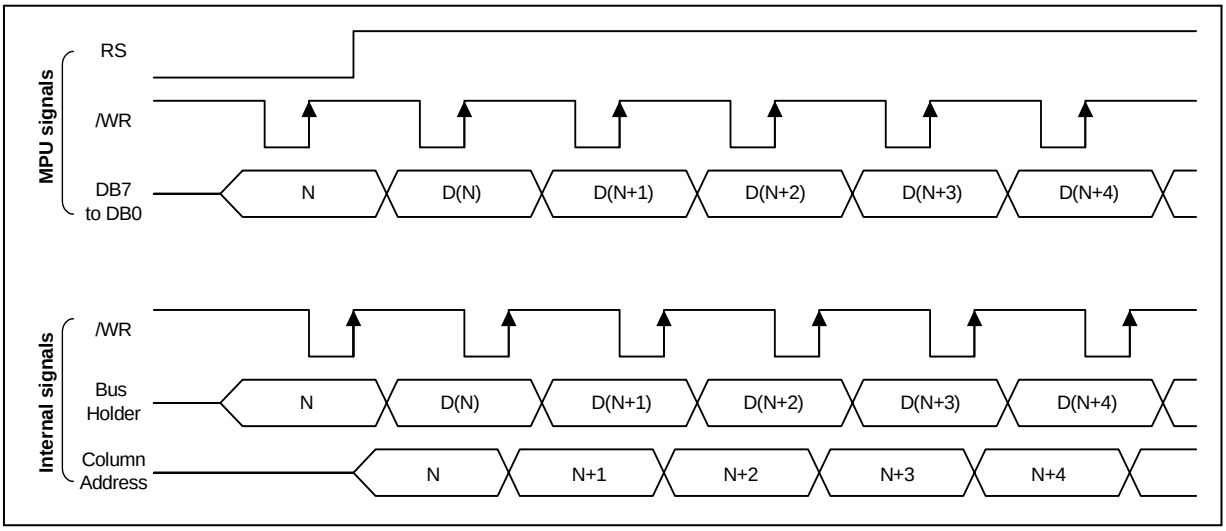

Figure 5-2. Write timing

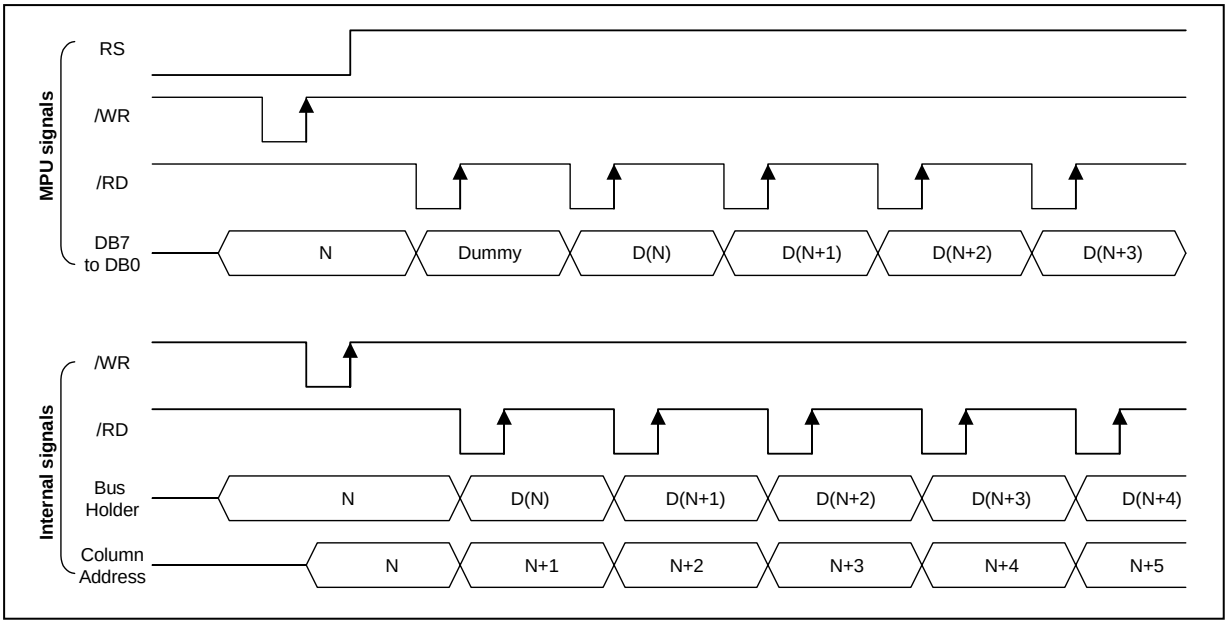

Figure 5-3. Read timing

5-2. DISPLAY DATA RAM (DDRAM)

a. DDRAM

The DDRAM stores pixel data for the LCD.

It has 65-row (8 page x 8 bit + 1) by 132-column addressable array.

Each pixel can be selected by specifying the page and the column address.

The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB7 to DB0.

The display data of DB0 to DB7 from the MPU correspond to the LCD common direction as shown in Figure 5-4.

The MPU can read from and write to DDRAM through the I/O buffer, which is independent operation from signal reading for the LCD driver.

This independent operation makes it possible that the MPU writes the data into the DDRAM at the same time as data is being displayed without causing the LCD flicker.

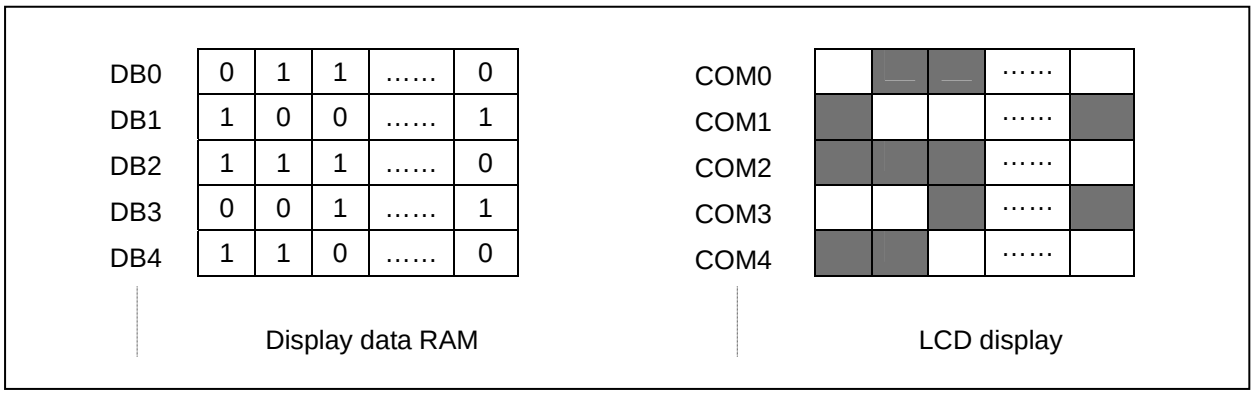

Figure 5-4. RAM-to-LCD data transfer

b. Page address circuit

This circuit is for providing a page address to DDRAM shown in figure 6-6.

The 4-bit page address register changed by only the “Set page” instruction.

Page address 8 (DB3, DB2, DB1, DB0 = 1, 0, 0, 0) is a special RAM area for the icons and display data DB0 is only valid.

When Page Address is above 8, it is impossible to access to on-chip RAM.

c. Column address circuit

Column address circuit has a 8-bit preset counter that provides column address to the DDRAM as shown in figure 5-6.

When the “Set column address MSB / LSB” instruction is issued, 8-bit [Y7:Y0] is updated.

And this address is increased by +1 each display data Read/Write instruction.

This allows that the MPU display data can be accessed continuously.

The increment of the column address stops with 83H. And the counter is not increased and locked if the address is specified over 84H.

It is unlocked if a column address is set again by “Set column address MSB / LSB” instruction.

The column address counter is independent of the page address register.

The ADC select instruction makes it possible to convert the relationship between the column address and the segment outputs.

It is necessary to rewrite the display data on built-in RAM after issuing the ADC select instruction.

Refer to the figure 5-5.

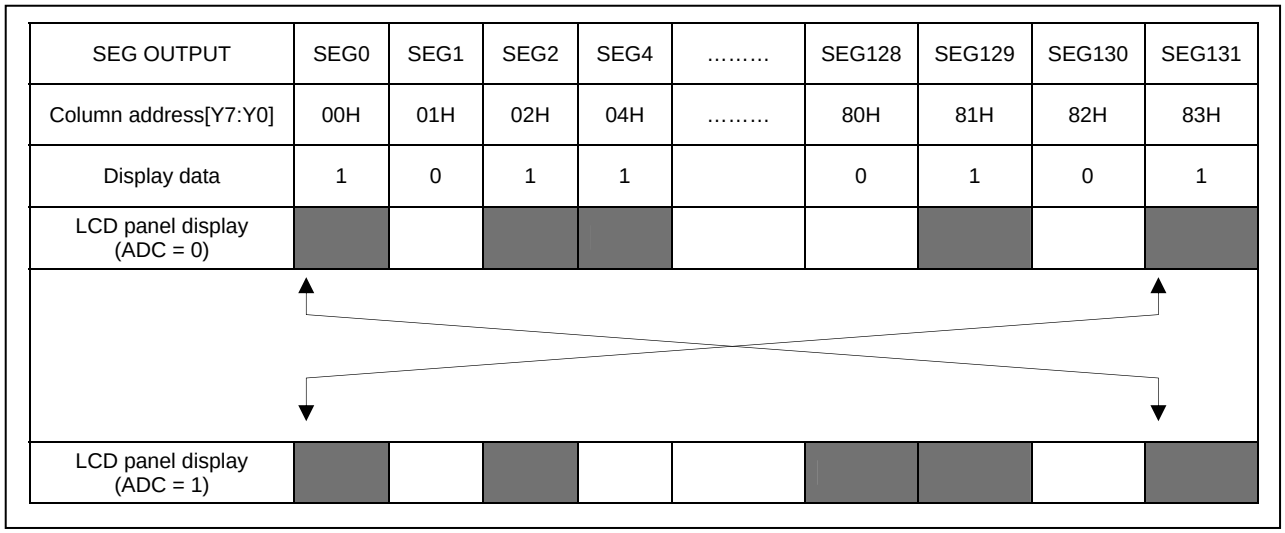

Figure 5-5. The relationship between the column address and the segment outputs

d. Line address circuit

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display.

Using the display start line address set command, what is normally the top line of the display can be specified. By setting the line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of DDRAM as shown in figure 5-6.

At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by +1 and the line address is generated for transferring the 132-bit RAM data to the display data latch circuit.

However, the display data of icons is not scrolled because the MPU can not access the line address of icons.

e. Segment control circuit

This circuit controls the display data by the Display ON / OFF, reverse display ON / OFF and entire display ON /OFF instructions without changing the data in the DDRAM.

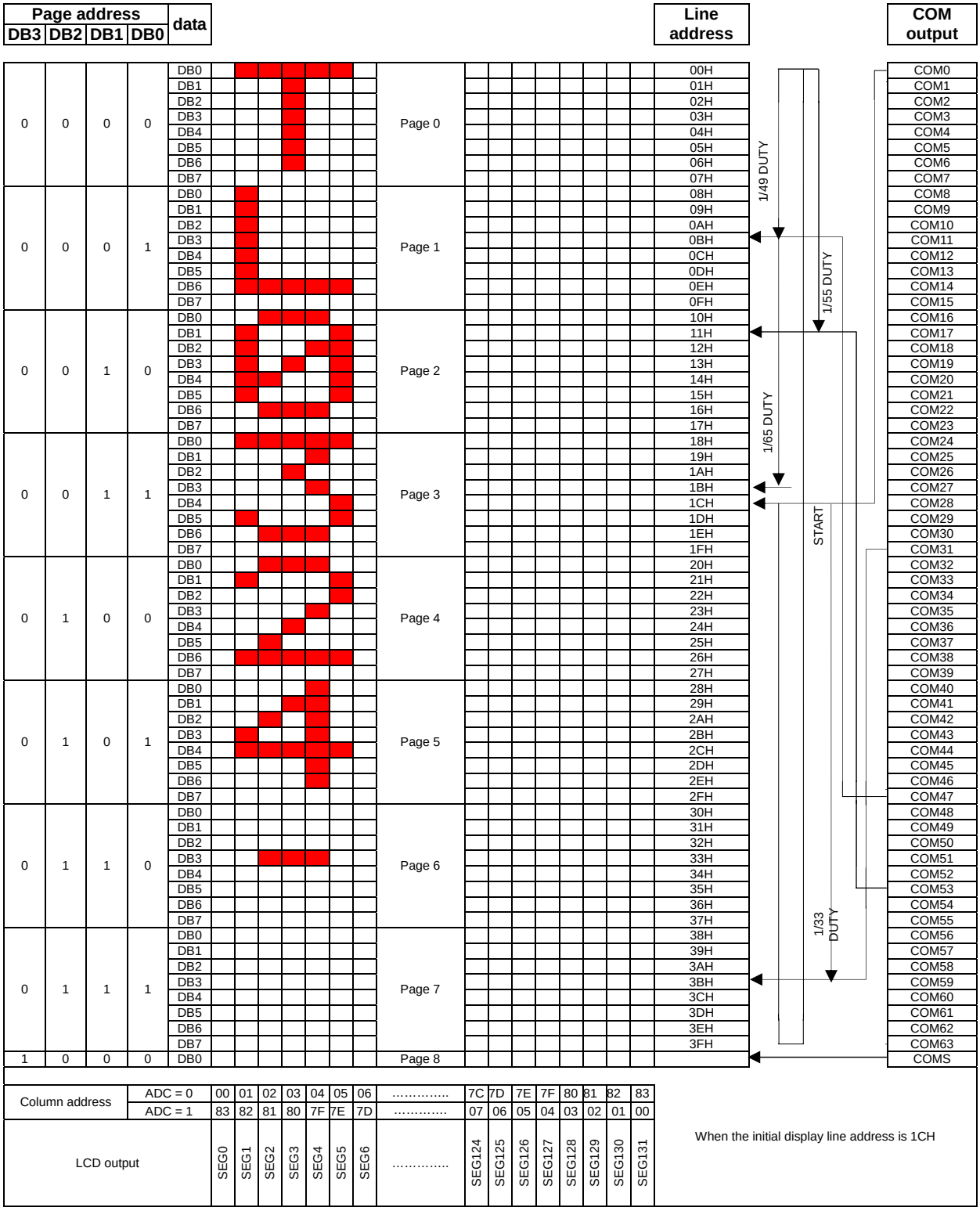

Figure 5-6. Display data RAM map

5-3. LCD DISPLAY CIRCUITS

a. Oscillator

TL0324S implement complete on-chip oscillator and its frequency is nearly independent of V_{DD}.

This oscillator signal is used in the voltage converter and display timing generation circuit.

The oscillator circuit is enabled when MS="H" and CLS="H".

When the external clock is used, set CLS="L" and imply clock signal to CL pin.

b. Display timing generator circuit

This circuit generates timing signals to be used for displaying LCD.

The display clock (CL) is generated by oscillation clock and CL generates the clock for the line counter and the signal for the display data latch.

The line address of DDRAM is generated in synchronization with CL.

The 132-bit display data is latched in the display data latch circuit synchronized with CL.

Reading to the display data liquid crystal driver circuit is completely independent of access to the DDRAM by the MPU.

The display timing generator circuit generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver.

Driving 2-frame AC driver waveform and internal timing signal are shown in figure 5-7.

When TL0324S is used multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master.

Table 5-4 shows the M, CL, and DISP status.

Table 5-4. Master and slave timing signal status

Operation mode	Clock	MS	CLS	M	CL	FRS, FR	DISP
Master mode	Internal	H	H	Output	Output	Output	Output
	External	H	L	Output	Input	Output	Output
Slave mode	Internal	L	H	Input	Input	Output	Input
	External	L	L	Input	Input	Output	Input

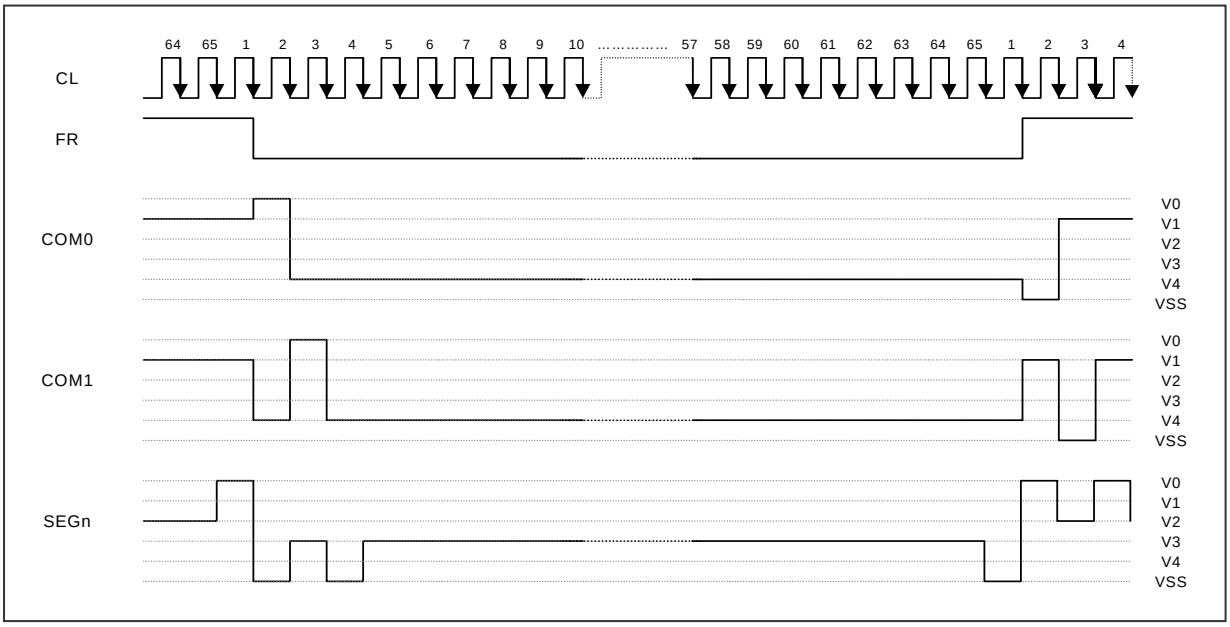

Figure 5-7. 2-frame AC driving waveform (Duty ratio = 1/65)

c. Common output control circuit

This circuit controls the relationship between the number of common output and specified duty ratio.

SHL select instruction specifies the scanning direction of the common output pins.

Table 5-5. The relationship between duty ratio and common output

Duty	SHL	Common output pins							
		COM [0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM [48:63]	COMS
1/33	0	COM[0:15]	*NC					COM[16:31]	COMS
	1	COM[31:16]	*NC					COM[15:0]	
1/49	0	COM[0:23]		*NC			COM[24:47]		COMS
	1	COM[47:24]		*NC			COM[23:0]		
1/55	0	COM[0:26]			*NC	COM[27:53]			COMS
	1	COM[53:27]			*NC	COM[26:0]			
1/65	0	COM[0:63]							COMS
	1	COM[63:0]							

*NC : No Connection

5-4. LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel common drivers (including 2COMS channels) and 132-channel segment drivers.

This LCD panel driver voltage depends on the combination of display data and FR signal.

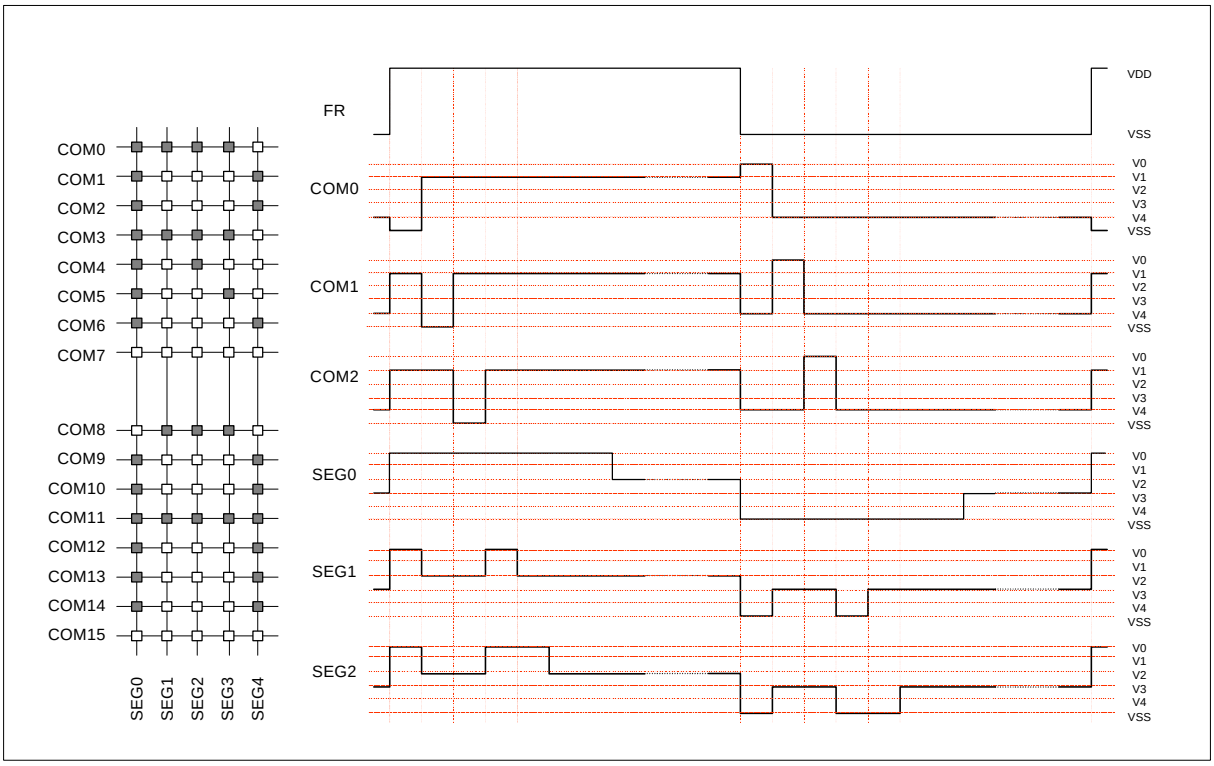

Figure 5-8. Segment and common timing

5-5. POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components.

There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits.

They are valid only in master operation and controlled by power control instruction.

For details, refers to "Instruction description".

Table 5-6 shows the referenced combinations in using power supply circuits.

Table 5-6. Recommended power supply combinations

Mode Settings	VC,VR,VF	Voltage converter	Voltage regulator	Voltage follower	V_{OUT}	V0	V1 to V4
All Internal power supply	1, 1, 1	ON	ON	ON	Open	Open	Open
Voltage regulator and voltage follower	0, 1, 1	OFF	ON	ON	External input	Open	Open
Voltage follower	0 , 0, 1	OFF	OFF	ON	Open	External input	Open
All external power supply	0, 0, 0	OFF	OFF	OFF	Open	External input	External input

a. Voltage converter circuits

These circuits boost up the electric potential between VCI and VSS to 2, 3, 4 or 5 times toward positive side and boosted voltage is outputted from V_{OUT} pin.

[C1 = 1.0 to 4.7μF]

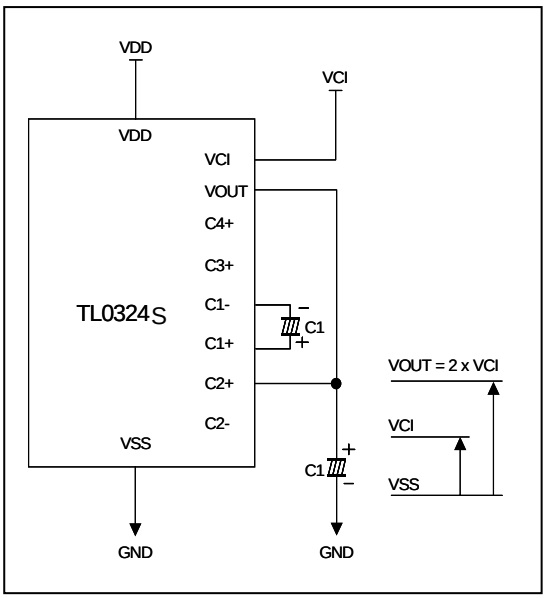

Figure 5-9. Two times boosting circuit

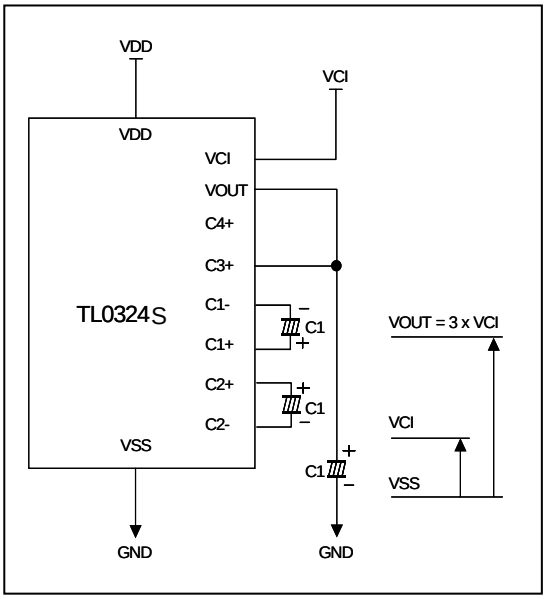

Figure 5-10. Three times boosting circuit

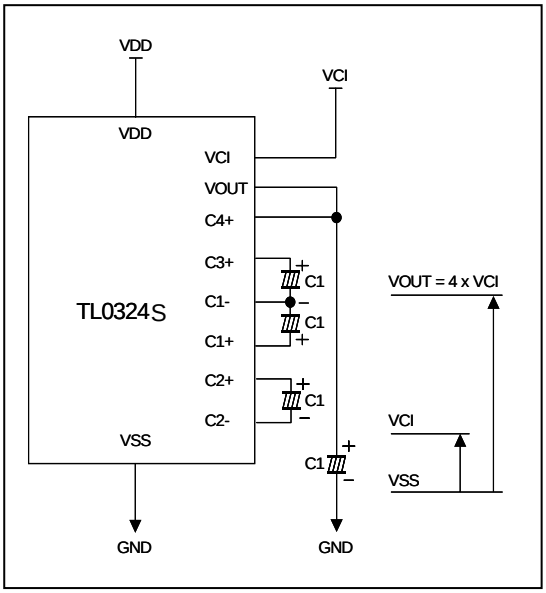

Figure 5-11. Four times boosting circuit

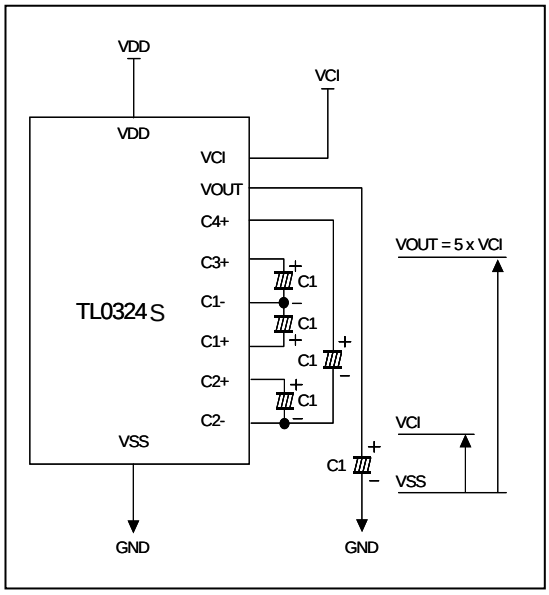

Figure 5-12. Five times boosting circuit

*. The VCI voltage range must be set so that the V_{OUT} voltage does not exceed the absolute maximum rated value.

b. Voltage regulator circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by the adjusting resistors, Ra and Rb, within the range of |V0| < | V_{OUT} |.

Because V_{OUT} is the operating voltage of operational-amplifier circuits as shown in figure 5-13, it is necessary to be applied internally or externally.

For the equation 1, we determine V0 by Ra, Rb and V_{EV}. Ra and Rb are connected internally or externally by INTRS pin.

The voltage of electronic volume, V_{EV}, is determined by equation 2, where the reference voltage parameter α is the value selected by instruction, "Set reference voltage register", within the range 0 to 63. Refer to table 5-8.

VREF voltage at Ta =25°C is show in table 5-7.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \quad \text{------ (Equation 1)}$$

$$V_{EV} = \left(1 - \frac{(63-\alpha)}{162}\right) \times VREF \quad [V] \text{ ------ (Equation 2)}$$

Table 5-7. VREF voltage at Ta =25°C

REF	Temp. coefficient	V_{REF}[V]
H	-0.05% / °C	2.1
L	External input	VEXT

Table 5-8. Electronic contrast control register (Reference Voltage Parameter: α, 64step)

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62	:	:
1	1	1	1	1	1	63	Maximum	High

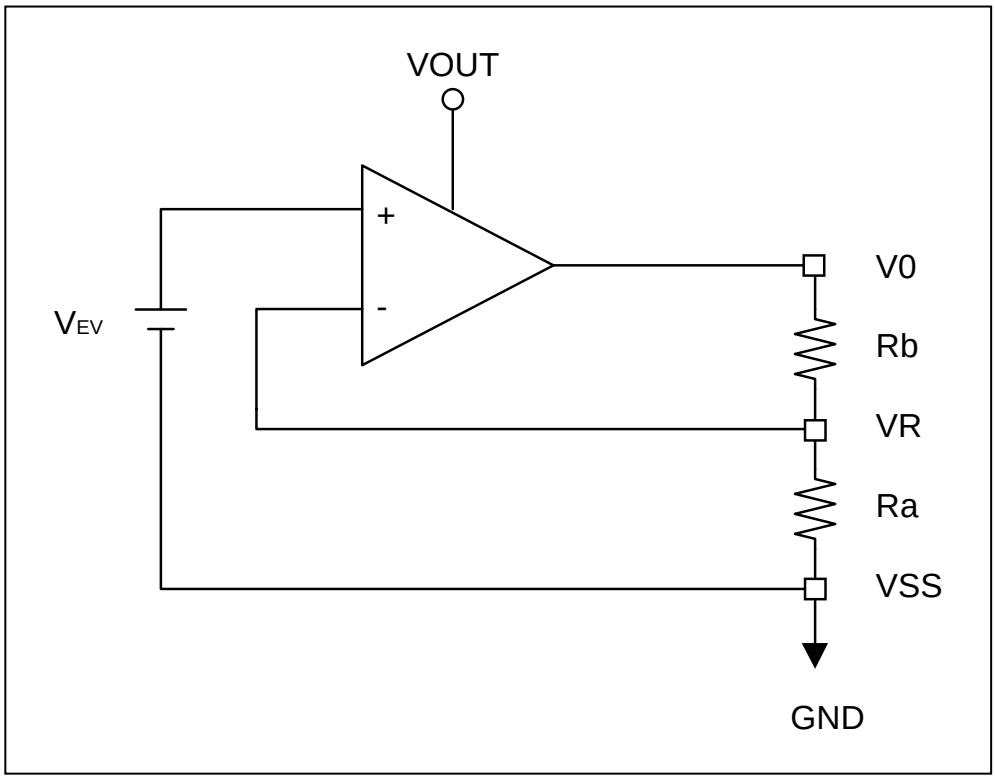

Figure 5-13. Internal voltage regulator circuit

b-1. In case of using internal resistors, Ra and Rb (INTRS = "H")

When INTRS pin is “H”, resistor Ra is connected internally between VR pin and V_{SS}, and Rb is connected between V0 and VR.

We determine V0 by two instructions, " Select Regulator resistor" and "Set reference voltage".

Table 5-9. Internal Rb / Ra ratio depending on 3-bit Data (R2, R1, R0)

	3-bit data settings (R2 R1 R0: gain)							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
1+(Rb/Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

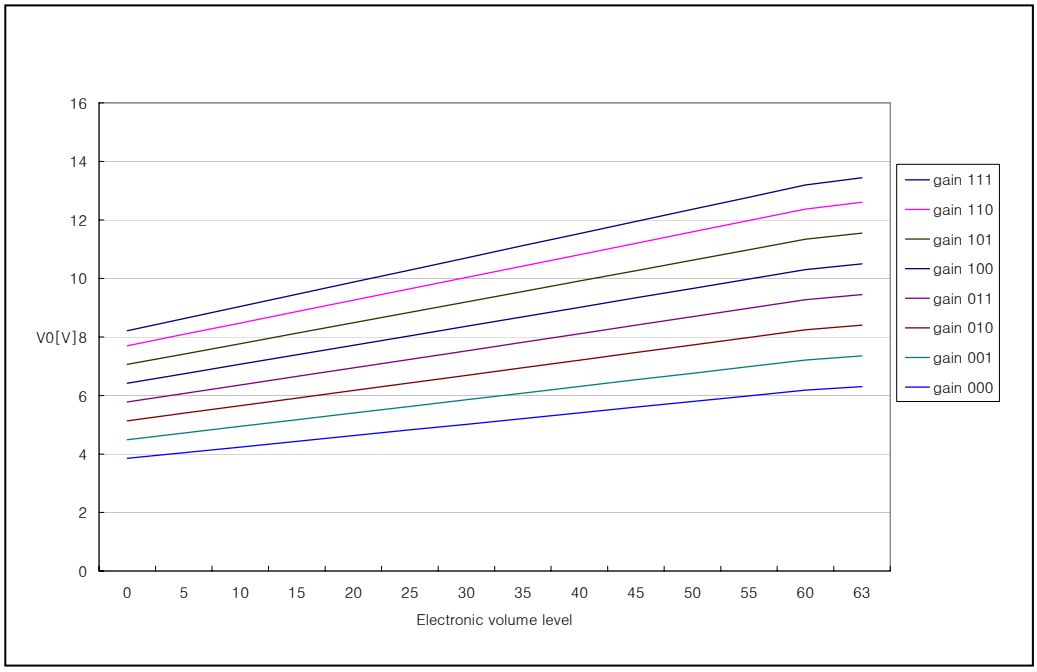

Figure 5-14. Electronic volume level

b-2. In case of using external resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is “L”, it is necessary to connect external regulator resistor Ra between VR and V_{SS}, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0 : α = 32)
3. Maximum current flowing Ra, Rb = 1[μA]

From equation 1

$$10 = \left(1 + \frac{Rb}{Ra} \right) \times V_{EV} \quad [V] \quad \text{------} \qquad \text{(Equation 3)}$$

From equation 2

$$V_{EV} = \left(1 - \frac{(63-32)}{162} \right) \times 2.1 \cong 1.698 \quad [V] \text{ ------ (Equation 4)}$$

From equation 3

$$\frac{10}{(Ra + Rb)} = 1[\mu A] \quad \text{------ (Equation 5)}$$

From equation 3, 4 and 5

Ra = 1.69[MΩ]
Rb = 8.31[MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 5-10. V0 depending on electronic volume level

	Electric Volume Level				
	0	**------**	**32**	**-------**	**63**
V0	7.57	------	10.00	-------	12.43

c. Voltage follower circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the voltage follower for increasing drive capability.

The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 5-11. The relationship between V1 to V4 level and duty ratio

Duty Ratio	DSEL1	DSEL0	LCD Bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
			1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/49	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/55	H	L	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/65	H	H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
			1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

d. High power mode

The power supply circuit equipped in the TL0324S for LCD drive has very low power consumption (in normal mode : /HPM = “H”).

If use for LCD panels with large loads, this low-power supply may cause display quality to degrade.

When this occurs, setting the /HPM pin to “L”(high power mode) can improve the quality of the display. Moreover, if the quality of display is inadequate even after High Power mode has been set, then it is necessary to add a liquid crystal drive power supply externally (V_{OUT} or V0 or V1 V2 V3 V4).

5-6. REFERECE CIRCUIT EXAMPLS

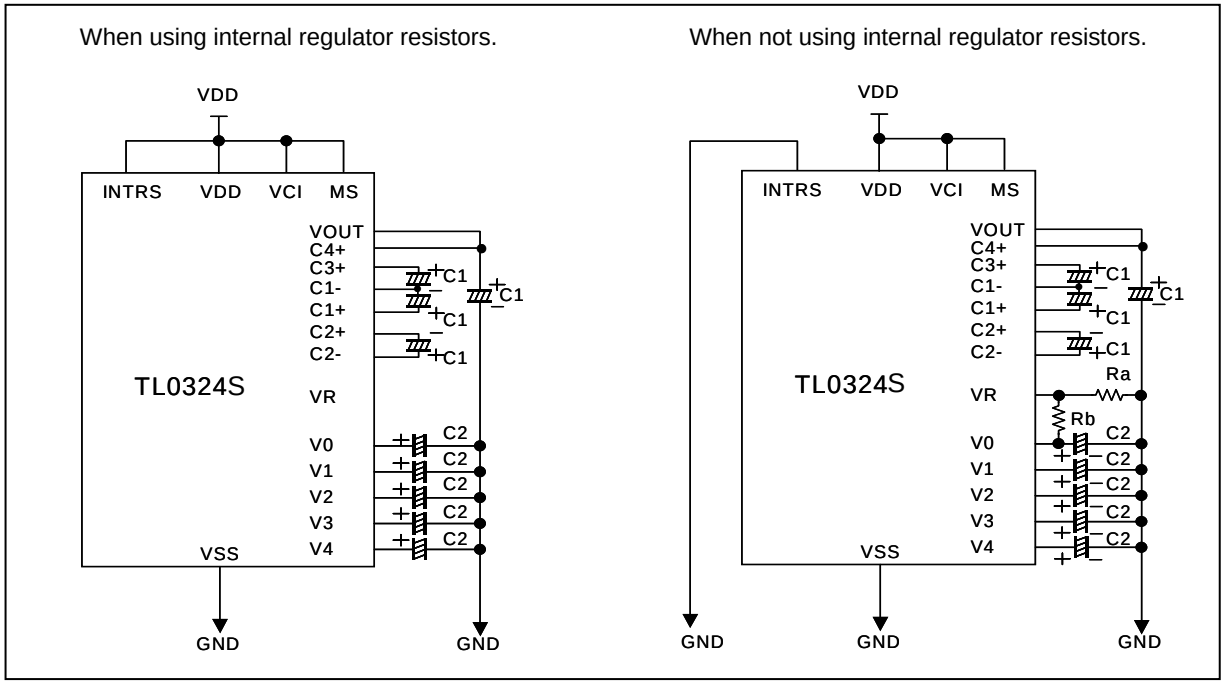

Figure 5-15. When using all LCD power circuits (VCI = VDD, 4-time, V/C: ON, V/R: ON, V/F: ON)

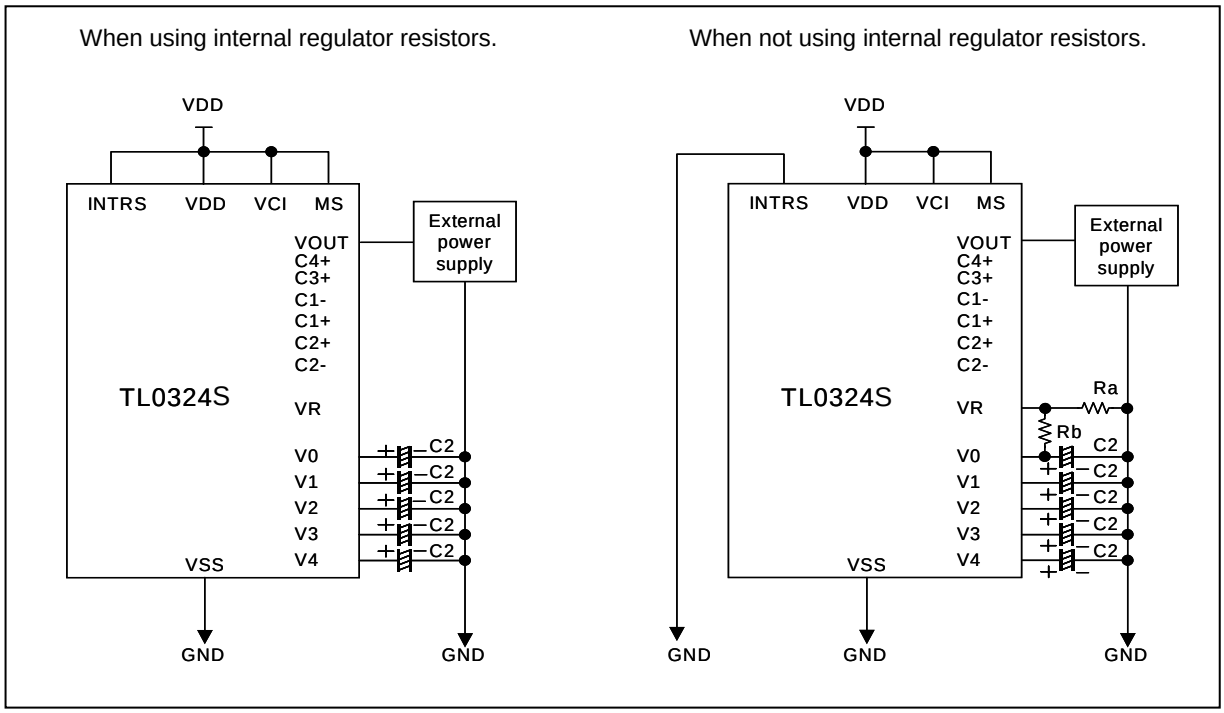

Figure 5-16. When using some LCD power circuits (VCI = VDD, V/C: OFF, V/R: ON, V/F: ON)

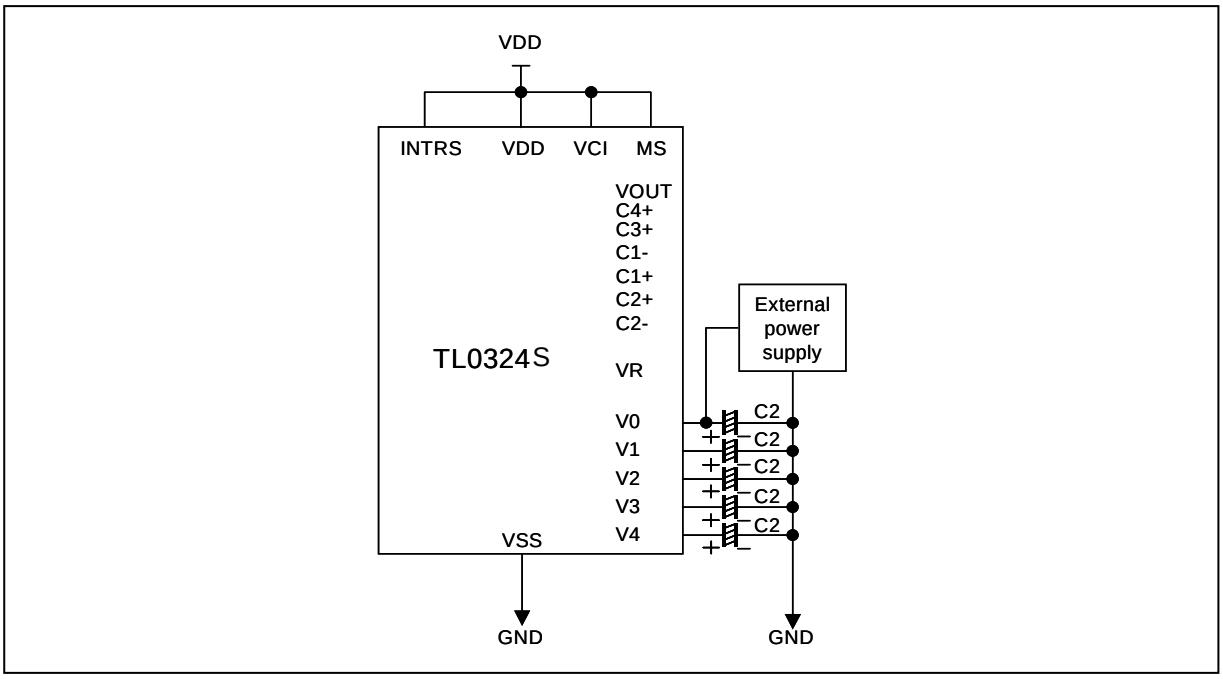

Figure 5-17. When using some LCD power circuits (VCI = VDD, V/C: OFF, V/R: OFF, V/F: ON)

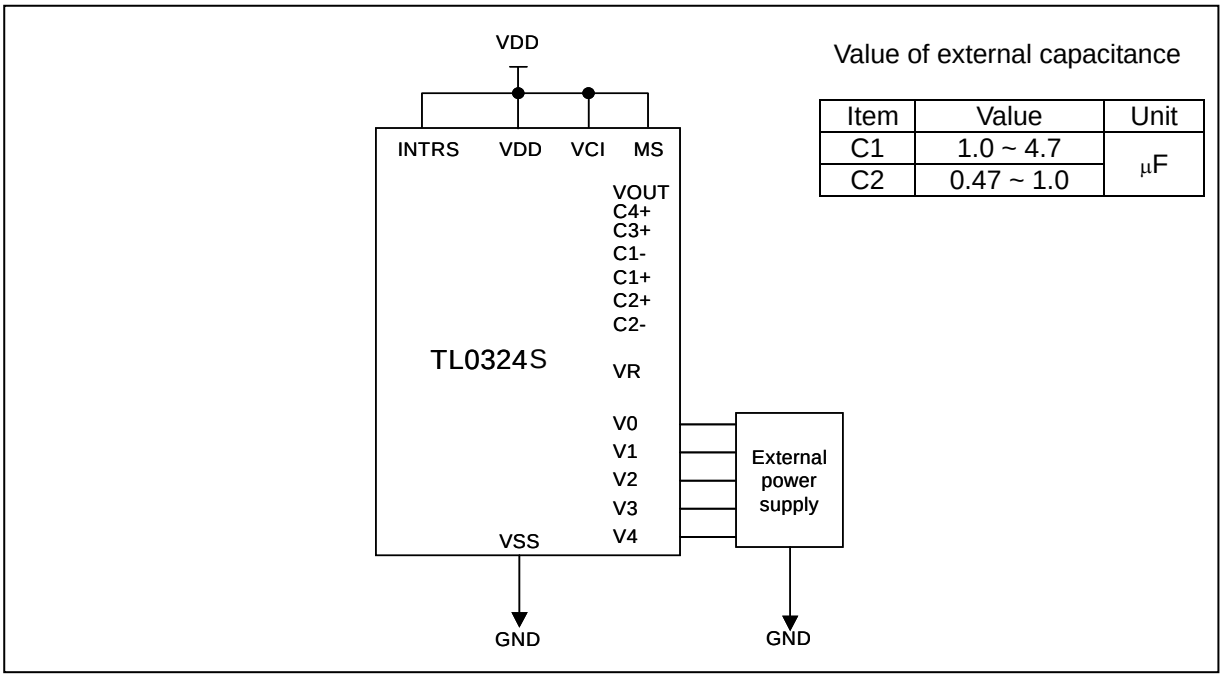

Figure 5-18. When not using any LCD power supply circuits(VCI = VDD, V/C: OFF, V/R: OFF, V/F: OFF)

*. C1 and C2 are determined by the size of the LCD being driven.
Select a value that will stabilize the liquid crystal drive voltage.

5-7. RESET CIRCUIT

Setting /RESET to “L” or reset instruction can initialize internal function.
When /RESET becomes “L”, following procedure is occurred.

Display ON / OFF: OFF (DON = 0).
Entire display ON / OFF: OFF (normal = 0).
ADC select: OFF (normal = 0)
Reverse display ON / OFF: OFF (normal = 0).
Power control register (VC, VR, VF) = (0, 0, 0)
Serial interface internal register data clear
LCD power supply bias ratio: bias bit 0

(Refer to LCD bias select of instruction table and duty ratio by DSEL1, DSEL0 pin setting)

Duty ratio	DSEL1	DSEL0	Liquid crystal bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

On-chip oscillator OFF (while /RESET is “L”)
Power save release
Set modify-read: OFF
SHL select: OFF (normal = 0).
Static indicator mode: OFF.
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0.
Page address: 0
Select Regulator Resistor register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

When RESET instruction is issued, following procedure is occurred.

Set modify-read: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: OFF (normal = 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Select Regulator Resistor register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

While /RESET is “L”, or Reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4.
After DB4 becomes “L”, any instruction can be accepted.
/RESET must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by /RESET is essential before used.

6. PROGRAM INSTRUCTION DESCRIPTION

Table 6-1. Instruction table X: Don't' care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON / OFF	/RESET	0	0	0	0	Read the internal status
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF LCD panel When DON = 0: display OFF When DON=1 : display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	X	X	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction. When ADC = 0 : normal direction (SEG0 ⇒ SEG131) When ADC = 1 ; reverse direction (SEG131⇒ SEG 0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0 : normal display When REV = 1 : reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0 : normal display When EON = 1 : entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal function
SHL select	0	0	1	1	0	0	SHL	X	X	X	Select COM output direction When SHL = 0 : normal direction (COM0⇒ COM63) When SHL = 1 : reverse direction (COM63 ⇒ COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select Regulator Resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	X	X	X	X	X	X	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON
NOP	0	0	1	1	1	0	0	0	1	1	Non-Operation command
Test Instruction_1	0	0	1	1	1	1	X	X	X	X	Don't use this instruction
Test Instruction_2	0	0	1	0	0	1	X	X	X	X	Don't use this instruction

6-1. Read display data

The 8-bit data from DDRAM specified by the column address and the page address can be read by this instruction.

As the column address is increased by 1 automatically after each this instruction, the MPU can continuously read the data from the addressed page.

A dummy read is required after loading an address into the column address register.

Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

6-2. Write display data

8-bit data of display data from the MPU can be written to the RAM location specified by the column address and page address.

The column address is increased by 1 automatically so that the MPU can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

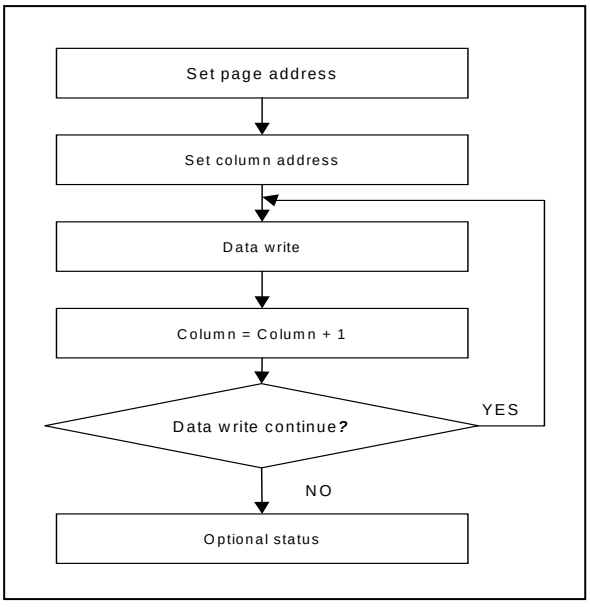

Figure 6-1. Sequence for writing display data

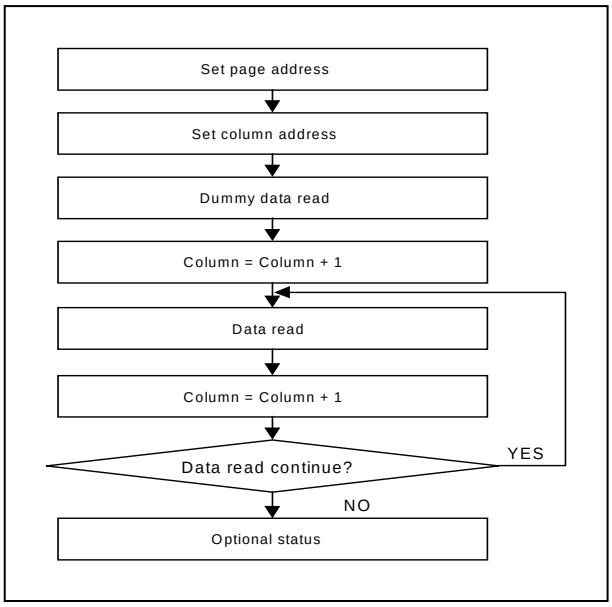

Figure 6-2. Sequence for reading display data

6-3. Read status

Indicates the internal status of the TL0324S.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	/RESET	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG131 –>SEG0), 1: normal direction (SEG0 –>SEG131)
ON / OFF	Indicates display ON / OFF status 0: display ON, 1: display OFF
/RESET	Indicate the /RESET. 0: chip is active, 1: chip is being reset

6-4. Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

6-5. Initial Display Line

Sets the line address of DDRAM to determine the initial display line.

The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

6-6. Reference voltage select

Consists of 2-byte instruction the first instruction sets reference voltage mode, the second one updates the contents of reference voltage register.

After second instruction, reference voltage mode is released.

The first instruction: Set reference voltage select mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The second instruction: Set reference voltages select mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (α)	V0	Contrast
0	0	0	0	0	0	0	Min	Low
0	0	0	0	0	1	1	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62	:	:
1	1	1	1	1	1	63	Max	High

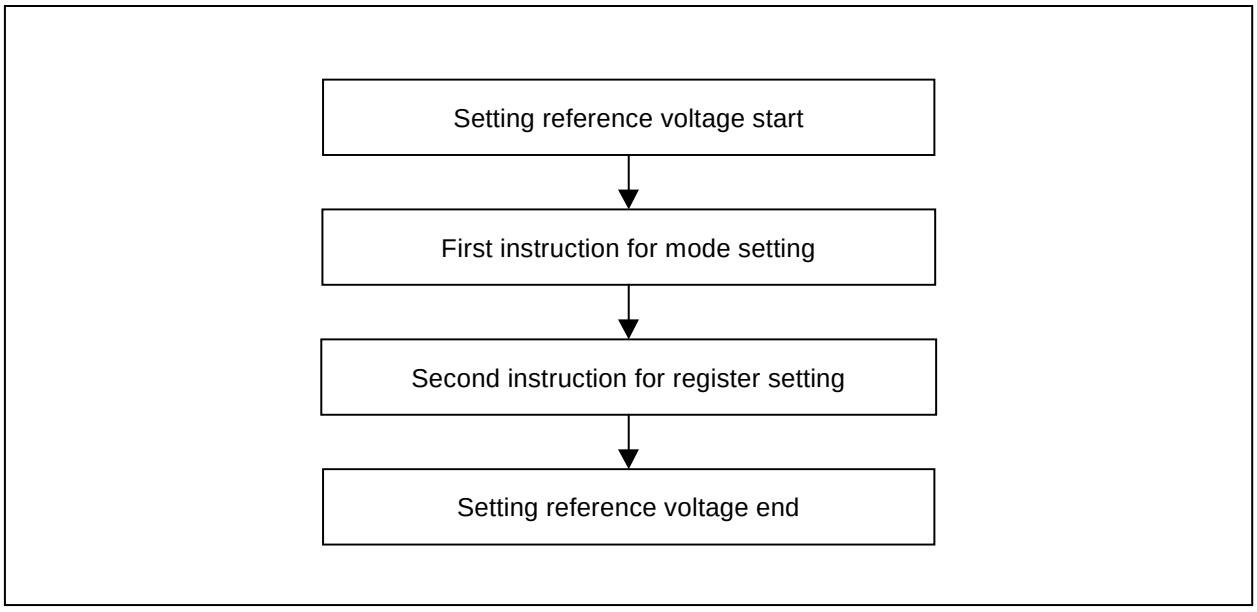

Figure 6-3. Sequence for setting the reference voltage

6-7. Set page address

Sets the page address of DDRAM from the MPU into the page address register.

Any RAM data bit can be accessed when its page address and column address are specified.

Along with the column address, the page address defines the address of the DDRAM to write or read display data.

Changing the page address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P 3	P 2	P 1	P 0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

6-8. Set column address

Sets the column address of DDRAM from the MPU into the column address register.

Along with the column address, the column address defines the address of the DDRAM to write or read display data.

When the MPU reads or writes display data to or from DDRAM, column addresses are automatically increased.

Set column address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set column address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:			:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

6-9. ADC select

Changes the relationship between DDRAM column address and segment driver.

The direction of segment driver output pin can be reversed by software.

This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 ⇒ SEG131)
ADC = 1: reverse direction (SEG131 ⇒ SEG0)

6-10. Reverse display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the DDRAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0(Normal)	Liquid crystal pixel is illuminated	Liquid crystal pixel is not illuminated
1(Reversed)	Liquid crystal pixel is not illuminated	Liquid crystal pixel is illuminated

6-11. Entire display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the DDRAM.

At this time, the contents of the DDRAM are held.

This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

6-12. Select LCD bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DSEL1	DSEL0	Liquid crystal bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

6-13. Set modify-read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction.

And it reduces the load of the MPU when the data of a specific area is repeatedly changed during cursor blinking or others.

This mode is canceled by the reset modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

6-14. Reset modify-read

This instruction cancels the modify-read mode, and makes the column address return to its initial value just before the set modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

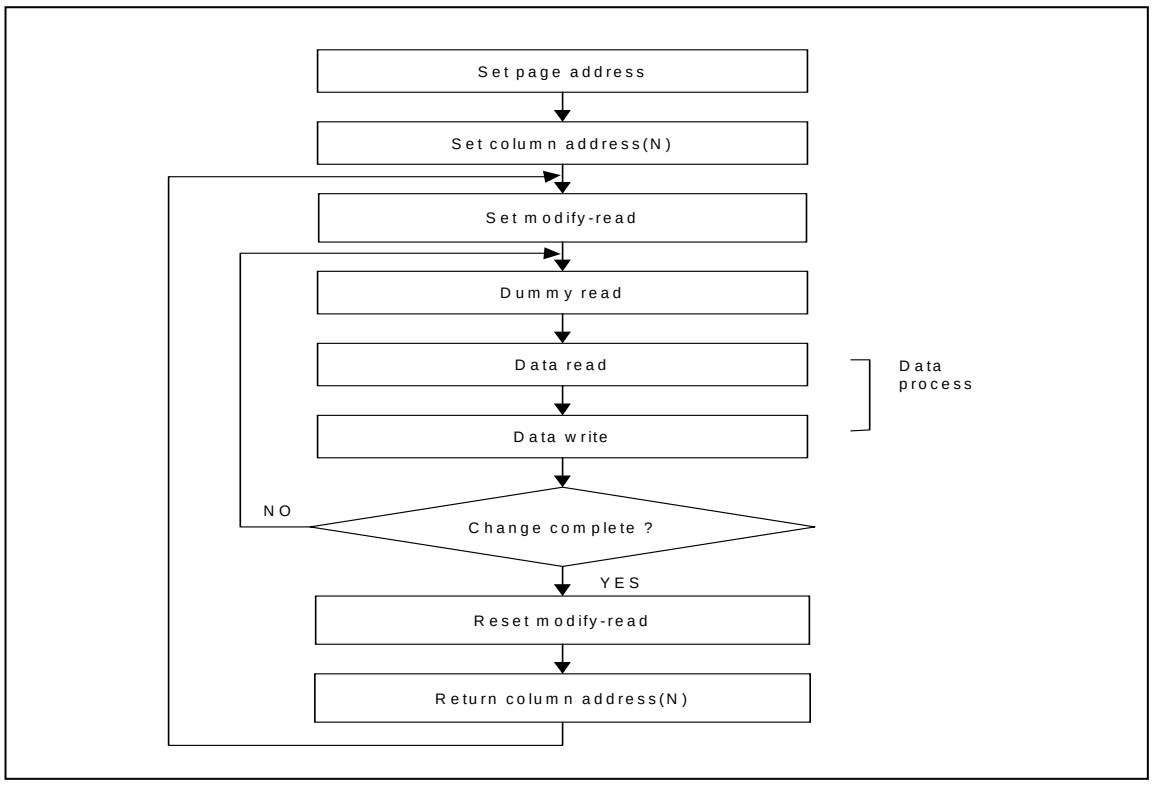

Figure 6-4. Sequence for cursor display

6-15. Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affects the contents of DDRAM.

This instruction can not initialize the LCD power supply which is initialized by the /RESET pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

6-16. SHL select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	X	X	X

SHL = 0: normal direction (COM0 ⇒ COM63) X : Don't care
SHL = 1: reverse direction (COM63 ⇒ COM0)

6-17. Power control

Selects one of eight power circuit functions by using 3-bit register.

An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Internal power supply circuits status
0 1			Voltage converter circuit is OFF Voltage converter circuit is ON
	0 1		Voltage regulator circuit is OFF Voltage regulator circuit is ON
		0 1	Voltage follower circuit is OFF Voltage Follower circuit is ON

6-18. Select Regulator Resistor

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 5-9.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

6-19. Set static indicator state

Consists of two bytes instruction.

The first byte instruction (set static indicator mode) enables the second byte instruction (set static indicator register) to be valid.

The first byte sets the static indicator ON / OFF. When it is ON, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

The first instruction: Set static indicator mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The second instruction: Set static indicator register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	X	X	X	X	S1	S0

S1	S0	Static indicator output status
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

6-20. NOP

Non Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

6-21. Test Instruction (Test Instruction_1 & Test Instruction_2)

These are the instruction for IC chip testing.

Please do not use it.

If the Test Instruction is used by accident, it can be cleared by applying “0” signal to the /RESET input pin or the reset instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	X	X	X	X
0	0	1	0	0	1	X	X	X	X

6-22. Power save (Compound instruction).

If the entire display ON / OFF instruction is issued during the display OFF state, TL0324S enters the power save status to reduce the power consumption to the static power consumption value.

According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode).

When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued.

Power save mode is released by the display OFF instruction.

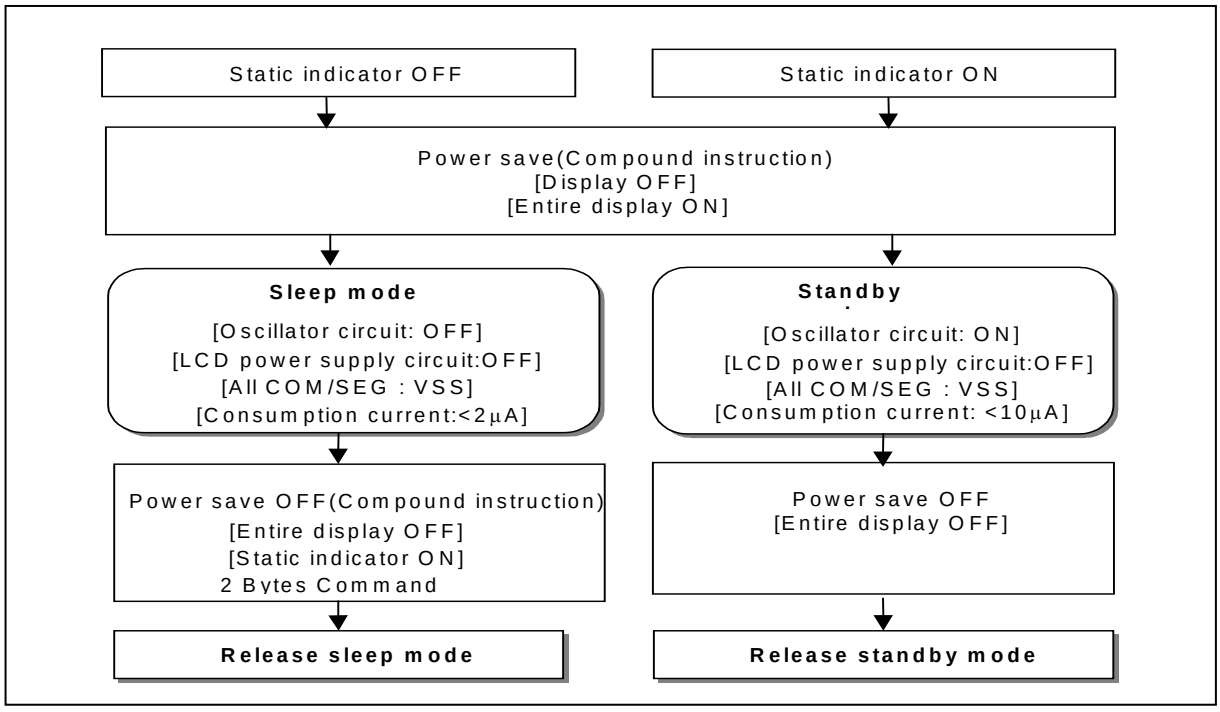

Figure 6-5. Power save routine

-Sleep Mode

This stops all operations in the LCD display system, and as long as there are no access from the MPU, the consumption current is reduced to a value near the static current.

The internal modes during sleep mode are as follows:

a. The oscillator circuit and the LCD power supply circuit are halted.
b. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VSS level.

-Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive.

The internal modes are in the following states during standby mode.

a. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
b. The duty drive system liquid crystal drive circuits are halted and the segment and common drive outputs a VSS level.
   When a reset command is performed while in standby mode, the system enters sleep mode.

6-23. Referential instruction setup flow (1)

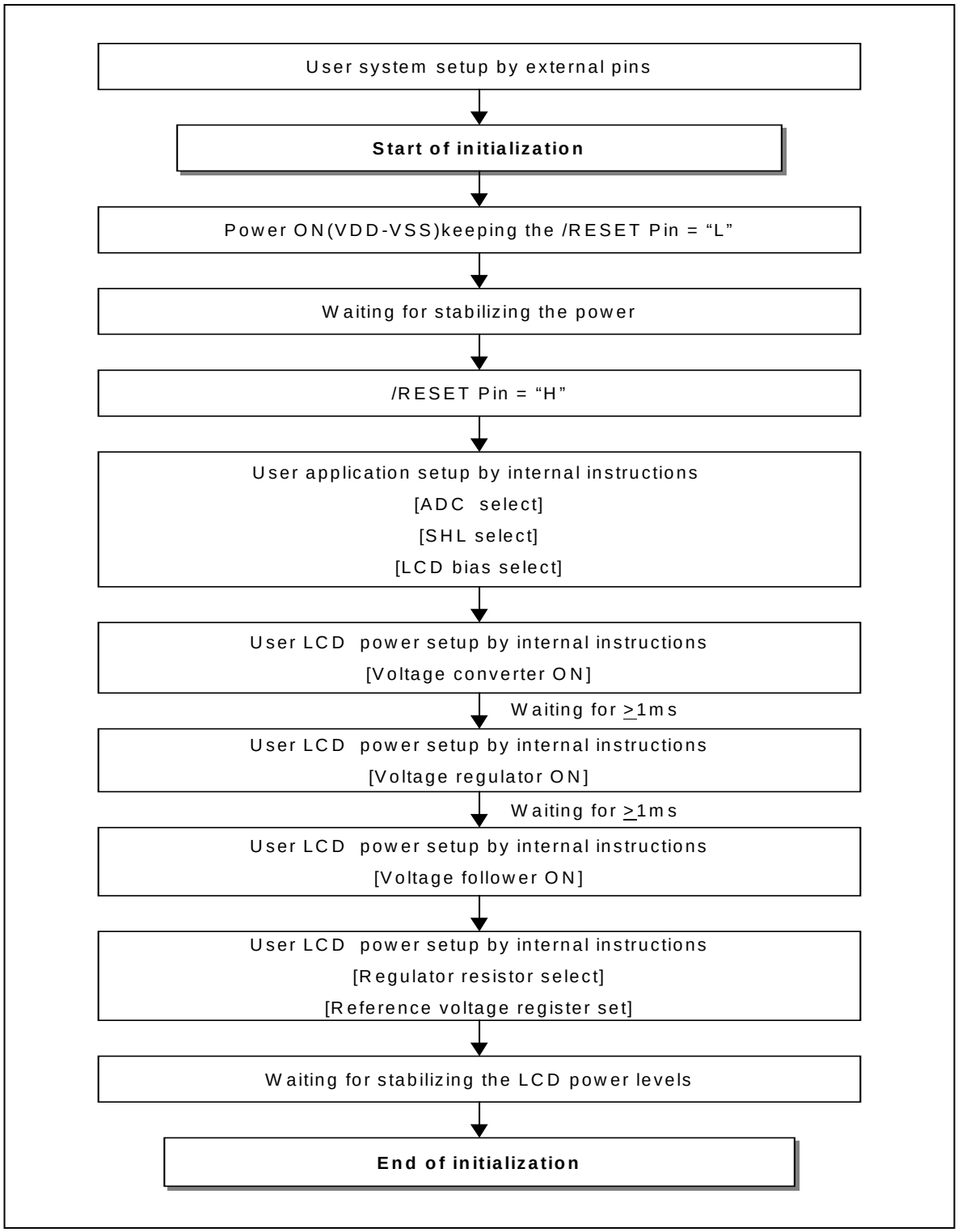

Figure 6-6. Initializing with the built-in power supply circuits

Referential instruction setup flow (2)

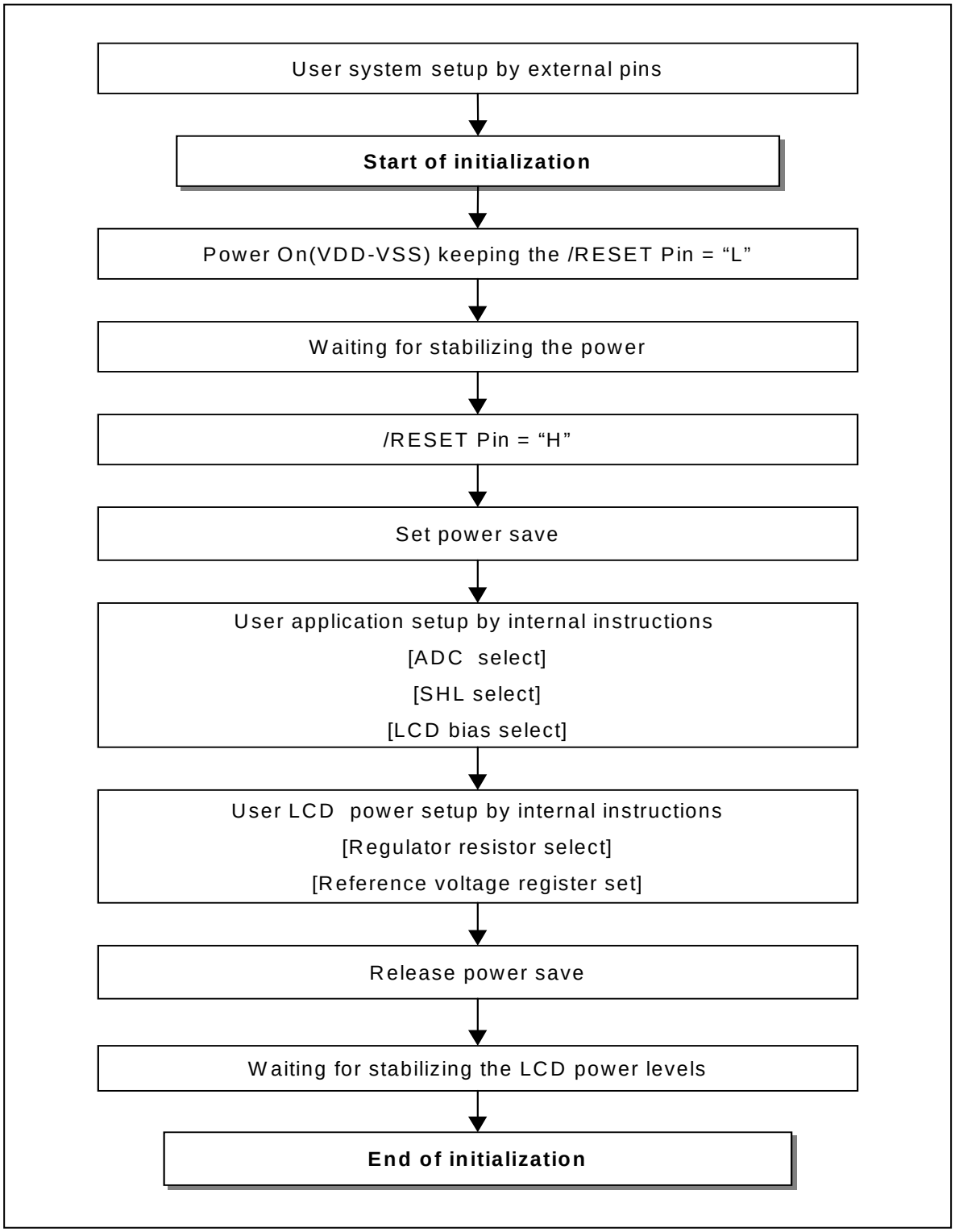

Figure 6-7. Initializing without the built -in power supply circuits

Referential Instruction Setup Flow (3)

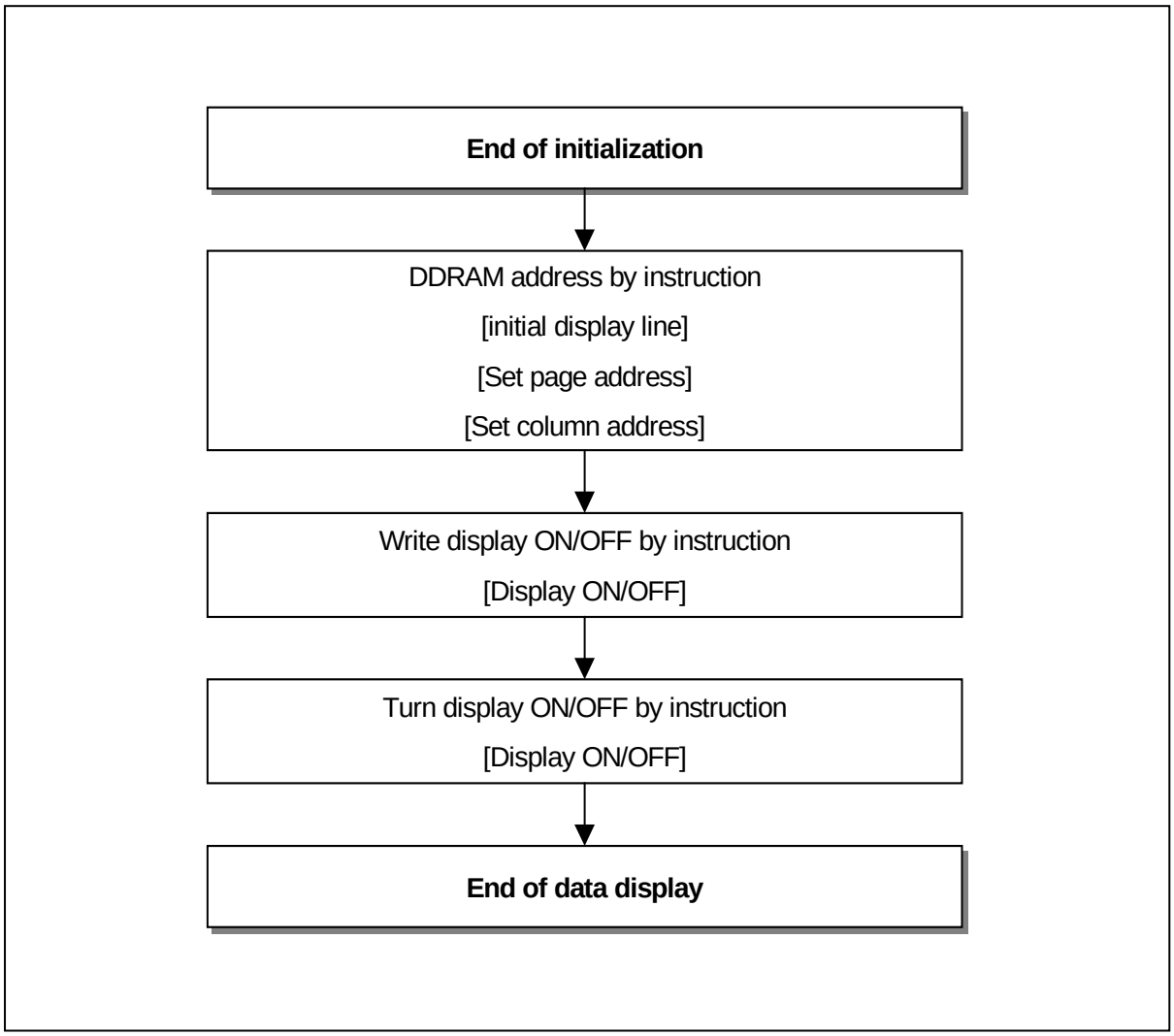

Figure 6-8. Data display

Referential instruction setup flow (4)

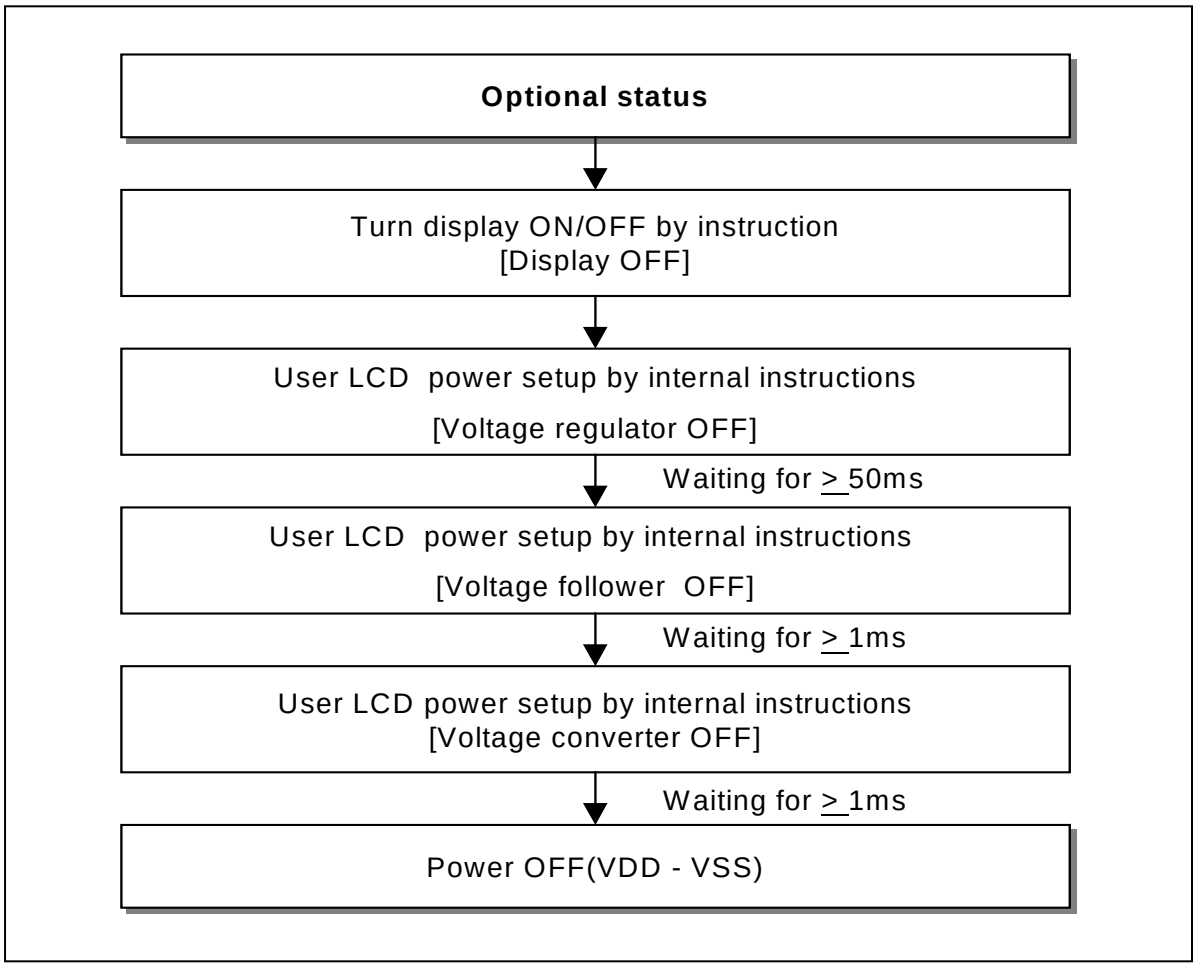

Figure 6-9. Power off.

7. SPECIFICATIONS

7-1. Absolute maximum ratings

Table 7-1. Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	
Input voltage range	V_{IN}	-0.3 to V_{DD} +0.3	
Operating temperature range	T_{OPR}	-40 to +85	^{o}C
Storage temperature range	T_{STR}	-55 to +125	

Notes:

1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥V1≥V2≥V3≥V4≥VSS(GND) must always be satisfied.(VLCD = V0 - VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

7-2. DC Characteristics

Table 7-2. DC characteristics (VSS = 0V, VDD = 2.4V to 3.6V, Ta = -40 to +85°C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Pin Used
Operating voltage(1)		VDD		2.4	-	3.6	V	VDD *1
Operating voltage(2)		V0		4.5	-	15.0		V0 *2
Input voltage	High	VIH		0.8VDD	-	VDD		*3
	Low	VIL		VSS	-	0.2VDD		
Output voltage	High	VOH	IOH=-0.5mA	0.8VDD	-	VDD		*4
	Low	VOL	IOL=0.5mA	VSS	-	0.2VDD		
Input leakage current		IIL	VIN=VDD or VSS	-1.0	-	+1.0	μA	*5
Output leakage current		IOZ	VIN=VDD or VSS	-3.0	-	+3.0		*6
LCD driver ON resistance		RON	Ta = 25 °C V0 = 8V	-	2.0	3.0	KΩ	SEGn COMn *7
Oscillator frequency	Internal	**f**OSC	Ta = 25 °C Duty ratio = 1/65	32.7	43.6	54.5	KHz	CL*8
	External	**f**CL		4.09	5.45	6.81		
Voltage converter input voltage		VCI	x 2	2.4	-	3.6	V	VCI
			x 3	2.4		3.6		
			x 4	2.4		3.6		
			x 5	2.4		3.2		
Voltage converter output voltage		V_{OUT}	x 2 / x 3 / x 4 / x 5 voltage conversion (no-load)	95	99	-	%	V_{OUT}
Voltage regulator operating voltage		V_{OUT}	-	6.0	-	16.0	V	V_{OUT}
Voltage follower operating voltage		V0	-	4.5	-	15.0		V0*9
Reference voltage		VREF	Ta = 25 °C -0.05%/ °C	2.04	2.1	2.16		*10

Table 7-2. DC Characteristics (Continued) (VSS = 0V, VDD = 2.4V to 3.6V, Ta = -40 to +85°C)

Item	Symbol	Condition	Min	Typ	Max	Unit	Pin Used
Dynamic current consumption (1): Built-in circuit OFF (At operating mode)							
Dynamic current consumption (1)	IDD1	VDD = 3.0V, V0 – VSS= 11.0V, 1/65 duty ratio, display OFF	-	15	23	μA	*11
Dynamic Current Consumption (2): Built-in circuit ON (At operating mode)							
Dynamic current consumption (2)	IDD2	VDD = 3.0V, (VCI=VDD,4times boosting) V0 – VSS= 11.0V, 1/65 duty ratio, display OFF, normal power mode	-	100	150	μA	*12
		VDD = 3.0V, (VCI=VDD, 4 times boosting) V0 – VSS= 11.0V, 1/65 duty ratio, display (check pattern) normal power mode	-	150	200	μA	*12
Current consumption during power save mode							
Sleep mode current	IDDS1	During sleep	-	-	2.0	μA	
Standby mode current	IDDS2	During standby		10.0	-	μA	

Table 7-3. The relationship between oscillation frequency and frame frequency

Duty ratio	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator circuit is used	f_{OSC} / 8	f_{OSC} / (2 x 8 x 65)
	External clock is used	External Input(f_{CL})	f_{CL} / (2 x 65)
1/55	On-chip oscillator circuit is used	Fosc / 9	Fosc / (2 x 9 x 55)
	External clock is used	External input (f_{CL})	f_{CL} / (2 x 55)
1/49	On-chip oscillator circuit is used	f_{OSC} / 10	f_{OSC} / (2 x 10 x 49)
	External clock is used	External Input (f_{CL})	f_{CL} / (2 x 49)
1/33	On-chip oscillator circuit is used	f_{OSC} / 15	f_{OSC} / (2 x 15 x 33)
	External clock is used	External Input (f_{CL})	f_{CL} / (2 x 33)

*(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: LCD AC signal frequency)

<* Remark solves>

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU
*2. In case of external power supply is applied.
*3. /CS1, CS2, RS, DB7 to DB0, E_/RD, RW_/RW, /RESET, MS, C68, PS, INTRS, /HPM, CLS, CL, M, DISP pins.
*4. DB0 to DB7, M, FR, FRS, DISP, CL pin.
*5. /CS1, CS2, RS, DB7 to DB0, E_/RD, RW_/WR, /RESET, MS, C68, PS, INTRS, /HPM, CLS, CL, M, DISP pins.
*6. Applies when then DB7 to DB0, M, FR, FRS, DISP, and CL, pins are in high impedance.
*7. Resistance value when ±0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON = ΔV / 0.1[kΩ] (ΔV :Voltage change when ±0.1[mA]is applied in the on status)
*8. See table 7-3 for the relationship between oscillation frequency and frame frequency.
*9. The Voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11, 12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built -in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD penal capacity, wiring capacity, etc.

7-3. AC CHARACTERISTICS

a. Read / write characteristics (8080-series MPU)

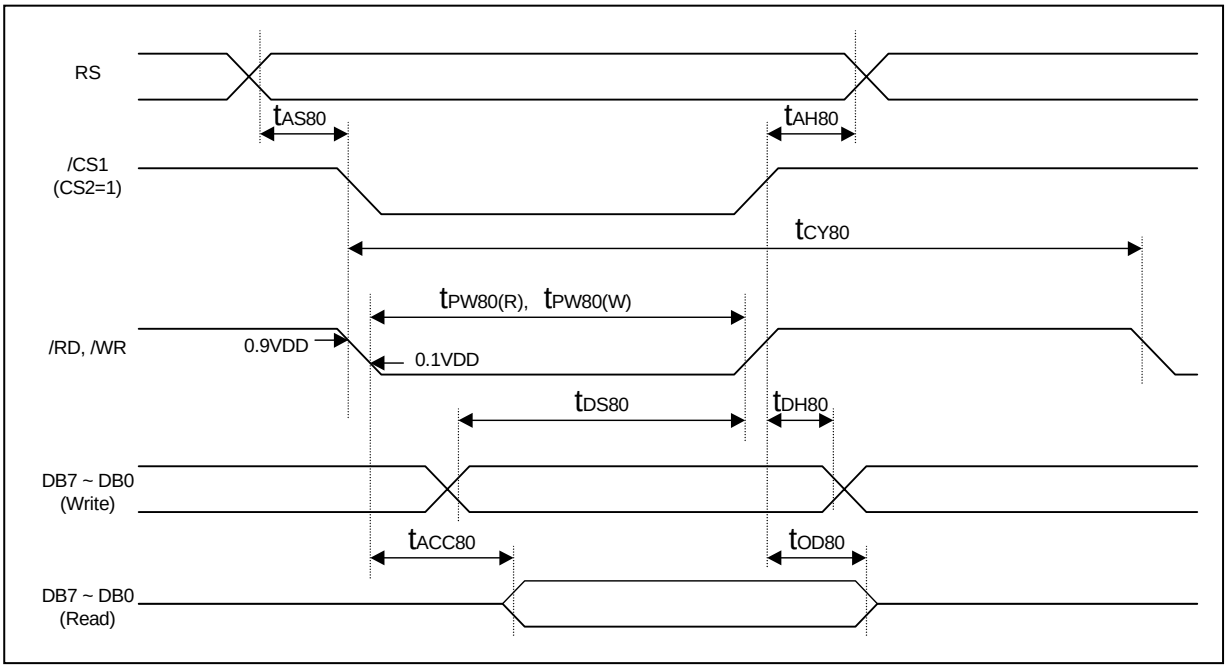

Figure 7-4. Read / write timing chart (8080-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time	RS	t_{CY80}	300	-	-	ns	
Pulse width(/WR)	RW-/WR	$t_{PW80\ (W)}$	60	-	-	ns	
Pulse width(/RD)	E-/RD	$t_{PW80\ (R)}$	60	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	140 100	ns	CL = 100pF

b. Read / write characteristics (6800-series MPU)

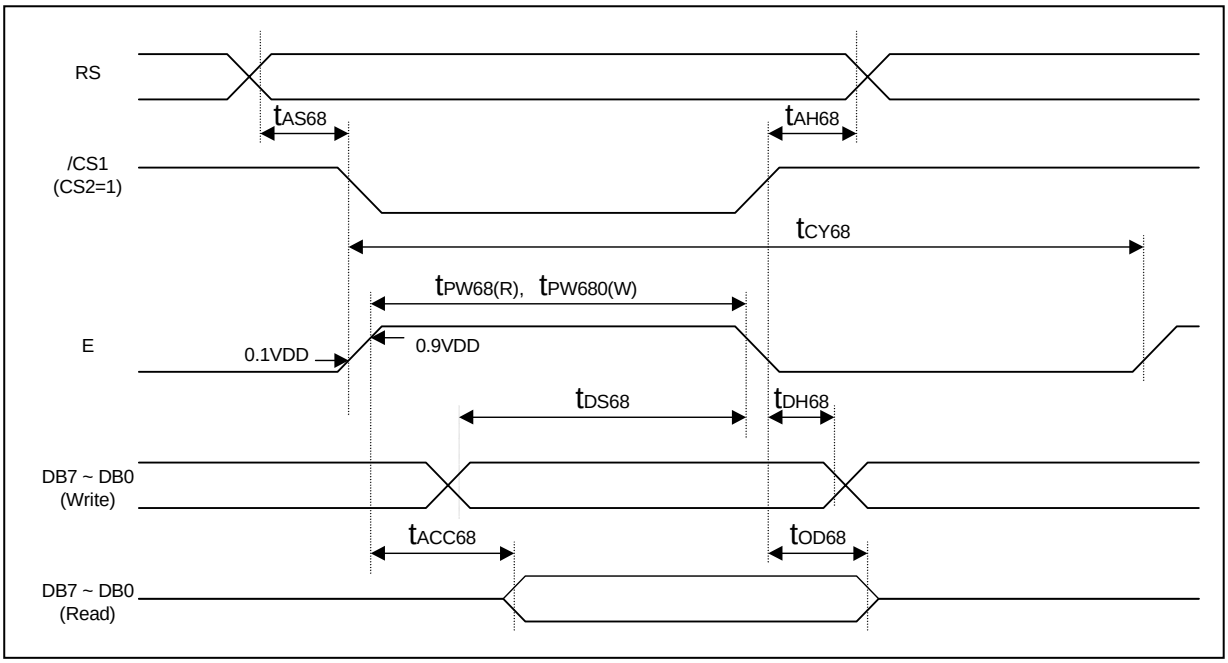

Figure 7-5. Read / write timing chart (6800-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	t_{AS68} t_{AH68}	0 0	-	-	ns	
System cycle time		RS	t_{CY68}	300	-	-	ns	
Enable pulse width	Read Write	E_/RD	t_{PW68} (R) t_{PW68} (W)	120 60	-	-	ns	
Data setup time Data hold time		DB7 to DB0	t_{DS68} t_{DH68}	40 15	-	-	ns	
Access time Output disable time			t_{ACC68} t_{OD68}	- 10	-	140 100	ns	CL = 100pF

c. Serial interface characteristics

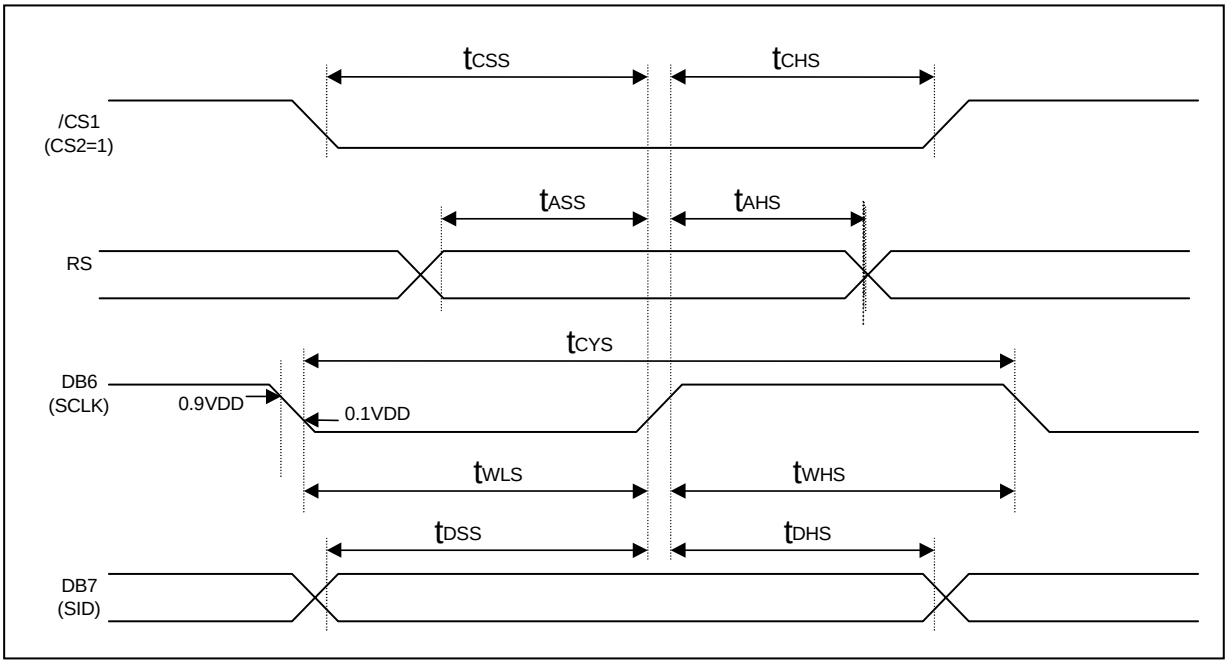

Figure 7-6. Serial interface characteristics

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYC} t_{WHS} t_{WLS}	250 100 100	-	-	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	150 150	-	-	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	100 100	-	-	ns	
/CS1 set up time /CS1 hold time	/CS1	t_{CSS} t_{CHS}	150 150	-	-	ns	

d. Reset input timing

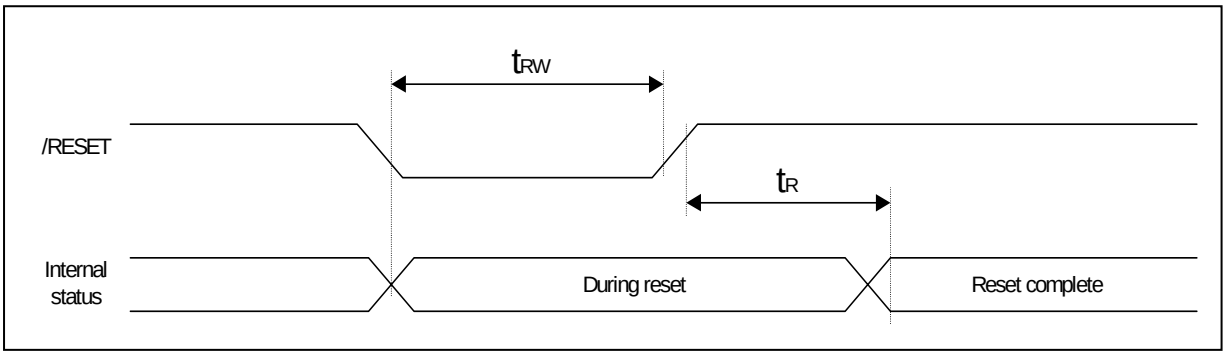

Figure 7-7. Reset input timing

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	/RESET	t_{RW}	1.0	-	-	μs	
Reset time	-	t_R	-	-	1.0	μs	

e. Display control output timing

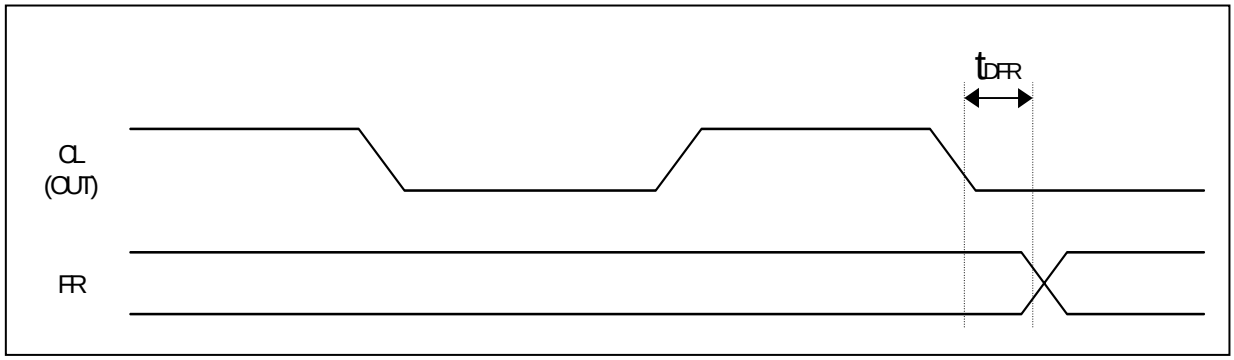

Figure 7-8. Display control output timing

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	C_L = 50 pF

8. REFERENCE APPLICATION

8-1. Microprocessor interface

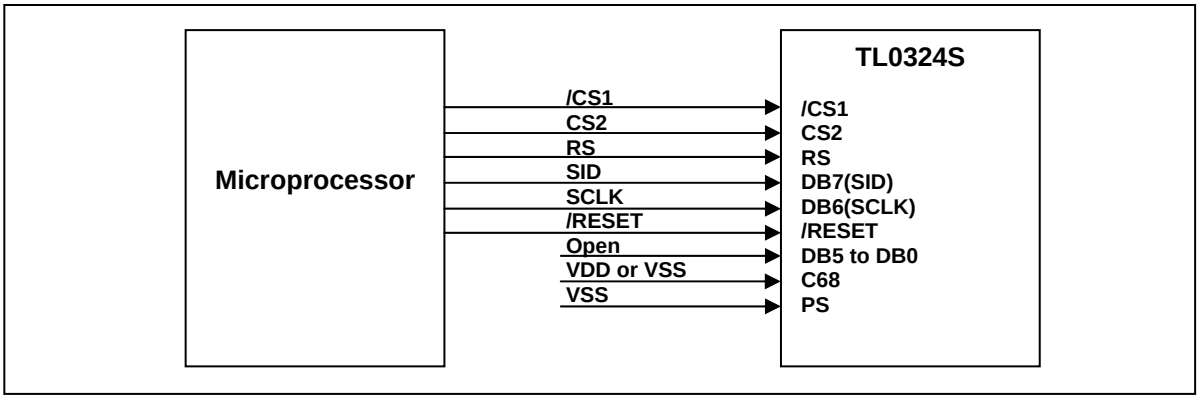

Figure 8-1. Serial Interface (PS = "L", C68 = " H or L", E_/RD = "H or L", RW_/WR = "H or L")

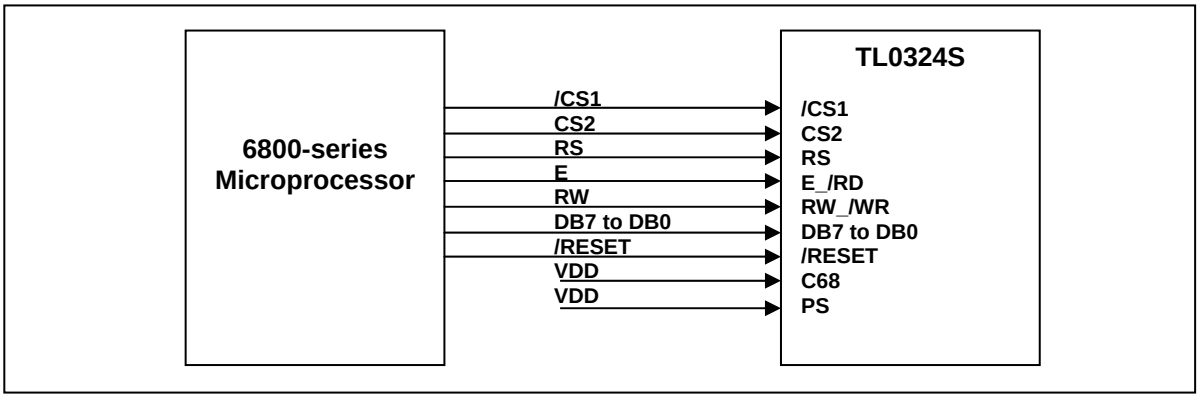

Figure 8-2. 6800-series MPU Interface (PS = "H", C68 = " H")

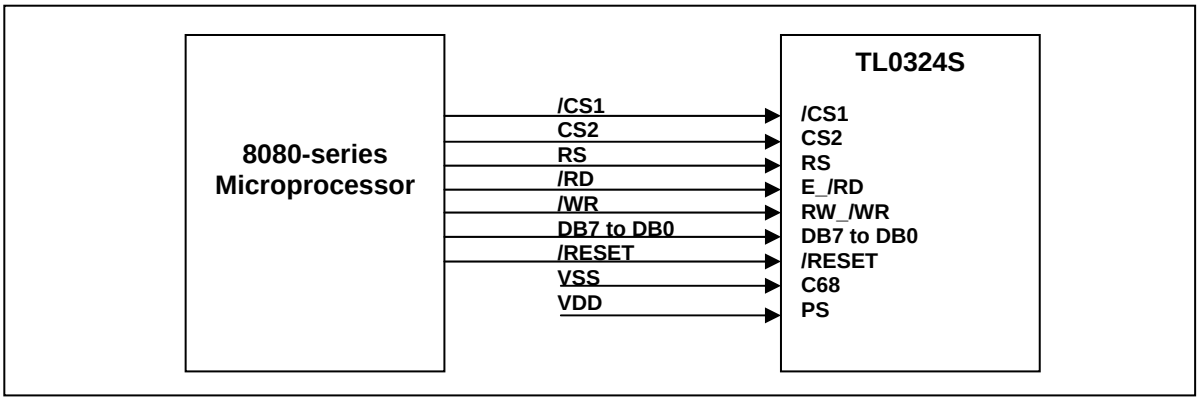

Figure 8-3. 8080-series MPU Interface (PS = "H", C68 = " L")

8-2. CONNECTIONS BETWEEN TL0324S AND LCD PANEL

a. Single chip configuration (1/65 duty configurations)

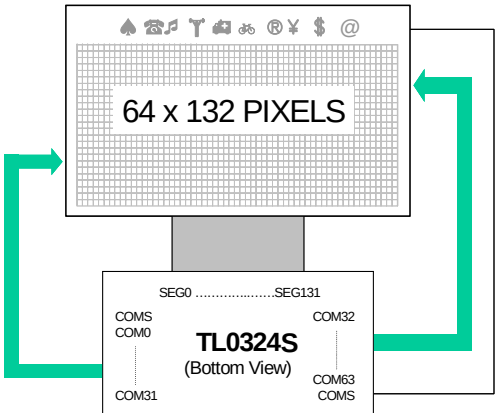

Figure 8-4. SHL = 1, ADC = 0

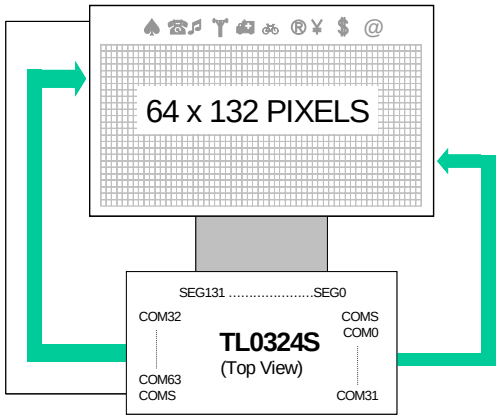

Figure 8-5. SHL = 1, ADC = 1

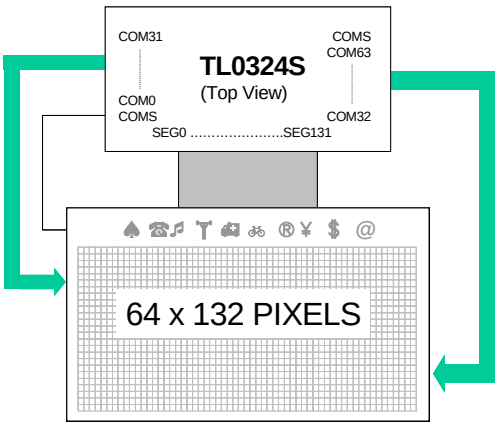

Figure 8-6. SHL = 0, ADC = 0

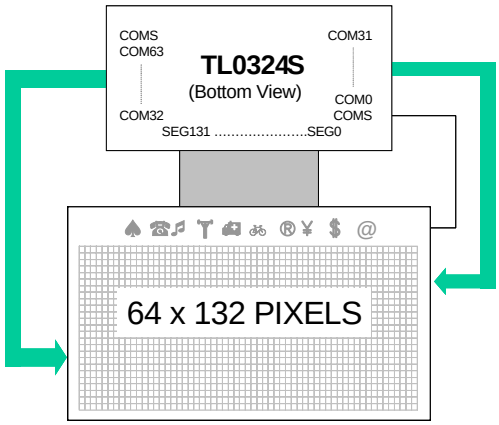

Figure 8-7. SHL = 0, ADC = 1

b. Single chip configuration (1/55 duty configurations)

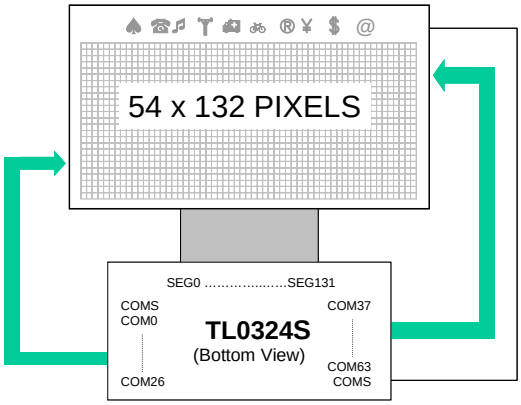

Figure 8-8. SHL = 1, ADC = 0

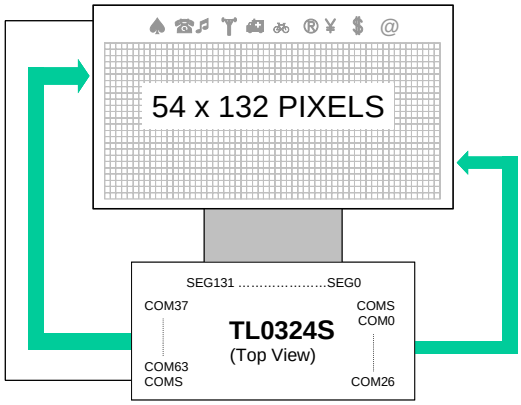

Figure 8-9. SHL = 1, ADC = 1

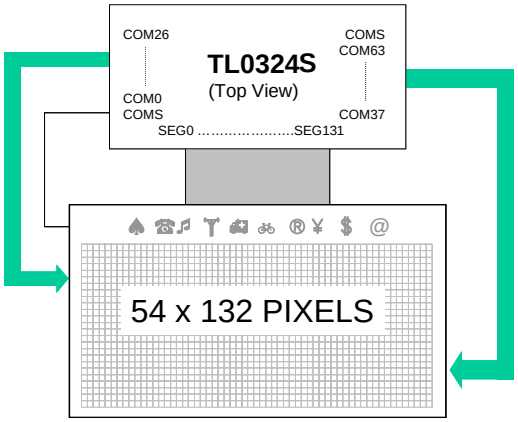

Figure 8-10. SHL = 0, ADC = 0

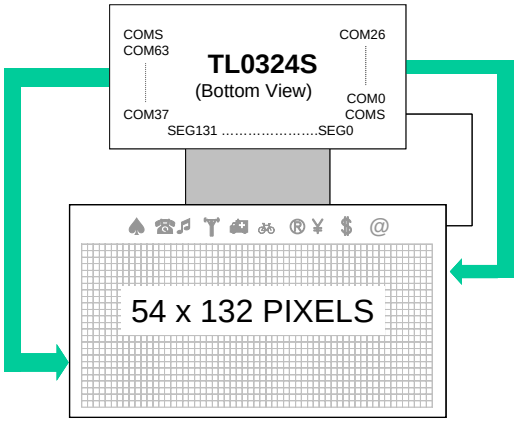

Figure 8-11. SHL = 0, ADC = 1

c. Single chip configuration (1/49 duty configurations)

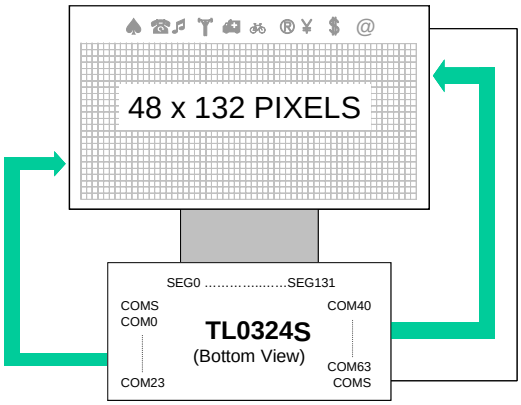

Figure 8-12. SHL = 1, ADC = 0

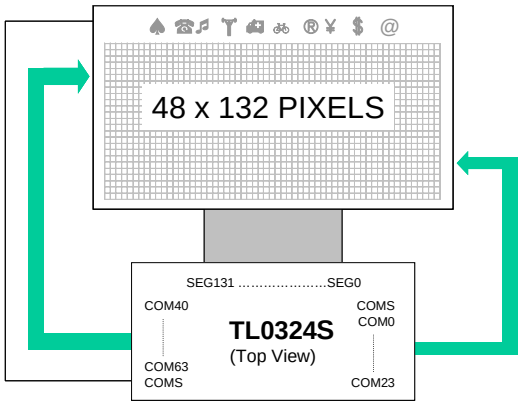

Figure 8-13. SHL = 1, ADC = 1

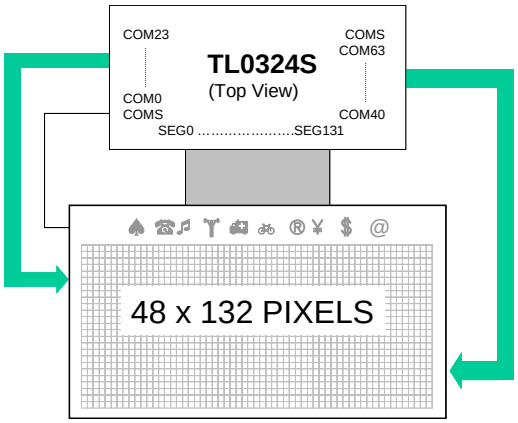

Figure 8-14. SHL = 0, ADC = 0

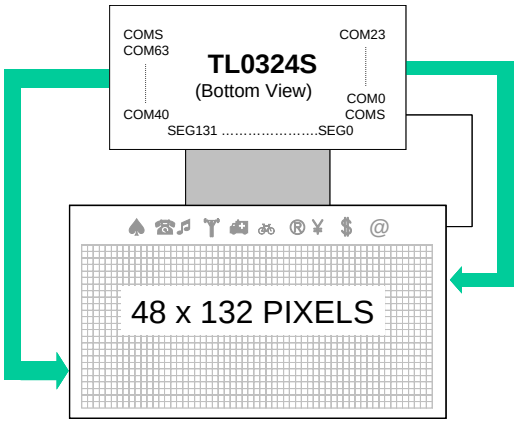

Figure 8-15. SHL = 0, ADC = 1

d. Single chip configuration (1/33 duty configurations)

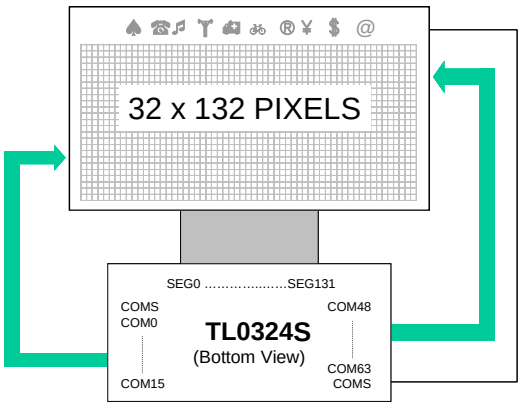

Figure 8-16. SHL = 1, ADC = 0

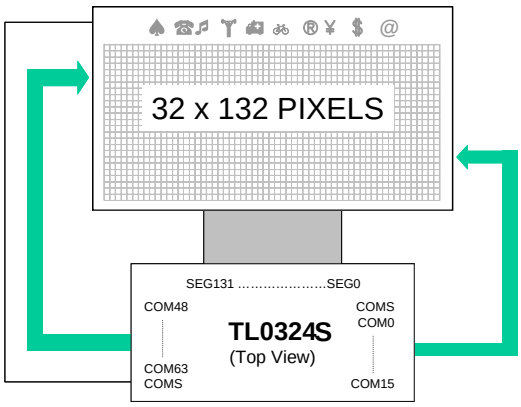

Figure 8-17. SHL = 1, ADC = 1

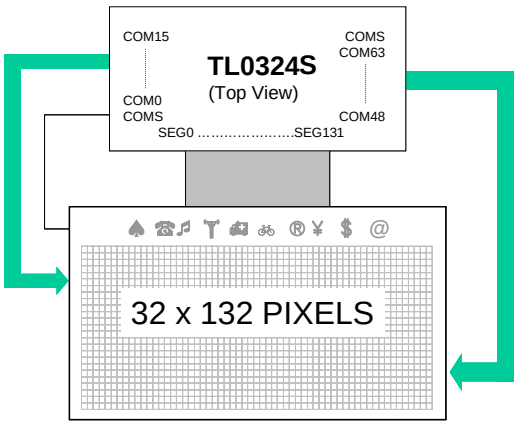

Figure 8-18. SHL = 0, ADC = 0

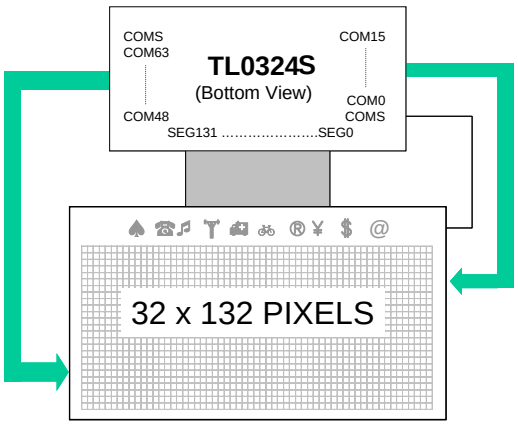

Figure 8-19. SHL = 0, ADC = 1

e. Multiple chip configuration

- 65COM (64COM + 1COMS) x 264SEG (132SEG x 2)

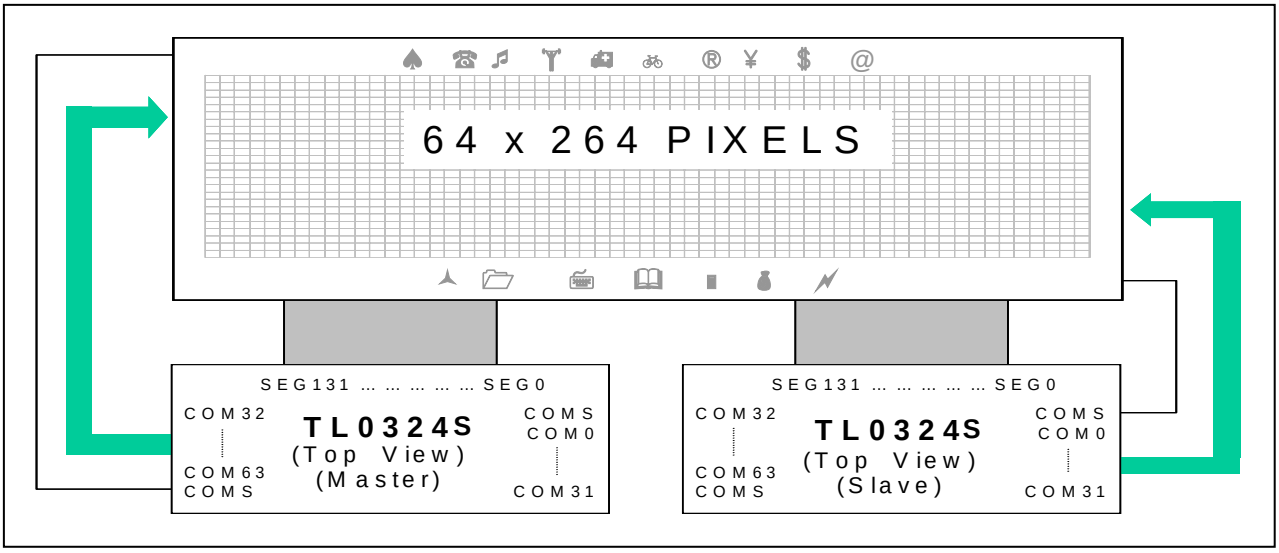

Figure 8-20. SHL = 1, ADC = 1

***.** Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

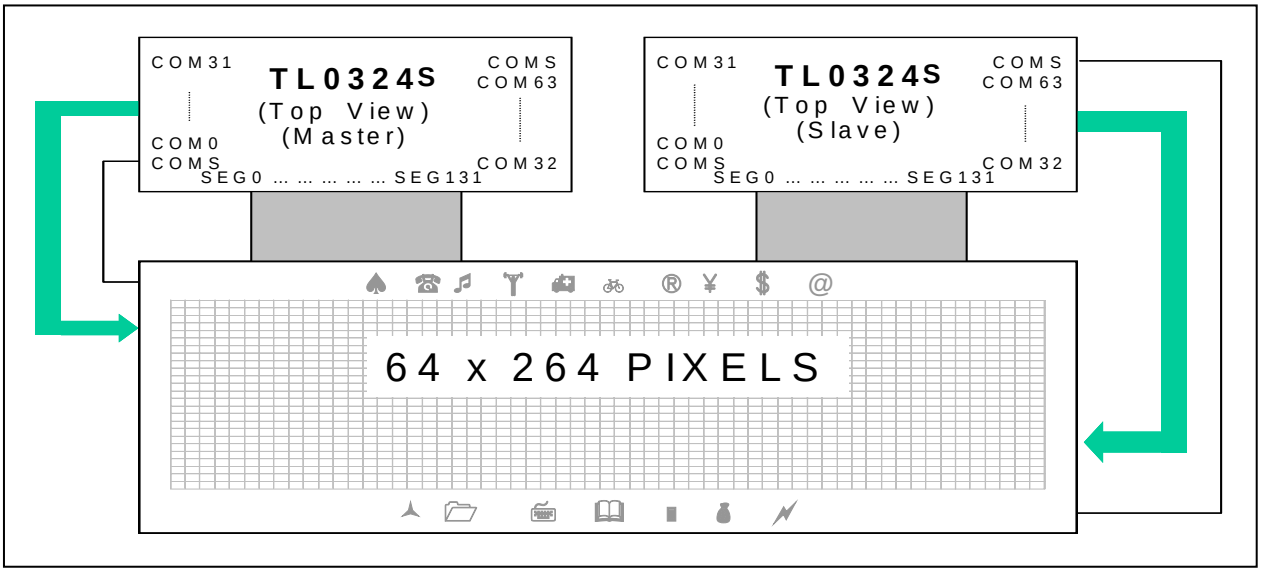

Figure 8-21. SHL = 0, ADC = 0

*. Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

- **130COM (128COM + 2COMS) x 132SEG**

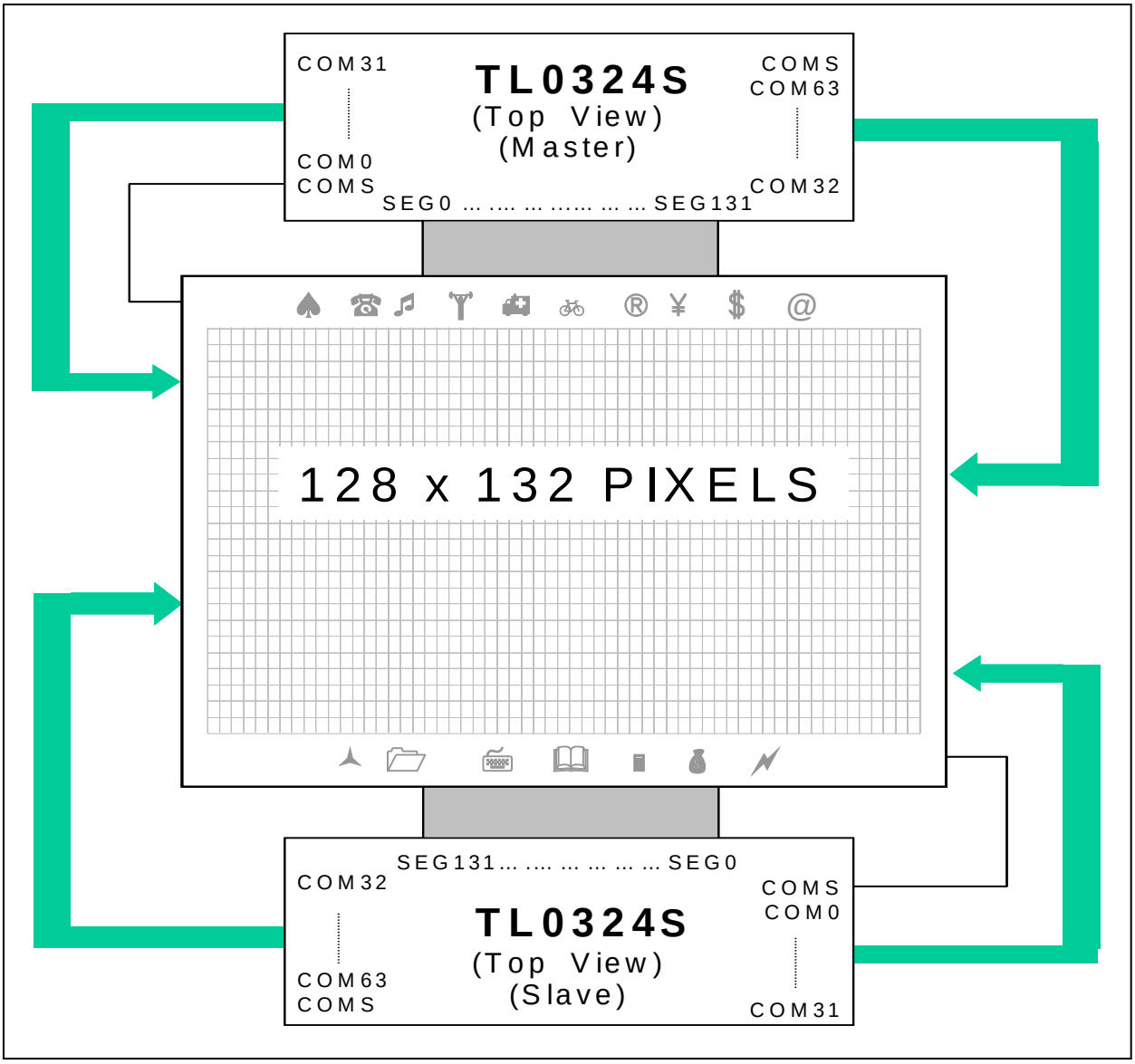

Figure 8-22. 130COM (128COM + 2COMS) x 132SEG

***.** Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

***.** Common / Segment output direction select
- Master chip: SHL = 0, ADC = 0
- Slave chip: SHL = 1, ADC = 1

8-3. TCP Pin lay out (sample)

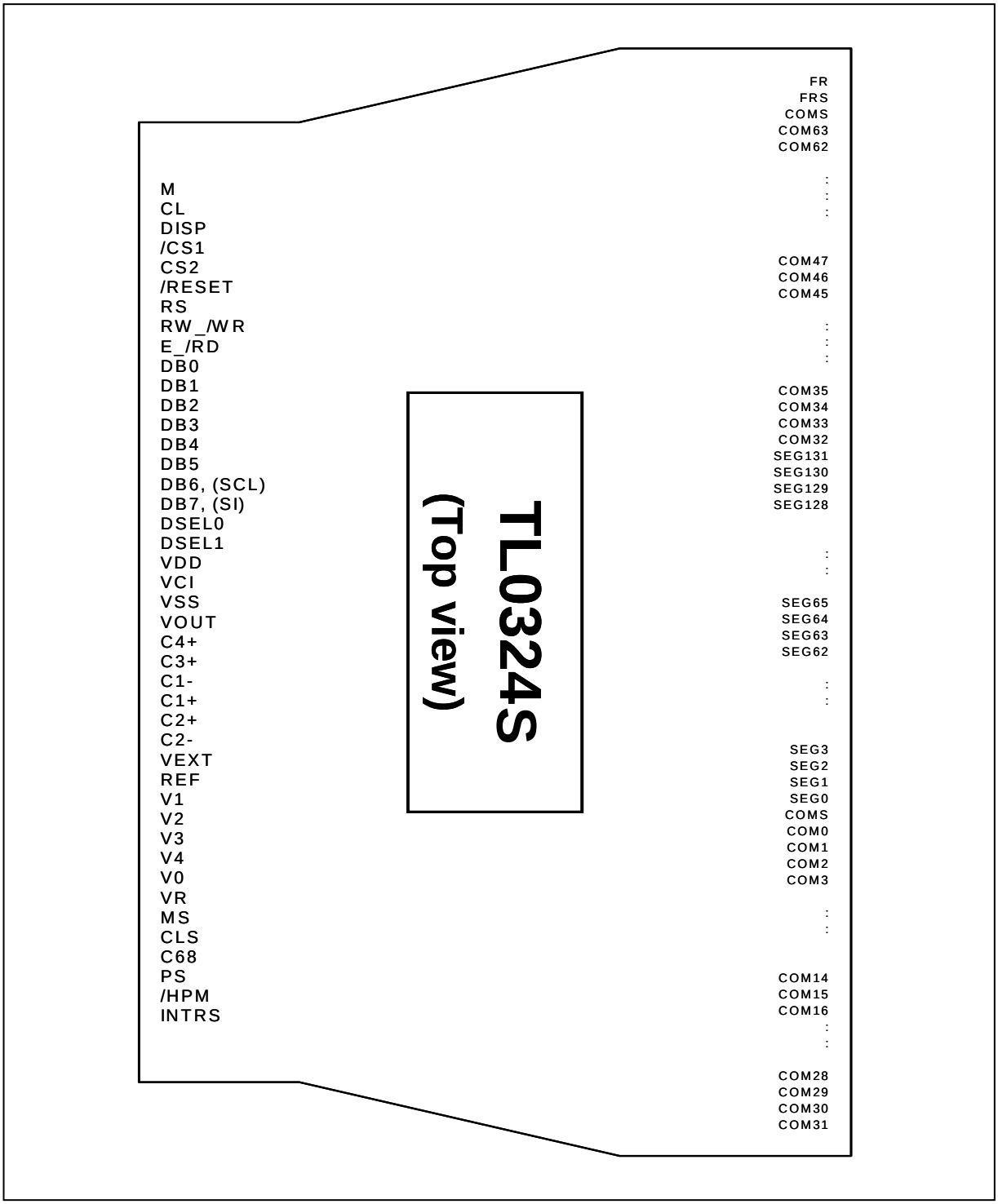

Figure 8-23. TCP pin layout

8-4. Application circuit for serial

-. Package type: TCP
-. Device mode: Master mode, Internal OSC, normal mode, 4-times boost-up, internal resistor

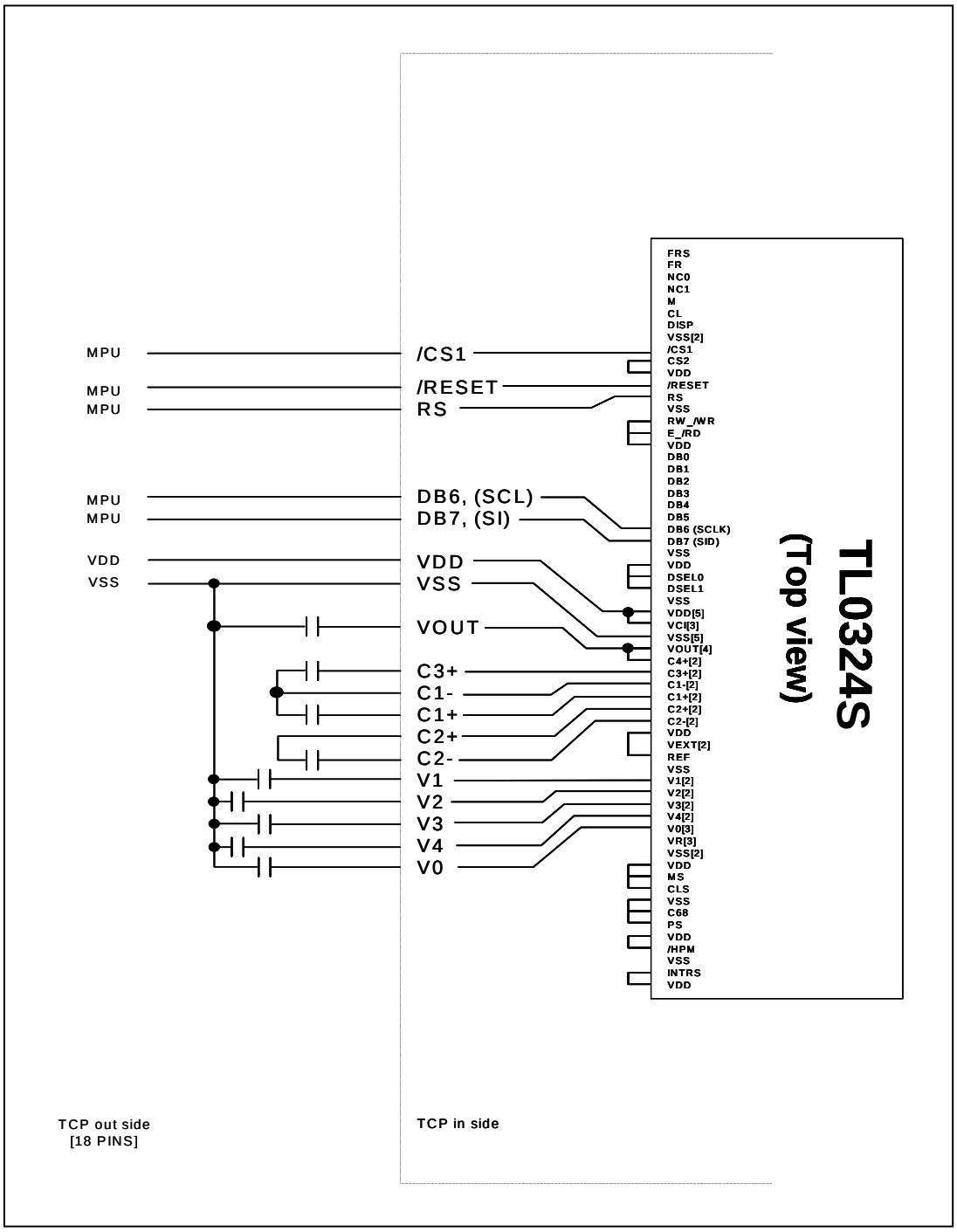

Figure 8-24. TL0324S Application circuit for serial

9. PAD CONFIGURATION

Figure 9.1 Chip pad configuration (TOP View)

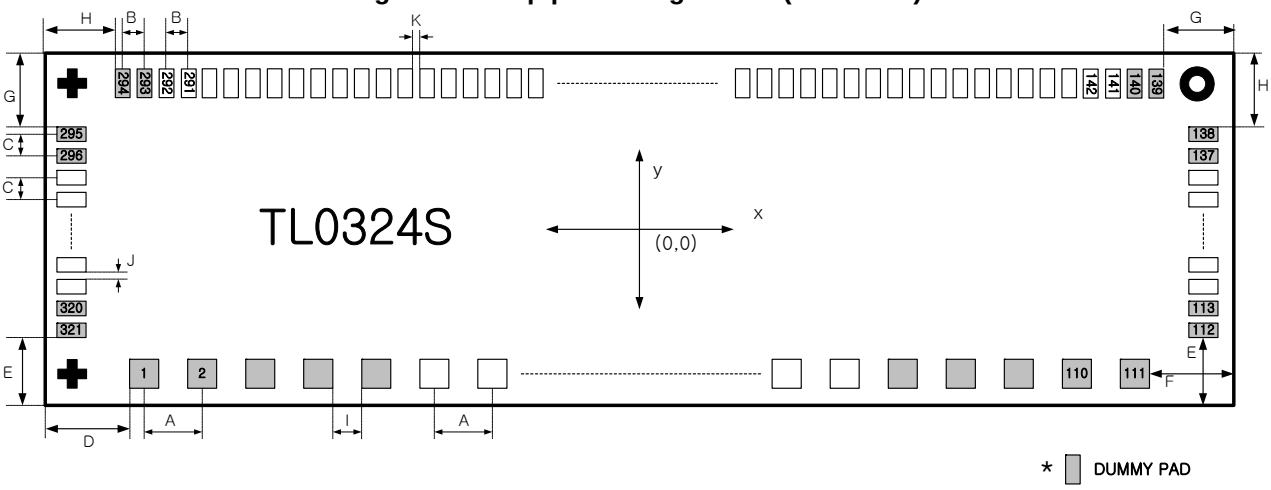

Table 9-1. Pad Dimensions

Item	Pad No.		Size X	Size Y	Unit
Chip Size (without S/L)			8550	1900	um
Pad Pitch	Input		70		
	Output		52, 55		
	Dummy	input	70		
		output	52, 55		
Bumped pad size	1~111		44	72	
	112~138, 295~321		78	34	
	139~294		34	78	
Bumped pad height	18 ± 3um				

Chip Outline Dimensions <Basis of Bump PAD> [unit : um]

SYMBOL	DIMENSION	SYMBOL	DIMENSION	SYMBOL	DIMENSION
A	**70**	**B**	**52**	**C**	**55**
D	**410.3**	**E**	**224.3**	**F**	**395.7**
G	**211.7**	**H**	**228**	**I**	**26**
J	**21**	**K**	**18**	**L**	

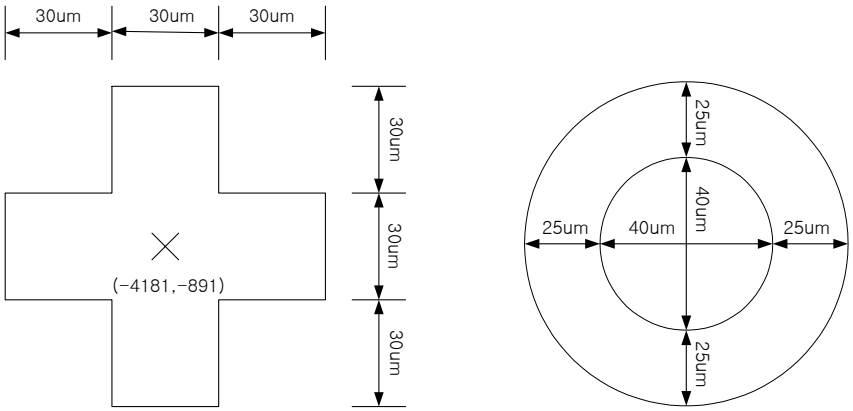

Figure 9-2. COG align key

9-2. PAD CENTER COORDINATES

Table 9-1 Pad Center Coordinates [Unit : um]

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
1	DUMMY1	-3842.7	-891	36	VDD	-1392.7	-891	71	C1M	1057.3	-891
2	DUMMY2	-3772.7	-891	37	VDD	-1322.7	-891	72	C1M	1127.3	-891
3	DUMMY3	-3702.7	-891	38	VDD	-1252.7	-891	73	C1P	1197.3	-891
4	DUMMY4	-3632.7	-891	39	VCI	-1182.7	-891	74	C1P	1267.3	-891
5	DUMMY5	-3562.7	-891	40	VCI	-1112.7	-891	75	C2P	1337.3	-891
6	FRS	-3492.7	-891	41	VCI	-1042.7	-891	76	C2P	1407.3	-891
7	FR	-3422.7	-891	42	VCI	-972.7	-891	77	C2M	1477.3	-891
8	M	-3352.7	-891	43	VSS	-902.7	-891	78	C2M	1547.3	-891
9	CL	-3282.7	-891	44	VSS	-832.7	-891	79	VDD	1617.3	-891
10	DISP	-3212.7	-891	45	VSS	-762.7	-891	80	VEXT	1687.3	-891
11	VSS	-3142.7	-891	46	VSS	-692.7	-891	81	REF	1757.3	-891
12	VSS	-3072.7	-891	47	VSS	-622.7	-891	82	VSS	1827.3	-891
13	/CS1	-3002.7	-891	48	TEST0	-552.7	-891	83	V1	1897.3	-891
14	CS2	-2932.7	-891	49	TEST1	-482.7	-891	84	V1	1967.3	-891
15	VDD	-2862.7	-891	50	TEST2	-412.7	-891	85	V2	2037.3	-891
16	/RESET	-2792.7	-891	51	TEST3	-342.7	-891	86	V2	2107.3	-891
17	RS	-2722.7	-891	52	TEST4	-272.7	-891	87	V3	2177.3	-891
18	VSS	-2652.7	-891	53	TEST5	-202.7	-891	88	V3	2247.3	-891
19	RW_/WR	-2582.7	-891	54	TEST6	-132.7	-891	89	V4	2317.3	-891
20	E_/RD	-2512.7	-891	55	TEST7	-62.7	-891	90	V4	2387.3	-891
21	VDD	-2442.7	-891	56	TEST8	7.3	-891	91	V0	2457.3	-891
22	DB0	-2372.7	-891	57	TEST9	77.3	-891	92	V0	2527.3	-891
23	DB1	-2302.7	-891	58	TEST10	147.3	-891	93	VR	2597.3	-891
24	DB2	-2232.7	-891	59	TEST11	217.3	-891	94	VR	2667.3	-891
25	DB3	-2162.7	-891	60	TEST12	287.3	-891	95	VSS	2737.3	-891
26	DB4	-2092.7	-891	61	TEST13	357.3	-891	96	VDD	2807.3	-891
27	DB5	-2022.7	-891	62	TEST14	427.3	-891	97	MS	2877.3	-891
28	DB6	-1952.7	-891	63	V_{OUT}	497.3	-891	98	CLS	2947.3	-891
29	DB7	-1882.7	-891	64	V_{OUT}	567.3	-891	99	VSS	3017.3	-891
30	VSS	-1812.7	-891	65	V_{OUT}	637.3	-891	100	C68	3087.3	-891
31	VDD	-1742.7	-891	66	V_{OUT}	707.3	-891	101	PS	3157.3	-891
32	DSEL0	-1672.7	-891	67	C4P	777.3	-891	102	VDD	3227.3	-891
33	DSEL1	-1602.7	-891	68	C4P	847.3	-891	103	/HPM	3297.3	-891
34	VSS	-1532.7	-891	69	C3P	917.3	-891	104	VSS	3367.3	-891
35	VDD	-1462.7	-891	70	C3P	987.3	-891	105	INTRS	3437.3	-891

Table 9-1 Pad Center Coordinates (Continued)

[Unit : um]

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
106	VDD	3507.3	-891	141	COM8	3926	856	176	SEG25	2106	856
107	DUMMY6	3577.3	-891	142	COM7	3874	856	177	SEG26	2054	856
108	DUMMY7	3647.3	-891	143	COM6	3822	856	178	SEG27	2002	856
109	DUMMY8	3717.3	-891	144	COM5	3770	856	179	SEG28	1950	856
110	DUMMY9	3787.3	-891	145	COM4	3718	856	180	SEG29	1898	856
111	DUMMY10	3857.3	-891	146	COM3	3666	856	181	SEG30	1846	856
112	DUMMY11	4181	-708.7	147	COM2	3614	856	182	SEG31	1794	856
113	DUMMY12	4181	-653.7	148	COM1	3562	856	183	SEG32	1742	856
114	COM31	4181	-598.7	149	COM0	3510	856	184	SEG33	1690	856
115	COM30	4181	-543.7	150	COMS0	3458	856	185	SEG34	1638	856
116	COM29	4181	-488.7	151	SEG0	3406	856	186	SEG35	1586	856
117	COM28	4181	-433.7	152	SEG1	3354	856	187	SEG36	1534	856
118	COM27	4181	-378.7	153	SEG2	3302	856	188	SEG37	1482	856
119	COM26	4181	-323.7	154	SEG3	3250	856	189	SEG38	1430	856
120	COM25	4181	-268.7	155	SEG4	3198	856	190	SEG39	1378	856
121	COM24	4181	-213.7	156	SEG5	3146	856	191	SEG40	1326	856
122	COM23	4181	-158.7	157	SEG6	3094	856	192	SEG41	1274	856
123	COM22	4181	-103.7	158	SEG7	3042	856	193	SEG42	1222	856
124	COM21	4181	-48.7	159	SEG8	2990	856	194	SEG43	1170	856
125	COM20	4181	6.3	160	SEG9	2938	856	195	SEG44	1118	856
126	COM19	4181	61.3	161	SEG10	2886	856	196	SEG45	1066	856
127	COM18	4181	116.3	162	SEG11	2834	856	197	SEG46	1014	856
128	COM17	4181	171.3	163	SEG12	2782	856	198	SEG47	962	856
129	COM16	4181	226.3	164	SEG13	2730	856	199	SEG48	910	856
130	COM15	4181	281.3	165	SEG14	2678	856	200	SEG49	858	856
131	COM14	4181	336.3	166	SEG15	2626	856	201	SEG50	806	856
132	COM13	4181	391.3	167	SEG16	2574	856	202	SEG51	754	856
133	COM12	4181	446.3	168	SEG17	2522	856	203	SEG52	702	856
134	COM11	4181	501.3	169	SEG18	2470	856	204	SEG53	650	856
135	COM10	4181	556.3	170	SEG19	2418	856	205	SEG54	598	856
136	COM9	4181	611.3	171	SEG20	2366	856	206	SEG55	546	856
137	DUMMY13	4181	666.3	172	SEG21	2314	856	207	SEG56	494	856
138	DUMMY14	4181	721.3	173	SEG22	2262	856	208	SEG57	442	856
139	DUMMY15	4030	856	174	SEG23	2210	856	209	SEG58	390	856
140	DUMMY16	3978	856	175	SEG24	2158	856	210	SEG59	338	856

Table 9-1 Pad Center Coordinates (Continued)

[Unit : um]

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
211	SEG60	286	856	246	SEG95	-1534	856	281	SEG130	-3354	856
212	SEG61	234	856	247	SEG96	-1586	856	282	SEG131	-3406	856
213	SEG62	182	856	248	SEG97	-1638	856	283	COM32	-3458	856
214	SEG63	130	856	249	SEG98	-1690	856	284	COM33	-3510	856
215	SEG64	78	856	250	SEG99	-1742	856	285	COM34	-3562	856
216	SEG65	26	856	251	SEG100	-1794	856	286	COM35	-3614	856
217	SEG66	-26	856	252	SEG101	-1846	856	287	COM36	-3666	856
218	SEG67	-78	856	253	SEG102	-1898	856	288	COM37	-3718	856
219	SEG68	-130	856	254	SEG103	-1950	856	289	COM38	-3770	856
220	SEG69	-182	856	255	SEG104	-2002	856	290	COM39	-3822	856
221	SEG70	-234	856	256	SEG105	-2054	856	291	COM40	-3874	856
222	SEG71	-286	856	257	SEG106	-2106	856	292	COM41	-3926	856
223	SEG72	-338	856	258	SEG107	-2158	856	293	DUMMY17	-3978	856
224	SEG73	-390	856	259	SEG108	-2210	856	294	DUMMY18	-4030	856
225	SEG74	-442	856	260	SEG109	-2262	856	295	DUMMY19	-4181	721.3
226	SEG75	-494	856	261	SEG110	-2314	856	296	DUMMY20	-4181	666.3
227	SEG76	-546	856	262	SEG111	-2366	856	297	COM42	-4181	611.3
228	SEG77	-598	856	263	SEG112	-2418	856	298	COM43	-4181	556.3
229	SEG78	-650	856	264	SEG113	-2470	856	299	COM44	-4181	501.3
230	SEG79	-702	856	265	SEG114	-2522	856	300	COM45	-4181	446.3
231	SEG80	-754	856	266	SEG115	-2574	856	301	COM46	-4181	391.3
232	SEG81	-806	856	267	SEG116	-2626	856	302	COM47	-4181	336.3
233	SEG82	-858	856	268	SEG117	-2678	856	303	COM48	-4181	281.3
234	SEG83	-910	856	269	SEG118	-2730	856	304	COM49	-4181	226.3
235	SEG84	-962	856	270	SEG119	-2782	856	305	COM50	-4181	171.3
236	SEG85	-1014	856	271	SEG120	-2834	856	306	COM51	-4181	116.3
237	SEG86	-1066	856	272	SEG121	-2886	856	307	COM52	-4181	61.3
238	SEG87	-1118	856	273	SEG122	-2938	856	308	COM53	-4181	6.3
239	SEG88	-1170	856	274	SEG123	-2990	856	309	COM54	-4181	-48.7
240	SEG89	-1222	856	275	SEG124	-3042	856	310	COM55	-4181	-103.7
241	SEG90	-1274	856	276	SEG125	-3094	856	311	COM56	-4181	-158.7
242	SEG91	-1326	856	277	SEG126	-3146	856	312	COM57	-4181	-213.7
243	SEG92	-1378	856	278	SEG127	-3198	856	313	COM58	-4181	-268.7
244	SEG93	-1430	856	279	SEG128	-3250	856	314	COM59	-4181	-323.7
245	SEG94	-1482	856	280	SEG129	-3302	856	315	COM60	-4181	-378.7

Table 9-1 Pad Center Coordinates (Continued)

[Unit : um]

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
316	COM61	-4181	-433.7								
317	COM62	-4181	-488.7								
318	COM63	-4181	-543.7								
319	COMS1	-4181	-598.7								
320	DUMMY21	-4181	-653.7								
321	DUMMY22	-4181	-708.7								
	COG Align KEY1	-4181	-891								
	COG Align KEY2	-4159.9	842.5								
	COG Align KEY3	4159.9	842.5								

TL0324S Specification revision history		
Version	Content	Date
0.0	1. Initial Version	Jun. 2002
0.1	1. pp.5, VSS Pin description VSS PAD numbers are changed from 41~45 to 43~47. 2. pp.63, 67, Coordinate of COG align key is added.	May 2003
0.2	1. Add COG align keys	April 2004