Sitronix

ST7592

396 x 132 Dot Matrix LCD Controller/Driver

INTRODUCTION

ST7592 is a single-chip LSI for graphic dot-matrix LCD systems. It incorporates power system, LCD controller and drivers for common/segment outputs. ST7592 can be connected directly to a microprocessor with 8-bit parallel interface or 4-line serial interface (SPI-4) or 3-line serial interface (SPI-3). Display data sent from MCU is stored into internal Display Data RAM (DDRAM) of 396x132 bits. ST7592 contains 396 segment-output and 132 common-output. The display data bits in DDRAM are directly related to the pixels on LCD panel. With built-in oscillation circuit and low power consumption power circuits, ST7592 can drive LCD panel without external clock or power, so that it is possible to make a display system with the fewest components and minimal power consumption.

FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

- 396 segment outputs / 132 common outputs

On-chip Display Data RAM

- Capacity: 396 x 132 = 52,272 bits

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MCU
- 4-Line (8-bit) and 3-Line (9-bit) serial interfaces support write-operation and register-read (status/temperature…)
- All interfaces can read temperature (when sensor is ON), IC status and PROM data (register value)

External RSTB (Hardware Reset) Pin

On-chip Oscillator Circuit

- Internal oscillator requires no external component (external clock input is also supported)

On-chip Low Power Analog Circuit

- V3 generator with built-in boost-capacitors
- Built-in voltage regulator with programmable contrast
- Built-in PROM (Programmable Read-Only Memory) to optimize Vop for LCD panel (3 times programmable)
- Built-in voltage follower for LCD bias voltages: 1/6 ~ 1/16
- Support external power supply

Display Function

- Display duty: 1/8 ~ 1/132 (in 4-line basis)
  Scan duty: 1/64 ~ 1/132 (in 4-line basis)
- Support interlace-scanning method
- N-lines inversion

Built-in Temperature Sensor

- Temperature compensation with built-in thermal sensor
- Programmable Vop thermal gradient (19 slopes) and frame frequencies in -40~87℃

Operating Voltage Range

- Digital Power (VDD1, VDD3): 3.3V ~ 5.0V (TYP.)
- Analog Power (VDD2): 3.3V ~ 5.0V (TYP.)

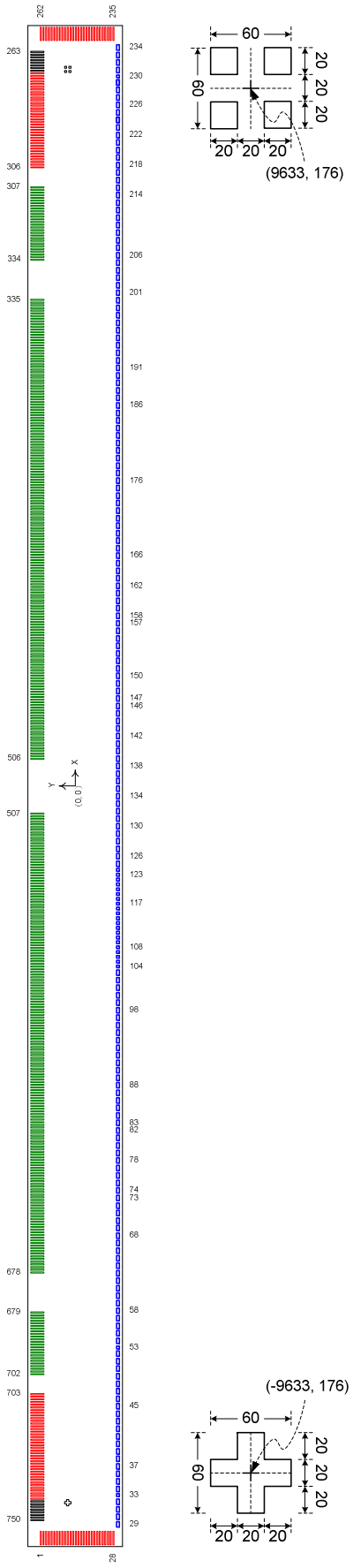
LCD Operating Voltage Range

- Maximum Vop: 25.0V (Vop=V3-MV3, i.e. V3=12.5V)

Package Type: COG & COF

ST7592-G2 **ST7592-G2-B1**	**6800, 8080, 4-Line & 3-Line Interface**	ST

PAD ARRANGEMENT



Chip Size: 20706 x 1276 (+/- 15) Unit: um

Chip Thickness	480	Bump Height	15
PAD		**Bump Size**	
1~28, 235~262		96 x 26	
29~32, 34~52, 54~103, 125~229, 231~234		80 x 45	
33, 53, 104~124, 230		30 x 45	
263~750		26 x 96	
PAD		**Minimal Pitch**	
1~28, 235~262, 263~750		40	
29~234		52.5	
* Refer to “PAD CENTER COORDINATES” for ITO layout			

PAD CENTER COORDINATES

PAD	NAME	X	Y
1	COM[27]	-10273.5	540
2	COM[26]	-10273.5	500
3	COM[25]	-10273.5	460
4	COM[24]	-10273.5	420
5	COM[23]	-10273.5	380
6	COM[22]	-10273.5	340
7	COM[21]	-10273.5	300
8	COM[20]	-10273.5	260
9	COM[19]	-10273.5	220
10	COM[18]	-10273.5	180
11	COM[17]	-10273.5	140
12	COM[16]	-10273.5	100
13	COM[15]	-10273.5	60
14	COM[14]	-10273.5	20
15	COM[13]	-10273.5	-20
16	COM[12]	-10273.5	-60
17	COM[11]	-10273.5	-100
18	COM[10]	-10273.5	-140
19	COM[9]	-10273.5	-180
20	COM[8]	-10273.5	-220
21	COM[7]	-10273.5	-260
22	COM[6]	-10273.5	-300
23	COM[5]	-10273.5	-340
24	COM[4]	-10273.5	-380
25	COM[3]	-10273.5	-420
26	COM[2]	-10273.5	-460
27	COM[1]	-10273.5	-500
28	COM[0]	-10273.5	-540
29	Dummy	-10132.5	-584
30	Dummy	-10027.5	-584
31	Dummy	-9922.5	-584
32	Dummy	-9817.5	-584
33	Dummy	-9738.75	-584
34	VPP	-9660	-584
35	VPP	-9555	-584
36	EXTB	-9450	-584
37	T19	-9345	-584
38	CL	-9240	-584
39	T18	-9135	-584
40	CSB	-9030	-584
41	RSTB	-8925	-584
42	A0	-8820	-584
43	RWR	-8715	-584
44	ERD	-8610	-584
45	D0	-8505	-584
46	D1	-8400	-584

PAD	NAME	X	Y
47	D2	-8295	-584
48	D3	-8190	-584
49	D4	-8085	-584
50	D5	-7980	-584
51	D6	-7875	-584
52	D7	-7770	-584
53	VSS1	-7691.25	-584
54	MODE	-7612.5	-584
55	CLS	-7507.5	-584
56	IF2	-7402.5	-584
57	IF1	-7297.5	-584
58	VDD2	-7192.5	-584
59	VDD2	-7087.5	-584
60	VDD2	-6982.5	-584
61	VDD2	-6877.5	-584
62	VDD2	-6772.5	-584
63	VDD2	-6667.5	-584
64	VDD2	-6562.5	-584
65	VDD2	-6457.5	-584
66	VDD2	-6352.5	-584
67	VDD2	-6247.5	-584
68	VDD1	-6142.5	-584
69	VDD1	-6037.5	-584
70	VDD1	-5932.5	-584
71	VDD1	-5827.5	-584
72	VDD1	-5722.5	-584
73	VDD3	-5617.5	-584
74	VD1O	-5512.5	-584
75	VD1O	-5407.5	-584
76	VD1O	-5302.5	-584
77	VD1O	-5197.5	-584
78	VD1I	-5092.5	-584
79	VD1I	-4987.5	-584
80	VD1I	-4882.5	-584
81	VD1I	-4777.5	-584
82	VSS3	-4672.5	-584
83	VSS1	-4567.5	-584
84	VSS1	-4462.5	-584
85	VSS1	-4357.5	-584
86	VSS1	-4252.5	-584
87	VSS1	-4147.5	-584
88	VSS2	-4042.5	-584
89	VSS2	-3937.5	-584
90	VSS2	-3832.5	-584
91	VSS2	-3727.5	-584
92	VSS2	-3622.5	-584

PAD	NAME	X	Y
93	VSS2	-3517.5	-584
94	VSS2	-3412.5	-584
95	VSS2	-3307.5	-584
96	VSS2	-3202.5	-584
97	VSS2	-3097.5	-584
98	VC	-2992.5	-584
99	VC	-2887.5	-584
100	VC	-2782.5	-584
101	VC	-2677.5	-584
102	VC	-2572.5	-584
103	VC	-2467.5	-584
104	T17	-2388.75	-584
105	T16	-2336.25	-584
106	T15	-2283.75	-584
107	T14	-2231.25	-584
108	TFCOM0	-2178.75	-584
109	T13	-2126.25	-584
110	T12	-2073.75	-584
111	T11	-2021.25	-584
112	T10	-1968.75	-584
113	T9	-1916.25	-584
114	T8	-1863.75	-584
115	T7	-1811.25	-584
116	T6	-1758.75	-584
117	TFCOM1	-1706.25	-584
118	T5	-1653.75	-584
119	T4	-1601.25	-584
120	T3	-1548.75	-584
121	T2	-1496.25	-584
122	T1	-1443.75	-584
123	T0	-1391.25	-584
124	VREF	-1338.75	-584
125	TCAP	-1260	-584
126	V2	-1155	-584
127	V2	-1050	-584
128	V2	-945	-584
129	V2	-840	-584
130	V1	-735	-584
131	V1	-630	-584
132	V1	-525	-584
133	V1	-420	-584
134	MV1	-315	-584
135	MV1	-210	-584
136	MV1	-105	-584
137	MV1	0	-584
138	MV2	105	-584
139	MV2	210	-584
140	MV2	315	-584

PAD	NAME	X	Y
141	MV2	420	-584
142	V3I	525	-584
143	V3I	630	-584
144	V3I	735	-584
145	V3I	840	-584
146	V3S	945	-584
147	V3O	1050	-584
148	V3O	1155	-584
149	V3O	1260	-584
150	MV3OI	1365	-584
151	MV3OI	1470	-584
152	MV3OI	1575	-584
153	MV3OI	1680	-584
154	MV3OI	1785	-584
155	MV3OI	1890	-584
156	MV3OI	1995	-584
157	MV3S	2100	-584
158	CB1P	2205	-584
159	CB1P	2310	-584
160	CB1P	2415	-584
161	CB1P	2520	-584
162	CB1N	2625	-584
163	CB1N	2730	-584
164	CB1N	2835	-584
165	CB1N	2940	-584
166	AVDD	3045	-584
167	AVDD	3150	-584
168	AVDD	3255	-584
169	AVDD	3360	-584
170	AVDD	3465	-584
171	AVDD	3570	-584
172	AVDD	3675	-584
173	AVDD	3780	-584
174	AVDD	3885	-584
175	AVDD	3990	-584
176	CA1P	4095	-584
177	CA1P	4200	-584
178	CA1P	4305	-584
179	CA1P	4410	-584
180	CA1P	4515	-584
181	CA1P	4620	-584
182	CA1P	4725	-584
183	CA1P	4830	-584
184	CA1P	4935	-584
185	CA1P	5040	-584
186	CA1N	5145	-584
187	CA1N	5250	-584
188	CA1N	5355	-584

PAD	NAME	X	Y
189	CA1N	5460	-584
190	CA1N	5565	-584
191	CA2P	5670	-584
192	CA2P	5775	-584
193	CA2P	5880	-584
194	CA2P	5985	-584
195	CA2P	6090	-584
196	CA2P	6195	-584
197	CA2P	6300	-584
198	CA2P	6405	-584
199	CA2P	6510	-584
200	CA2P	6615	-584
201	CA2N	6720	-584
202	CA2N	6825	-584
203	CA2N	6930	-584
204	CA2N	7035	-584
205	CA2N	7140	-584
206	NAVDD	7245	-584
207	NAVDD	7350	-584
208	NAVDD	7455	-584
209	NAVDD	7560	-584
210	NAVDD	7665	-584
211	NAVDD	7770	-584
212	NAVDD	7875	-584
213	NAVDD	7980	-584
214	CD1P	8085	-584
215	CD1P	8190	-584
216	CD1P	8295	-584
217	CD1P	8400	-584
218	CD1N	8505	-584
219	CD1N	8610	-584
220	CD1N	8715	-584
221	CD1N	8820	-584
222	CD2P	8925	-584
223	CD2P	9030	-584
224	CD2P	9135	-584
225	CD2P	9240	-584
226	CD2N	9345	-584
227	CD2N	9450	-584
228	CD2N	9555	-584
229	CD2N	9660	-584
230	Dummy	9738.75	-584
231	Dummy	9817.5	-584
232	Dummy	9922.5	-584
233	Dummy	10027.5	-584
234	Dummy	10132.5	-584
235	COM[68]	10273.5	-540
236	COM[69]	10273.5	-500

PAD	NAME	X	Y
237	COM[70]	10273.5	-460
238	COM[71]	10273.5	-420
239	COM[72]	10273.5	-380
240	COM[73]	10273.5	-340
241	COM[74]	10273.5	-300
242	COM[75]	10273.5	-260
243	COM[76]	10273.5	-220
244	COM[77]	10273.5	-180
245	COM[78]	10273.5	-140
246	COM[79]	10273.5	-100
247	COM[80]	10273.5	-60
248	COM[81]	10273.5	-20
249	COM[82]	10273.5	20
250	COM[83]	10273.5	60
251	COM[84]	10273.5	100
252	COM[85]	10273.5	140
253	COM[86]	10273.5	180
254	COM[87]	10273.5	220
255	COM[88]	10273.5	260
256	COM[89]	10273.5	300
257	COM[90]	10273.5	340
258	COM[91]	10273.5	380
259	COM[92]	10273.5	420
260	COM[93]	10273.5	460
261	COM[94]	10273.5	500
262	COM[95]	10273.5	540
263	Dummy	10146.49	558.5
264	Dummy	10106.49	558.5
265	Dummy	10066.49	558.5
266	Dummy	10026.49	558.5
267	Dummy	9986.49	558.5
268	Dummy	9946.49	558.5
269	Dummy	9906.49	558.5
270	Dummy	9866.49	558.5
271	COM[96]	9826.49	558.5
272	COM[97]	9786.49	558.5
273	COM[98]	9746.49	558.5
274	COM[99]	9706.49	558.5
275	COM[100]	9666.49	558.5
276	COM[101]	9626.49	558.5
277	COM[102]	9586.49	558.5
278	COM[103]	9546.49	558.5
279	COM[104]	9506.49	558.5
280	COM[105]	9466.49	558.5
281	COM[106]	9426.49	558.5
282	COM[107]	9386.49	558.5
283	COM[108]	9346.49	558.5
284	COM[109]	9306.49	558.5

PAD	NAME	X	Y
285	COM[110]	9266.49	558.5
286	COM[111]	9226.49	558.5
287	COM[112]	9186.49	558.5
288	COM[113]	9146.49	558.5
289	COM[114]	9106.49	558.5
290	COM[115]	9066.49	558.5
291	COM[116]	9026.49	558.5
292	COM[117]	8986.49	558.5
293	COM[118]	8946.49	558.5
294	COM[119]	8906.49	558.5
295	COM[120]	8866.49	558.5
296	COM[121]	8826.49	558.5
297	COM[122]	8786.49	558.5
298	COM[123]	8746.49	558.5
299	COM[124]	8706.49	558.5
300	COM[125]	8666.49	558.5
301	COM[126]	8626.49	558.5
302	COM[127]	8586.49	558.5
303	COM[128]	8546.49	558.5
304	COM[129]	8506.49	558.5
305	COM[130]	8466.49	558.5
306	COM[131]	8426.49	558.5
307	SEG[395]	8306.24	558.5
308	SEG[394]	8266.24	558.5
309	SEG[393]	8226.24	558.5
310	SEG[392]	8186.24	558.5
311	SEG[391]	8146.24	558.5
312	SEG[390]	8106.24	558.5
313	SEG[389]	8066.24	558.5
314	SEG[388]	8026.24	558.5
315	SEG[387]	7986.24	558.5
316	SEG[386]	7946.24	558.5
317	SEG[385]	7906.24	558.5
318	SEG[384]	7866.24	558.5
319	SEG[383]	7826.24	558.5
320	SEG[382]	7786.24	558.5
321	SEG[381]	7746.24	558.5
322	SEG[380]	7706.24	558.5
323	SEG[379]	7666.24	558.5
324	SEG[378]	7626.24	558.5
325	SEG[377]	7586.24	558.5
326	SEG[376]	7546.24	558.5
327	SEG[375]	7506.24	558.5
328	SEG[374]	7466.24	558.5
329	SEG[373]	7426.24	558.5
330	SEG[372]	7386.24	558.5
331	SEG[371]	7346.24	558.5
332	SEG[370]	7306.24	558.5

PAD	NAME	X	Y
333	SEG[369]	7266.24	558.5
334	SEG[368]	7226.24	558.5
335	SEG[367]	6963.57	558.5
336	SEG[366]	6923.57	558.5
337	SEG[365]	6883.57	558.5
338	SEG[364]	6843.57	558.5
339	SEG[363]	6803.57	558.5
340	SEG[362]	6763.57	558.5
341	SEG[361]	6723.57	558.5
342	SEG[360]	6683.57	558.5
343	SEG[359]	6643.57	558.5
344	SEG[358]	6603.57	558.5
345	SEG[357]	6563.57	558.5
346	SEG[356]	6523.57	558.5
347	SEG[355]	6483.57	558.5
348	SEG[354]	6443.57	558.5
349	SEG[353]	6403.57	558.5
350	SEG[352]	6363.57	558.5
351	SEG[351]	6323.57	558.5
352	SEG[350]	6283.57	558.5
353	SEG[349]	6243.57	558.5
354	SEG[348]	6203.57	558.5
355	SEG[347]	6163.57	558.5
356	SEG[346]	6123.57	558.5
357	SEG[345]	6083.57	558.5
358	SEG[344]	6043.57	558.5
359	SEG[343]	6003.57	558.5
360	SEG[342]	5963.57	558.5
361	SEG[341]	5923.57	558.5
362	SEG[340]	5883.57	558.5
363	SEG[339]	5843.57	558.5
364	SEG[338]	5803.57	558.5
365	SEG[337]	5763.57	558.5
366	SEG[336]	5723.57	558.5
367	SEG[335]	5683.57	558.5
368	SEG[334]	5643.57	558.5
369	SEG[333]	5603.57	558.5
370	SEG[332]	5563.57	558.5
371	SEG[331]	5523.57	558.5
372	SEG[330]	5483.57	558.5
373	SEG[329]	5443.57	558.5
374	SEG[328]	5403.57	558.5
375	SEG[327]	5363.57	558.5
376	SEG[326]	5323.57	558.5
377	SEG[325]	5283.57	558.5
378	SEG[324]	5243.57	558.5
379	SEG[323]	5203.57	558.5
380	SEG[322]	5163.57	558.5

PAD	NAME	X	Y
381	SEG[321]	5123.57	558.5
382	SEG[320]	5083.57	558.5
383	SEG[319]	5043.57	558.5
384	SEG[318]	5003.57	558.5
385	SEG[317]	4963.57	558.5
386	SEG[316]	4923.57	558.5
387	SEG[315]	4883.57	558.5
388	SEG[314]	4843.57	558.5
389	SEG[313]	4803.57	558.5
390	SEG[312]	4763.57	558.5
391	SEG[311]	4723.57	558.5
392	SEG[310]	4683.57	558.5
393	SEG[309]	4643.57	558.5
394	SEG[308]	4603.57	558.5
395	SEG[307]	4563.57	558.5
396	SEG[306]	4523.57	558.5
397	SEG[305]	4483.57	558.5
398	SEG[304]	4443.57	558.5
399	SEG[303]	4403.57	558.5
400	SEG[302]	4363.57	558.5
401	SEG[301]	4323.57	558.5
402	SEG[300]	4283.57	558.5
403	SEG[299]	4243.57	558.5
404	SEG[298]	4203.57	558.5
405	SEG[297]	4163.57	558.5
406	SEG[296]	4123.57	558.5
407	SEG[295]	4083.57	558.5
408	SEG[294]	4043.57	558.5
409	SEG[293]	4003.57	558.5
410	SEG[292]	3963.57	558.5
411	SEG[291]	3923.57	558.5
412	SEG[290]	3883.57	558.5
413	SEG[289]	3843.57	558.5
414	SEG[288]	3803.57	558.5
415	SEG[287]	3763.57	558.5
416	SEG[286]	3723.57	558.5
417	SEG[285]	3683.57	558.5
418	SEG[284]	3643.57	558.5
419	SEG[283]	3603.57	558.5
420	SEG[282]	3563.57	558.5
421	SEG[281]	3523.57	558.5
422	SEG[280]	3483.57	558.5
423	SEG[279]	3443.57	558.5
424	SEG[278]	3403.57	558.5
425	SEG[277]	3363.57	558.5
426	SEG[276]	3323.57	558.5
427	SEG[275]	3283.57	558.5
428	SEG[274]	3243.57	558.5

PAD	NAME	X	Y
429	SEG[273]	3203.57	558.5
430	SEG[272]	3163.57	558.5
431	SEG[271]	3123.57	558.5
432	SEG[270]	3083.57	558.5
433	SEG[269]	3043.57	558.5
434	SEG[268]	3003.57	558.5
435	SEG[267]	2963.57	558.5
436	SEG[266]	2923.57	558.5
437	SEG[265]	2883.57	558.5
438	SEG[264]	2843.57	558.5
439	SEG[263]	2803.57	558.5
440	SEG[262]	2763.57	558.5
441	SEG[261]	2723.57	558.5
442	SEG[260]	2683.57	558.5
443	SEG[259]	2643.57	558.5
444	SEG[258]	2603.57	558.5
445	SEG[257]	2563.57	558.5
446	SEG[256]	2523.57	558.5
447	SEG[255]	2483.57	558.5
448	SEG[254]	2443.57	558.5
449	SEG[253]	2403.57	558.5
450	SEG[252]	2363.57	558.5
451	SEG[251]	2323.57	558.5
452	SEG[250]	2283.57	558.5
453	SEG[249]	2243.57	558.5
454	SEG[248]	2203.57	558.5
455	SEG[247]	2163.57	558.5
456	SEG[246]	2123.57	558.5
457	SEG[245]	2083.57	558.5
458	SEG[244]	2043.57	558.5
459	SEG[243]	2003.57	558.5
460	SEG[242]	1963.57	558.5
461	SEG[241]	1923.57	558.5
462	SEG[240]	1883.57	558.5
463	SEG[239]	1843.57	558.5
464	SEG[238]	1803.57	558.5
465	SEG[237]	1763.57	558.5
466	SEG[236]	1723.57	558.5
467	SEG[235]	1683.57	558.5
468	SEG[234]	1643.57	558.5
469	SEG[233]	1603.57	558.5
470	SEG[232]	1563.57	558.5
471	SEG[231]	1523.57	558.5
472	SEG[230]	1483.57	558.5
473	SEG[229]	1443.57	558.5
474	SEG[228]	1403.57	558.5
475	SEG[227]	1363.57	558.5
476	SEG[226]	1323.57	558.5

PAD	NAME	X	Y
477	SEG[225]	1283.57	558.5
478	SEG[224]	1243.57	558.5
479	SEG[223]	1203.57	558.5
480	SEG[222]	1163.57	558.5
481	SEG[221]	1123.57	558.5
482	SEG[220]	1083.57	558.5
483	SEG[219]	1043.57	558.5
484	SEG[218]	1003.57	558.5
485	SEG[217]	963.57	558.5
486	SEG[216]	923.57	558.5
487	SEG[215]	883.57	558.5
488	SEG[214]	843.57	558.5
489	SEG[213]	803.57	558.5
490	SEG[212]	763.57	558.5
491	SEG[211]	723.57	558.5
492	SEG[210]	683.57	558.5
493	SEG[209]	643.57	558.5
494	SEG[208]	603.57	558.5
495	SEG[207]	563.57	558.5
496	SEG[206]	523.57	558.5
497	SEG[205]	483.57	558.5
498	SEG[204]	443.57	558.5
499	SEG[203]	403.57	558.5
500	SEG[202]	363.57	558.5
501	SEG[201]	323.57	558.5
502	SEG[200]	283.57	558.5
503	SEG[199]	243.57	558.5
504	SEG[198]	203.57	558.5
505	SEG[197]	163.57	558.5
506	SEG[196]	123.57	558.5
507	SEG[195]	-123.57	558.5
508	SEG[194]	-163.57	558.5
509	SEG[193]	-203.57	558.5
510	SEG[192]	-243.57	558.5
511	SEG[191]	-283.57	558.5
512	SEG[190]	-323.57	558.5
513	SEG[189]	-363.57	558.5
514	SEG[188]	-403.57	558.5
515	SEG[187]	-443.57	558.5
516	SEG[186]	-483.57	558.5
517	SEG[185]	-523.57	558.5
518	SEG[184]	-563.57	558.5
519	SEG[183]	-603.57	558.5
520	SEG[182]	-643.57	558.5
521	SEG[181]	-683.57	558.5
522	SEG[180]	-723.57	558.5
523	SEG[179]	-763.57	558.5
524	SEG[178]	-803.57	558.5

PAD	NAME	X	Y
525	SEG[177]	-843.57	558.5
526	SEG[176]	-883.57	558.5
527	SEG[175]	-923.57	558.5
528	SEG[174]	-963.57	558.5
529	SEG[173]	-1003.57	558.5
530	SEG[172]	-1043.57	558.5
531	SEG[171]	-1083.57	558.5
532	SEG[170]	-1123.57	558.5
533	SEG[169]	-1163.57	558.5
534	SEG[168]	-1203.57	558.5
535	SEG[167]	-1243.57	558.5
536	SEG[166]	-1283.57	558.5
537	SEG[165]	-1323.57	558.5
538	SEG[164]	-1363.57	558.5
539	SEG[163]	-1403.57	558.5
540	SEG[162]	-1443.57	558.5
541	SEG[161]	-1483.57	558.5
542	SEG[160]	-1523.57	558.5
543	SEG[159]	-1563.57	558.5
544	SEG[158]	-1603.57	558.5
545	SEG[157]	-1643.57	558.5
546	SEG[156]	-1683.57	558.5
547	SEG[155]	-1723.57	558.5
548	SEG[154]	-1763.57	558.5
549	SEG[153]	-1803.57	558.5
550	SEG[152]	-1843.57	558.5
551	SEG[151]	-1883.57	558.5
552	SEG[150]	-1923.57	558.5
553	SEG[149]	-1963.57	558.5
554	SEG[148]	-2003.57	558.5
555	SEG[147]	-2043.57	558.5
556	SEG[146]	-2083.57	558.5
557	SEG[145]	-2123.57	558.5
558	SEG[144]	-2163.57	558.5
559	SEG[143]	-2203.57	558.5
560	SEG[142]	-2243.57	558.5
561	SEG[141]	-2283.57	558.5
562	SEG[140]	-2323.57	558.5
563	SEG[139]	-2363.57	558.5
564	SEG[138]	-2403.57	558.5
565	SEG[137]	-2443.57	558.5
566	SEG[136]	-2483.57	558.5
567	SEG[135]	-2523.57	558.5
568	SEG[134]	-2563.57	558.5
569	SEG[133]	-2603.57	558.5
570	SEG[132]	-2643.57	558.5
571	SEG[131]	-2683.57	558.5
572	SEG[130]	-2723.57	558.5

PAD	NAME	X	Y
573	SEG[129]	-2763.57	558.5
574	SEG[128]	-2803.57	558.5
575	SEG[127]	-2843.57	558.5
576	SEG[126]	-2883.57	558.5
577	SEG[125]	-2923.57	558.5
578	SEG[124]	-2963.57	558.5
579	SEG[123]	-3003.57	558.5
580	SEG[122]	-3043.57	558.5
581	SEG[121]	-3083.57	558.5
582	SEG[120]	-3123.57	558.5
583	SEG[119]	-3163.57	558.5
584	SEG[118]	-3203.57	558.5
585	SEG[117]	-3243.57	558.5
586	SEG[116]	-3283.57	558.5
587	SEG[115]	-3323.57	558.5
588	SEG[114]	-3363.57	558.5
589	SEG[113]	-3403.57	558.5
590	SEG[112]	-3443.57	558.5
591	SEG[111]	-3483.57	558.5
592	SEG[110]	-3523.57	558.5
593	SEG[109]	-3563.57	558.5
594	SEG[108]	-3603.57	558.5
595	SEG[107]	-3643.57	558.5
596	SEG[106]	-3683.57	558.5
597	SEG[105]	-3723.57	558.5
598	SEG[104]	-3763.57	558.5
599	SEG[103]	-3803.57	558.5
600	SEG[102]	-3843.57	558.5
601	SEG[101]	-3883.57	558.5
602	SEG[100]	-3923.57	558.5
603	SEG[99]	-3963.57	558.5
604	SEG[98]	-4003.57	558.5
605	SEG[97]	-4043.57	558.5
606	SEG[96]	-4083.57	558.5
607	SEG[95]	-4123.57	558.5
608	SEG[94]	-4163.57	558.5
609	SEG[93]	-4203.57	558.5
610	SEG[92]	-4243.57	558.5
611	SEG[91]	-4283.57	558.5
612	SEG[90]	-4323.57	558.5
613	SEG[89]	-4363.57	558.5
614	SEG[88]	-4403.57	558.5
615	SEG[87]	-4443.57	558.5
616	SEG[86]	-4483.57	558.5
617	SEG[85]	-4523.57	558.5
618	SEG[84]	-4563.57	558.5
619	SEG[83]	-4603.57	558.5
620	SEG[82]	-4643.57	558.5

PAD	NAME	X	Y
621	SEG[81]	-4683.57	558.5
622	SEG[80]	-4723.57	558.5
623	SEG[79]	-4763.57	558.5
624	SEG[78]	-4803.57	558.5
625	SEG[77]	-4843.57	558.5
626	SEG[76]	-4883.57	558.5
627	SEG[75]	-4923.57	558.5
628	SEG[74]	-4963.57	558.5
629	SEG[73]	-5003.57	558.5
630	SEG[72]	-5043.57	558.5
631	SEG[71]	-5083.57	558.5
632	SEG[70]	-5123.57	558.5
633	SEG[69]	-5163.57	558.5
634	SEG[68]	-5203.57	558.5
635	SEG[67]	-5243.57	558.5
636	SEG[66]	-5283.57	558.5
637	SEG[65]	-5323.57	558.5
638	SEG[64]	-5363.57	558.5
639	SEG[63]	-5403.57	558.5
640	SEG[62]	-5443.57	558.5
641	SEG[61]	-5483.57	558.5
642	SEG[60]	-5523.57	558.5
643	SEG[59]	-5563.57	558.5
644	SEG[58]	-5603.57	558.5
645	SEG[57]	-5643.57	558.5
646	SEG[56]	-5683.57	558.5
647	SEG[55]	-5723.57	558.5
648	SEG[54]	-5763.57	558.5
649	SEG[53]	-5803.57	558.5
650	SEG[52]	-5843.57	558.5
651	SEG[51]	-5883.57	558.5
652	SEG[50]	-5923.57	558.5
653	SEG[49]	-5963.57	558.5
654	SEG[48]	-6003.57	558.5
655	SEG[47]	-6043.57	558.5
656	SEG[46]	-6083.57	558.5
657	SEG[45]	-6123.57	558.5
658	SEG[44]	-6163.57	558.5
659	SEG[43]	-6203.57	558.5
660	SEG[42]	-6243.57	558.5
661	SEG[41]	-6283.57	558.5
662	SEG[40]	-6323.57	558.5
663	SEG[39]	-6363.57	558.5
664	SEG[38]	-6403.57	558.5
665	SEG[37]	-6443.57	558.5
666	SEG[36]	-6483.57	558.5
667	SEG[35]	-6523.57	558.5
668	SEG[34]	-6563.57	558.5

PAD	NAME	X	Y
669	SEG[33]	-6603.57	558.5
670	SEG[32]	-6643.57	558.5
671	SEG[31]	-6683.57	558.5
672	SEG[30]	-6723.57	558.5
673	SEG[29]	-6763.57	558.5
674	SEG[28]	-6803.57	558.5
675	SEG[27]	-6843.57	558.5
676	SEG[26]	-6883.57	558.5
677	SEG[25]	-6923.57	558.5
678	SEG[24]	-6963.57	558.5
679	SEG[23]	-7226.24	558.5
680	SEG[22]	-7266.24	558.5
681	SEG[21]	-7306.24	558.5
682	SEG[20]	-7346.24	558.5
683	SEG[19]	-7386.24	558.5
684	SEG[18]	-7426.24	558.5
685	SEG[17]	-7466.24	558.5
686	SEG[16]	-7506.24	558.5
687	SEG[15]	-7546.24	558.5
688	SEG[14]	-7586.24	558.5
689	SEG[13]	-7626.24	558.5
690	SEG[12]	-7666.24	558.5
691	SEG[11]	-7706.24	558.5
692	SEG[10]	-7746.24	558.5
693	SEG[9]	-7786.24	558.5
694	SEG[8]	-7826.24	558.5
695	SEG[7]	-7866.24	558.5
696	SEG[6]	-7906.24	558.5
697	SEG[5]	-7946.24	558.5
698	SEG[4]	-7986.24	558.5
699	SEG[3]	-8026.24	558.5
700	SEG[2]	-8066.24	558.5
701	SEG[1]	-8106.24	558.5
702	SEG[0]	-8146.24	558.5
703	COM[67]	-8266.49	558.5
704	COM[66]	-8306.49	558.5
705	COM[65]	-8346.49	558.5
706	COM[64]	-8386.49	558.5
707	COM[63]	-8426.49	558.5
708	COM[62]	-8466.49	558.5
709	COM[61]	-8506.49	558.5
710	COM[60]	-8546.49	558.5
711	COM[59]	-8586.49	558.5
712	COM[58]	-8626.49	558.5
713	COM[57]	-8666.49	558.5
714	COM[56]	-8706.49	558.5
715	COM[55]	-8746.49	558.5
716	COM[54]	-8786.49	558.5

PAD	NAME	X	Y
717	COM[53]	-8826.49	558.5
718	COM[52]	-8866.49	558.5
719	COM[51]	-8906.49	558.5
720	COM[50]	-8946.49	558.5
721	COM[49]	-8986.49	558.5
722	COM[48]	-9026.49	558.5
723	COM[47]	-9066.49	558.5
724	COM[46]	-9106.49	558.5
725	COM[45]	-9146.49	558.5
726	COM[44]	-9186.49	558.5
727	COM[43]	-9226.49	558.5
728	COM[42]	-9266.49	558.5
729	COM[41]	-9306.49	558.5
730	COM[40]	-9346.49	558.5
731	COM[39]	-9386.49	558.5
732	COM[38]	-9426.49	558.5
733	COM[37]	-9466.49	558.5
734	COM[36]	-9506.49	558.5
735	COM[35]	-9546.49	558.5
736	COM[34]	-9586.49	558.5
737	COM[33]	-9626.49	558.5
738	COM[32]	-9666.49	558.5
739	COM[31]	-9706.49	558.5
740	COM[30]	-9746.49	558.5
741	COM[29]	-9786.49	558.5
742	COM[28]	-9826.49	558.5
743	Dummy	-9866.49	558.5
744	Dummy	-9906.49	558.5
745	Dummy	-9946.49	558.5
746	Dummy	-9986.49	558.5
747	Dummy	-10026.49	558.5
748	Dummy	-10066.49	558.5
749	Dummy	-10106.49	558.5
750	Dummy	-10146.49	558.5

Unit : um

Note:

- Please refer to the instruction “COM Output Status” to decide COM layout sequence.

BLOCK DIAGRAM

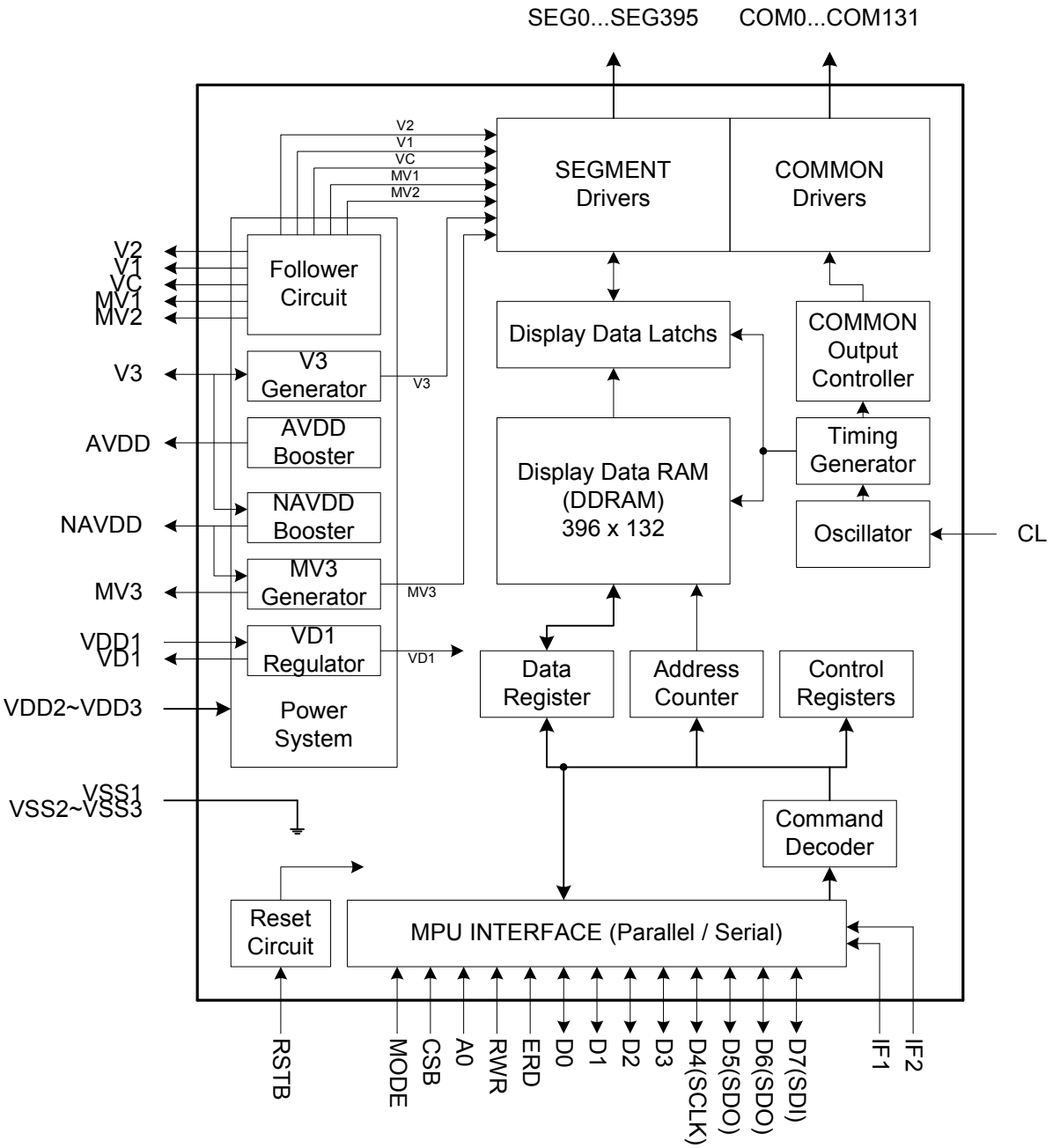


Fig. 1 Block Diagram

PIN DESCRIPTION

Power System

Name	Type	Description
VDD1	Power	VDD1 is the power of interface I/O circuit and OSC circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.
VDD2	Power	VDD2 is the analog power for booster circuit and OP.
VDD3	Power	VDD3 is the power of VREF circuit. VDD1 and VDD3 are separated in ITO and connected together by FPC or PCB.
VSS1	Power	Ground of interface, logic and OSC circuit. Ground system should be connected by FPC or PCB.
VSS2	Power	Ground of booster circuit and OP. Ground system should be connected by FPC or PCB.
VSS3	Power	Ground of VREF circuit. Ground system should be connected by FPC or PCB.
VD1I VD1O	Power	VD1I is the power source of digital circuit. VD1O is the VD1 output. VD1I and VD1O should be connected together by FPC or PCB. VD1 is generated by internal VD1 generator. Those pins can not connect with VDD power (VDD1, VDD2 and VDD3). The power level of VD1 is 1.8V.
V3O V3I V3S	Power	LCD driver supply. V3O is the output voltage of V3 generated by ST7592. V3I is the V3 supply of LCD drivers. V3S is the sensor of the V3 generator. V3O, V3I and V3S should be connected together by FPC.
V2	Power	LCD driver supply.
V1	Power	LCD driver supply.
VC	Power	LCD driver supply for center level. VC should be connected with ground system by FPC or PCB.
MV1	Power	LCD driver supply.
MV2	Power	LCD driver supply.
MV3OI MV3S	Power	LCD driver supply. MV3OI is the output voltage of MV3 generated by ST7592 for supply LCD drivers. MV3S is the sensor of the MV3 generator. MV3OI and MV3S should be connected together by FPC.

Name	Type	Description
AVDD	Power	DC/DC converter for LCD driver circuit. Connect a capacitor between AVDD pin and VSS2.
NAVDD	Power	DC/DC converter for LCD driver circuit. Connect a capacitor between NAVDD pin and VSS2.
CA1P CA1N CA2P CA2N	Power	DC/DC converter for AVDD power circuit. Connect a non-polar capacitor between CA1P pin and CA1N pin. Connect a non-polar capacitor between CA2P pin and CA2N pin.
CB1P CB1N	Power	DC/DC converter for MV3 power circuit. Connect a non-polar capacitor between CB1P pin and CB1N pin.
CD1P CD1N CD2P CD2N	Power	DC/DC converter for NAVDD power circuit. Connect a non-polar capacitor between CD1P pin and CD1N pin. Connect a non-polar capacitor between CD2P pin and CD2N pin.

LCD Driver Outputs

Name	Type	Description
SEG0 to SEG395	Output	LCD SEG-driver outputs. One voltage level of V2, V1, VC, MV1 and MV2 is selected by combining display DDRAM.
COM0 to COM131	Output	LCD COM-driver outputs. One voltage level of V3, VC and MV3 is selected by combining display DDRAM.

Microprocessor Interface

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSTB</td><td>Input</td><td>Reset input pin. When RSTB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>IF[2:1]</td><td>Input</td><td>These pins select interface operation mode.
<table>
<tr><th>IF2</th><th>IF1</th><th>MCU interface type</th></tr>
<tr><td>H</td><td>H</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>68 series 8-bit parallel</td></tr>
<tr><td>L</td><td>H</td><td>8-bit serial (4-Line)</td></tr>
<tr><td>L</td><td>L</td><td>9-bit serial (3-Line)</td></tr>
</table>
Note: Refer to “Interface Selection” for detailed information.</td></tr>
<tr><td>CSB</td><td>Input</td><td>Chip select input pin.
CSB=“L”: This chip is selected and the MCU interface is active.
CSB=“H”: This chip is not selected and the MCU interface is disabled (D[7:0] are high impedance).</td></tr>
<tr><td>A0</td><td>Input</td><td>A0 determines whether the access is related data or command.
● In parallel interface and 4-Line SPI: A0 is register selection input.
A0 = "H": inputs on data bus are display data;
A0 = "L": inputs on data bus are command.
● A0 is not used in 3-Line SPI. Please fix to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>Input</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MCU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
R/W = “H” : read
R/W = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable clock input pin.
The data are latched at the rising edge of the /WR signal.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to “H” by VDD1.</td></tr>
<tr><td>ERD</td><td>Input</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MCU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin.
R/W = “H”: When E is “H”, data bus is in output status.
R/W = “L”: The data are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, data bus is in output status.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to “H” by VDD1.</td></tr>
<tr><td>D[7:0]</td><td>I/O</td><td>The bi-directional data bus of the MCU interface. When CSB is “H”, they are high impedance.
● If using serial interface:
SDI: D7
SDO: D5, D6
SCL: D4
D0~D3 must connected to “H” by VDD1.</td></tr>
</table>

Note:

1. After VDD1 is turned ON, all MCU interface pins should not be left OPEN.
2. The un-used pins should be connected to VDD1.

PROM Pins

Name	Type	Description
VPP	Power	The programming power supply of the built-in PROM. Apply external power (VPP=7.25~7.75V, VPP_{TYP}=7.5V) here when programming (> 4mA for successful programming).
EXTB	Input	EXTB="L": Enable the extension operation mode. When programming PROM, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

System Pins

Name	Type	Description
MODE	Input	Must fix to "H" by VDD1.
CLS	Input	When using internal clock oscillator, please connect this pin to "H" by VDD1. When using external clock oscillator, please connect this pin to "L" by VSS1.
CL	I/O	When using internal clock oscillator, this pin is oscillator output. When using external clock oscillator, this pin is oscillator input.

Test Pins

Name	Type	Description
TCAP	Test	Reserved for testing only. Leave this pin open.
VREF	Test	Reserved for testing only. Leave this pin open.
T0~T19	Test	Reserved for testing only. Leave those pins open.
TFCOM0 TFCOM1	Test	Reserved for testing only. Leave those pins open.

Note: Please refer to LCD LAYOUT GUIDE for Application Circuit, ITO Layout Suggestion and ITO Resistance.

FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

CSB pin is used for chip selection. ST7592 can interface with a MCU when CSB is “L”. If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is “H”.

Interface Selection

The interface selection is controlled by IF[2:1] pins. Please refer to the table below:

Table 1

Setting		MCU Type	Interface Pin Function				
IF2	IF1		CSB	A0	RWR	ERD	D[7:0]
H	H	Parallel 8080 series MCU	CSB	A0	/WR	/RD	D[7:0]
H	L	Parallel 6800 series MCU			R/W	E	
L	H	Serial 4-Line series MCU			-	-	D7=SDI, D[5:6]=SDO, D4=SCL, D[0:3] are not used
L	L	Serial 3-Line series MCU		-	-	-	

Note: The un-used pins are marked as “-” and should be connected to “H” by VDD1.

Parallel Interface

When parallel interface is selected, the interface transmission type will be determined by the combination of the control signals. Please refer to the table below:

Table 2

8080 series MCU		6800 series MCU		A0	CSB	Interface Transmission Type
/WR	/RD	R/W	E			
↑	H	L	↓	L	L	Write Command
↑	H	L	↓	H		Write Display Data or Parameter
H	↓	H	↑	H		Read Display Data or Parameter Start
H	↑	H	↓	H		Read Display Data or Parameter Stop

Note:

1. Reading Display Data or Parameter is specified by the instruction before the read operation.
2. When reading Display Data (DDRAM contents), the first output byte is dummy byte.
3. When reading Parameter (temperature, status and PROM data), the first output byte is valid.

Serial Interface

In serial interface (4-Line or 3-Line), IC is active and the control signals (SDI, SDO, SCL and A0 for 4-Line) are enabled when CSB is “L”. When CSB is “H”, the MCU interface is not active and the internal shift-register and serial-counter are reset.

If CSB is set to “H” before all data bits (8 bits) are entered completely, the data concerned is invalidated. Before entering succeeding sets of data, you must input the data concerned again. In order to avoid transfer error due to incoming noise when write command or data, it is recommended to set CSB at “H” on byte basis, so that the serial-to-parallel counter and the shift-register can be cleared after each byte of transmission.

The serial interface can read: temperature, status and PROM parameter, except Display Data. Please note that:

1. A read transfer will be stopped if CSB is set to “H”.
2. When reading IC status, the first output bit is dummy bit.
3. When reading temperature and PROM content, the first output bit is valid (without dummy bit).

4-Line Serial Interface

In 4-Line serial interface, A0 signal is latched at the 8th rising edge of the SCL signal (refer to Fig. 2).

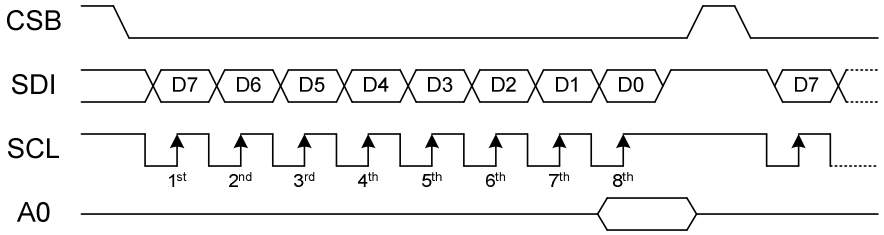


Fig. 2 Write-Operation of 4-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at "L" during this period. The 1st read out data (1st Data) is 9 bits, which includes a dummy bit at the 1st bit. After 1st Data, all read out data (2nd Data) will be 8 bits.

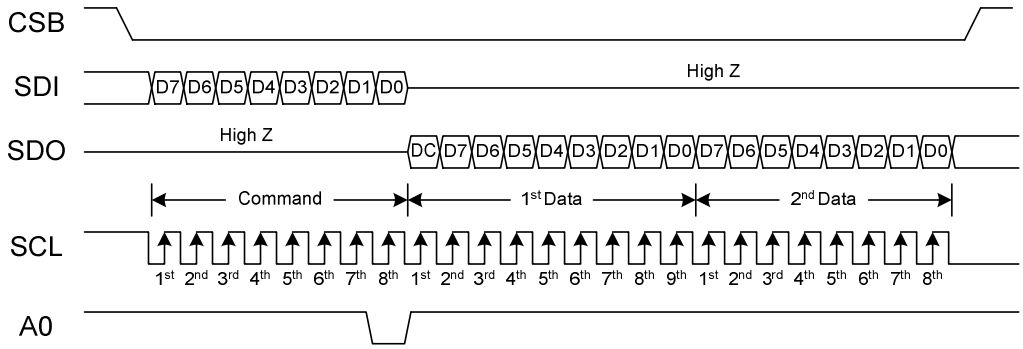


Fig. 3 Read-Operation of 4-Line Serial Interface

3-Line Serial Interface

In 3-Line interface, A0 signal is not available. The 1st output bit defines command byte or parameter byte (refer to Fig. 4).

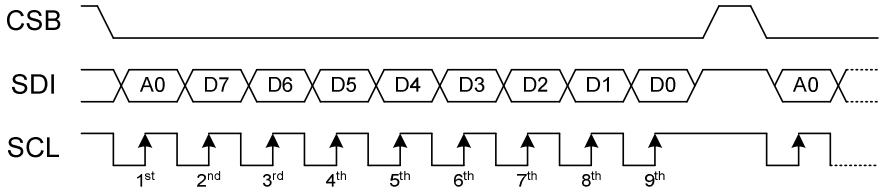


Fig. 4 Write-Operation of 3-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at "L" during this period. The 1st read out data (1st Data) is 9 bits, which includes a dummy bit at the 1st bit. After 1st Data, all read out data (2nd Data) will be 8 bits.

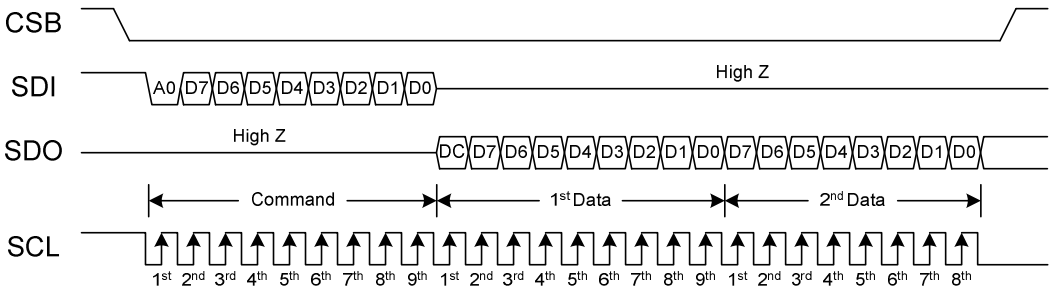


Fig. 5 Read-Operation of 3-Line Serial Interface

Display Data RAM (DDRAM)

ST7592 containing a 396x132 bits static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 396 columns by 132 rows. When the data bit in DDRAM is “1”, the segment driver will output “ON” voltage. If it is “0”, the segment driver will output “OFF” voltage. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.

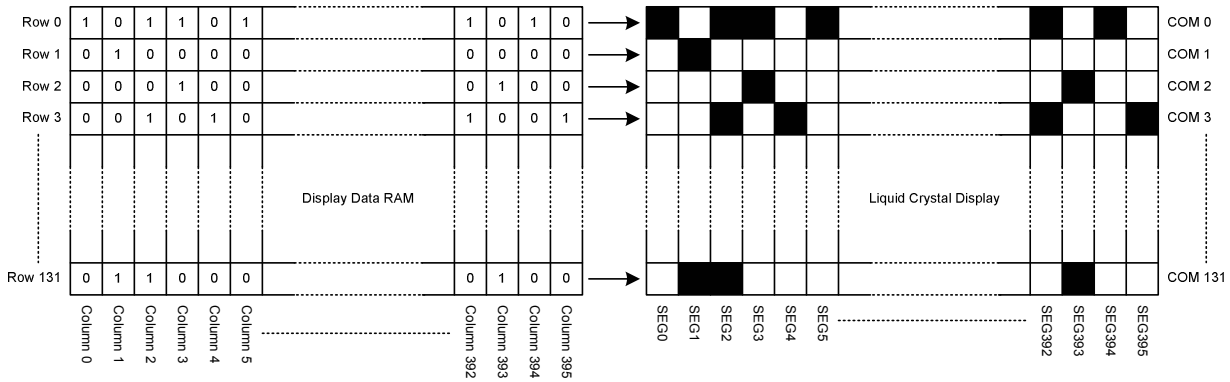


Fig. 6 DDRAM Mapping

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates a 5-bit Page Address Register which can be modified by the instruction of Page Address Set only. As shown in Fig. 7, the 132 rows are configured as 16 pages with 8-bit (for COM0~COM127 while row address direction is normal) and 1 page with 4-bit (for COM128~COM131 while row address direction is normal). The page address must be set before accessing DDRAM content.

Column Address Circuit

This circuit provides the column address of DDRAM. It incorporates a 9-bit Column Address Register which can be modified by the instruction of “Column Address” only. The column address must be set before accessing DDRAM content.

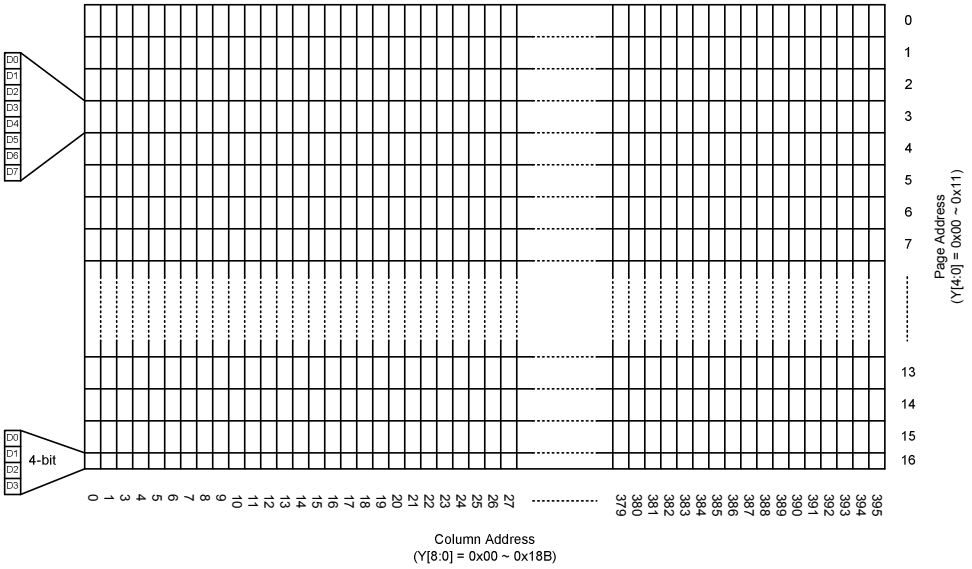


Fig. 7 DDRAM Format

Addressing

Data is downloaded into the Display Data RAM matrix in ST7592 as byte-format. The Display Data RAM has a matrix of 396 by 132 bits. The address ranges are: X=0~395 (column address), Y=0~17 (page address). Address outside these ranges is not allowed.

Addressing the target DDRAM of access is specified with the Page Address Set command and Column Address Set command. Using the Display Data Input/Output Direction command allows you to increase the address either in the page or column direction. In both case, the address is increased by one (+1) after the write or read operation.

When Display Data Input/Output Direction command setting is column direction, the column address counter is increased by 1 (+1) after the write or read operation as shown in Fig. 8. If column address counter is over 18Bh after data accessed, the page address is increased by one (+1) and the column address is returned to 00h respectively.

Besides, when Display Data Input/Output Direction command setting is page direction, the page address counter is increase by 1 (+1) after the write or read operation as shown in Fig. 9. If the page address counter is over 10h after data accessed, the column address is increased by 1 (+1) and page address is returned to 00h respectively.

Whichever direction is selected, the page address counter and column address counter are returned to 00h and 00h respectively, after the DDRAM of column address 18Bh and page address 10h is accessed.

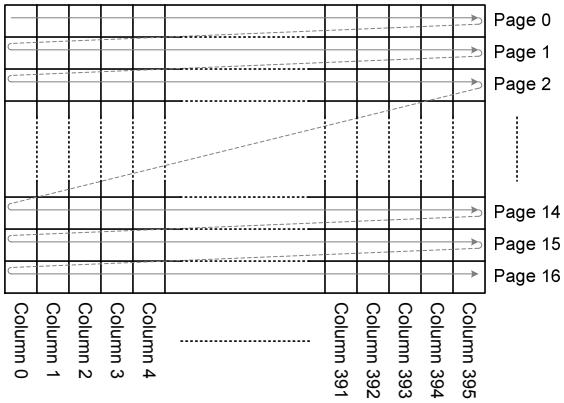


Fig. 8 Display Data Input Direction (DIR=0 & MX=0)

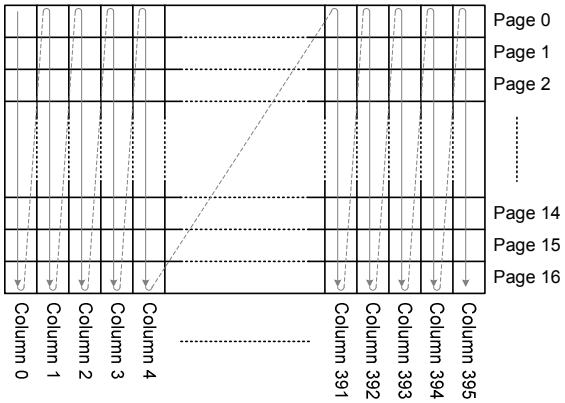


Fig. 9 Display Data Input Direction (DIR=1 & MX=0)

LCD Display Function

DDRAM Map to LCD Driver Output

The internal relation between DDRAM and LCD driver circuit (SEG/COM output path) with different MX or MY setting is illustrated below. Please refer to the instruction “COM Output Status” to decide COM layout sequence.

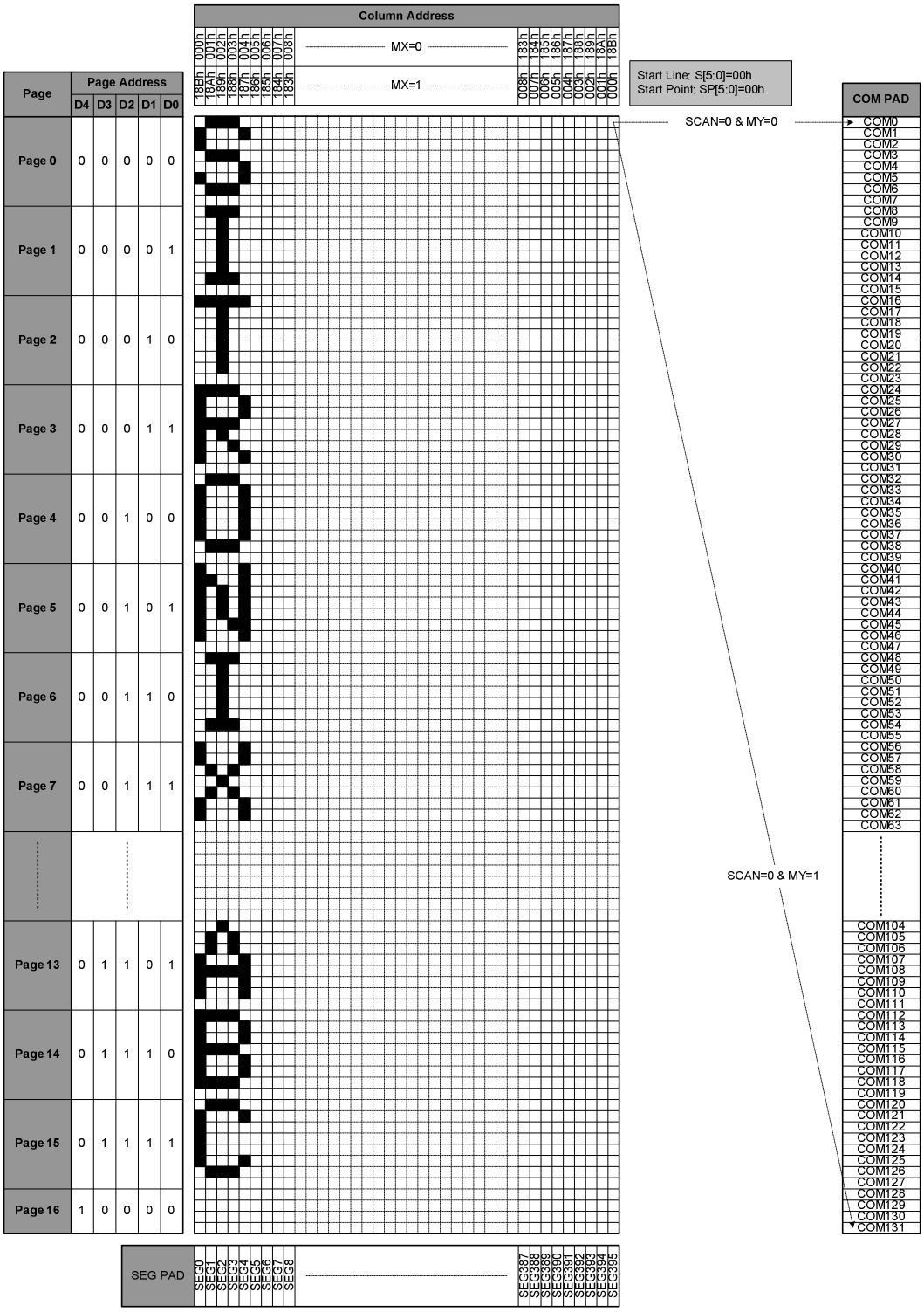


Fig. 10 DDRAM Display Direction (Normal Scan)

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (setting by instruction of Display Area Set) of the display. Therefore, by setting Line Address repeatedly, ST7592 is possible to realize the screen scrolling (4-lines basis) and page switching without changing the content of DDRAM as shown in Fig. 11.

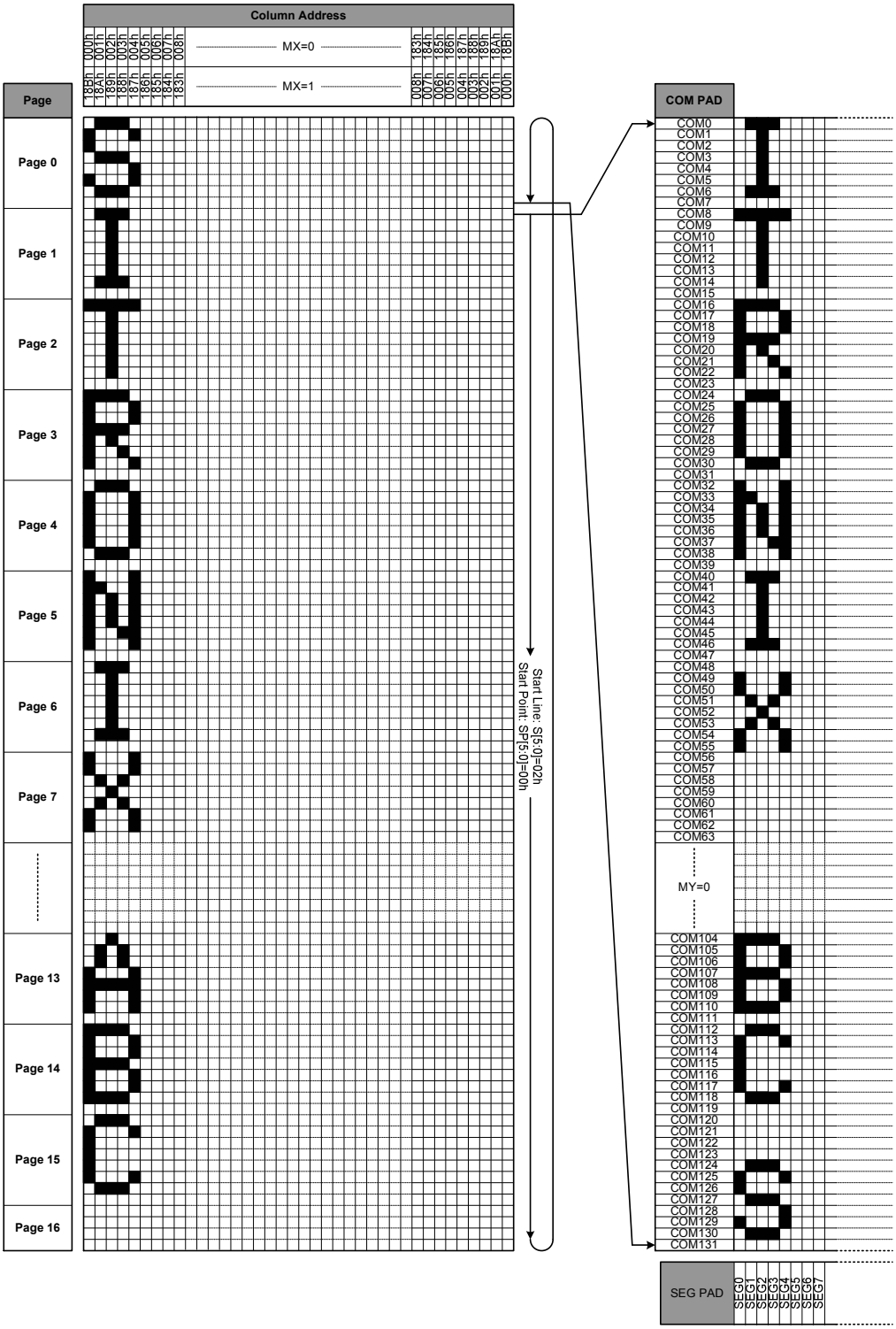


Fig. 11 Display Data RAM Map (1/132 Duty)

Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST7592 is OFF, a Power OFF procedure is needed. Please refer to the OPERATION FLOW section.

External Component of Power Circuit

The recommended external power components need thirteen capacitors. The detailed values of these thirteen capacitors are determined by panel size and loading.

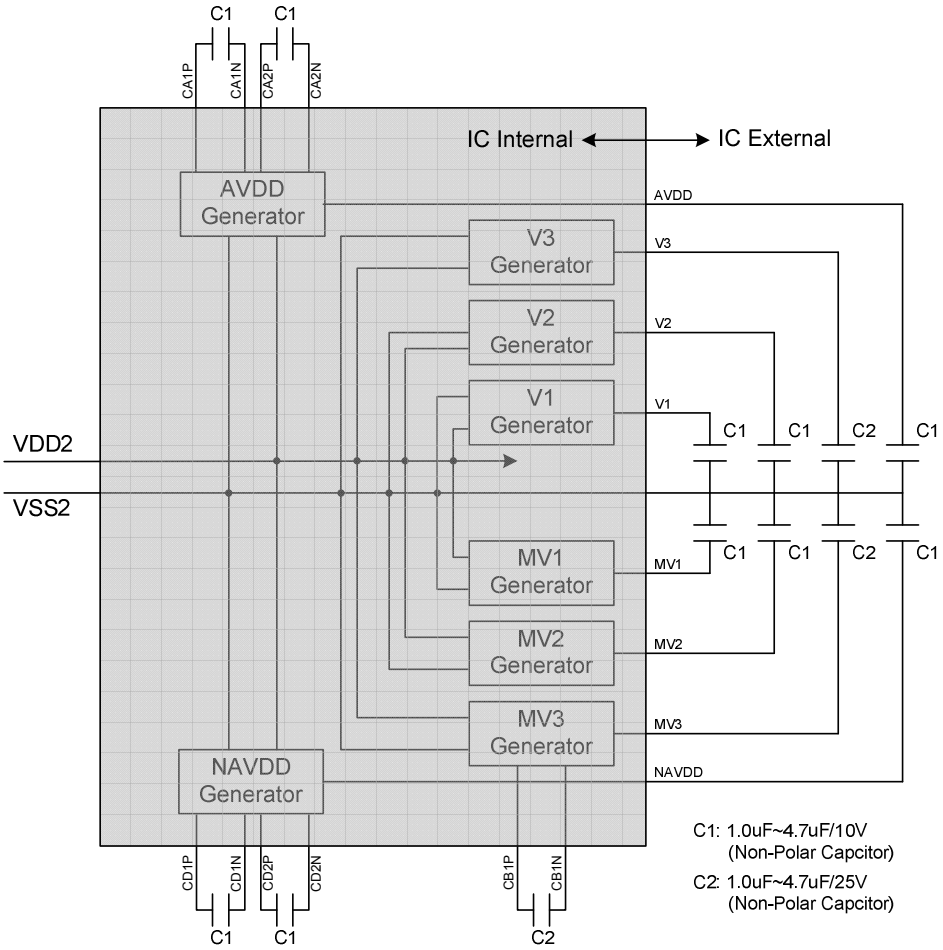


Fig. 12 Power Circuit

V3/MV3 Voltage Regulator

The built-in regulator regulates a stable voltage V3 and MV3. The voltage level of V3/MV3 can be programmed by software instruction. Besides software instruction, ST7592 also provide extra function to adjust the voltage level of V3/MV3, such as Voltage Offset and Temperature Component. The voltage level of V3/MV3 is controlled through the parameters of EV[8:0] and VOF[7:0]. EV[8:0] is set by software instruction and the VOF[7:0] is downloaded from PROM.

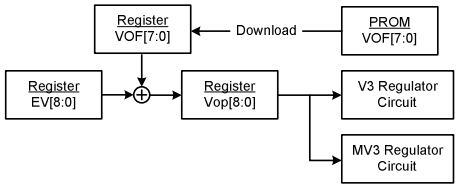


Fig. 13 V3/MV3 Generation

The V3/MV3 calculation formula is shown below. The default value of VOF[7:0] is 00h that download from PROM.

Vop[8:0] = EV[8:0] + VOF[7:0]

V3 = 6.0 + 0.02 x Vop[8:0] = 6.0 + 0.02 x (EV[8:0] + VOF[7:0])

MV3 = -6.0 – 0.02 x Vop[8:0] = -6.0 – 0.02 x (EV[8:0] + VOF[7:0])

LCD Vop = V3 – MV3

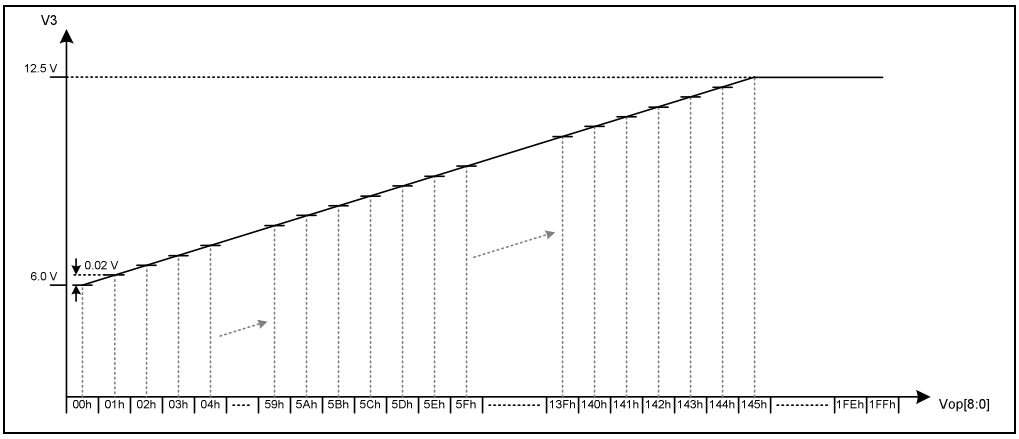


Fig. 14 V3 Programmable Range

The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2 voltage and the loading of LCD module. VOF[7:0] is 2's complement, so that VOF[7:0] can increase or decrease V3 and MV3 respectively. The value of Vop[8:0] will return to 000h while the value of Vop[8:0] add one step (+1) is over 1FFh.

VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	V3 Offset	MV3 Offset	Vop Offset
0	1	1	1	1	1	1	1	+2540 mV	-2540 mV	+5080 mV
	1	1	1	1	1	1	0	+2520 mV	-2520 mV	+5040 mV
	:	:	:	:	:	:	:	:	:	:
	0	0	0	0	0	1	0	+40 mV	-40 mV	+80 mV
	0	0	0	0	0	0	1	+20 mV	-20 mV	+40 mV
	0	0	0	0	0	0	0	0 mV	0mV	0 mV
1	1	1	1	1	1	1	1	-20 mV	+20 mV	-40 mV
	1	1	1	1	1	1	0	-40 mV	+40 mV	-80 mV
	:	:	:	:	:	:	:	:	:	:
	0	0	0	0	0	0	1	-2540 mV	+2540 mV	-5080 mV
	0	0	0	0	0	0	0	-2560 mV	+2560 mV	-5120 mV

BIAS Voltage Follower

The internal bias ratio resistors divide V3 and MV3 into four reference levels for V2, V1, MV1 and MV2. The BIAS Voltage Follower generates V2, V1, MV1 and MV2 according to these four reference levels. This circuit is operated in AVDD and NAVDD voltage system as the power source. The idea BIAS ratio is shown in below formula:

Idea BIAS ratio: BIAS=(Duty)$^{0.5}$

The available range for V2, V1, MV1 and MV2 is shown in below table.

Symbol	Available Range
V2	2.0V < V2 < AVDD-0.7V
V1	1.0V < V1 < V2
MV1	MV2 < MV1 < -1.0V
MV2	NAVDD+0.7V < MV2 < -2.0V

The bias ratio and available V3, MV3 and Vop are shown in below table.

BIAS	Available V3 Range	Available MV3 Range	Available Vop Range
1/6	6.0V ~ 6.45V	-6.45V ~ -6.0V	12.0V ~ 12.9V
1/7	6.0V ~ 7.525V	-7.525V ~ -6.0V	12.0V ~ 15.05V
1/8	6.0V ~ 8.6V	-8.6V ~ -6.0V	12.0V ~ 17.2V
1/9	6.0V ~ 9.675V	-9.675V ~ -6.0V	12.0V ~ 19.35V
1/10	6.0V ~ 10.75V	-10.75V ~ -6.0V	12.0V ~ 21.5V
1/11	6.0V ~ 11.825V	-11.825V ~ -6.0V	12.0V ~ 23.65V
1/12	6.0V ~ 12.5V	-12.5V ~ -6.0V	12.0V ~ 25.0V
1/13	6.5V ~ 12.5V	-12.5V ~ -6.5V	13.0V ~ 25.0V
1/14	7.0V ~ 12.5V	-12.5V ~ -7.0V	14.0V ~ 25.0V
1/15	7.5V ~ 12.5V	-12.5V ~ -7.5V	15.0V ~ 25.0V
1/16	8.0V ~ 12.5V	-12.5V ~ -8.0V	16.0V ~ 25.0V

Note:

1. The maximum voltage level of V3 or minimum voltage level of MV3 that can be generated is dependent on the VDD2, AVDD and the loading of LCD module.
2. The upper limit of the available Vop is absolutely voltage level without consider temperature compensation for V3 and MV3. The voltage level of Vop must be within “Available Vop Range” after considering temperature compensation for V3 and MV3.

For example, if we reserved -1V ~ +2.4V (Vop) for temperature compensation, the recommended power parameters are:

BIAS	Available V3 Range	Available MV3 Range	Available Vop Range
1/6 ~ 1/7			
1/8	6.5V ~ 7.4V	-7.4 ~ -6.5V	13.0V ~ 14.8
1/9	6.5V ~ 8.475V	-8.475V ~ -6.5V	13.0V ~ 16.95V
1/10	6.5V ~ 9.55V	-9.55V ~ -6.5V	13.0V ~ 19.1V
1/11	6.5V ~ 10.625V	-10.625V ~ -6.5V	13.0V ~ 21.25V
1/12	6.5V ~ 11.3V	-11.3V ~ -6.5V	13.0V ~ 22.6V
1/13	7.0V ~ 11.3V	-11.3V ~ -7.0V	14.0V ~ 22.6V
1/14	7.5V ~ 11.3V	-11.3V ~ -7.5V	15.0V ~ 22.6V
1/15	8.0V ~ 11.3V	-11.3V ~ -8.0V	16.0V ~ 22.6V
1/16	8.5V ~ 11.3V	-11.3V ~ -8.5V	17.0V ~ 22.6V

Power System Setup

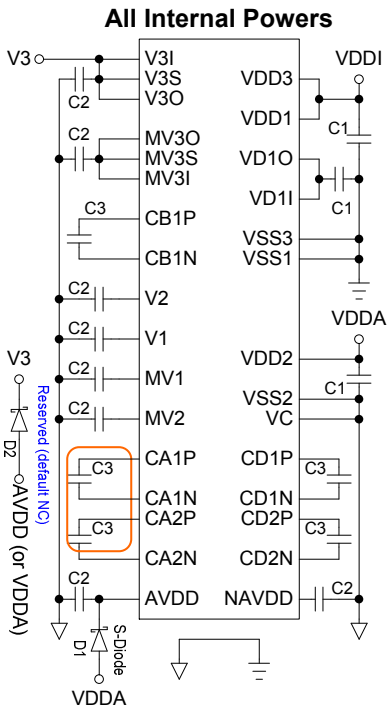
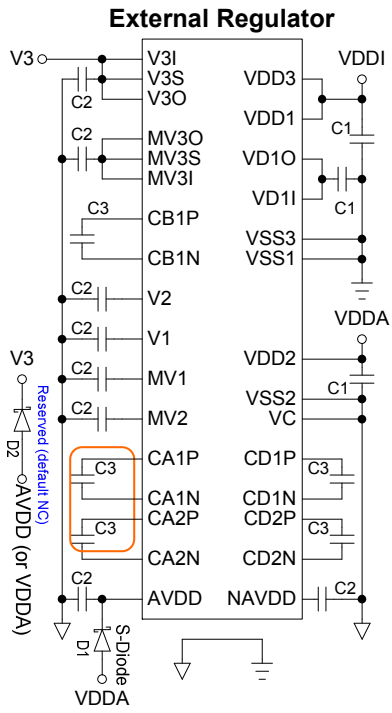
The power system of ST7592 can be constructed in different ways. The power system can use internal power circuits or external positive level power supplies. The combination of the internal power circuits or external positive level power supplies is also allowed. The power supplies of negative voltage level for negative power system are disallowed. The following table describes how to use the power system (internal or external). Be sure both of the hardware connection and software setting must be correct.

Software Setting for Power Control						Hardware Setting
VAD	V3	VPF	VMV3	VNAD	VNF	
1	-	-	-	-	-	**Internal AVDD** 1. Connect booster capacitor between CA1P and CA1N. 2. Connect booster capacitor between CA2P and CA2N. 3. Connect storage capacitor between AVDD and VSS2.
0	-	-	-	-	-	**External AVDD** 1. Connect storage capacitor between AVDD and VSS2. 2. Apply external voltage level to AVDD.
-	1	-	-	-	-	**Internal V3** 1. Connect storage capacitor between V3 and VSS2.
-	0	-	-	-	-	**External V3** 1. Connect storage capacitor between V3 and VSS2. 2. Apply external voltage level to V3.
-	-	1	-	-	-	**Internal Positive Follower** 1. Connect storage capacitor between V2 and VSS2. 2. Connect storage capacitor between V1 and VSS2.
-	-	0	-	-	-	**External Positive Follower** 1. Connect storage capacitor between V2 and VSS2. 2. Connect storage capacitor between V1 and VSS2. 3. Apply external voltage levels to V2 and V1.
-	-	-	1	1	1	**Internal NAVDD, MV3 and Negative Follower** 1. Connect booster capacitor between CD1P and CD1N. 2. Connect booster capacitor between CD2P and CD2N. 3. Connect storage capacitor between NAVDD and VSS2. 4. Connect booster capacitor between CB1P and CB1N. 5. Connect storage capacitor between MV3 and VSS2. 6. Connect storage capacitor between MV2 and VSS2. 7. Connect storage capacitor between MV1 and VSS2.

Note:

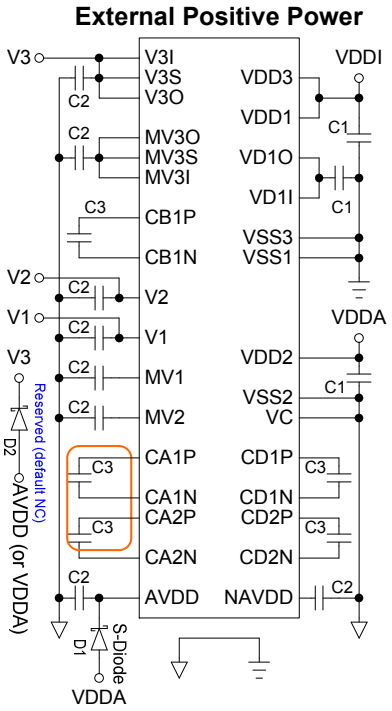
- Whether power on or power off sequence must according to section of System Power ON or Power OFF to avid abnormal phenomenon.

The following figures illustrate the connection of typical power applications.

Case 1: All Internal LCD Power Circuits	Case 2: External Regulator (V3)
[Hardware Connection] 	**[Hardware Connection]** 
[Software Setting] Power Control: V3=VPF=VMV3=VNAD=VNF=1 **[Optional Setting]** ● External AVDD: VAD=0 Remove 2 CAPs at CA1P/N, CA2P/N (for 5V system) ● Internal AVDD: VAD=1 Connect 2 CAPs at CA1P/N, CA2P/N (for 3.3V system) **[Related Features]** Contrast Control: Software Control Vop Adjustment: Adjust by Internal PROM BIAS Control: Software Control Vop Temperature Compensation: Software Defined fFR Temperature Compensation: Software Defined **The Schottky diode (D1) is always connected**. **The Schottky diode (D2) is reserved**.	**[Software Setting]** Power Control: V3=0, VPF=VMV3=VNAD=VNF=1 **[Optional Setting]** ● External AVDD: VAD=0 Remove 2 CAPs at CA1P/N, CA2P/N; (for 5V system) ● Internal AVDD: VAD=1 Connect 2 CAPs at CA1P/N, CA2P/N; (for 3.3V system) **[Related Features]** Contrast Control: External Circuit Vop Adjustment: External Circuit BIAS Control: Software Control Vop Temperature Compensation: External Circuit fFR Temperature Compensation: Software Defined **The Schottky diode (D1) is always connected**. **The Schottky diode (D2) is reserved**.
➢ The Schottky diode is used to isolate the AVDD noise and it also keeps AVDD power quality.	➢ The Schottky diode is used to isolate the AVDD noise and it also keeps AVDD power quality.

Case 3: External Regulator & Follower (V3 & VPF)

[Hardware Connection]



[Software Setting]

Power Control: V3=VPF=0, VMV3=VNAD=VNF=1

[Optional Setting]

- External AVDD: VAD=0
  Remove 2 CAPs at CA1P/N, CA2P/N;
  (for 5V system)
- Internal AVDD: VAD=1
  Connect 2 CAPs at CA1P/N, CA2P/N;
  (for 3.3V system)

[Related Features]

Contrast Control: External Circuit

Vop Adjustment: External Circuit

BIAS Control: External Circuit (Fixed)

Vop Temperature Compensation: External Circuit

fFR Temperature Compensation: Software Defined

The Schottky diode (D1) is always connected.

The Schottky diode (D2) is reserved.

This case uses only external positive power circuits.

➢ The Schottky diode is used to isolate the AVDD noise and it also keeps AVDD power quality.

External Components of Power Circuit

The optimum values of C1, C2 and C3 depend on the loading of LCD panel. The value should be determined by customer. When determining the capacitor value, customer can display a pattern with large loading and than check if the capacitor makes the voltage stable or not. The following table is a quick reference for the initial setting.

Symbol	Type	Reference Value (uF)
C1	Capacitor for supply voltage regulation	0.1 ~ 4.7
C2	Capacitor for LCD voltage stabilization	1.0 ~ 4.7
C3	Capacitor for booster	1.0 ~ 4.7

Note:

1. Please place all these capacitors close to the related pin of IC.
2. If the LCD panel is large or the ITO resistance is not good, the capacitor value maybe large than the reference value. If the value is more than 10uF, customer should consider the following suggestion.
3. When the LCD panel size is large and desired display quality is unavailable by increasing the value of capacitor, it is recommended to use the LCD related power externally.
4. The acceptable voltage level of each capacitor as shown in Application Circuit.

Temperature Gradient Selection Circuit

Set V3 with Temperature Compensation (Temperature ≠ 24℃)

There are 19-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8℃. Please see Fig. 15 as below.

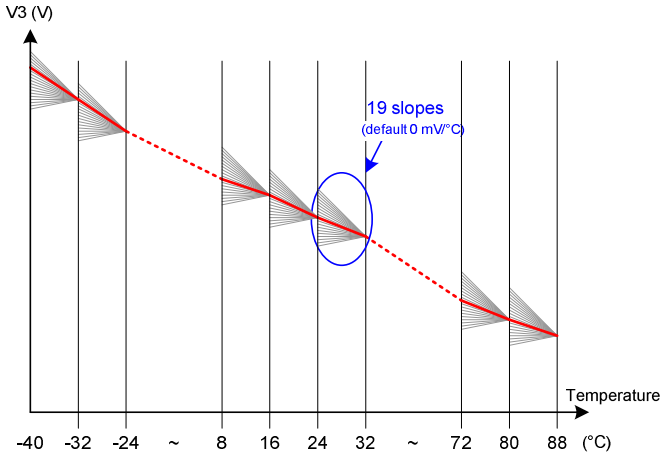


Fig. 15 Temperature Compensation Coefficient Selection

The temperature compensation circuit includes negative and positive temperature gradient slope coefficient. If the temperature gradient slope coefficient is negative (FMTx=0), the available gradient Mx is 0mV/℃, -5 mV/ ℃, -10 mV/℃, … and -75 mV/℃. The parameter (MTx) of Temperature Gr adient Set instruction where x=0, 1, 2, …, E, F has a setting value between 0 and 15. MTx=0 results in Mx=0 mV/℃ increm ent on V3, MTx=1 results in Mx=-5 mV/℃ increment, …, MTx=15 results in Mx=15x(-5) mV/℃ increment. If the temper ature gradient slope coefficient is positive (FMTx=1), the available gradient Mx is 0mV/℃, 5 mV/℃, 10 mV/℃ and 15 mV/℃. The parameter (MTx) of Temperature Gradient Set instruction where x=0, 1, 2, …, E, F has a setting value between 0 and 3. MTx=0 results in Mx=0 mV/℃ decrement on V 3, MTx=1 results in Mx=5 mV/℃ increment, MTx=2 results in Mx =10 mV/℃ increment and MTx=3 results in Mx=15 mV/℃ increment. Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V3 quantity due to temperature V3(T) are described in the equation shown in Table 3.

Temperature Range	Equation V0(T) at temperature=T℃
-40℃ ≤ T < -32℃	V3(T) = V3(T24) + (-32 – T) x M0 + (M1 + M2 + M3 + M4 + M5 + M6 + M7) x 8
-32℃ ≤ T < -24℃	V3(T) = V3(T24) + (-24 – T) x M1 + (M2 + M3 + M4 + M5 + M6 + M7) x 8
-24℃ ≤ T < -16℃	V3(T) = V3(T24) + (-16 – T) x M2 + (M3 + M4 + M5 + M6 + M7) x 8
-16℃ ≤ T < -8℃	V3(T) = V3(T24) + (-8 – T) x M3 + (M4 + M5 + M6 + M7) x 8
-8℃ ≤ T < 0℃	V3(T) = V3(T24) + (0 – T) x M4 + (M5 + M6 + M7) x 8
0℃ ≤ T < 8℃	V3(T) = V3(T24) + (8 – T) x M5 + (M6 + M7) x 8
8℃ ≤ T < 16℃	V3(T) = V3(T24) + (16 – T) x M6 + M7 x 8
16℃ ≤ T < 24℃	V3(T) = V3(T24) + (24 – T) x M7
24℃ ≤ T < 32℃	V3(T) = V3(T24) – (T – 24) x M8
32℃ ≤ T < 40℃	V3(T) = V3(T24) – (T – 32) x M9 – M8 x 8
40℃ ≤ T < 48℃	V3(T) = V3(T24) – (T – 40) x M10 – (M9 + M8) x 8
48℃ ≤ T < 56℃	V3(T) = V3(T24) – (T – 48) x M11 – (M10 + M9 + M8) x 8
56℃ ≤ T < 64℃	V3(T) = V3(T24) – (T – 56) x M12 – (M11 + M10 + M9 + M8) x 8
64℃ ≤ T < 72℃	V3(T) = V3(T24) – (T – 64) x M13 – (M12 + M11 + M10 + M9 + M8) x 8
72℃ ≤ T < 80℃	V3(T) = V3(T24) – (T – 72) x M14 – (M13 + M12 + M11 + M10 + M9 + M8) x 8
80℃ ≤ T < 88℃	V3(T) = V3(T24) – (T – 80) x M15 – (M14 + M13 + M12 + M11 + M10 + M9 + M8) x 8

Table 3

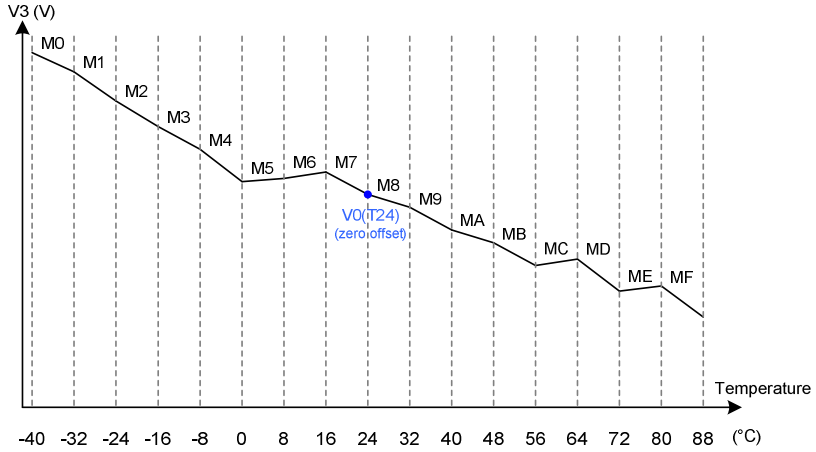


Fig. 16 Temperature Gradient Compensation

Note:

- Please make sure to avoid any kind of heating source near ST7592 such as back light, to prevent V3 is not anticipative because of temperature compensation circuit is working.

For example, Vop=18.6V, TC=-15mV/℃, the V3 (Vop) in 8~39℃ are listed below:

Range (Mx)	Parameter (MTn)	Flag (FMTn)	Slope (mV/℃)	Ta (℃)	V3 (V)	Vop (V)
:	:	:	:	:	:	:
M6	3	0	-15	8	9.540	19.08
				9	9.525	19.05
				10	9.510	19.02
				11	9.495	18.99
				12	9.480	18.96
				13	9.465	18.93
				14	9.450	18.90
				15	9.435	18.87
M7	3	0	-15	16	9.420	18.84
				17	9.405	18.81
				18	9.390	18.78
				19	9.375	18.75
				20	9.360	18.72
				21	9.345	18.69
				22	9.330	18.66
				23	9.315	18.63
M8	3	0	-15	24	9.300	18.60
				25	9.285	18.57
				26	9.270	18.54
				27	9.255	18.51
				28	9.270	18.54
				29	9.255	18.51
				30	9.240	18.48
				31	9.225	18.45
M9	3	0	-15	32	9.210	18.42
				33	9.195	18.39
				34	9.180	18.36
				35	9.165	18.33
				36	9.180	18.36
				37	9.165	18.33
				38	9.150	18.30
				39	9.135	18.27
:	:	:	:	:	:	:

Frequency Temperature Gradient Compensation Coefficient

ST7592 will auto-switch frame rate in different temperature such as Fig. 17. TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Set Frequency Compensation Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Operation Clock Frequency Select. The temperature hysteresis “THF” in the Fig. 17 that defines the sensitivity of internal temperature sensor and the value can be altered by instruction Temperature Hysteresis Value Set.

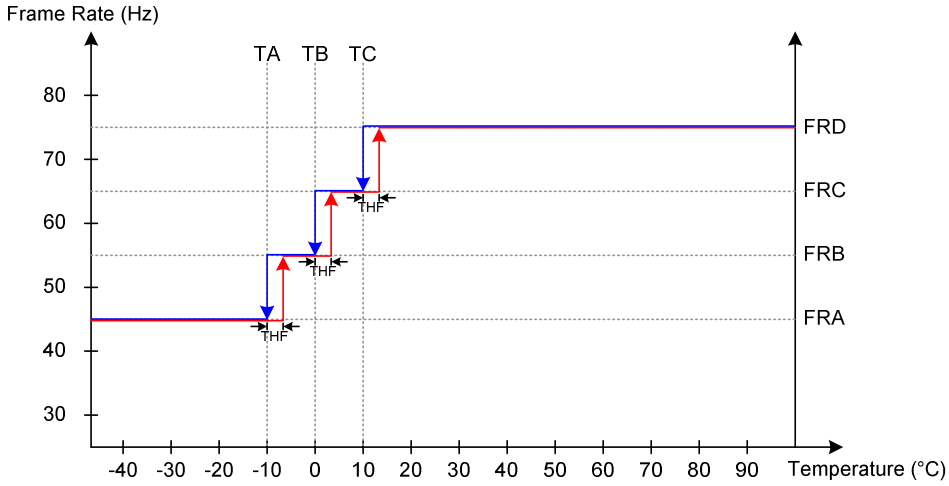


Fig. 17 Frame Rate

RESET CIRCUIT

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDD1 is not stable at the time that the system power is just turned ON. The hardware reset is required to initialize internal registers after VDD1 is stable. Initialization by RSTB pin is essential before operating. The default values of registers are listed below:

Procedure	After Hardware Reset
Content of DDRAM	No Change
Display ON/OFF	Display OFF
Display Inverse	Normal
Display All Pixel ON	Normal
COM Output Status	Normal Scan, COM0→COM131
Display Start Line	S[5:0]=00h
Page Address	Y[4:0]=00h
Column Address	X[8:0]=00h
Display Data Input/Output Direction	Column Direction
Column Address Direction	SEG0→SEG395
N-Line Inversion	NL[4:0]=00h
N-Line Inversion ON/FF	OFF
Display Area	DTY[5:0]=20h, SP[5:0]=00h
Read Modify Write	Disable
Built-in Oscillator Circuit ON/OFF	OFF
Operation Clock Frequency	FRx[3:0]=05h (FR=80Hz)
Power Control	All Power OFF
Booster Level	Booster Level1
BIAS	BS[3:0]=00h
Electronic Volume	EV[8:0]=00h
Power Discharge	All Discharge OFF
Power Save	Non-Standby Mode (Normal Mode)
Temperature Gradient Compensation	MTx[3:0]=00h
Temperature Gradient Compensation Flag	FMTx=00h
Temperature Detection	OFF
LCD Driving Method	NLFR=1
Frequency Compensation Temperature Range	Tx[6:0]=00h
Temperature Hysteresis Value	THV[3:0]=04h, THF[3:0]=02h
Test	Disable

Table 4

INSTRUCTION TABLE

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	Set LCD display mode D=0: display off D=1: display on
Display Inverse	0	0	1	0	1	0	0	1	1	INV	Set inverse display mode INV=0: normal display INV=1: inverse display
Display All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all pixel on mode AP=0: normal display AP=1: all pixel on
COM Output Status	0	0	1	1	0	0	0	1	0	0	Set COM output mode SCAN=0: normal scan SCAN=1: interlace scan MY=0: COM0→COM131 MY=1: COM131→COM0
	1	0	-	-	-	-	-	-	SCAN	MY	
Display Start Line	0	0	1	0	0	0	1	0	1	0	Set display start line
	1	0	-	-	S5	S4	S3	S2	S1	S0	
Page Address	0	0	1	0	1	1	0	0	0	1	Set the page address of DDRAM
	1	0	-	-	-	Y4	Y3	Y2	Y1	Y0	
Column Address	0	0	0	0	0	1	0	0	1	1	Set the column address of DDRAM
	1	0	-	-	-	-	-	-	-	X8	
	1	0	X7	X6	X5	X4	X3	X2	X1	X0	
Display Data Write	0	0	0	0	0	1	1	1	0	1	Write display data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Read	0	0	0	0	0	1	1	1	0	0	Read display data from DDRAM
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
Display Data Input/Output Direction	0	0	1	0	0	0	0	1	0	DIR	Set DDRAM data input direction DIR=0: column direction DIR=1: page direction
Column Address Direction	0	0	1	0	1	0	0	0	0	MX	Set column addressing direction MX=0: SEG0→SEG395 MX=1: SEG395→SEG0
N-Line Inversion	0	0	0	0	1	1	0	1	1	0	Set N-Line inversion
	1	0	-	-	-	NL4	NL3	NL2	NL1	NL0	
N-Line Inversion ON/OFF	0	0	1	1	1	0	0	1	0	NL	Set N-Line inversion mode NL=0: N-Line inversion off NL=1: N-Line inversion on
Display Area	0	0	0	1	1	0	1	1	0	1	Set the display area DTY[5:0]=00h~20h SP[5:0]=00h~20h
	1	0	-	-	DTY5	DTY4	DTY3	DTY2	DTY1	DTY0	
	1	0	-	-	SP5	SP4	SP3	SP2	SP1	SP0	
Read Modify Write	0	0	1	1	1	0	0	0	0	0	Enable Read Modify Write mode
Read Modify Write End	0	0	1	1	1	0	1	1	1	0	Disable Read Modify Write mode
Built-in Oscillator Circuit ON/OFF	0	0	1	0	1	0	1	0	1	OSC	Set built-in oscillator mode OSC=0: built-in oscillator off OSC=1: built-in oscillator on

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Operation Clock Frequency	0	0	0	1	0	1	1	1	1	1	Set frame rate in different temperature range
	1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
	1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	
Power Control	0	0	0	0	1	0	0	1	0	1	Set built-in power circuits on/off
	1	0	-	-	VAD	V3	VPF	VMV3	VNAD	VNF	
Booster Level	0	0	0	0	1	0	1	0	1	1	Set the level of built-in booster circuit
	1	0	-	-	-	-	-	-	0	BL	
BIAS	0	0	1	0	1	0	0	0	1	0	Set the bias ratio of liquid crystal driving voltage
	1	0	-	-	-	-	BS3	BS2	BS1	BS0	
Electronic Volume	0	0	1	0	0	0	0	0	0	1	Set the V3 level for liquid crystal driving voltage
	1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
	1	0	-	-	-	-	-	-	-	EV8	
Power Discharge	0	0	1	1	1	0	1	0	1	0	Set power circuits discharge
	1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	
Power Save	0	0	1	0	1	0	1	0	0	PD	Set power save mode PD=0: normal mode PD=1: standby mode
Temperature Gradient Compensation	0	0	0	1	0	0	1	1	1	0	Set temperature gradient compensation coefficient
	1	0	MT1[3:0]				MT0[3:0]				
	1	0	MT3[3:0]				MT2[3:0]				
	1	0	MT5[3:0]				MT4[3:0]				
	1	0	MT7[3:0]				MT6[3:0]				
	1	0	MT9[3:0]				MT8[3:0]				
	1	0	MTB[3:0]				MTA[3:0]				
	1	0	MTD[3:0]				MTC[3:0]				
	1	0	MTF[3:0]				MTE[3:0]				
Temperature Gradient Compensation Flag	0	0	0	0	1	1	1	0	0	1	Set the slope of temperature gradient is positive or negative
	1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
	1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	
Read Status	0	0	1	0	0	0	1	1	1	0	Read IC status
	1	1	D	OSC	AVD	V3	VPF	VMV3	VNAD	VNF	
	1	1	DISV	SCAN	MY	PD	TD	NLFR	-	-	
Temperature Detection	0	0	0	1	1	0	1	0	0	TD	Set temperature detection mode TD=0: disable mode TD=1: enable mode
LCD Driving Method	0	0	1	1	1	0	0	1	1	1	Set LCD driving method
	1	0	-	-	-	NLFR	1	-	-	1	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Frequency Compensation Temperature Range	0	0	1	1	1	0	1	1	0	0	Set temperature range for frequency compensation
	1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Hysteresis Value	0	0	1	1	1	0	1	1	0	1	Set temperature hysteresis value
	1	0	-	-	0	0	THV3	THV2	THV1	THV0	
	1	0	-	-	-	-	THF3	THF2	THF1	THD0	
Current Temperature	0	0	1	1	1	0	1	1	1	1	Monitor current temperature
	1	1	T7	T6	T5	T4	T3	T2	T1	T0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode TE=0: normal command mode TE=1: test command mode T: select test command mode

INSTRUCTION DESCRIPTION

Display ON/OFF

This instruction turns the display ON or OFF. When ST7592 enters display off, the display output is blank regardless of the content of DDRAM. When ST7592 enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	1	1	D	D=0: Display off (Default) D=1: Display on

Display Inverse

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	1	INV	INV=0: Normal display (Default) INV=1: Inverse display

Display All Pixel ON

When ST7592 enters all pixels on mode, all display pixels are turned on regardless of the content of DDRAM. The content of DDRAM is not changed by setting Display All Pixel ON.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	0	AP	AP=0: Normal display (Default) AP=1: All pixel on

COM Output Status

This instruction defines the COM scan method and the direction of scan read from DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	0	1	0	0	SCAN=0: Normal scan (Default) SCAN=1: Interlace scan
1	0	-	-	-	-	-	-	SCAN	MY	MY=0: COM0→COM131 (Default) MY=1: COM131→COM0

Note: "-" is disable bit. It can be either logic 0 or 1.

For ITO layout, a quick reference map is shown in below table:

DDRAM	SCAN	MY	Group 1				Group 2				Group 3				Group 4			
Scan	0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Direction	0	1	131	130	129	128	127	126	125	124	123	122	121	120	119	118	117	116
to	1	0	0	1	2	3	68	69	70	71	4	5	6	7	72	73	74	75
COMx	1	1	67	66	65	64	131	130	129	128	63	62	61	60	127	126	125	124

Group 5				Group 6				Group 7				Group 8				Group 9			
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
115	114	113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
8	9	10	11	76	77	78	79	12	13	14	15	80	81	82	83	16	17	18	19
59	58	57	56	123	122	121	120	55	54	53	52	119	118	117	116	51	50	49	48

Group 10				Group 11				Group 12				Group 13				Group 14			
36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76
84	85	86	87	20	21	22	23	88	89	90	91	24	25	26	27	92	93	94	95
115	114	113	112	47	46	45	44	111	110	109	108	43	42	41	40	107	106	105	104

Group 15				Group 16				Group 17				Group 18				Group 19			
56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56
28	29	30	31	96	97	98	99	32	33	34	35	100	101	102	103	36	37	38	39
39	38	37	36	103	102	101	100	35	34	33	32	99	98	97	96	31	30	29	28

Group 20				Group 21				Group 22				Group 23				Group 24			
76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
104	105	106	107	40	41	42	43	108	109	110	111	44	45	46	47	112	113	114	115
95	94	93	92	27	26	25	24	91	90	89	88	23	22	21	20	87	86	85	84

Group 25				Group 26				Group 27				Group 28				Group 29			
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115
35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
48	49	50	51	116	117	118	119	52	53	54	55	120	121	122	123	56	57	58	59
19	18	17	16	83	82	81	80	15	14	13	12	79	78	77	76	11	10	9	8

Group 30				Group 31				Group 32				Group 33			
116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
124	125	126	127	60	61	62	63	128	129	130	131	64	65	66	67
75	74	73	72	7	6	5	4	71	70	69	68	3	2	1	0

Display Start Line

This instruction sets the display start line address of DDRAM shown in Fig. 11. The display data of specified display start line address is displayed at the start point (start point is specified by instruction Display Area). Continuously increasing or decreasing the start line address results in vertical-scrolling in 4-line basis. The detail description is showed in the section of Line Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	0	1	0	S[5:0]=00h~20h
1	0	-	-	S5	S4	S3	S2	S1	S0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter S[5:0] and the line address of DDRAM is shown below.

S5	S4	S3	S2	S1	S0	Line Address of DDRAM
0	0	0	0	0	0	0 x 4 = 0 (Default)
0	0	0	0	0	1	1 x 4 = 4
0	0	0	0	1	0	2 x 4 = 8
:	:	:	:	:	:	:
0	1	1	1	1	0	30 x 4 = 120
0	1	1	1	1	1	31 x 4 =124
1	0	0	0	0	0	32 x 4 = 128

Page Address

This instruction defines the page address corresponding to line address of DDRAM when MCU access to the DDRAM shown in Fig. 10. The detail description is showed in the section of Page Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	0	0	0	1	Y[4:0]=00h~10h
1	0	-	-	-	Y4	Y3	Y2	Y1	Y0	

Note: "-" is disable bit. It can be either logic 0 or 1.

Y4	Y3	Y2	Y1	Y0	Page Address
0	0	0	0	0	Page 0
0	0	0	0	1	Page 1
0	0	0	1	0	Page 2
:	:	:	:	:	:
0	1	1	1	0	Page 14
0	1	1	1	1	Page 15
1	0	0	0	0	Page16

Column Address

This instruction defines the column address of DDRAM. The detail description is showed in the section of Column Address Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	0	1	1	X[8:0]=00h~18Bh
1	0	-	-	-	-	-	-	-	X8	
1	0	X7	X6	X5	X4	X3	X2	X1	X0	

Note: "-" is disable bit. It can be either logic 0 or 1.

X8	X7	X6	X5	X4	X3	X2	X1	X0	Column Address
0	0	0	0	0	0	0	0	0	Column 0
0	0	0	0	0	0	0	0	1	Column 1
0	0	0	0	0	0	0	1	0	Column 2
:	:	:	:	:	:	:	:	:	:
1	1	0	0	0	1	0	0	1	Column 393
1	1	0	0	0	1	0	1	0	Column 394
1	1	0	0	0	1	0	1	1	Column 395

Display Data Write

This instruction is used to transfer data from MCU to DDRAM without changing status of ST7592. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Display Data Write would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	1	
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

Display Data Read

The instruction is used to transfer data from DDRAM to MCU without changing status of ST7592. The page address and column address will be reset to customer setting when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. After each access, column address counter or page address counter is automatically increased by one (+1). The increment method of page address counter or column address counter is depending on instruction Display Data Input Direction. Read Display Data would be stopped when any other instruction is accepted. Read Display Data is only available via the parallel interface.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	1	1	0	0	
1	1	D7	D6	D5	D4	D3	D2	D1	D0	

Display Data Input/Output Direction

This instruction defines the direction where the address counter of DDRAM is automatically increment. The detail description is showed in the section of Addressing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	1	0	DIR	DIR=0: Column direction (Default) DIR=1: Page direction

Column Address Direction

This instruction defines the addressing direction of column address as shown in Fig. 10.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	0	MX	MX=0: SEG0→SEG395 (Default) MX=1: SEG395→SEG0

N-Line Inversion

This instruction defines the liquid crystal alternating line number which alters the driving signal phase (in 4-line basis).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	1	1	0	NL[4:0]=00h~1Fh
1	0	-	-	-	NL4	NL3	NL2	NL1	NL0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter NL[4:0] and the number of inverted lines is shown below.

NL4	NL3	NL2	NL1	NL0	N-Line Inversion
0	0	0	0	0	8 (4x2)
0	0	0	0	1	8 (4x2)
0	0	0	1	0	12 (4x3)
:	:	:	:	:	:
1	1	1	0	1	120 (4x30)
1	1	1	1	0	124 (4x31)
1	1	1	1	1	128 (4x32)

N-Line Inversion ON/OFF

This instruction defines the function of N-Line inversion is disable or enable. If the N-Line inversion is turning off, the liquid crystal is alternated by frame inversion.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	NL	NL=0: N-Line inversion off (Default) NL=1: N-Line inversion on

Display Area

This instruction defines the display duty and the start point (in 4-line basis). The display duty is specified the number of display line in 4-line basis. The start point is specified the first output COM number that mapping to Display Start Line of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	1	0	1	DTY[5:0]=00h~20h SP[5:0]=00h~20h
1	0	-	-	DTY5	DTY4	DTY3	DTY2	DTY1	DTY0	
1	0	-	-	SP5	SP4	SP3	SP2	SP1	SP0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter DTY[5:0] and the number of display lines is shown below.

DTY5	DTY4	DTY3	DTY2	DTY1	DTY0	Display Duty	Scan Duty
0	0	0	0	0	0	1/8	1/64
0	0	0	0	0	1	1/8	1/64
0	0	0	0	1	0	1/12	1/64
:	:	:	:	:	:	:	:
0	0	1	1	1	1	1/64	1/64
:	:	:	:	:	:	:	:
0	1	1	1	1	0	1/124	1/124
0	1	1	1	1	1	1/128	1/128
1	0	0	0	0	0	1/132	1/132

The relationship between the parameter SP[5:0] and the start point is shown below.

SP5	SP4	SP3	SP2	SP1	SP0	Start Point
0	0	0	0	0	0	0 (COM0~COM3)
0	0	0	0	0	1	1 (COM4~COM7)
0	0	0	0	1	0	2 (COM8~COM11)
:	:	:	:	:	:	:
0	1	1	1	1	0	30(COM120~COM123)
0	1	1	1	1	1	31 (COM124~COM127)
1	0	0	0	0	0	32 (COM128~COM131)

Read Modify Write

This instruction is used to enter Read Modify Write mode. When entering Read Modify Write mode, the display data read will not increase address counter. Only the display data write will increase the address counter. This mode is maintained until the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	

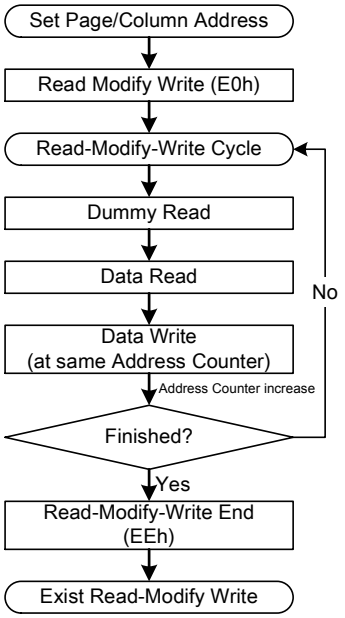


Fig. 18 Read Modify Write Flow

Read Modify Write End

This instruction is used to release the Read Modify Write mode. The page address and column address will return to initial address while the instruction Read Modify Write End is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	0	

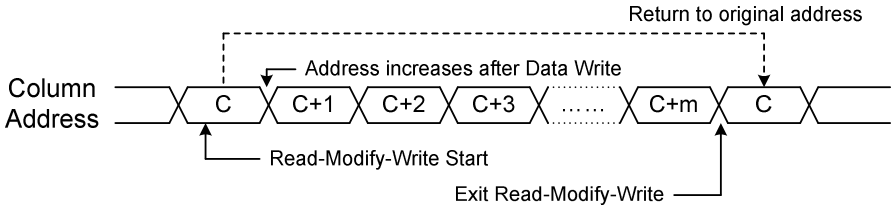


Fig. 19 Address Relationship of Read Modify Write

Built-in Oscillator Circuit ON/OFF

This instruction is used to turn on or off the built-in oscillator circuit. When the built-in power supply is used, the Built-in Oscillator Circuit ON must be executed before the instruction Power Control. If the built-in oscillator circuit is turned off while the built-in power supply is used, abnormal display may occur.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	OSC	OSC=0: Built-in oscillator off OSC=1: Built-in oscillator on

Operation Clock Frequency

This instruction defines the temperature compensation gradient of frequency which automatically adjusts the frame frequency according to the current temperature.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	1	1	FRA[3:0]: FR for -40℃~TA FRB[3:0]: FR for TA~TB FRC[3:0]: FR for TB~TC FRD[3:0]: FR for TC~88℃
1	0	FRB3	FRB2	FRB1	FRB0	FRA3	FRA2	FRA1	FRA0	
1	0	FRD3	FRD2	FRD1	FRD0	FRC3	FRC2	FRC1	FRC0	

This instruction is used to specify the divide-ratio of the internal operation clock (PWMCK) to the built-in oscillator frequency (fOSC). This instruction is enable only when built-in oscillator clock is turned on. If the built-in oscillator circuit is turned off, the external clock entered to CL pin is used as the internal operation clock. The below table shows the relation between the divide-ratio and the register value which is set by the parameter (FRx[3:1]). This table also illustrates the relation between the internal operation clock (PWMCK) and the display operation clock (fDCLK).

FRx[3:1]	DIV	PWMCK (kHz) fOSC/DIV	fDCLK (kHz) PWMCK/15	fFR (Hz)					
				132 Lines	120 Lines	104 Lines	92 Lines	80 Lines	64 Lines
0000	5	326.0	21.7	160	175	201	226	258	319
0001	6	271.7	18.1	133	146	168	189	215	266
0010	7	232.9	15.5	114	125	144	161	185	228
0011	8	203.8	13.6	100	110	126	142	162	200
0100	9	181.1	12.1	89	98	112	126	144	178
0101	10	163.0	10.9	80	88	101	114	130	160
0110	12	135.8	9.1	67	73	84	95	108	134
0111	14	116.4	7.8	57	63	72	81	93	115
1000	15	108.7	7.2	53	58	67	75	86	106
1001	16	101.9	6.8	50	55	63	71	81	100
1010	18	90.6	6.0	44	48	56	63	71	88
1011	20	81.5	5.4	40	44	50	56	64	79
1100	21	77.6	5.2	38	42	48	54	62	76
1101	24	67.9	4.5	33	36	42	47	54	66
1110	25	65.2	4.3	32	35	40	45	51	63
1111	28	58.2	3.9	29	31	36	41	46	57

Note:

fOSC: Oscillator frequency of the built-in oscillator circuit.

PWMCK: Internal operation clock. It is the basic clock used by the synchronous circuit of ST7592. PWMCK is obtained by dividing fOSC.

fDCLK: Display Operation Clock. It is used to specify a single duration in the sequential drive of liquid crystal. It constantly meets the relation of PWMCK/15 independent of the value of the operation clock frequency select command. The relationship will not change even when the external clock is used.

fFR: The frequency of Frame Rate.

Power Control

This instruction used to control the status of built-in power circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	1	0	1	
1	0	-	-	VAD	V3	VPF	VMV3	VNAD	VNF	

Note: "-" is disable bit. It can be either logic 0 or 1.

ST7592 provides built-in power supply for LCD driving voltage. ST7592 allows using some part(s) of the built-in power circuit(s) with some external voltage(s). The following table shows how these circuits can be controlled through this command. The detail description of power circuit setup is showed in Power System Setup. The power on/off flow please refers to the sections of System Power ON and Power OFF to avoid abnormal display.

Flag	Status of Built-in Power Circuit
VAD	VAD=0: Built-in AVDD Booster Circuit OFF VAD=1: Built-in AVDD Booster Circuit ON
V3	V3=0: Built-in V3 Regulator Circuit OFF V3=1: Built-in V3 Regulator Circuit ON
VPF	VPF=0: Built-in Positive Follower Circuit OFF VPF=1: Built-in Positive Follower Circuit ON
VMV3	VMV3=0: Built-in MV3 Regulator Circuit OFF VMV3=1: Built-in MV3 Regulator Circuit ON
VNAD	VNAD=0: Built-in NAVDD Booster Circuit OFF VNAD=1: Built-in NAVDD Booster Circuit ON
VNF	VNF=0: Built-in Negative Follower Circuit OFF VNF=1: Built-in Negative Follower Circuit ON

The internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside. If the built-in oscillator circuit is used, please execute the built-in oscillator circuit turning on before the power circuit turning on. If the external oscillator is used, must operate the external oscillator before the power circuit turning on. If the internal clock is cut off during the operation of the built-in power circuit, abnormal display mat occur.

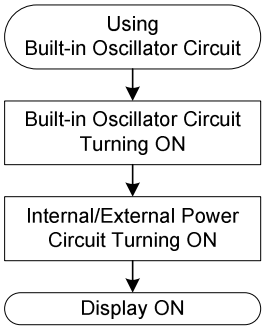


Fig. 20 Power Control (Using Built-in Oscillator)

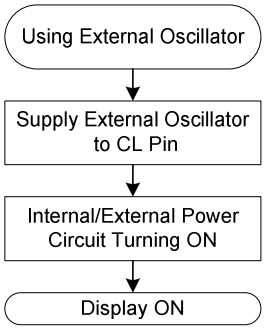


Fig. 21 Power Control (Using External Oscillator)

Booster Level

This instruction defines the booster level without change any hardware connection.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	1	0	1	1	BL=0: Booster Level 1
1	0	-	-	-	-	-	-	0	BL	BL=1: Reserved for testing

Note: "-" is disable bit. It can be either logic 0 or 1.

BIAS

This instruction defines the bias ratio of voltage requirement for liquid crystal.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	0	1	0	
1	0	-	-	-	-	BS3	BS2	BS1	BS0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter BS[3:0] and the bias ratio is shown below.

BS3	BS2	BS1	BS0	BIAS Ratio
0	0	0	0	1/6
0	0	0	1	1/7
0	0	1	0	1/8
0	0	1	1	1/9
0	1	0	0	1/10
0	1	0	1	1/11
0	1	1	0	1/12
0	1	1	1	1/13
1	0	0	0	1/14
1	0	0	1	1/15
1	0	1	0	1/16

The relationship between the bias ratio and the analog voltage level is shown below.

Symbol	Voltage Level
V3	V3 = Vop/2
V2	V2 = 2 x BIAS x Vop
V1	V1 = BIAS x Vop
VC	VC = VSS2
MV1	MV1 = -BIAS x Vop
MV2	MV2 = -2 x BIAS x Vop
MV3	MV3 = -Vop/2

Note: The limitation of analog voltage is shown in section of BIAS Voltage Follower.

Electronic Volume

This instruction defines the liquid crystal driving voltage V3 that issued from built-in analog power circuit. The maximum voltage level of Vop that can be generated is dependent on the VDD2 voltage and the loading of LCD module. The detail description is showed in section of V3/MV3 Voltage Regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	0	0	1	EV[8:0]=00h~145h
1	0	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
1	0	-	-	-	-	-	-	-	EV8	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter EV[8:0] and the voltage level of V3/MV3/Vop is shown below.

EV8	EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	V3	MV3	Vop
0	0	0	0	0	0	0	0	0	6.00	-6.00	12
0	0	0	0	0	0	0	0	1	6.02	-6.02	12.04
0	0	0	0	0	0	0	1	0	6.04	-6.04	12.08
:	:	:	:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	0	1	1	12.46	-12.46	24.92
1	0	1	0	0	0	1	0	0	12.48	-12.48	24.96
1	0	1	0	0	0	1	0	1	12.50	-12.50	25.00
1	0	1	0	0	0	1	1	0	12.50	-12.50	25.00
:	:	:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	0	12.50	-12.50	25.00
1	1	1	1	1	1	1	1	1	12.50	-12.50	25.00

Note: The formula of idea Vop is shown in section of V3/MV3 Voltage Regulator.

Power Discharge

This instruction used to discharge the capacitor connected to the analog power supply circuit. The discharge flow please refers to the sections of Power OFF to avoid abnormal display.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	0	1	0	
1	0	-	-	-	-	DV3	DVPF	DVNF	DVMV3	

Flag	Status of Built-in Power Circuit
DV3	DV3=0: Disable discharge V3 DV3=1: Enable discharge V3
DVPF	DVPF=0: Disable discharge positive follower (V2 & V1) DVPF=1: Enable discharge positive follower (V2 & V1)
DVNF	DVNF=0: Disable discharge negative follower (MV1 & MV2) and NAVDD DVNF=1: Enable discharge negative follower (MV1 & MV2) and NAVDD
DVMV3	DVMV3=0: Disable discharge MV3 DVMV3=1: Enable discharge MV3

Note:

1. Do not discharge before related power is turned off while using internal power system.
2. Do not discharge before related power is turned off while using external power system.

Power Save

This instruction defines the status of chip is normal mode or standby mode. When ST7592 enters the standby mode, the mode causes the LCD module entering the minimum power consumption. Besides, the internal analog circuit will be turned off without discharge power and the display will turn off.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	PD	PD=0: Normal mode PD=1: Standby mode

Temperature Gradient Compensation

This instruction defines the temperature gradient compensation coefficient. Depend on the instruction of Temperature Gradient Compensation Flag, the temperature gradient slope can be set either positive or negative. The detail description is showed in the section of Temperature Gradient Selection Circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	1	1	1	0	MTx[3:0]=0h~Fh (Negative TC) MTx[3:0]=0h~3h (Positive TC)
1	0	MT1[3:0]				MT0[3:0]				
1	0	MT3[3:0]				MT2[3:0]				
1	0	MT5[3:0]				MT4[3:0]				
1	0	MT7[3:0]				MT6[3:0]				
1	0	MT9[3:0]				MT8[3:0]				
1	0	MTB[3:0]				MTA[3:0]				
1	0	MTD[3:0]				MTC[3:0]				
1	0	MTF[3:0]				MTE[3:0]				

The related temperature range and available setting value of MTx[3:0] is shown below.

Flag	Temperature Range	Negative TC Value	Positive TC Value
MT0[3:0]	-40℃ ≤ T < -32℃	0h~Fh	0h~3h
MT1[3:0]	-32℃ ≤ T < -24℃	0h~Fh	0h~3h
MT2[3:0]	-24℃ ≤ T < -16℃	0h~Fh	0h~3h
MT3[3:0]	-16℃ ≤ T < -8℃	0h~Fh	0h~3h
MT4[3:0]	-8℃ ≤ T < 0℃	0h~Fh	0h~3h
MT5[3:0]	0℃ ≤ T < 8℃	0h~Fh	0h~3h
MT6[3:0]	8℃ ≤ T < 16℃	0h~Fh	0h~3h
MT7[3:0]	16℃ ≤ T < 24℃	0h~Fh	0h~3h
MT8[3:0]	24℃ ≤ T < 32℃	0h~Fh	0h~3h
MT9[3:0]	32℃ ≤ T < 40℃	0h~Fh	0h~3h
MTA[3:0]	40℃ ≤ T < 48℃	0h~Fh	0h~3h
MTB[3:0]	48℃ ≤ T < 56℃	0h~Fh	0h~3h
MTC[3:0]	56℃ ≤ T < 64℃	0h~Fh	0h~3h
MTD[3:0]	64℃ ≤ T < 72℃	0h~Fh	0h~3h
MTE[3:0]	72℃ ≤ T < 80℃	0h~Fh	0h~3h
MTF[3:0]	80℃ ≤ T < 88℃	0h~Fh	0h~3h

The relationship between the parameters FMTx/MTx[3:0] and the voltage level of V3/MV3/Vop is shown below. The FMTx is set by instruction of Temperature Gradient Compensation Flag.

FMTx	MTx3	MTx2	MTx1	MTx0	V3(mV/℃)	MV3(mV/℃)	Vop(mV/℃)
0	0	0	0	0	0	0	0
	0	0	0	1	-5	5	-10
	0	0	1	0	-10	10	-20
	0	0	1	1	-15	15	-30
	0	1	0	0	-20	20	-40
	0	1	0	1	-25	25	-50
	0	1	1	0	-30	30	-60
	0	1	1	1	-35	35	-70
	1	0	0	0	-40	40	-80
	1	0	0	1	-45	45	-90
	1	0	1	0	-50	50	-100
	1	0	1	1	-55	55	-110
	1	1	0	0	-60	60	-120
	1	1	0	1	-65	65	-130
	1	1	1	0	-70	70	-140
	1	1	1	1	-75	75	-150
1	0	0	0	0	0	0	0
	0	0	0	1	5	-5	10
	0	0	1	0	10	-10	20
	0	0	1	1	15	-15	30

Temperature Gradient Compensation Flag

This instruction defines the temperature gradient compensation coefficient is negative or positive temperature gradient compensation coefficient.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	1	0	0	1	FMTx=0: Negative TC FMTx=1: Positive TC
1	0	FMT7	FMT6	FMT5	FMT4	FMT3	FMT2	FMT1	FMT0	
1	0	FMTF	FMTE	FMTD	FMTC	FMTB	FMTA	FMT9	FMT8	

Read Status

This instruction can read out the status of ST7592.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	1	1	1	0	
1	1	D	OSC	AVD	V3	VPF	VMV3	VNAD	VNF	
1	1	DISV	SCAN	MY	PD	TD	NLFR	-	-	

The relationship between the flag and the status of IC is shown below.

Flag	Function	0	1
D	Display ON/OFF	OFF	ON
OSC	Built-in OSC Circuit ON/OFF	OFF	ON
AVD	AVDD ON/OFF	OFF	ON
V3	V3 ON/OFF	OFF	ON
VPF	Positive Follower ON/OFF	OFF	ON
VMV3	MV3 ON/OFF	OFF	ON
VNAD	NAVDD ON/OFF	OFF	ON
VNF	Negative Follower ON/OFF	OFF	ON
DISV	Power Discharge ON/OFF	OFF	ON
SCAN	COM Output Mode	Normal	Interlace
MY	COM Output Direction	Normal	Reverse
PD	Power Save	Normal	Standby
TD	Temperature Detection ON/OFF	OFF	ON
NLFR	N-Line Inversion Reset by Frame ON/OFF	ON	OFF

Temperature Detection

This instruction defines the status of temperature detection. All temperature related functions will be disabled if TD=0. If temperature detection and compensation is not used, please set TD=0, MTn[3:0]=0 and FRA=FRB=FRC=FRD=0.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	0	1	0	0	TD	TD=0: Disable mode TD=1: Enable mode

LCD Driving Method

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	1	1	
1	0	-	-	-	NLFR	1	-	-	1	

Note: “-“ is disable bit. It can be either logic 0 or 1.

Flag	Status
NLFR	NLFR=0: N-Line Inversion Reset by Frame Inversion ON NLFR=1: N-Line Inversion Reset by Frame Inversion OFF

The relationship between parameters (NL & NLFR) and COM output method is shown below.

A. 20 lines display without N-Line inversion (NL=0, NLFR=x)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			+ + + +					- - - -		
COM[15:12]				+ + + +					- - - -	
COM[19:16]					+ + + +					- - - -

B. 12-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					+ + + +			
COM[11:8]			+ + + +					+ + + +		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					- - - -					- - - -

C. 8-Line inversion in 20 lines display without frame inversion (NL=1, NLFR=1)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					+ + + +				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			- - - -					- - - -		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					+ + + +					+ + + +

D. 12-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			+ + + +					- - - -		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					- - - -					+ + + +

E. 8-Line inversion in 20 lines display with frame inversion (NL=1, NLFR=0)

COM	Positive Frame					Negative Frame				
COM[3:0]	+ + + +					- - - -				
COM[7:4]		+ + + +					- - - -			
COM[11:8]			- - - -					+ + + +		
COM[15:12]				- - - -					+ + + +	
COM[19:16]					+ + + +					- - - -

NOP

"No Operation" instruction. ST7592 will do nothing when receiving this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	1	No operation

Frequency Compensation Temperature Range

This instruction defines the temperature range for automatic frame rate adjustment according to current temperature as shown in Fig. 17.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	0	TA[6:0]=09h~76h
1	0	-	TA6	TA5	TA4	TA3	TA2	TA1	TA0	TB[6:0]=09h~76h
1	0	-	TB6	TB5	TB4	TB3	TB2	TB1	TB0	TC[6:0]=09h~76h
1	0	-	TC6	TC5	TC4	TC3	TC2	TC1	TC0	TA<TB-8 and TB<TC-8

Note: "-" is disable bit. It can be either logic 0 or 1.

The target temperature add 40 will become the decimal value of register TA[6:0]/TB[6:0]/TC[6:0].

Temp. Range Value	Temp. Rising State (℃)	Temp. Falling State (℃)	Restriction
Freq. Changing Point A (TA)	(TA[6:0]-40)+THF[3:0]	TA[6:0]-40	TB[6:0]>TA[6:0]+THF[3:0]
Freq. Changing Point B (TB)	(TB[6:0]-40)+THF[3:0]	TB[6:0]-40	TC[6:0]>TB[6:0]+THF[3:0]
Freq. Changing Point C (TC)	(TC[6:0]-40)+THF[3:0]	TC[6:0]-40	87℃ ≥ TC[6:0]+THF[3:0]

Example:

If TA wants to be set at -10℃, TA[6:0]=-10+40=30=1Eh

If TB wants to be set at 0℃, TB[6:0]=0+40=40=28h

If TC wants to be set at 10℃, TC[6:0]=10+40=50=32h

Temperature Hysteresis Value

This instruction defines the temperature compensation threshold. THV[3:0] is used to set the threshold (hysteresis) value for Vop while THF[3:0] is used to set the threshold (hysteresis) value for frame frequency (fFR). The threshold values (THV & THF) can avoid the Vop/fFR switching up and down, when the ambient temperature changes around the junction of two temperature ranges. When the ambient temperature is decreasing, the Vop/fFR is changed at the junction temperature between two temperature ranges. But if the temperature is increasing, the Vop/fFR is not changed until the temperature exceeds the "junction + hysteresis".

For example,

- THV[3:0]=4 (2℃) and the ambient temperature is inc reasing from 27℃ to 35℃. Vop slope is MT8 in 27.0 ℃ ~33.5℃, and it changes to MT9 if Ta is 34℃ or higher.
- Similarly, if we set THF[3:0]=3 (3℃) and TA at -20 ℃ as a point to change fFR. fFR changes from FRB[3: 0] to FRA[3:0] when temperature decreases from -19.5℃ to -20.0℃. But fFR changes from FRA[3:0] to FRB[3:0] when temperature increases from -17.5℃ to -17.0℃.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	0	1	THV[3:0]=00h~0Fh THF[3:0]=00h~0Fh
1	0	-	-	0	0	THV3	THV2	THV1	THV0	
1	0	-	-	-	-	THF3	THF2	THF1	THF0	

Note: "-" is disable bit. It can be either logic 0 or 1.

The relationship between the parameter THV[3:0] and the temperature hysteresis for Vop is shown below.

THV3	THV2	THV1	THV0	Temp. Hysteresis for Vop
0	0	0	0	0℃ (stop TC auto-adjust of Vop)
0	0	0	1	0.5℃
0	0	1	0	1.0℃
:	:	:	:	:
1	1	0	1	6.5℃
1	1	1	0	7.0℃
1	1	1	1	7.5℃

The relationship between the parameter THF[3:0] and the temperature hysteresis for frame rate is shown below.

THF3	THF2	THF1	THF0	Temp. Hysteresis for FR
0	0	0	0	0℃ (stop TC auto-adjust of fFR)
0	0	0	1	1℃
0	0	1	0	2℃
:	:	:	:	:
1	1	0	1	13℃
1	1	1	0	14℃
1	1	1	1	15℃

Current Temperature

This instruction used to detect current temperature. If the value of T[7:0] is 00h means the internal detected temperature is -40℃ and the current temperature is: **Temperature=T[7:0]x0.5-40** (℃). The ambient temperature maybe varies in a sm all range and the temperature compensation function will adjust Vop (or fFR) up-and-down. As the result, the display looks like flickering. To prevent this kind of problem, THV[3:0] and THF[3:0] are used to reduce the sensitivity of ambient temperature.

- The accuracy of temperature detection will not be affected by THV/THF.
- The built-in thermal sensor is designed for temperature compensation of Vop and fFR. It can't be used to replace a real thermal meter.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	1	Ta=T[7:0]x0.5-40 (℃)
1	1	T7	T6	T5	T4	T3	T2	T1	T0	

Test

This instruction is reserved for IC testing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	1	1	TE	T	TE=0: Normal command mode TE=1: Test command mode T: Select test command mode

INSTRUCTION TABLE (PROM Function)

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Test	0	0	1	1	1	1	1	1	TE	T	Set test command mode
TE=1 & T=1											
Vop Increase	0	0	1	1	0	1	0	1	1	0	Vop increase one step
Vop Decrease	0	0	1	1	0	1	0	1	1	1	Vop decrease one step
Vop Offset	0	0	1	1	0	1	0	0	1	1	Vop offset
	1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	
PROM WR/RD Control	0	0	1	0	0	1	0	0	0	1	PROM WR/RD control WR/RD=0: enable PROM read WR/RD=1: enable PROM write
	1	0	0	0	WR /RD	0	0	0	0	0	
PROM Control Out	0	0	1	0	0	1	0	0	1	0	Cancel PROM control function
PROM Write	0	0	1	0	0	1	0	0	1	1	PROM programming procedure
PROM Read	0	0	1	0	0	1	0	1	0	0	PROM up-load procedure
PROM Auto Read Control	0	0	1	0	0	1	0	1	1	0	PROM Auto Read Control XARD=0: enable auto read XARD=1: disable auto read
	1	0	0	0	0	XARD	0	0	0	0	

INSTRUCTION DESCRIPTION (PROM Function)

Vop Increase

This instruction is used to increase Vop step by one (VOF[7:0]+1).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	0	

Vop Decrease

This instruction is used to decrease Vop step by one (VOF[7:0]-1).

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	1	

Vop Offset

This instruction is changes VopOffset directly. It is not recommended to set VopOffset directly with this instruction.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	1	1	
1	0	VOF7	VOF6	VOF5	VOF4	VOF3	VOF2	VOF1	VOF0	

PROM WR/RD Control

This instruction is used to set the status of PROM that write to PROM or read from PROM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	0	1	WR/RD=0: Enable PROM read RW/RD=1: Enable PROM write
1	0	0	0	WR /RD	0	0	0	0	0	

PROM Control Out

This instruction is used to cancel PROM control function.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	0	

PROM Write

This instruction is used to trigger PROM programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	0	1	1	

PROM Read

This instruction is used to trigger PROM up-load procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	0	0	

PROM Auto Read Control

This instruction is used to set status of PROM auto read function is enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	1	0	
1	0	0	0	0	XARD	0	0	0	0	

OPERATION FLOW

System Power ON Sequence

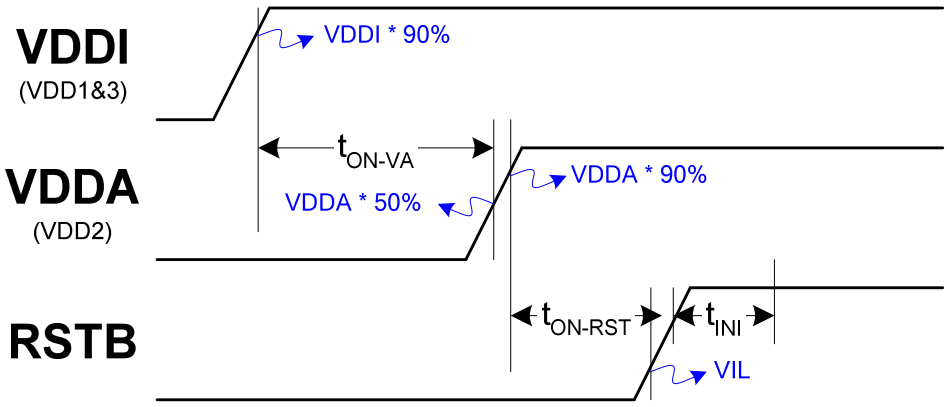


Fig. 22 System Power ON Sequence

Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-VA}	$0 \le t_{ON-VA}$	● If VDDI and VDDA are separated, turn ON VDDI first and then VDDA. ● The hardware reset must be kept LOW until the last power is stable (higher than 90% of the rated value). ● Applying VDDI and VDDA in any order will not damage IC.
RSTB wait time	t_{ON-RST}	$0 \le t_{ON-RST}$	● Keep "$t_{ON-VA} + t_{ON-RST}$" $\ge t_{RW}$. ● Increasing t_{ON-RST} can cover the power stable time difference in customer's system.
Initial wait time	t_{INI}	$t_R \le t_{INI}$	● The initial procedure starts after t_{INI}. ● It is recommended to keep t_{INI} larger than t_R.

Note:

1. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
   The specification listed below just wants to prevent abnormal display on LCD module.
2. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. The power stable-time depends on system and the time is not included in this specification (customer should consider this factor).

Initial Flow

Referential Flow

After the system power ON, the initial flow should set the driver IC for the first display ON.

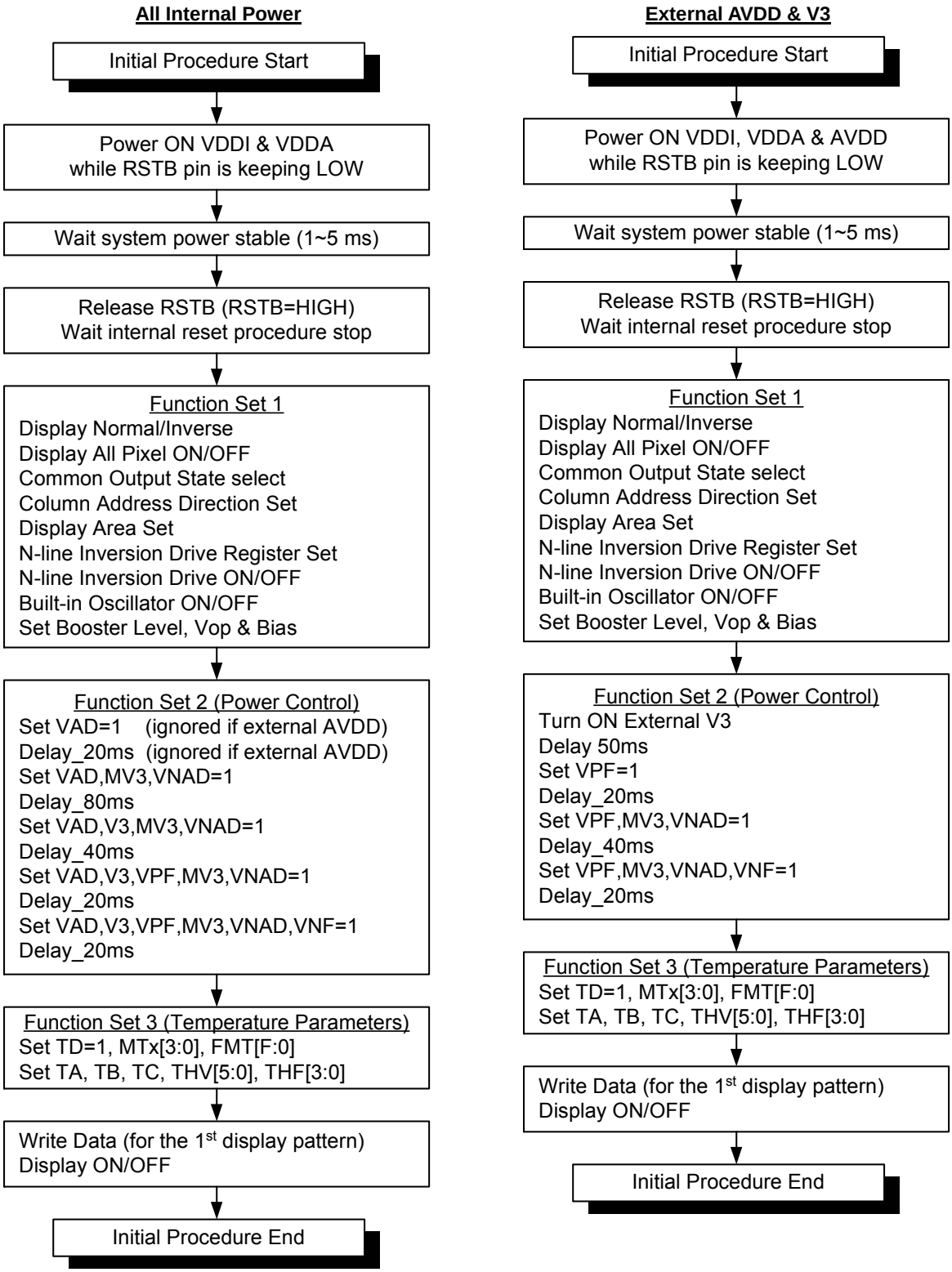


Fig. 23 Initial Flow

Referential Initial Code

The following codes are listed for quick reference. Customer should fine tune parameters according to LCD performance.

```
void initial(void)
{
  Reset_ms(1);
  Delay_ms(5);
  Write(COMMAND, 0xAE);      // Display OFF
  Write(COMMAND, 0xEA);      // Power Discharge OFF
  Write(COMMAND, 0xA6);      // Display Inverse OFF
  Write(COMMAND, 0xA4);      // Disable Display All Pixel ON
  Write(COMMAND, 0xC4);      // COM Output Status
  Write(DATA, 0x02);           // Interlace mode, MY=0
  Write(COMMAND, 0xA0);      // Column Address Direction: MX=0
  Write(COMMAND, 0x6D);      // Display Area
  Write(DATA, 0x20);           // Duty = 1/132 duty
  Write(DATA, 0x00);           // Start Point = 0(COM0~COM3)
  Write(COMMAND, 0x84);      // Display Data Input Direction: Column
  Write(COMMAND, 0x36);      // Set N-Line
  Write(DATA, 0x08);           // N-Line=(8+1)x4=36
  Write(COMMAND, 0xE4);      // N-Line OFF
  Write(COMMAND, 0xAB);      // OSC ON
  Write(COMMAND, 0xE7);      // LCD Drive Method
  Write(DATA, 0x19);           // NLFR=1

  Write(COMMAND, 0xA2);      // BIAS
  Write(DATA, 0x04);           // 1/10 BIAS
  Write(COMMAND, 0x25);      // Power Control
  Write(DATA, 0x20);           // AVDD ON
  Delay_ms(20);
  Write(COMMAND, 0x25);      // Power Control
  Write(DATA, 0x26);           // AVDD, MV3 & NAVDD ON
  Delay_ms(80);
  Write(COMMAND, 0x25);      // Power Control
  Write(DATA, 0x36);           // AVDD, MV3, NAVDD & V3 ON
  Delay_ms(40);
  Write(COMMAND, 0x25);      // Power Control
  Write(DATA, 0x3E);           // AVDD, MV3, NAVDD, V3 & VPF ON
  Delay_ms(20);
  Write(COMMAND, 0x25);      // Power Control
  Write(DATA, 0x3F);           // AVDD, MV3, NAVDD, V3, VPF & VNF ON
  Delay_ms(20);
  Write(COMMAND, 0x81);      // Set EV=64h
  Write(DATA, 0x64);           // VOP=16V
  Write(DATA, 0x00);

  Write(COMMAND, 0x69);      // Temperature Detection ON
  Write(COMMAND, 0x4E);      // TC Setting
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(DATA, 0x00);           // 0mV/℃, should be adjusted by  customer
  Write(COMMAND, 0x39);      // TC Flag
  Write(DATA, 0x00);
  Write(DATA, 0x00);
  Write(COMMAND, 0x5F);      // Set Frame Frequency
  Write(DATA, 0x55);           // fFR=80Hz in all temperature range
  Write(DATA, 0x55);           // should be adjusted by customer
  Write(COMMAND, 0xEC);      // FR Compensation Temp. Range
  Write(DATA, 0x19);           // TA = -15 degree
  Write(DATA, 0x2D);           // TB = 5 degree
  Write(DATA, 0x55);           // TC = 45 degree
  WriteCom(0xED);            // Temp. Hysteresis Value (thermal sensitivity)
```

```
  WriteData(0x04);                  // Vop threshold: +2℃
  WriteData(0x04);                  // fFR threshold: +4℃

  Write(COMMAND, 0xB1);         // Page Address
  Write(DATA, 0x00);                // Page 0
  Write(COMMAND, 0x13);         // Column Address
  Write(DATA, 0x00);                // Start Column = 0
  Write(DATA, 0x00);
  Write(COMMAND, 0x1D);         // Write Data 6732bytes to all DDRAM
  for(init i=0; i<6732; i++)
  Write(DATA, 0x00);                // Write Data 0x00 for 1st Display pattern

  Write(COMMAND, 0xAF);         // Display ON
}
```

This initial code is used for the applications with all internal power circuits. The internal power sequence is shown below:

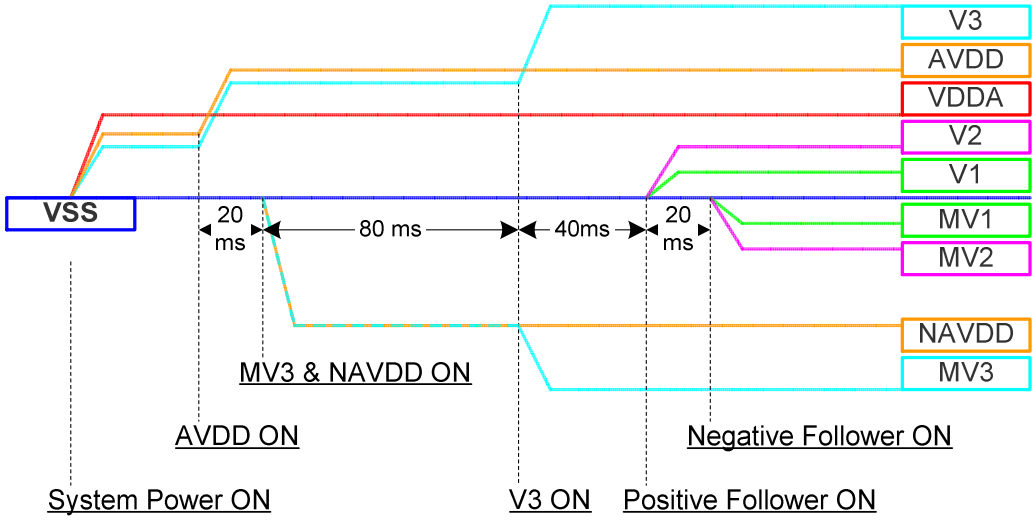
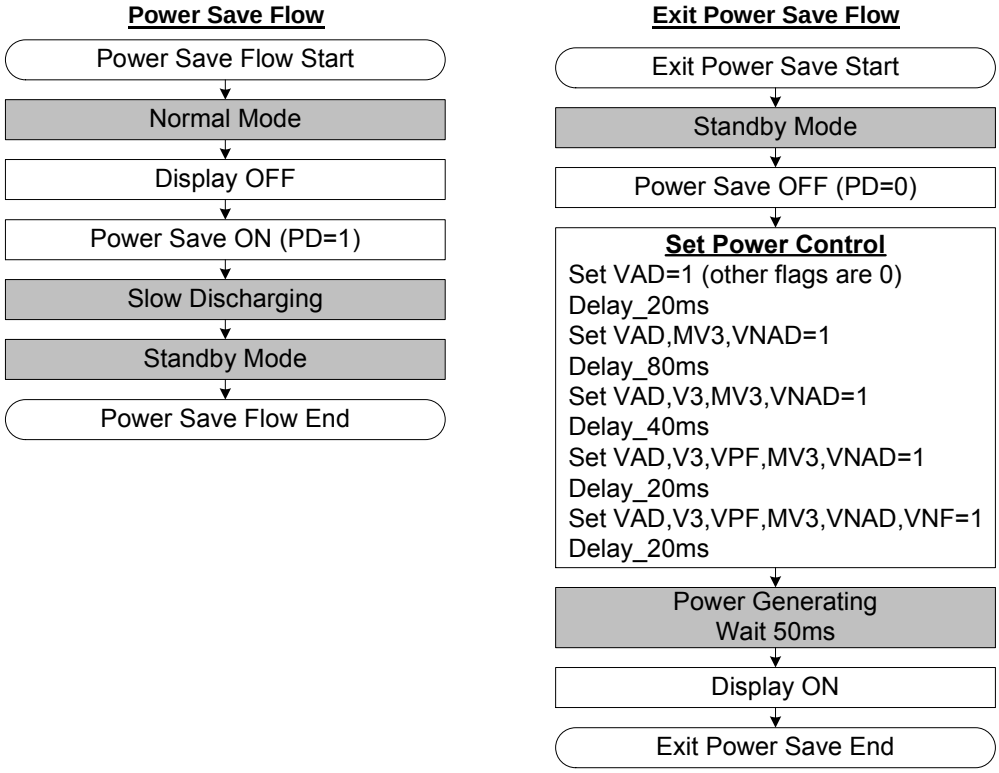


Fig. 24 Internal Analog Power ON Sequence

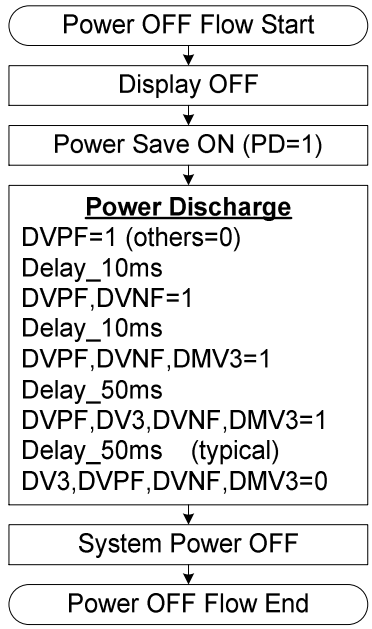
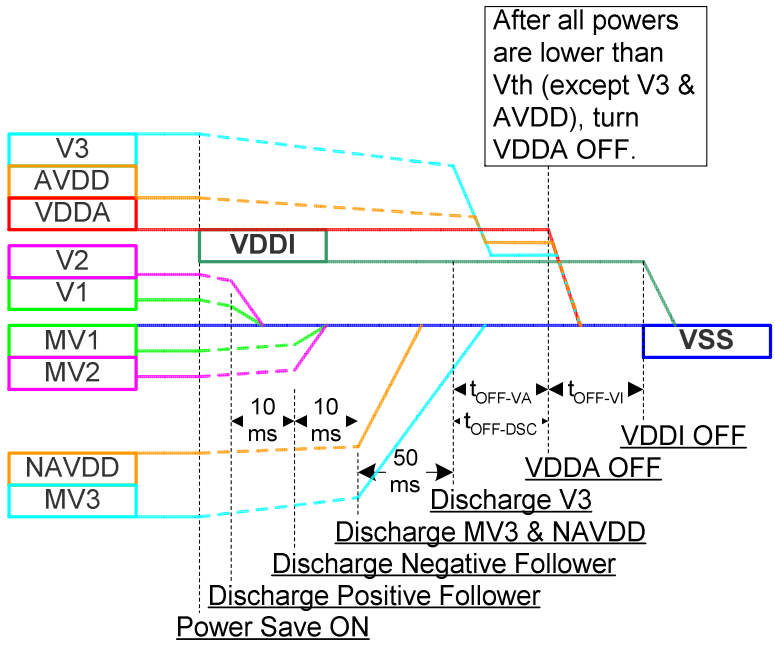
Power Saving Flow

Referential Flow



Note: For external power application, please refer to the initial flow for the correct Power Control sequence.

Power OFF

Referential Operation Flow	Operation Sequence
	

Item	Symbol	Requirement	Description
Analog circuit discharge off delay	$t_{OFF-DSC}$	30ms ≤ $t_{OFF-DSC}$	● It is recommended to turn OFF analog discharge after the discharge procedure is finished. ● The discharge process is finished when: V2, V1, MV1 & MV2 are lower than Vth of liquid crystal; VDDA > AVDD > V3. ● The time will be different from LCD modules, since the panel loading & ITO resistance are different. And the system power and external capacitors will also influence it. ● The typical value is 50ms. And it is recommended to measure the time by real LCD module and application system.
VDDA power off delay	t_{OFF-VA}	$t_{OFF-DSC}$ ≤ t_{OFF-VA}	● Turn VDDA off after discharge procedure is finished. ● AVDD and V3 fall as VDDA falling.
VDDI power off delay	t_{OFF-VI}	0 ≤ t_{OFF-VI}	● If VDDI and VDDA are separated, turn VDDI off after VDDA. ● The AVDD falling time depends on the LCD module and power circuit on the application system.

PROM Operation

Referential PROM Program Flow

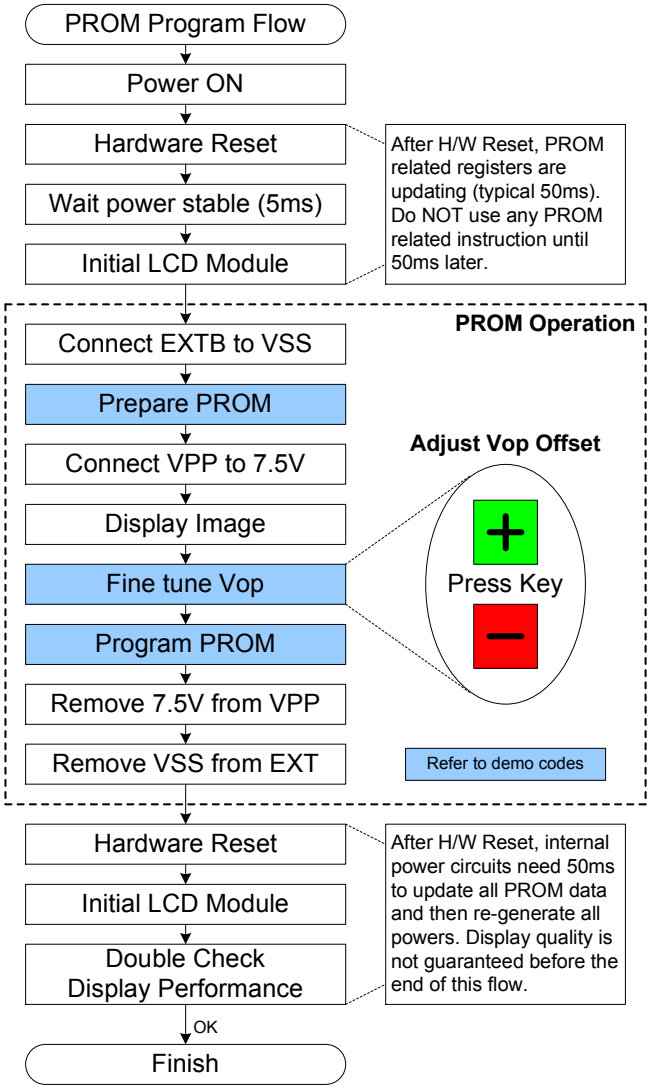


Fig. 25 PROM Program Flow

Referential PROM Operation Code

```
void PreparePROM (void)
{       //---------- Preset PROM mode before Programming PROM ----------
        Write(COMMAND, 0xFF);                   // Enter PROM Test Mode
        Write(COMMAND, 0x96);
        Write(DATA, 0x10);                      // Disable Auto-Load
        Write(COMMAND, 0x94);                   // Load Programmed data into Register
        Delay_ms(50);
        PROM_LED(ON);                           // GPIO control LED ON
                                                // Reserved for PROM indicator of 7.5V switch (ON)
}

void FineTuneVop (void)
{       //---------- Fine tune Vop with "+" & "-" buttons ----------
        Write(COMMAND, 0xD6);                   // Write command 0xD6 if "+" button is pressed
        or                                      // Vop increase 1 step (VopOffset+1)
        Write(COMMAND, 0xD7);                   // Write command 0xD7 if "-" button is pressed
                                                // Vop decrease 1 step (VopOffset-1)
}

void ProgramPROM (void)
{       //---------- Program PROM after VopOffset is adjusted ----------
        Write(COMMAND, 0x95);                   // Program mode parameter
        Write(DATA, 0x08);
        Write(COMMAND, 0x91);                   // Change PROM Control into Program mode
        Write(DATA, 0x20);
        Delay_ms(50);
        Write(COMMAND, 0x93);                   // Program Start
        Delay_ms(50);
        Write(COMMAND, 0x92);                   // Exit PROM control
        Write(COMMAND, 0x94);                   // Load Programmed data into Register
        Delay_ms(50);
        Write(COMMAND, 0xFC);                   // Exit PROM Test Mode
        PROM_LED(OFF);                          // GPIO control LED OFF. Confirm display quality.
                                                // Reserved for PROM indicator of 7.5V switch (OFF)
}
```

Note:

1. If Vop is incorrect and display performance is not accepted after PROM programmed, please redo this flow again to fine tune Vop again.
2. Each press on the "+" or "-" key should execute one command 0xD6 (0xD7) to adjust VopOffset one step up (down).
3. Do not have the backlight closed to IC, because the temperature compensation is turned ON during the burning process. The backlight may heat IC and influence the altitude of Vop.
4. This flow (Burning Flow) is used for LCM assembler.
5. PROM can be written 3 times.

The programmed VopOffset parameter can be read out by the following codes.

```
void ReadVopOffset (void)
{       //---------- Read VopOffset from PROM Register ----------
        byte VopOffset;                          // Allocate 1 byte for VopOffset
        Write(COMMAND, 0xFF);                    // Enter Test mode
        Write(COMMAND, 0x91);                    // Set PROM Control to Download mode
        Write(DATA, 0x00);
        Delay_ms(50);
        Write(COMMAND, 0x94);                    // Load Programmed data into Register
        Delay_ms(50);
        Write(COMMAND, 0x92);                    // Exit PROM control
        Write(COMMAND, 0x34);                    // Set PROM Read to byte mode (VopOffset)
        Write(DATA, 0x03);
        Write(COMMAND, 0x35);                    // Execute PROM Read (byte read)
        VopOffset = Read_LCD(1,PROM);            // LCD interface read 1-byte without dummy read
        DisplayPROM(VopOffset);                  // Display VopOffset to screen
        Write(COMMAND, 0x92);                    // Exit PROM control
        Write(COMMAND, 0xFC);                    // Exit Test mode
}
```

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ABSOLUTE MAXIMUM RATINGS

VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1 & VDD3)	–0.3 ~ 6.0	V
Analog Power supply voltage	VDDA (VDD2)	–0.3 ~ 6.0	V
LCD Power supply voltage	V3	–0.3 ~ 13.75	V
LCD Power supply voltage	V2, V1	–0.3 ~ 6.0	V
LCD Power supply voltage	AVDD	–0.3 ~ 6.0	V
LCD Power supply voltage	NAVDD	-6.0 ~ 0.3	V
LCD Power supply voltage	MV1, MV2	-6.0 ~ 0.3	V
LCD Power supply voltage	MV3	-13.75 ~ 0.3	V
MCU Interface Input Voltage	VIN	–0.3 ~ VDDI+0.3	V
MCU Interface Output Voltage	VOUT	–0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	–40 to +85	℃
Storage temperature	TSTR	–55 to +105	℃

Note:

1. All voltages are respect to VSS1 unless otherwise noted (VSS1=VSS2=VSS3).
2. Stresses exceed the ranges listed above may cause permanent damage to IC.
3. Parameters are valid over operating temperature range unless otherwise specified.
4. Insure the voltage levels always match the correct relation (except Power ON and Power OFF sequence):
   V3 > AVDD > V2 > V1 > VSS2 > MV1 > MV2 > NAVDD > MV3
5. Stresses exceed the ABSOLUTE MAXIMUM RATINGS listed above may cause permanent damage to IC. These ratings are stress only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met. IC operation may be error and the reliability may be deteriorated.

DC CHARACTERISTICS

VSS1=VSS2=VSS3 =0V and Ta = –40 ~ 85 ℃, unless otherwise sp ecified.

Item	Symbol	Condition		Related Pin	Rating			Unit
					Min.	Typ.	Max.	
Digital Operating Voltage	VDDI			VDD1, VDD3	3.0	–	5.5	V
Analog Operating Voltage	VDDA			VDD2	3.0	–	5.5	V
Input High-level Voltage	V_{IH}			MCU Interface	0.8*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}			MCU Interface	VSS1	–	0.2*VDD1	V
Output High-level Voltage	V_{OH}	I_{OH}=1.0mA, VDD1=3.0V		D[7:0] TSYNC	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}	I_{OL}=–1.0mA, VDD1=3.0V		D[7:0] TSYNC	VSS1	–	0.2*VDD1	V
V3 Accuracy	ΔV3	Ta=25℃, VDD=3.0V V3=10V, Bias=1/12		V3	-0.12	–	0.12	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS1		MCU Interface	–1.0	–	1.0	μA
ON Resistance of LCD Drivers	R_{ON}	Ta=25℃	Vop=18.0V, BIAS=1/12 ΔV=10%	COM Drivers	–	1.8	–	KΩ
			Vop=18.0V, BIAS=1/12 ΔV=10%	SEG Drivers	–	1.8	–	KΩ
Read Temperature Offset	ΔT_{RD}	VDD=3.3V, Ta=25℃		–	–2	–	2	℃
		VDD=3.3V, Ta=-40~85℃		–	–4 *1	–	4 *1	
Operation Clock	f_{OSC}	Ta = 25℃		–	–	1630	–	KHz

Note:

- Temperature accuracy is for reference only now. The target for all temperature range is +/- 4℃ and i t is still under yield improvement stage.

The current consumed by whole IC (bare die) with internal power system:

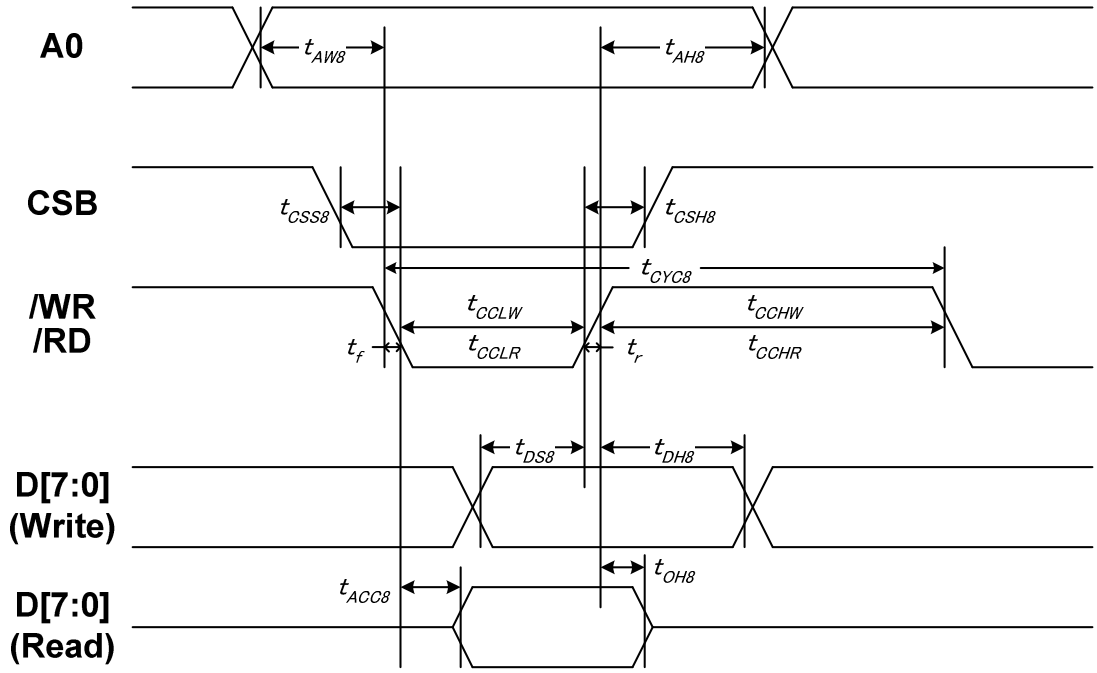
Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display Current (Digital)	IDDI	Display ON, Pattern: SNOW (Static), VDDI=VDDA=3.3V, Internal AVDD, Booster Level1, Vop = 15V, Bias=1/10 N-Line OFF, fFR= 85Hz, Ta=25℃	–	150	–	μA
Display Current (Analog)	IDDA			1350 *2 1000 *3		
Standby	ISS	VDDI=VDDA=3.3V, Internal AVDD, Ta=25℃	–	80	–	μA

Note:

1. The current is DC characteristic of a “Bare Chip”.
2. Current of ST7592-G2
3. Current of ST7592-G2-B1

TIMING CHARATERISTIC

System Bus Timing for 8080 MCU Interface



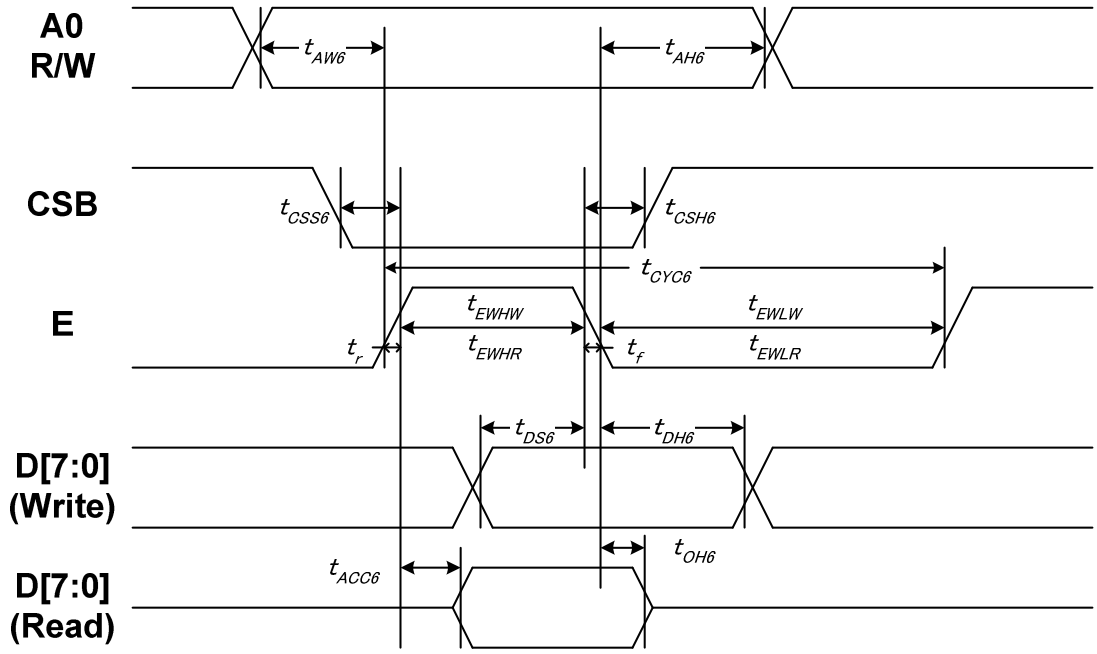
VDD1 = 3.3V~5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		1100	—	
/WR L pulse width (WRITE)		tCCLW		500	—	
/WR H pulse width (WRITE)		tCCHW		500	—	
/RD L pulse width (READ)	/RD	tCCLR		950	—	
/RD H pulse width (READ)		tCCHR		500	—	
CSB setup time	CSB	tCSS8		100	—	
CSB hold time		tCSH8		100	—	
WRITE Data setup time	D[7:0]	tDS8		200	—	
WRITE Data hold time		tDH8		50	—	
READ access time		tACC8	CL = 100 pF	—	950	
READ Output disable time		tOH8	CL = 100 pF	5	200	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns widther than /WR (or /RD).

System Bus Timing for 6800 MCU Interface



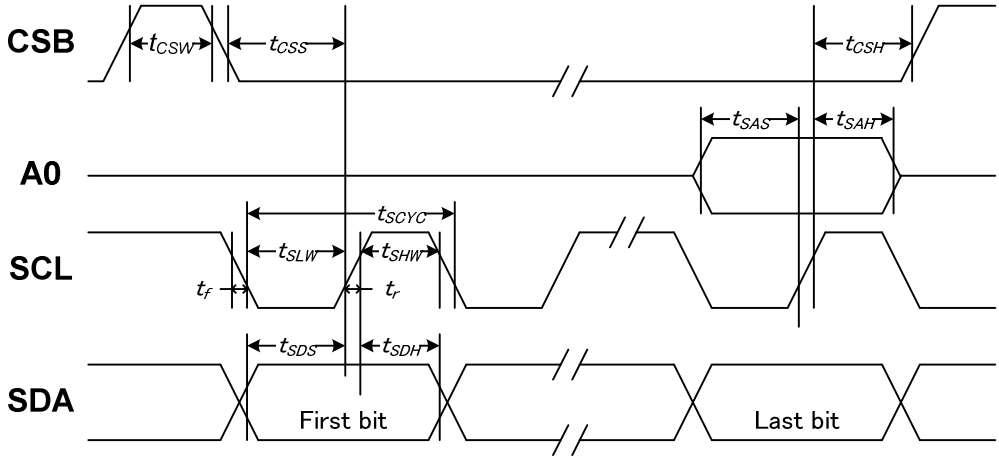
VDD1 = 3.3V~5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		1100	—	
Enable L pulse width (WRITE)		tEWLW		500	—	
Enable H pulse width (WRITE)		tEWHW		500	—	
Enable L pulse width (READ)		tEWLR		500	—	
Enable H pulse width (READ)		tEWHR		500	—	
CSB setup time	CSB	tCSS6		100	—	
CSB hold time		tCSH6		100	—	
Write data setup time	D[7:0]	tDS6		200	—	
Write data hold time		tDH6		60	—	
Read data access time		tACC6	CL = 100 pF	—	950	
Read data output disable time		tOH6	CL = 100 pF	5	200	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≤ (tCYC6 – tEWLR – tEWHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.
3. tEWLW and tEWLR are specified as the overlap between CSB being “L” and E.
   CSB and E cannot act at the same time and CSB should be 100ns widther than E.

System Bus Timing for 4-Line SPI MCU Interface



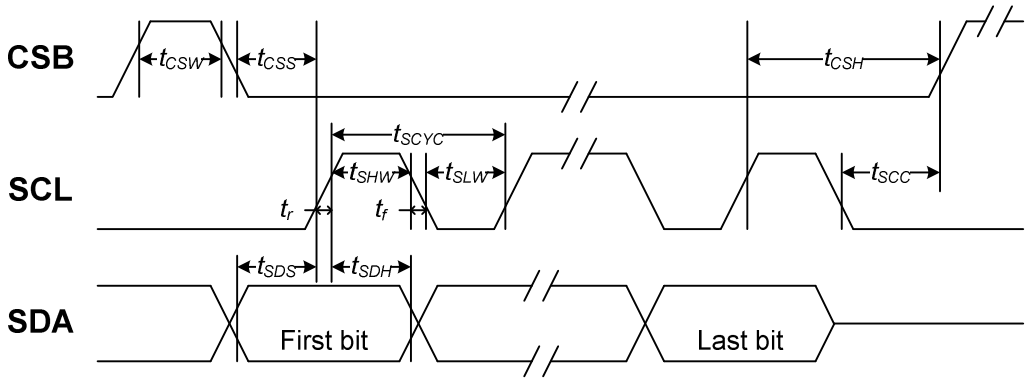
VDD1 = 3.3V~5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		250	—	ns
SCL “H” pulse width		tSHW		100	—	
SCL “L” pulse width		tSLW		100	—	
Address setup time	A0	tSAS		150	—	
Address hold time		tSAH		150	—	
Data setup time	SDA	tSDS		100	—	
Data hold time		tSDH		100	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB “H” pulse width		tCSW		25	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

System Bus Timing for 3-Line SPI MCU Interface



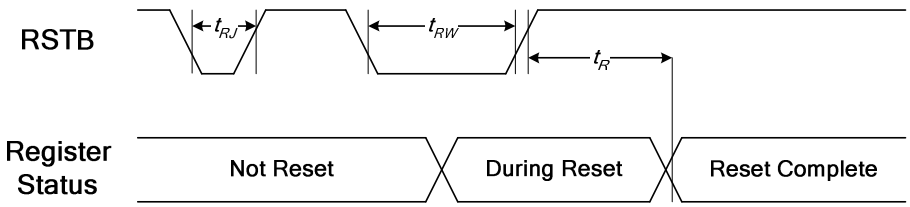
VDD1 = 3.3V~5.0V, Ta = 25℃

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial Clock Period	SCL	tSCYC		250	—	ns
SCL “H” pulse width		tSHW		100	—	
SCL “L” pulse width		tSLW		100	—	
SCL wait time		tSCC		100	—	
Data setup time	SDA	tSDS		100	—	
Data hold time		tSDH		100	—	
CSB-SCL time	CSB	tCSS		150	—	
CSB-SCL time		tCSH		150	—	
CSB “H” pulse width		tCSW		10	—	

Note:

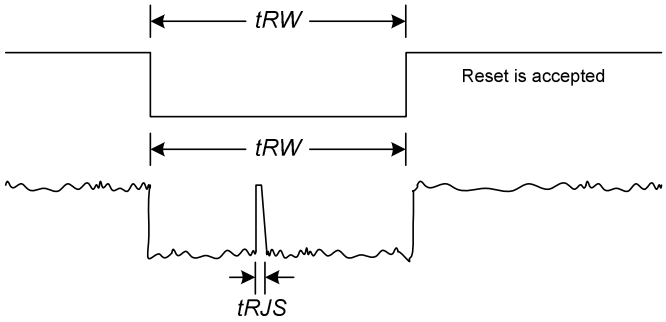
1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

Reset Timing



VDD1 = 3.3V~5.0V , Ta = 25℃

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 *1	us
Reset “L” pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns



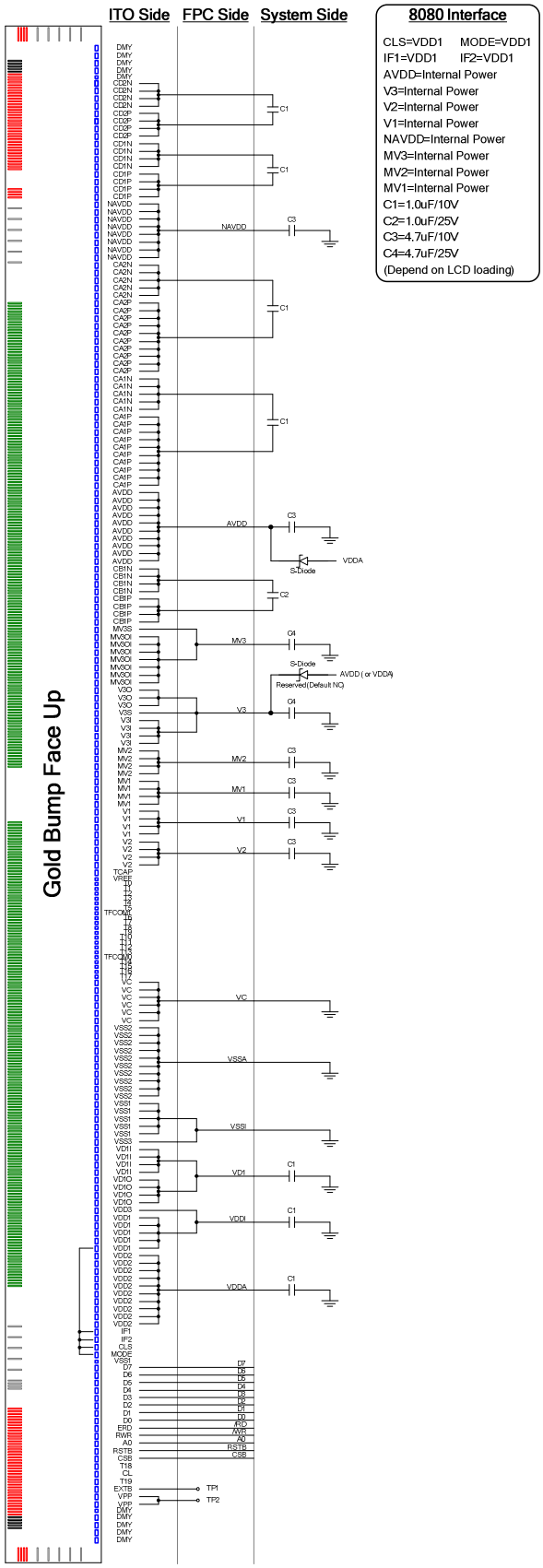
Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than tRW specified above. If the LOW pulse is less than tRJ specified above, the reset procedure of IC will not start. If the LOW pulse is longer than tRJ and less than tRW, the reset procedure of IC is not guaranteed.

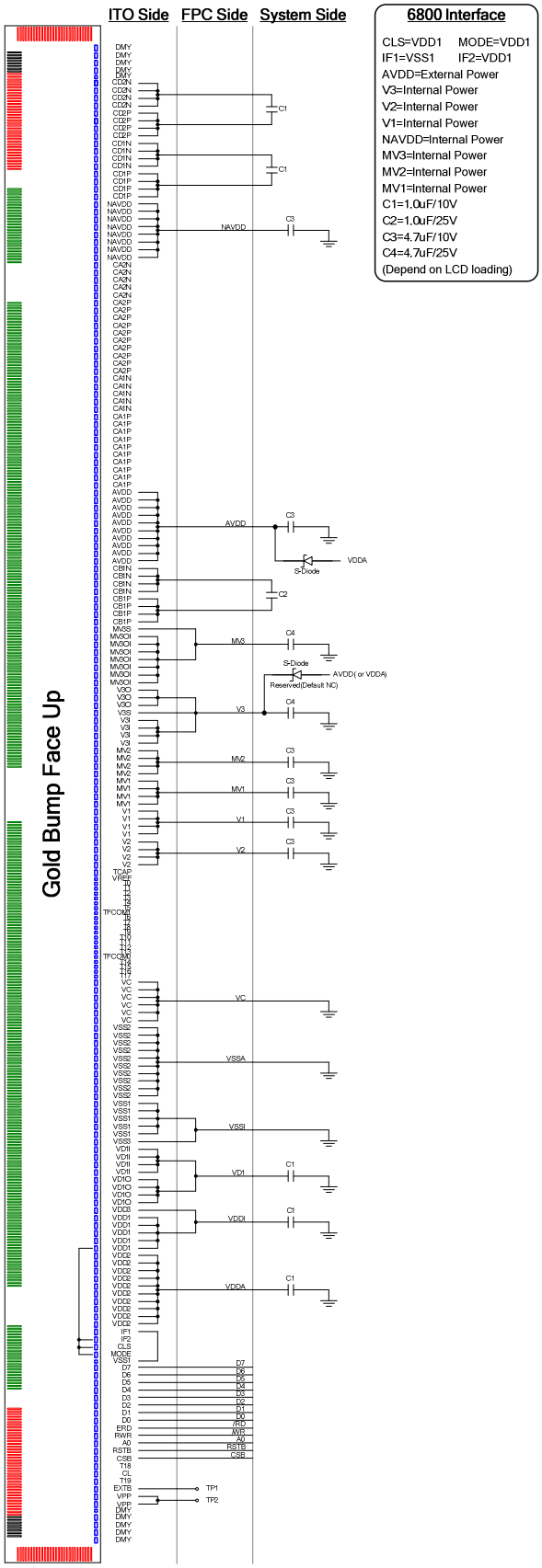
LCD LAYOUT GUIDE

Application Circuit

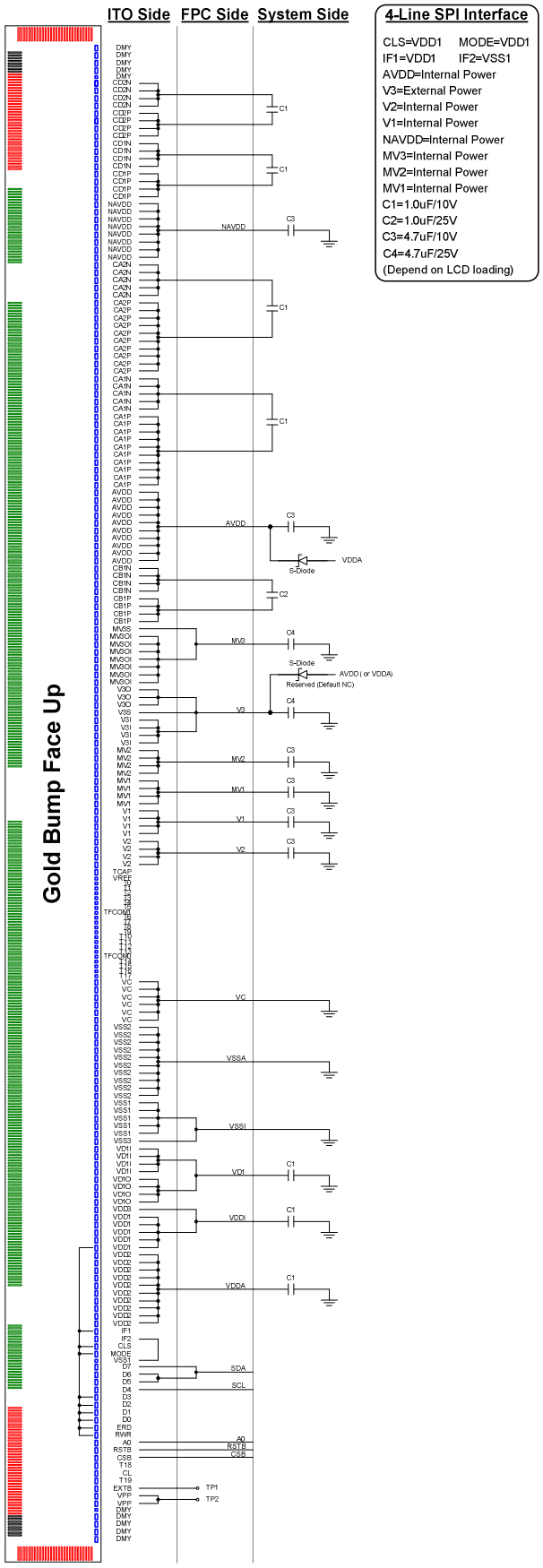
Parallel 8080 Interface



Parallel 6800 Interface



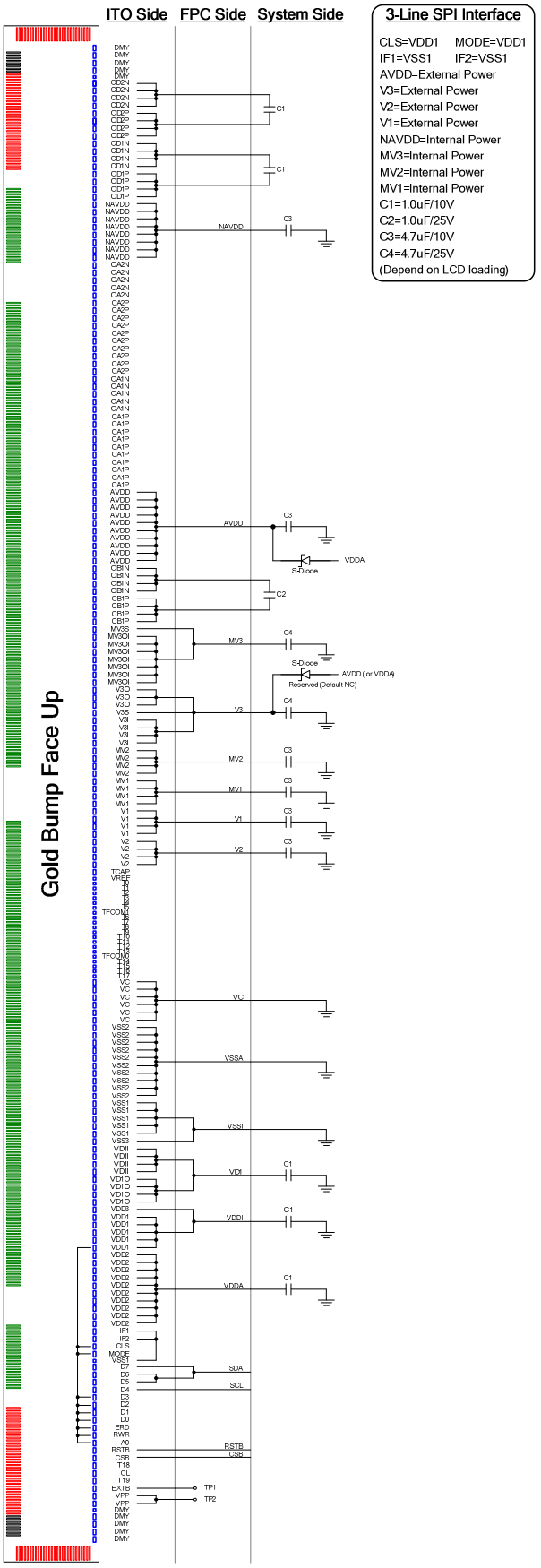
Serial 4-Line SPI



4-Line SPI Interface

CLS=VDD1 MODE=VDD1
IF1=VDD1 IF2=VSS1
AVDD=Internal Power
V3=External Power
V2=Internal Power
V1=Internal Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/10V
C2=1.0uF/25V
C3=4.7uF/10V
C4=4.7uF/25V
(Depend on LCD loading)

Serial 3-Line SPI



3-Line SPI Interface

CLS=VDD1 MODE=VDD1
IF1=VSS1 IF2=VSS1
AVDD=External Power
V3=External Power
V2=External Power
V1=External Power
NAVDD=Internal Power
MV3=Internal Power
MV2=Internal Power
MV1=Internal Power
C1=1.0uF/10V
C2=1.0uF/25V
C3=4.7uF/10V
C4=4.7uF/25V
(Depend on LCD loading)

ITO Layout Suggestion

The ITO layout suggestion is shown as below:

- **For V3, MV3, VD1, VSS and VDD**

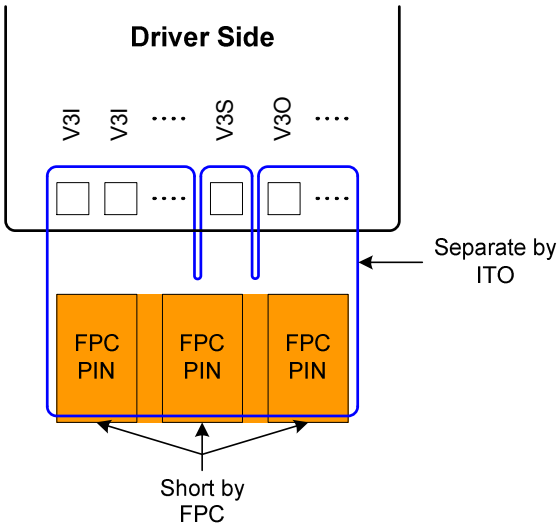


Fig. 26 V3 ITO Layout

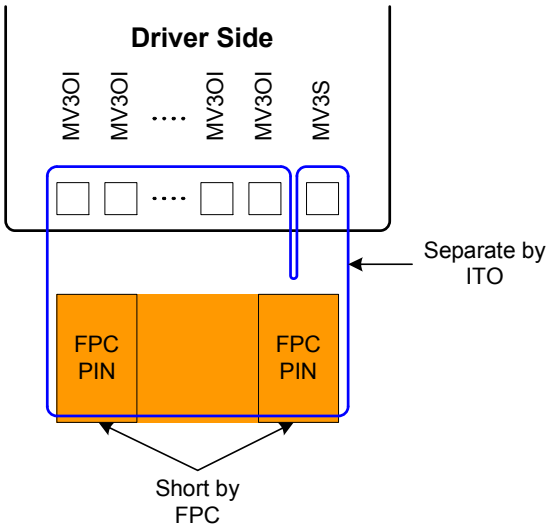


Fig. 27 MV3 ITO Layout

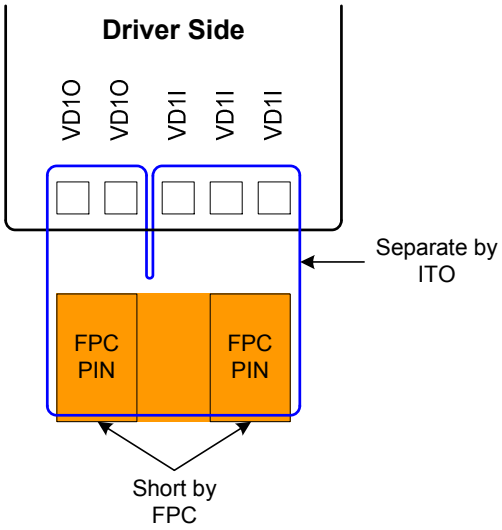


Fig. 28 VD1 ITO Layout

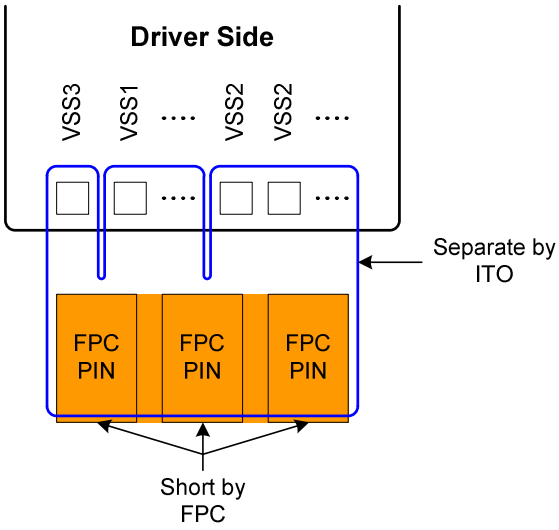


Fig. 29 VSS ITO Layout

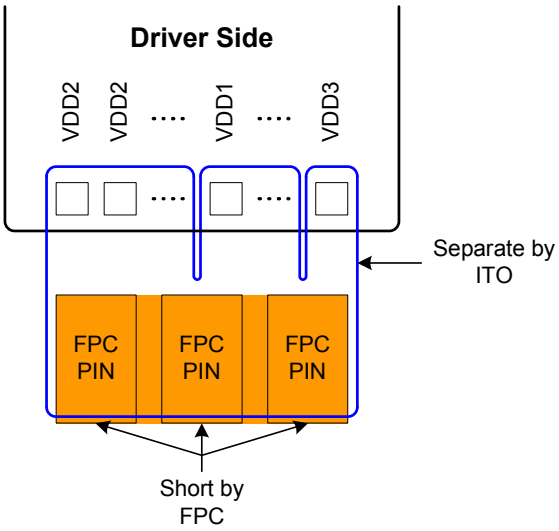


Fig. 30 VDD ITO Layout

- **For VPP**

  This is the power source for programming the internal PROM. If the ITO resistance is too high, the operation current will cause the voltage drop while programming PROM. Please try to keep the ITO resistance as low as possible.

ITO Resistance

Pin Name	ITO Resister
VPP	<50Ω
VDD1, VDD2, VDD3, VSS1, VSS2, VSS3, VD1I, VD1O, V3O, V3I, V3S, V2, V1, VC, MV1, MV2, MV3OI, MV3S, AVDD, NAVDD, CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, CD1P, CD1N, CD2P, CD2N	<100Ω
A0, ERD, RWR, CSB, D[7:0]	<700Ω
IF[2:1], CLS, MODE, EXTB	<1KΩ
RSTB	<10KΩ
TCAP, CL, VREF, T0~T19, TFCOM0, TFCOM1	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM131 is equal, and so is it of SEG0 ~ SEG395.
2. These Limitations include the bottleneck of ITO layout.
3. The ITO layout suggestions are listed above.
4. The resistance of RSTB is 2KΩ~5KΩ generally. It can be the combination of ITO and external resistor.

REVERSION HISTORY

Version	Date	Description
0.0	2010/02/23	● Draft version.
0.1	2010/06/04	● Add IC Outline, PAD CENTER COORDINATES and Application Circuit.
0.2	2010/07/13	● Modify the table of bias ratio. ● Modify the table of ABSOLUTE MAXIMUM RATINGS. ● Modify the description of Current Temperature. ● Modify the label mistake of BIAS Voltage Follower. ● Modify the description mistake of N-Line Inversion. ● Add the rating of TIMING CHARATERISTIC. ● Modify the pin description of TFCOM0 and TFCOM1. ● Modify Application Circuit.
0.3	2010/10/12	● Add the items of ITO Resistance Limitation. ● Modify the wrong description of Temperature Gradient Selection Circuit.
0.4	2010/12/01	● Modify the figure of Power Circuit. ● Modify the recommended capacitor value of Application Circuit.
0.5	2011/05/17	● Add ITO Limitation for VD1I and VD1O. ● Add the description for VD1 power. ● Modify pin description of CA1P, CA1N, CA2P, CA2N, CB1P, CB1N, CD1P, CD1N, CD2P, and CD2N. ● Add recommended ITO resistance for RSTB. ● Modify available voltage range for different BIAS ratio. ● Add the content of ABSOLUTE MAXIMUM RATINGS. ● Add the formula for ideal BIAS ratio. ● Modify power system application. ● Remove the description of temperature compensation depend on V3 power. ● Add instruction description of Booster Level. ● Modify the instruction mistake of Vop Increase and Vop Decrease. ● Modify Application Circuit. ● Modify the description of programmable temperature compensation. ● Modify the description of Serial Interface. ● Modify the description of DDRAM Map to LCD Driver Output. ● Modify the mistake of figure “Temperature Gradient Compensation”. ● Modify the description of BIAS. ● Modify the description of Electronic Volume. ● Modify the description of Current Temperature.
0.5a	2011/7/28	● VDD Range: 3.3V ~ 5V (typical). ● Rewrite Features at Page 1 to emphasis IC function. ● Add notes for MPU interface: Read of Parallel and Serial Interfaces. ● Fix typing mistakes and wrong power connection examples. ● Reserved Booster Level 2. ● Reserved MLS=0 condition (it decreases response time under low temperature). ● Temperature accuracy T.B.D. ● Add PROM flow. ● Add Serial 3-Line timing parameter tSCC. ● Remove Case-2 of 8080 and 6800 AC timing to prevent misunderstanding. ● Add V3 tolerance.

Version	Date	Description
0.5b	2011/8/1	● Modify Operation Flow: Initial, Power Save, Power OFF & PROM Flow. ● Modify Parallel Timing Chart and fix CSB timing: tCSS & tCSH. ● Fix typing mistakes.
0.6	2011/8/9	● Add RSTB resistance note. ● Add Vop range example for temperature compensation. ● Remove old power circuit (with resistor). Use Schottky diode as new circuit and add Schottky diode into application circuits. ● Fix typing mistake in Drive Method instruction. ● Add display duty and scan duty into “Display Area” instruction. ● Add demo initial code. ● Update Power OFF section. ● Finalize DC / AC Characteristic and remove TBD.
0.7	2011/9/29	● Move ITO Resistance to LCD LAYOUT GUIDE. ● Fix description mistakes in Serial Interface: 1. Reading IC Status: a dummy bit is output before IC status. 2. Reading Temperature, PROM register: no dummy bit. 3. Data read in serial interface is not available. ● Fix calculation mistake of Vop-Bias example in “BIAS Voltage Follower”. ● Add Vop Temperature Compensation calculation example. ● Fix Booster Level parameter mistake: bit-D1 should be “0”. ● Reserve control flags: NLF (fix to 1) & THV[5:4] (fix to 0,0). ● Redraw figure of “Read Modify Write End” for detailed illustration. ● Add parameter restriction of TA[6:0], TB[6:0] & TC[6:0]. ● Rewrite description of “Temperature Hysteresis Value” instruction to prevent end user misunderstanding. ● Add more description of “Vop Offset” instruction to prevent improper operation. ● Fine tune parameters in example initial code: N-Line, Drive Mode & Vop; Fix typing mistakes in comments. ● Release internal analog power ON sequence timing chart. ● Add PROM_LED procedure in PROM operation codes for customer to have a manual-operation indicator. ● Fix typing mistake in PROM Operation code: the 2nd PreparePROM(…) should be ProgramPROM(…). ● Remove “ReadPROM();” and add ReadVopOffset(…) code. ● Separate Display Current into Digital and Analog parts (and adjust typical values). ● Rename APPLICATION NOTE as LCD LAYOUT GUIDE and collect LCD layout related information into this section.
0.7a	2011/10/4	● Fix typing mistakes. ● Rewrite some description to prevent misunderstanding. ● Modify description of power applications.
1.0	2011/11/8	● Change Version to V1.0 for mass production. ● Part Number : ST7592-G2.
1.1	2012/6/1	● Release ST7592-G2-B1 (smaller VDD2 current). ● Fix description of TA ~ TC restriction: “-TF[3:0]” => “+TF[3:0]” (Page 51).