■ FEATURES

- Direct display of RAM data through the display data RAM.
- RAM capacity：192 x 97 = 18624bits
- Display duty selectable by hardware
- 1/97 duty： 97common x 160segment
  1/65 duty： 65common x 192segment
  1/33 duty： 33common x 192segment
  1/17 duty： 17common x 192segment
  1/9 duty： 9 common x 192segment
  1/5 duty： 5 common x 192segment
  Static ： 1 common x 192segment
- Both 6800 and 8080 series MPU can directly connected by 8-bit parallel interface, also 4 line / 3 line serial interface and IIC interface are supportable.
- Abundant command functions
- Low-power liquid crystal display power supply circuit equipped internally.
- Bias set 1/2 1/3 1/4 1/5 1/6 1/7 1/8 1/9 1/10 by software
- Booster circuit (with Boost ratios of 2X/3X/4X/5X/6X/7X, where the step-up voltage reference power supply can be input externally).
  V0 voltage regulator resistors equipped internally, V1 to VSS voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower
- CR oscillator circuit equipped internally (external clock can also be input)
- Low power consumption.
  Logic power supply VDD – VSS = 1.8V to 3.6 V
  Boost reference voltage: VDD2 – VSS = 2.4V to 3.6V
  Booster maximum voltage limited VOUT=18.0V
  Liquid crystal drive power supply:
  V0 – VSS = 5.0V to 14.0 V
- Wide range of operating temperatures: –40 to 85℃
- CMOS process
- Shipping forms include bare chip and COG.
- Software compatible to SED1065/SED1565/SED1575
- Static Display function support

■ GENERAL DESCRIPTION

The RW1092 is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the RW1092 contain 97x192 bits of display data RAM and there is a 1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power LCD driver power supply, and a display clock CR oscillator circuit, the RW1092 can be used to create the lowest power display system with the fewest components for High-performance portable devices.

PART NO.	VRS temperature gradient	VRS range
RW1092	-0.05%/℃	2.1V ±0.03V

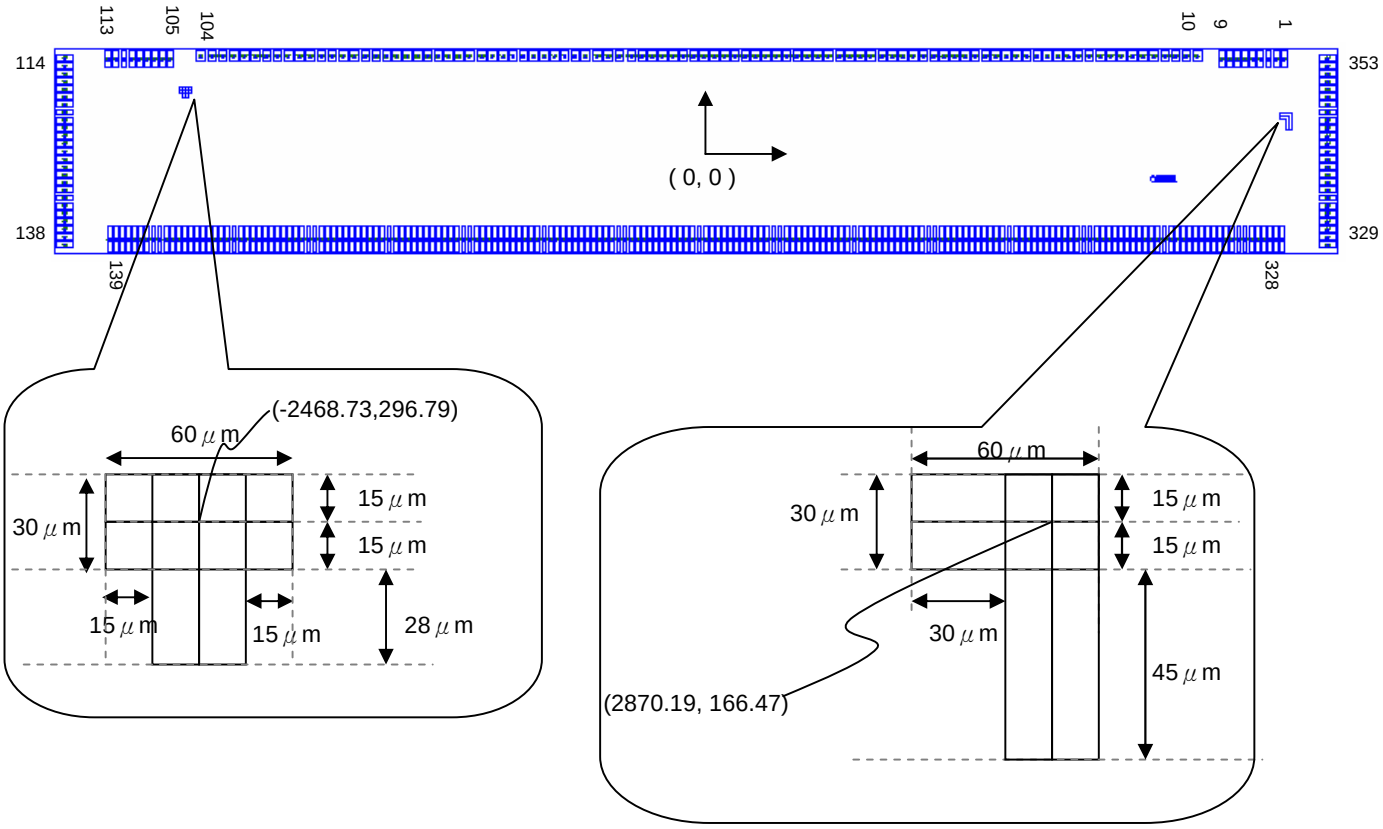
RW1092 Revision History		
Version	**Date**	**Description**
1.0	2010/01/04	Add static on Function、Add 3SPI data length command、N-line Reversal Function valid for all mode
1.1	2010/05/18	Add application circuit and static application note, modify the chip thickness to 500um
1.2	2010/07/12	Add external RA、RB use command and Frame frequency adjustment command
1.3	2010/08/12	Make correction for numbers of duty. P.1, P.4 ~P.9, P.10 ~ P.15, P.16 ~ P.21, P.22~ P.27, P.28 ~ P.33, P.34 ~ P.39, P.43, P.44, P.48, P.49
1.4	2010/9/13	Modify Power of sequence

■ PAD ARRANGEMENT

Chip Size: 6,294 μm x 1,074 μm
Min. Bump Pitch: 30 μm(Min.)

Bump Size:	PAD No. 001～009	22.4 μm x 81 μm
	PAD No. 010～104	35 μm x 52 μm
	PAD No. 105～113	22.4 μm x 81 μm
	PAD No. 114～138	81 μm x 22.4 μm
	PAD No. 139～328	15 μm x 124 μm
	PAD No. 329～353	81 μm x 22.4 μm

Bump Height: 15 μm(Typ)
Chip Thickness: 500 μm



■ PAD Coordinate(1/97 Duty, SHL=0,3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM[88]	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	COM[89]	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	COM[90]	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	COM[91]	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	COM[92]	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	COM[93]	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	COM[94]	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	COM[95]	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	COM[47]	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	COM[46]	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	COM[45]	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	COM[44]	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	COM[43]	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	COM[42]	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	COM[41]	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	COM[40]	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	COM[39]	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	COM[38]	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	COM[37]	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	COM[36]	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	COM[35]	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	COM[34]	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	COM[33]	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	COM[32]	-3055	224.7

■ PAD Coordinate(1/97 Duty, SHL=0,3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[31]	-3055	187.3	161	SEG[7]	-2175.3	-423.5	201	SEG[47]	-975.3	-423.5
122	COM[30]	-3055	149.9	162	SEG[8]	-2145.3	-423.5	202	SEG[48]	-945.3	-423.5
123	COM[29]	-3055	112.5	163	SEG[9]	-2115.3	-423.5	203	SEG[49]	-915.3	-423.5
124	COM[28]	-3055	75.1	164	SEG[10]	-2085.3	-423.5	204	SEG[50]	-885.3	-423.5
125	COM[27]	-3055	37.7	165	SEG[11]	-2055.3	-423.5	205	SEG[51]	-855.3	-423.5
126	COM[26]	-3055	0.3	166	SEG[12]	-2025.3	-423.5	206	SEG[52]	-825.3	-423.5
127	COM[25]	-3055	-37.1	167	SEG[13]	-1995.3	-423.5	207	SEG[53]	-795.3	-423.5
128	COM[24]	-3055	-74.5	168	SEG[14]	-1965.3	-423.5	208	SEG[54]	-765.3	-423.5
129	COM[23]	-3055	-111.9	169	SEG[15]	-1935.3	-423.5	209	SEG[55]	-735.3	-423.5
130	COM[22]	-3055	-149.3	170	SEG[16]	-1905.3	-423.5	210	SEG[56]	-705.3	-423.5
131	COM[21]	-3055	-186.7	171	SEG[17]	-1875.3	-423.5	211	SEG[57]	-675.3	-423.5
132	COM[20]	-3055	-224.1	172	SEG[18]	-1845.3	-423.5	212	SEG[58]	-645.3	-423.5
133	COM[19]	-3055	-261.5	173	SEG[19]	-1815.3	-423.5	213	SEG[59]	-615.3	-423.5
134	COM[18]	-3055	-298.9	174	SEG[20]	-1785.3	-423.5	214	SEG[60]	-585.3	-423.5
135	COM[17]	-3055	-336.3	175	SEG[21]	-1755.3	-423.5	215	SEG[61]	-555.3	-423.5
136	COM[16]	-3055	-373.7	176	SEG[22]	-1725.3	-423.5	216	SEG[62]	-525.3	-423.5
137	COM[15]	-3055	-411.1	177	SEG[23]	-1695.3	-423.5	217	SEG[63]	-495.3	-423.5
138	COM[14]	-3055	-448.5	178	SEG[24]	-1665.3	-423.5	218	SEG[64]	-465.3	-423.5
139	COM[13]	-2835.3	-423.5	179	SEG[25]	-1635.3	-423.5	219	SEG[65]	-435.3	-423.5
140	COM[12]	-2805.3	-423.5	180	SEG[26]	-1605.3	-423.5	220	SEG[66]	-405.3	-423.5
141	COM[11]	-2775.3	-423.5	181	SEG[27]	-1575.3	-423.5	221	SEG[67]	-375.3	-423.5
142	COM[10]	-2745.3	-423.5	182	SEG[28]	-1545.3	-423.5	222	SEG[68]	-345.3	-423.5
143	COM[9]	-2715.3	-423.5	183	SEG[29]	-1515.3	-423.5	223	SEG[69]	-315.3	-423.5
144	COM[8]	-2685.3	-423.5	184	SEG[30]	-1485.3	-423.5	224	SEG[70]	-285.3	-423.5
145	COM[7]	-2655.3	-423.5	185	SEG[31]	-1455.3	-423.5	225	SEG[71]	-255.3	-423.5
146	COM[6]	-2625.3	-423.5	186	SEG[32]	-1425.3	-423.5	226	SEG[72]	-225.3	-423.5
147	COM[5]	-2595.3	-423.5	187	SEG[33]	-1395.3	-423.5	227	SEG[73]	-195.3	-423.5
148	COM[4]	-2565.3	-423.5	188	SEG[34]	-1365.3	-423.5	228	SEG[74]	-165.3	-423.5
149	COM[3]	-2535.3	-423.5	189	SEG[35]	-1335.3	-423.5	229	SEG[75]	-135.3	-423.5
150	COM[2]	-2505.3	-423.5	190	SEG[36]	-1305.3	-423.5	230	SEG[76]	-105.3	-423.5
151	COM[1]	-2475.3	-423.5	191	SEG[37]	-1275.3	-423.5	231	SEG[77]	-75.3	-423.5
152	COM[0]	-2445.3	-423.5	192	SEG[38]	-1245.3	-423.5	232	SEG[78]	-45.3	-423.5
153	COMS2	-2415.3	-423.5	193	SEG[39]	-1215.3	-423.5	233	SEG[79]	-15.3	-423.5
154	SEG[0]	-2385.3	-423.5	194	SEG[40]	-1185.3	-423.5	234	SEG[80]	14.7	-423.5
155	SEG[1]	-2355.3	-423.5	195	SEG[41]	-1155.3	-423.5	235	SEG[81]	44.7	-423.5
156	SEG[2]	-2325.3	-423.5	196	SEG[42]	-1125.3	-423.5	236	SEG[82]	74.7	-423.5
157	SEG[3]	-2295.3	-423.5	197	SEG[43]	-1095.3	-423.5	237	SEG[83]	104.7	-423.5
158	SEG[4]	-2265.3	-423.5	198	SEG[44]	-1065.3	-423.5	238	SEG[84]	134.7	-423.5
159	SEG[5]	-2235.3	-423.5	199	SEG[45]	-1035.3	-423.5	239	SEG[85]	164.7	-423.5
160	SEG[6]	-2205.3	-423.5	200	SEG[46]	-1005.3	-423.5	240	SEG[86]	194.7	-423.5

■ PAD Coordinate(1/97 Duty, SHL=0,3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[87]	224.7	-423.5	281	SEG[127]	1424.7	-423.5	321	COM[55]	2624.7	-423.5
242	SEG[88]	254.7	-423.5	282	SEG[128]	1454.7	-423.5	322	COM[56]	2654.7	-423.5
243	SEG[89]	284.7	-423.5	283	SEG[129]	1484.7	-423.5	323	COM[57]	2684.7	-423.5
244	SEG[90]	314.7	-423.5	284	SEG[130]	1514.7	-423.5	324	COM[58]	2714.7	-423.5
245	SEG[91]	344.7	-423.5	285	SEG[131]	1544.7	-423.5	325	COM[59]	2744.7	-423.5
246	SEG[92]	374.7	-423.5	286	SEG[132]	1574.7	-423.5	326	COM[60]	2774.7	-423.5
247	SEG[93]	404.7	-423.5	287	SEG[133]	1604.7	-423.5	327	COM[61]	2804.7	-423.5
248	SEG[94]	434.7	-423.5	288	SEG[134]	1634.7	-423.5	328	COM[62]	2834.7	-423.5
249	SEG[95]	464.7	-423.5	289	SEG[135]	1664.7	-423.5	329	COM[63]	3055	-448.5
250	SEG[96]	494.7	-423.5	290	SEG[136]	1694.7	-423.5	330	COM[64]	3055	-411.1
251	SEG[97]	524.7	-423.5	291	SEG[137]	1724.7	-423.5	331	COM[65]	3055	-373.7
252	SEG[98]	554.7	-423.5	292	SEG[138]	1754.7	-423.5	332	COM[66]	3055	-336.3
253	SEG[99]	584.7	-423.5	293	SEG[139]	1784.7	-423.5	333	COM[67]	3055	-298.9
254	SEG[100]	614.7	-423.5	294	SEG[140]	1814.7	-423.5	334	COM[68]	3055	-261.5
255	SEG[101]	644.7	-423.5	295	SEG[141]	1844.7	-423.5	335	COM[69]	3055	-224.1
256	SEG[102]	674.7	-423.5	296	SEG[142]	1874.7	-423.5	336	COM[70]	3055	-186.7
257	SEG[103]	704.7	-423.5	297	SEG[143]	1904.7	-423.5	337	COM[71]	3055	-149.3
258	SEG[104]	734.7	-423.5	298	SEG[144]	1934.7	-423.5	338	COM[72]	3055	-111.9
259	SEG[105]	764.7	-423.5	299	SEG[145]	1964.7	-423.5	339	COM[73]	3055	-74.5
260	SEG[106]	794.7	-423.5	300	SEG[146]	1994.7	-423.5	340	COM[74]	3055	-37.1
261	SEG[107]	824.7	-423.5	301	SEG[147]	2024.7	-423.5	341	COM[75]	3055	0.3
262	SEG[108]	854.7	-423.5	302	SEG[148]	2054.7	-423.5	342	COM[76]	3055	37.7
263	SEG[109]	884.7	-423.5	303	SEG[149]	2084.7	-423.5	343	COM[77]	3055	75.1
264	SEG[110]	914.7	-423.5	304	SEG[150]	2114.7	-423.5	344	COM[78]	3055	112.5
265	SEG[111]	944.7	-423.5	305	SEG[151]	2144.7	-423.5	345	COM[79]	3055	149.9
266	SEG[112]	974.7	-423.5	306	SEG[152]	2174.7	-423.5	346	COM[80]	3055	187.3
267	SEG[113]	1004.7	-423.5	307	SEG[153]	2204.7	-423.5	347	COM[81]	3055	224.7
268	SEG[114]	1034.7	-423.5	308	SEG[154]	2234.7	-423.5	348	COM[82]	3055	262.1
269	SEG[115]	1064.7	-423.5	309	SEG[155]	2264.7	-423.5	349	COM[83]	3055	299.5
270	SEG[116]	1094.7	-423.5	310	SEG[156]	2294.7	-423.5	350	COM[84]	3055	336.9
271	SEG[117]	1124.7	-423.5	311	SEG[157]	2324.7	-423.5	351	COM[85]	3055	374.3
272	SEG[118]	1154.7	-423.5	312	SEG[158]	2354.7	-423.5	352	COM[86]	3055	411.7
273	SEG[119]	1184.7	-423.5	313	SEG[159]	2384.7	-423.5	353	COM[87]	3055	449.1
274	SEG[120]	1214.7	-423.5	314	COM[48]	2414.7	-423.5				
275	SEG[121]	1244.7	-423.5	315	COM[49]	2444.7	-423.5				
276	SEG[122]	1274.7	-423.5	316	COM[50]	2474.7	-423.5				
277	SEG[123]	1304.7	-423.5	317	COM[51]	2504.7	-423.5				
278	SEG[124]	1334.7	-423.5	318	COM[52]	2534.7	-423.5				
279	SEG[125]	1364.7	-423.5	319	COM[53]	2564.7	-423.5				
280	SEG[126]	1394.7	-423.5	320	COM[54]	2594.7	-423.5				

■ PAD Coordinate(1/97 Duty, SHL=1,3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM[7]	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	COM[6]	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	COM[5]	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	COM[4]	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	COM[3]	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	COM[2]	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	COM[1]	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	COM[0]	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	COM[48]	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	COM[49]	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	COM[50]	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	COM[51]	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	COM[52]	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	COM[53]	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	COM[54]	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	COM[55]	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	COM[56]	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	COM[57]	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	COM[58]	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	COM[59]	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	COM[60]	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	COM[61]	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	COM[62]	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	COM[63]	-3055	224.7

■ PAD Coordinate(1/97 Duty, SHL=1,3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[64]	-3055	187.3	161	SEG[7]	-2175.3	-423.5	201	SEG[47]	-975.3	-423.5
122	COM[65]	-3055	149.9	162	SEG[8]	-2145.3	-423.5	202	SEG[48]	-945.3	-423.5
123	COM[66]	-3055	112.5	163	SEG[9]	-2115.3	-423.5	203	SEG[49]	-915.3	-423.5
124	COM[67]	-3055	75.1	164	SEG[10]	-2085.3	-423.5	204	SEG[50]	-885.3	-423.5
125	COM[68]	-3055	37.7	165	SEG[11]	-2055.3	-423.5	205	SEG[51]	-855.3	-423.5
126	COM[69]	-3055	0.3	166	SEG[12]	-2025.3	-423.5	206	SEG[52]	-825.3	-423.5
127	COM[70]	-3055	-37.1	167	SEG[13]	-1995.3	-423.5	207	SEG[53]	-795.3	-423.5
128	COM[71]	-3055	-74.5	168	SEG[14]	-1965.3	-423.5	208	SEG[54]	-765.3	-423.5
129	COM[72]	-3055	-111.9	169	SEG[15]	-1935.3	-423.5	209	SEG[55]	-735.3	-423.5
130	COM[73]	-3055	-149.3	170	SEG[16]	-1905.3	-423.5	210	SEG[56]	-705.3	-423.5
131	COM[74]	-3055	-186.7	171	SEG[17]	-1875.3	-423.5	211	SEG[57]	-675.3	-423.5
132	COM[75]	-3055	-224.1	172	SEG[18]	-1845.3	-423.5	212	SEG[58]	-645.3	-423.5
133	COM[76]	-3055	-261.5	173	SEG[19]	-1815.3	-423.5	213	SEG[59]	-615.3	-423.5
134	COM[77]	-3055	-298.9	174	SEG[20]	-1785.3	-423.5	214	SEG[60]	-585.3	-423.5
135	COM[78]	-3055	-336.3	175	SEG[21]	-1755.3	-423.5	215	SEG[61]	-555.3	-423.5
136	COM[79]	-3055	-373.7	176	SEG[22]	-1725.3	-423.5	216	SEG[62]	-525.3	-423.5
137	COM[80]	-3055	-411.1	177	SEG[23]	-1695.3	-423.5	217	SEG[63]	-495.3	-423.5
138	COM[81]	-3055	-448.5	178	SEG[24]	-1665.3	-423.5	218	SEG[64]	-465.3	-423.5
139	COM[82]	-2835.3	-423.5	179	SEG[25]	-1635.3	-423.5	219	SEG[65]	-435.3	-423.5
140	COM[83]	-2805.3	-423.5	180	SEG[26]	-1605.3	-423.5	220	SEG[66]	-405.3	-423.5
141	COM[84]	-2775.3	-423.5	181	SEG[27]	-1575.3	-423.5	221	SEG[67]	-375.3	-423.5
142	COM[85]	-2745.3	-423.5	182	SEG[28]	-1545.3	-423.5	222	SEG[68]	-345.3	-423.5
143	COM[86]	-2715.3	-423.5	183	SEG[29]	-1515.3	-423.5	223	SEG[69]	-315.3	-423.5
144	COM[87]	-2685.3	-423.5	184	SEG[30]	-1485.3	-423.5	224	SEG[70]	-285.3	-423.5
145	COM[88]	-2655.3	-423.5	185	SEG[31]	-1455.3	-423.5	225	SEG[71]	-255.3	-423.5
146	COM[89]	-2625.3	-423.5	186	SEG[32]	-1425.3	-423.5	226	SEG[72]	-225.3	-423.5
147	COM[90]	-2595.3	-423.5	187	SEG[33]	-1395.3	-423.5	227	SEG[73]	-195.3	-423.5
148	COM[91]	-2565.3	-423.5	188	SEG[34]	-1365.3	-423.5	228	SEG[74]	-165.3	-423.5
149	COM[92]	-2535.3	-423.5	189	SEG[35]	-1335.3	-423.5	229	SEG[75]	-135.3	-423.5
150	COM[93]	-2505.3	-423.5	190	SEG[36]	-1305.3	-423.5	230	SEG[76]	-105.3	-423.5
151	COM[94]	-2475.3	-423.5	191	SEG[37]	-1275.3	-423.5	231	SEG[77]	-75.3	-423.5
152	COM[95]	-2445.3	-423.5	192	SEG[38]	-1245.3	-423.5	232	SEG[78]	-45.3	-423.5
153	COMS2	-2415.3	-423.5	193	SEG[39]	-1215.3	-423.5	233	SEG[79]	-15.3	-423.5
154	SEG[0]	-2385.3	-423.5	194	SEG[40]	-1185.3	-423.5	234	SEG[80]	14.7	-423.5
155	SEG[1]	-2355.3	-423.5	195	SEG[41]	-1155.3	-423.5	235	SEG[81]	44.7	-423.5
156	SEG[2]	-2325.3	-423.5	196	SEG[42]	-1125.3	-423.5	236	SEG[82]	74.7	-423.5
157	SEG[3]	-2295.3	-423.5	197	SEG[43]	-1095.3	-423.5	237	SEG[83]	104.7	-423.5
158	SEG[4]	-2265.3	-423.5	198	SEG[44]	-1065.3	-423.5	238	SEG[84]	134.7	-423.5
159	SEG[5]	-2235.3	-423.5	199	SEG[45]	-1035.3	-423.5	239	SEG[85]	164.7	-423.5
160	SEG[6]	-2205.3	-423.5	200	SEG[46]	-1005.3	-423.5	240	SEG[86]	194.7	-423.5

■ PAD Coordinate(1/97 Duty, SHL=1,3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[87]	224.7	-423.5	281	SEG[127]	1424.7	-423.5	321	COM[40]	2624.7	-423.5
242	SEG[88]	254.7	-423.5	282	SEG[128]	1454.7	-423.5	322	COM[39]	2654.7	-423.5
243	SEG[89]	284.7	-423.5	283	SEG[129]	1484.7	-423.5	323	COM[38]	2684.7	-423.5
244	SEG[90]	314.7	-423.5	284	SEG[130]	1514.7	-423.5	324	COM[37]	2714.7	-423.5
245	SEG[91]	344.7	-423.5	285	SEG[131]	1544.7	-423.5	325	COM[36]	2744.7	-423.5
246	SEG[92]	374.7	-423.5	286	SEG[132]	1574.7	-423.5	326	COM[35]	2774.7	-423.5
247	SEG[93]	404.7	-423.5	287	SEG[133]	1604.7	-423.5	327	COM[34]	2804.7	-423.5
248	SEG[94]	434.7	-423.5	288	SEG[134]	1634.7	-423.5	328	COM[33]	2834.7	-423.5
249	SEG[95]	464.7	-423.5	289	SEG[135]	1664.7	-423.5	329	COM[32]	3055	-448.5
250	SEG[96]	494.7	-423.5	290	SEG[136]	1694.7	-423.5	330	COM[31]	3055	-411.1
251	SEG[97]	524.7	-423.5	291	SEG[137]	1724.7	-423.5	331	COM[30]	3055	-373.7
252	SEG[98]	554.7	-423.5	292	SEG[138]	1754.7	-423.5	332	COM[29]	3055	-336.3
253	SEG[99]	584.7	-423.5	293	SEG[139]	1784.7	-423.5	333	COM[28]	3055	-298.9
254	SEG[100]	614.7	-423.5	294	SEG[140]	1814.7	-423.5	334	COM[27]	3055	-261.5
255	SEG[101]	644.7	-423.5	295	SEG[141]	1844.7	-423.5	335	COM[26]	3055	-224.1
256	SEG[102]	674.7	-423.5	296	SEG[142]	1874.7	-423.5	336	COM[25]	3055	-186.7
257	SEG[103]	704.7	-423.5	297	SEG[143]	1904.7	-423.5	337	COM[24]	3055	-149.3
258	SEG[104]	734.7	-423.5	298	SEG[144]	1934.7	-423.5	338	COM[23]	3055	-111.9
259	SEG[105]	764.7	-423.5	299	SEG[145]	1964.7	-423.5	339	COM[22]	3055	-74.5
260	SEG[106]	794.7	-423.5	300	SEG[146]	1994.7	-423.5	340	COM[21]	3055	-37.1
261	SEG[107]	824.7	-423.5	301	SEG[147]	2024.7	-423.5	341	COM[20]	3055	0.3
262	SEG[108]	854.7	-423.5	302	SEG[148]	2054.7	-423.5	342	COM[19]	3055	37.7
263	SEG[109]	884.7	-423.5	303	SEG[149]	2084.7	-423.5	343	COM[18]	3055	75.1
264	SEG[110]	914.7	-423.5	304	SEG[150]	2114.7	-423.5	344	COM[17]	3055	112.5
265	SEG[111]	944.7	-423.5	305	SEG[151]	2144.7	-423.5	345	COM[16]	3055	149.9
266	SEG[112]	974.7	-423.5	306	SEG[152]	2174.7	-423.5	346	COM[15]	3055	187.3
267	SEG[113]	1004.7	-423.5	307	SEG[153]	2204.7	-423.5	347	COM[14]	3055	224.7
268	SEG[114]	1034.7	-423.5	308	SEG[154]	2234.7	-423.5	348	COM[13]	3055	262.1
269	SEG[115]	1064.7	-423.5	309	SEG[155]	2264.7	-423.5	349	COM[12]	3055	299.5
270	SEG[116]	1094.7	-423.5	310	SEG[156]	2294.7	-423.5	350	COM[11]	3055	336.9
271	SEG[117]	1124.7	-423.5	311	SEG[157]	2324.7	-423.5	351	COM[10]	3055	374.3
272	SEG[118]	1154.7	-423.5	312	SEG[158]	2354.7	-423.5	352	COM[9]	3055	411.7
273	SEG[119]	1184.7	-423.5	313	SEG[159]	2384.7	-423.5	353	COM[8]	3055	449.1
274	SEG[120]	1214.7	-423.5	314	COM[47]	2414.7	-423.5				
275	SEG[121]	1244.7	-423.5	315	COM[46]	2444.7	-423.5				
276	SEG[122]	1274.7	-423.5	316	COM[45]	2474.7	-423.5				
277	SEG[123]	1304.7	-423.5	317	COM[44]	2504.7	-423.5				
278	SEG[124]	1334.7	-423.5	318	COM[43]	2534.7	-423.5				
279	SEG[125]	1364.7	-423.5	319	COM[42]	2564.7	-423.5				
280	SEG[126]	1394.7	-423.5	320	COM[41]	2594.7	-423.5				

■ PAD Coordinate(1/65 Duty, SHL=0, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM[56]	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	COM[57]	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	COM[58]	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	COM[59]	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	COM[60]	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	COM[61]	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	COM[62]	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	COM[63]	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	COM[31]	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	COM[30]	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	COM[29]	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	COM[28]	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	COM[27]	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	COM[26]	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	COM[25]	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	COM[24]	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	COM[23]	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	COM[22]	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	COM[21]	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	COM[20]	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	COM[19]	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	COM[18]	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	COM[17]	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	COM[16]	-3055	224.7

■ PAD Coordinate(1/65 Duty, SHL=0, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[15]	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	COM[14]	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	COM[13]	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	COM[12]	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	COM[11]	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	COM[10]	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	COM[9]	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	COM[8]	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[7]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[6]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[5]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[4]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[3]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[2]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[1]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[0]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/65 Duty, SHL=0, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[32]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[33]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[34]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[35]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[36]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[37]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[38]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[39]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	COM[40]	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	COM[41]	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	COM[42]	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	COM[43]	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	COM[44]	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	COM[45]	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	COM[46]	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	COM[47]	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	COM[48]	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	COM[49]	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	COM[50]	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	COM[51]	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	COM[52]	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	COM[53]	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	COM[54]	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	COM[55]	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/65 Duty, SHL=1, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM[7]	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	COM[6]	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	COM[5]	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	COM[4]	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	COM[3]	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	COM[2]	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	COM[1]	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	COM[0]	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RST	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	COM[32]	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	COM[33]	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	COM[34]	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	COM[35]	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	COM[36]	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	COM[37]	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	COM[38]	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	COM[39]	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	COM[40]	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	COM[41]	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	COM[42]	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	COM[43]	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	COM[44]	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	COM[45]	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	COM[46]	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	COM[47]	-3055	224.7

■ PAD Coordinate(1/65 Duty, SHL=1, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[48]	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	COM[49]	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	COM[50]	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	COM[51]	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	COM[52]	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	COM[53]	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	COM[54]	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	COM[55]	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[56]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[57]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[58]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[59]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[60]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[61]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[62]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[63]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/65 Duty, SHL=1, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[31]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[30]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[29]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[28]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[27]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[26]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[25]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[24]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	COM[23]	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	COM[22]	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	COM[21]	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	COM[20]	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	COM[19]	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	COM[18]	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	COM[17]	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	COM[16]	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	COM[15]	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	COM[14]	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	COM[13]	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	COM[12]	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	COM[11]	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	COM[10]	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	COM[9]	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	COM[8]	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/33 Duty, SHL=0, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM[24]	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	COM[25]	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	COM[26]	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	COM[27]	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	COM[28]	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	COM[29]	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	COM[30]	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	COM[31]	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	COM[31]	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	COM[30]	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	COM[29]	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	COM[28]	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	COM[27]	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	COM[26]	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	COM[25]	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	COM[24]	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	COM[23]	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	COM[22]	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	COM[21]	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	COM[20]	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	COM[19]	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	COM[18]	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	COM[17]	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	COM[16]	-3055	224.7

■ PAD Coordinate(1/33 Duty, SHL=0, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[15]	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	COM[14]	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	COM[13]	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	COM[12]	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	COM[11]	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	COM[10]	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	COM[9]	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	COM[8]	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[7]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[6]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[5]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[4]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[3]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[2]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[1]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[0]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/33 Duty, SHL=0, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[0]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[1]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[2]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[3]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[4]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[5]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[6]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[7]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	COM[8]	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	COM[9]	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	COM[10]	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	COM[11]	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	COM[12]	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	COM[13]	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	COM[14]	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	COM[15]	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	COM[16]	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	COM[17]	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	COM[18]	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	COM[19]	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	COM[20]	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	COM[21]	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	COM[22]	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	COM[23]	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/33 Duty, SHL=1, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	COM[7]	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	COM[6]	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	COM[5]	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	COM[4]	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	COM[3]	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	COM[2]	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	COM[1]	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	COM[0]	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	COM[0]	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	COM[1]	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	COM[2]	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	COM[3]	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	COM[4]	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	COM[5]	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	COM[6]	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	COM[7]	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	COM[8]	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	COM[9]	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	COM[10]	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	COM[11]	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	COM[12]	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	COM[13]	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	COM[14]	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	COM[15]	-3055	224.7

■ PAD Coordinate(1/33 Duty, SHL=1, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[16]	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	COM[17]	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	COM[18]	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	COM[19]	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	COM[20]	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	COM[21]	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	COM[22]	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	COM[23]	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[24]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[25]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[26]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[27]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[28]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[29]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[30]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[31]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/33 Duty, SHL=1, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[31]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[30]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[29]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[28]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[27]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[26]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[25]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[24]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	COM[23]	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	COM[22]	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	COM[21]	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	COM[20]	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	COM[19]	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	COM[18]	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	COM[17]	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	COM[16]	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	COM[15]	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	COM[14]	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	COM[13]	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	COM[12]	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	COM[11]	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	COM[10]	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	COM[9]	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	COM[8]	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/17 Duty, SHL=0, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

■ PAD Coordinate(1/17 Duty, SHL=0, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[15]	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	COM[14]	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	COM[13]	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	COM[12]	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	COM[11]	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	COM[10]	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	COM[9]	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	COM[8]	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[7]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[6]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[5]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[4]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[3]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[2]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[1]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[0]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/17 Duty, SHL=0, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[0]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[1]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[2]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[3]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[4]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[5]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[6]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[7]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	COM[8]	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	COM[9]	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	COM[10]	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	COM[11]	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	COM[12]	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	COM[13]	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	COM[14]	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	COM[15]	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/17 Duty, SHL=1, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

■ PAD Coordinate(1/17 Duty, SHL=1, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	COM[0]	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	COM[1]	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	COM[2]	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	COM[3]	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	COM[4]	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	COM[5]	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	COM[6]	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	COM[7]	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[8]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[9]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[10]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[11]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[12]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[13]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[14]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[15]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/17 Duty, SHL=1, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[15]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[14]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[13]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[12]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[11]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[10]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[9]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[8]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	COM[7]	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	COM[6]	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	COM[5]	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	COM[4]	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	COM[3]	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	COM[2]	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	COM[1]	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	COM[0]	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/9 Duty, SHL=0, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

■ PAD Coordinate(1/9 Duty, SHL=0, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	NC	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	NC	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	NC	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	NC	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	NC	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	NC	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	NC	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	NC	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[7]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[6]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[5]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[4]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[3]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[2]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[1]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[0]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/9 Duty, SHL=0, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[0]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[1]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[2]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[3]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[4]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[5]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[6]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[7]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	NC	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	NC	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	NC	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	NC	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	NC	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	NC	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	NC	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	NC	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/9 Duty, SHL=1, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

■ PAD Coordinate(1/9 Duty, SHL=1, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	NC	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	NC	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	NC	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	NC	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	NC	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	NC	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	NC	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	NC	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	COM[0]	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	COM[1]	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	COM[2]	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	COM[3]	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[4]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[5]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[6]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[7]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/9 Duty, SHL=1, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[7]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[6]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[5]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[4]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	COM[3]	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	COM[2]	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	COM[1]	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	COM[0]	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	NC	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	NC	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	NC	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	NC	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	NC	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	NC	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	NC	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	NC	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/5 Duty, SHL=0, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

■ PAD Coordinate(1/5 Duty, SHL=0, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	NC	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	NC	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	NC	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	NC	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	NC	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	NC	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	NC	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	NC	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	NC	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	NC	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	NC	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	NC	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[3]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[2]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[1]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[0]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/5 Duty, SHL=0, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[0]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[1]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[2]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[3]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	NC	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	NC	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	NC	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	NC	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	NC	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	NC	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	NC	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	NC	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	NC	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	NC	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	NC	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	NC	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(1/5 Duty, SHL=1, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

■ PAD Coordinate(1/5 Duty, SHL=1, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	NC	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	NC	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	NC	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	NC	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	NC	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	NC	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	NC	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	NC	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	NC	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	NC	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	NC	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	NC	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	COM[0]	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	COM[1]	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	COM[2]	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	COM[3]	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(1/5 Duty, SHL=1, 3-3)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	COM[3]	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	COM[2]	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	COM[1]	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	COM[0]	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	NC	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	NC	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	NC	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	NC	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	NC	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	NC	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	NC	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	NC	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	NC	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	NC	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	NC	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	NC	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ PAD Coordinate(Static, SHL=0, 3-1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	2843.23	445	41	VOUT	843.94	459.4	81	T[7]	-1197.58	459.4
2	NC	2805.83	445	42	VOUT	793.94	459.4	82	T[6]	-1247.58	459.4
3	NC	2768.43	445	43	VOUT	743.94	459.4	83	T[5]	-1297.58	459.4
4	NC	2731.03	445	44	VOUT	693.94	459.4	84	T[4]	-1347.58	459.4
5	NC	2693.63	445	45	CAP5P	637.84	459.4	85	T[3]	-1397.58	459.4
6	NC	2656.23	445	46	CAP5P	587.84	459.4	86	T[2]	-1447.58	459.4
7	NC	2618.83	445	47	CAP1N	537.84	459.4	87	T[1]	-1497.58	459.4
8	NC	2581.43	445	48	CAP1N	487.84	459.4	88	T[0]	-1547.58	459.4
9	COMS1	2544.03	445	49	CAP3P	437.84	459.4	89	VDD	-1599.67	459.4
10	STACOM	2424.72	459.4	50	CAP3P	387.84	459.4	90	CLS	-1653.75	459.4
11	VSS	2370.61	459.4	51	CAP1N	337.84	459.4	91	VSS	-1705.84	459.4
12	CS1B	2318.55	459.4	52	CAP1N	287.84	459.4	92	C86	-1759.92	459.4
13	CS2	2268.55	459.4	53	CAP1P	237.84	459.4	93	VDD	-1812.01	459.4
14	VDD	2214.47	459.4	54	CAP1P	187.84	459.4	94	PSB	-1866.09	459.4
15	RSTP	2162.38	459.4	55	CAP2P	137.84	459.4	95	VSS	-1918.18	459.4
16	A0	2112.38	459.4	56	CAP2P	87.84	459.4	96	IRS	-1972.26	459.4
17	VSS	2058.3	459.4	57	CAP2N	37.84	459.4	97	VDD	-2024.35	459.4
18	RW(XWR)	2006.21	459.4	58	CAP2N	-12.16	459.4	98	SEL1	-2078.43	459.4
19	E(XRD)	1956.21	459.4	59	CAP4P	-62.16	459.4	99	VSS	-2130.52	459.4
20	VDD	1902.13	459.4	60	CAP4P	-112.16	459.4	100	SEL2	-2184.6	459.4
21	D0	1850.04	459.4	61	CAP2N	-162.16	459.4	101	VDD	-2236.69	459.4
22	D1	1800.04	459.4	62	CAP2N	-212.16	459.4	102	SEL3	-2290.77	459.4
23	D2	1750.04	459.4	63	CAP6P	-262.16	459.4	103	VSS	-2340.77	459.4
24	D3	1700.04	459.4	64	CAP6P	-312.16	459.4	104	V0	-2396.87	459.4
25	D4	1650.04	459.4	65	VSS	-371.7	459.4	105	NC	-2544.03	445
26	D5	1600.04	459.4	66	VRS	-424.72	459.4	106	NC	-2581.43	445
27	D6	1550.04	459.4	67	VDD	-477.72	459.4	107	NC	-2618.83	445
28	D7	1500.04	459.4	68	V4	-535.04	459.4	108	NC	-2656.23	445
29	VDD	1450.04	459.4	69	V4	-585.04	459.4	109	NC	-2693.63	445
30	VDD	1400.04	459.4	70	V3	-635.04	459.4	110	NC	-2731.03	445
31	VDD	1350.04	459.4	71	V3	-685.04	459.4	111	NC	-2768.43	445
32	VDD	1300.04	459.4	72	V2	-735.04	459.4	112	NC	-2805.83	445
33	VDD2	1250.04	459.4	73	V2	-785.04	459.4	113	NC	-2843.23	445
34	VDD2	1200.04	459.4	74	V1	-835.04	459.4	114	NC	-3055	449.1
35	VDD2	1150.04	459.4	75	V1	-885.04	459.4	115	NC	-3055	411.7
36	VDD2	1100.04	459.4	76	V0	-935.04	459.4	116	NC	-3055	374.3
37	VSS	1050.04	459.4	77	V0	-985.04	459.4	117	NC	-3055	336.9
38	VSS	1000.04	459.4	78	VRAB	-1035.04	459.4	118	NC	-3055	299.5
39	VSS	950.04	459.4	79	VDD	-1097.58	459.4	119	NC	-3055	262.1
40	VSS	900.04	459.4	80	T[8]	-1147.58	459.4	120	NC	-3055	224.7

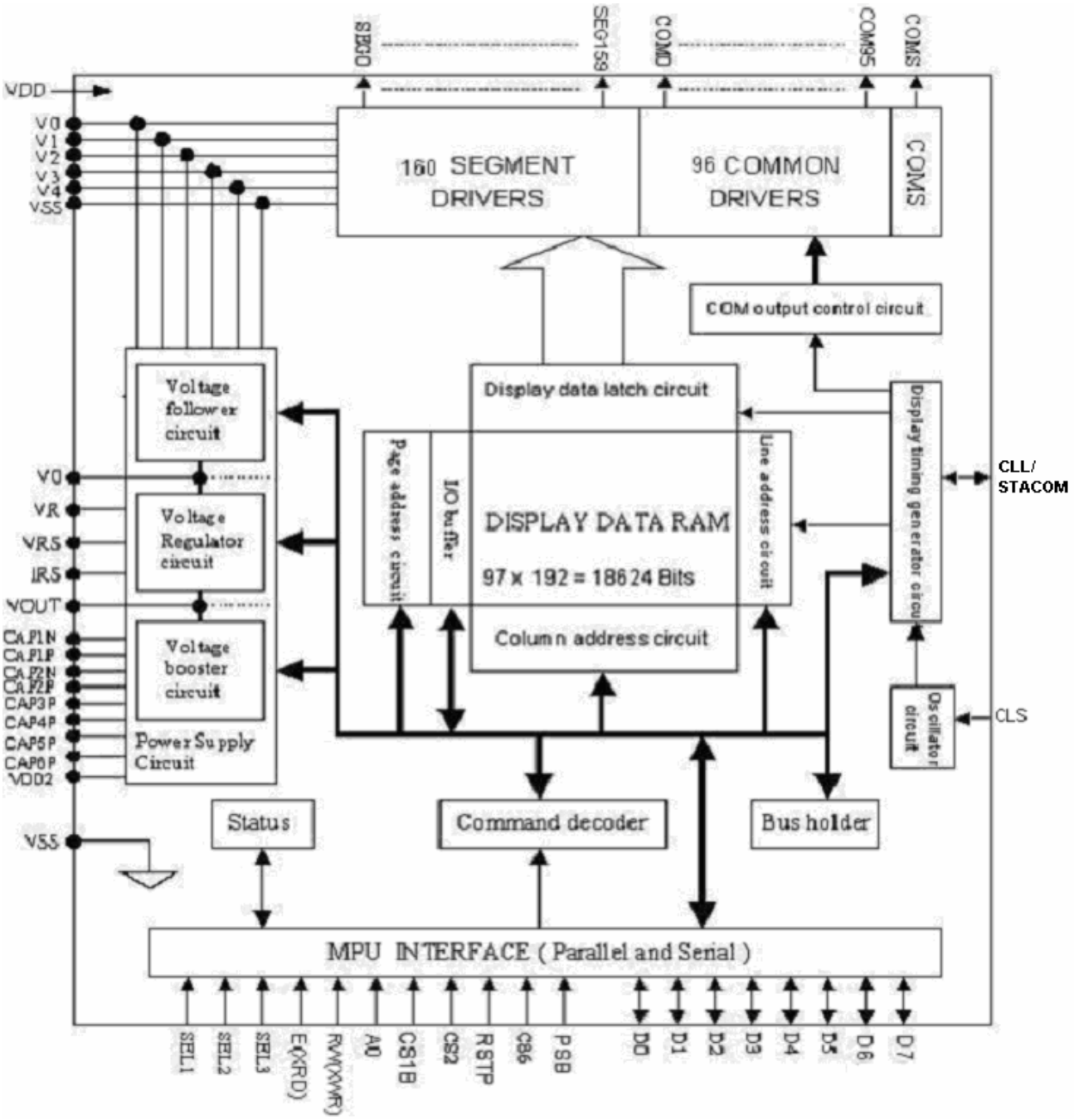
■ PAD Coordinate(Static, SHL=0, 3-2)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	NC	-3055	187.3	161	SEG[23]	-2175.3	-423.5	201	SEG[63]	-975.3	-423.5
122	NC	-3055	149.9	162	SEG[24]	-2145.3	-423.5	202	SEG[64]	-945.3	-423.5
123	NC	-3055	112.5	163	SEG[25]	-2115.3	-423.5	203	SEG[65]	-915.3	-423.5
124	NC	-3055	75.1	164	SEG[26]	-2085.3	-423.5	204	SEG[66]	-885.3	-423.5
125	NC	-3055	37.7	165	SEG[27]	-2055.3	-423.5	205	SEG[67]	-855.3	-423.5
126	NC	-3055	0.3	166	SEG[28]	-2025.3	-423.5	206	SEG[68]	-825.3	-423.5
127	NC	-3055	-37.1	167	SEG[29]	-1995.3	-423.5	207	SEG[69]	-795.3	-423.5
128	NC	-3055	-74.5	168	SEG[30]	-1965.3	-423.5	208	SEG[70]	-765.3	-423.5
129	NC	-3055	-111.9	169	SEG[31]	-1935.3	-423.5	209	SEG[71]	-735.3	-423.5
130	NC	-3055	-149.3	170	SEG[32]	-1905.3	-423.5	210	SEG[72]	-705.3	-423.5
131	NC	-3055	-186.7	171	SEG[33]	-1875.3	-423.5	211	SEG[73]	-675.3	-423.5
132	NC	-3055	-224.1	172	SEG[34]	-1845.3	-423.5	212	SEG[74]	-645.3	-423.5
133	NC	-3055	-261.5	173	SEG[35]	-1815.3	-423.5	213	SEG[75]	-615.3	-423.5
134	NC	-3055	-298.9	174	SEG[36]	-1785.3	-423.5	214	SEG[76]	-585.3	-423.5
135	NC	-3055	-336.3	175	SEG[37]	-1755.3	-423.5	215	SEG[77]	-555.3	-423.5
136	NC	-3055	-373.7	176	SEG[38]	-1725.3	-423.5	216	SEG[78]	-525.3	-423.5
137	COMS2	-3055	-411.1	177	SEG[39]	-1695.3	-423.5	217	SEG[79]	-495.3	-423.5
138	SEG[0]	-3055	-448.5	178	SEG[40]	-1665.3	-423.5	218	SEG[80]	-465.3	-423.5
139	SEG[1]	-2835.3	-423.5	179	SEG[41]	-1635.3	-423.5	219	SEG[81]	-435.3	-423.5
140	SEG[2]	-2805.3	-423.5	180	SEG[42]	-1605.3	-423.5	220	SEG[82]	-405.3	-423.5
141	SEG[3]	-2775.3	-423.5	181	SEG[43]	-1575.3	-423.5	221	SEG[83]	-375.3	-423.5
142	SEG[4]	-2745.3	-423.5	182	SEG[44]	-1545.3	-423.5	222	SEG[84]	-345.3	-423.5
143	SEG[5]	-2715.3	-423.5	183	SEG[45]	-1515.3	-423.5	223	SEG[85]	-315.3	-423.5
144	SEG[6]	-2685.3	-423.5	184	SEG[46]	-1485.3	-423.5	224	SEG[86]	-285.3	-423.5
145	SEG[7]	-2655.3	-423.5	185	SEG[47]	-1455.3	-423.5	225	SEG[87]	-255.3	-423.5
146	SEG[8]	-2625.3	-423.5	186	SEG[48]	-1425.3	-423.5	226	SEG[88]	-225.3	-423.5
147	SEG[9]	-2595.3	-423.5	187	SEG[49]	-1395.3	-423.5	227	SEG[89]	-195.3	-423.5
148	SEG[10]	-2565.3	-423.5	188	SEG[50]	-1365.3	-423.5	228	SEG[90]	-165.3	-423.5
149	SEG[11]	-2535.3	-423.5	189	SEG[51]	-1335.3	-423.5	229	SEG[91]	-135.3	-423.5
150	SEG[12]	-2505.3	-423.5	190	SEG[52]	-1305.3	-423.5	230	SEG[92]	-105.3	-423.5
151	SEG[13]	-2475.3	-423.5	191	SEG[53]	-1275.3	-423.5	231	SEG[93]	-75.3	-423.5
152	SEG[14]	-2445.3	-423.5	192	SEG[54]	-1245.3	-423.5	232	SEG[94]	-45.3	-423.5
153	SEG[15]	-2415.3	-423.5	193	SEG[55]	-1215.3	-423.5	233	SEG[95]	-15.3	-423.5
154	SEG[16]	-2385.3	-423.5	194	SEG[56]	-1185.3	-423.5	234	SEG[96]	14.7	-423.5
155	SEG[17]	-2355.3	-423.5	195	SEG[57]	-1155.3	-423.5	235	SEG[97]	44.7	-423.5
156	SEG[18]	-2325.3	-423.5	196	SEG[58]	-1125.3	-423.5	236	SEG[98]	74.7	-423.5
157	SEG[19]	-2295.3	-423.5	197	SEG[59]	-1095.3	-423.5	237	SEG[99]	104.7	-423.5
158	SEG[20]	-2265.3	-423.5	198	SEG[60]	-1065.3	-423.5	238	SEG[100]	134.7	-423.5
159	SEG[21]	-2235.3	-423.5	199	SEG[61]	-1035.3	-423.5	239	SEG[101]	164.7	-423.5
160	SEG[22]	-2205.3	-423.5	200	SEG[62]	-1005.3	-423.5	240	SEG[102]	194.7	-423.5

■ PAD Coordinate(Static, SHL=0, 3-3)

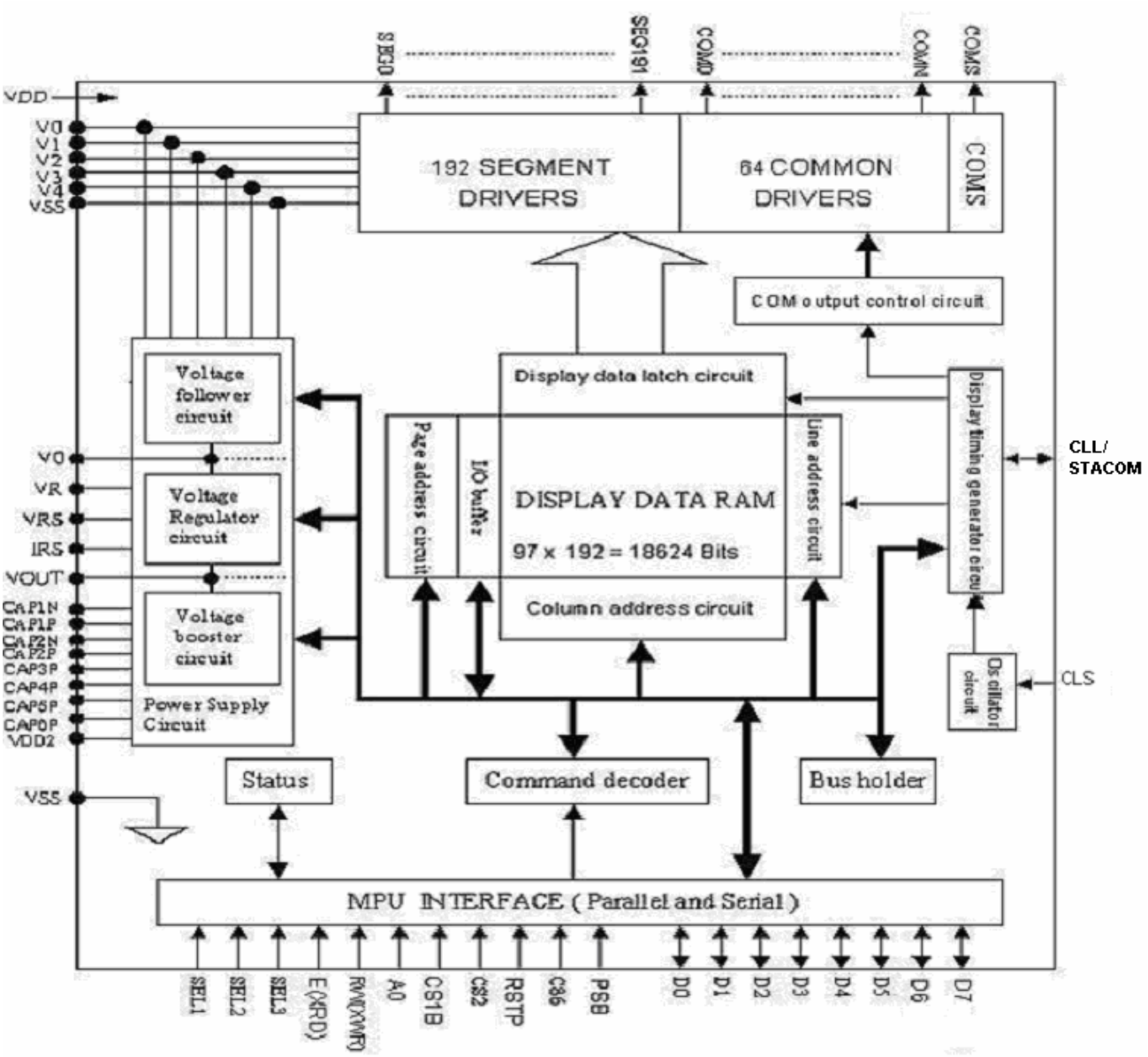
Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	SEG[103]	224.7	-423.5	281	SEG[143]	1424.7	-423.5	321	SEG[183]	2624.7	-423.5
242	SEG[104]	254.7	-423.5	282	SEG[144]	1454.7	-423.5	322	SEG[184]	2654.7	-423.5
243	SEG[105]	284.7	-423.5	283	SEG[145]	1484.7	-423.5	323	SEG[185]	2684.7	-423.5
244	SEG[106]	314.7	-423.5	284	SEG[146]	1514.7	-423.5	324	SEG[186]	2714.7	-423.5
245	SEG[107]	344.7	-423.5	285	SEG[147]	1544.7	-423.5	325	SEG[187]	2744.7	-423.5
246	SEG[108]	374.7	-423.5	286	SEG[148]	1574.7	-423.5	326	SEG[188]	2774.7	-423.5
247	SEG[109]	404.7	-423.5	287	SEG[149]	1604.7	-423.5	327	SEG[189]	2804.7	-423.5
248	SEG[110]	434.7	-423.5	288	SEG[150]	1634.7	-423.5	328	SEG[190]	2834.7	-423.5
249	SEG[111]	464.7	-423.5	289	SEG[151]	1664.7	-423.5	329	SEG[191]	3055	-448.5
250	SEG[112]	494.7	-423.5	290	SEG[152]	1694.7	-423.5	330	NC	3055	-411.1
251	SEG[113]	524.7	-423.5	291	SEG[153]	1724.7	-423.5	331	NC	3055	-373.7
252	SEG[114]	554.7	-423.5	292	SEG[154]	1754.7	-423.5	332	NC	3055	-336.3
253	SEG[115]	584.7	-423.5	293	SEG[155]	1784.7	-423.5	333	NC	3055	-298.9
254	SEG[116]	614.7	-423.5	294	SEG[156]	1814.7	-423.5	334	NC	3055	-261.5
255	SEG[117]	644.7	-423.5	295	SEG[157]	1844.7	-423.5	335	NC	3055	-224.1
256	SEG[118]	674.7	-423.5	296	SEG[158]	1874.7	-423.5	336	NC	3055	-186.7
257	SEG[119]	704.7	-423.5	297	SEG[159]	1904.7	-423.5	337	NC	3055	-149.3
258	SEG[120]	734.7	-423.5	298	SEG[160]	1934.7	-423.5	338	NC	3055	-111.9
259	SEG[121]	764.7	-423.5	299	SEG[161]	1964.7	-423.5	339	NC	3055	-74.5
260	SEG[122]	794.7	-423.5	300	SEG[162]	1994.7	-423.5	340	NC	3055	-37.1
261	SEG[123]	824.7	-423.5	301	SEG[163]	2024.7	-423.5	341	NC	3055	0.3
262	SEG[124]	854.7	-423.5	302	SEG[164]	2054.7	-423.5	342	NC	3055	37.7
263	SEG[125]	884.7	-423.5	303	SEG[165]	2084.7	-423.5	343	NC	3055	75.1
264	SEG[126]	914.7	-423.5	304	SEG[166]	2114.7	-423.5	344	NC	3055	112.5
265	SEG[127]	944.7	-423.5	305	SEG[167]	2144.7	-423.5	345	NC	3055	149.9
266	SEG[128]	974.7	-423.5	306	SEG[168]	2174.7	-423.5	346	NC	3055	187.3
267	SEG[129]	1004.7	-423.5	307	SEG[169]	2204.7	-423.5	347	NC	3055	224.7
268	SEG[130]	1034.7	-423.5	308	SEG[170]	2234.7	-423.5	348	NC	3055	262.1
269	SEG[131]	1064.7	-423.5	309	SEG[171]	2264.7	-423.5	349	NC	3055	299.5
270	SEG[132]	1094.7	-423.5	310	SEG[172]	2294.7	-423.5	350	NC	3055	336.9
271	SEG[133]	1124.7	-423.5	311	SEG[173]	2324.7	-423.5	351	NC	3055	374.3
272	SEG[134]	1154.7	-423.5	312	SEG[174]	2354.7	-423.5	352	NC	3055	411.7
273	SEG[135]	1184.7	-423.5	313	SEG[175]	2384.7	-423.5	353	NC	3055	449.1
274	SEG[136]	1214.7	-423.5	314	SEG[176]	2414.7	-423.5				
275	SEG[137]	1244.7	-423.5	315	SEG[177]	2444.7	-423.5				
276	SEG[138]	1274.7	-423.5	316	SEG[178]	2474.7	-423.5				
277	SEG[139]	1304.7	-423.5	317	SEG[179]	2504.7	-423.5				
278	SEG[140]	1334.7	-423.5	318	SEG[180]	2534.7	-423.5				
279	SEG[141]	1364.7	-423.5	319	SEG[181]	2564.7	-423.5				
280	SEG[142]	1394.7	-423.5	320	SEG[182]	2594.7	-423.5				

■ BLOCK DIAGRAM (DUTY=1/97)

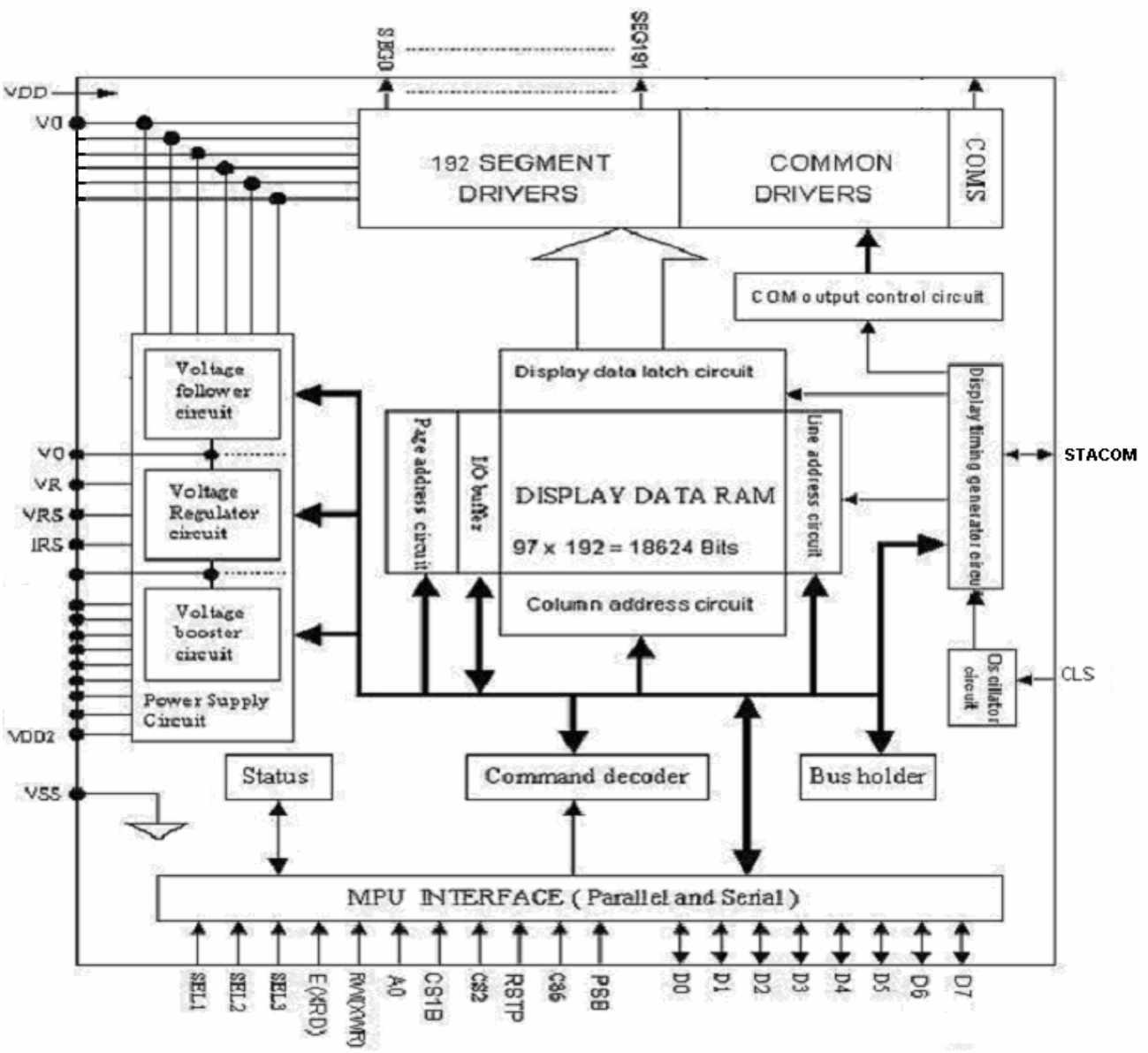


■ BLOCK DIAGRAM (DUTY=1/65,1/33,1/17,1/9,1/5)

COMMON=64,32,16,8,4 for different duty selection



■ BLOCK DIAGRAM (Static)



■ PIN DESCRIPITON

◆ Power Supply Pin

Pin Name	I/O	Function	No. of Pins
VDD	Power Supply	Power supply	4
VDD2	Power Supply	Power supply for DC-DC Converter	4
VSS	Power Supply	Ground	4
VRS	Power Supply	This is the internal-output VREG power supply for the LCD power supply voltage regulator.	1
V0, V1, V2, V3, V4	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VSS, and must maintain the relative magnitudes shown below. V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧VSS When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.	11

◆ LCD Power Supply Pin

Pin Name	I/O	Function	No. of Pins
CAP1P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
CAP1N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.	4
CAP2P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
CAP2N	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.	4
CAP3P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
CAP4P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
CAP5P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	2
CAP6P	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	2
VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD	2
VRAB	I	Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider. IRS = “L” : the V0 voltage regulator internal resistors are not used . IRS = “H” : the V0 voltage regulator internal resistors are used .	1

◆ System Bus Connection Pin

Pin Name	I/O	Function	No. of Pins
D0 to D7	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. --- When the 4/3 line serial interface is selected (PSB= “L”,C86=”H”) : D7: serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 are set to high impedance. When the chip select is not active, D0 to D7 are set to high impedance. --- When the IIC serial interface selected (PSB=”L”, C86=”L”); D7: serial clock input (SCL) D6 , D5 , D4: serial input data (SDA_IN) D3, D2: (SDA_OUT) serial data acknowledge for the IIC interface. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully IIC interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible during the acknowledge cycle the RW1092 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level. **D6, D5, ….D2 must be connected together (SDA)** D1, D0: Is slave address (SA) bit1, 0, must connect to VDD or VSS. When chip select is not active, D0 to D7 is high impedance.	8
A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.	1
RSTP	I	When RSTP is set to “L,” the settings are initialized. The reset operation is performed by the RSTP signal level.	1
CS1B CS2	I	This is the chip select signal. When CS1B = “L” and CS2 = “H,” then the chip select becomes active, and data/command I/O is enabled.	2
E(XRD)	I	• When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the XRD signal of the 8080 MPU, and the RW1092 series data bus is in an output status when this signal is “L”. • When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.	1
RW(XWR)	I	• When connected to an 8080 MPU, this is active LOW. RW This terminal connects to the 8080 MPU XWR signal. The signals on the data bus are latched at the rising edge of the XWR signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When RW = “H”: Read. When RW = “L”: Write.	1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>PSB,C86</td><td></td><td>Interface selection pins
<table><tr><td>PSB , C86</td><td>Interface</td></tr><tr><td>0 , 0</td><td>IIC</td></tr><tr><td>0 , 1</td><td>SPI4/SPI3</td></tr><tr><td>1 , 0</td><td>8-bit parallel 8080 series MPU</td></tr><tr><td>1 , 1</td><td>8-bit parallel 6800series MPU</td></tr></table></td><td></td></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS = “H” : used Internal oscillator circuit , STACOM output mode enable
CLS = “L” : used external clock input .(internal oscillator is disable)
When CLS = “L”, input the display clock through the STACOM terminal.</td><td>1</td></tr>
<tr><td>STACOM</td><td>I/O</td><td>This is the Static display Common Output or clock input terminal.(selected by software)
<table><tr><th>CLS</th><th>STACOM</th></tr><tr><td>“H”
“L”</td><td>Output
Input</td></tr></table></td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V0 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VRAB terminal</td><td>1</td></tr>
<tr><td>SEL3
SEL2
SEL1</td><td>I</td><td>These pins are DUTY selection.
<table><tr><td rowspan="2">SEL 3 , 2 , 1</td><td rowspan="2">DUTY</td><td>BE=0</td><td>BE=1</td></tr><tr><td>BIAS=(0,1)</td><td>BIAS=(0,1)</td></tr><tr><td>0 , 0 , 0</td><td>static</td><td>1/2</td><td>-</td></tr><tr><td>0 , 0 , 0</td><td>1/5</td><td>1/3, 1/2</td><td>-</td></tr><tr><td>0 , 0 , 1</td><td>1/9</td><td>1/5, 1/4</td><td>1/3, 1/2</td></tr><tr><td>0 , 1 , 0</td><td>1/17</td><td>1/5, 1/4</td><td>1/3, 1/2</td></tr><tr><td>0 , 1 , 1</td><td>1/33</td><td>1/6, 1/4</td><td>1/5 , 1/3</td></tr><tr><td>1 , 0 , 0</td><td>1/65(S1065)</td><td>1/9, 1/7</td><td>1/8, 1/6</td></tr><tr><td>1 , 0 , 1</td><td>1/65(S1575)</td><td>1/9, 1/7</td><td>1/8, 1/6</td></tr><tr><td>1 , 1 , 0</td><td>1/65</td><td>1/9, 1/7</td><td>1/8, 1/6</td></tr><tr><td>1, 1 , 1</td><td>1/97</td><td>1/10, 1/8</td><td>1/9, 1/7</td></tr></table></td><td>3</td></tr>
<tr><td>TEST0 ~ 8</td><td>I</td><td>These are terminals for IC testing.
They are set to open.</td><td>9</td></tr>
</table>

◆ LCD Driver Pin

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEGn</td><td>O</td><td>These are the LCD segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from VSS, V3, V2, and V0.
n=191 for Duty 1/65,1/33, 1/17, 1/9, 1/5
n=159 for Duty 1/97
<table>
<tr><th rowspan="2">RAM DATA</th><th rowspan="2">FR</th><th colspan="2">Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td>Power save</td><td>L</td><td colspan="2">VSS</td></tr>
</table></td><td>192</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>Through a combination of the contents of the scan data and with the FR signal, a single level is selected from VSS, V4, V1, and V0.
n=63, 31, 15, 7, 4 for Duty 1/65,1/33, 1/17, 1/9, 1/5
n=95 for Duty 1/97
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td>Power save</td><td>L</td><td>VSS</td></tr>
</table></td><td>67</td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.</td><td>2</td></tr>
</table>

RW1092 I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
C86 , PSB ,SEL1,SEL2,SEL3 , CLS ,IRS	No Limitation
TEST0…8	Floating
VDD, VDD2,VSS, VRS, VOUT ,V0, VRAB	<100Ω
CS1B ,CS2 ,STACOM, E(XRD) , RW(XWR) , A0 , D0 …D7	<1KΩ
V1 , V2 , V3 , V4 , CAP1P , CAP1N , CAP2P , CAP2N , CAP3P , CAP4P , CAP5P,CAP6P	<500Ω
RSTP	<10KΩ

■ DESCRIPTION OF FUNCTION

◆ The MPU Interface

● Selecting the Interface Type

With the RW1092 chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). Through selecting the PSB/ C86 terminal polarity to the “H” or “L” it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

Interface	PSB	C86	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
6800	H	H	CS1B	CS2	A0	E	RW	D7	D6	D5~D0
8080	H	L	CS1B	CS2	A0	XRD	XWR	D7	D6	D5~ D0
4SPI	L	H	CS1B	H	A0	—	—	SI	SCL	(HZ)
3SPI	L	H	CS1B	H	L	—	—	SI	SCL	(HZ)
IIC	L	L	—	—	—	—	—	SCL	SDA_IN:D6~D5 SDA_OUT: D3~D2 SA[1:0]: D1~ D0	

“—” indicates fixed to either “H” or to “L”

● The Parallel Interface

When the parallel interface has been selected (PSB=“H”), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (shown in Table 2) by selecting the C86 terminal to either “H” or to “L”.

Table 2

C86 (PSB=H)	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7~D0
H: 6800 Series	CS1B	CS2	A0	E	RW	D7~D0
L: 8080 Series	CS1B	CS2	A0	XRD	XWR	D7~D0

Moreover, data bus signals are recognized by a combination of A0, XRD (E), XWR (RW) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	RW	XRD	XWR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

● The 4-SPI Serial Interface (PSB="L", C86="H")

When the 4-SPI serial interface has been selected then when the chip is in active state (CS1B = "L" and CS2 = "H") the serial data input SI(DB7) and the serial clock input SCL(DB6) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.

The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is a serial interface signal chart.

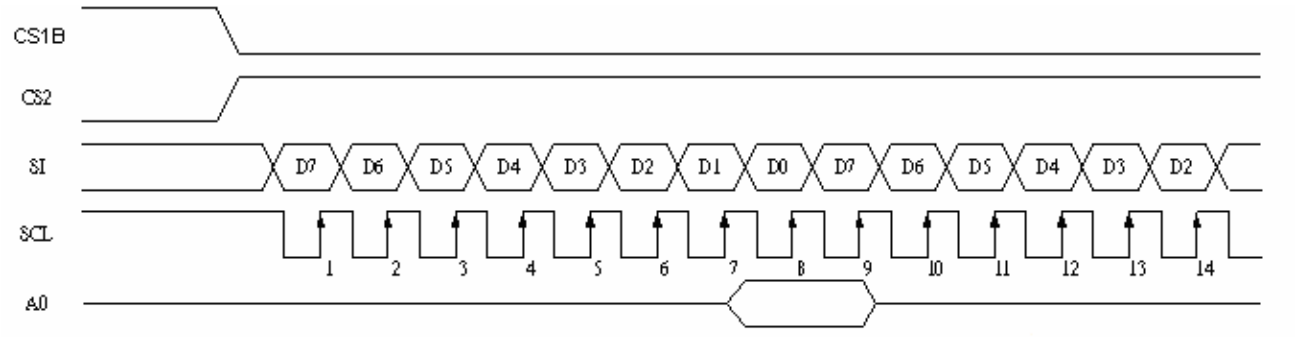


Figure 1

● The 3-SPI Serial Interface (PSB="L", C86="H")

If 3-Pin SPI mode is selected then when the chip is in active state (CS1B = "L" and CS2 = "H") , SI (DB7), and SCLK (DB6) are used. they are serial input data, and serial clock input, relatively. 3-Pin SPI mode does not use A0 for data/instruction selection.

Data length instruction should be used to realize data/instruction and data length instruction also indicates length of data. The example of timing sequence is shown below, data length instruction is followed by data set.

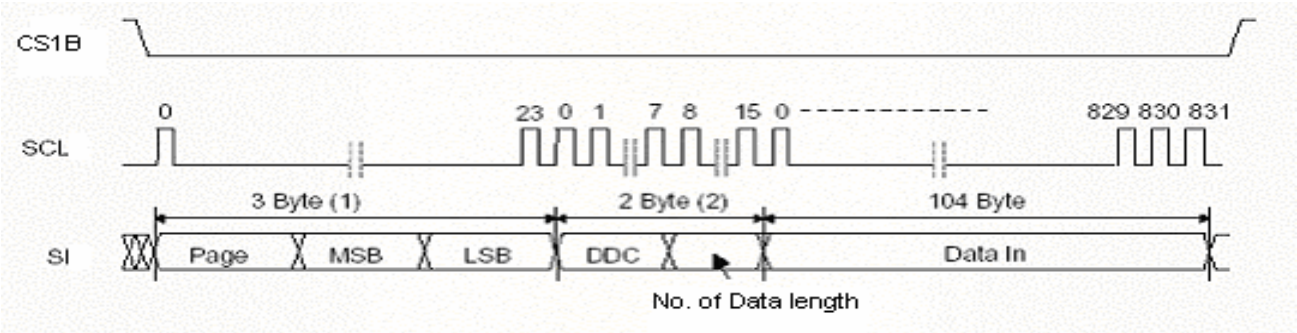


Figure 2

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

● IIC Interface(PSB="L", C86="L")

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules.

The two lines are a Serial Data line SDA and a Serial Clock line SCL. Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

➢ BIT Transfer

One data bit is transferred during each clock pulse. The data on the SDA(DB6) line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 1.

➢ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 2

➢ SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 3.
· Transmitter: the device, which sends the data to the bus.
· Receiver: the device, which receives the data from the bus.
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.
· Slave: the device addressed by a master.
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
· Synchronization: procedure to synchronize the clock signals of two or more devices.

➢ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Figure 4.

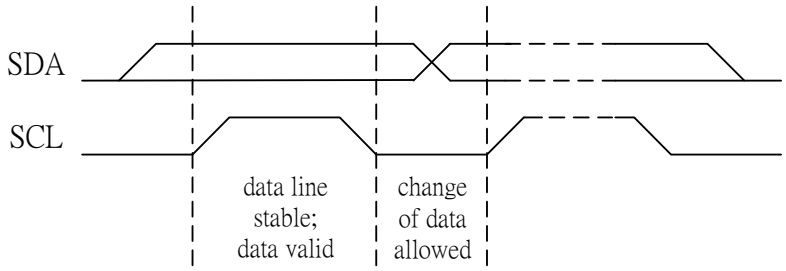


Figure 1 Bit transfer

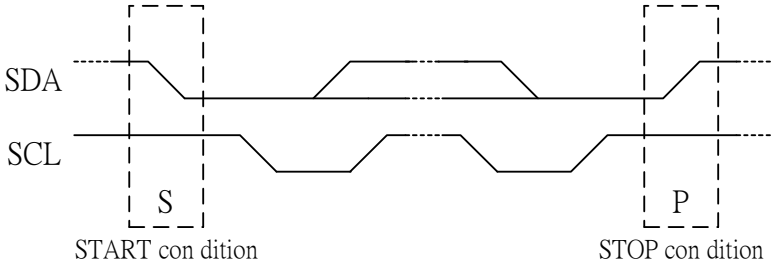


Figure 2 Definition of START and STOP conditions

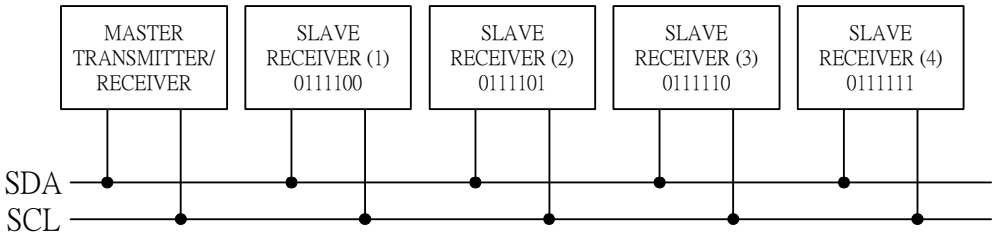


Figure 3 System configuration

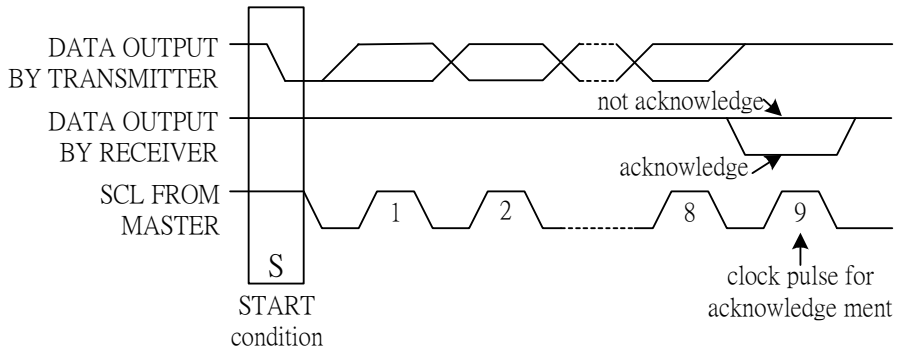


Figure 4 Acknowledgement on the 2-line Interface

➢ IIC Interface Protocol

The RW1092 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1092. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (VSS) or logic 1 (VDD).
The IIC Interface protocol is illustrated in Figure 5.

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1092 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

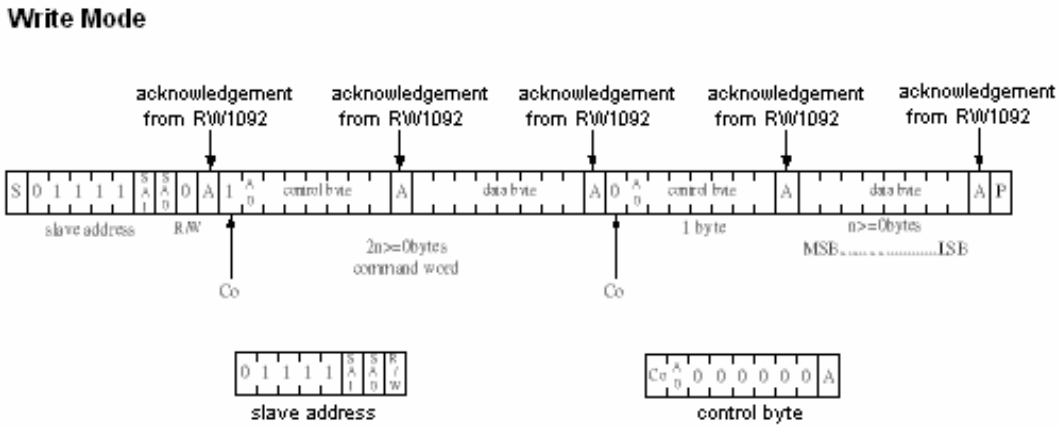


Figure 5 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

◆ The Chip Select

The RW1092 have two chip select terminals: CS1B and CS2. The MPU interface or the serial interface is enabled only when CS1B = “L” and CS2 = “H”.

When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, XRD, and XWR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

◆ The Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (tCYC) requirement alone in accessing the RW1092. Wait time may not be considered.

And, in the RW1092, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus. Internal data bus.

For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.

There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.

This relationship is shown in Figure 8.

◆ The Busy Flag

When the busy flag is “1” it indicates that the RW1092 is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

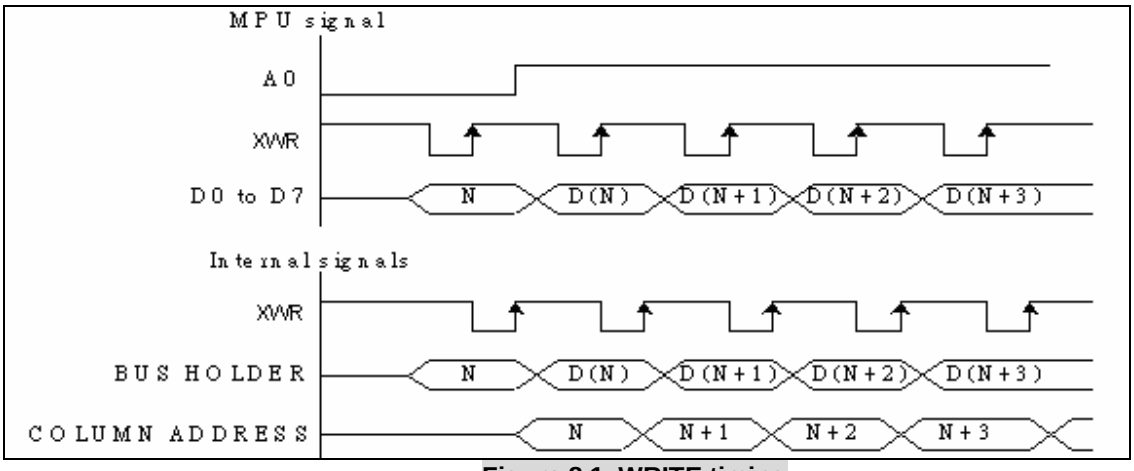


Figure 8.1 WRITE timing

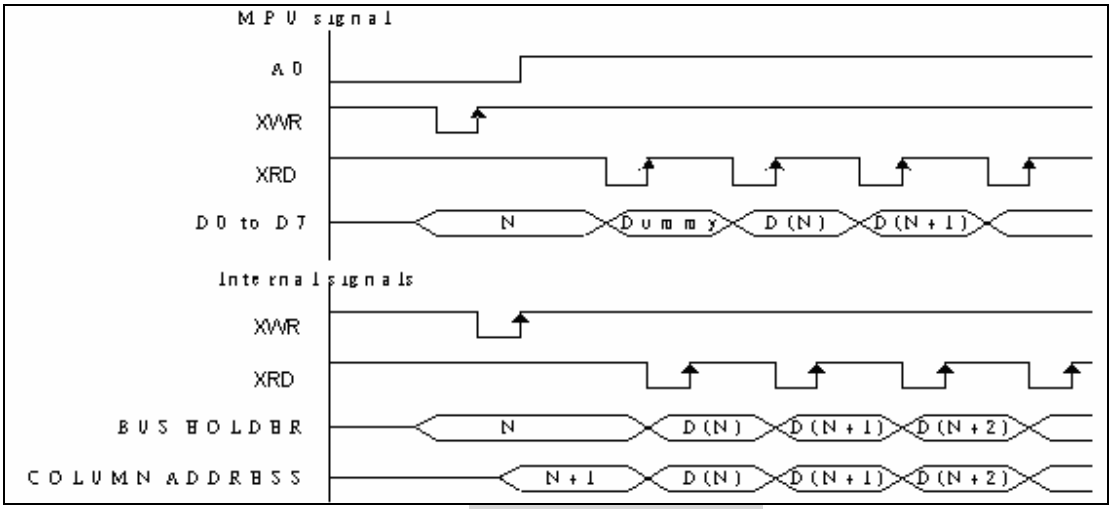


Figure 8.2 READ timing

◆ Display Data RAM

The display data RAM stores the dot data for the LCD. It has a 97 (12 page x 8 bit +1) x 192 bit structure.
As is shown in Figure 9, the D7 to D0 display data from the MPU corresponds to the LCD display common direction; there are few constraints at the time of display data transfer when multiple RW1092 are used, thus and display structures can be created easily and with a high degree of Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

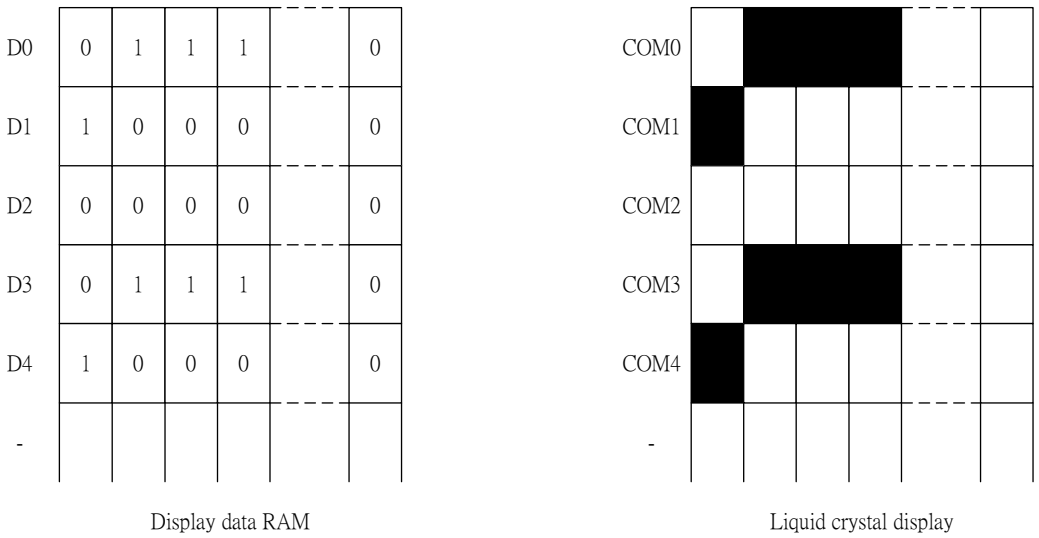


Figure 9

◆ The Page Address Circuit

Page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address 8(D3, D2, D1, D0 = 1, 0, 0, 0) is a special RAM for icons for S1065/S1575 Mode (SEL3,SEL2,SEL1=1, 0, X),and page address 15(D3, D2, D1, D0= 1, 1, 1, 1) is the icon RAM for all the other modes except S1065 and S1075, and only display data D0 is used for icon RAM.
(see Figure 10)

◆ The Column Address

The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementing of column addresses stops with 83H(S1065),A7H(S1575), or BFH(all the other mode except S1065 and S1575). Because the column address is independent of the page address, when moving, for example, from page 0 column 83H(S1065) to page 1 column 00H, it is necessary to respective both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized. As is shown in Figure 4.

Table 4

Mode Selection	Duty	SEG Output ADC	SEG0		SEG N
1, 1, 1	1/97	(D0) "0"	0 (H)	→ Column Address →	BF (H)
		(D0) "1"	BF (H)	← Column Address ←	0 (H)
1, 1, 0	1/65	(D0) "0"	0 (H)	→ Column Address →	BF (H)
		(D0) "1"	BF (H)	← Column Address ←	0 (H)
1, 0, 1**(S1575)**	1/65	(D0) "0"	0 (H)	→ Column Address→	A7 (H)
		(D0) "1"	A7 (H)	←Column Address←	0 (H)
1, 0, 0**(S1065)**	1/65	(D0) "0"	0 (H)	→ Column Address →	83 (H)
		(D0) "1"	83 (H)	← Column Address←	0 (H)
0, 1, 1	1/33	(D0) "0"	0 (H)	→Column Address→	BF (H)
		(D0) "1"	BF (H)	←Column Address←	0 (H)
0, 1, 0	1/17	(D0) "0"	0 (H)	→ Column Address →	BF (H)
		(D0) "1"	BF (H)	← Column Address ←	0 (H)
0, 0, 1	1/9	(D0) "0"	0 (H)	→ Column Address →	BF (H)
		(D0) "1"	BF (H)	← Column Address ←	0 (H)
0, 0, 0	1/5	(D0) "0"	0 (H)	→ Column Address →	BF (H)
		(D0) "1"	BF (H)	← Column Address ←	0 (H)
0, 0, 0	static	(D0) "0"	0 (H)	→ Column Address →	BF (H)
		(D0) "1"	BF (H)	← Column Address ←	0 (H)

◆ The Line Address Circuit

The line address circuit, as shown in Figure 10.1~10.3, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COMN (N is depend on duty selection) output for RW1092 , the detail is shown page 51 . The display area is a 97 line area for the RW1092(65 lines for S1065 and S1075).
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

Page Address				Data	Line Address	COM Output
D3	D2	D1	D0			
0	0	0	0	D0	00H	COM0
				D1	01H	COM1
				D2	02H	COM2
				D3	03H	COM3
				D4	04H	COM4
				D5	05H	COM5
				D6	06H	COM6
				D7	07H	COM7
0	0	0	1	D0	08H	COM8
				D1	09H	COM9
				D2	0AH	COM10
				D3	0BH	COM11
				D4	0CH	COM12
				D5	0DH	COM13
				D6	0EH	COM14
				D7	0FH	COM15
0	0	1	0	D0	10H	COM16
				D1	11H	COM17
				D2	12H	COM18
				D3	13H	COM19
				D4	14H	COM20
				D5	15H	COM21
				D6	16H	COM22
				D7	17H	COM23
0	0	1	1	D0	18H	COM24
				D1	19H	COM25
				D2	1AH	COM26
				D3	1BH	COM27
				D4	1CH	COM28
				D5	1DH	COM29
				D6	1EH	COM30
				D7	1FH	COM31
0	1	0	0	D0	20H	COM32
				D1	21H	COM33
				D2	22H	COM34
				D3	23H	COM35
				D4	24H	COM36
				D5	25H	COM37
				D6	26H	COM38
				D7	27H	COM39
0	1	0	1	D0	28H	COM40
				D1	29H	COM41
				D2	2AH	COM42
				D3	2BH	COM43
				D4	2CH	COM44
				D5	2DH	COM45
				D6	2EH	COM46
				D7	2FH	COM47
0	1	1	0	D0	30H	COM48
				D1	31H	COM49
				D2	32H	COM50
				D3	33H	COM51
				D4	34H	COM52
				D5	35H	COM53
				D6	36H	COM54
				D7	37H	COM55
0	1	1	1	D0	38H	COM56
				D1	39H	COM57
				D2	3AH	COM58
				D3	3BH	COM59
				D4	3CH	COM60
				D5	3DH	COM61
				D6	3EH	COM62
				D7	3FH	COM63
1	0	0	0	D0		COMS

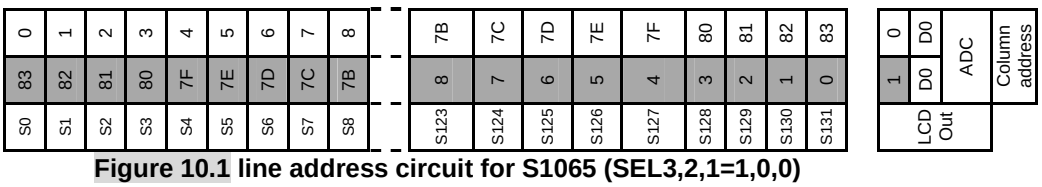


Figure 10.1 line address circuit for S1065 (SEL3,2,1=1,0,0)

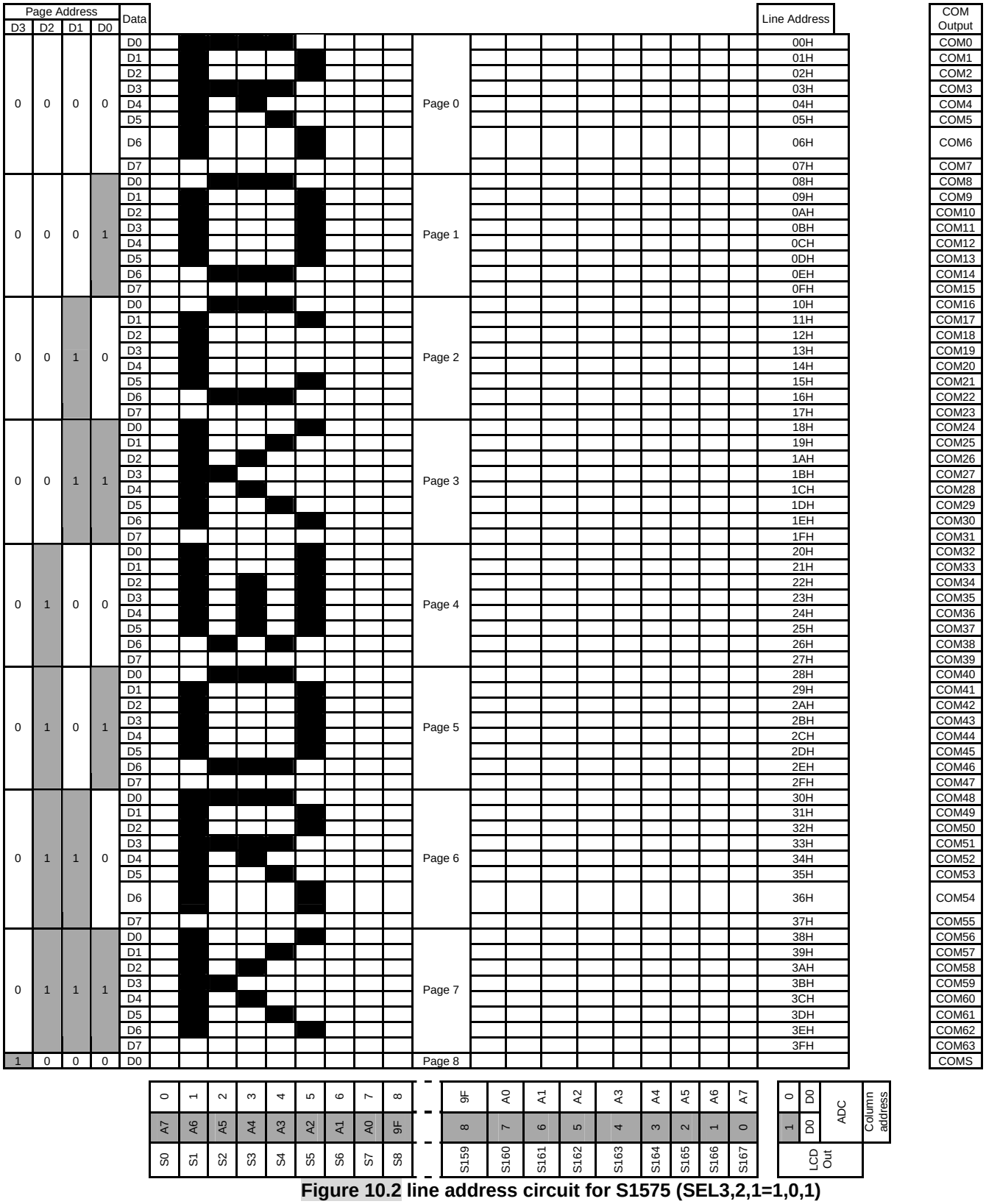


Figure 10.2 line address circuit for S1575 (SEL3,2,1=1,0,1)

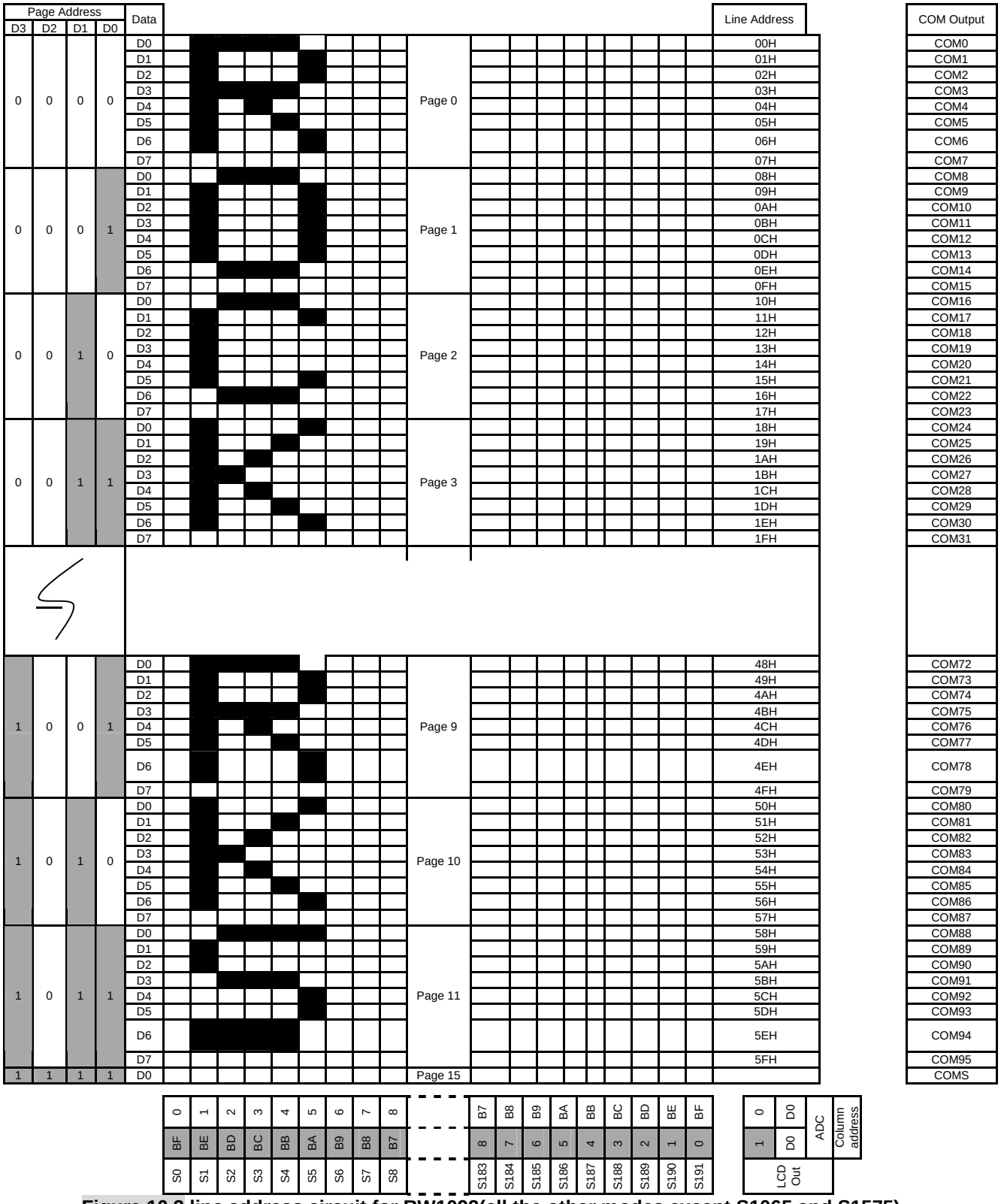


Figure 10.3 line address circuit for RW1092(all the other modes except S1065 and S1575)

◆ The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

◆ The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when CLS = “H”.
When CLS = “L” the oscillation stops, and the external clock is input through the STACOM terminal.

◆ Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 11, for the liquid crystal drive circuit.

➢ Two- frame alternating current drive waveform

N=98 for duty 1/97 (Dummy COM, COM0~COM95,COMS)
N=66 for duty 1/65 (Dummy COM, COM0~COM63,COMS)
N=34 for duty 1/33 (Dummy COM, COM0~COM31,COMS)
N=18 for duty 1/17 (Dummy COM, COM0~COM15,COMS)
N=9* for duty 1/9 (COM0~COM7,COMS)
N=5* for duty1/5 (COM0~COM3,COMS)
* Note: Duty 1/96+1, 1/64+1, 1/32+1, 1/16+1 have dummy COM scan line as 1st COM, but Duty 1/8+1 and 1/4+1having no dummy scan line.

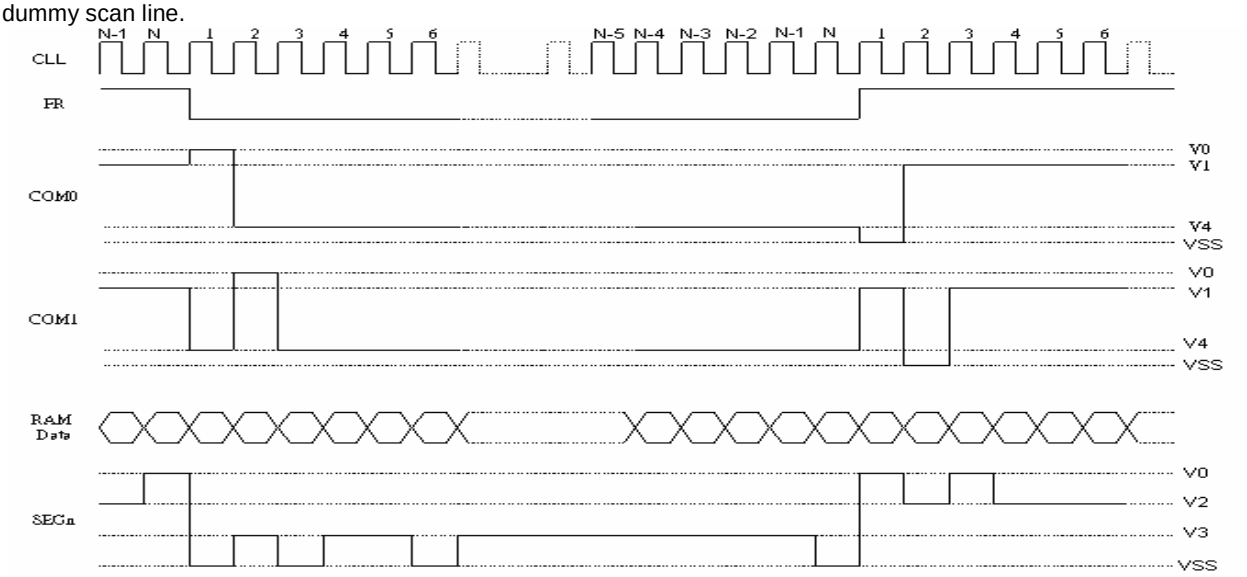


Figure 11

Table 5 Shows the status of STACOM

Table 5

Operation Mode	STACOM
CLS= "H"	Output
CLS= "L"	Input

■ The Common Output Status Select Circuit

In the RW1092 chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction					
Mode Select	**SEL3,2,1=1,1,1**	**SEL3,2,1=1,1,0 SEL3,2,1=1,0,1 SEL3,2,1=1,0,0**	**SEL3,2,1=0,1,1**	**SEL3,2,1=0,1,0**	**SEL3,2,1=0,0,1**	**SEL3,2,1=0,0,0**
Normal Reverse	COM0 → COM95 COM95 → COM0	COM0 → COM63 COM63 → COM0	COM0 → COM31 COM31 → COM0	COM0 → COM15 COM15 → COM0	COM0→ COM7 COM7→ COM0	COM0→COM3 COM3→ COM0

***Please refer to Page 3 ~ Page38 for the details**

■ The LCD Driver Circuit

These are a 257-channel that generates four voltage levels for driving the LCD . The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output. Figure 12 shows examples of the SEG and COM output waveform.

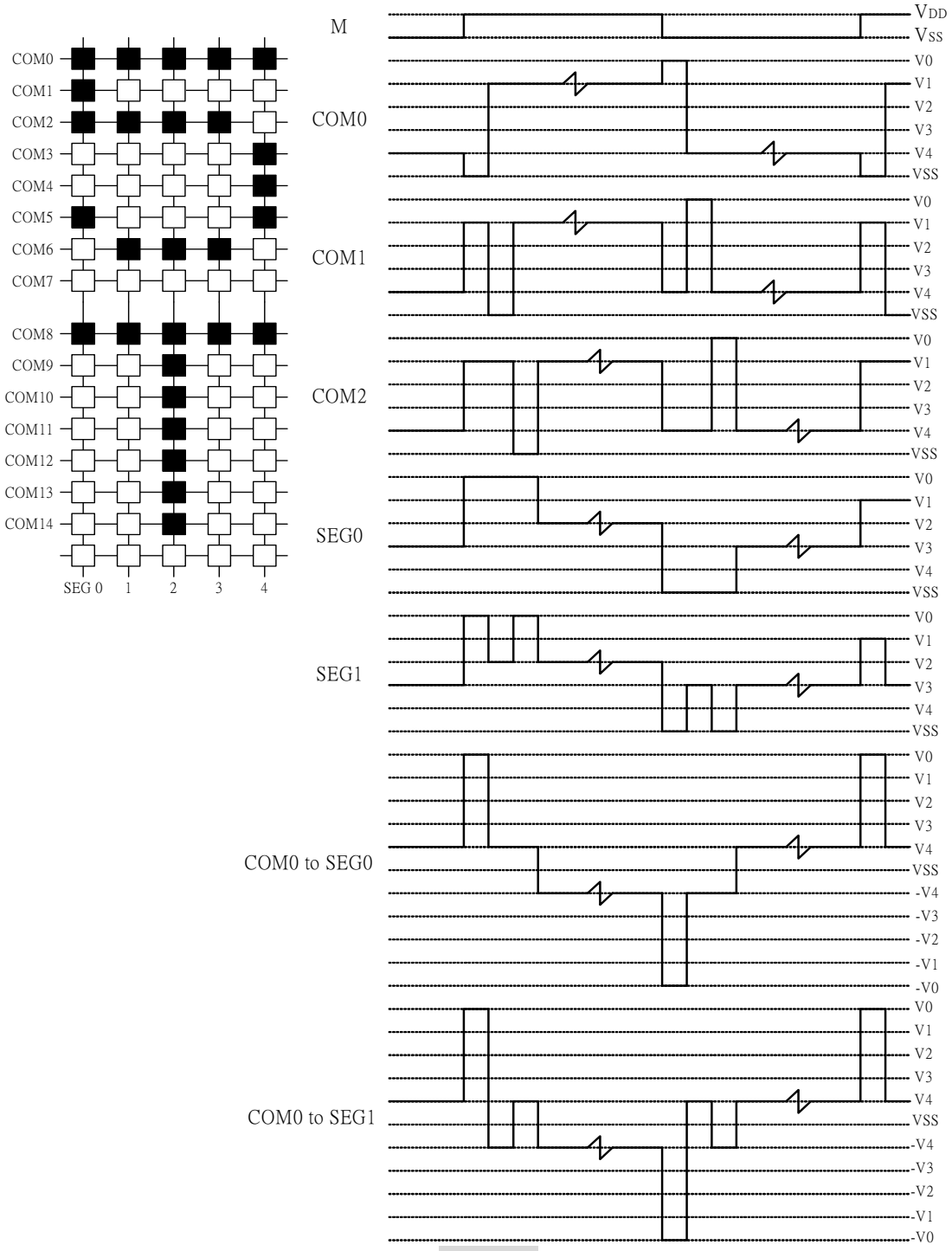


Figure 12

■ The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the LCD drivers. They are Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation. The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7

bit	function	Status "1"	Status "0"
D2	Booster circuit control bit	ON	OFF
D1	Voltage regulator circuit control bit (V/R circuit)	ON	OFF
D0	Voltage follower circuit control bit (V/F circuit)	ON	OFF

Table 8

Use Settings	D2	D1	D0	Voltage booster	Voltage regulator	Voltage follower	External voltage input	Step-up voltage
Only the internal power supply is used	1	1	1	ON	ON	ON	V_{DD2}	Used
Only the voltage regulator circuit and the voltage follower circuit are used	0	1	1	OFF	ON	ON	V_{OUT}, V_{DD2}	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V_0, V_{DD2}	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V_0 to V_4	Open

Reference Combinations

* The "step-up system terminals" refer CAP1N, CAP1P, CAP2N, CAP2P, and CAP3P,CAP4P,CAP5P,CAP6P.
* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

■ The Set-up Voltage Circuits

Using the step-up voltage circuits equipped within the RW1092 chips it is possible to product a 2X,3X,4X,5X,6X or 7X step-up of the VSS – VDD2 voltage levels.

7X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,between CAP1N and CAP5P, between CAP2N and CAP6P and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 6 times the voltage level between VSS and VDD2.

6X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,between CAP1N and CAP5P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 6 times the voltage level between VSS and VDD2.

5X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 5 times the voltage level between VSS and VDD2.

4X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, and between VDD2 and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 4 times the voltage level between VSS and VDD2.

3X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P and bet VDD2 and VOUT, and short between CAP3P VOUT to produce voltages level in the positiv at the VOUT terminal that is 3 times the voltag between VSS and VDD2.

2X step-up: Connect capacitor C1 between CAP1N and CAP1P, and between VDD2 and VOUT, leave CAP2N open, and short between CAP2P, CAP3P and VOUT to produce a voltage in the positive direction at the VOUT terminal that Is twice the voltage between VSS and VDD2.The step-up voltage relationships are shown in Figure 13.

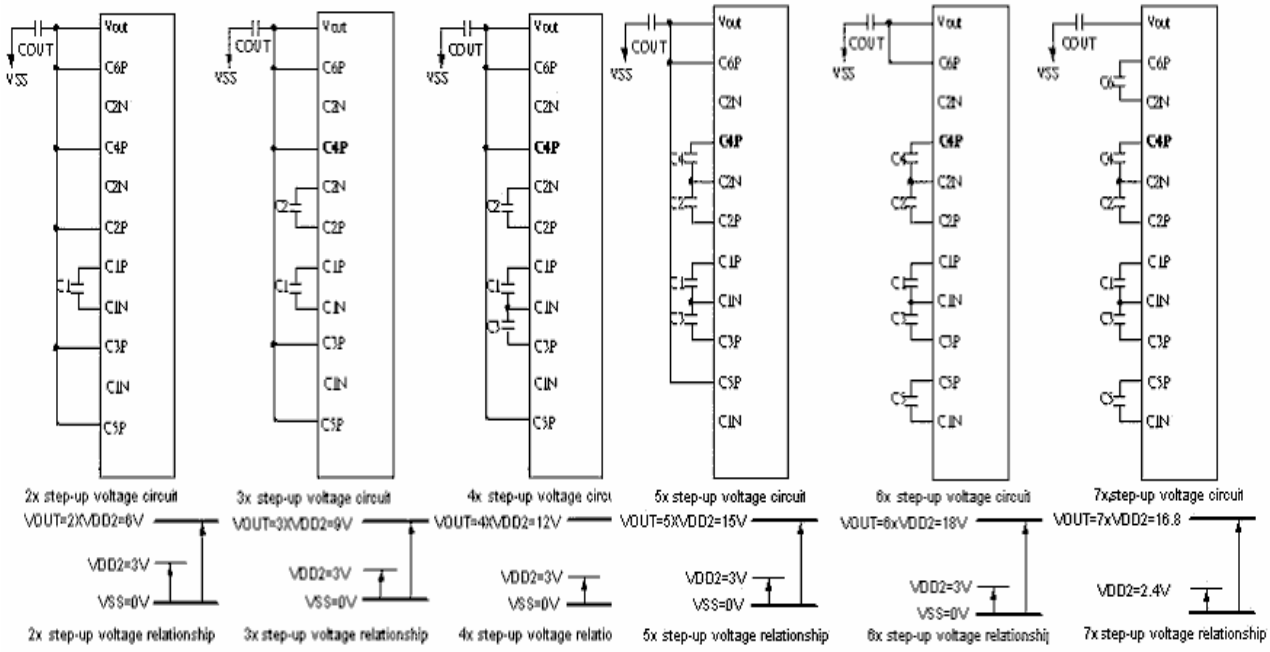


Figure 13

* The VDD_2 voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

■ The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the LCD driver voltage V0 through the voltage regulator circuit. Because the RW1092 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.
(VREG thermal gradients approximate -0.05%/℃)

➢ (A) When the V0 Voltage Regulator Internal resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where| V0 | < | VOUT |.

$$V_0 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

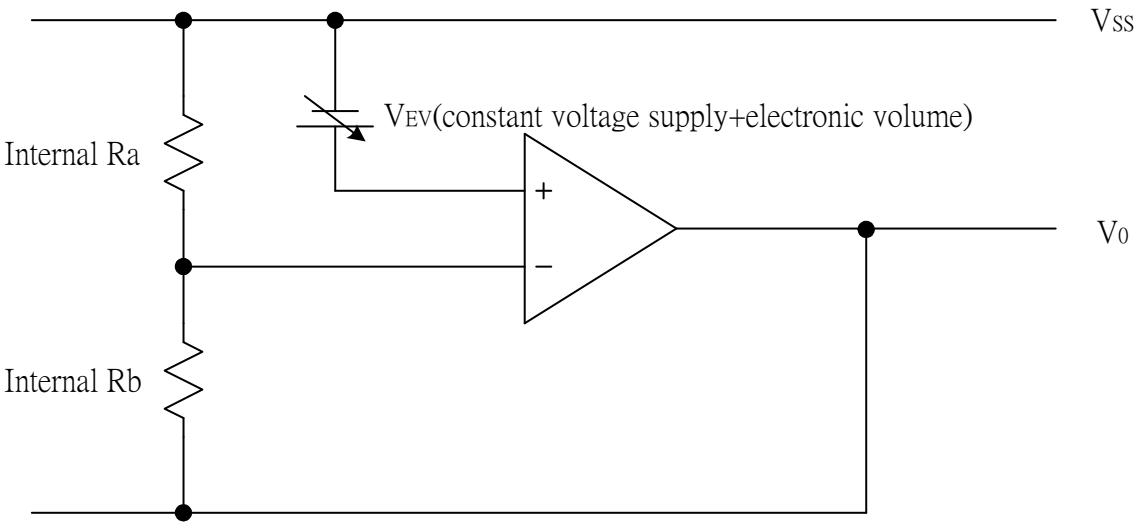


Figure 14

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25℃ is as shown in Table 9.

Table 9

Part no.	Equipment Type	Thermal Gradient	VREG
RW1092	Internal Power Supply	–0.05 %/℃	2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 10 shows the value for α depending on the electronic volume register settings. Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			RW1092
D2	D1	D0	(1) –0.05 %/℃
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Figures 15 show V0 voltage measured by values of the internal resistance ratio resistor for V0 voltage adjustment and electric volume resister for each temperature grade model.

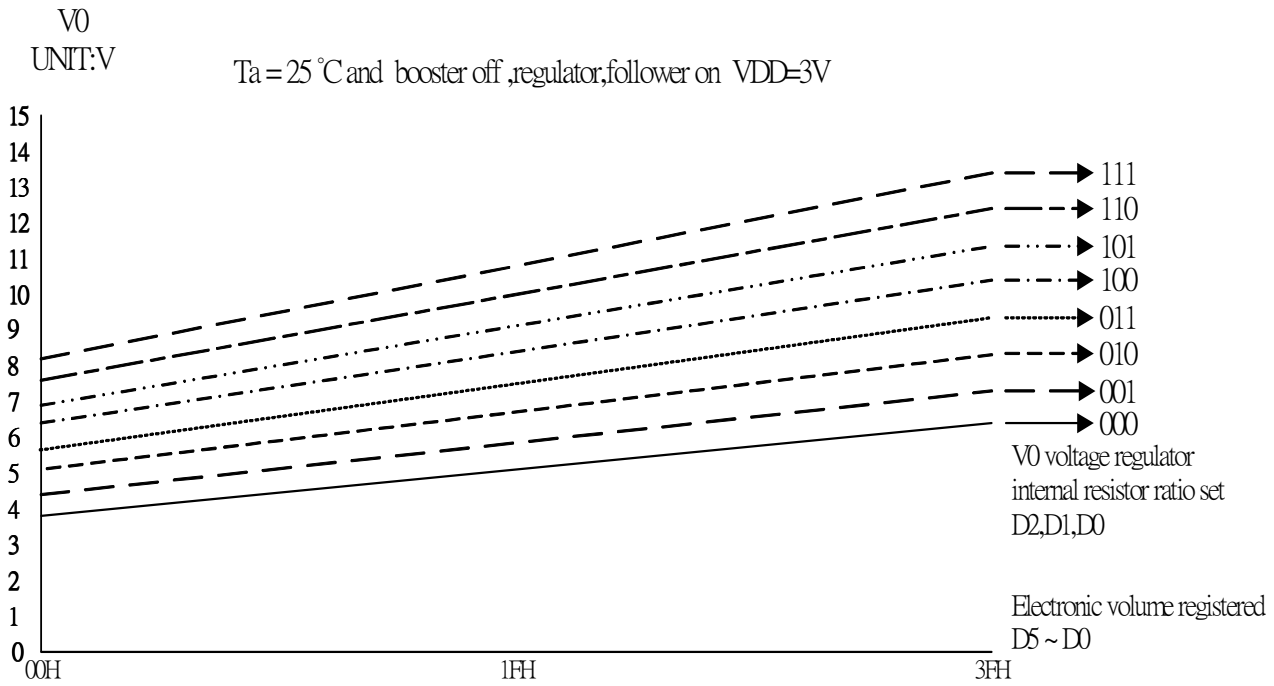


Figure 15 : (1) For RW1092 the Thermal Gradient = -0.05%/℃

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25℃ and V0 = 7V for an RW1092 on which Temperature gradient = –0.05%/℃.Using Figure 15 and the equation A-1, t he following setup is enabled.
At this time, the variable range and the notch width of the V0 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

Table 13

V_0	Min	Typ	Max	Units
Variable Range	5.1 (63 levels)	7.0 (central value)	8.4 (0 level)	[V]
Notch width		51		[mV]

➢ (B) When an External Resistance is Used (The V0 Voltage Regulator Internal Resistors Are Not Used(1)

The liquid crystal power supply voltage V0 can also be set without using the V0 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V0, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V0 through commands.

In the range where | V0 | < | VOUT |, the V0 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$

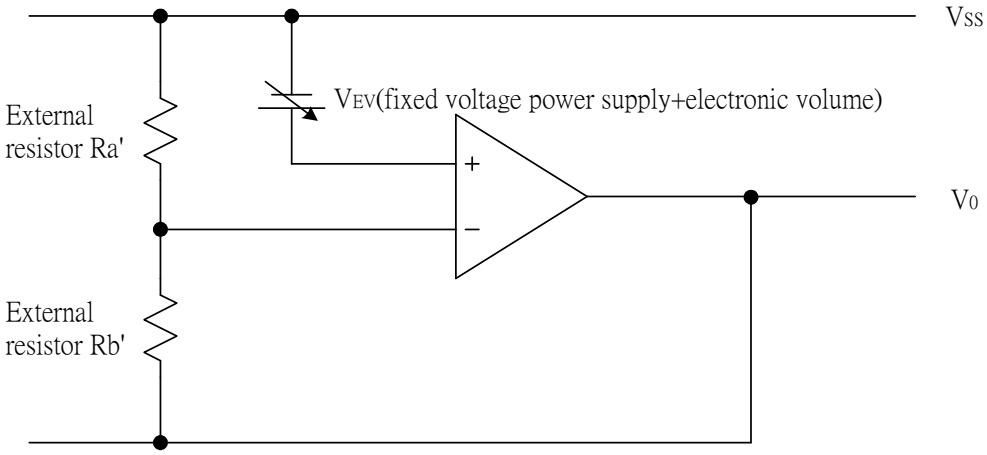


Figure 16

Setup example: When selecting Ta = 25℃ and V0 = 7 V for RW1092 the temperature gradient = –0.05%/℃. When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = 2.1V so, according to equation B-1,

$$V_0 = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$7V = \left(1 + \frac{Rb'}{Ra'}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet (2.1)$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 uA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

.

Consequently, by equations B-2 and B-3

$$\frac{Rb'}{Ra'} = 3.12$$

$$Ra' = 340k\Omega$$

$$Rb' = 1060k\Omega$$

At this time, the V0 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

➢ When External Resistors are Used (The V0 Voltage Regulator Internal Resistor Are Not Used) (2)

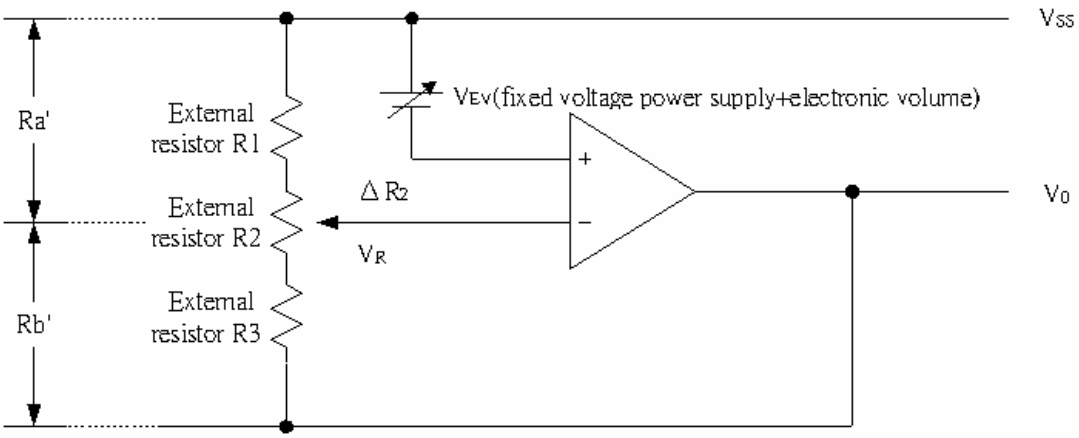
When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V0. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V0 by commands to adjust the liquid crystal display brightness.

In the range where | V0 | < | VOUT | the V0 voltage can be calculated by equation C-1 below based on the R1 and R2 (variable resistor) and R3 settings, where R2 can be subjected to fine adjustments (△ R2).

$$V_0 = \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet V_{EV}$$

$$= \left(1 + \frac{R3+R2-\Delta R2}{R1+\Delta R2}\right) \bullet \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \frac{\alpha}{162}\right) \bullet V_{REG}\right]$$



Setup example: When selecting Ta = 25℃ and V0= 5 to 9 V (using R2) for an RW1092 the temperature gradient = –0.05%/℃.

When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = 2.1 V so, according to equation C-1, when △R2 = 0 Ω, in order to make V0 = 9 V,

$$9V = \left(1 + \frac{R3+R2}{R1}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet \quad (2.1)$$

When △R2 = R2, in order to make V = –5 V,

$$5V = \left(1 + \frac{R3}{R1+R2}\right) \bullet \left(1 - \frac{31}{162}\right) \bullet \quad (2.1)$$

When the current flowing VDD and V0 is set to 5uA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R1 = 264k\Omega$$

$$R2 = 211k\Omega$$

$$R3 = 925k\Omega$$

The V0 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V0	Min	Typ	Max	Units
Variable Range	5.3 (63 levels)	7.0 (central value)	8.7 (0 level)	[V]
Notch width		53		[mV]

* When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
* The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L").
  When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the VR terminal is left open.
* Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

◆ The LCD Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3 and V4 to the liquid crystal drive circuit.

◆ The Internal Power Supply Shutdown Sequence

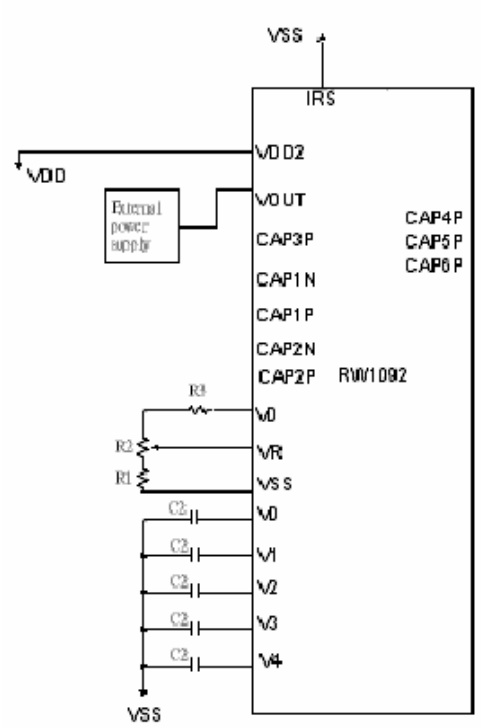
The sequence shown in Figure 18 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details(Command, status)	Command address								
		D7	D6	D5	D4	D3	D2	D1	D0	
Step 1	Display OFF	1	0	1	0	1	1	1	0	Power Saver commands (compound)
Step 2	Display all Point ON	1	0	1	0	0	1	0	1	
End	Internal Power Supply OFF									

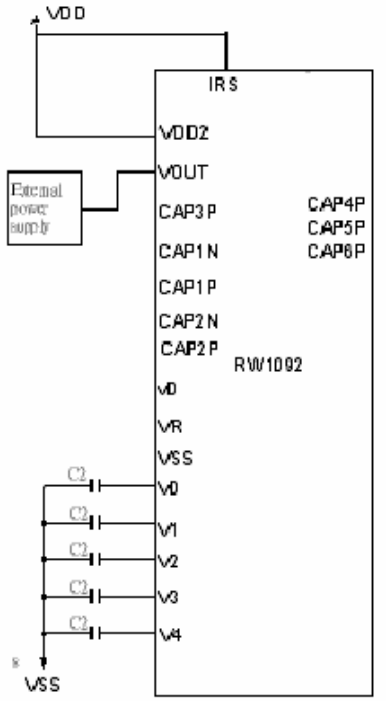
Figure 18

■ Reference Circuit Examples

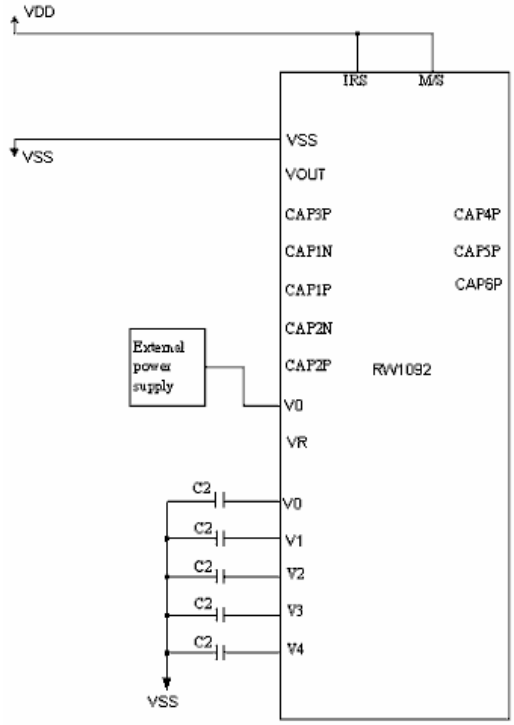
(1) When the V0 voltage regulator internal resistor is not used.



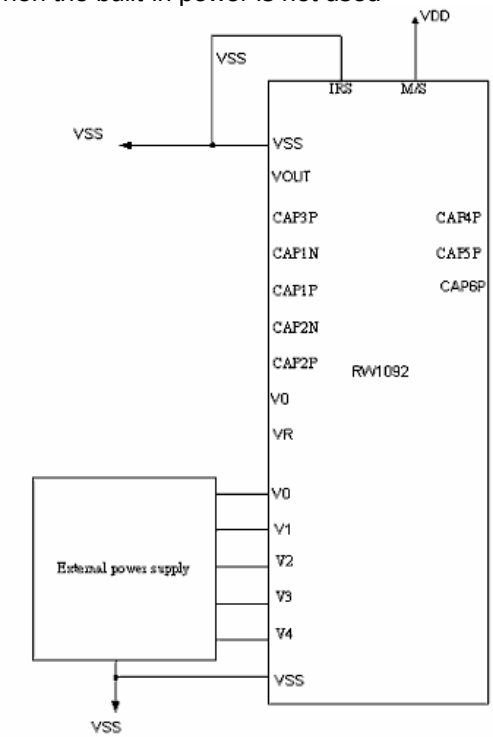
(2) When the V0 voltage regulator internal resistor is used.



(3) When the V/F circuit alone is used



(4) When the built-in power is not used



Item	Set value	units
C1	2.2 to 4.7	uF
C2	2.2 to 4.7	uF

C1 and C2 are determined by the size of the LCD being driven

* 1. Because the VR terminal input impedance is high, use short leads and shielded lines.
* 2. C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to VOUT from the outside.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V0 to V4). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

■ The Reset Circuit

When the RSTP input comes to the “L” level, these LSIs return to the default state. Their default states are as follows:

1. Display OFF.
2. Normal display.
3. ADC select: Normal (ADC command D0 = “L”)
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear.
6. LCD power supply bias rate:
   1/97 DUTY = 1/10 bias
   1/65 DUTY = 1/9 bias
   1/33 DUTY = 1/6 bias
   1/17,1/9 DUTY = 1/5 bias
   1/5 DUTY = 1/3 bias
7. All-indicator lamps-on OFF (All-indicator lamps ON/OFF. command D0 = “L”)
8. Power saving clear.
9. V0 voltage regulator internal resistors Ra and Rb separation.
10. Output conditions of SEG and COM terminals
    SEG=VSS , COM=VSS
11. Read modify write OFF.
12. Static indicator OFF Static indicator register : STA =0.
13. Display start line set to first line.
14. Column address set to Address 0.
15. Page address set to Page 0.
16. Common output status normal.
17. V0 voltage regulator internal resistor ratio set mode clear.
18. Electronic volume register set mode clear
    Electronic volume register :
    (D5, D4, D3, D2, D1, D0) = (1, 0. 0, 0, 0,0)
19. Test mode clear.
20. BE=0
21. Internal resistor used ExtR=1
22. DFR3~DFR0=0000

On the other hand, when the reset command is used, the above default settings from 11 to 22 are only executed.

When the power is turned on, the IC internal state becomes unstable, and it is necessary to initialize it using the RSTP terminal. After the initialization, each input terminal should be controlled normally.

Moreover, when the control signal from the MPU is in the high impedance, an over current may flow to the IC. After applying a current, it is necessary to take proper measures to prevent the input terminal from getting into the high impedance state.

If the internal liquid crystal power supply circuit is not used on RW1092,it is necessary that RSTP is “H” when the external liquid crystal power supply is turned on.

This IC has the function to discharge V0 when RSTP is “L,” and the external power supply short-circuits to VSS when RSTP is “L.”

While RSTP is “L,” the oscillator and the display timing generator stop, and the CL, FR terminals are fixed to “H.” The terminals D0 to D7 are not affected. The VSS level is output from the SEG and COM output terminals. This means that an internal resistor is connected between VSS and V0.

When the internal liquid crystal power supply circuit is not used on other models of RW1092 series, it is necessary that RSTP is “L” when the external liquid crystal power supply is turned on.

While RSTP is “L,” the oscillator works but the display timing generator stops, and the STACOM terminals is fixed to “H.” The terminals D0 to D7 are not affected

■ COMMANDS

The RW1092 identify the data bus signals by a combination of A0, XRD (E), XWR(R/W) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the RD terminal for reading, and inputting a low pulse to the XWR terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/W terminal and placed in a write mode when a "L" signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read XRD (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the serial interface is selected, the data is input in sequence starting with D7.<Explanation of Commands>

➢ Display ON/OFF

This command turns the display ON and OFF.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1 0	Display ON Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

➢ Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 10. For further details see the explanation of this function in "The Line Address Circuit".

(a) Start line set command for **S1065** and **S1575 (single byte command)**

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0 0 0 ↓ 1 1	0 0 0 ↓ 1 1	0 0 0 ↓ 1 1	0 0 0 ↓ 1 1	0 0 1 ↓ 1 1	0 1 0 ↓ 0 1	0 1 2 ↓ 62 63

(b) Start line set command for all the other modes except S1065 and S1575 **(double byte command)**

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1 **S6**	0 **S5**	0 **S4**	0 **S3**	0 **S2**	0 **S1**	0 **S0**	0 1 2 ↓ 94 95

➢ Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 10). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Page address For S1065 S1575	Page address For Other modes
0	1	0	1	0	1	1	0	0	0	0		0
							0	0	0	1	0	1
							0	0	1	0	1	2
							↓				2	↓
							0	1	1	1	↓	10
							1	0	0	0	7	11
							↓				8	↓
							1	1	1	1		15

➢ Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read /write to the display data. The column address increment is topped at 83H(S1065), A7H(S1575) and BFH(all the other modes except S1065 and S1575). This does not change the page address continuously. See the function explanation in “The Column Address Circuit,” for details.

	A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →				0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
	0	1	0									1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131(S1065)
																↓				↓
												1	0	1	0	0	1	1	0	166
												1	0	1	0	0	1	1	1	167(S1575)
																↓				↓
												1	0	1	1	1	1	1	0	190
												1	0	1	1	1	1	1	1	191(other modes)

➢ Status Read

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	**BUSY=1**:it indicates that either processing is occurring internally or a reset condition is in process **BUSY=0**:A new command can be accepted. If the cycle time can be satisfied , there us no need to check for BUSY condition.
ADC	This shows the relationship between the column address and the segment driver . **0:Normal** (column address n ↔ SEG n) **1:Reverse** (column address 131-n ↔ SEG n) (The ADC command switches the polarity)
ON/OFF	ON/OFF: indicates the display ON/OFF state. **0:Display ON** **1:Display OFF** (This display ON/OFF command switches the polarity)
RESET	This indicates that the chip is in the process of initialization either because of a RSTP signal or because of a reset command. **0:Operating state** **1:Reset in progress**

➢ Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by “1” after the write, the MPU can write the display data.

A0	E XRD	R/W XWR	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

➢ Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by “1” after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in “Display Data RAM” for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E XRD	R/W XWR	D7 D6 D5 D4 D3 D2 D1 D0
1	0	1	Read data

➢ ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0 1	Normal Reverse

➢ Display Normal / Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0 1	RAM Data "H" LCD ON voltage (normal) RAM Data "L" LCD ON voltage (reverse)

➢ Display All Point ON / OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0 1	Normal display mode Display all points ON

➢ LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status(BE=0)					
											1/97duty	1/65duty	1/33duty	1/17, 1/9duty	1/5duty	static
0	1	0	1	0	1	0	0	0	1	0	1/10 bias	1/9 bias	1/6 bias	1/5 bias	1/3 bias	-
										1	1/8 bias	1/7 bias	1/4 bias	1/4 bias	1/2 bias	1/2 bias

Furthermore,RW1092 provides more flexible LCD bias ratio by BE register which is set by a double byte command.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status(BE=1)				
											1/97duty	1/65duty	1/33duty	1/17, 1/9duty	1/5duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/5 bias	1/3 bias	-
										1	1/7 bias	1/6 bias	1/3 bias	1/2 bias	-

BE register set (double byte command)

	A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
1st Byte →	0	1	0	1	1	1	1	0	0	1	1
2nd Byte →	0	1	0	1	0	ExtR		BE	DFR3	~	DFR0

➢ Read/ Modify/Write

This command is used paired with the “END” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

	E	R/W							
A0	XRD	XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.

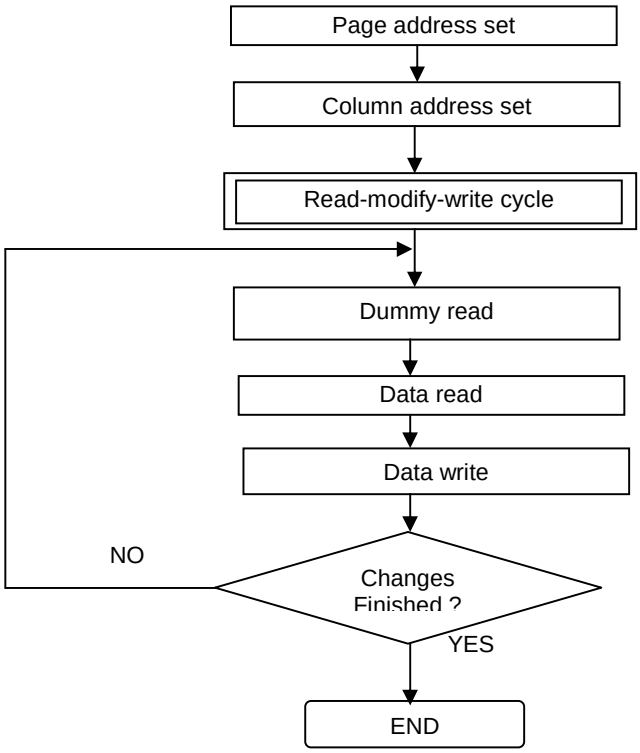


Figure 19 Command Sequence For read modify write

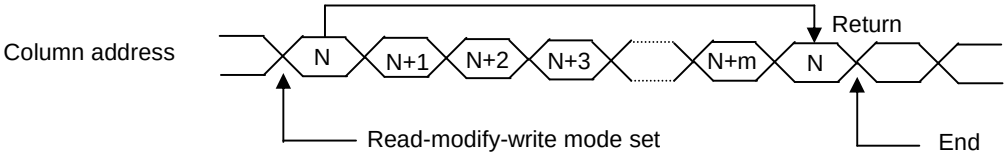


Figure 20

➢ End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

➢ Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V0 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in “Reset” for details.
The reset operation is performed after the reset command is entered.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

➢ Common Output Mode Select(SHL)

This command can select the scan direction of the COM output terminal. For details, see the function explanation in “Common Output Mode Select Circuit.”

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	1	1	0	0	0 1	*	*	*	Normal Reverse

* Disabled bit

Status	COM Scan Direction					
Mode Select	**SEL3,2,1=1,1,1**	**SEL3,2,1=1,1,0 SEL3,2,1=1,0,1 SEL3,2,1=1,0,0**	**SEL3,2,1=0,1,1**	**SEL3,2,1=0,1,0**	**SEL3,2,1=0,0,1**	**SEL3,2,1=0,0,0**
Normal Reverse	COM0 → COM95 COM95 → COM0	COM0 → COM63 COM63 → COM0	COM0 → COM31 COM31 → COM0	COM0 → COM15 COM15 → COM0	COM0→ COM7 COM7→ COM0	COM0→COM3 COM3→ COM0

***Please refer to Page 3 ~ Page38 for the details**

➢ Power Controller Set

This command sets the power supply circuit functions. See the function explanation in “The Power Supply Circuit,” for details

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

➢ V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see the function explanation is “The Voltage Regulator circuit " and table 11 .

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	1	
								1	1	1	Large

➢ The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

➢ The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

➢ Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V0 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E (XRD)	R/W (XWR)	(First Byte) D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	0	0	0	1	
A0	**E (XRD)**	**R/W (XWR)**	**(Second Byte) D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**| Vo |**
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set “0”)
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

The Electronic Volume Register Set Sequence

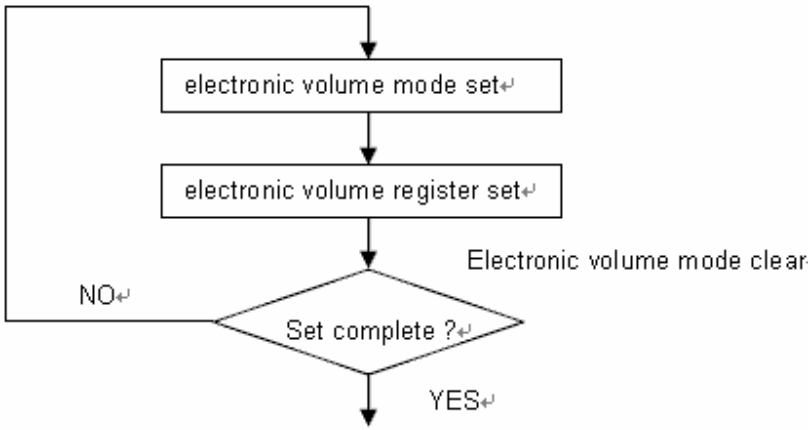


Figure 21

➢ Static Indicator ON/OFF

When the power saver mode indicator ON command is entered, the power saver indicator register set command is enabled. Once the power saver indicator ON command has been entered, no other command aside from the power saver indicator register set command can be used. This mode is cleared when data is set in the register by the power saver indicator register set command.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

➢ Static Indicator register set

This command sets one bit of data into the static indicator register, and is used to set static display enable.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Static Display
0	1	0	*	*	*	*	*	*	*	0	disable
										1	enable

* Disabled bit (set “0”)

➢ Power Save(valid for all modes except S1575,Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 23 for power save off sequence.

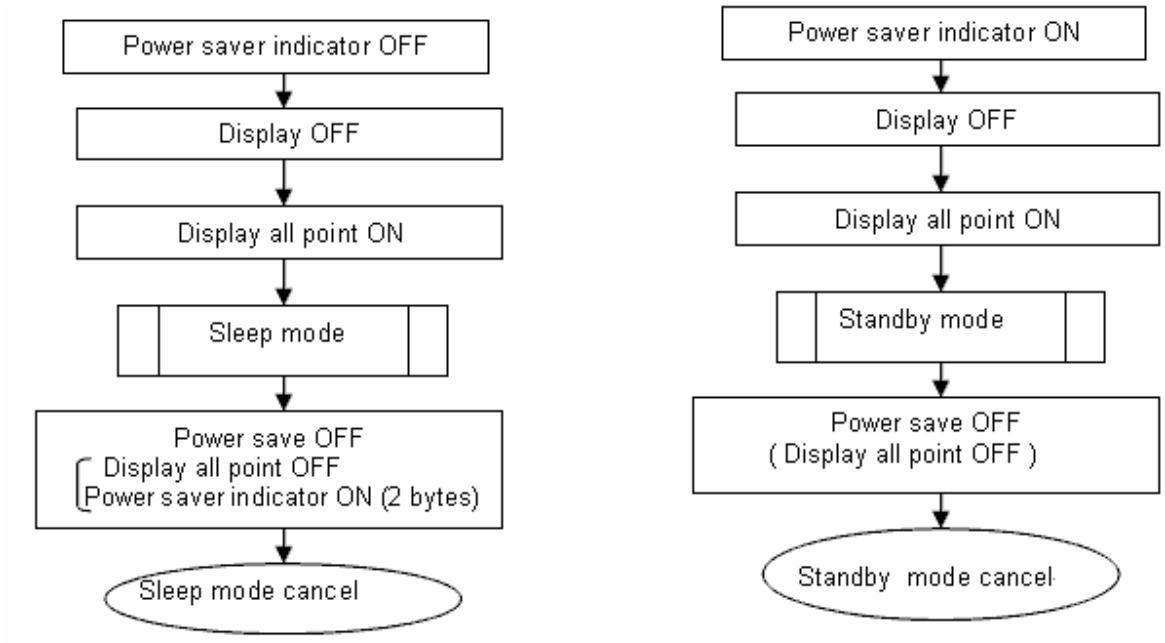


Figure 23

Power Save for S1575 (SEL3,2,1=1,0,1) used only

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	0	0	0 1	Stand-by state Sleep state

Power Save Reset for S1575(SEL3,2,1=1,0,1) used only

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	1

➢ Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption.
current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VSS level.

➢ Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a VSS level.
The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect.

➢ N-line Reversal Drive Register Set

This command sets the number of reversal lines of the liquid crystal drive in register. 2 to 16 lines can be set.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0	No. of reversal line
0	1	0	0	0	1	1	0	0	0	1	--
			0	0	1	1	0	0	1	0	2
			0	0	1	1	0	0	1	1	3
								↓			↓
			0	0	1	1	1	1	1	0	15
			0	0	1	1	1	1	1	1	16

➢ N-line Reversal Drive Reset

This command resets the n-line reversal alternating current drive and returns to the normal 2-frame reversal alternating current drive system. The value of the n-line reversal alternating current drive register is not changed.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

➢ Set Data Length for 3-SPI (double byte command)

In 3 lines SPI mode, set Data length command indicates the length of data which, are going to be received by RW1092. User should set data length before display data sent. Each data length instruction maximum can set 192 bytes of data. The table below shows how SPA bits set the data length

A0	E (XRD)	R/W (XWR)	(First Byte) D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	1	1	0	0	0	0	
A0	**E (XRD)**	**R/W (XWR)**	**(Second Byte) SPA7**	**SPA6**	**SPA5**	**SPA4**	**SPA3**	**SPA2**	**SPA1**	**SPA0**	**Function**
0	1	0	0	0	0	0	0	0	0	0	Followed by 1 data write
			0	0	0	0	0	0	0	1	Followed by 2 data write
							↓				↓
			1	0	1	1	1	1	1	1	Followed by 192 data write

➢ Built-in Oscillator Circuit ON(valid for S1575 only)

This command starts the operation of the built-in CR oscillator circuit. This command is valid only in S1575 mode and when CLS="H".

A0	E (XRD)	R/W (XWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	1

The built-in oscillator circuit will be turned on when the reset procedure is completed and CLS="H' for all the other modes except S1575(SEL3,2,1=1,0,1).

➢ NOP

Non-Operation Command

A0	E (XRD)	R/W (XWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

➢ External Ra,Rb used command

BE register set (double byte command)

	A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
1st Byte →	0	1	0	1	1	1	1	0	0	1	1
2nd Byte →	0	1	0	1	0	ExtR	BE	DF3	FR2	DFR1	DFR0

Initial value after reset : ExtR=1, BE=0, DFR3~DFR0=0000

ExtR=1: internal resistor Ra,Rb used, IRSP pin set to “H”
ExtR=0: external resistor Ra,Rb used, IRSP pin set to “L”

➢ Frame frequency adjustment command

BE register set (double byte command)

	A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
1st Byte →	0	1	0	1	1	1	1	0	0	1	1
2nd Byte →	0	1	0	1	0	ExtR	BE	DFR3	~	DFR0	

Initial value after reset : ExtR=1, BE=0, DFR3~DFR0=0000

DFR3 ~ DFR0 =0000 slow
0001
0010
0011
0100
0101
.
.
.
1100
1101
1110
1111 fast

➢ TEST

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a “L” signal to the RSTP input by the reset command or by using an NOP.

A0	E XRD	R/W XWR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Inactive bit

Note: The RW1092 maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the RW1092 . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16: Table of RW1092 Commands (Note) *: disabled data

Command	Command Code										Function
	A0	XRD	XWR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2-1) Display start line set (valid for S1065 and S1575 only)	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(2-2) Display start line set (valid for all the other modes except S1065 and S1575, double byte commands)	0	1	0	0 0	1 Display	0	0	0 start	0	0 address	0	
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	ADC	Sets the display RAM address SEG output correspondence ADC=0: normal, ADC=1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (RW1092)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	SHL	*	*	*	Select COM output scan direction SHL=0: normal direction SHL=1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode

Table 16 (continued) : Table of RW1092 Commands (Note) *: disabled data

Command	Command Code										Function
	A0	**XRD**	**XWR**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static display enable register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	1: stand by indicator on 0: sleep indicator on Mode=1: static display enable Mode=0: static display disable
(20)Set sleep mode(valid for all modes except S1575)												Power saver indicator set for **sleep** indicator on (2 bytes) ↓ Display off ↓ Display all point ON
(21)Set stand by mode(valid for all modes except S1575)												Power saver indicator set for **stand by** indicator on (2 bytes) ↓ Display off ↓ Display all point ON
(22) Power save(valid for S1575)	0	1	0	1	0	1	0	1	0	0	0 1	Moves to the power save state 0: stand by 1: sleep
(23)Power save reset (valid for S1575))				1	1	1	0	0	0	0	1	Resets power save
(24) N-line Reversal Drive Register Set	0	1	0	0	0	1	1	Number of Reversal lines				Sets the number of line reversal drive lines.
(25) N-line Reversal Drive reset	0	1	0	1	1	1	0	0	1	0	0	Resets the line reversal drive
(26)Set Data Length for 3SPI	0	1	0	0 Set Data Length for SPA bits	1	1	1	0	0	0	0	Set Data Length for 3-line serial interface
(27)Built in oscillator circuit on (Valid for S1575 only)	0	1	0	1	1	1	0	0	1	0	0	Start the built-in Oscillator
(28) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(29)External RA,RB used and frame frequency adjustment	0	1	0	1 1	1 0	1 ExtR	1 BE	0 DF3	0 ~	1 	1 DF0	ExtR=1:internal resistor used ExtR=0:external resistor used BE: register set DF3~DF0:frame frequency adjustment
(29) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

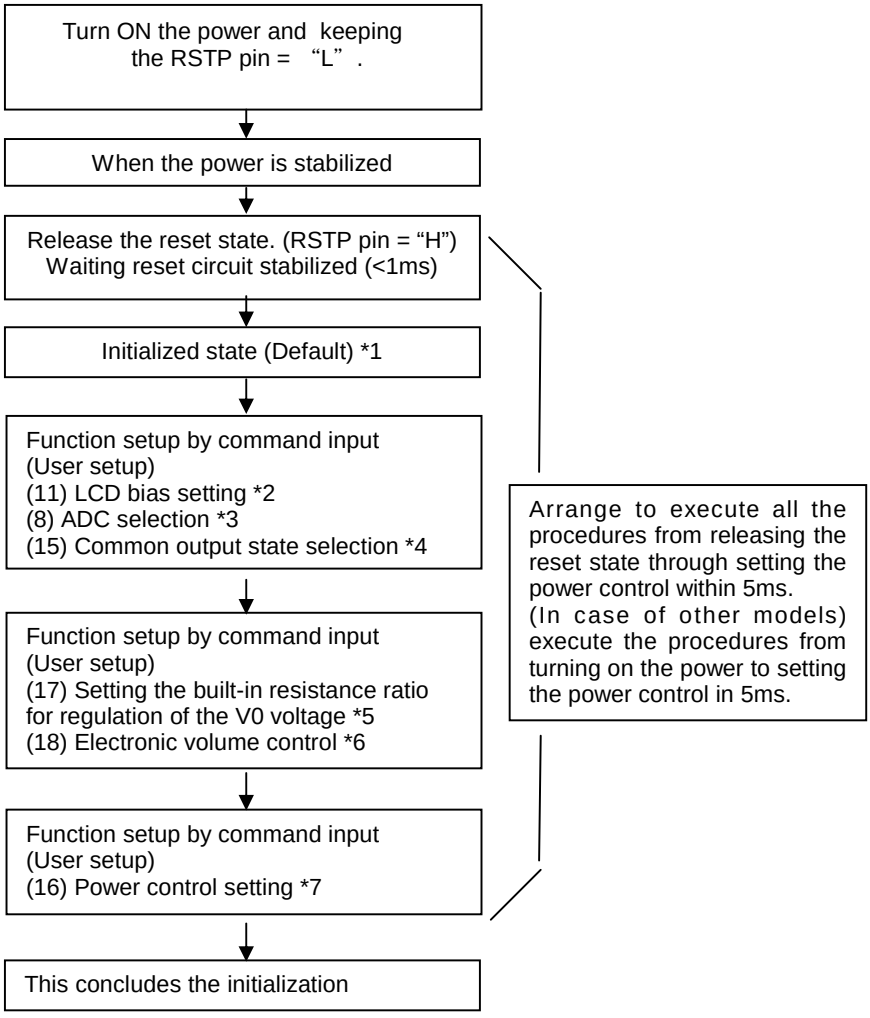
■ COMMAND DESCRIPTION

Instruction Setup : Reference

(1).Initialization:

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 ~ V4) and the VSS pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the
following flow when turning on the power.

1. When the built-in power is being used immediately after turning on the power:

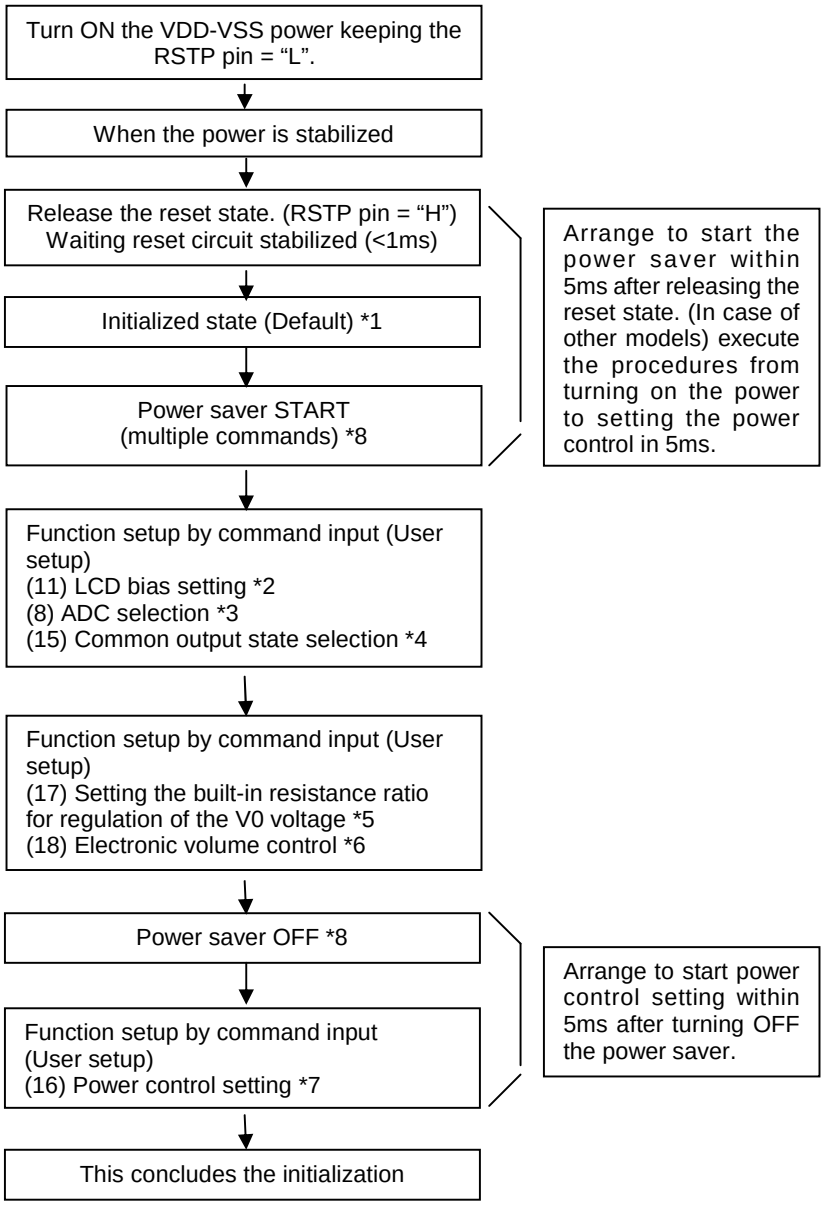


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit.
*2: Command description; LCD bias setting.
*3: Command description; ADC selection.
*4: Command description; Common output state selection.
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance ratio for regulation of the V0 voltage.
*6: Description of functions; Power circuit & Command description; Electronic volume control.
*7: Description of functions; Power circuit & Command description; Power control setting.

2. When the built-in power is not being used immediately after turning on the power:

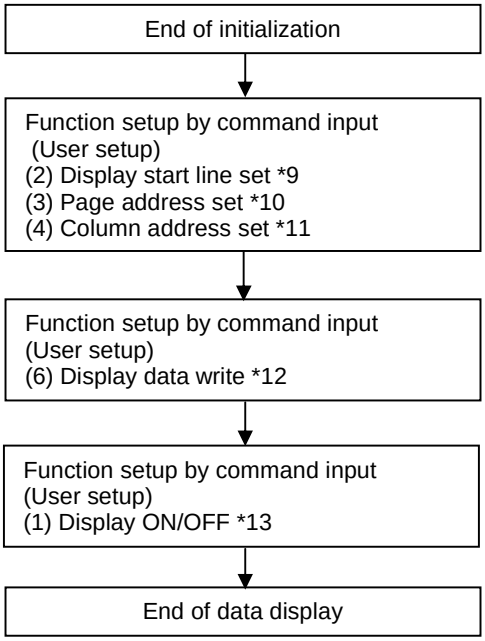


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit.
*2: Command description; LCD bias setting.
*3: Command description; ADC selection.
*4: Command description; Common output state selection.
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V0 voltage.
*6: Description of functions; Power circuit & Command description; Electronic volume control.
*7: Description of functions; Power circuit & Command description; Power control setting.
*8: The power saver ON state can either be in sleep state or stand-by state.
Command description; Power saver START. (multiple commands)

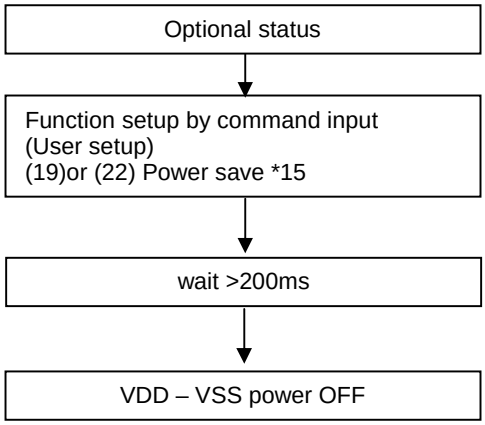
(2)Data Display



Notes: Reference items

*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF
Avoid displaying all the data at the data display start (when the display is ON) in white.

(3) Power OFF *14



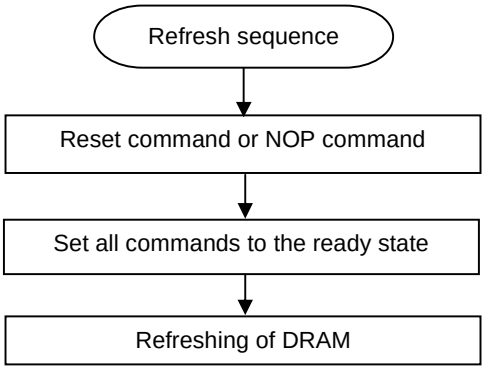
Notes: Reference items

*14: The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VSS – V0. So, if the power supply VDD - VSS is cut off when the LCD power supply VSS – V0 has still any residual voltage, the driver (COM. SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:

• After turning off the internal power supply, make sure that the potential V0 ~ V4 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS).

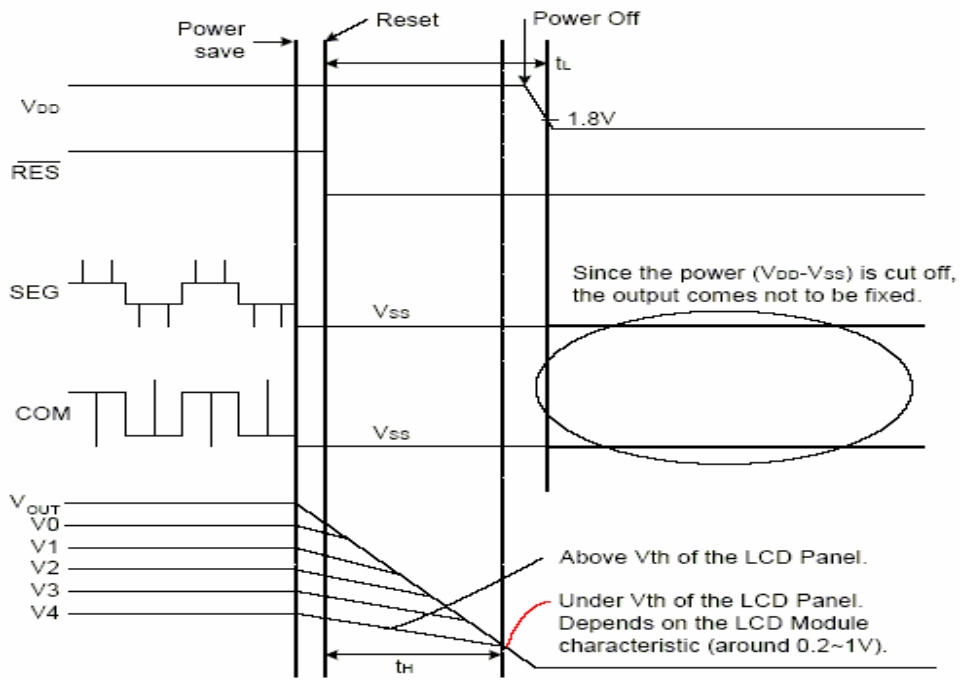
Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



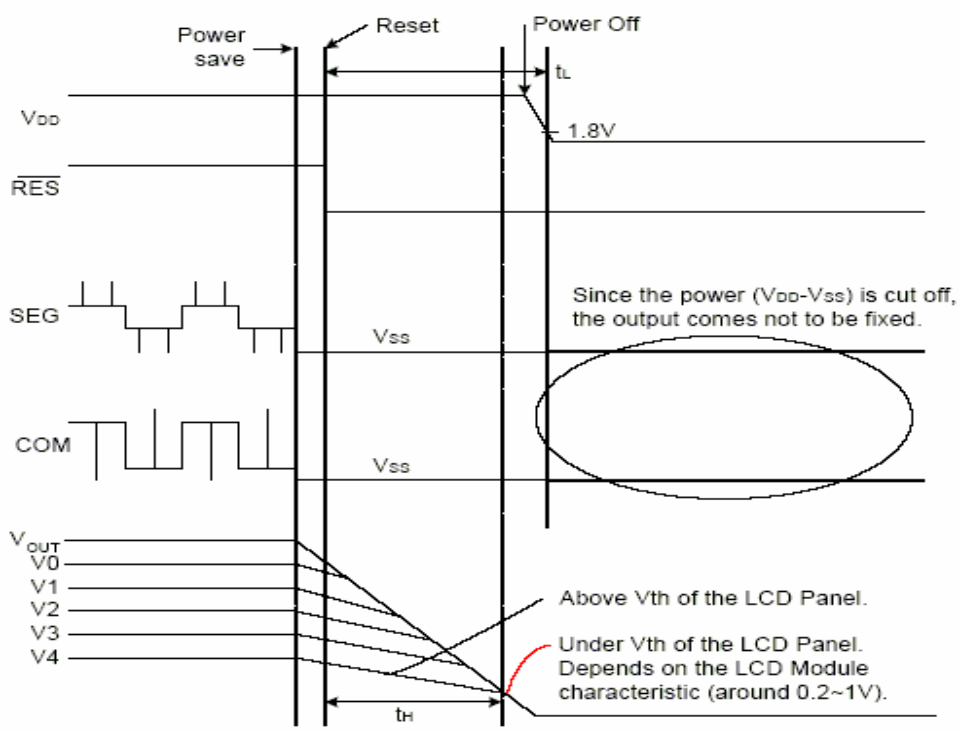
■ Precautions on Turning off the Power

<Turning the power (VDD - VSS) off>
1) Power Save (The LCD powers (V0 - VSS) are off.) → Reset input → Power (VDD - VSS) OFF
• Observe tL > tH.
• When tL < tH, an irregular display may occur.
Set tL on the MPU according to the software. tH is determined according to the external capacity C2 (smoothing capacity of V0 ~ V4) and the driver's discharging capacity.



<Turning the power (VDD - VSS) off : When command control is not possible.>

2) Reset (The LCD powers (VDD - VSS) are off.) → Power (VDD - VSS) OFF
• Observe tL > tH.
• When tL < tH, an irregular display may occur.
For tL, make the power (VDD - VSS) falling characteristics longer or consider any other method. tH is determined according to the external capacity C2 (smoothing capacity of V4 to V0) and the driver's discharging capacity.



<Reference Data>
V0 voltage falling (discharge) time (tH) after the process of operation → power save → reset.
V0 voltage falling (discharge) time (tH) after the process of operation → reset.

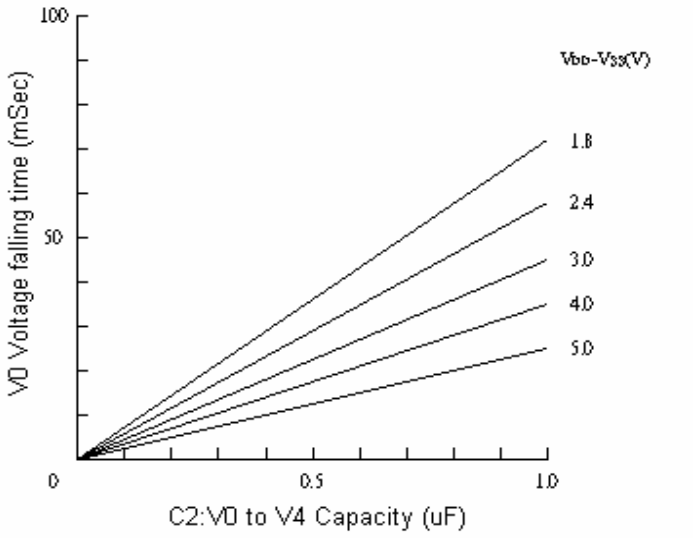


Figure 24

■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, VDD = 0V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		VDD	0.3 ~ 5.0	V
Power supply voltage (VDD standard)		VDD2	0.3 ~ 4.0	V
Power supply voltage (VDD standard)		V0, VOUT	0.3 ~ 18.0	V
Power supply voltage (VDD standard)		V1, V2, V3, V4	V0 to 0.3	V
Operating temperature		TOPR	–40 to +85	℃
Storage temperature	Bare chip	TSTR	–55 to +125	℃

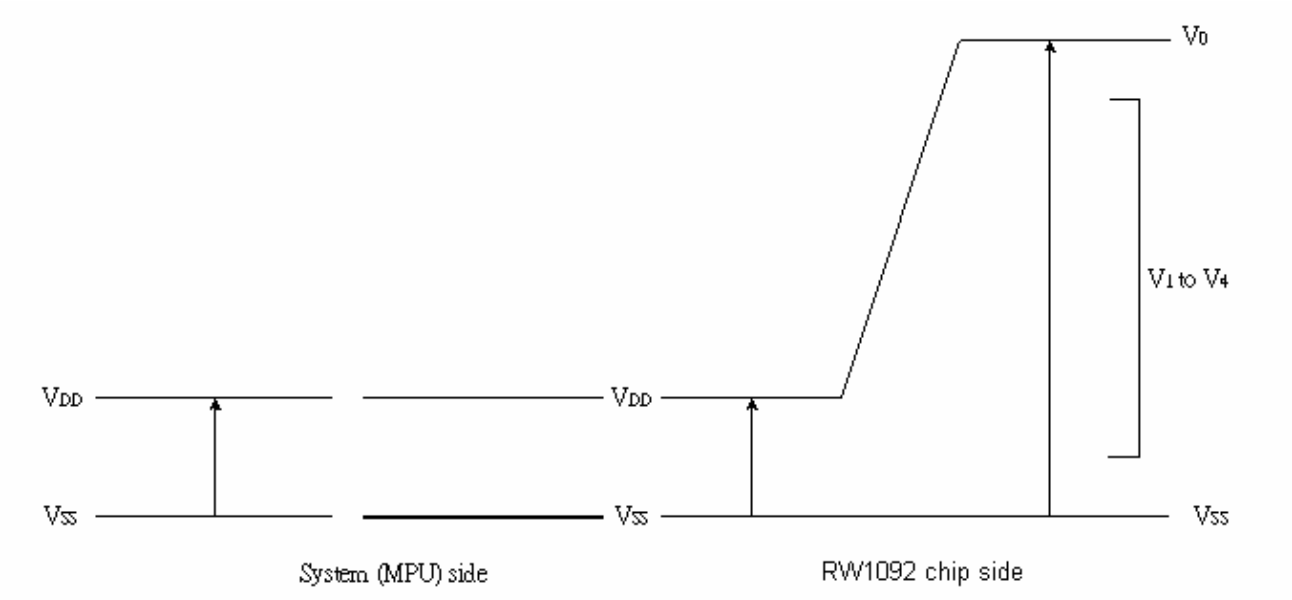


Figure 25

Notes and Cautions
1. The VDD2, V0 to V4 and VOUT are relative to the VSS = 0V reference.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that VOUT ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

■ DC CHARACTERISTICS

Unless otherwise specified, VSS = 0 V, VDD = 3.0 V ± 10%, Ta = –40 to 85℃

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD			1.8	—	3.6	V	VSS*1
Operating Voltage (2)		VDD2	(Relative to VSS)		2.4	—	3.6	V	VSS
High-level Input Voltage		VIHC			0.8 x VDD	—	VDD	V	*3
Low-level Input Voltage		VILC			VSS	—	0.2 x VDD	V	*3
High-level Output Voltage		VOHC	IOH = –0.5 mA		0.8 x VDD	—	VDD	V	*4
Low-level Output Voltage		VOLC	IOL = 0.5 mA		VSS	—	0.2 x VDD	V	*4
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*5
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*6
Liquid Crystal Driver ON Resistance		RON	Ta = 25℃ (Relative To VDD)	V0 = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *7
				V0 = 8.0 V	—	3.2	5.4		
Static Consumption Current		ISSQ	V0 = 13.0 V(Relative To VDD)		—	0.01	2	μA	VDD, VDD2
Output Leakage Current		I5Q			—	0.01	10	μA	V0
Input Terminal Capacitance		CIN	Ta = 25℃ , f = 1 MHz		—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	fOSC	1/65 duty 1/33 duty	Ta = 25℃	105.5	124.1	148.9	kHz	*8
	External Input	fCL			105.5	124.1	148.9	kHz	CL

Table 19

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD2	(Relative To VSS)	2.4	—	3.6	V	VSS
	Supply Step-up output voltage Circuit	VOUT	(Relative To VSS)	—	—	16.0	V	VOUT
	Voltage regulator Circuit Operating Voltage	VOUT	(Relative To VSS)	6.0	—	18.0	V	VOUT
	Voltage Follower Circuit Operating Voltage	V0	(Relative To VSS)	4.0	—	14.0	V	V0 * 9
	Base Voltage	VR	Ta = 25℃ , (Relative To VSS) –0.05%/℃	2.07	2.10	2.13	V	*10

- **Dynamic Consumption Current : During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .**

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	IDD	VDD = 3.0 V, V0 – VSS = 11.0 V	—	11	19	μA	*11
Display Pattern Checker	IDD	VDD = 3.0 V, V0 – VSS = 11.0 V	—	15	26	μA	*11

- **Dynamic Consumption Current : During Display, with the Internal Power Supply ON**

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern OFF	IDD	VDD = 3.0 V, Quad step-up 4x voltage. V0 – VSS = 11.0 V	—	200	260	μA	*12
Display Pattern Checker	IDD	VDD = 3.0 V, Quad step-up 4x voltage. V0 – VSS = 11.0 V	—	220	280	μA	*12

- **Consumption Current Time of Power Saver Mode : VSS= -3.0 ± 10%**

Table 22

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Sleep mode	IDD	Ta = 25℃	—	0.1	4	μA	
Standby Mode	IDD	Ta = 25℃	—	4.4	10		

■ The Relationship Between Oscillator Frequency fOSC, Display Clock Frequency fCL and the Liquid Crystal Frame Rate Frequency fFR

Table 23

Item		fCL	fFR
1/97 DUTY	Used internal oscillator circuit	fOSC / 16	fOSC / (16*98)
	Used **externa**l display clock	fOSC / 16	fOSC / (16*98)
1/65 DUTY	Used internal oscillator circuit	fOSC / 24	fOSC / (24*66)
	Used **external** display clock	fOSC / 24	fOSC / (24*66)
1/33 DUTY	Used internal oscillator circuit	fOSC / 48	fOSC / (48*34)
	Used **external** display clock	fOSC / 48	fOSC / (48*34)
1/17 DUTY	Used internal oscillator circuit	fOSC / 88	fOSC / (88*18)
	Used **external** display clock	fOSC / 88	fOSC / (88*18)
1/9 DUTY	Used internal oscillator circuit	fOSC / 176	fOSC / (176*9)
	Used **external** display clock	fOSC / 176	fOSC / (176*9)
1/5 DUTY	Used internal oscillator circuit	fOSC / 320	fOSC / (320*5)
	Used **external** display clock	fOSC / 320	fOSC / (320*5)

(fFR is the liquid crystal alternating current period, and not the FR signal period.)

➢ **References for items market with ***

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.
*2 The operating voltage range for the VSS system and the V0 system is. This applies when the external power supply is being used.
*3 The A0, D0 to D5, D6, D7, XRD (E), XWR (RW), CS1B, CS2, CLS, STACOM, C86, PSB, RSTP, and IRS terminals.
*4 The D0 to D7and STACOM terminals.
*5 The A0, XRD (E), XWR (RW), CS1B, CS2, CLS, C86, PSB, RSTP, and IRS terminals.
*6 Applies when the D0 to D5, D6 ,D7, STACOM, and FR terminals are in a high impedance state.
*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage (3) range.
RON = 0.1 V / △I (Where △I is the current that flows when 0.1 V is applied while the power supply is ON.)
*8 See Table 23 for the relationship between the oscillator frequency and the frame rate frequency.
*9 The V0 voltage regulator circuit regulates within the operating voltage range of the voltage follower.
*10 This is the internal voltage reference supply for the V0 voltage regulator circuit. In the RW1092 , the temperature range approximately –0.05%/℃.
*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on. The RW1092 is 1/9 biased. Does not include the current due to the LCD panel capacity and wiring capacity. Applicable only when there is no access from the MPU.
*12 It is the value on a RW1092 having the VREG temperature gradient is –0.05%/℃ when the V0 voltage regulator internal resistor is used.

■ TIMING CHARACTERISTICS

➢ System Bus Read / Write Characteristics 1 (For the 8080 Series MPU)

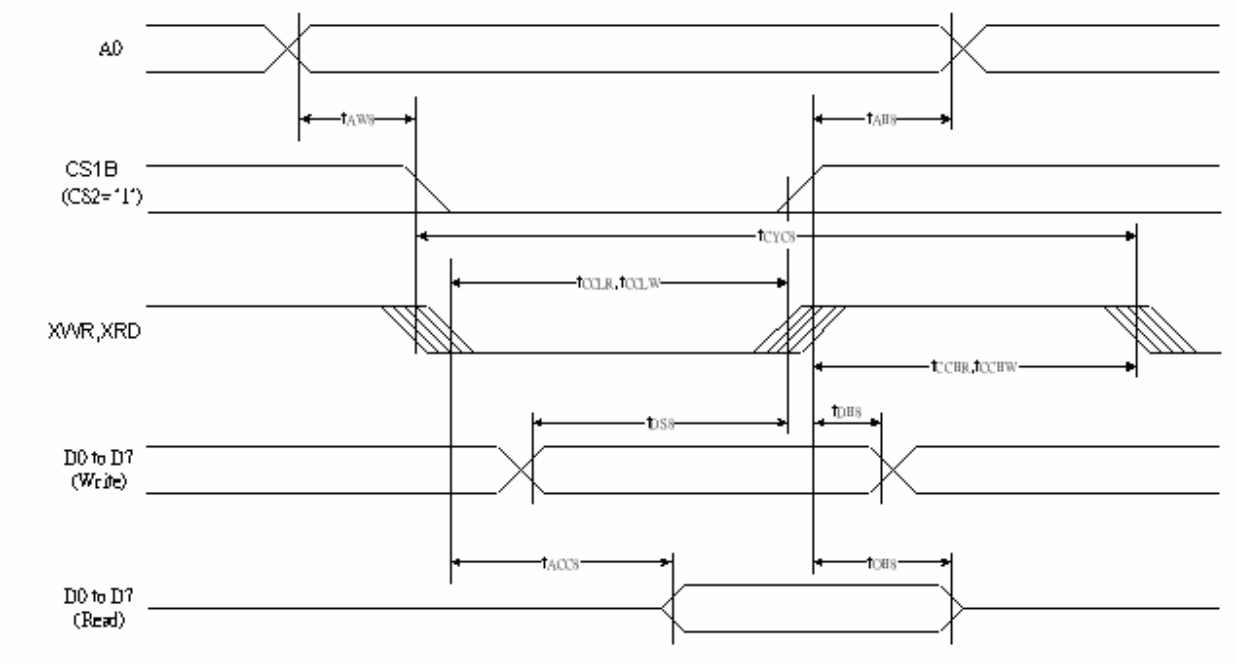


Figure 26

Table 24

(VDD = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	Ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

Table 25

(VDD = 2.7 V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

Table 26

(VDD = 1.8V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
*2 All timing is specified using 20% and 80% of VDD as the reference.
*3 tCCLW and tCCLR are specified as the overlap between CS1B being “L” (CS2 = “H”) and XWR and XRD being at the “L” level.

➢ **System Bus Read / Write Characteristics 2 (For the 6800 Series MPU)**

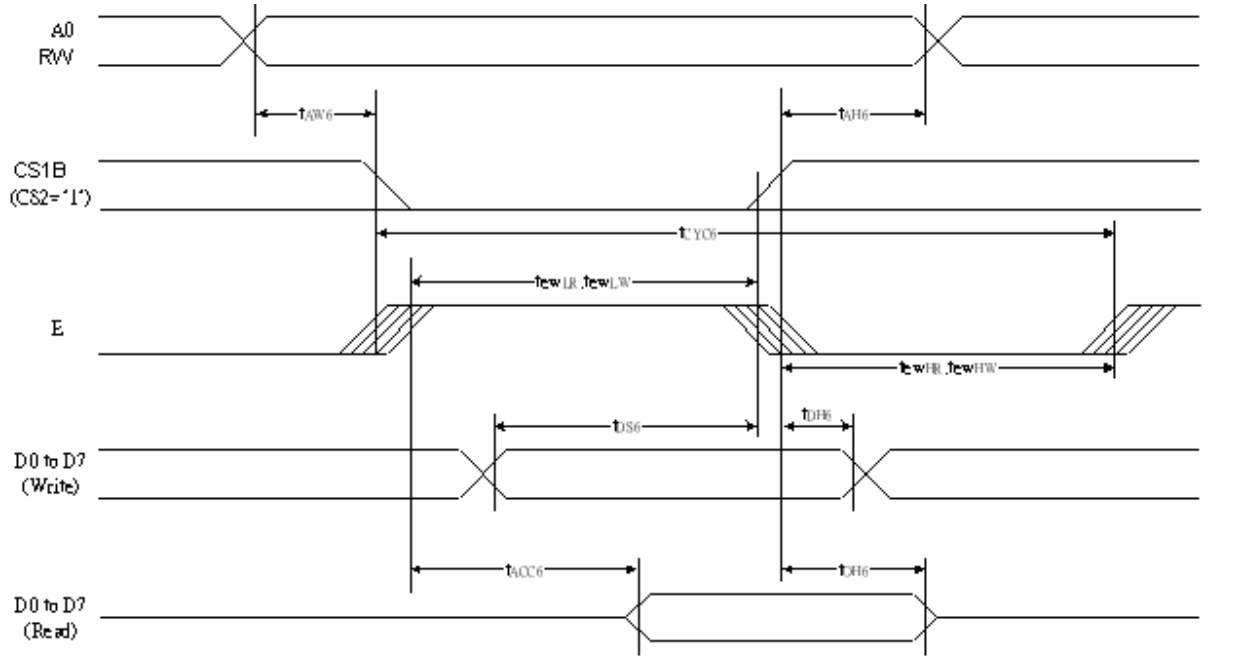


Figure 27

Table 27

(VDD = 3.3 V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	WR	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	RD	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

Table 28

(VDD = 2.7V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	WR	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	RD	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

Table 29

(VDD =1.8V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	WR	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	RD	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.
*2 All timing is specified using 20% and 80% of VDD as the reference.
*3 tEWLW and tEWLR are specified as the overlap between CS1B being “L” (CS2 = “H”) and E.

➢ **The Serial Interface**

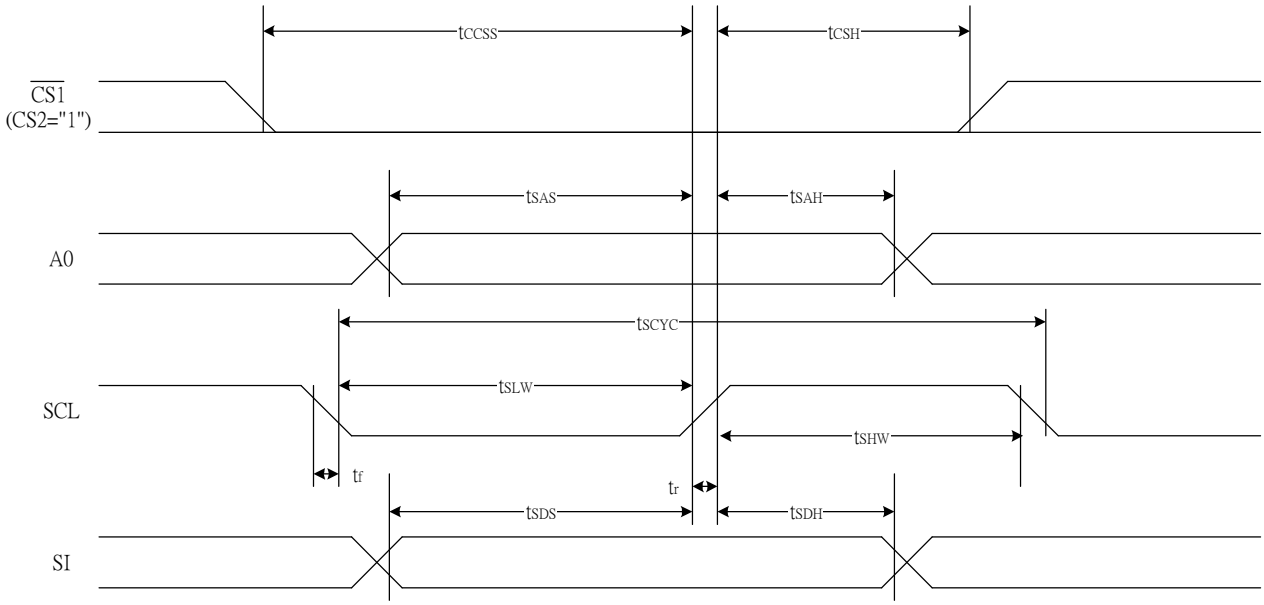


Figure 28

Table 30

(VDD = 3.3V, Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	Tscyc		50	—	ns
SCL “H” pulse width		Tshw		25	—	
SCL “L” pulse width		TSLW		25	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

Table 31

(VDD =2.7V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	Tscyc		100	—	ns
SCL “H” pulse width		TSHW		50	—	
SCL “L” pulse width		TSLW		50	—	
Address setup time	A0	TSAS		30	—	
Address hold time		TSAH		20	—	
Data setup time	SI	TSDS		30	—	
Data hold time		TSDH		20	—	
CS-SCL time	CS	TCSS		30	—	
CS-SCL time		TCSH		60	—	

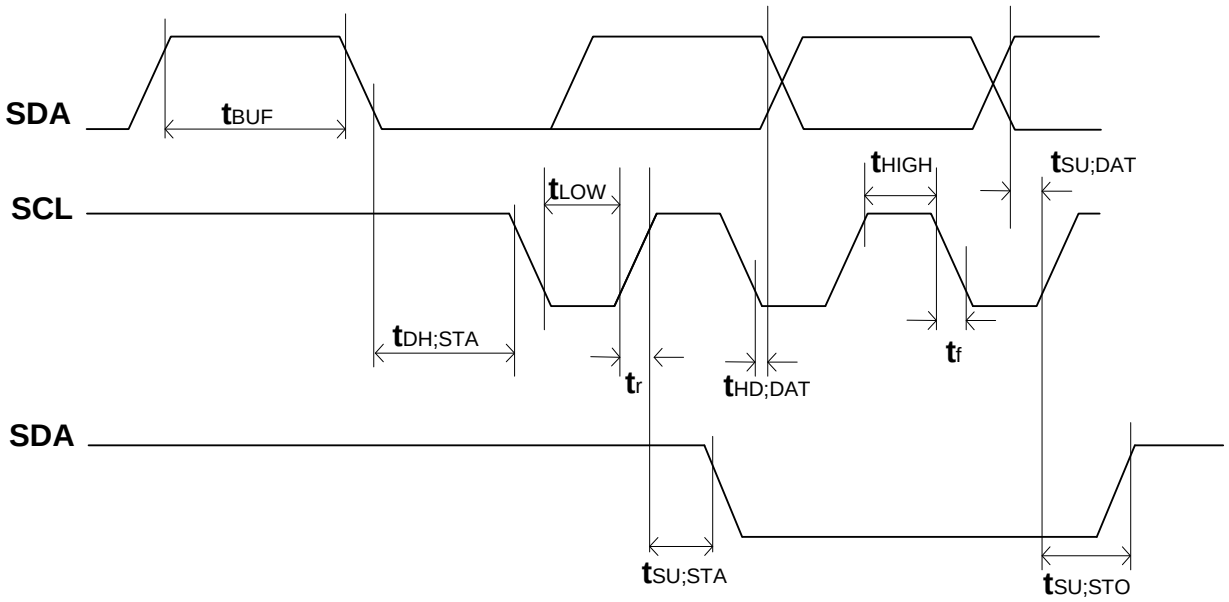
Table32

(VDD = 1.8V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	TSCYC		200	—	ns
SCL “H” pulse width		TSHW		80	—	
SCL “L” pulse width		TSLW		80	—	
Address setup time	A0	TSAS		60	—	
Address hold time		TSAH		30	—	
Data setup time	SI	TSDS		60	—	
Data hold time		TSDH		30	—	
CS-SCL time	CS	TCSS		40	—	
CS-SCL time		TCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of VDD as the standard.

➢ **IIC interface**



(Ta = 25℃)

Item	Signal	Symbol	Condition	VDD=1.8 to 2.7V Rating		VDD=2.7 to 3.6V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SI	$t_{SU;DAT}$	—	180	–	80	–	ns
Data hold time		$t_{HD:DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SI	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

■ RESET TIMING

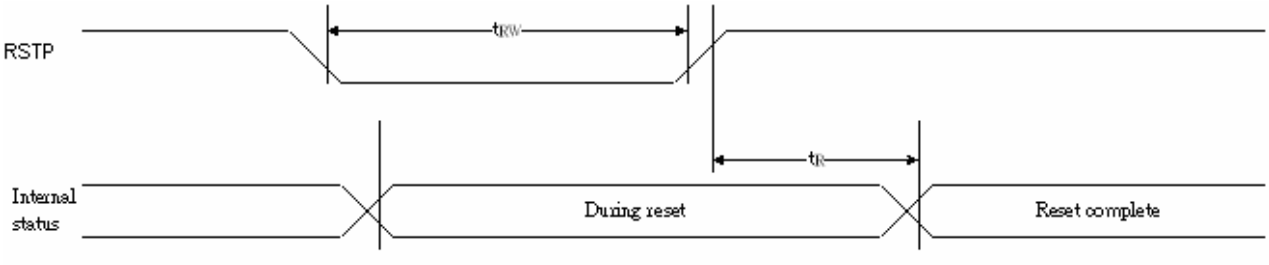


Figure 29

Table 36

(VDD = 3.3V , Ta = –40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.0	us
Reset “L” pulse width	RSTP	tRW		1.0	—	—	us

Table 37

(VDD = 2.7V , Ta = –40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RSTP	tRW		2.0	—	—	us

Table 38

(VDD = 1.8V , Ta = –40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	3.0	us
Reset “L” pulse width	RSTP	tRW		3.0	—	—	us

*1 All timing is specified with 20% and 80% of VDD as the standard.

★Application Notes for Static Display:

RW1092 can support Static display with different gray level thru STACOM pad and SEG0~191 pads.
When static display has been selected, please set up the relative registers as follow:

1. static indicator set to “ON” and static indicator register set to “1” (instruction code : ADH + 01H)
2. LCD bias set to 1/2 bias (instruction code : A3H)
3. Switch off all LCD power including booster, regulator, follower.(instruction code : 28H)
4. duty set to 1/5 duty (Pin select : SEL1=”L”, SEL2=”L”, SEL3=”L”)
5. CLS set to VDD (internal oscillator used)
6. Connect V0 to VDD
7. keep all COMMON pads opened

◆ Gray scale output static display

RW1092 has a special design for the static output, that can make user to get a different gray level output display. Figure. A-1 and Table A-1 shows a example for the gray scale output display waveform for static display

Page Address	Data	Column Address							
		S0	S1	S2	S3	S4	S5	→	S191
0,0,0,0	DB0	■	■	■	■	■		→	
	DB1	■	■	■	■				
	DB2	■	■	■					
	DB3	■	■						
1,1,1,1	DB0	■							

Table A-1 RAM map for static display

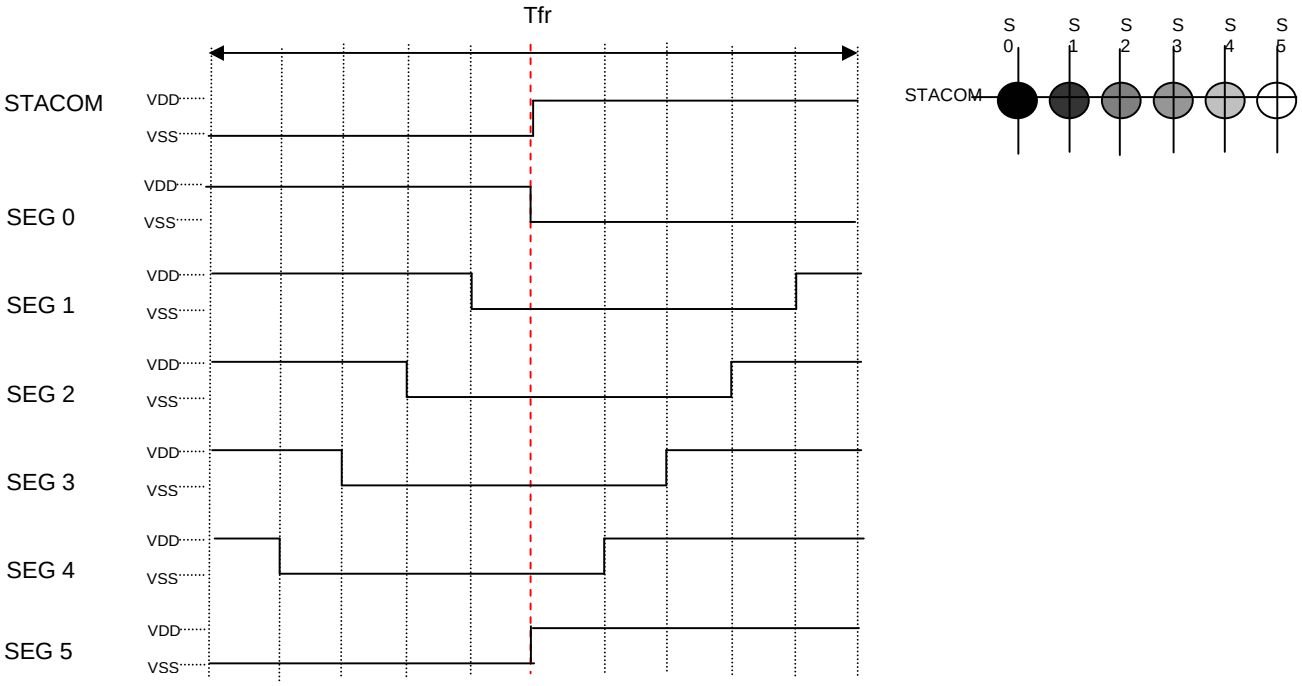
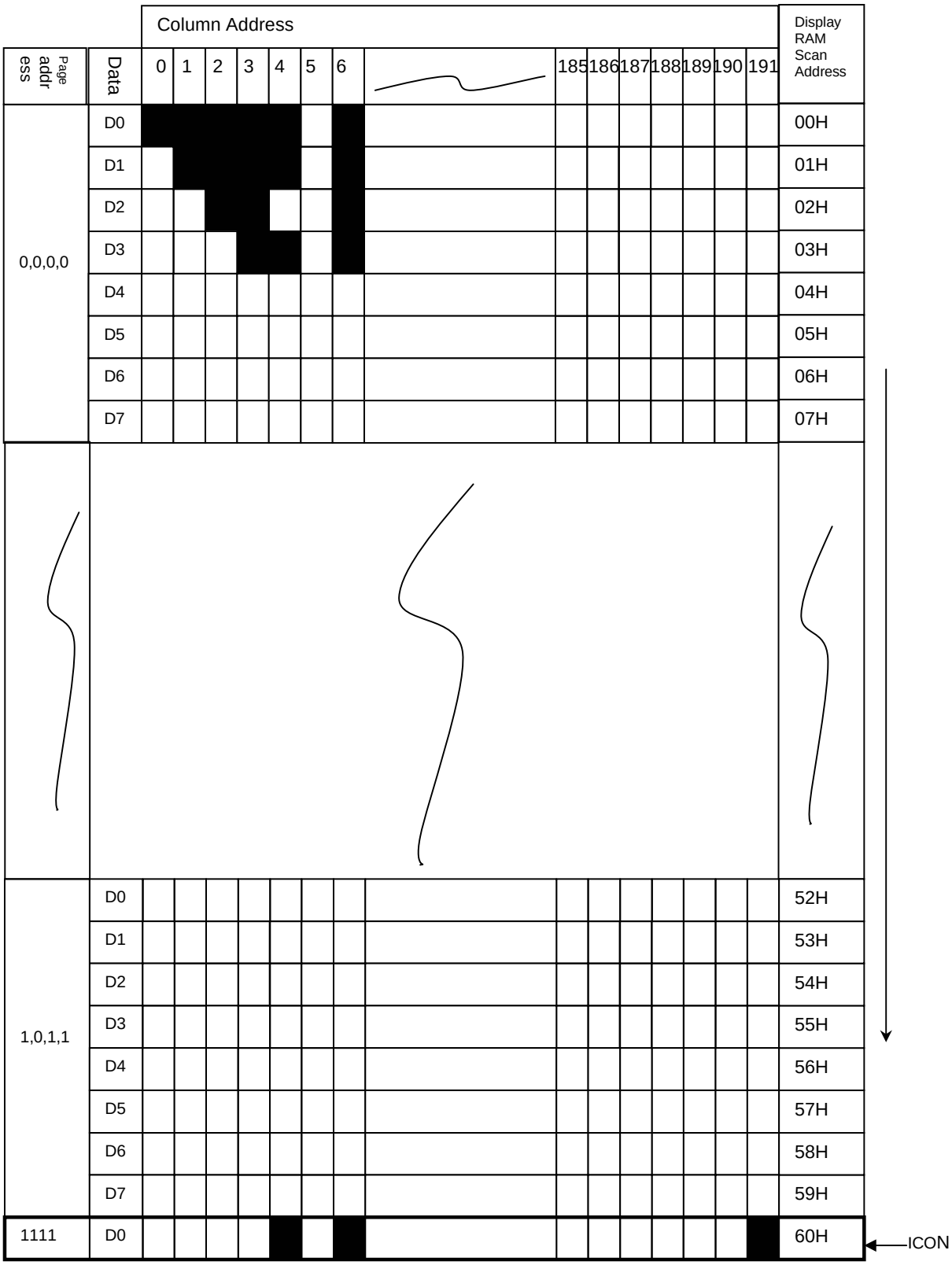


Figure A-1 static display waveform for different gray level LCD output

The following shows Example waveform for Static Display for RW1092.



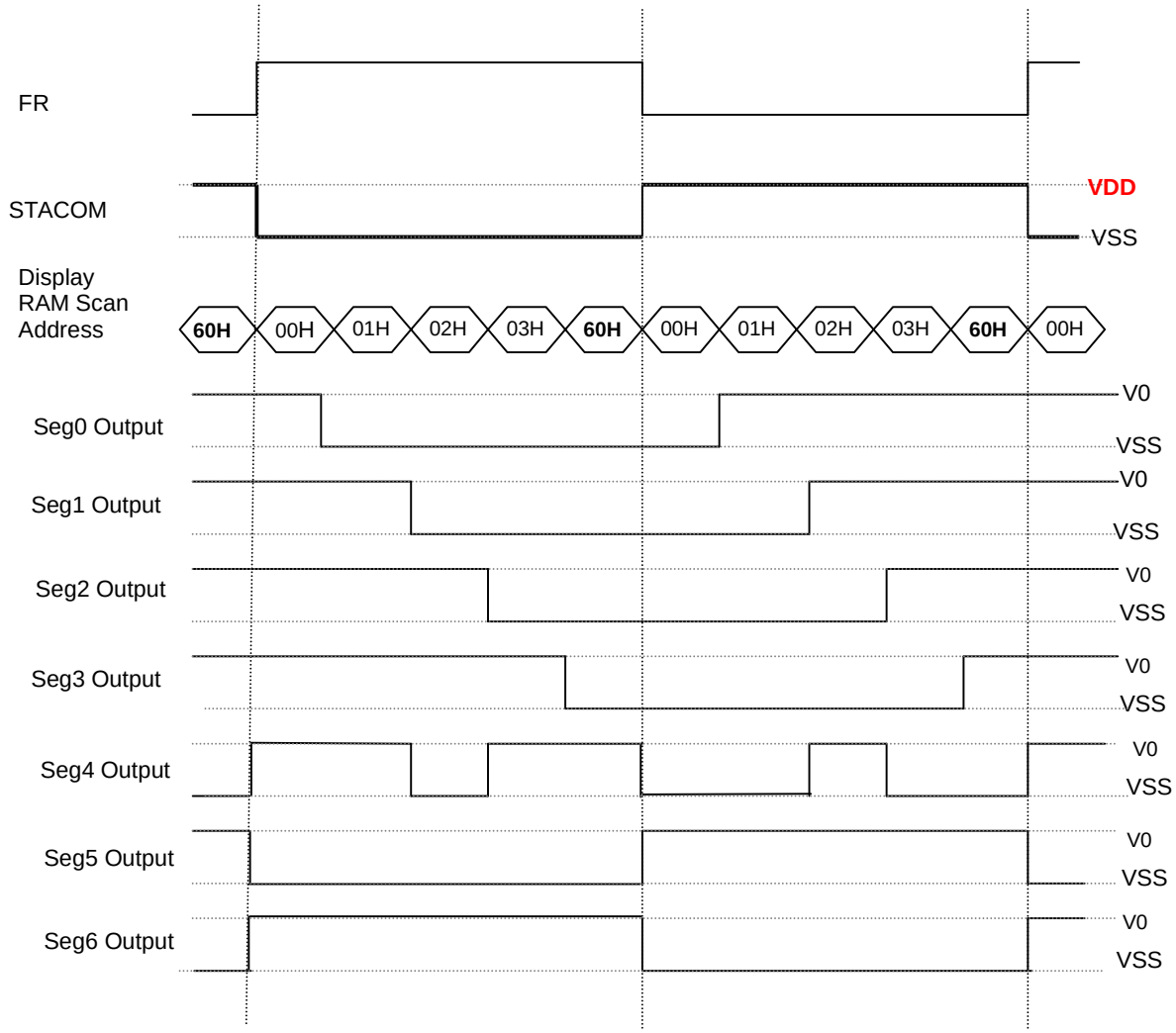


Fig 22 Static Display Output Waveform

■ THE MPU INTERFACE (REFERENCE EXAMPLES)

The RW1092 Series can be connected to either 80X86 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the RW1092 series chips with fewer signal lines.
The display area can be enlarged by using multiple RW1092 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 6800 Series MPUs (PSB="H",C86="H")

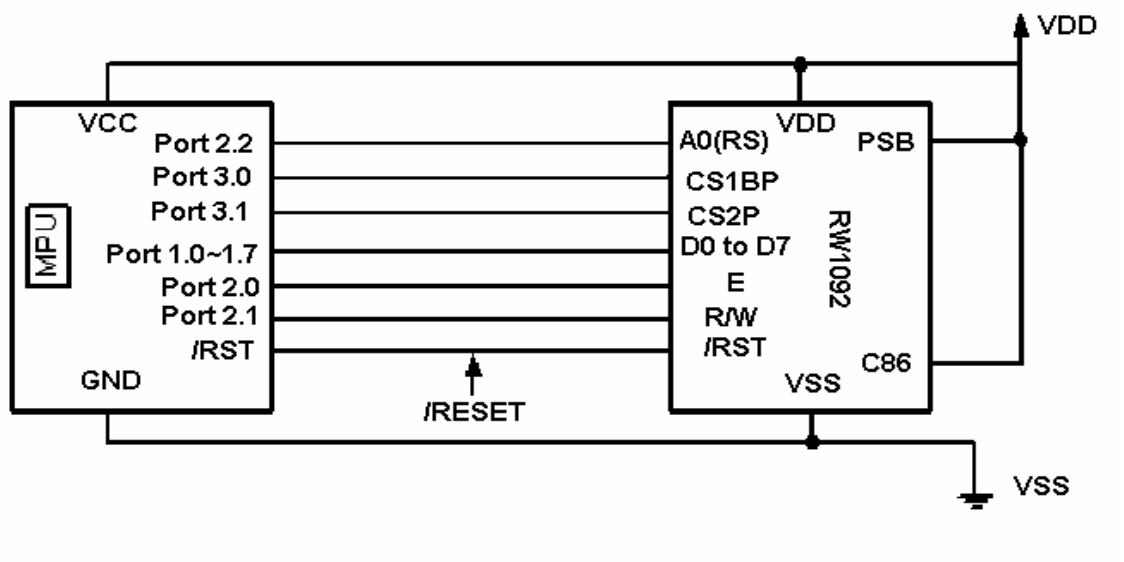


Figure 30-1

(2) 8080 Series MPUs (PSB="H",C86="L")

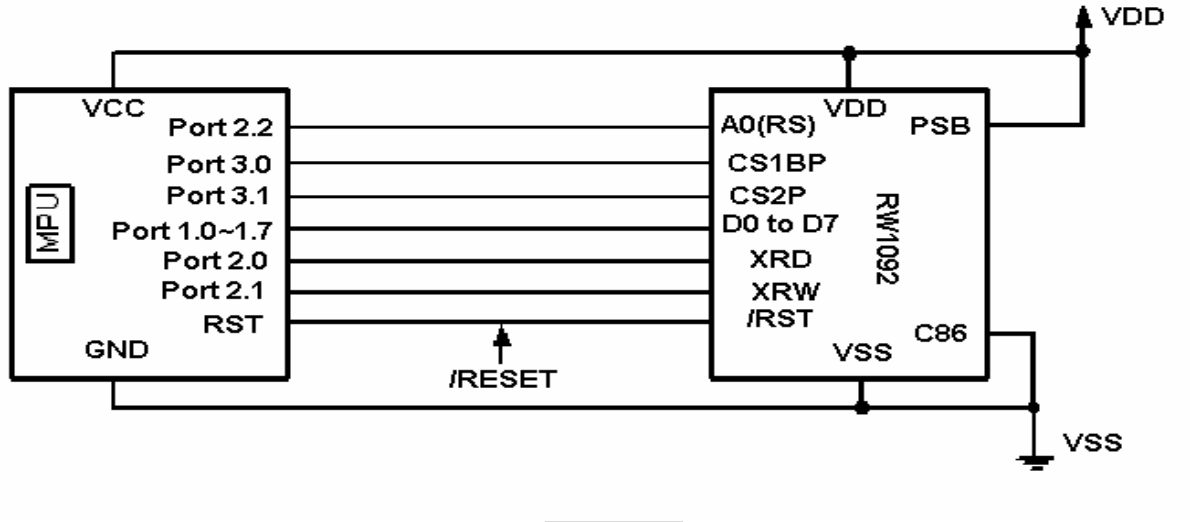


Figure 30-2

(3) Using the Serial Interface(4-line) (PSB="L",C86="H")

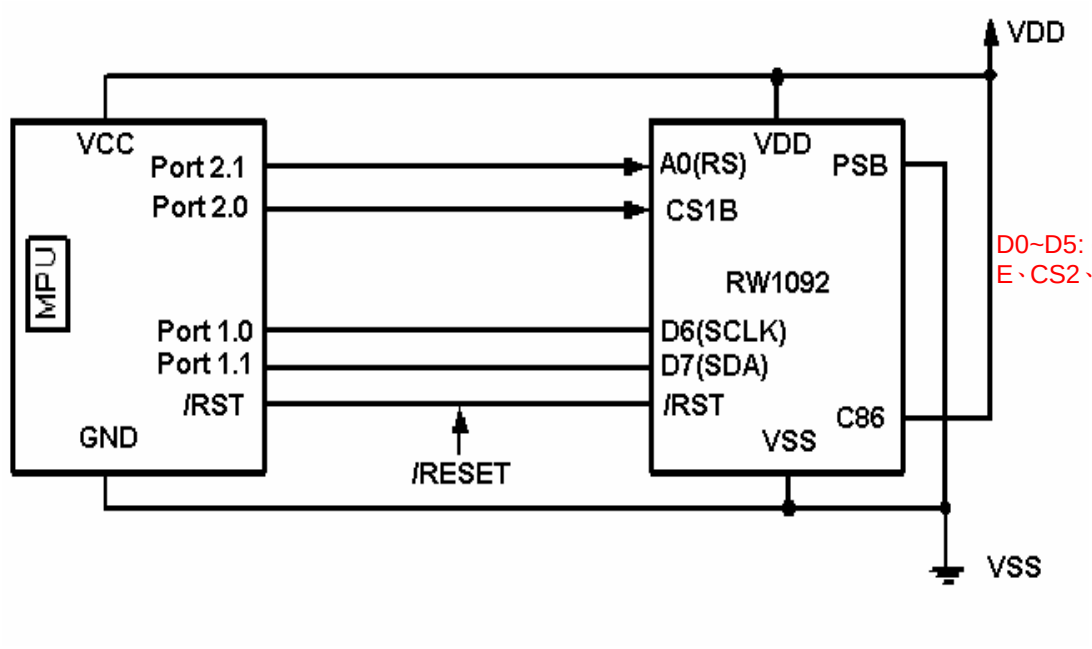


Figure 30-3

(4) Using the Serial Interface(3-line) (PSB="L",C86="H")

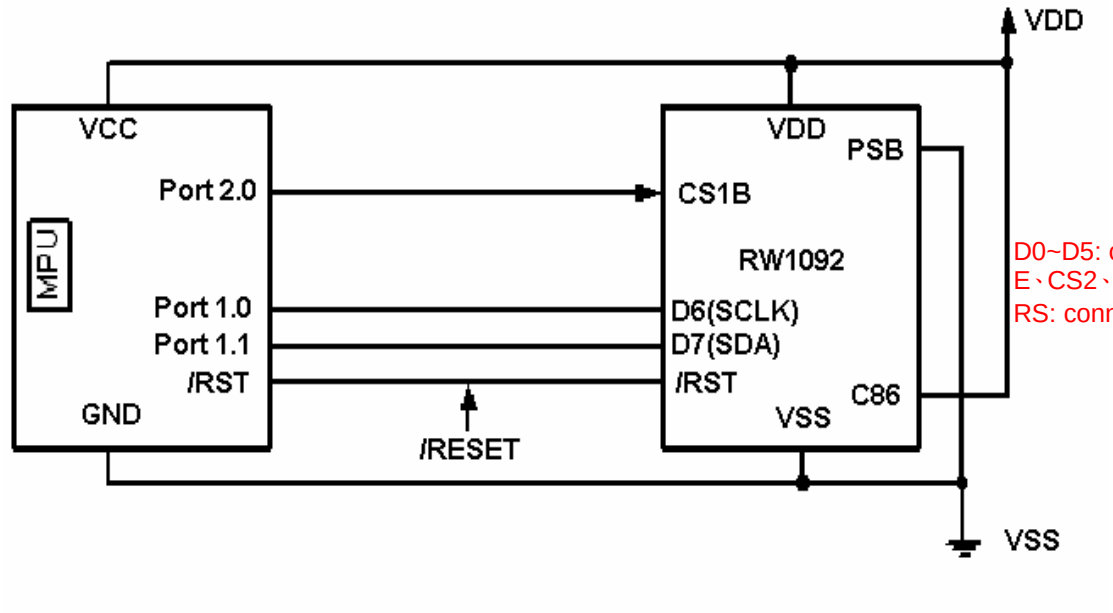


Figure 30-4

(5) Using the Serial Interface(IIC) (PSB="L",C86="L")

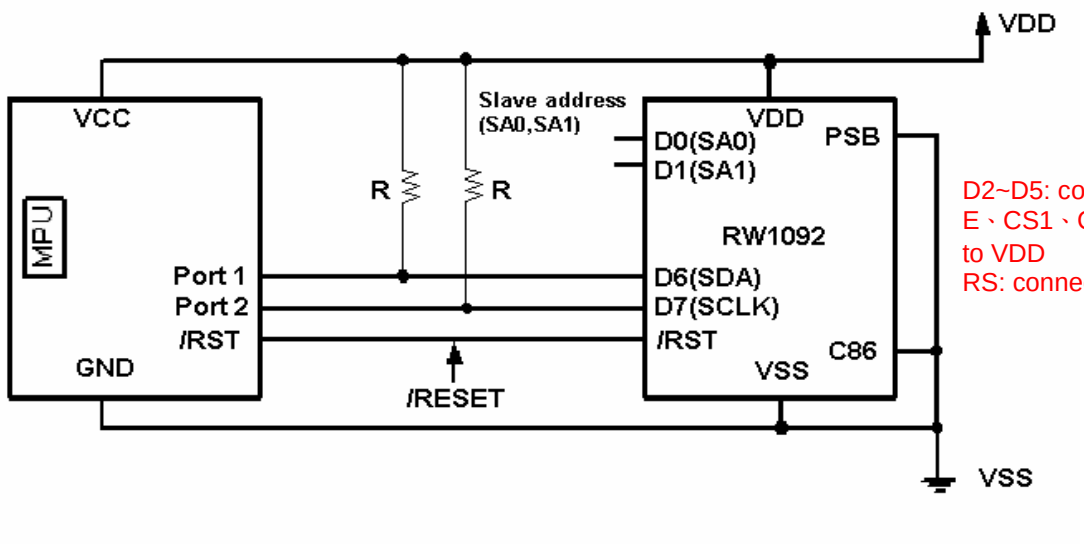


Figure 30-5

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting

Interface databus pin setting

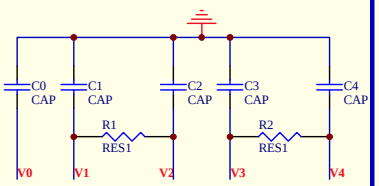
Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

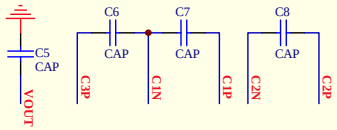
Bias ratio default :1/10 bias(Instruction setting)

Regulator,Follower Circuit



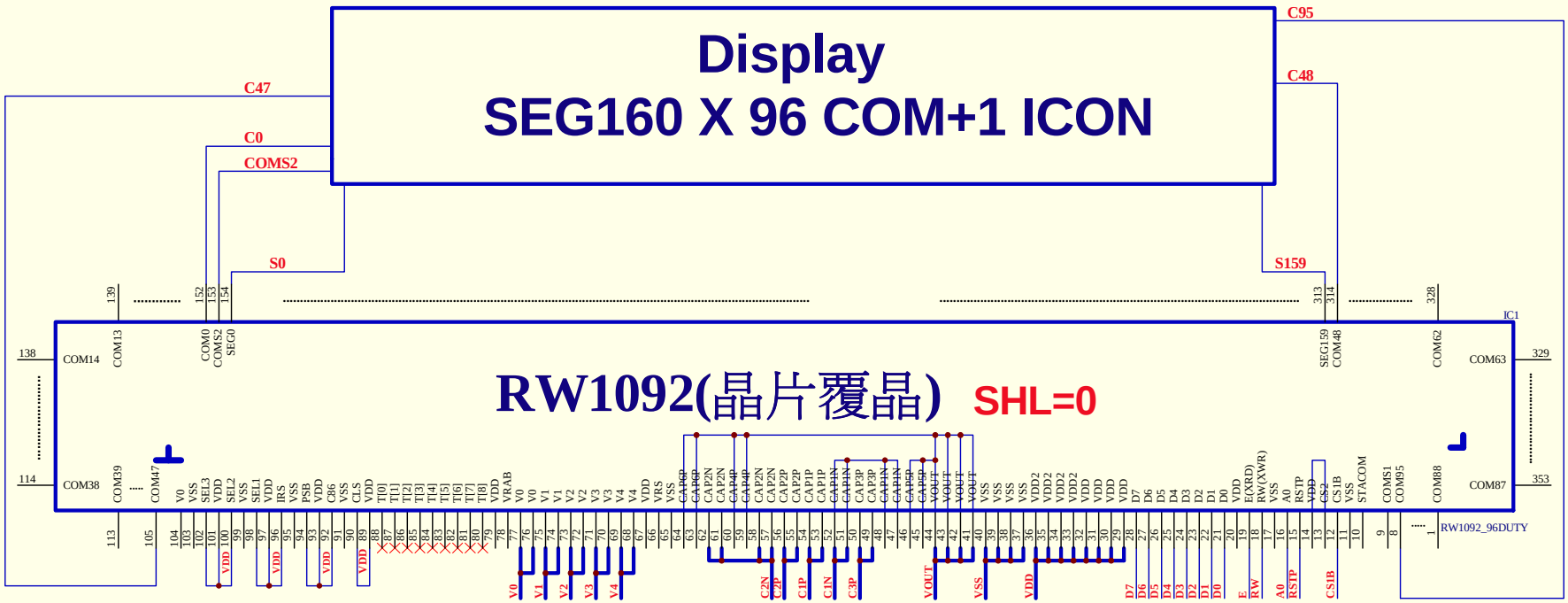
Cap: 2.2uF~4.7uF

Booster Circuit



Now Setting: 4X
Cap: 2.2uF~4.7uF

Display
SEG160 X 96 COM+1 ICON



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Size	B
Number	RW1092_160x96
Revision	A
Date:	17-May-2010
File:	D:\公司資料\99se\MyDesign.ddb
Sheet of	
Drawn By:	

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting

Interface databus pin setting

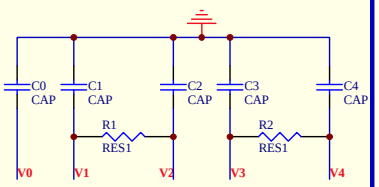
Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

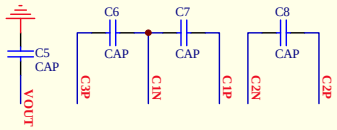
Bias ratio default :1/9 bias(Instruction setting)

Regulator,Follower Circuit



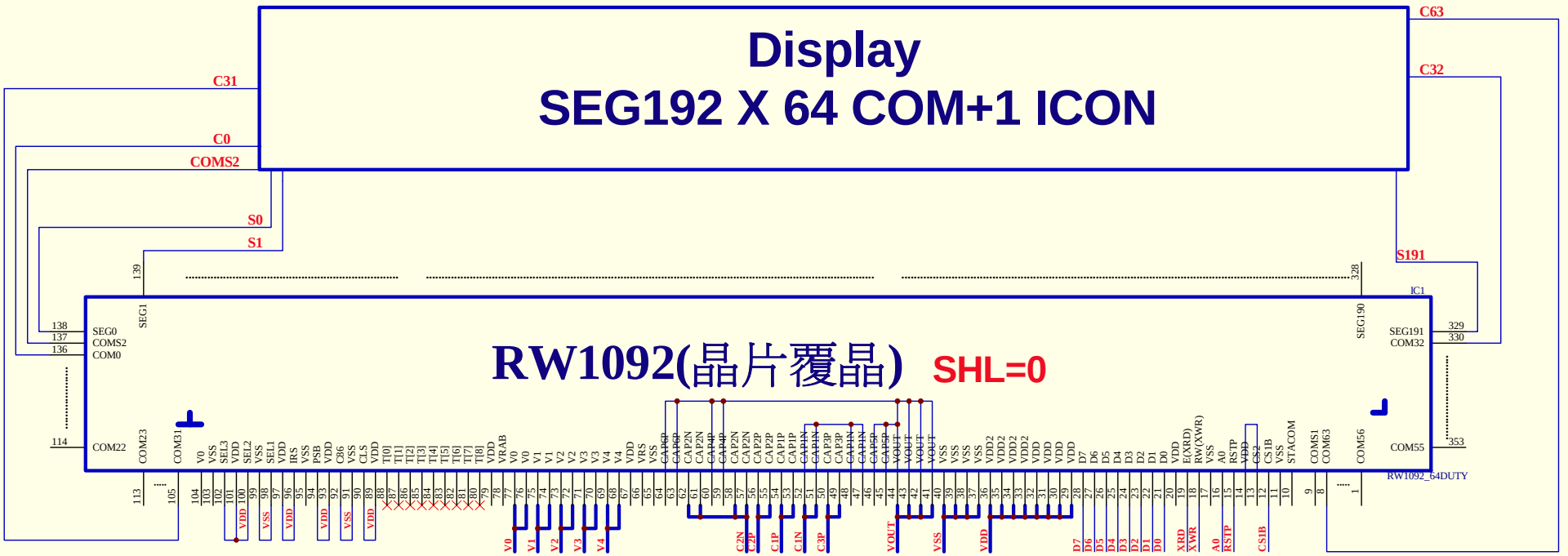
Cap: 2.2uF~4.7uF

Booster Circuit



Now Setting: 4X
Cap: 2.2uF~4.7uF

Display
SEG192 X 64 COM+1 ICON



RW1092(晶片覆晶) SHL=0

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Size	Number		Revision
B	RW1092_192x64		A
Date:	17-May-2010	Sheet of	
File:	D:\公司資料\99se\MyDesign.ddb	Drawn By:	

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting 4SPI

Interface databus pin setting

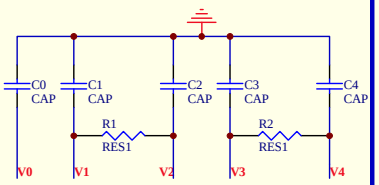
Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

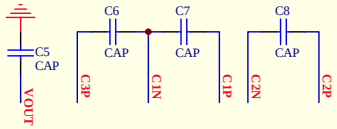
Bias ratio default :1/6 bias(Instruction setting)

Regulator,Follower Circuit



Cap: 2.2uF~4.7uF

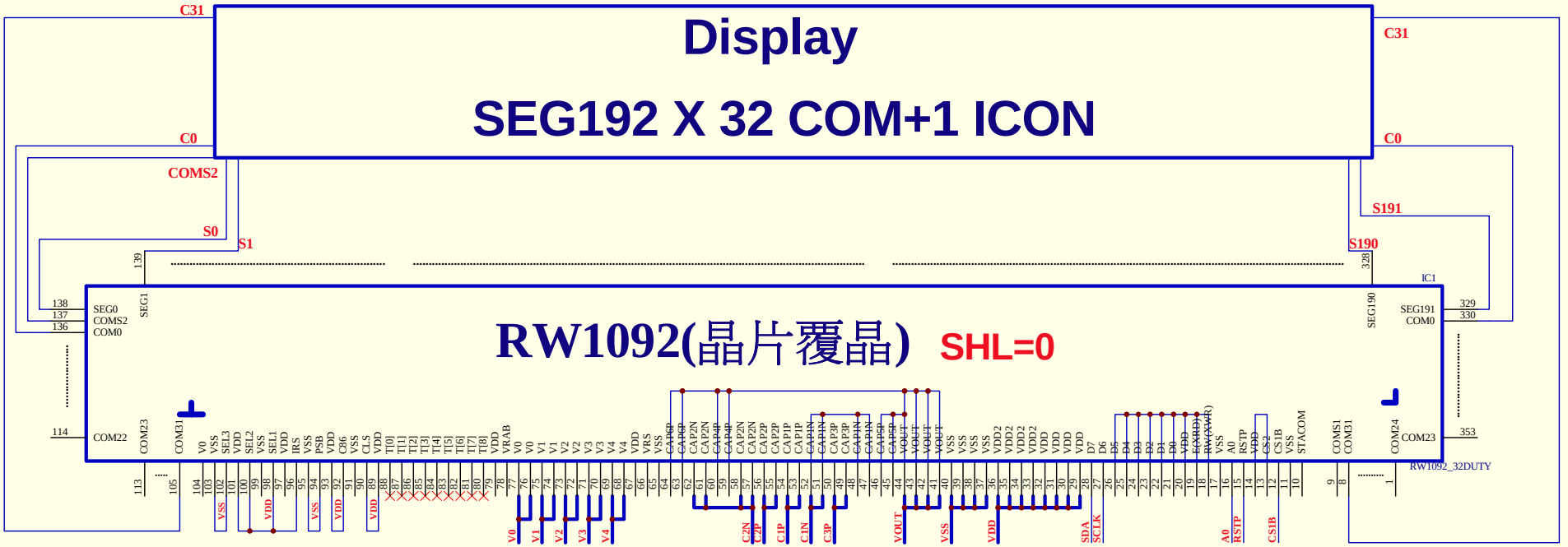
Booster Circuit



Now Setting: 4X
Cap: 2.2uF~4.7uF

Display

SEG192 X 32 COM+1 ICON



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Date: 17-May-2010		Sheet of	
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:	

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting 3SPI

Interface databus pin setting

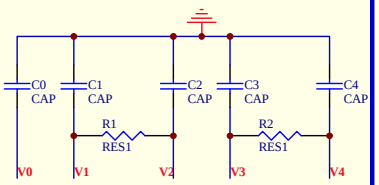
Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

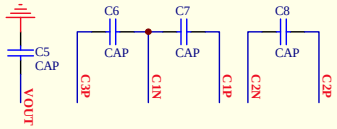
Bias ratio default :1/5 bias(Instruction setting)

Regulator,Follower Circuit



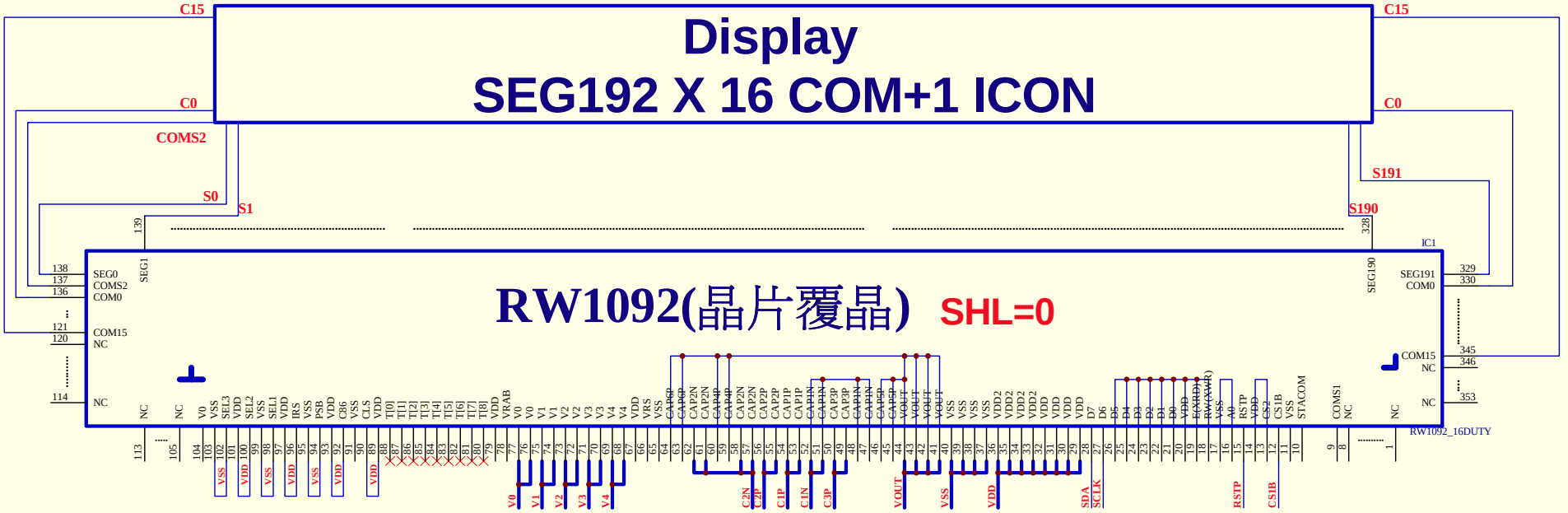
Cap: 2.2uF~4.7uF

Booster Circuit



Now Setting: 4X
Cap: 2.2uF~4.7uF

Display
SEG192 X 16 COM+1 ICON



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Size: B	Number: RW1092_192x16	Revision: A	
Date: 17-May-2010	Sheet of		
File: D:\公司資料\99se\MyDesign.ddb	Drawn By:		

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting

Interface databus pin setting

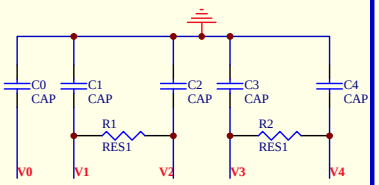
Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

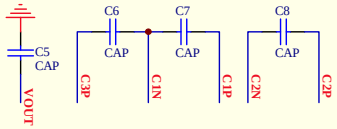
Bias ratio default :1/5 bias(Instruction setting)

Regulator,Follower Circuit



Cap: 2.2uF~4.7uF

Booster Circuit

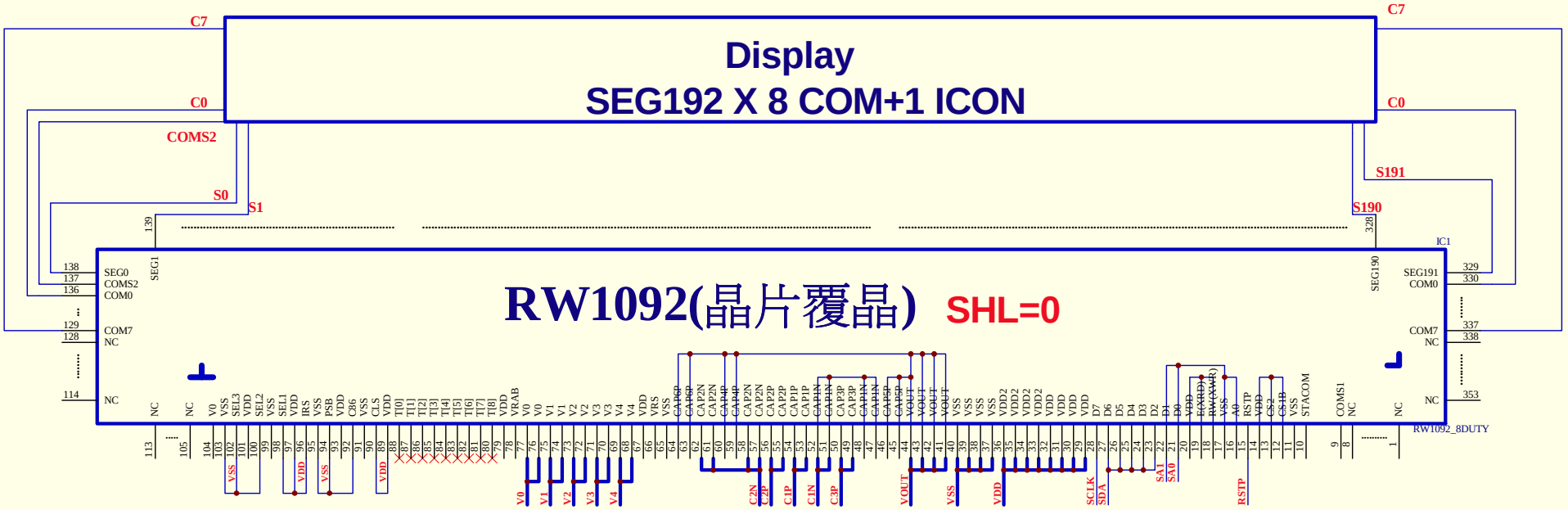


Now Setting: 4X

Cap: 2.2uF~4.7uF

Display
SEG192 X 8 COM+1 ICON

RW1092(晶片覆晶) SHL=0



	SA1	SA0	Slave address
01111	0	0	0x78
01111	0	1	0x7a
01111	1	0	0x7c
01111	1	1	0x7e

Now Setting

Title: RockWorks		
Size: B	Number: RW1092_192x8	Revision: A
Date: 17-May-2010		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting

Interface databus pin setting

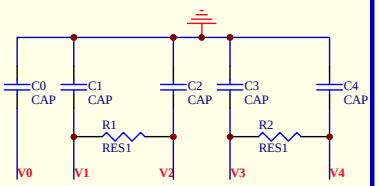
Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

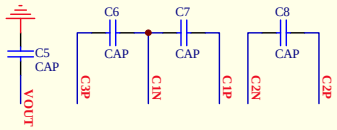
Bias ratio default :1/3 bias(Instruction setting)

Regulator,Follower Circuit



Cap: 2.2uF~4.7uF

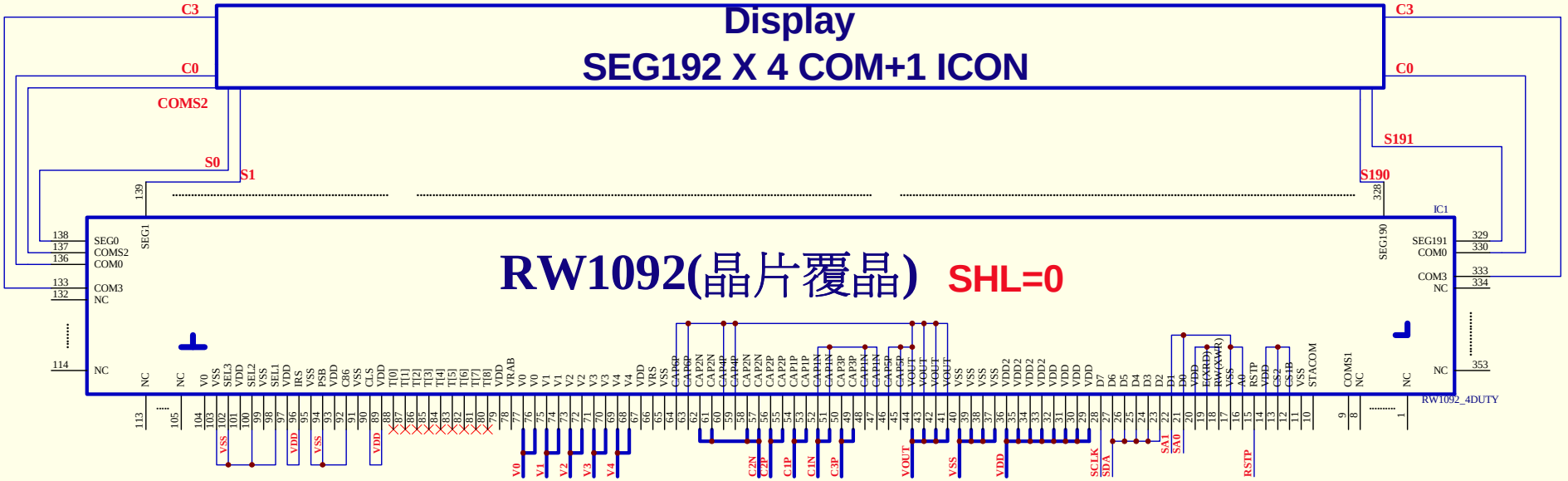
Booster Circuit



Now Setting: 4X

Cap: 2.2uF~4.7uF

Display
SEG192 X 4 COM+1 ICON



	SA1	SA0	Slave address
01111	0	0	0x78
01111	0	1	0x7a
01111	1	0	0x7c
01111	1	1	0x7e

Now Setting

Title: RockWorks		
Size: B	Number: RW1092_192x4	Revision: A
Date: 17-May-2010		Sheet of
File: D:\公司資料\99se\MyDesign.ddb		Drawn By:

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8080 series
1	1	6800 series

Now Setting

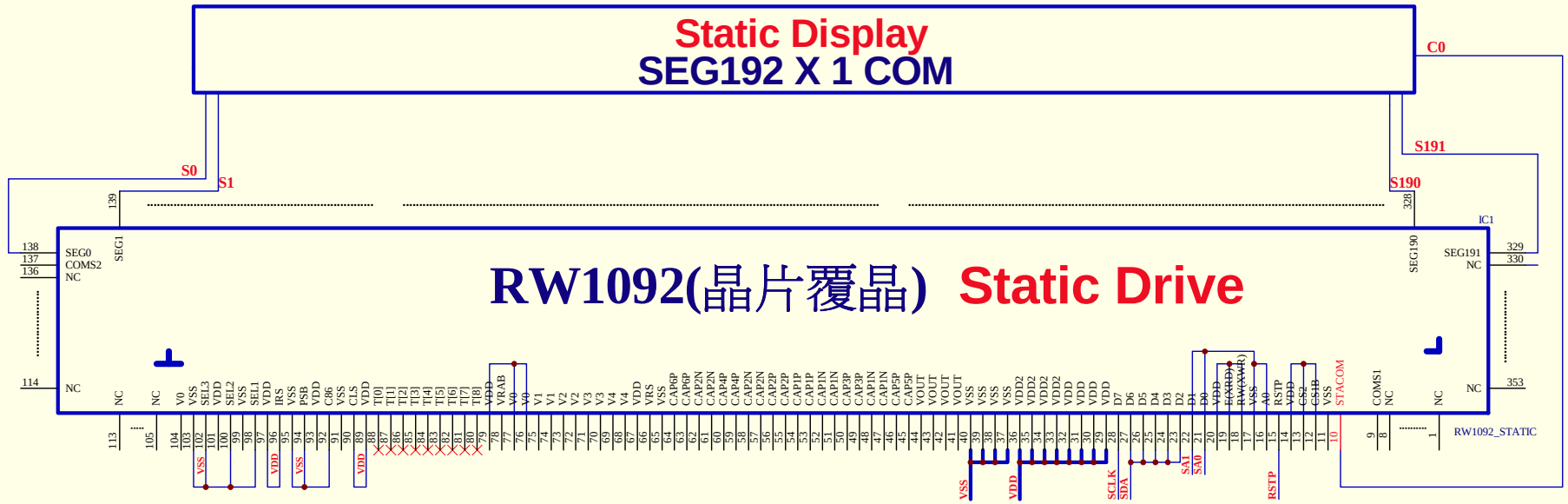
Interface databus pin setting

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCLK	SDA	D5~D2 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	A0	VDD	VDD	SDA	SCLK	VDD
4SPI	CS1B	VDD	VSS	VDD	VDD	SDA	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A1	E	RW	D7	D6	D5~D0

CLS="H" used internal oscillator circuit

IRS="H" use the internal resistors

Bias selection must be set to 1/2 bias



	SA1	SA0	Slave address
01111	0	0	0x78
01111	0	1	0x7a
01111	1	0	0x7c
01111	1	1	0x7e

Now Setting

Title	RockWorks	
Size: B	Number: RW1092_192x1_Static	Revision: A
Date: 17-May-2010	Sheet of	
File: D:\公司資料\99se\MyDesign.ddb	Drawn By:	