DATA SHEET

OTA5180A

1440x544 System-On-Chip Driver for 480RGBx272 TFT LCD

Preliminary

APR. 01, 2008

Version 0.2

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1440x544 TFT-LCD DRIVER AND CONTROLLER

1. GENERAL DESCRIPTION

OTA5180A is a single chip driver solution combining a source driver, a gate driver, a timing controller, a power supply circuit and a back-light control circuit, especially designed for color TFT LCDs. The OTA5180A supports panel resolutions of 480xRGBx272. The system can be configured through a R/W 3-wire serial interface.

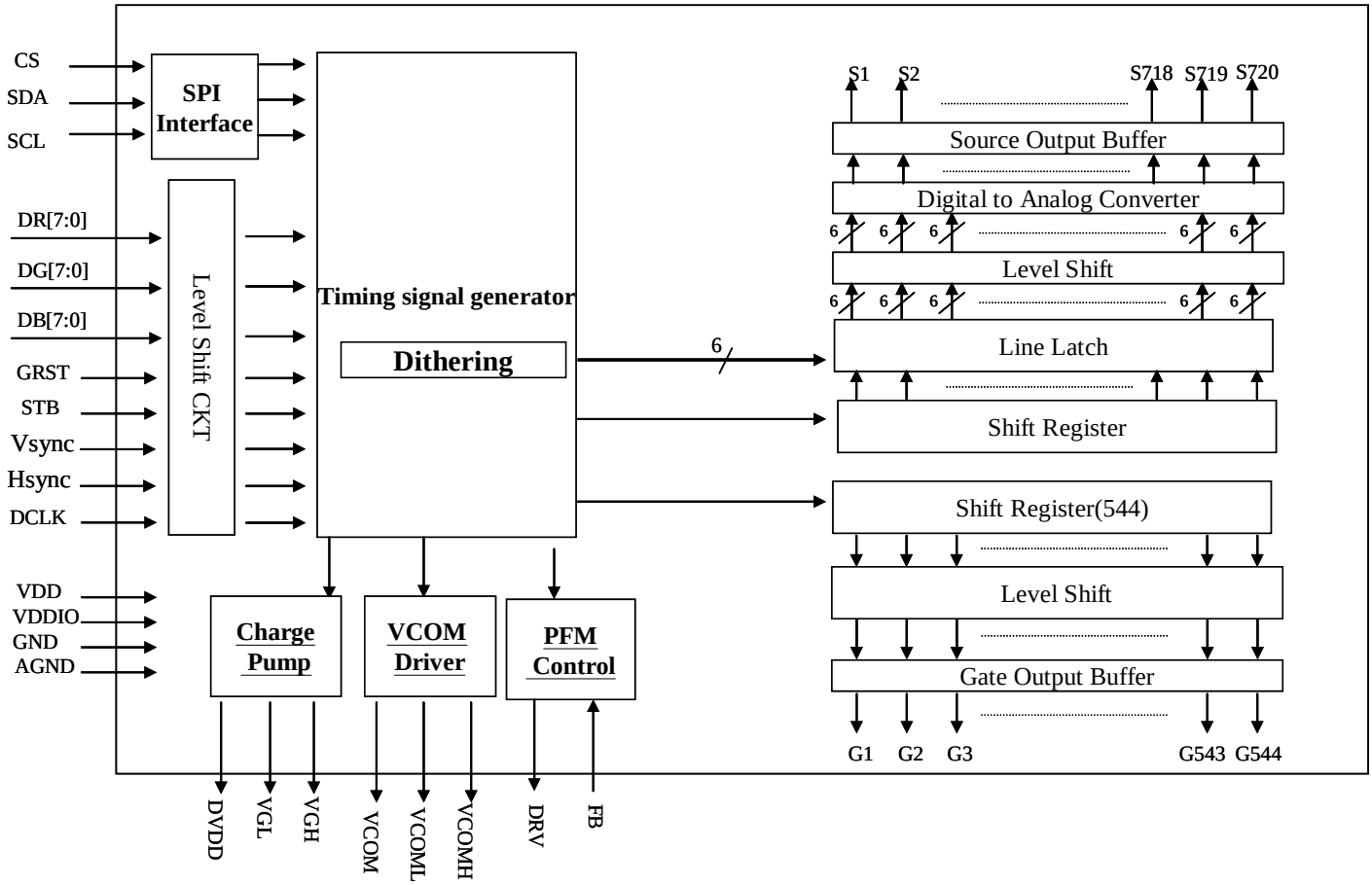
2. FEATURES

- LCD driver with timing controller
- Line/Frame Inversion
- 720 source output channels
- 544 gate output channels
- 8-bit resolution 256 gray scale with dithering (6 bits DAC +2 bit dithering)
- Support both SYNC and SYNC-DE mode input timing
- Support parallel RGB (24-bit) input interface and Serial RGB (8-bit) input interface
- Display control and configuration selected by 3-wire serial communication control
- Built-in DC-DC control circuit, charge pump circuit, VCOM circuit with programmable adjustment
- Built-in R-DAC gamma correction
- Output deviation: 20mV
- Power for LCD driving: 4.2V ~ 6V
- Power for charge pump supply (VDD): 2.25V ~ 3.6V
- Power for digital interface: 1.8V ~ VDD
- COG package
- Built-in power saving mode

3. ORDERING INFORMATION

Product Number	Package Type
OTA5180A-C	Chip form with Gold Bump

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
Serial Communication Interface / Timming Controller (Tcon) / Mode Selection		
CS	I (VDDIO)	Serial communication chip select
SDA	I/O (VDDIO)	Serial communication data input and output
SCL	I (VDDIO)	Serial communication clock input
PARA_SERI	I (VDDIO)	Parallel 24-bit and Serial 8-bit data input selection. PARA_SERI="H", Parallel 24-bit RGB input through DR0~7, DB0~DB7, DG0~DG7 (Default) PARA_SERI="L", Serial 8-bit data input through DR0~DR7
DR0~DR7	I (VDDIO)	When PARA_SERI="H", these will be treated as 8-bit digital Red data input When PARA_SERI="L", these will be treated as serial 8-bit data input
DG0~DG7	I (VDDIO)	8-bit digital Green data input, only valid when PARA_SERI="H"
DB0~DB7	I (VDDIO)	8-bit digital Blue data input, only valid when PARA_SERI="H"
DCLK	I (VDDIO)	Clock signal; latching data at the falling edge
HSYNC	I (VDDIO)	Horizontal sync signal; negative polarity
VSYNC	I (VDDIO)	Vertical sync signal; negative polarity
DE	I (VDDIO)	Data input enable. Active High to enable the data input.
SYNC	I (VDDIO)	SYNC or SYNC-DE mode selection: SYNC = "Low": accepted SYNC-DE mode input timing (Default) SYNC = "High": accepted SYNC mode input timing
HDIR	I (VDDIO)	Horizontal scan direction control (Please refer to the register setting : HDIR) HDIR(pin) = "Low" : The definition of HDIR register setting is inversion from original. HDIR(register) = "0" : Shift from left to right; HDIR(register) = "1" : Shift from right to left. (Default of the Register) HDIR(pin) = "High":The definition of HDIR register setting is invariant. (Default) HDIR(register) = "0" : Shift from right to left; HDIR(register) = "1" : Shift from left to right. (Default of the Register)
VDIR	I (VDDIO)	Vertical scan direction control (Please refer to the register setting : VDIR) VDIR(pin) = "Low": The definition of VDIR register setting is inversion from original. VDIR(register) = "0": Shift from up to down; VDIR(register) = "1": Shift from down to up. (Default of the Register) VDIR(pin) = "High": The definition of VDIR register setting is invariant. (Default) VDIR(register) = "0": Shift from down to up; VDIR(register) = "1": Shift from up to down. (Default of the Register)
MVA_TN	I (VDDIO)	Set the TN or MVA mode. MVA_TN= "Low" : TN MVA_TN= "High" : MVA mode. (Default)
TN_TYPE	I (VDDIO)	To identify the liquid crystal is TN or not. TN_TYPE = "Low" : The liquid crystal is TN mode1, with lower VCOM power applied. TN_TYPE = "High" : The liquid crystal is TN mode2 or MVA, with higher VCOM power applied. (Default)

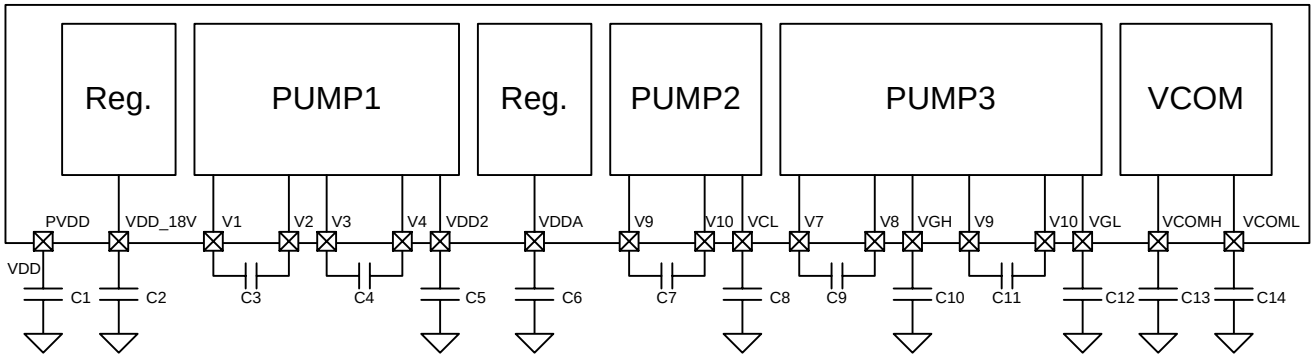
<table>
<tr><td>PWR_SEL</td><td>I
(VDDIO)</td><td colspan="3">Charge pump power selection
When VDD=2.5V, PWR_SEL = “Low”
When VDD=3.3V, PWR_SEL = “High” (Default)</td></tr>
<tr><td>OP0 - OP1</td><td>I
(VDDIO)</td><td colspan="3">Source driver driving capability selection. OP0 and OP1 pins are internal pulled to default setting.
<table><tr><th>OP1</th><th>OP0</th><th>Driving capability</th></tr><tr><td>LOW</td><td>LOW</td><td>-25%</td></tr><tr><td>LOW (Default)</td><td>HIGH (Default)</td><td>Normal (Default)</td></tr><tr><td>HIGH</td><td>LOW</td><td>+25%</td></tr><tr><td>HIGH</td><td>HIGH</td><td>+50%</td></tr></table></td></tr>
<tr><td>VDPOL</td><td>I
(VDDIO)</td><td colspan="3">Vsync polarity control.
VDPOL=”1”, negative polarity (default)
VDPOL=0, positive polarity</td></tr>
<tr><td>HDPOL</td><td>I
(VDDIO)</td><td colspan="3">Hsync polarity control.
HDPOL=”1”, negative polarity (default)
HDPOL=”0”, positive polarity</td></tr>
<tr><td>DCLKPOL</td><td>I
(VDDIO)</td><td colspan="3">DCLK polarity control.
DCLKPOL=”1”, negative polarity (default)
DCLKPOL=”0”, positive polarity</td></tr>
<tr><td>DATA_RB</td><td>I
(VDDIO)</td><td colspan="3">Data R[7:0] & B[7:0] exchanged internally
DATA_RB=”1” R[7:0]→B[7:0](internally) B[7:0]→R[7:0](internally)
DATA_RB=”0” R[7:0]→R[7:0](internally) B[7:0]→B[7:0](internally) (default)</td></tr>
<tr><td>GRB</td><td>I
(VDDIO)</td><td colspan="3">Global reset. Active low, Internal pull high</td></tr>
<tr><td>LVR_EN</td><td>I
(VDDIO)</td><td colspan="3">Low voltage reset enable. Active high. Internal pull high.</td></tr>
<tr><td>DISP</td><td>I
(VDDIO)</td><td colspan="3">Display control / standby mode selection.
DISP = “Low” : Standby; (Default)
DISP = “High” : Normal display</td></tr>
<tr><td colspan="4">Source / Gate Driver</td></tr>
<tr><td>S1~S720</td><td>O</td><td colspan="3">Source driver output signals</td></tr>
<tr><td>G1~G544</td><td>O</td><td colspan="3">Gate driver output signals</td></tr>
<tr><td colspan="4">DC/DC Converter</td></tr>
<tr><td>DRV</td><td>O</td><td colspan="3">Power transistor gate signal for the boost converter</td></tr>
<tr><td>FB</td><td>I</td><td colspan="3">Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold can be selected by register setting, usually 0.6V (default).</td></tr>
<tr><td colspan="4">VCOM Generator</td></tr>
<tr><td>VCOM</td><td>O</td><td colspan="3">Frame polarity output for VCOM. Swing between VCOMH and VCOML.</td></tr>
<tr><td>VCOMH</td><td>C</td><td colspan="3">Power supply for VCOM high level output.</td></tr>
<tr><td>VCOML</td><td>C</td><td colspan="3">Power supply for VCOM low level output.</td></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>VDD</td><td>P</td><td colspan="3">Power supply for digital circuit</td></tr>
<tr><td>GND</td><td>P</td><td colspan="3">Ground pin for digital circuit</td></tr>
<tr><td>PVDD</td><td>P</td><td colspan="3">Power supply for charge pump circuit</td></tr>
<tr><td>PGND</td><td>P</td><td colspan="3">Ground pin for charge pump circuit</td></tr>
<tr><td>AGND</td><td>P</td><td colspan="3">Ground for analog circuit</td></tr>
<tr><td>VDDIO</td><td>P</td><td colspan="3">Power supply for digital interface I/O pins</td></tr>
<tr><td>V_OTP</td><td>P</td><td colspan="3">Power input pin for customer OTP.</td></tr>
</table>

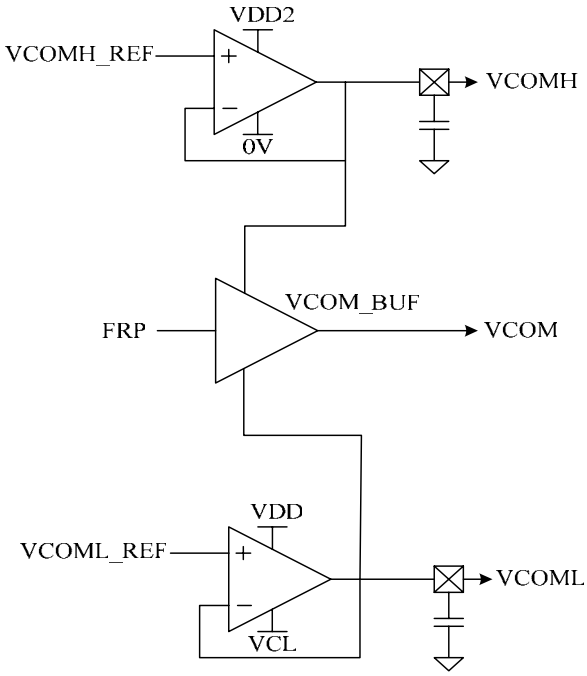
V[1:10]	C	Capacitor connect pin for internal charge pump. Refer to the illustration of power application circuit.
VDD_18	C	Power setting capacitor connect pin
VDD2	C	Power setting capacitor connect pins
VDDA	C	Power setting capacitor connect pins
VCL	C	Power setting capacitor connect pins
VGH	C	Power setting capacitor connect pins. Positive power supply for gate driver output.
VGL	C	Power setting capacitor connect pins. Negative power supply for gate driver output.
Others		
TEST[0:34]	T	Test pins for OriseTech internal testing only. User should leave it open.
TEST_S[0:2]	T	Test pins for OriseTech internal testing only. Internal pull low. User should leave it open or connect it to “low”.
COMPASS_L[0:1]	S	Internal left pass line for COM signal between input and output pins
COMPASS_R[0:1]	S	Internal right pass line for COM signal between input and output pins

Classification of TYPE:

I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, S: short pin, T: test pin, M: mark, C: capacitor pin

6. POWER APPLICATION CIRCUIT





Component	Recommended Value	Voltage Proof
C2	1uF	>10V
C9,C11	1uF	>16V
C3,C4,C7	2.2uF	>6V
C10,C12	2.2uF	>16V
C5,C6,C8,C13,C14	4.7uF	>10V

Remarks:

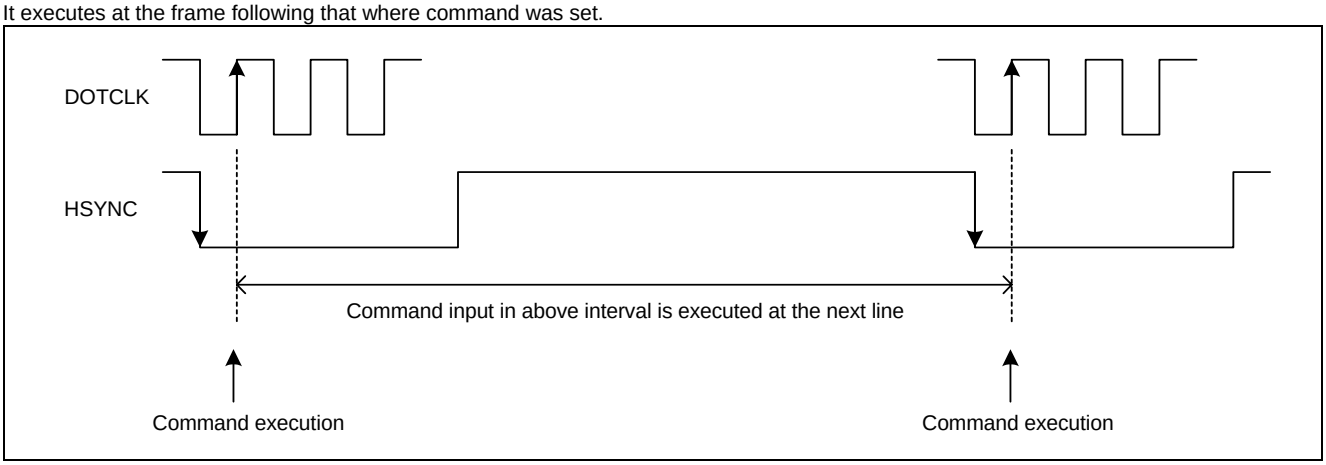
1. PVDD is connected to VDD externally
2. VDD2 is pumped from VDD by charge pump1:
   When VDD=2.5V, PWR_SEL=L, VDD2=3x VDD
   When VDD=3.3V, PWR_SEL=H, VDD2=2x VDD

7. REGISTER BANK

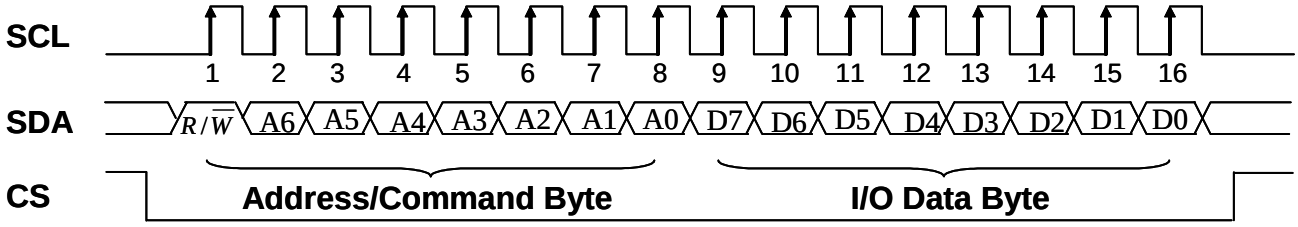
7.1 The executing time of Registers

Registers are not executed immediately after accepting a command through serial interface.

It executes at the frame following that where command was set.



Serial Control Timing Chart



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

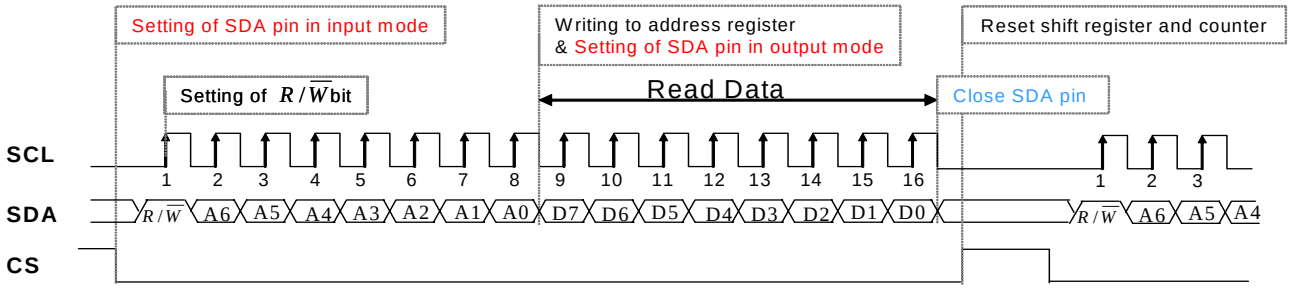
e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before the rising edge of CS pulse are valid data.

f. Serial block operates with the SCL clock

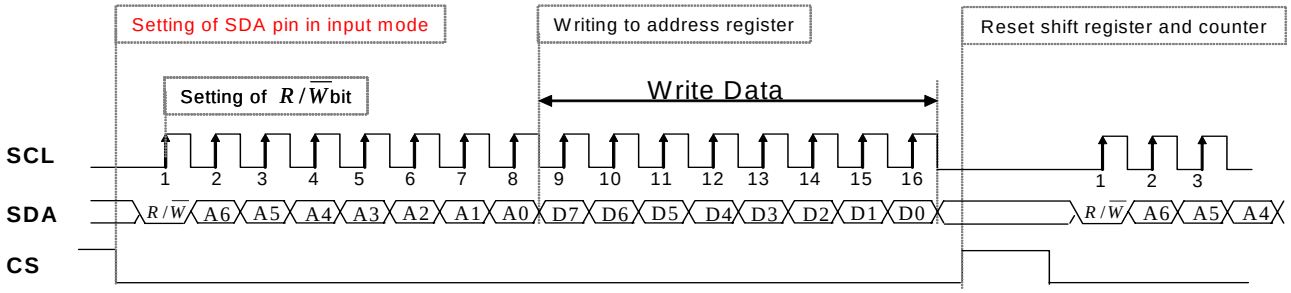
g. Serial data can be accepted in the power save mode.

$R/\overline{W}$: Establishes the read mode when set to '1', and the write mode when set to '0'.

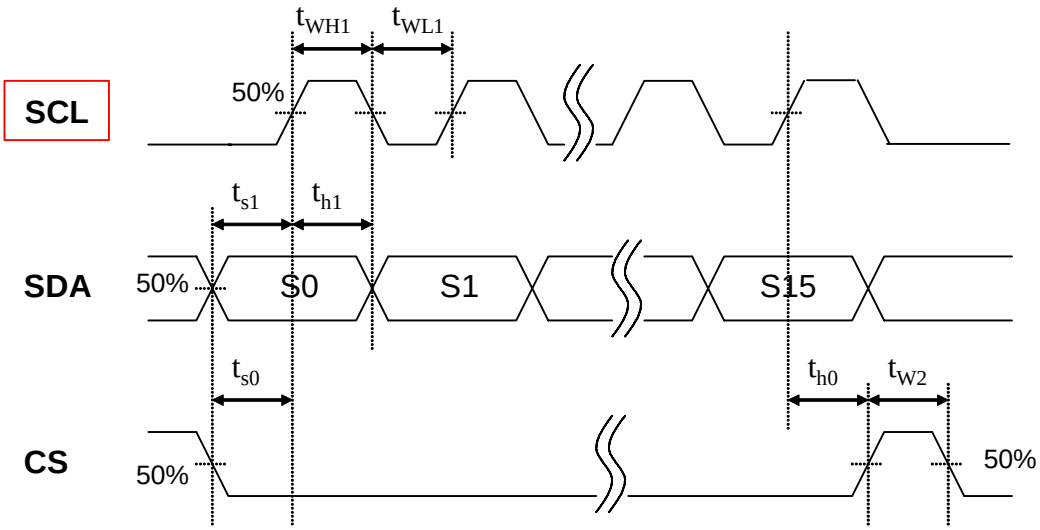
Read Mode:



Write Mode:



7.2 Serial Control Timing Chart



Item	Symbol	Min.	Typ.	Max.	Unit
CS input setup time	t_{S0}	50			ns
Serial data input setup time	t_{S1}	50			ns
CS input hold time	t_{h0}	50			ns
Serial data input hold time	t_{h1}	50			ns
SCL pulse high width	t_{WH1}	50			ns
SCL pulse low width	t_{WL1}	50			ns
CS pulse high width	t_{W2}	400			ns

7.3 Register summary

Register	Register Adress								Register Data (Default)							
	$R/\overline{W}$	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	X	VDIR(1)	HDIR(1)	X	X	X	X	X
R1	0	0	0	0	0	0	0	1	X	X	X	X	GRB(1)	SHDB2(1)	SHDB1(0)	DISP(0)
R2	0	0	0	0	0	0	1	0	CONTRAST(40h)							
R3	0	0	0	0	0	0	1	1	X	SUB-CONTRAST_R(40h)						
R4	0	0	0	0	0	1	0	0	X	SUB-CONTRAST_B(40h)						
R5	0	0	0	0	0	1	0	1	BRIGHTNESS(40h)							
R6	0	0	0	0	0	1	1	0	X	SUB-BRIGHTNESS_R(40h)						
R7	0	0	0	0	0	1	1	1	X	SUB-BRIGHTNESS_B(40h)						
R8	0	0	0	0	1	0	0	0	HSYNC_BLANKING(2Bh)							
R9	0	0	0	0	1	0	0	1	VDPOL(1)	HDPOL(1)	VSYNC BLANKING(0Ch)					
R10	0	0	0	0	1	0	1	0	SYNC(0)	DCLKpol	CP3_FREQ(10)		CP2_FREQ(10)		CP1_FREQ(10)	
R11	0	0	0	0	1	0	1	1	LED_CURRENT(00)		BL_DRV(00)		DRV_FERQ(00)		PFM_DUTY(10)	
R12	0	0	0	0	1	1	0	0	LED_ON_CYCLE(0111)				LED_ON_RATIO(1111)			
R13	0	0	0	0	1	1	0	1	X	OP(1XX)			X	X	X	X
R14	0	0	0	0	1	1	1	0	X	X	X	X	LC_TYPE(00)		X	X
R15	0	0	0	0	1	1	1	1	X	X	VGH_SEL(1XX)			VGL_SEL(1XX)		
R16	0	0	0	1	0	0	0	0	X	X		X	INVERSION(1)	X	X	X
R17	0	0	0	1	0	0	0	1	X	VCOMH(4Dh)						
R18	0	0	0	1	0	0	1	0	X	VCOML(1Bh)						

X: reversed, please set to '0'

Note:

1. When GRB is low, all registers reset to default values
2. Serial commands are executed at next VSYNC signal

7.4 Register description

7.4.1 R0: Direction setting

Address	Bit	Description		Default
00000000	[6:5]	B6(VDIR)	Vertical shift direction setting	0_1100110b
		B5(HDIR)	Horizontal shift direction setting	

B6	Function(VDIR)
0	Shift from down to up, Last line = G1<G2<-…<G543<G544 = First line U2D = 0, D2U = 1
1	Shift from up to down, First line = G1->G2->…->G543->G544 = Last line **(Default)** U2D = 1, D2U = 0

B5	Function(HDIR)
0	Shift from right to left, Last data = S1<S2<-…<S719<S720 = First data
1	Shift from left to right, First data = S1->S2->…->S719->S720 = Last data **(Default)**

7.4.2 R1: GRB、SHDB2、SHDB1、DISP

Address	Bit	Description		Default
00000001	[6:0]	B3(GRB)	Register reset setting	0_1001100b
		B2(SHDB2)	Charge pump shutdown setting	
		B1(SHDB1)	DC-DC converter shutdown setting	
		B0(DISP)	Display control / standby mode setting	

B3	Function(GRB)
0	Reset all registers to default value
1	Normal operation (Default)

B2	Function(SHDB2)
0	Charge pump is off
1	Charge pump is controlled by DISP and power on/off sequence (Default)

B1	Function(SHDB1)
0	DC-DC converter is off (Default)
1	DC-DC converter is controlled by DISP and power on/off sequence

B0	Function(DISP)
0	Standby mode (Display OFF). Timing control, driver, and DC/DC converter are off and all output are

	High-Z.. (Default)
1	Normal operation (Display ON)

7.4.3 R2: CONSTRAST

Address	Bit	Description	Default
00000010	[7:0]	RGB contrast level setting, the gain changes (1/64) / bit	01000000b

B7-B0	Contrast Gain
00h	0
40h	1(default)
FFh	3.984

7.4.4 R3: SUB-CONTRAST_R

Address	Bit	Description	Default
00000011	[6:0]	R sub-contrast level setting, the gain changes (1/256) / bit	0_1000000b

B6-B0	Sub-Contrast_R Gain
00h	0.75
40h	1(default)
7Fh	1.246

7.4.5 R4: SUB-CONTRAST_B

Address	Bit	Description	Default
00000100	[6:0]	B sub-contrast level setting, the gain changes (1/256) / bit	0_1000000b

B6-B0	Sub-Contrast_B Gain
00h	0.75
40h	1(default)
7Fh	1.246

7.4.6 R5: BRIGHTNESS

Address	Bit	Description	Default
00000101	[7:0]	RGB bright level setting, setting accuracy : 1 step / bit	01000000b

B7-B0	Brightness Setting
00h	Dark (-64)
40h	Center (0)(Default)
FFh	Bright (+191)

7.4.7 R6: SUB- BRIGHTNESS _R

Address	Bit	Description	Default
00000110	[6:0]	R sub-brightness level setting, setting accuracy : 1 step / bit	0_1000000b

B6-B0	Sub-Contrast_R Gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)

7.4.8 R7: SUB- BRIGHTNESS _B

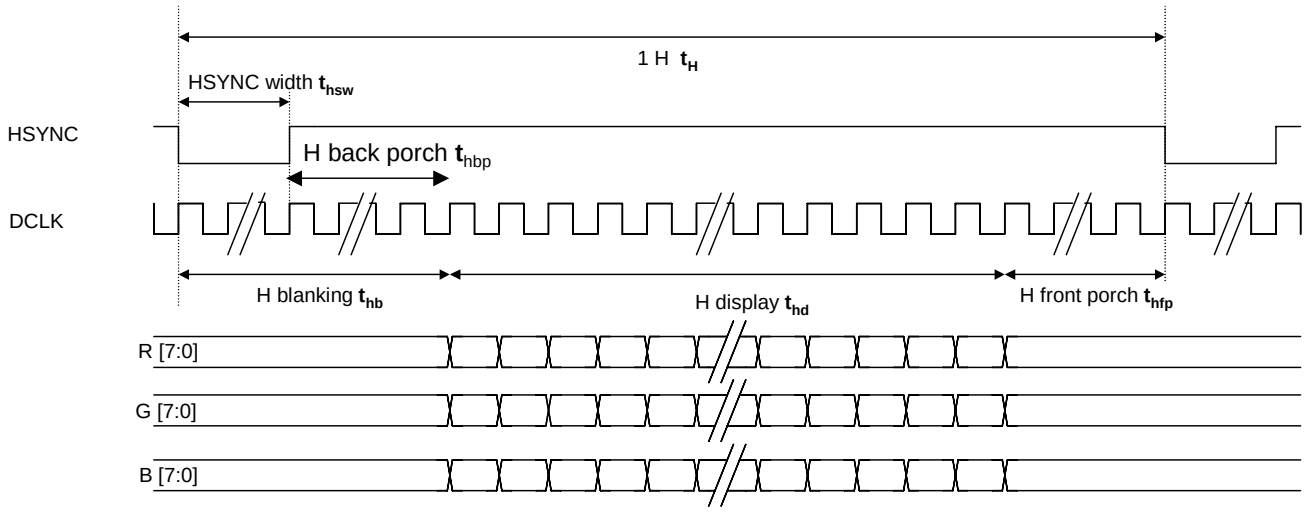
Address	Bit	Description	Default
00000111	[6:0]	B sub-brightness level setting, setting accuracy : 1 step / bit	0_1000000b

B6-B0	Sub-Contrast_B Gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)

7.4.9 R8: HSYNC BLANKING

Address	Bit	Description	Default
00001000	[7:0]	Horizontal blanking setting	00101011b

B7-B0	HBLK(Unit: DCLK)
00h	0
2Bh	43(default)
FFh	255



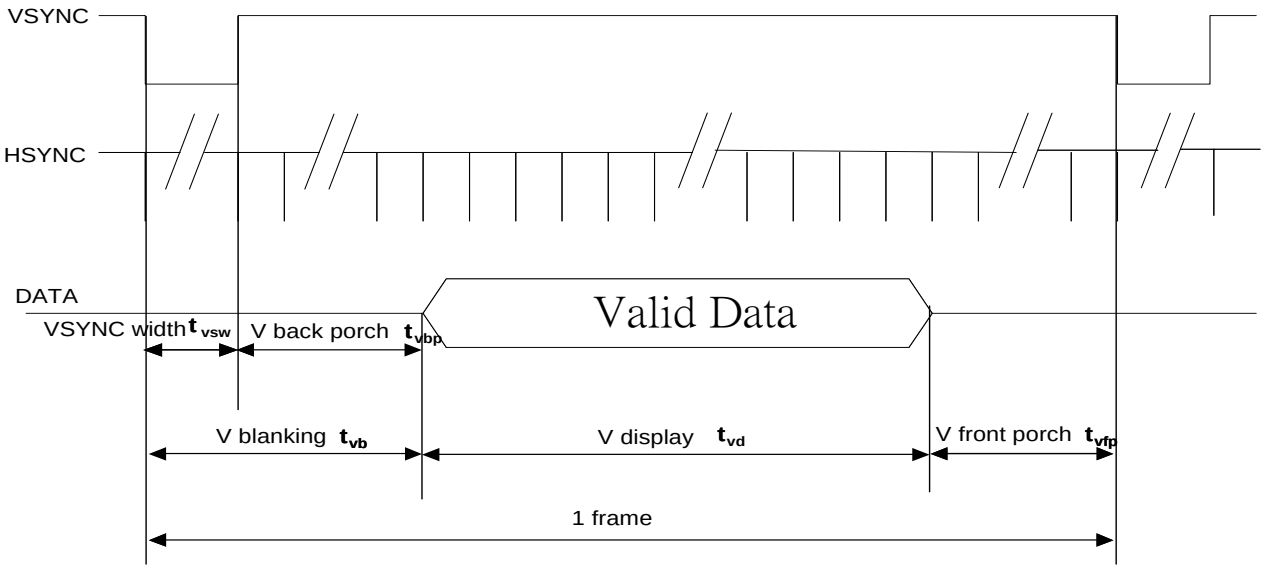
7.4.10 R9: HSYNC BLANKING

Address	Bit	Description		Default
00001001	[7:0]	B7(VDPOL)	VSYNC polarity selection	11001100b
		B6(HDPOL)	HSYNC polarity selection	
		B5-B0(VYSNC_BLANKING)	Vertical blanking setting	

B7	Function(VDPOL)
0	Positive polarity
1	Negative polarity (Default)

B6	Function(HDPOL)
0	Positive polarity
1	Negative polarity (Default)

B5-B0	VSYNC BLANKING (Unit: H)
00h	0
0Ch	12(default)
3Fh	63



7.4.11 R10: SYNC、DCLKPOL、CP3_FREQ、CP2_FREQ、CP1_FREQ

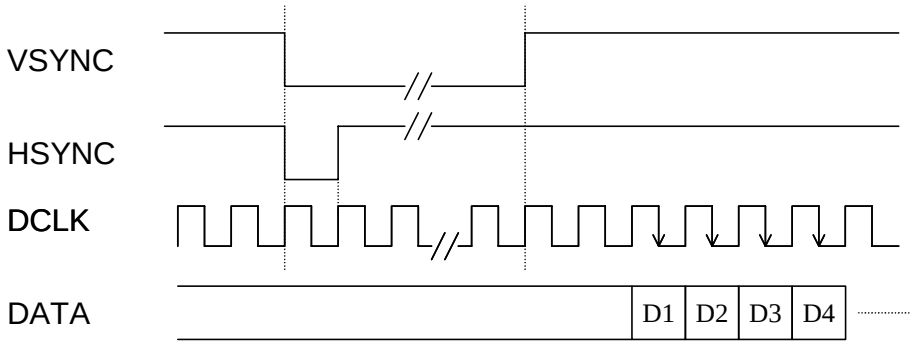
Address	Bit	Description		Default
00001010	[7:0]	B7(SYNC)	SYNC and SYNC-DE mode selection	01xx1010b
		B6(DCLKPOL)	DCLK polarity selection	
		B5-B4(PUMP3 Frequency)	Charge Pump3 Frequency Setting	
		B3-B2(PUMP2 Frequency)	Charge Pump2 Frequency Setting	
		B1-B0(PUMP1 Frequency)	Charge Pump1 Frequency Setting	

B7	Function(SYNC)
0	SYNC-DE Mode(Default)
1	SYNC Mode

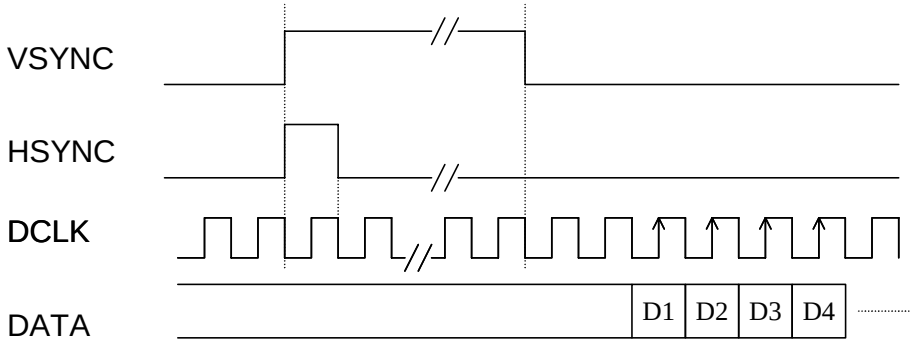
B6	Function(DCLKPOL)
0	Positive polarity
1	Negative polarity (Default)

Note: When the command is sent to ASIC, it will be executed immediately.

• HDPOL=1, VDPOL=1, CLKPOL=1



• HDPOL=0, VDPOL=0, CLKPOL=0



The Relationship of HDPOL/VDPOL/CLKPOL

CP1,2,3_FREQ		Function(Charge Pump Frequency)
0	0	1/2*HSYNC Freq.
0	1	1*HSYNC Freq.
1	0	2*HSYNC Freq.
1	1	4*HSYNC Freq.

7.4.12 R11: LED_CURRENT、BL_DRV、DRV_FREQ、PFM_DUTY

Address	Bit	Description		Default
00001011	[7:0]	B7-B6(LED_CURRENT)	Adjust LED current	00000010b
		B5-B4(BL_DRV)	Backlight driving capability setting	
		B3-B2(DRV_FREQ)	DRV signal frequency setting	
		B1-B0(PFM_DUTY)	PFM duty cycle selection for back light power converter	

		DC2DC Feedback Voltage(V)
B7	B6	Function(LED_CURRENT)
0	0	0.6 V (default, 20mA)
0	1	0.75V (25mA)
1	0	0.45V (15mA)
1	1	0.3V (10mA)

B5	B4	Function(BL_DRV)
0	0	Normal capability (Default)
0	1	4 times the Normal capability
1	0	8 times the Normal capability
1	1	12 times the Normal capability

B3	B2	Function(DRV_FREQ)
0	0	DCLK / 32 (Default)
0	1	DCLK / 64
1	0	DCLK / 128
1	1	DCLK / 256

B3	B2	Function(PFM_DUTY)	NOTE
0	0	50 %	16/32
0	1	60 %	19/32
1	0	65 % (Default)	21/32
1	1	70 %	22/32

7.4.13 R12: LED_ON_CYCLE、LED_ON_RATIO

Address	Bit	Description		Default
00001001	[7:0]	B7-B4 (LED_ON_CYCLE)	Set the cycle of enable signal , and we can use it to adjust brightness of the LEDs.	01111111b
		B3-B0 (LED_ON_RATIO)	Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs	

B7	B6	B5	B4	Function (LED_ON_CYCLE)
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8 (Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

B3	B2	B1	B0	Function (LED_ON_RATIO)
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16(Default)

7.4.14 R13: OP

Address	Bit	Description		Default
00001011	[6:4]	B6-B4(OP)	Source output driving capability selection	0_1001100b

			DAC output driving capacity
B6	B5	B4	Function(OP)
0	0	0	-25%
0	0	1	Normal (satisfy output settling time 2.6us)
0	1	0	+25% (satisfy output settling time 2.2us)
0	1	1	+50%
1	0	0	Controlled by input pin OP0, OP1 (Default)

7.4.15 R14: LC_TYPE

Address	Bit	Description		Default
00100000	[6:0]	B3-B2(LC_TYPE)	LC type selection	10010000b

B3	B2	Function(LC_TYPE)
0	0	Setting by input pins TN_TYPE and MVA_TN (Default)
0	1	TN_Mode1 and Lower VCOM Power
1	0	MVA and Higher VCOM Power
1	1	TN_Mode2 and Higher VCOM Power

7.4.16 R15:VGH_SEL、VGL_SEL

Address	Bit	Description		Default
00001111	[5:0]	B5-B3(VGH_SEL)	VGH_SEL : VGH voltage Selection	011b
		B2-B0(VGL_SEL)	VGL voltage Selection	

			Unit: V
B5	B4	B3	Function(VGH_SEL)
0	0	0	|VGL|+2
0	0	1	|VGL|+3
0	1	0	|VGL|+4
0	1	1	|VGL|+5 (Default)
1	X	X	Auto Select by LC_TYPE

			Unit: V
B2	B1	B0	Function(VGL_SEL)
0	0	0	-7
0	0	1	-8
0	1	0	-9
0	1	1	-10 (Default)
1	X	X	Auto Select by LC_TYPE

7.4.17 R16: INVERSION

Address	Bit	Description		Default
01001111	[3]	B3 (INVERSION)	Line/Frame inversion control bit	0_0000111b

B3	Function (INVERSION)
0	Frame inversion
1	Line inversion (Default)

7.4.18 R17: VCOMH

Address	Bit	Description		Default
00010001	[6:0]	B6-B0(VCOMH)	VCOMH level adjustment	1001101b

B6-B0	VCOMH level(Unit: V)
00h	2.46
1Bh	3
4Dh	4(default)
7Fh	5

7.4.19 R18: VCOML

Address	Bit	Description		Default
00010010	[6:0]	B6-B0(VCOML)	VCOMH level adjustment	0011011b

B6-B0	VCOML level(Unit: V)
00h	-0.46
1Bh	-1(default)
4Dh	-2
7Fh	-3

8. ELECTRICAL SPECIFICATIONS

8.1 Absolute Maximum Ratings

Rating	Symbol	Value			Unit
Digital supply voltage	VDDIO	-0.3	to	+4.5	V
Power Supply for Pump	VDD	-0.3	to	+4.5	V
Analog supply voltage	VDD2	-0.3	to	+7.0	V
Storage temperature	T_{STG}	-55	to	100	℃
Operating temperature	T_A	-30	to	85	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

8.2 DC Characteristics (VDDIO=1.8V, VDD = 3.0V, AVDD = 5.5V, AGND = 0V, T_A = -20℃ to 80℃)

8.2.1 For digital circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Digital Supply Voltage	V_{DDIO}	1.65	1.8	V_{DD}	V	
Power Supply for Pump	V_{DD}	3	3.3	3.6	V	PWR_SEL=H
	V_{DD}	2.25	2.5	3	V	PWR_SEL=L
Input Leakage Current	I_L	-1.0	-	1.0	uA	
Pull High/Low Resistor	R_P	-	940K	-	ohm	
Digital Stand-by current	I_{DST}	-	5.0	20	uA	DCLK stopped, Output Hi-Z
Digital operation current	I_{CC}	-	4	-	mA	DCLK = 9MHz

8.2.2 For analog circuit

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Analog Supply Voltage	VDD2		6		V	
VCOM Supply Voltage	FRP	-3	-	5	V	
Output Voltage Deviation	V_{OD}	-	±20	±35	mV	V_O = 0.15V ~ 0.5V, 3.45V~3.8V
		-	±15	±20		V_O = 0.5V ~ 3.45V
Output Dynamic Range	V_{DR}	0.2	-	3.8		MVA / TN4.5 Mode
		0.15		3.15		TN3.2 Mode
Analog Operation Current	I_{DD}	-	5.0	-	mA	Without panel loading
Analog Standby Current	I_{AST}	-	-	20	uA	
Feed Back Voltage	V_{FB}	0.57	0.6	0.63	V	Setting by Register (Default)
		0.71	0.75	0.79	V	Setting by Register
		0.43	0.45	0.47	V	Setting by Register
		0.28	0.30	0.32	V	Setting by Register
DRV Output Voltage	V_{DRV}	0	-	VDD	V	
DRV Drive Current	I_{DRV}	-	-	20	mA	VDD = 3.0V, FB = 0.60V (Default)
		-	-	25	mA	VDD = 3.0V, FB = 0.75V
		-	-	15	mA	VDD = 3.0V, FB = 0.45V
		-	-	10	mA	VDD = 3.0V, FB = 0.30V

8.3 Output Signal Characteristics

8.3.1 Output Voltage

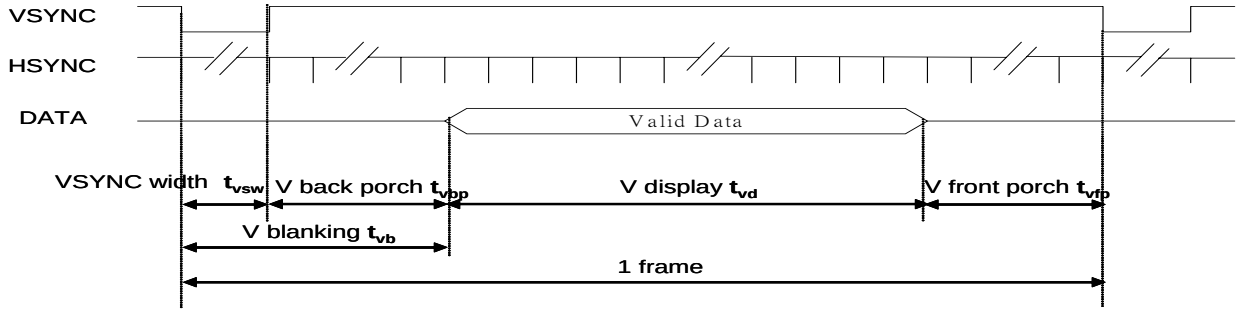
Item	Symbol	Applicable pins	Conditions	Min.	Typ.	Max.	Unit
Output voltage 1	V_{GH}	VGH	MVA				V
			TN1		15		
			TN2				
Output voltage 2	V_{GL}	VGL	MVA				V
			TN1		-10		
			TN2				

8.4 INPUT TIMING

8.4.1 480XRGBX272 Vertical Timing

Item	Min.	Typ.	Max.	Unit
V display t_{VD}		272		H
V blanking t_{VB}		12		
V front porch t_{VFP}		3		
VSYNC width t_{VSW}		10		
1 frame		287		

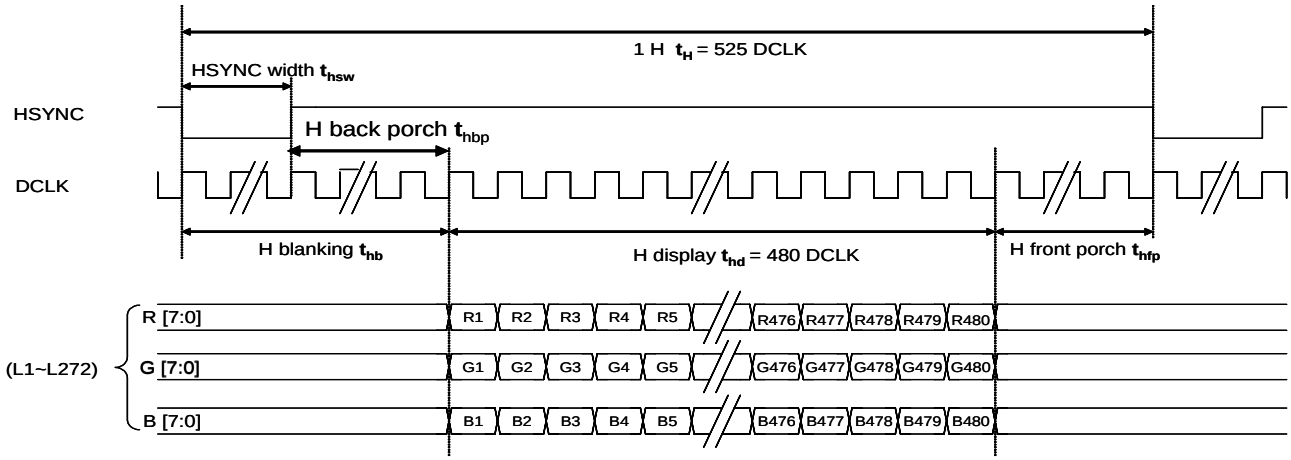
NOTE: t_{VB} is programmable



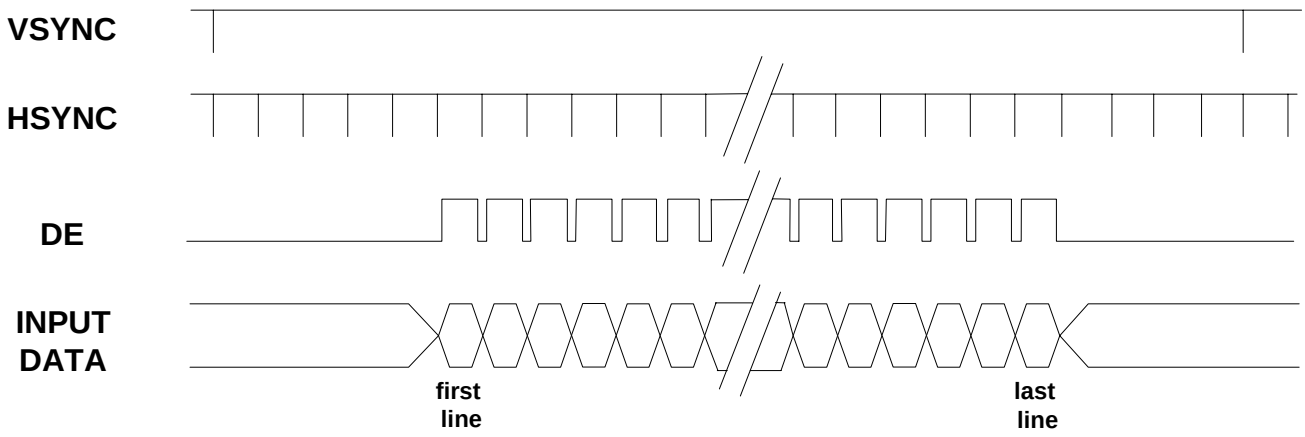
8.4.2 480XRGBX272 Horizontal Timing

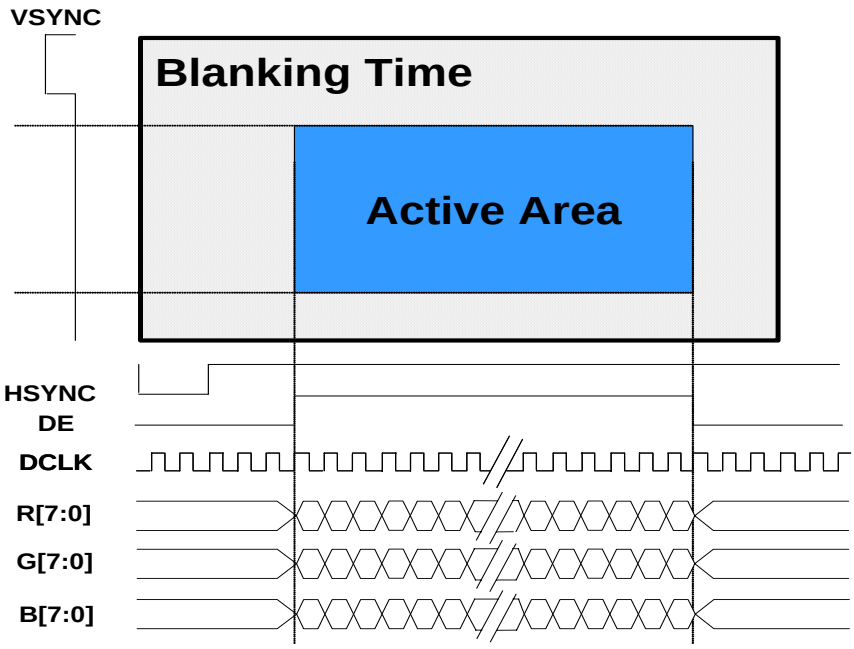
640x240 mode	Min	Min	Max	UNIT
H display t_{hd}		480		DCLK
1 H t_H		576		
H blanking t_{hb} (*)		88		
H front porch t_{hfp}		8		
HSYNC width t_{hsw}		41		
Frequency		9.0		MHz

NOTE: t_{hb} is programmable



8.5 SYNC-DE Mode





9. OUTPUT TIMING

TBD

10. POWER ON/OFF SEQUENCE

The power sequence is shown in fig. power sequence.

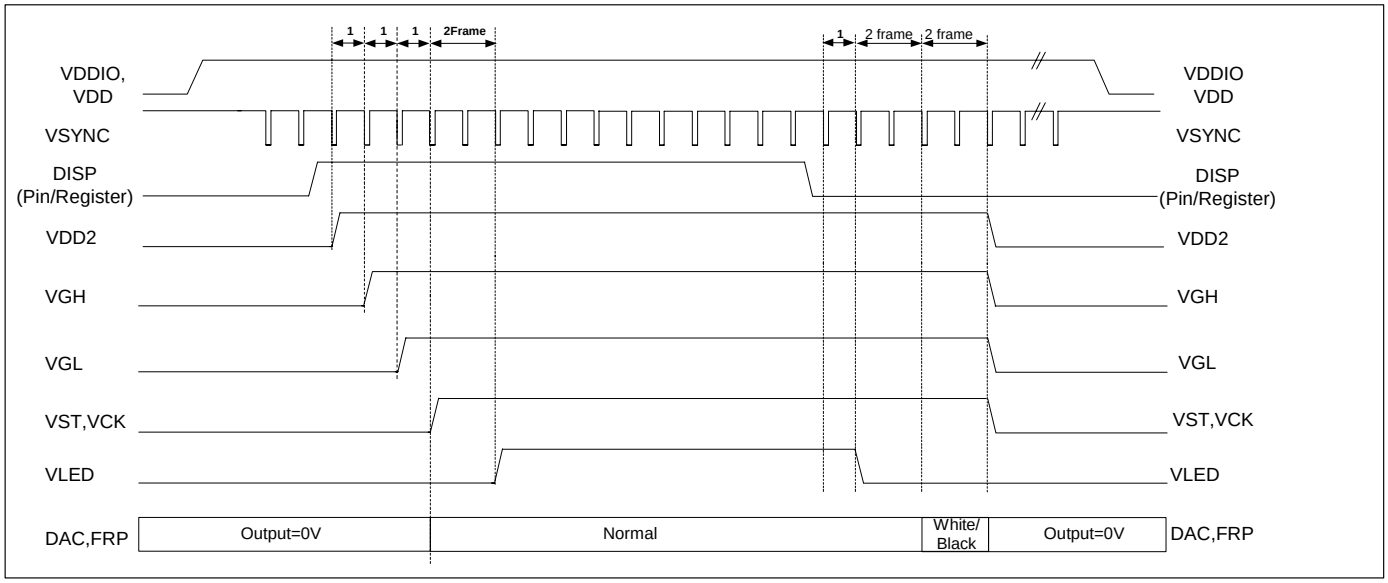


Fig. Power Sequence

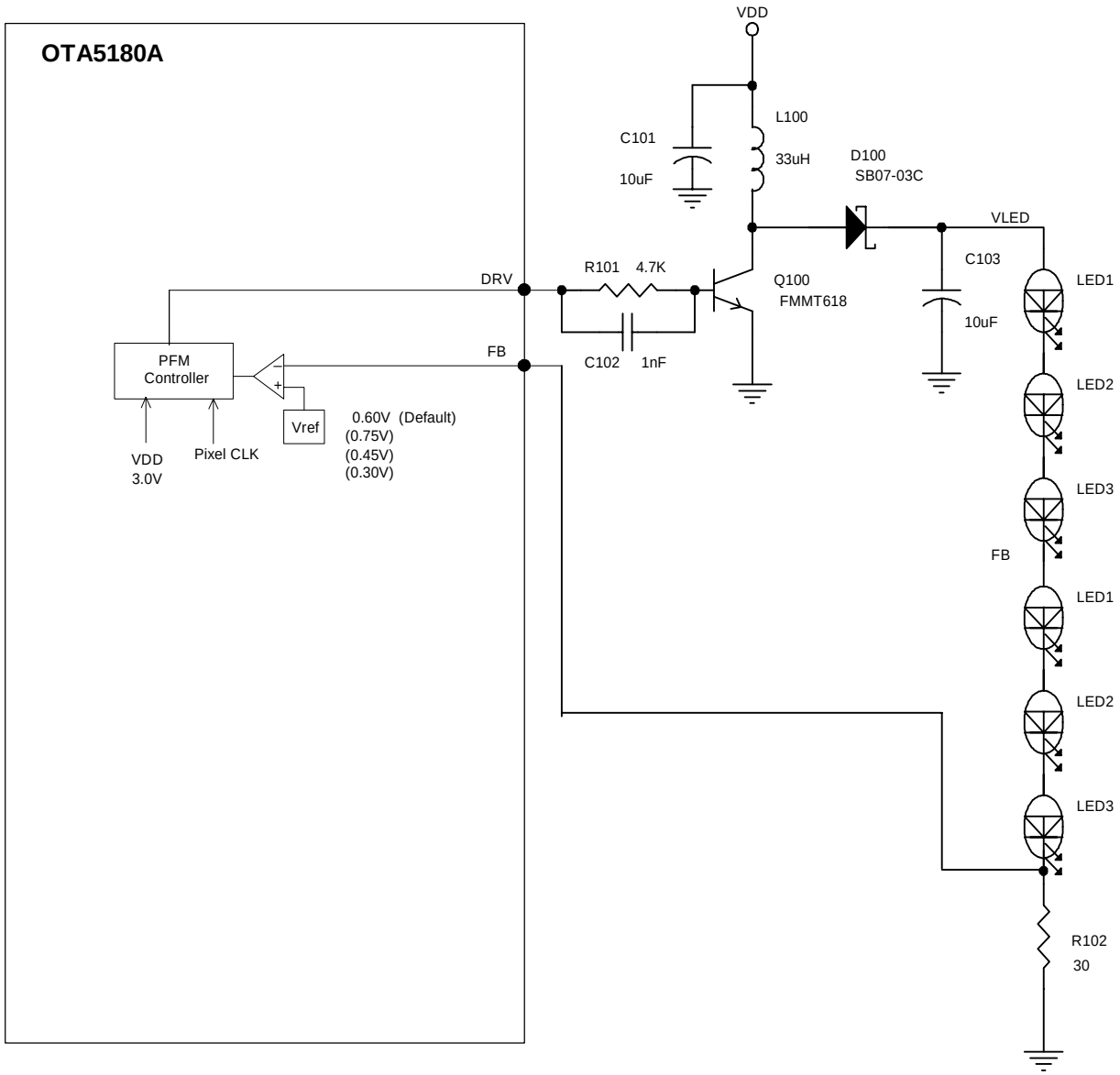
Note:

a. When MVA mode (Normally black LC) is applied, it needs to send **black pattern** to discharge the pixel.

b. When TN_MODE2 or TN_MODE1 mode (Normally white LC) is applied, it needs to send **white pattern** to discharge the pixel.

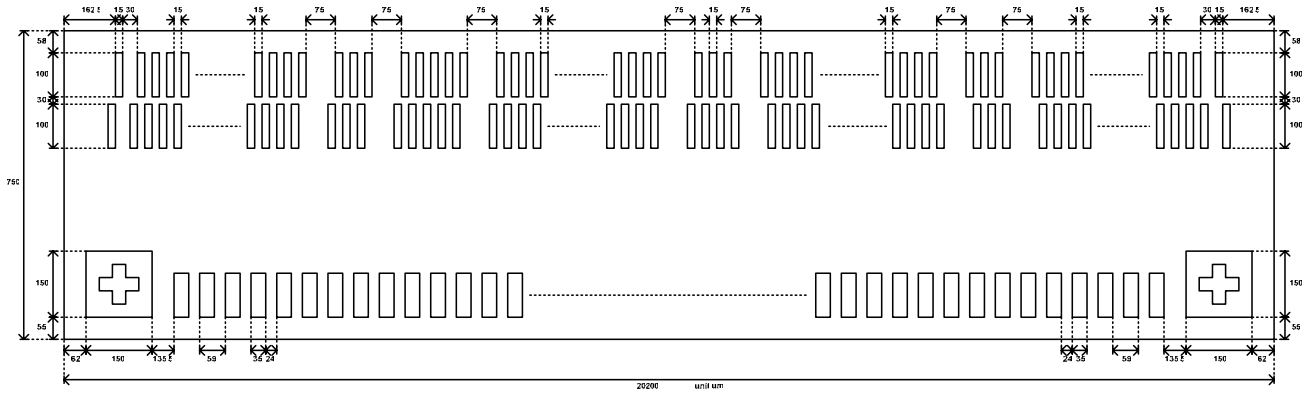
11. APPLICATION CIRCUIT for DC-DC Converter

The PWM controller provides high efficient boost power supply circuit control that generates the power of LED back light and Level Shift. The boost converter uses a Power transistor to provide maximum efficiency and to minimize the number of external components. A precision 0.6V reference voltage with ±0.01V Hysteresis is included.



12. CHIP INFORMATION

12.1 PAD Assignment



Note: Dimension includes scribe line

12.2 PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	20200	750	μm
Chip thickness	-	300 ± 25		
Pad pitch	Input Pads	59	-	
	Output Pads	15	-	
Pad size	Input Pads	35	100	
	Output Pads	15	100	

Note: Chip size includes scribe line.

12.3 Bump Characteristic

Item	Standard	Note
Bump Hardness	75HV	± 25HV
Bump Height	15μm	± 3μm
Co-planarity (in Chip)	R≦ 2μm	R : Max-Min
Roughness (in Bump)	R≦ 2μm	R : Max-Min
Bump Size	“X” ± 3μm x “Y” ± 3μm	X/Y: bump size
Shear Force	>4.5g/mil^2	

12.4 Pad Locations

TBD

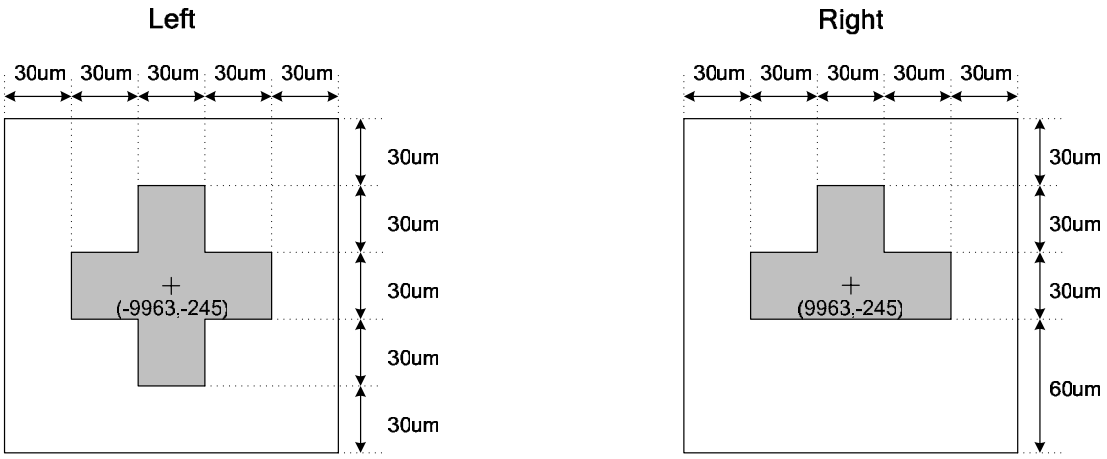
12.5 Align Key Locations

--Alignment Mark coordinate

Left (-9963,-245)

Right (9963,-245)

--Alignment Mark size



13. COG PRODUCTS MANUFACTURING GUIDELINES

13.1 Purpose:

The purpose of this specification is to identify ACF bonding process, so that customers can use properly ACF and Chip during the assembly.

13.2 Scope:

ACF bonding process

13.3 Noun definition

13.3.1 COG: Chip on Glass

13.3.2 ACF (Anisotropic Cunductive Film): .ACF is a functional adhesive tape which is able to connect (conductivity, adhesion, insulation) multiterminals in one time.

13.3.3 CTE: Coefficient of thermal expansion

13.4 Responsibility unity:

ORISETECH Quality Assurance unity

13.5 Contents:

13.5.1 Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

IPC-A-610: Acceptability of Electronic Assemblies

13.5.2 ACF Characteristics:

Three factors to achieve the connection: Temperature, Pressure, Time.

13.5.3 ACF process :

To use Low Temperature and Low stress ACF is recommended for thin chip as 300 um.

Warp issues may happen if customers do not use Low Temperature and Low stress ACF for long chip .And warp issues may induce chip broken after ACF bonding for the CTE mismatch of Glass and ACF and Chip.

To use 3um ACF is recommended for BUMP space is less than 13um.

To use Low temperature and long time bonding is recommended if delamination happens in edge of chip.

For fine pitch and thin chip (300 um) products, customer should review ACF bonding condition with ACF maker.

13.6 References:

*IPC:

http://www.ipc.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

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15. REVISION HISTORY

Date	Revision #	Description	Page
APR. 01, 2008	0.2	1. Change default setting of SYNC pin and “SYNC” function register	6, 12, 18
		2. Update section 6	9
		3. Update section 12.2 and 12.3.	30
		4. Update section 12.5	31
		5. Add COG PRODUCTS MANUFACTURING GUIDELINES.	32
MAR. 31, 2008	0.1	Original	33