NOVATEK

NT7605

Single-chip 20C X 2L Dot-Matrix LCD Controller / Driver

Features

- Internal LCD drivers
  - 16 common signal drivers
  - 100 segment signal drivers
- Maximum display dimensions
  - 20 characters * 2 lines or
  - 40 characters * 1 line
- Interfaces with 4-bit or 8-bit MPU
- Versatile display functions provided on chip:
  - Display Clear, Cursor Home, Display ON/OFF, Cursor ON/OFF, Character Blinking, Cursor Shift, and Display Shift
- Three duty factors, selected by PROGRAM:
  - 1/8, 1/11, and 1/16
- Displays Data RAM (DD RAM): 80 X 8 bits (Displays up to 80 characters)
- Character Generator RAM (CG RAM):
  - 64 X 8 bits for general data,
  - 8 5 X 8 programmable dot patterns, or
  - 4 5 X 10 programmable dot patterns
- Low voltage reset
- ITO option for A-type and B-type LCD waveform
- 2 kinds of LCD pads sequence
- Character Generator ROM (CG ROM):
  2 kinds of CG ROM sizes:
  - 192 characters:
    - 160 5 X 8 dot patterns
    - 32 5 X 10 dot patterns
  - 240 characters:
    - 192 5 X 8 dot patterns
    - 48 5 X 10 dot patterns

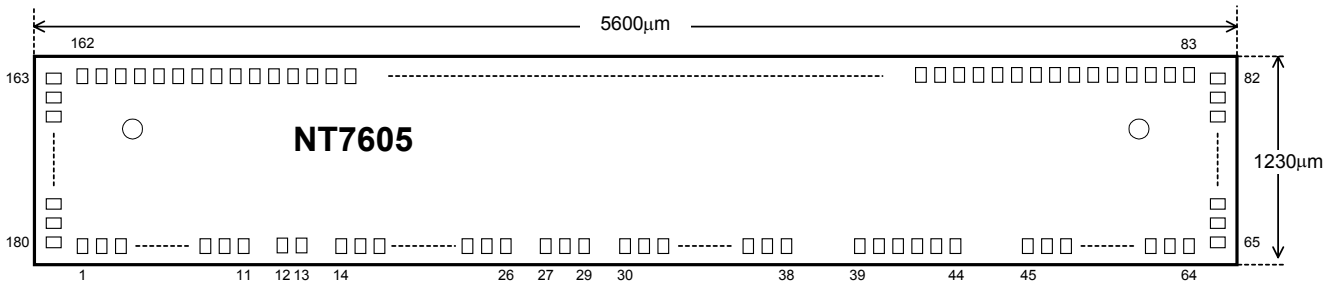
  Custom CG ROM is also available
- Built-in power-on reset function
- Logic power supply: 2.8V ~ 5.5V
- LCD driver power supply: V1 ~ V5
  divided by Built-in LCD power division resister.
- Two oscillator operations
  (Freq. = 500KHz - 540KHz):
  - Built-in RC oscillation
  - External clock
- CMOS Process
- Available in COG FORM

General Description

The NT7605 is a dot matrix LCD controller and driver LSI that can operate with either a 4-bit or an 8-bit microprocessor (MPU). NT7605 receives control character codes from the MPU, stores them in an internal RAM (up to 80 characters), transforms each character code into a 5 X 7, 5 X 8, or 5 X 10 dot matrix character pattern, and then displays the codes on the LCD panel. The built-in Character Generator ROM consists of 256 different character patterns.

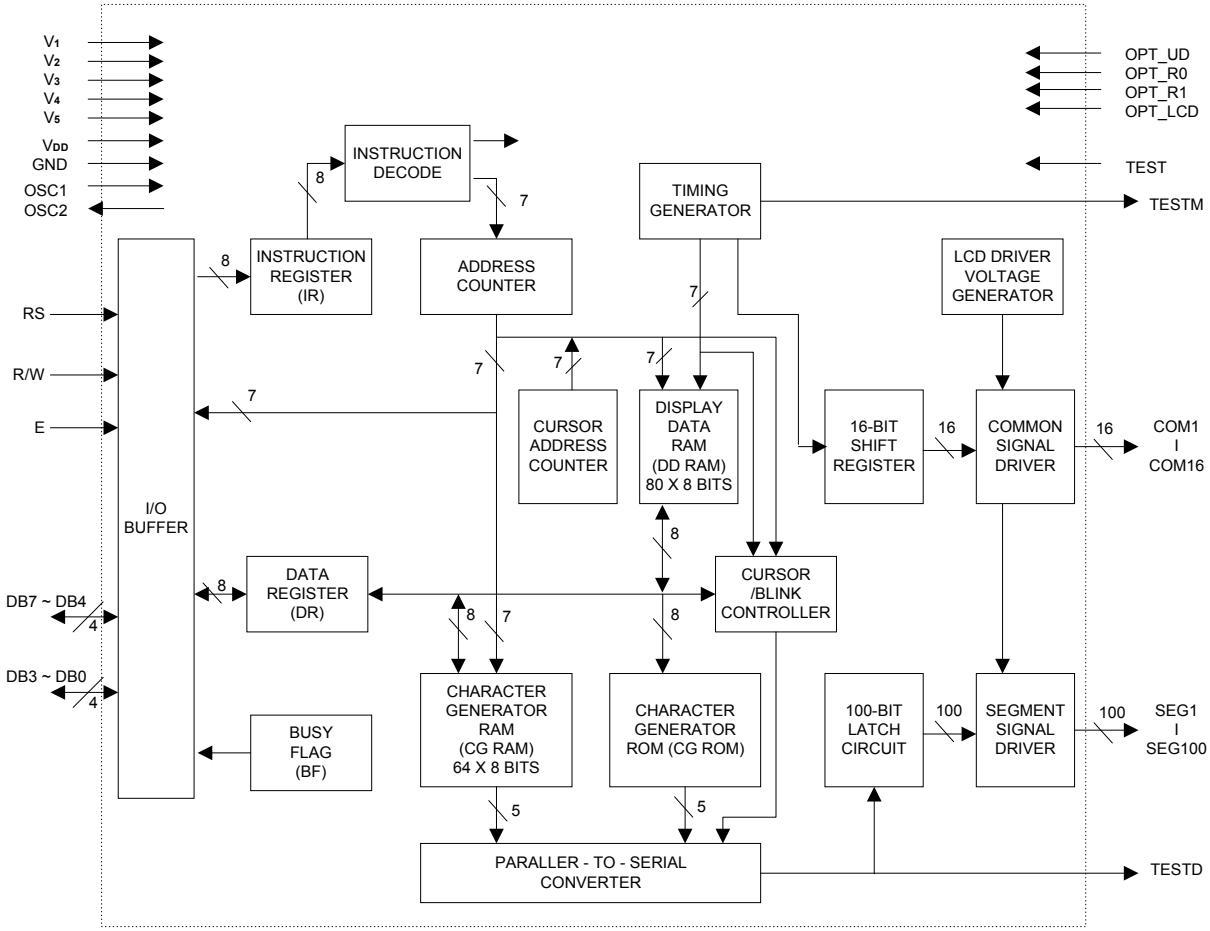
The NT7605 also contains Character Generator RAM where the user can store 8 different character patterns at run time. These memory features make the character display flexible. NT7605 also provides many display instructions to achieve versatile LCD display functions. The NT7605 is fabricated on a single LSI chip using the CMOS process, resulting in very low power requirements.

Pad Configuration



Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	1230	5600	μm
Pad pitch	1 - 180	65		

Block Diagram



Pad Description (Total 180 pads for COG type)

Pad No.	Designation	I/O	External Connection	Description
1	TEST	I	Test pin	Test pin internally pull-down. (No connect for user)
2	TESTM	O	Test output	LCD driver clock output. (No connect for user)
3 - 11	GND	P	Power supply	GND: 0V
12	OSC1	I		For external clock operation, clock inputs to OSC1
13	OSC2	O		Clock output
14, 15	V1	P	Power supply	Power supply for LCD driver. $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq GND$
16, 17	V2	P	Power supply	Power supply for LCD driver
18, 19	V3	P	Power supply	Power supply for LCD driver
20, 21	V4	P	Power supply	Power supply for LCD driver
22 - 26	V5	P	Power supply	Power supply for LCD driver
27, 29	OPT_R0, OPT_R1	I	ITO Option	The built-in bias resister select: OPT_R1, OPT_R0: No ITO = 1. ITO on = 0 1, 1: 2.2KΩ; 1, 0: 4KΩ; 0, 1: 6.8KΩ; 0, 0: No built-in bias resister:
30 - 38	V_{DD}	P	Power supply	V_{DD}: +5V
30, 40	RS	I	MPU	Register select signal 0: Instruction register (write), Busy flag, address counter (read) 1: Data register (write, read)
41, 42	R/W	I	MPU	Read/Write control signal 0: Write 1: Read
43, 44	E	I	MPU	Read/Write start signal (Schmitt trigger input)
45, 46	DB0	I/O	MPU	Lower 4 tri-state bi-directional data bus for transmitting data between MPU and NT7605. Not used during 4-bit operation
47, 48	DB1			
49, 50	DB2			
51, 52	DB3			
53, 54	DB4	I/O	MPU	Higher 4 tri-state bi-directional data bus for transmitting data between MPU and NT7605. DB7 is also used as busy flag
55, 56	DB5			
57, 58	DB6			
59, 60	DB7			
61	OPT_LCD	I	ITO Option	No ITO. (Option = 1): B-Type waveform ITO On. (Option = 0): A-Type waveform
63	OPT_UD	I	ITO Option	No ITO. (Option = 1): COM1→COM8→COM9→COM16; SEG1→SEG100 ITO On. (Option = 0): COM9→COM16→COM1→ COM8; SEG100→SEG1
64	TESTD	O	Test output	Test data output. (No connect for user)
180 - 173	COM1 - 8	O	LCD panel	Common signal output pins, for place on the upper glass (OPT_UD=1)
65 - 72	COM9 - 16	O	LCD panel	
65 - 72	COM1 - 8	O	LCD panel	Common signal output pins, for place on the lower glass (OPT_UD=0)
180 - 173	COM9 - 16	O	LCD panel	
172 - 73	SEG1 - 100	O	LCD panel	Segment signal output pins (OPT_UD = 1)
73 - 172	SEG1 - 100	O	LCD panel	Segment signal output pins (OPT_UD = 0)
28, 62	GND_OUT	P		GND output pin, use for pull-down ITO option

Functional Description

The NT7605 is a dot-matrix LCD controller and driver LSI. It operates with either a 4-bit or an 8-bit microprocessor (MPU). The NT7605 receives both instructions and data from the MPU. Some instructions set operation modes, such as the function mode, data entry mode, and display mode; as well as some control LCD display functions, such as clear display, restore display, shift display as well as controlling the cursor. Other instructions include reading and writing both data and addresses. All the instructions allow users convenient and powerful functions to control the LCD dot-matrix displays.

Data is written into and read from the Data Display RAM (DD RAM) or the Character Generator RAM (CG RAM). As display character codes, the data stored in the DD RAM decodes a set of dot-matrix character patterns that are built into the Character Generator ROM (CG ROM). The CG ROM, with many character patterns (up to 256 patterns), defines the character pattern fonts. The NT7605 regularly scans the character patterns through the segment drivers. The CG RAM stores character pattern fonts at run time if users intend to show character patterns that are not defined in the CG ROM. This feature makes character display flexible. Other unused bytes can be used as general-purpose data storage.

The LCD driver circuit consists of 16 common signal drivers and 100 segment signal drivers allowing a variety of application configurations to be implemented.

Character Generator ROM (CG ROM)

The character generator ROM generates LCD dot character patterns from the 8-bit character pattern codes. The NT7605 provides 2 CG ROM configurations:

1. 192 Characters:

The CG ROM contains 160 5 X 8 dot character patterns and 32 5 X 10 dot character patterns. The relation between the character codes and character patterns is shown in Table 1. The character codes from 00H to 0FH are used to get character patterns from the CG RAM. The character codes 10H to 1FH, 80H to 9FH and 20H all map to null character patterns. The character codes from E0H to FFH are assigned to generate 5 X 10 dot character patterns, and other codes are used to generate 5x8 dot character patterns.

2. 240 Characters:

The CG ROM contains 192 5 X 8 dot character patterns and 48 5 X 10 dot character patterns. The relation between the character codes and character patterns is shown in Table 2. The character codes from 00H to 0FH are used to get character patterns from the CG RAM. The character codes from 10H to 1FH and from E0H to FFH are assigned to generate 5 X 10 dot character patterns, and other codes to generate 5 X 8 dot character patterns. Only one null character pattern exists in this type. Note that the underlined cursor, displayed on the 8th duty may be obscure if the 8th row of a dot character pattern is coded. We recommend that users display the cursor in the blinking mode if coding 5 X 8 dot character patterns is their custom CG ROM.

Custom character patterns are available by mask-programming the ROM. For convenience of character pattern development, NOVATEK has developed a user-friendly editor program for the NT7605 to help determine the character patterns users prefer. By executing the program on the computer, users can easily create and modify their character patterns. By transferring the resulting files generated by the program through a modem or some other communication method, the user and NOVATEK can establish a reliable, fast link for programming the CG ROM.

Absolute Maximum Ratings*

Power Supply Voltage (V_{DD}) . . . . . -0.3V to +7.0V
Power Supply Voltage (V_1 to V_5) . . . . . GND to V_{DD} + 0.3V
Input Voltage (V_I) . . . . . -0.3V to V_{DD} + 0.3V
Operating Temperature (T_{OPR}) . . . . . -20°C to +70°C
Storage Temperature (T_{STG}) . . . . . -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

- All voltage values are referenced to GND = 0V
- V_1 to V_5, must maintain $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5 \geq$ GND

DC Electrical Characteristics (V_{DD} = 4.5V~5.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin
V_{DD}	Operating Voltage	4.5	5.0	5.5	V		
V_{IH1}	"H" Level Input Voltage	0.8 V_{DD}	-	V_{DD}	V		DB0 - DB7, RS, R/W, E, OSC1
V_{IL1}	"L" Level Input Voltage	-0.3	-	0.2 V_{DD}	V		
V_{OH1}	"H" Level Output Voltage	V_{DD} - 0.6	-	-	V	I_{OH} = -1.2mA	DB0 - DB7 (CMOS)
V_{OL1}	"L" Level Output Voltage	-	-	GND + 0.6	V	I_{OL} = 1.2mA	
V_{COMD}	Driver Voltage Descending (COM)	-	-	0.3	V	I_D = 5μA	COM1 - 16
V_{SEGD}	Driver Voltage Descending (SEG)	-	-	0.3	V	I_D = 5μA	SEG1 - 100
I_{IL}	Input Leakage Current	-1	-	1	μA	V_{IN} = 0 to V_{DD}	
-I_P	Pull-up MOS Current	50	125	250	μA	V_{DD} = 5V	RS, R/W, DB0 - DB7
I_{OP}	Power Supply Current	-	1	1.5	mA	Rf oscillation, from external clock V_{DD} = 5V, f_{OSC} = f_{CP} = 540KHz, include LCD bias current	V_{DD}
External Clock Operation							
f_{CP}	External Clock Operating Frequency	380	540	750	KHz		
t_{DUTY}	External Clock Duty Cycle	45	50	55	%		
t_{RCP}	External Clock Rise Time	0.1	-	0.5	μs		
t_{FCP}	External Clock Fall Time	0.1	-	0.5	μs		
Internal Clock Operation (Built-in RC Oscillator)							
f_{OSC}	Oscillator Frequency	380	540	750	KHz	Rf = 50KΩ (reference only) V_{DD} = 2 .8V ~ 5.5V	
V_{LCD}	LCD Driving Voltage	3.0	-	V_{DD}	V	V_{DD} - V_5	

DC Electrical Characteristics (continued) (V_{DD} = 2.8V~4.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions	Applicable Pin
V_{DD}	Operating Voltage	2.8	3.0	4.5	V		
V_{IH1}	"H" Level Input Voltage	0.8 V_{DD}	-	V_{DD}	V		DB0 - DB7, RS, R/W, E, OSC1
V_{IL1}	"L" Level Input Voltage	-0.3	-	0.2 V_{DD}	V		
V_{OH1}	"H" Level Output Voltage	V_{DD} - 0.4	-	-	V	I_{OH} = -0.8mA	DB0 - DB7 (CMOS)
V_{OL1}	"L" Level Output Voltage	-	-	GND + 0.4	V	I_{OL} = 0.8mA	
V_{COMD}	Driver Voltage Descending (COM)	-	-	0.3	V	I_D = 5μA	COM1 - 16
V_{SEGD}	Driver Voltage Descending (SEG)	-	-	0.3	V	I_D = 5μA	SEG1 - 100
I_{IL}	Input Leakage Current	-1	-	1	μA	V_{IN} = 0 to V_{DD}	
-I_P	Pull-up MOS Current	30	75	150	μA	V_{DD} = 3V	RS, R/W, DB0 - DB7
I_{OP}	Supply Current Power Supply Current	-	1	1.5	mA	Rf oscillation, from external clock V_{DD} = 3V, f_{OSC} = f_{CP} = 540KHz, include LCD bias current	V_{DD}
External Clock Operation							
f_{CP}	External Clock Operating Frequency	380	540	750	KHz		
t_{DUTY}	External Clock Duty Cycle	45	50	55	%		
t_{RCP}	External Clock Rise Time	0.1	-	0.5	μs		
t_{FCP}	External Clock Fall Time	0.1	-	0.5	μs		
Internal Clock Operation (Built-in RC Oscillator)							
f_{OSC}	Oscillator Frequency	380	540	750	KHz	Rf = 50KΩ (reference only) V_{DD} = 2 .8V ~ 5.5V	
V_{LCD}	LCD Driving Voltage	2.5	-	V_{DD}	V	V_{DD} - V_5	

AC Characteristics

Read Cycle (V_{DD} = 4.5V~5.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 1
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 1
t_{RE}, t_{FE}	Enable Rise/Fall Time	-	-	25	ns	Figure 1
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 1
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 1
t_{RD}	Read Data Output Delay	-	-	190	ns	Figure 1
t_{DHR}	Read Data Hold Time	20	-	-	ns	Figure 1

Write Cycle (V_{DD} = 4.5V~5.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 2
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 2
t_{RE}, t_{FE}	Enable Rise/Fall Time	-	-	25	ns	Figure 2
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 2
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 2
t_{DS}	Data Output Delay	100	-	-	ns	Figure 2
t_{DHW}	Data Hold Time	10	-	-	ns	Figure 2

Notes: 1: 8-bit operation mode
2: 4-bit operation mode

Power Supply Conditions Using Internal Reset Circuit

(V_{DD} = 4.5V~5.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{RON}	Power Supply Rise Time	0.1	-	10	ms	Figure 3
t_{OFF}	Power Supply OFF Time	1	-	-	ms	Figure 3

AC Characteristics (continued)

Read Cycle (V_{DD} = 2.8V~4.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 1
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 1
t_{RE}, t_{FE}	Enable Rise/Fall Time	-	-	25	ns	Figure 1
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 1
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 1
t_{RD}	Read Data Output Delay	-	-	190	ns	Figure 1
t_{DHR}	Read Data Hold Time	20	-	-	ns	Figure 1

Write Cycle (V_{DD} = 2.8V~4.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CYCE}	Enable Cycle Time	500	-	-	ns	Figure 2
t_{WHE}	Enable "H" Level Pulse Width	300	-	-	ns	Figure 2
t_{RE}, t_{FE}	Enable Rise/Fall Time	-	-	25	ns	Figure 2
t_{AS}	RS, R/W Setup Time	60[1]	-	-	ns	Figure 2
		100[2]				
t_{AH}	RS, R/W Address Hold Time	10	-	-	ns	Figure 2
t_{DS}	Data Output Delay	150	-	-	ns	Figure 2
t_{DHW}	Data Hold Time	10	-	-	ns	Figure 2

Notes: 1: 8-bit operation mode
2: 4-bit operation mode

Power Supply Conditions Using Internal Reset Circuit

(V_{DD} = 2.8V~4.5V, GND = 0V, T_A = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{RON}	Power Supply Rise Time	0.1	-	10	ms	Figure 3
t_{OFF}	Power Supply OFF Time	1	-	-	ms	Figure 3

Timing Waveforms

Read Operation

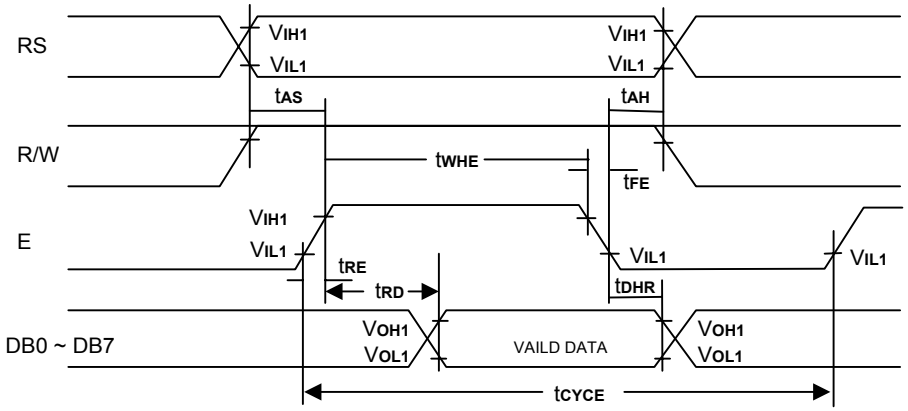


Figure 1. Bus Read Operation Sequence
(Reading out data from NT7605 to MPU)

Write Operation

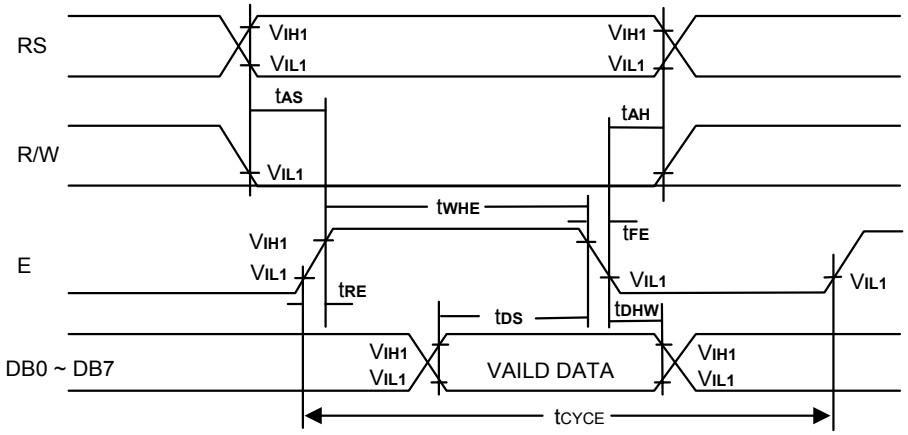


Figure 2. Bus Write Operation Sequence
(Writing data from MPU to NT7605)

Interface Signals with Segment Driver LSI

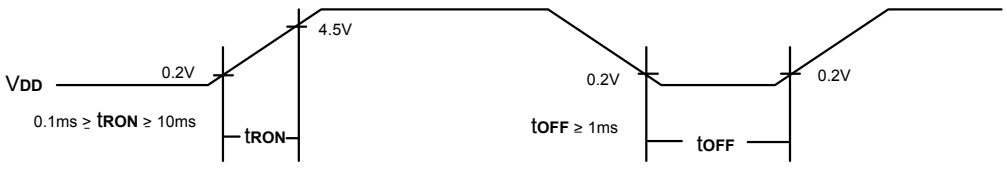
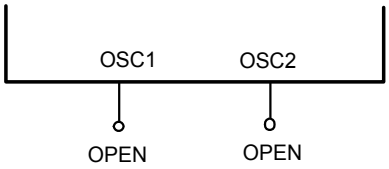


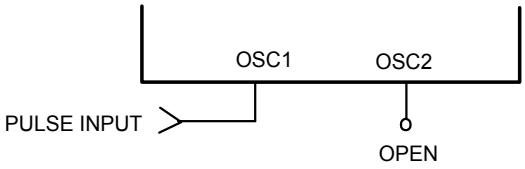
Figure 3. t_{OFF} stipulates the time of power off for instantaneous Power supply to or when power supply repeats ON and OFF.

Note 1: The NT7605 has two clock options:

A. Internal Oscillator (Built-in RC)



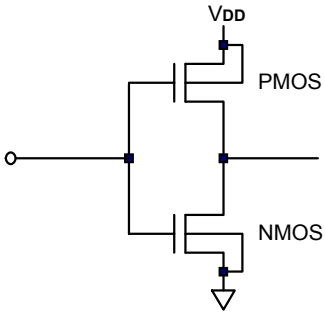
B. External Clock Operation



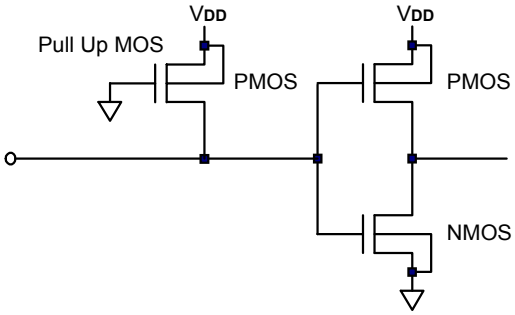
Note 2: Input/Output Terminals:

A. Input Terminal

Applicable Terminal: E (No Pull Up MOS)

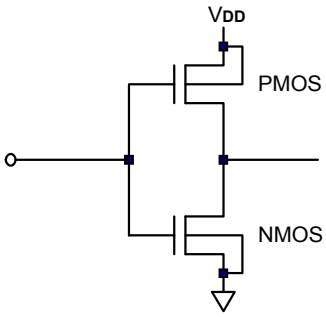


Applicable Terminal: RS, R/W (with Pull Up MOS)



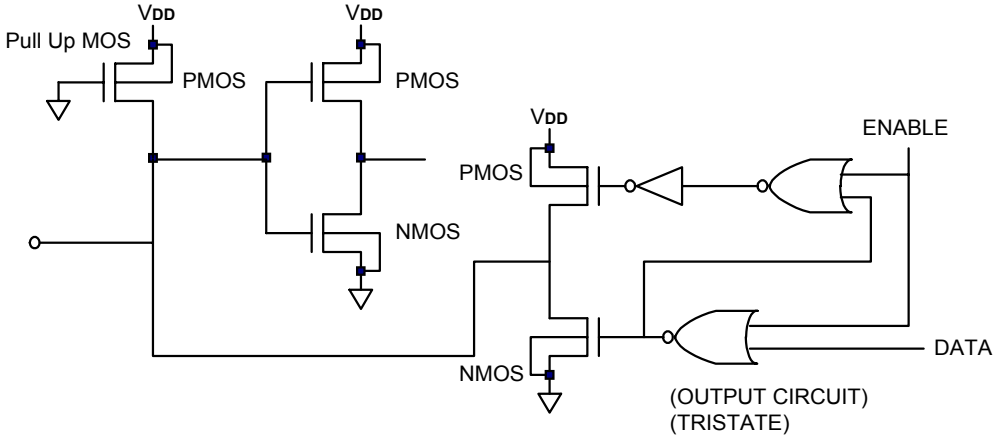
B. Output Terminal

Applicable Terminal: TESTM



C. I/O Terminal

Applicable Terminal: DB0 to DB7



Note 3: ITO Options:

Set Option = 0: Place ITO on the Option Pad.
Set Option = 1: No ITO on the Option Pad.

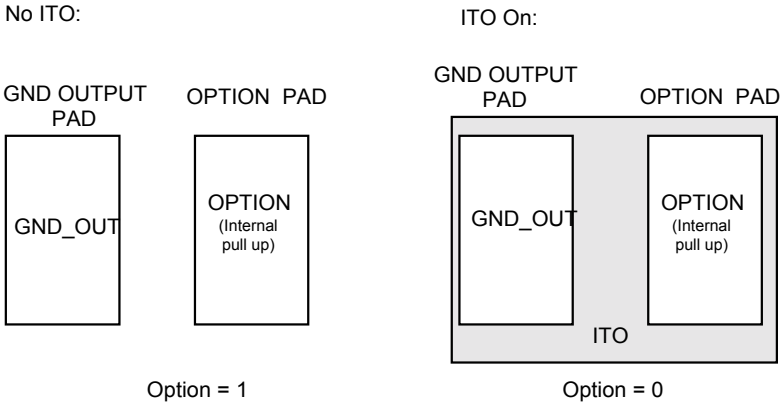


Table 1. NT7605H-BDT01 Correspondence between Character Codes and Character Patterns (NOVATEK Standard 192 Character CG ROM)

Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (1)															
1	CG RAM (2)															
2	CG RAM (3)															
3	CG RAM (4)															
4	CG RAM (5)															
5	CG RAM (6)															
6	CG RAM (7)															
7	CG RAM (8)															
8	CG RAM (1)															
9	CG RAM (2)															
A	CG RAM (3)															
B	CG RAM (4)															
C	CG RAM (5)															
D	CG RAM (6)															
E	CG RAM (7)															
F	CG RAM (8)															

Instruction Set

Instruction	Code										Function	Execution time (max) (fosc = 540KHz)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display Clear	0	0	0	0	0	0	0	0	0	1	Clear entire display area, Restore display from shift, and load address counter with DD RAM address 00H	1.64ms
Display/ Cursor Home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00H	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Specify direction of cursor movement and display shift mode. This operation takes place after each data transfer (read/write)	40μs
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D) cursor (C) and blinking of character at cursor position (B)	40μs
Display/ Cursor Shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift display or move cursor	40μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Set interface data length (DL), number of the display line (N), and character font (F)	40μs
RAM Address Set	0	0	0	1	ACG						Load the address counter with a CG RAM address Subsequent data access is for CG RAM data	40μs
DD RAM Address Set	0	0	1	ADD							Load the address counter with a DD RAM address Subsequent data access is for DD RAM data	40μs
Busy Flag/ Address Counter Read	0	1	BF	AC							Read Busy Flag (BF) and contents of Address Counter (AC)	1μs
CG RAM/ DD RAM Data Write	1	0	Write data								Write data to CG RAM or DD RAM	40μs
CG RAM/ DD RAM Data Read	1	1	Read data								Read data from CG RAM or DD RAM	40μs
	I/D = 1 : Increment S = 1 : Display Shift On D = 1 : Display On C = 1 : Cursor Display On B = 1 : Cursor Blink On S/C = 1 : Shift Display R/L = 1 : Shift Right DL = 1 : 8-Bit N = 1 : Dual Line F = 1 : 5x10 dots BF = 1 : Internal Operation BF = 0 : Ready for Instruction						I/D = 0 : Decrement S/C = 0 : Move Cursor R/L = 0 : Shift Left DL = 0 : 4-Bit N = 0 : Signal Line F = 0 : 5x8 dots				DD RAM : Display Data RAM CG RAM : Character Generator RAM ACG : Character Generator RAM Address ADD : Display Data RAM Address AC : Address Counter	

Note 1: Symbol " * " signifies an insignificant bit (disregard).

Note 2: Correct input value for "N" is predetermined for each model.

Note 3: The variation of execution time depends on the change of oscillator frequency; for example:

if fOSC = 380KHz, then execution time = 40μs✕ (540KHz / 380KHz) = 57μs

Interface to LCD

(1) Character Font and Number of Lines

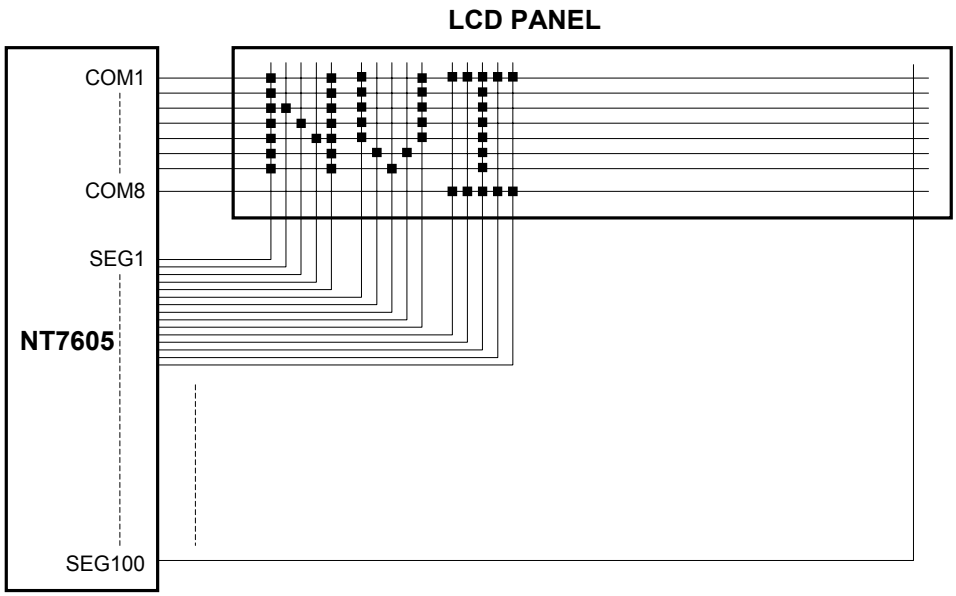
The NT7605 provides a 5 X 7 dot character font 1-line mode, a 5 X 10 dot character font 1-line mode and a 5 X 7 dot character font 2-line mode, as shown in the table below.
Three types of common signals are available as displayed in the table. The number of lines and the font type can be selected by the program.

Number of Lines	Character Font	Number of Common Signals	Duty Factor	Bias
1	5 X 7 dots + Cursor (or 5 X 8 dots)	8	1/8	1/4
1	5 X 10 dots + Cursor	11	1/11	1/4
2	5 X 7 dots + Cursor (or 5 X 8 dots)	16	1/16	1/5

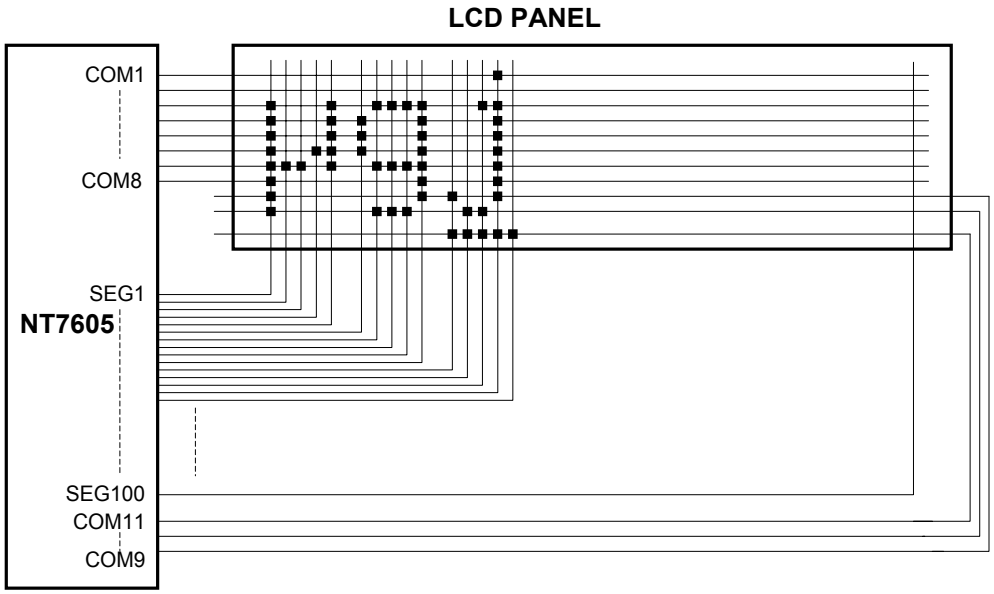
(2) Connection to LCD

The following 4 LCD connection examples show the various combinations between characters and lines.
NT7605 can directly drive the following combinations:

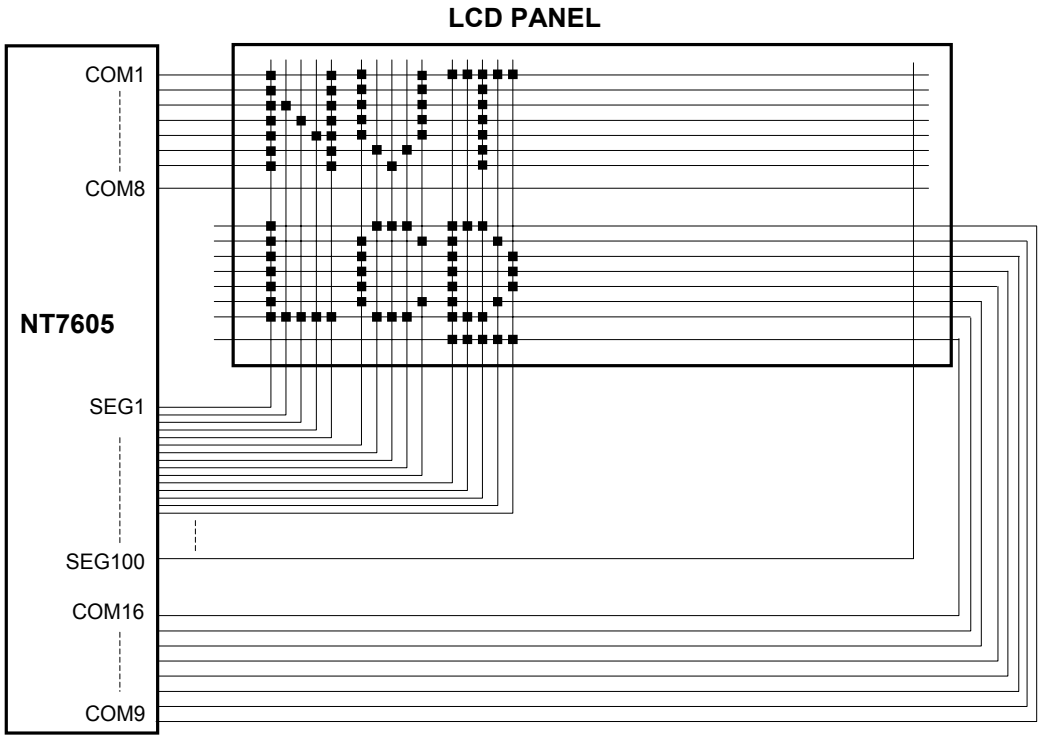
(a) 5 X 8 Font – 20 characters X 1 line (1/8 duty cycle, 1/4 bias)



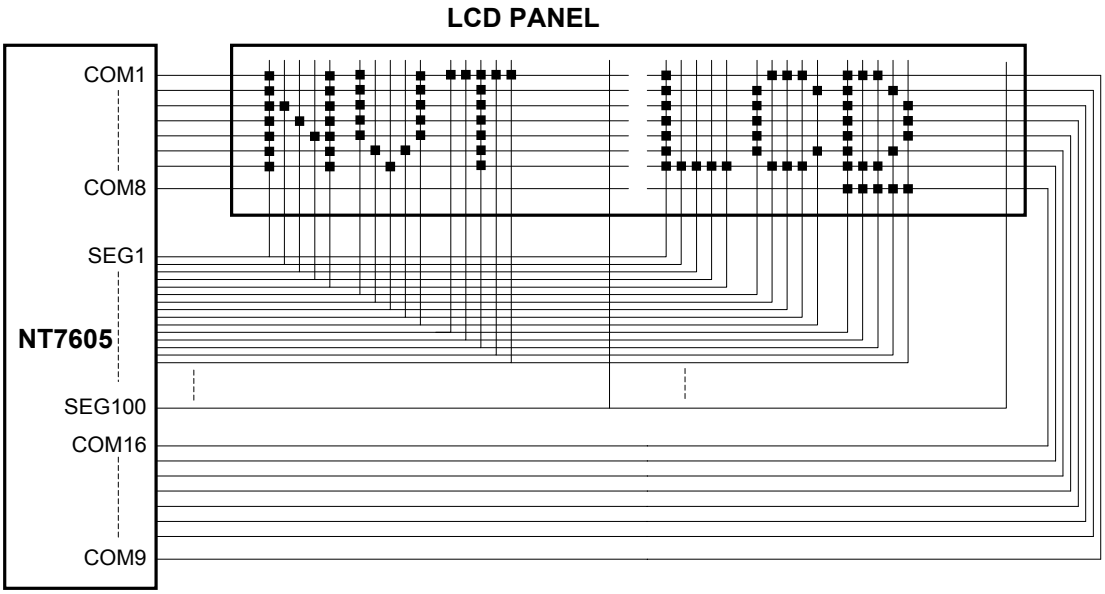
(b) 5 X 10 Font - 20 characters X 1 line (1/11 duty cycle, 1/4 bias)



(c) 5 X 8 Font - 20 characters X 2 line (1/16 duty cycle, 1/5 bias)

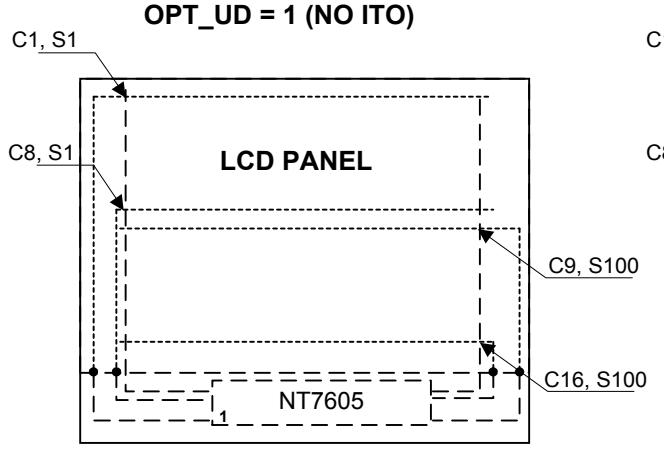


(d) 5 X 8 Font - 40 characters X 1 line (1/16 duty cycle, 1/5bias)

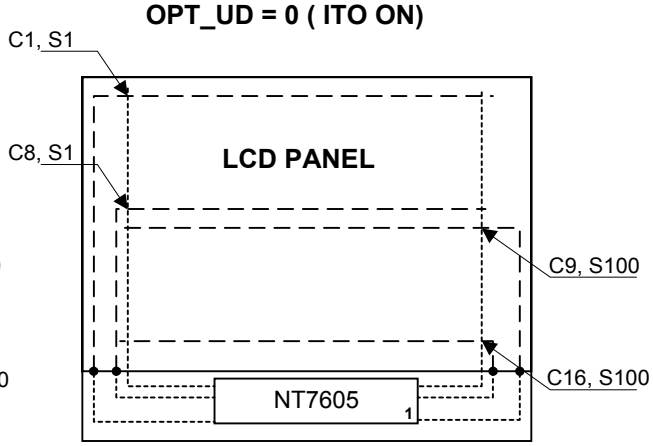


(3) Orientation Type of NT7605:

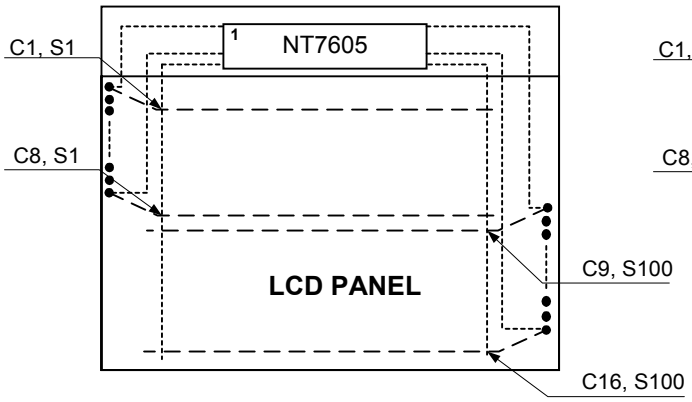
Type1: Place the chip on the upper glass(IC face up)
OPT_UD = 1 (NO ITO)



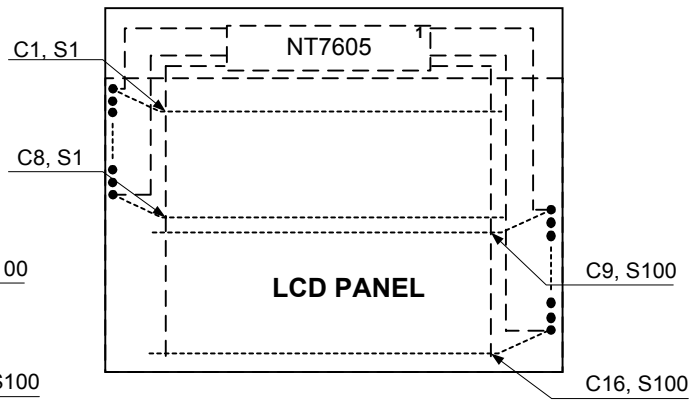
Type2: Place the chip on the lower glass(IC face down)
OPT_UD = 0 (ITO ON)



Type3: Place the chip on the lower glass(IC face down)
OPT_UD = 1 (NO ITO)



Type4: Place the chip on the upper glass(IC face up)
OPT_UD = 0 (ITO ON)



Note:
1. Dot line: ITO layout on lower glass.
2. Dash line: ITO layout on upper glass.

(3) Bias Power Connection

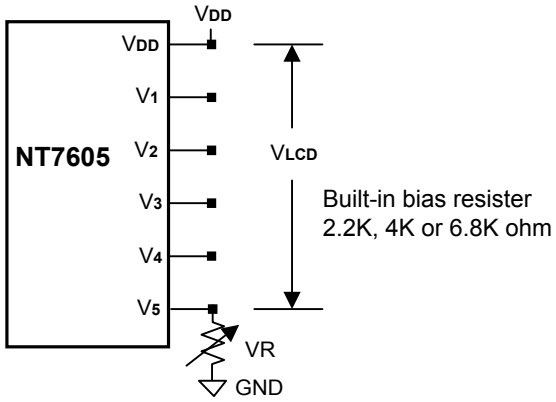
NT7605 provides 1/4 or 1/5 bias for various duty cycle applications. The built-in power division resister divide voltage is described in the following table. The connection of NT7605, power supply, and resistors are also shown as follows:

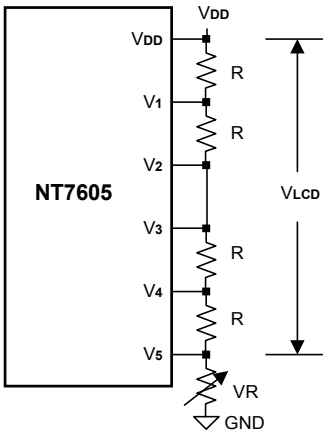
Power Division	1/8, 1/11 Duty Cycle - 1/4 Bias	1/16 Duty Cycle - 1/5 Bias
V_1	V_{DD} - 1/4 V_{LCD}	V_{DD} - 1/5 V_{LCD}
V_2	V_{DD} - 1/2 V_{LCD}	V_{DD} - 2/5 V_{LCD}
V_3	V_{DD} - 1/2 V_{LCD}	V_{DD} - 3/5 V_{LCD}
V_4	V_{DD} - 3/4 V_{LCD}	V_{DD} - 4/5 V_{LCD}
V_5	V_{DD} - V_{LCD}	V_{DD} - V_{LCD}

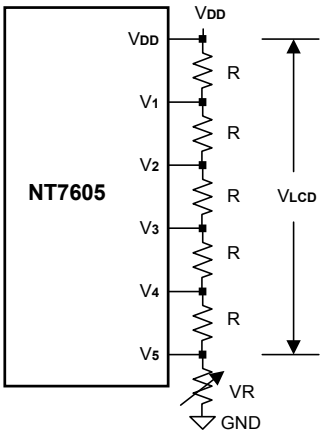
The bias is auto selected by the duty cycle. When the LCD is set to 1/16 duty, the bias is set to 1/5. Otherwise, the bias is set to 1/4.

The ITO Option can select the division resister value:

OPT_R1	OPT_R0	Division Resister
No ITO (1)	No ITO (1)	2.2KΩ
No ITO (1)	ITO On (0)	4KΩ
ITO On (0)	No ITO (1)	6.8KΩ
ITO On (0)	No ITO (0)	No built-in resister (external input)



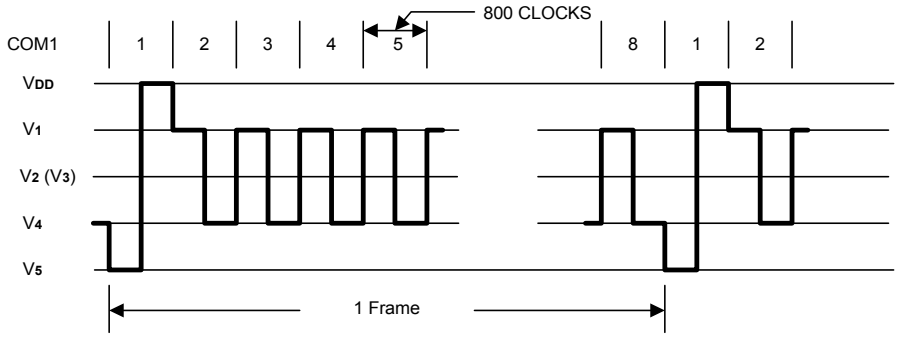




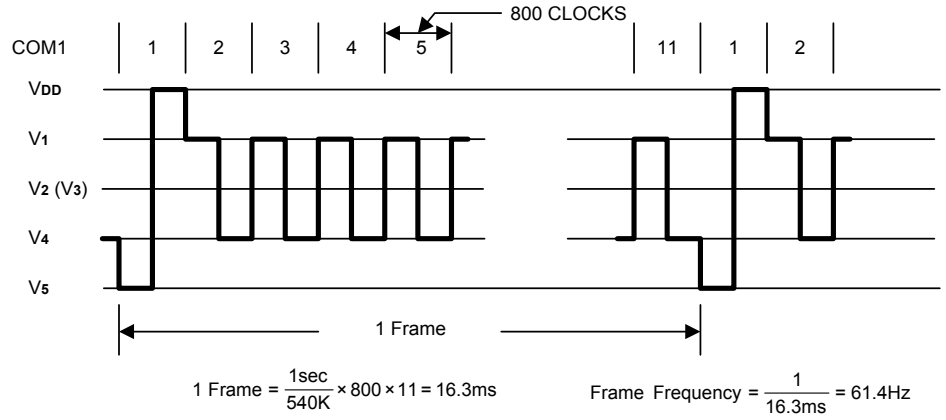
Exit Power division. (The resistance value depends on the LCD panel size)

(4) LCD Waveform

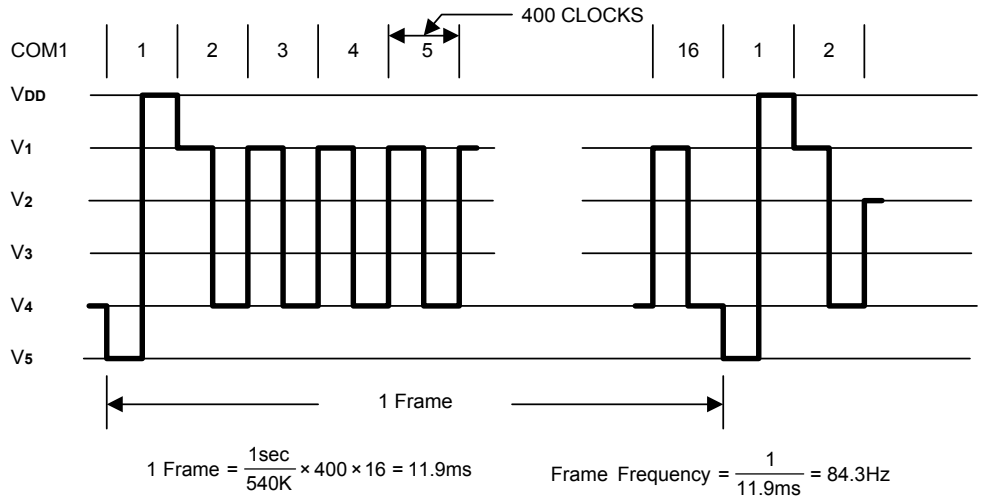
A-type, 1/8 Duty Cycle, 1/4 Bias



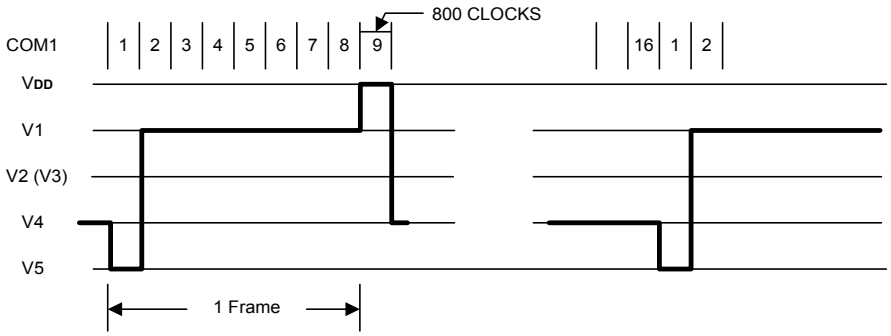
A-type, 1/11 Duty Cycle, 1/4 Bias



A-type, 1/16 Duty Cycle, 1/5 Bias

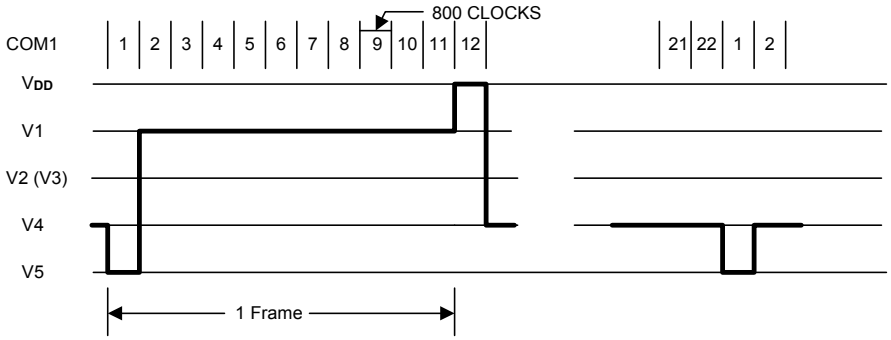


B-type, 1/8 Duty Cycle, 1/4 Bias



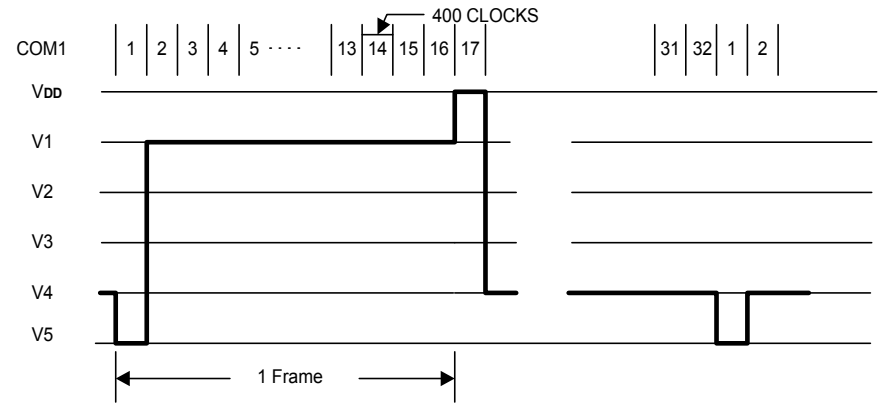
$$1\text{Frame} = \frac{1\text{sec}}{540\text{K}} \times 800 \times 8 = 11.9\text{ms} \qquad \text{Frame Frequency} = \frac{1}{11.9\text{ms}} = 84.3\text{Hz}$$

B-type, 1/11 Duty Cycle, 1/4 Bias



$$1\text{Frame} = \frac{1\text{sec}}{540\text{K}} \times 800 \times 11 = 16.3\text{ms} \qquad \text{Frame Frequency} = \frac{1}{16.3\text{ms}} = 61.4\text{Hz}$$

B-type, 1/16 Duty Cycle, 1/5 Bias



$$1\text{Frame} = \frac{1\text{sec}}{540\text{K}} \times 400 \times 16 = 11.9\text{ms} \qquad \text{Frame Frequency} = \frac{1}{11.9\text{ms}} = 84.3\text{Hz}$$

Low Voltage Reset

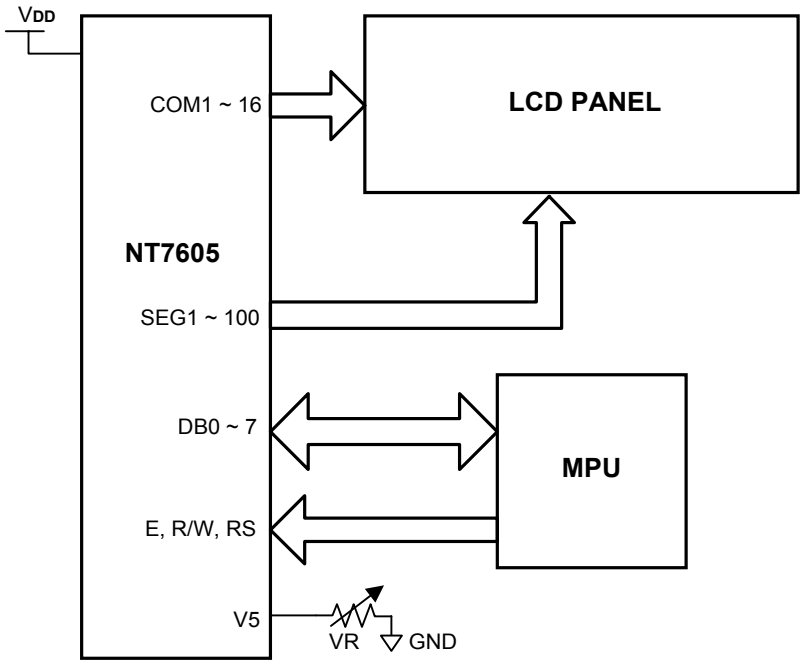
The Low voltage reset function is used to monitor the supply voltage and applies an internal reset at the time when a low voltage is detected.

Functions of the Low Voltage Reset Circuit

The Low voltage reset circuit has the following functions:

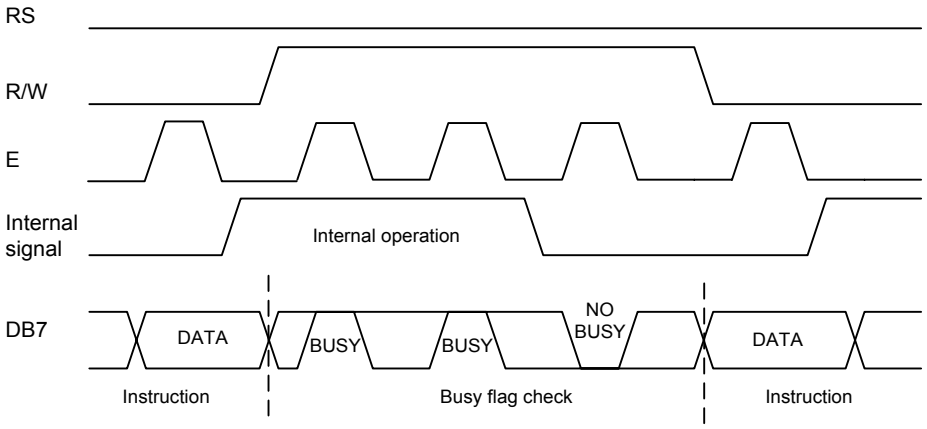
- Generates an internal reset signal when $V_{DD} \leq V_{LVR}$.
- Cancels the internal reset signal when $V_{DD} > V_{LVR}$.
  Here, V_{DD}: power supply voltage, V_{LVR}: Low voltage reset detection voltage, about 2.0V.

Application Circuit (for reference only)

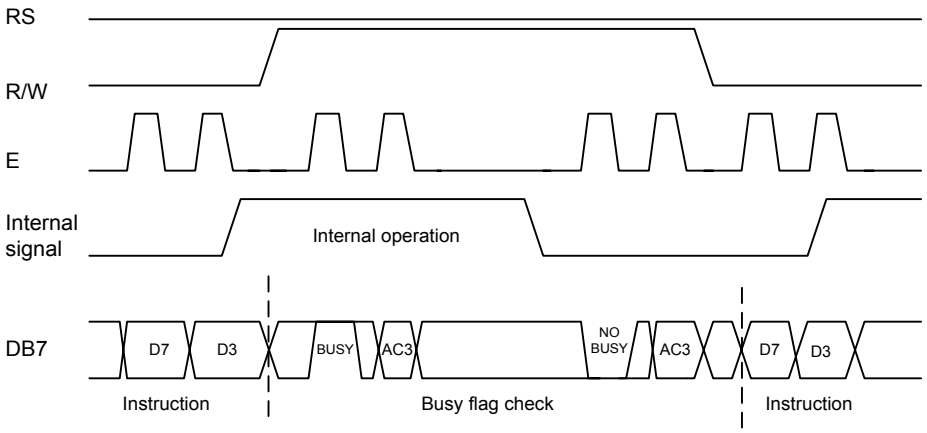


Example (for reference only)

Interface with 8-bit MPU

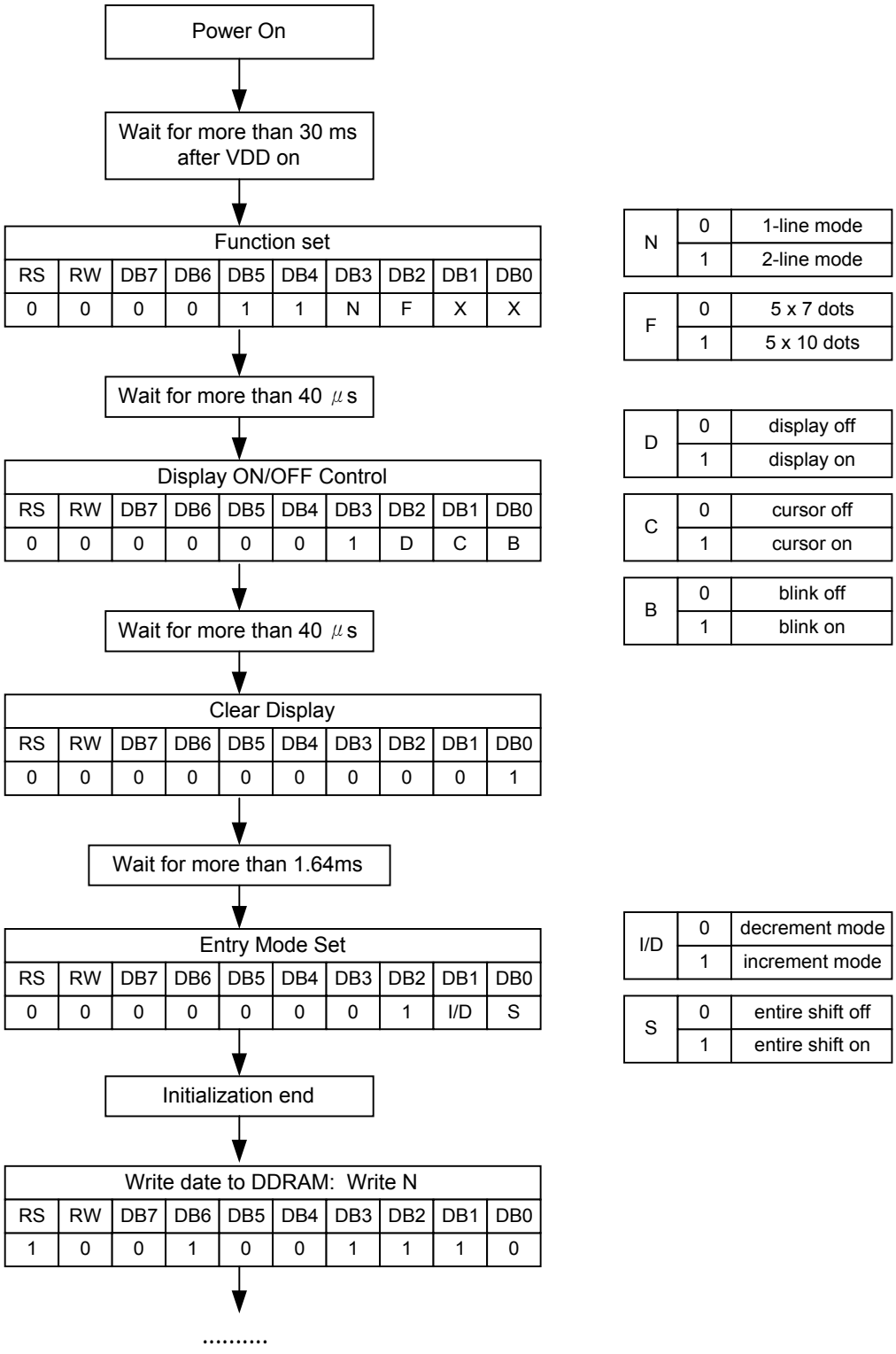


Interface with 4-bit MPU

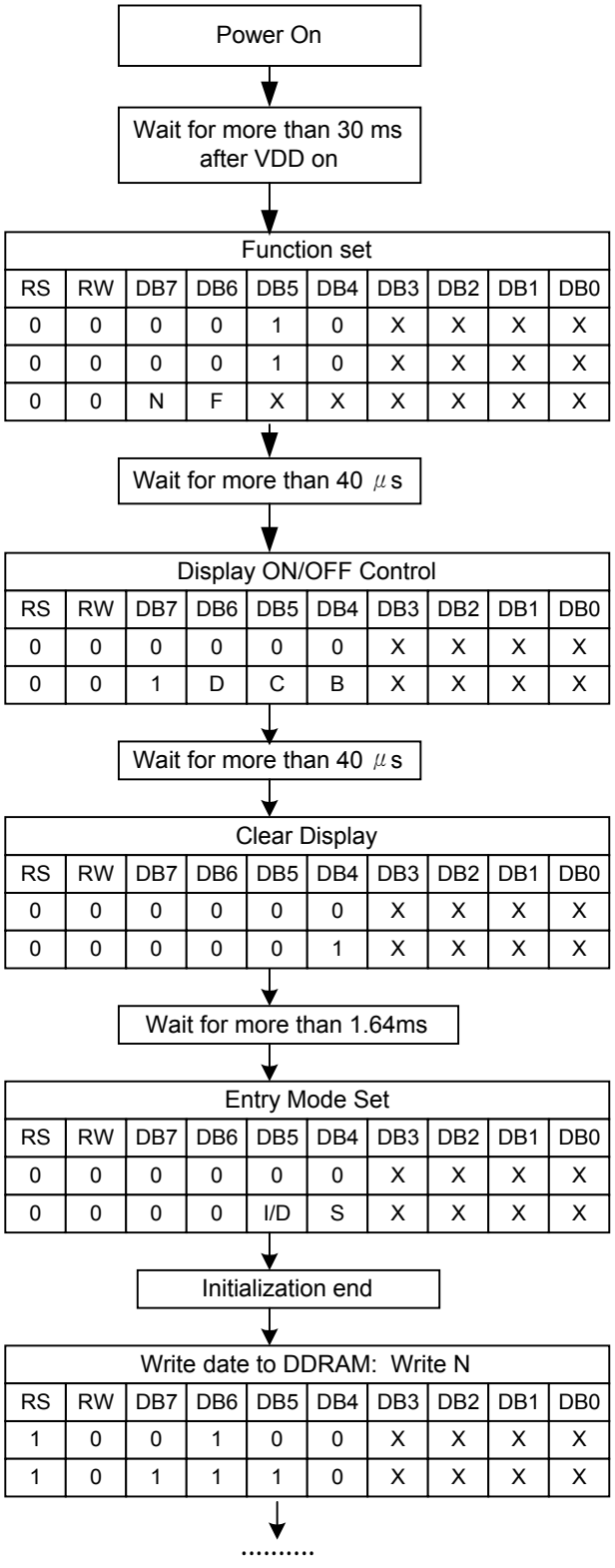


Initializing by Instruction

1. 8-bit Interface



2. 4-bit Interface



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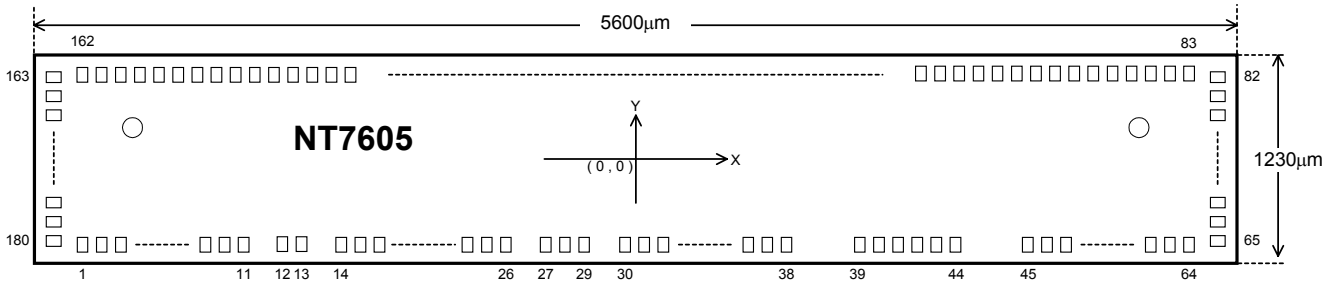
Ordering Information

Part No.	CG ROM	Package	Shipment Style
NT7605H-BDB01	192 CGROM (ref P13)	COG CHIP FORM	Bumped Die on Blue tape
NT7605H-BDT01	192 CGROM (ref P13)	COG CHIP FORM	Bumped Die on chip Tray
NT7605-BDW01	192 CGROM (ref P13)	COG CHIP FORM	Bumped Die on Wafer

Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	TEST	-2567.5	-546.25	31	V_{DD}	-357.5	-546.25
2	TESTM	-2502.5	-546.25	32	V_{DD}	-292.5	-546.25
3	GND	-2437.5	-546.25	33	V_{DD}	-227.5	-546.25
4	GND	-2372.5	-546.25	34	V_{DD}	-162.5	-546.25
5	GND	-2307.5	-546.25	35	V_{DD}	-97.5	-546.25
6	GND	-2242.5	-546.25	36	V_{DD}	-32.5	-546.25
7	GND	-2177.5	-546.25	37	V_{DD}	32.5	-546.25
8	GND	-2112.5	-546.25	38	V_{DD}	97.5	-546.25
9	GND	-2047.5	-546.25	39	RS	552.5	-546.25
10	GND	-1982.5	-546.25	40	RS	617.5	-546.25
11	GND	-1917.5	-546.25	41	RW	682.5	-546.25
12	OSC1	-1787.5	-546.25	42	RW	747.5	-546.25
13	OSC2	-1722.5	-546.25	43	E	812.5	-546.25
14	V_1	-1592.5	-546.25	44	E	877.5	-546.25
15	V_1	-1527.5	-546.25	45	DB0	1332.5	-546.25
16	V_2	-1462.5	-546.25	46	DB0	1397.5	-546.25
17	V_2	-1397.5	-546.25	47	DB1	1462.5	-546.25
18	V_3	-1332.5	-546.25	48	DB1	1527.5	-546.25
19	V_3	-1267.5	-546.25	49	DB2	1592.5	-546.25
20	V_4	-1202.5	-546.25	50	DB2	1657.5	-546.25
21	V_4	-1137.5	-546.25	51	DB3	1722.5	-546.25
22	V_5	-1072.5	-546.25	52	DB3	1787.5	-546.25
23	V_5	-1007.5	-546.25	53	DB4	1852.5	-546.25
24	V_5	-942.5	-546.25	54	DB4	1917.5	-546.25
25	V_5	-877.5	-546.25	55	DB5	1982.5	-546.25
26	V_5	-812.5	-546.25	56	DB5	2047.5	-546.25
27	OPT_R0	-682.5	-546.25	57	DB6	2112.5	-546.25
28	GND_OUT	-617.5	-546.25	58	DB6	2177.5	-546.25
29	OPT_R1	-552.5	-546.25	59	DB7	2242.5	-546.25
30	V_{DD}	-422.5	-546.25	60	DB7	2307.5	-546.25

Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	OPT_LCD	2372.5	-546.25	101	SEG72	1397.5	546.25
62	GND_OUT	2437.5	-546.25	102	SEG71	1332.5	546.25
63	OPT_UD	2502.5	-546.25	103	SEG70	1267.5	546.25
64	TESTD	2567.5	-546.25	104	SEG69	1202.5	546.25
65	COM9	2731.5	-552.5	105	SEG68	1137.5	546.25
66	COM10	2731.5	-487.5	106	SEG67	1072.5	546.25
67	COM11	2731.5	-422.5	107	SEG66	1007.5	546.25
68	COM12	2731.5	-357.5	108	SEG65	942.5	546.25
69	COM13	2731.5	-292.5	109	SEG64	877.5	546.25
70	COM14	2731.5	-227.5	110	SEG63	812.5	546.25
71	COM15	2731.5	-162.5	111	SEG62	747.5	546.25
72	COM16	2731.5	-97.5	112	SEG61	682.5	546.25
73	SEG100	2731.5	-32.5	113	SEG60	617.5	546.25
74	SEG99	2731.5	32.5	114	SEG59	552.5	546.25
75	SEG98	2731.5	97.5	115	SEG58	487.5	546.25
76	SEG97	2731.5	162.5	116	SEG57	422.5	546.25
77	SEG96	2731.5	227.5	117	SEG56	357.5	546.25
78	SEG95	2731.5	292.5	118	SEG55	292.5	546.25
79	SEG94	2731.5	357.5	119	SEG54	227.5	546.25
80	SEG93	2731.5	422.5	120	SEG53	162.5	546.25
81	SEG92	2731.5	487.5	121	SEG52	97.5	546.25
82	SEG91	2731.5	552.5	122	SEG51	32.5	546.25
83	SEG90	2567.5	546.25	123	SEG50	-32.5	546.25
84	SEG89	2502.5	546.25	124	SEG49	-97.5	546.25
85	SEG88	2437.5	546.25	125	SEG48	-162.5	546.25
86	SEG87	2372.5	546.25	126	SEG47	-227.5	546.25
87	SEG86	2307.5	546.25	127	SEG46	-292.5	546.25
88	SEG85	2242.5	546.25	128	SEG45	-357.5	546.25
89	SEG84	2177.5	546.25	129	SEG44	-422.5	546.25
90	SEG83	2112.5	546.25	130	SEG43	-487.5	546.25
91	SEG82	2047.5	546.25	131	SEG42	-552.5	546.25
92	SEG81	1982.5	546.25	132	SEG41	-617.5	546.25
93	SEG80	1917.5	546.25	133	SEG40	-682.5	546.25
94	SEG79	1852.5	546.25	134	SEG39	-747.5	546.25
95	SEG78	1787.5	546.25	135	SEG38	-812.5	546.25
96	SEG77	1722.5	546.25	136	SEG37	-877.5	546.25
97	SEG76	1657.5	546.25	137	SEG36	-942.5	546.25
98	SEG75	1592.5	546.25	139	SEG35	-1007.5	546.25
99	SEG74	1527.5	546.25	139	SEG34	-1072.5	546.25
100	SEG73	1462.5	546.25	140	SEG33	-1137.5	546.25

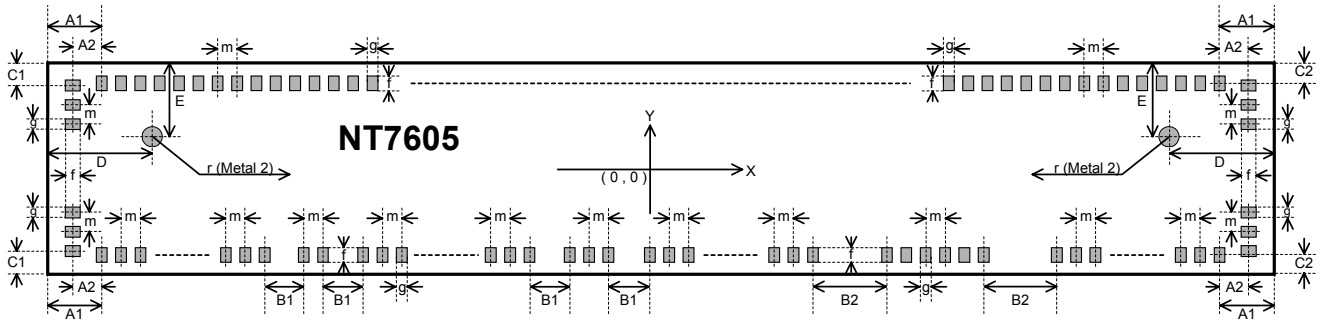
Bonding Diagram (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	SEG32	-1202.5	546.25	162	SEG11	-2567.5	546.25
142	SEG31	-1267.5	546.25	163	SEG10	-2731.5	552.5
143	SEG30	-1332.5	546.25	164	SEG9	-2731.5	487.5
144	SEG29	-1397.5	546.25	165	SEG8	-2731.5	422.5
145	SEG28	-1462.5	546.25	166	SEG7	-2731.5	357.5
146	SEG27	-1527.5	546.25	167	SEG6	-2731.5	292.5
147	SEG26	-1592.5	546.25	168	SEG5	-2731.5	227.5
148	SEG25	-1657.5	546.25	169	SEG4	-2731.5	162.5
149	SEG24	-1722.5	546.25	170	SEG3	-2731.5	97.5
150	SEG23	-1787.5	546.25	171	SEG2	-2731.5	32.5
151	SEG22	-1852.5	546.25	172	SEG1	-2731.5	-32.5
152	SEG21	-1917.5	546.25	173	COM8	-2731.5	-97.5
153	SEG20	-1982.5	546.25	174	COM7	-2731.5	-162.5
154	SEG19	-2047.5	546.25	175	COM6	-2731.5	-227.5
155	SEG18	-2112.5	546.25	176	COM5	-2731.5	-292.5
156	SEG17	-2177.5	546.25	177	COM4	-2731.5	-357.5
157	SEG16	-2242.5	546.25	178	COM3	-2731.5	-422.5
158	SEG15	-2307.5	546.25	179	COM2	-2731.5	-487.5
159	SEG14	-2372.5	546.25	180	COM1	-2731.5	-552.5
160	SEG13	-2437.5	546.25		ALK_L	-2230.95	95
161	SEG12	-2502.5	546.25		ALK_R	2230.95	95

Package Information

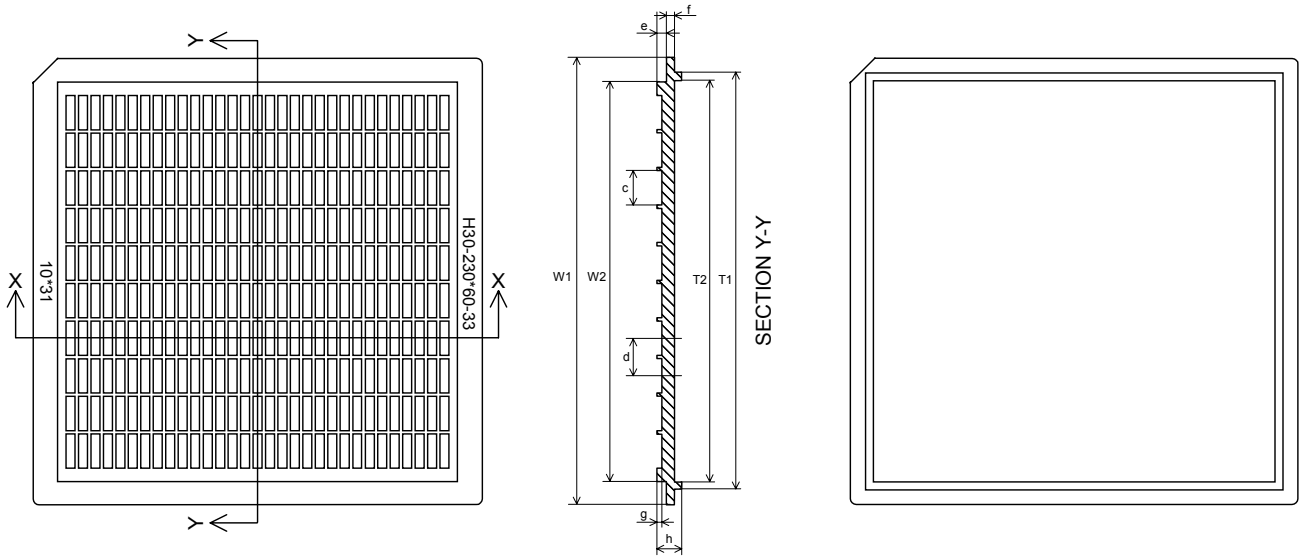
Chip Outline Dimensions

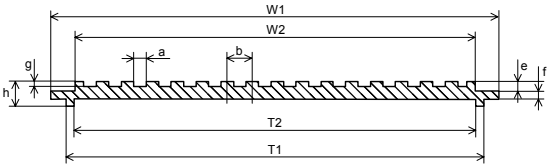
unit: μm



Symbol	Dimensions in μm	Symbol	Dimensions in μm
A1	232.5	D	569.05
A2	164	E	520
B1	130	g	42
B2	455	f	90
C1	62.5	m	65
C2	68.75	r	35

Tray Information





SECTION X-X

Tray Outline Dimensions

unit: mm

Symbol	Dimensions in mm	Symbol	Dimensions in mm
a	1.54	g	0.84
b	2.12	h	4.20
c	5.84	W1	76.0
d	6.14	W2	68.0
e	1.60	T1	71.0
f	1.40	T2	68.3

Product Spec. Change Notice

NT7605 Specification Revision History		
Version	**Content**	**Date**
2.1	Adding Note 3 and modified fosc from 270KHz to 540KHz (Page 14 , Document mistake corrected) Modify the number of clock in single duty from 400 to 800 (1/8 duty and 1/11 duty),200 to 400(1/16 duty) and fosc from 270K to 540K(Page 21) (Document mistake corrected)	Jul.2002
2.0	ROM Table deleted(Page 14) B-type waveform modified(Page 21 , Document mistake corrected)	Apr.2002
1.0	Add new orientation type of NT7605 (page 19) Correct 4-bit interface Initializing sample. (page 26) VDD conditions in Electrical Characteristics changed.(page 6~9) Add more description for OPT_UD option. (page 4)	Nov.2001
0.4	Original	Feb.2001