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# *Data Sheet*

## ***NT39016 D***

**One Chip TFT LCD Driver IC with Timing Controller  
For S960xG240 TFT LCD**

V0.7  
Preliminary Spec.

**Revise History**

<b>NT39016 Specification Revision History</b>			
<b>Version</b>	<b>Content</b>	<b>Page</b>	<b>Date</b>
<b>0.7</b>	<b>Modify DC Electrical Characteristics</b>	<b>29、28</b>	<b>2008/3/10</b>
0.6	Modify pin description	8	2008/2/18
	Remove CPMPDB function	14	
0.5	Modify Analog Supply Voltage	29	2008/2/4
0.4	Modify 3-Wire Control Register	12	2008/1/14
0.3	Modify STBYB initial value	14	2007/11/26
	Modify Digital Operating Current value	28	
	Modify Analog Operating Current value	29	
0.2	Source Driver Output Timing Diagram	33	2007/11/16
0.1	New Spec.	--	2007/10/22

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## Features

- One-Chip solution for 960 x 240 dot TFT LCD Driver
- 8-bit resolution 256 gray scale with Dithering
- Support 8-bit / 24-bit digital (RGB) or CCIR\_601/656 input timing
- Support two sets of 3-Wire commands for internal parameters setting
- Build-In DC2DC power supplies (VGH/VGL/VCOMAC/VCOMDC voltage supply)
- Configurable color filter type for both Delta and Stripe type
- 3.0 ~ 3.6V digital supply voltage with Build-In 1.8V LDO for internal circuit
- 3.0 ~ 3.6V charge pump supply voltage
- Configurable VCOMAC : 4.6V~6.1V
- Configurable VCOMDC : 1.0V~2.26V
- Source output deviation: 20mV(max)
- Source output settling time: 30uS(max)
- Operating frequency: 30MHz(max)
- Right/Left shift, Up and Down scan function selectable
- Support VCOM swing driving output
- Support Cs on Common structure
- Build-In PWM circuit for LED Back-light
- Support stand-by mode for low power consumption
- Frame / One Line / Two Line Inversion driving method selectable
- Built-in Auto Test Pattern
- COG package

## General Description

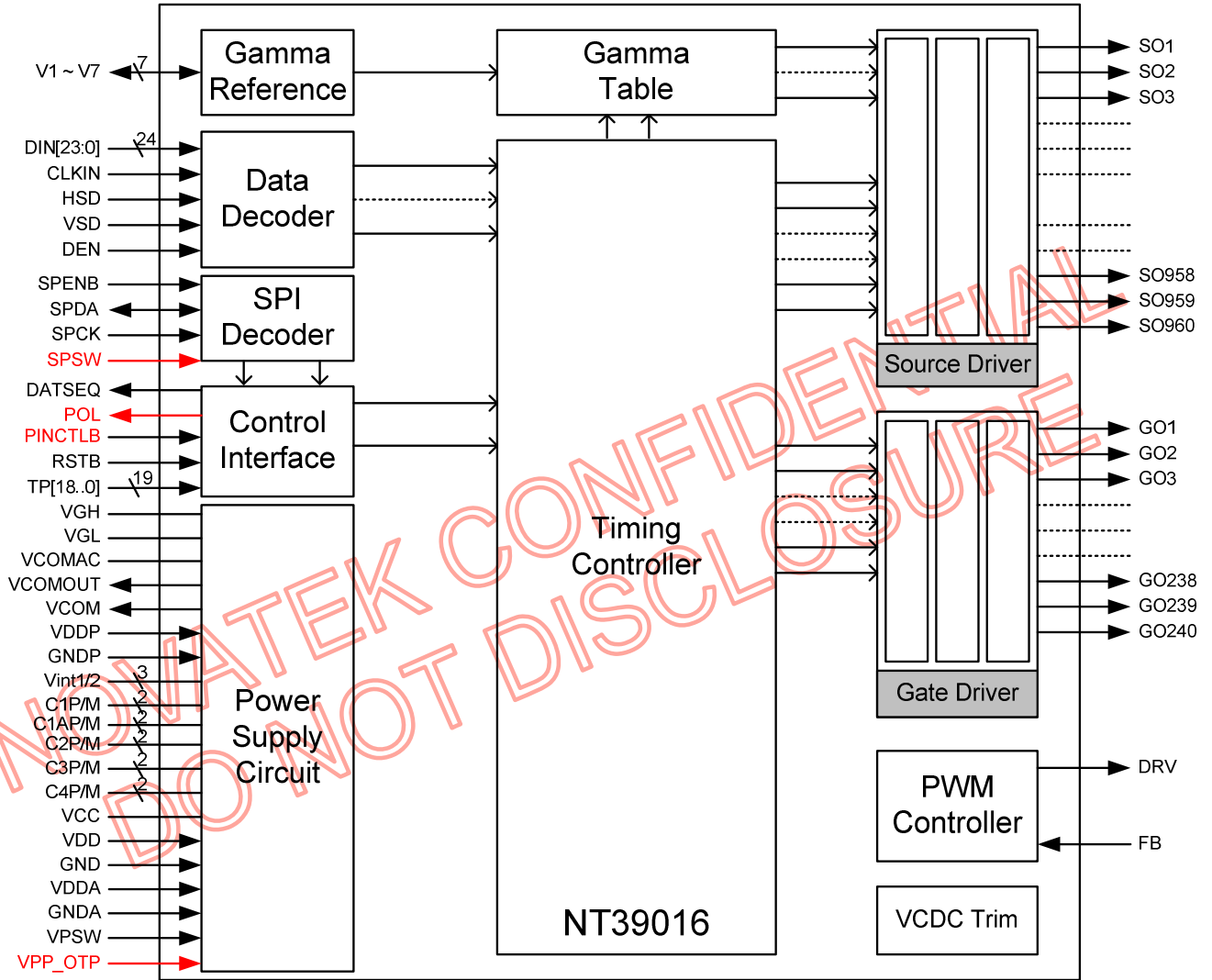
NT39016 is a single-chip solution for 960x240 dot color TFT-LCD panel, which integrated source driver, gate driver, timing controller, power generator and 3-wire interface for system function control.

With highly integration technology, NT39016 integrate 960 channels source driver and 240 channels gate driver on single silicon. Data Input support 8 bit digital image data with standard CCIR601/656, serial 8-bit RGB data format or parallel 24-bit RGB data format. Source outputs support 8-bit resolution (256 gray scales) with dithering function on. Custom parameters can be set by using 3-wire commands. Special circuit architecture is designed for system lower power dissipation.

NT39016 is designed for wide voltage supply range and small output deviation for better display quality. Power dissipation for internal 5 sections reference voltage resistors for 64-level gamma resistors are also concerned. Supporting multiple input timings make this chip more suitable to various applications of small size TFT-LCD panel.

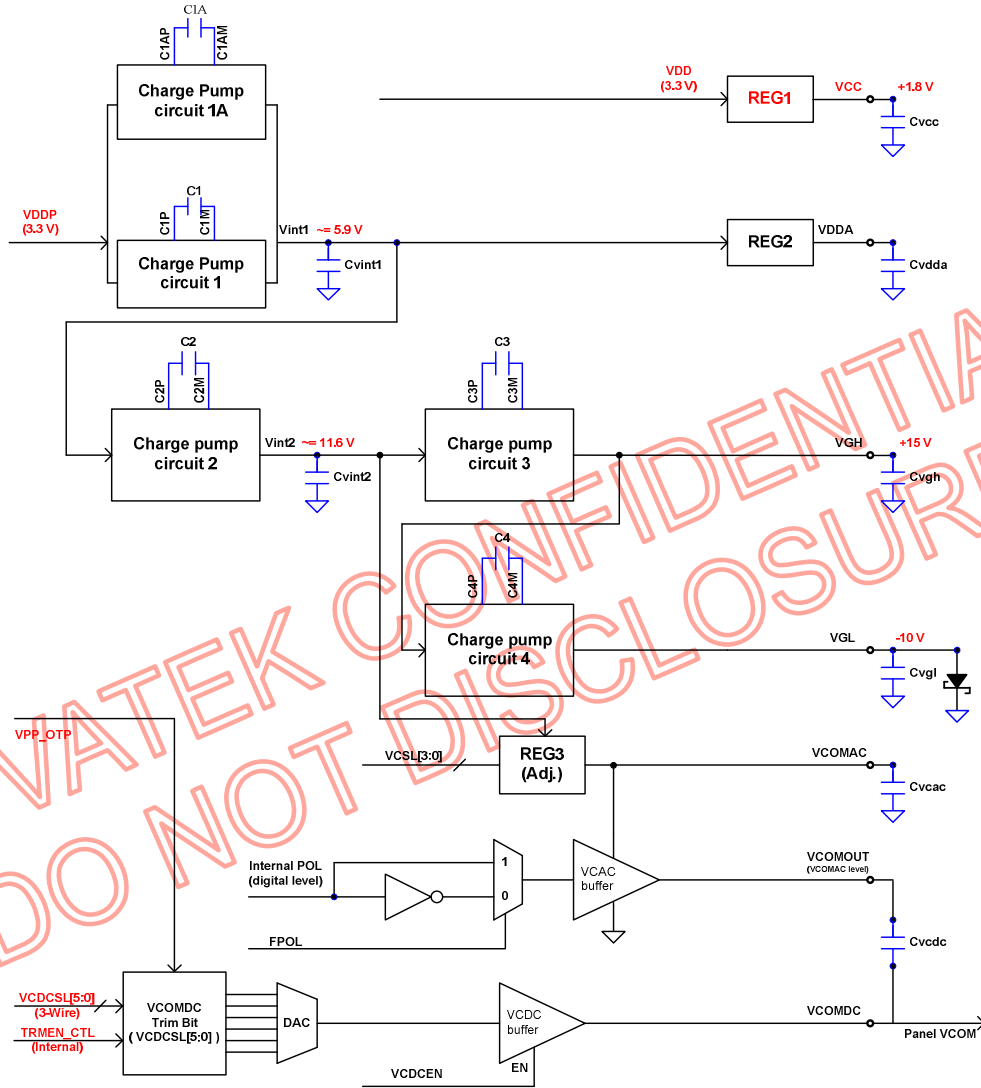
## Function Block Diagram

### System Block Diagram



### Charge Pump Circuit Block Diagram

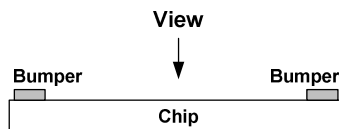
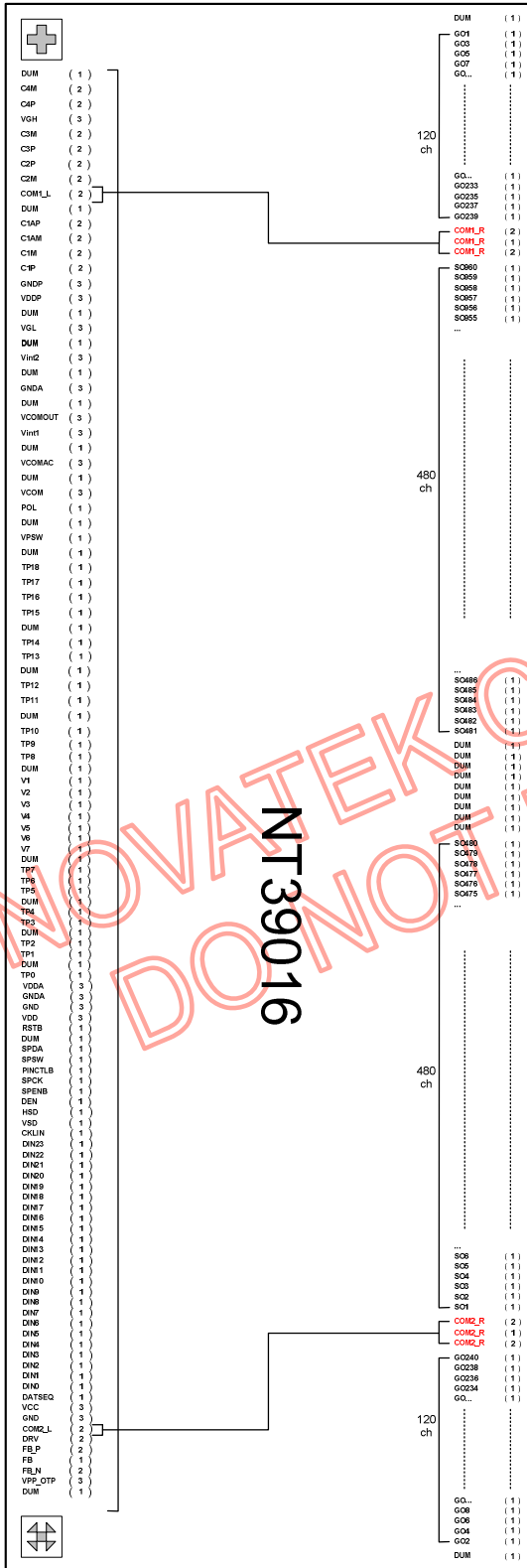
NT39016 built in charge pump circuit for gate driver VGH / VGL voltage and panel VCOMAC/VCOMDC voltage. Following block diagram illustrate how the charge pump circuit works.



#### <Value of wiring resistance and Cap.>

Pin name	Resistor of wiring (ohm)	Cap no.	CAP (uF)
C1P	< 10	C1	≥1uF
C1M	< 10		
C2P	< 10	C2	
C2M	< 10		
C3P	< 10	C3	
C3M	< 10		
C4P	< 10	C4	
C4M	< 10		
C1AP	< 10	C1A	
C1AM	< 10		

**\*Note: Others Cap. Suggest value ≥ 4.7 uF  
Schottky diode turn-on voltage=0.2V**

**Pad Sequence (Bump Side)**




## Pad Description

### NT39016 Pad Description:

Designation	I/O	Description
DIN[23..0]	I	Data Input. For 8/24-bit digital (RGB) or 8-bit CCIR601/656 image data input 8-bit mode: DIN7: MSB; DIN0: LSB; the remainder should be connect to GND. 24-bit mode: DIN[7:0] = R[7:0] data; DIN[15:8] = G[7:0] data; DIN[23:16] = B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data bus to GND.
CLKIN	I	Clock for Input Data. Data latched at rising/falling edge of this signal. Default Negative polarity.
HSD	I	Horizontal Sync input. Default Negative polarity, can be change by HSDPOL register.
VSD	I	Vertical Sync input. Default Negative polarity, can be change by VSDPOL register.
DEN	I (Pull Low)	Data Input Enable. Active High to enable the data input Bus under "DE Mode". Normally pull low.
DATSEQ	O	Data sequence control pin for external T-CON. Output "1": for Odd line, "0": for Even line
POL	O	Frame polarity output. Amplitude of signal is from 0V to 3.3V.
V1 ~ V7	I/O	Gamma correction reference voltage. When VSET="1" is used. The voltage of pins V1 ~ V7 must be swing and must be AVDD-0.1V > V1 > V2 > V3 > V5 > V6 > V7 > AGND+0.1V when POL="1" and AGND+0.1V < V1' < V2' < V3' < V5' < V6' < V7' < AVDD-0.1V when POL="0", Where V1-V2=V2'-V1', V2-V3=V3'-V2', ... V5-V6=V6'-V5', V6-V7=V7'-V6'. Note: V1~V7 must be supplied voltage external when VSET="1". Vx is external power of positive polarity and Vx' is external power of negative polarity
SPENB	I (Pull High)	3-Wire Communication Enable. Active Low. Normally pull high. <b>Please pull high or floating under PINCTLB=0 mode.</b>
SPDA	I/O	3-Wire Communication Data input/output.
SPCK	I	3-Wire Communication Clock input. Rising edge latch.
SPSW	I (Pull Low)	3-Wire register map select. "0" for default 3-Wire register map, "1" for optional 3-Wire register map.
RSTB	I (Pull High)	Global reset pin. Active Low to enter Reset State. Suggest connecting with a RC reset circuit for stability. Normally pull high.
PINCTLB	I (Pull High)	Enable pin control function. Normally pull high PINCTLB = "0", Enable pin control function. TP0~14 and TP16~18 active as input pin for function control propose. Refer to the TP0~18 description for more information. PINCTLB = "1", Default mode. TP0~14 and TP16~18 active as unknown state ; Don't connect TP0~14 and TP16~18 to any state under this mode. <b>Note: The 3-wire control register will be disabled under PINCTLB = 0 mode.</b>
SO1~SO960	O	Source Driver Output Signals.
GO1~GO240	O	Gate Driver Output Signals.
ALIGN_T/B	M	For assembly alignment.
TP15	I	Charge pump on/off control pin. TP15=CPMPDB CPMPDB = "0", internal charge pump will be shut down CPMPDB = "1", internal charge pump normal operating TP15 active as input pin under any state of PINCTLB. If floating TP15, the charge pump will turn off
TP0~14 TP16~18	T I	TEST Pin / Function control pin. When PINCTLB = "1", TP0~14, TP16~18 act as test pin. Floating those pins for normal operation. When PINCTLB = "0", TP0~14, TP16~18 act as function control input pin. All the input pin should be connect to GND or VDD. Floating those pins will result in input unknown problem.
VPSW	I (Pull Low)	Voltage control switch. Normally pull low. VPSW = "0". Default mode. VGH · VGL · VCOMAC and VCOMDC active as normal use and control by 3-wire. VPSW = "1". Voltage fix mode. VGH = 18V · VGL = -7V · VCOMAC = 5.4V and VCOMDC



		= 1.7V. Under the mode voltage can't control by 3-wire
VPP_OTP	P	Customer OTP power input pin
VGH	PS	Capacitor pin. Positive power supply for Gate Driver output
VGL	PS	Capacitor pin. Negative power supply for Gate Driver output
VCOMAC	PS	Capacitor pin. Power supply for VCOMOUT output
VCOM	PS	VCOM DC voltage output pin for DC re-construction
VCOMOUT	O	Frame polarity output for panel VCOM. Amplitude of signal is from GNDA1 to VDDA1 The polarity of VCOMOUT is inversed with internal signal "POL" when "FPOL" = 0
VDDA	PO	Power supply for source driver and gamma circuit
GNDA	PI	Ground pins for source driver and gamma circuit
VDD	PI	Power supply for digital circuits
GND	PI	Ground pins for digital circuits
VDDP	PI	Power supply for charge pump circuits
GNDP	PI	Ground pins for charge pump circuits
VCC	C	Capacitor connect pin for internal regulator Refer to the section of "Power Circuit" for the application.
C1P/M C1AP/M C2P/M C3P/M C4P/M Vint1/2	C	Capacitor connect pin for internal charge pump Refer to the section of "Power Circuit" for the application.
FB_P	I	Internal power switch current input pad. <b>Note: Voltage on this pad should be &lt; 5.5V. Pull low in more than one LED case.</b>
FB_N	O	Internal power switch current output pad. <b>Note: Voltage on this pad should be &lt; 5.5V. Pull low in more than one LED case.</b>
FB	VI	PWM controller feedback input. FB threshold is 0.6 V nominal
DRV	O	PWM output driver signal for the boost converter
COM1_L/R	S	The internal link together between input side and Output side.
COM2_L/R	S	The internal link together between input side and Output side.
<b>DUM</b>	<b>D</b>	<b>Don't connect to any signal or pull high/low.</b>

Note:

I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, T: Testing  
I/O: Input / Output, PS: Power Setting, C: Capacitor pin.

**NT39016 Align Mark:**

ALIGN_T	M	For assembly alignment.
ALIGN_B	M	For assembly alignment.

**NT39016 Pass Line Description:**

Pass Line No:	Pad Name	
1	COM1_L	COM1_R
2	COM2_L	COM2_R

**TP0 ~ TP14 and TP16~TP18 Function Control Pin Mapping Table (When PINCTLB = "0"):**

TPx	PINCTLB = "0"
	Input control function (Related to 3-wire control register)
0	STBYB
1	UPDN
2	SHLR
3	SEL0
4	SEL1
5	SEL2
6	SEL3
7	FRAD0
8	FRAD1
9	PAL
10	PALM
11	SKIPMOD
12	HDNC0
13	HDNC1
14	FPOL
16	PWMPDB
17	AVGY
18	Auto Test Pattern Enable

Note 1: PINCTLB function has higher priority than the 3-wire command. The 3-wire control register will be disabled when PINCTLB = "0". **Please pull high or floating SPENB under PINCTLB=0 mode.**

**Remark:**

TP15=CPMPDB · Charge pump on/off control pin.

CPMPDB = "0", internal charge pump will be shut down

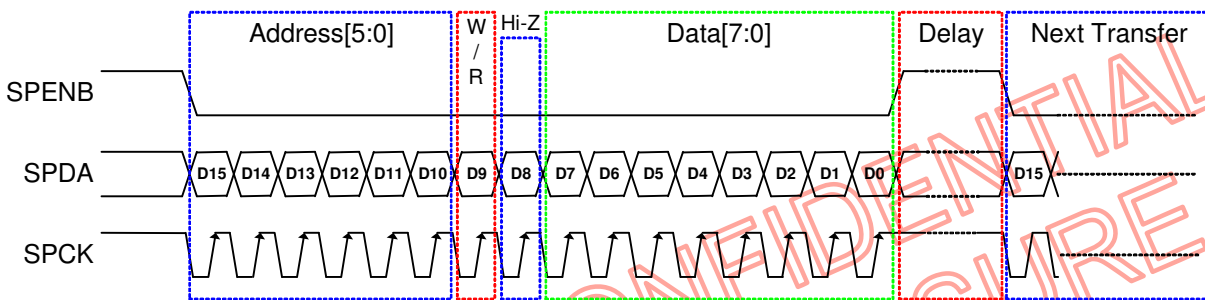
CPMPDB = "1", internal charge pump normal operating

TP15 active as input pin under any state of PINCTLB.

### 3-Wire Serial Port Interface (Default Register Map)

#### 3-Wire Command Format

NT39016 uses the 3-wire serial port as communication interface for all the function and parameter setting. 3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. NT39016 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself. Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SPCK by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SPDA pin under “Hi-Z phase” and “Data phase”. Refer to the section of “3-Wire Timing Diagram” for the detail timing, please.



#### 3-Wire Command Format:

Bit	Description
D15-D10	Register Address [5:0].
D9	W/R control bit. “1” for Write; “0” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7-D0	Data for the W/R operation to the address indicated by Address phase

#### 3-Wire Writer Format:

MSB																LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Address [5:0]						1	X	DATA (Issue by external controller)								

#### 3-Wire Read Format:

MSB																LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Register Address [5:0]						0	Hi-Z	DATA (Issue by NT39016)								

### 3-Wire Control Registers (Default)

Following table list the default 3-Wire control registers and bit name definition for NT39016. Refer to the next section for detail register function description, please.

**NT39016 3-Wire Control Register List (Default)**

3-Wire Registers		Register Description		
D[15:10]	Name	Init.	R/W	Function Description
000000b	R00	07h	R/W	System control register
000001b	R01	00h	R/W	Timing Controller function register
000010b	R02	03h	R/W	Operation control register
000011b	R03	CCh	R/W	Input data Format control register
000100b	R04	46h	R/W	Source Timing delay control register
000101b	R05	0Dh	R/W	Gate Timing delay control register
000110b	R06	00h	R/W	Reserved
000111b	R07	00h	R/W	Internal function control register
001000b	R08	08h	R/W	RGB Contrast control register
001001b	R09	40h	R/W	RGB Brightness control register
001010b	R0A	88h	R/W	Hue / Saturation control register
001011b	R0B	88h	R/W	R / B Sub-Contrast control register
001100b	R0C	20h	R/W	R Sub-Brightness control register
001101b	R0D	20h	R/W	B Sub-Brightness control register
001110b	R0E	10h	R/W	VCOMDC Level Control Register
001111b	R0F	A4h	R/W	VCOMAC Level Control Register
010000b	R10	04h	R/W	VGAM2 level control register
010001b	R11	24h	R/W	VGAM3/4 level control register
010010b	R12	24h	R/W	VGAM5/6 level control register
011110b	R1E	00h	R/W	VCOMDC Trim function control register
100000b	R20	00h	R/W	Wide and narrow display mode control register

**NT39016 3-Wire Register Bit Definition (Default)**

3-Wire Control Register Bit Map								
Reg.	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
R00	PAT3	PAT2	PAT1	PAT0	PWMPDB	X	STBYB	RESETB
R01	X	X	X	SWD2	SWD1	SWD0	DITHB	CFTYP
R02	SKIPMOD	HDNC1	HDNC0	X	FPOL	VSET	UPDN	SHLR
R03	DENPOL	CLKPOL	HSDPOL	VSDPOL	SEL3	SEL2	SEL1	SEL0
R04	DDL7	DDL6	DDL5	DDL4	DDL3	DDL2	DDL1	DDL0
R05	X	HDLY6	HDLY5	HDLY4	HDLY3	HDLY2	HDLY1	HDLY0
R06	X	X	X	X	X	X	X	X
R07	FRAD1	FRAD0	INVSL1	INVSL0	PAL	PALM	-	AVGY
R08	X	X	X	CON4	CON3	CON2	CON1	CON0
R09	X	BRI6	BRI5	BRI4	BRI3	BRI2	BRI1	BRI0
R0A	HUE3	HUE2	HUE1	HUE0	SAT3	SAT2	SAT1	SAT0
R0B	SCONB1	SCONB0			SCONR1	SCONR0		
R0C	X	X	SBRIR5	SBRIR4	SBRIR3	SBRIR2	SBRIR1	SBRIR0
R0D	X	X	SBRIB5	SBRIB4	SBRIB3	SBRIB2	SBRIB1	SBRIB0
R0E	X	OTP_BYPS	VCDCSL5	VCDCSL4	VCDCSL3	VCDCSL2	VCDCSL1	VCDCSL0
R0F	VGLSL1	VGLSL0	VGHSL1	VGHSL0	VCACSL3	VCACSL2	VCACSL1	VCACSL0
R10	X	X	X	GAMEN	X	V2GAM2	V2GAM1	V2GAM0
R11	X	X	V4GAM2	V4GAM1	V4GAM0	V3GAM2	V3GAM1	V3GAM0
R12	X	X	V6GAM2	V6GAM1	V6GAM0	V5GAM2	V5GAM1	V5GAM0
R1E	TRMEN7	TRMEN6	TRMEN5	TRMEN4	TRMEN3	TRMEN2	TRMEN1	TRMEN0
R20	X	X	X	X	X	X	WNSEL1	WNSEL0

**Note: Register function active at the falling edge of VSD except STBYB, RESETB register bits.**

**Registers require Vsync trigger table**

DITHB	CFTYP	SKIPMOD	HDNC	FPOL	VSET	UPDN	SHLR	DDL7	HDLY	FRAD	INVSL
PAL	PALM	AVGY	CON	BRI	HUE	SAT	SCONB	SCONR	SBRIR	SBRIB	

### 3-Wire Registers Function Description

#### R00: System Control Register

Bit	Name	Initial	R/W	Description
Bit [7:4]	PAT[3:0]	0000b	R/W	Internal Test Pattern Selection PAT[3:0] : Select chip embedded test pattern.
Bit [3]	PWMPDB	0b	(R) R/W	Internal PWM controller Power Down bit PWMPDB = "0", internal PWM controller will be shut down PWMPDB = "1", internal PWM controller normal operating
Bit [2]	-	-	-	<b>Reserve</b>
Bit [1]	STBYB	1b	(R) R/W	Standby Mode function control. STBYB = "0", TCON, Source output will turn off and outputs are High-Z. STBYB = "1", Normal operation
Bit [0]	RESETB	1b	R/W	Global Reset Register. Write "0" to reset whole chip. This bit will set to "1" automatically after chip was reset.

#### PAT[3:0] : Embedded Auto Test Pattern Selection Register

PAT[3:0]	Test Pattern	Note
00H	Disable Internal Test Pattern Function	Default
01H	White	
02H	Black	
03H	Red	
04H	Green	
05H	Blue	
06H	Yellow	
07H	Cyan	
08H	Magenta	
09H	Gray Level 8	
0AH	Gray Level 16	
0BH	Color Bar	
0CH	Checker Board	
0DH	Cross Talk Pattern	
0EH	Horizontal Flick Pattern	
0FH	Test Pattern Auto Run Mode	

Note: WNSEL[1:0] will be disabled under Internal Test Pattern mode.

**R01: Timing Controller Function Register**

Bit	Name	Initial	R/W	Description
Bit [4:2]	SWD[2:0]	000b	R/W	Control and switch the relationship between the R,G,B and outputs. This register is used to match different types of color filters on LCD panel
Bit [1]	DITHB	0b	R/W	Dithering enable. Active low DITHB = "0", Dithering on, (Pseudo 8-bits resolution). (Default mode) DITHB = "1", Dithering off, (6-bits resolution, truncation last 2-bits of the input data) Note 1: Recommend user to enable this function under all modes except for 18 bit RGB input application.
Bit [0]	CFTYP	0b	R/W	Color Filter Type Select. Select Delta or Stripe mode for data arrangement. CFTYP = "0", Stripe mode, Data arrangement keep in the "odd line" state of SWD[2:0] selection. CFTYP = "1", Delta mode, Data arrangement controlled by SWD[2:0] setting.

**SWD[2:0] function control:**

SWD2	SWD1	SWD0	Output (n=0 to 319)			Condition
			3n+1	3n+2	3n+3	
0	0	0	R	G	B	Odd Line
			G	B	R	Even Line
0	0	1	G	B	R	Odd Line
			B	R	G	Even Line
0	1	X	B	R	G	Odd Line
			R	G	B	Even Line
1	0	0	G	B	R	Odd Line
			R	G	B	Even Line
1	0	1	B	R	G	Odd Line
			G	B	R	Even Line
1	1	X	R	G	B	Odd Line
			B	R	G	Even Line

Note 1: X = Don't care

Note 2: Data arrangement will keep in the "odd line" state when CFTYP = 0 for stripe mode.



**R02: Operation Control Register**

Bit	Name	Initial	R/W	Description
Bit [7]	SKIPMOD	0b	(R) R/W	Horizontal data processing algorithms select register. SKIPMOD = "0": Horizontal data weighting skip mode. (Default mode) SKIPMOD = "1": Horizontal data direct skip mode.
Bit [6:5]	HDNC[1:0]	00b	(R) R/W	Horizontal Data scaling mode select register. This function is active under CCIR601 and CCIR656 mode only.
Bit [4]	-	-	-	Reserve
Bit [3]	FPOL	0b	R/W	VCOMOUT polarity inverse control. FPOL = "0": VCOMOUT normal polarity (Default mode). FPOL = "1": VCOMOUT inverse polarity.
Bit [2]	VSET	0b	R/W	Gamma correction source select. VSET = "0", used internal Gamma Reference voltage (VDDA). (Default mode) VSET = "1", used external Gamma Reference Input (V1~V7).
Bit [1]	UPDN	1b	(R) R/W	Gate Driver Up/down scan control of gate driver. UPDN = "0", Shift from down to up, First line=L240->L239->...->L2->L1= Last line UPDN = "1", Shift from up to down, First line=L1->L2->...->L239->L240= Last line (Default mode)
Bit [0]	SHLR	1b	(R) R/W	Right/Left sequence control of source driver. SHLR = "0", shift left: Last data = S1 ← S2 ← S3..... ← S960 =First data. SHLR = "1", shift right: First data = S1 → S → S3..... → S960 = Last data.

**HDNC[1:0] function setting for different horizontal data skip mode**

HDNC1	HDNC0	Source Data	Data Skip Mode
0	0	1440 / 1280 clock	1440 clock -> 720 RGB -> (scale down) 320 RGB 1280 clock -> 640 RGB -> (scale down) 320 RGB
0	1	1440 clock	1440 clock -> 720 RGB -> (Skip Right/Left 10 RGB) 700 RGB -> (scale down) 320 RGB
1	0	1440 clock	1440 clock -> 720 RGB -> (Skip Right/Left 20 RGB) 680 RGB -> (scale down) 320 RGB
1	1	1440 clock	1440 clock -> 720 RGB -> (Skip Right/Left 40 RGB) 640 RGB -> (scale down) 320 RGB

**Note: HDNC function is active under CCIR601/656 mode only**

**R03: Input Data Format Control Register**

Bit	Name	Initial	R/W	Description
Bit [7]	DENPOL	1b	R/W	DEN input pin polarity control. DENPOL = "0", DEN negative polarity. DENPOL = "1", DEN positive polarity. (Default mode)
Bit [6]	CLKPOL	1b	R/W	CLKIN pin polarity control. CLKPOL = "0", CLKIN negative edge latch data. CLKPOL = "1", CLKIN positive edge latch data. (Default mode)
Bit [5]	HSDPOL	0b	R/W	HSD pin polarity control. HSDPOL = "0", HSD negative polarity. (Default mode) HSDPOL = "1", HSD positive polarity.
Bit [4]	VSDPOL	0b	R/W	VSD pin polarity control. VSDPOL = "0", VSD negative polarity. (Default mode) VSDPOL = "1", VSD positive polarity
Bit [3:0]	SEL[3:0]	1100b	(R) R/W	Input data format selection. Note: Different SEL [3:0] setting resolute in different AC timing.

**SEL[3:0]: Data input mode**

SEL3	SEL2	SEL1	SEL0	Data input format	Operating frequency
0	0	0	0	CCIR601 YUV 1280 input format (YUV mode A)	24.54 MHz
0	0	0	1	CCIR601 YUV 1280 input format (YUV mode B)	24.54 MHz
0	0	1	0	CCIR601 YUV 1440 input format (YUV mode A)	27 MHz
0	0	1	1	CCIR601 YUV 1440 input format (YUV mode B)	27 MHz
0	1	0	0	CCIR656 YCbCr input format (YcbCr mode A)	27 MHz
0	1	0	1	CCIR656 YCbCr input format (YcbCr mode B)	27 MHz
0	1	1	0	-	-
0	1	1	1	-	-
1	0	0	0	8-bit digital RGB input format HV Mode (NTSC only)	27 MHz
1	0	0	1	8-bit digital RGB input format DE Mode (NTSC only)	27 MHz
1	0	1	0	8-bit digital RGB through mode input format HV Mode (NTSC only)	27 MHz
1	0	1	1	8-bit digital RGB through mode input format DE Mode (NTSC only)	27 MHz
1	1	0	0	24-bit digital RGB input format HV Mode (NTSC only)	6.4 MHz
1	1	0	1	24-bit digital RGB input format DE Mode (NTSC only)	6.4 MHz
1	1	1	0	-	-
1	1	1	1	-	-

Note : Hsync and Vsync will be floated in CCIR656 and DE mode

Remark:

YUV mode A: Data sequence are "Cb\_Y\_Cr\_Y..."

YUV mode B: Data sequence are "Cr\_Y\_Cb\_Y..."

RGB through mode will bypass 3-wire SWD[2:0] function; TCON will not arrange data color mapping.

**R04: Source Timing Delay Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:0]	DDL[7:0]	46h	R/W	Select the HSD signal to 1 <sup>st</sup> input data delay timing Under CCIR601 mode, $T_{hs} = DDL[7:0] + 128$ , (Unit = CLKIN) Under CCIR656 mode, $T_{hs} = DDL[7:0] + 136$ , (Unit = CLKIN) Under RGB 8/24 bit mode, $T_{hs} = DDL[7:0]$ , (Unit = CLKIN) The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of "Timing Table" for the detail, please.

Note: DDL function will be disabled under 8/24bit DE mode and PINCTLB = 0 condition. The default value list in the timing table will be used when PINCTLB = 0.

**R05: Gate Timing Delay Control Register**

Bit	Name	Initial	R/W	Description
Bit [7]	-	-	-	Reserve
Bit [6:0]	HDLY[6:0]	0Dh	R/W	Select the Gate start pulse output delay timing $T_{vs} = HDLY[6:0]$ , (Unit = HSD) The register value will be update to the different default value each time when SEL[3:0] changed. Read the section of "Timing Table" for the detail, please.

Note: HDLY function will be disabled under 8/24bit DE mode and PINCTLB = 0 condition. The default value list in the timing table will be used when PINCTLB = 0.

**R06: Reserved**

Bit	Name	Initial	R/W	Description
Bit [7:0]	-	-	-	Reserve

**R07: Internal Function Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:6]	FRAD[1:0]	00b	R/W	Odd frame or Even frame advance control
Bit [5:4]	INVSL[1:0]	00b	R/W	Source Driving Mode Selection Register
Bit [3]	PAL	0b	(R) R/W	NTSC or PAL mode selection. <b>Only for 601 and 656 mode.</b> PAL = "0", Select NTSC interface mode. (Default mode) PAL = "1", Select PAL interface mode.
Bit [2]	PALM	0b	(R) R/W	PAL mode input data format selection PALM = "0", Select PAL 280 line mode. (Default mode) PALM = "1", Select PAL 288 line mode
Bit [1]	-	-	-	Reserve
Bit [0]	AVGY	0b	R/W	Average YUV interface Luminance Y. AVGY = "0"; Only used odd Y sample for YUV conversion, AVGY = "1"; Used odd and even Y sample for YUV conversion. This function active under YUV mode only!

**INVSL[1:0]**

INVSL1	INVSL0	Driving Mode	Notes
0	0	1 - Line Inversion	Default
0	1	2 - Line Inversion	
1	0	Frame Inversion	
1	1	Reserved	

**FRAD[1:0]**

FRAD1	FRAD0	Advance Frame	Notes	Unit: H
0	0	Default	Odd/Even frame Tstv are the same	
0	1	Odd frame	Even frame Tstv = HDLY setting +1	
1	0	Even frame	ODD frame Tstv = HDLY setting +1	
1	1	Reserve	Reserve	

**Note: Remark: This function is available under CCIR601 and CCIR656 mode only.**

**R08: Contrast Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:5]	-	-	-	Reserve
Bit [4:0]	CON[4:0]	08h	R/W	Display Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0) to 0x1F(level = 3.875) Default value 08h(level = 1.0)

**R09: Brightness Control Register**

Bit	Name	Initial	R/W	Description
Bit [7]	-	-	-	Reserve
Bit [6:0]	BRI[6:0]	40h	R/W	Display Brightness level adjustment register. (2/Step) Adjust range from 0x00(level = -128) to 0x7F(level = +126) Default value 0x40(level = +0)

**R0A: Hue and Saturation Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:4]	HUE[3:0]	08h	R/W	YUV Hue level adjustment register. (5 Deg/Step) Adjust range from 0x00(level = -40 Deg) to 0x0F(level = +35 Deg) Default value 0x08(level = 0 Deg) $Cb' = Cb * \cos \theta + Cr * \sin \theta$ $Cr' = Cr * \cos \theta + Cb * \sin \theta$
Bit [3:0]	SAT[3:0]	08h	R/W	YUV saturation level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0) to 0x0F(level = 1.875) Default value 0x08(level = 1.00)

**Note: Hue and Saturation function was available under YUV input mode only.**

**R0B: R / B Sub-Contrast Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:6]	SCONB[1:0]	02h	R/W	B Data Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0.75) to 0x0F(level = 1.125) Default value 08h(level = 1.0)
Bit [3:2]	SCONR[1:0]	02h	R/W	R Data Contrast level adjustment register. (0.125/Step) Adjust range from 0x00(level = 0.75) to 0x0F(level = 1.125) Default value 08h(level = 1.0)

**R0C: R Sub-Brightness Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:6]	-	-	-	Reserve
Bit [5:0]	SBRIR[5:0]	20h	R/W	R Data Brightness level adjustment register. (1/Step) Adjust range from 0x00(level = -32) to 0x3F(level = +31) Default value 20h(level = 0)

**R0D: B Sub-Brightness Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:6]	-	-	-	Reserve
Bit [5:0]	SBRIB[5:0]	20h	R/W	B Data Brightness level adjustment register. (1/Step) Adjust range from 0x00(level = -32) to 0x3F(level = +31) Default value 20h(level = 0)

**R0E: VCOMDC Level Control Register**

Bit	Name	Initial	R/W	Description
Bit [7]	-	-	-	Reserve
Bit [6]	OTP_BYPS	0h	R/W	VDCSL[5:0] data source selection register OTP_BYPS = "0", VDCSL[5:0] is read from OTP memory. OTP_BYPS = "1", VDCSL[5:0] is switch to the 3-wire register memory when user want to adjust the VCOMDC level for test propose. Refer to the "TRMEN" control register for the proper OTP write operation.
Bit [5:0]	VDCSL [5:0]	10h	R/W	VCOMDC level control register (20mV/Step @ VDDA = 5.0V) VDCSL[5:0] = 00h, VCOMDC = 1.00V VDCSL[5:0] = 01h, VCOMDC = 1.02V ..... VDCSL[5:0] = 10h, VCOMDC = 1.32V ..... VDCSL[5:0] = 3eh, VCOMDC = 2.24V VDCSL[5:0] = 3fh, VCOMDC = 2.26V

Note : .VCOMDC always keep 1.7V When VPSW = "1" . The OTP value effect in VPSW=0.  
The offset value is equal to 50mV in default level

**R0F VCOMAC Level Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:6]	VGLSL	10	R/W	VGLSL level control register VGLSL Level = 1V / Step
Bit [5:4]	VGHSL	10	R/W	VGHSL level control register VGHSL Level = 1V / Step
Bit [3:0]	VCACSL[3:0]	0100	R/W	VCOMAC level control register VCOMAC Level = 0.1V / Step @ VDDA = 5.0V

**VCACSL [3:0]**

VCSL3	VCSL2	VCSL1	VCSL0	Level (V)
0	0	0	0	4.6
0	0	0	1	4.7
0	0	1	0	4.8
0	0	1	1	4.9
0	1	0	0	5.0 (Default)
0	1	0	1	5.1
0	1	1	0	5.2
0	1	1	1	5.3
1	0	0	0	5.4
1	0	0	1	5.5
1	0	1	0	5.6
1	0	1	1	5.7
1	1	0	0	5.8
1	1	0	1	5.9
1	1	1	0	6.0
1	1	1	1	6.1

Note : When VPSW = "1". The register can't be used  
The offset value is equal to 100mV in default level

**VGHSL[5:4]**

VGHSL1	VGHSL0	VGH(V)
0	0	12
0	1	13
1	1	14
1	0	15

When VPSW = "1". The register can't be used

**VGLSL[7:6]**

VGHSL1	VGHSL0	VGL(V)
0	0	-7
0	1	-8
1	1	-9
1	0	-10

When VPSW = "1". The register can't be used

**R10: VGAM2 Level Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:5]	-	-	-	Reserve
Bit [4]	GAMEN	0b	R/W	GAMMA adjustment enable control register. (adjustable voltage for V2-V6) GAEN="0" or VSET = 1, Gamma correction disabled. GAEN="1" & VSET="0", Gamma correction enabled
Bit [3]	-	-	-	Reserve
Bit [2:0]	V2GAM [2:0]	100b	R/W	V2 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step

**R11: VGAM3/4 Level Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:6]	-	-	-	Reserve
Bit [5:3]	V4GAM [2:0]	100b	R/W	V4 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step
Bit [2:0]	V3GAM [2:0]	100b	R/W	V3 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step

**R12: VGAM5/6 Level Control Register**

Bit	Name	Initial	R/W	Description
Bit [10:6]	-	-	-	Reserve
Bit [5:3]	V6GAM [2:0]	100b	R/W	V6 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step
Bit [2:0]	V5GAM [2:0]	100b	R/W	V5 GAMMA voltage level setting. Function enabled when VSET="0" Adjust level = 22mV / Step

**V2GAM/ V3GAM/ V4GAM/ V5GAM./ V6GAM Level Control Register Setting Table**

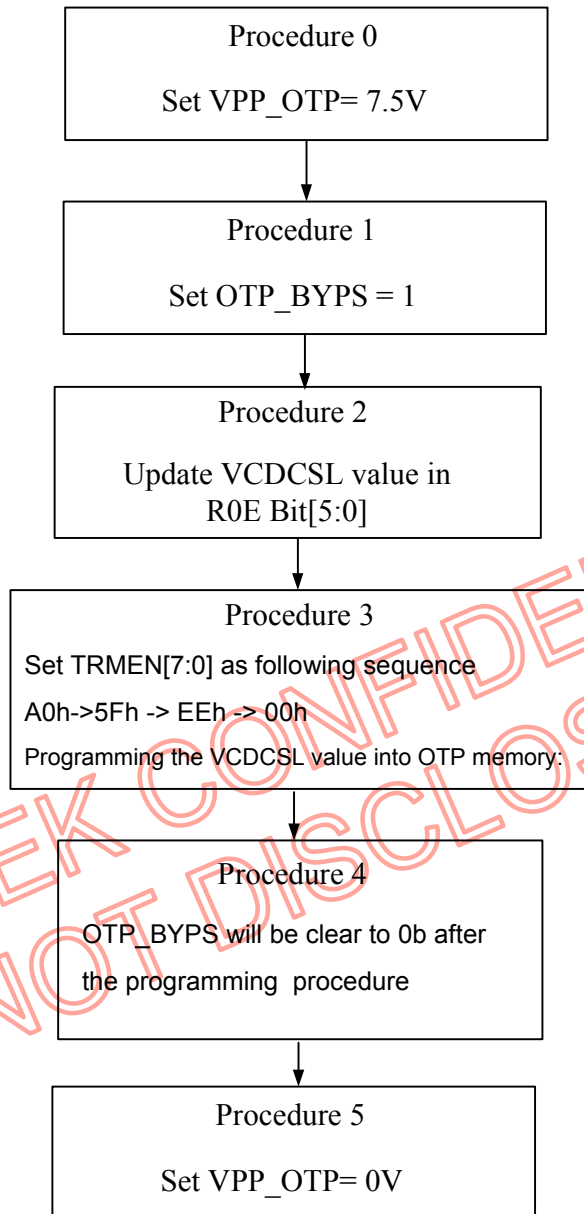
VxGMA2	VxGMA1	VxGMA0	Voltage level	Unit	Note
0	0	0	+88	mV	Refer to the Gamma Table for the default voltage level of V2 ~ V6
0	0	1	+66	mV	
0	1	0	+44	mV	
0	1	1	+22	mV	
1	0	0	+0(Default)	mV	
1	0	1	-22	mV	
1	1	0	-44	mV	
1	1	1	-66	mV	

Note: x = 2, 3, 4, 5, 6

**R1E: VCOMDC Trim Function Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:0]	TRMEN [7:0]	00b	R/W	VCOMDG Trim function control register Write the follow command sequentially to enable the VCOMDC trim function. Adjust VCDC level: Set TRMEN[7:0]=00h and write proper VCDCSL[5:0] value using 3-wire cmd. Programming the VCDCSL value into OTP memory: Set TRMEN[7:0] as following sequence A0h->5Fh -> EEh -> 00h OTP_BYPS will be clear to 0b after the programming procedure

Note: The Trim Block can be writing for only "2" times. Trim command exceed the limit may cause the VCOMDC output unknown value.


**R20: Wide and narrow display mode Control Register**

Bit	Name	Initial	R/W	Description
Bit [7:2]	-	-	-	Reserve
Bit [1:0]	WNSEL [1:0]	00b	R/W	Wide and narrow display mode select register

**WNSEL[1:0]: Wide and narrow display mode select register**

WNSEL1	WNSEL0	Display Mode
0	0	Normal display (Default)
0	1	Narrow display
1	0	Wide display
1	1	234-Line

Note: This function will be enabled under CCIR601 and CCIR656 mode

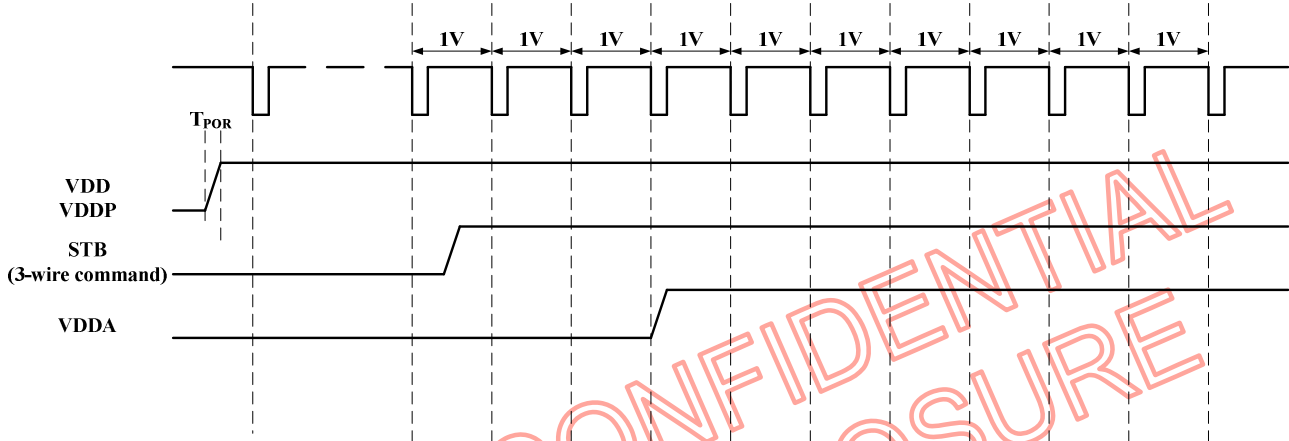


## Function Description

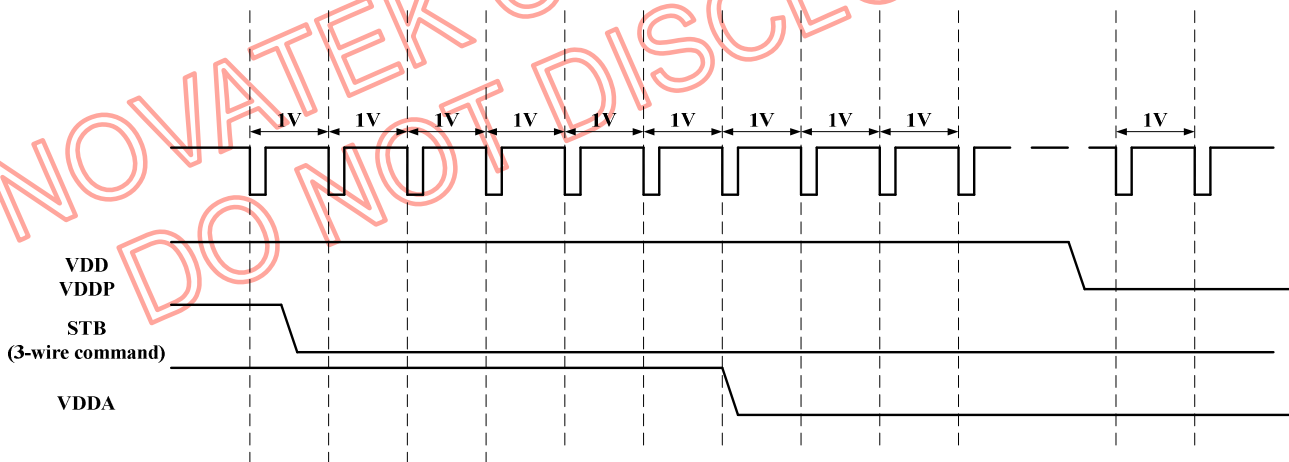
### Power On/Off Sequence

To prevent IC from power on reset fail, the rising time ( $T_{POR}$ ) of digital power supply VDD, should be control within the specification. Refer to the "AC Characteristic" for the detail timing, please.

#### Power-On Timing Sequence:



#### Power-off Timing Sequence:



### External Reset (RSTB)

To prevent from abnormal reset condition, a glitch filter for RSTB is embedded in this chip. The external reset signal should keep active for large then reset time ( $T_{RSTB}$ ). Refer to the AC/DC Specification for the requirement.

### Input Data VS Output Voltage

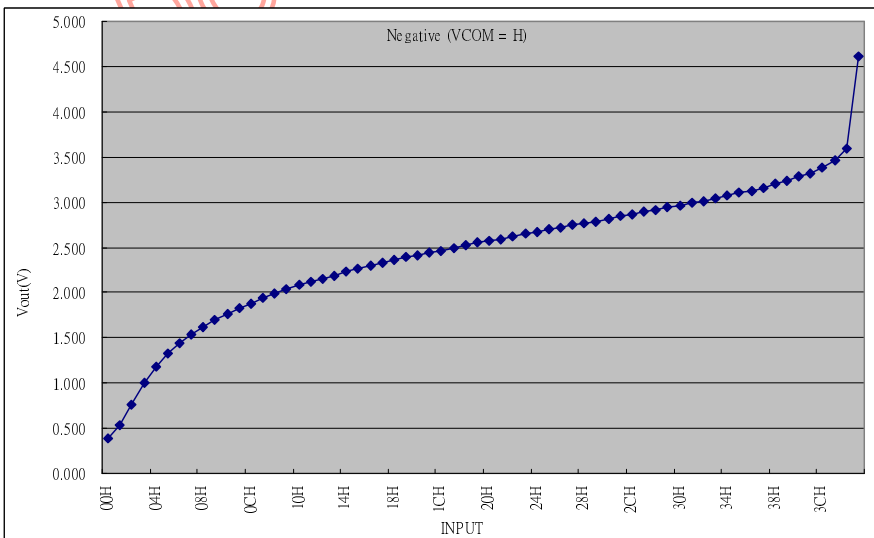
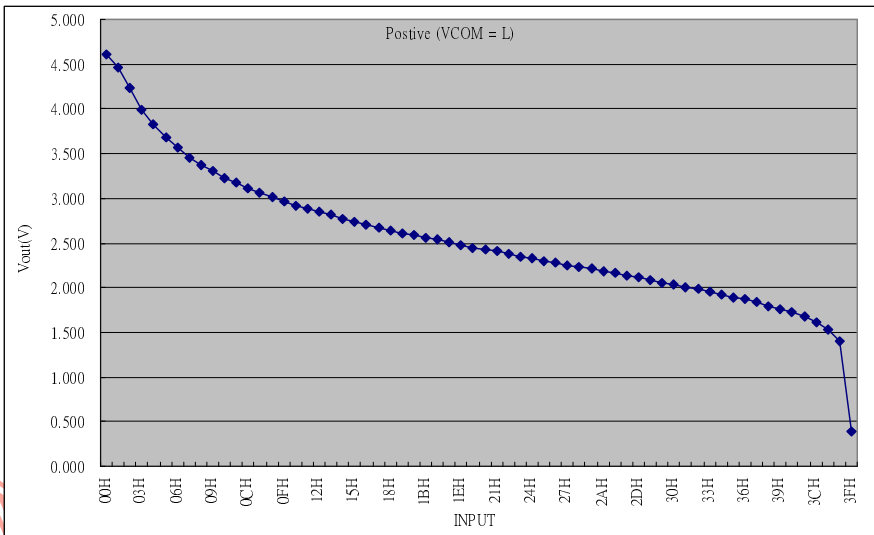
Source Driver data output sequence can be control by "SHLR".

Output	SO1	SO2	SO3	---	SO958	SO959	SO960
SHLR="1"	First data						Last data
SHLR="0"	Last data						First data

Gate Driver scan output sequence can be control by "UPDN".

Scan	GO1	GO2	GO3	---	GO238	GO239	GO240
UPDN="1"	First scan						Last scan
UPDN="0"	Last scan						First scan

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages to get the relative resistor value and voltage calculation method, please.



**Input Data and Output Voltage Reference Table (VSET = "0")**

@ VDDA = 5 V, VCOMOUT=L, POL=H	
Vno.	Unit = V
V1	4.610
V2	3.680
V3	3.115
V4	2.585
V5	2.185
V6	1.790
V7	0.390

@ VDDA = 5 V, VCOMOUT=H, POL=L	
Vno.	Unit = V
V1	0.390
V2	1.320
V3	1.885
V4	2.415
V5	2.815
V6	3.210
V7	4.610

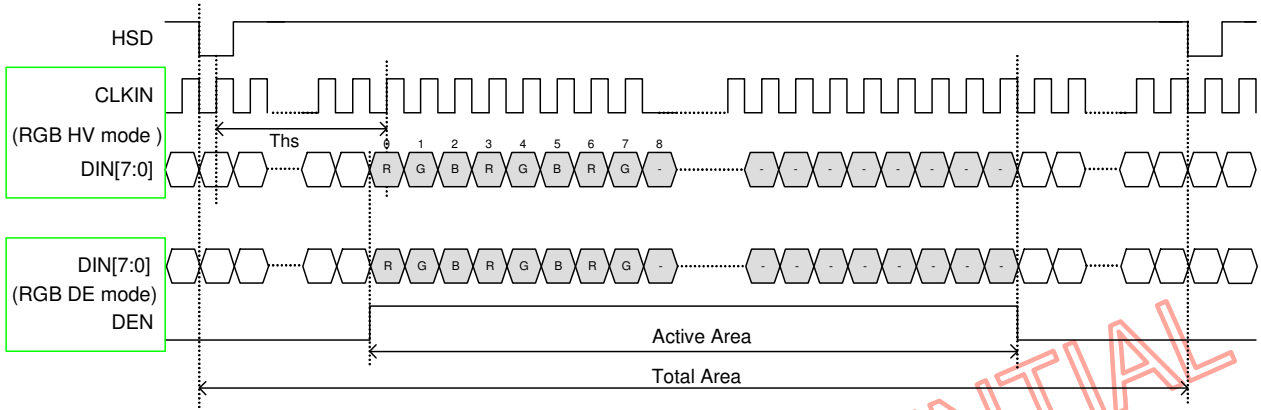
Data	VCOMOUT=H, POL=L
(V1) 00H	VDDA X 0.078
01H	VDDA X 0.107
02H	VDDA X 0.153
03H	VDDA X 0.201
04H	VDDA X 0.236
(V2) 05H	VDDA X 0.264
06H	VDDA X 0.288
07H	VDDA X 0.308
08H	VDDA X 0.325
09H	VDDA X 0.340
0AH	VDDA X 0.354
0BH	VDDA X 0.366
(V3) 0CH	VDDA X 0.377
0DH	VDDA X 0.388
0EH	VDDA X 0.398
0FH	VDDA X 0.408
10H	VDDA X 0.416
11H	VDDA X 0.424
12H	VDDA X 0.431
13H	VDDA X 0.438
14H	VDDA X 0.446
15H	VDDA X 0.453
16H	VDDA X 0.459
17H	VDDA X 0.465
18H	VDDA X 0.472
19H	VDDA X 0.478
(V4) 1AH	VDDA X 0.483
1BH	VDDA X 0.488
1CH	VDDA X 0.493
1DH	VDDA X 0.499
1EH	VDDA X 0.505
1FH	VDDA X 0.510
20H	VDDA X 0.514
21H	VDDA X 0.519
22H	VDDA X 0.525
23H	VDDA X 0.530
24H	VDDA X 0.535
25H	VDDA X 0.540
26H	VDDA X 0.545
27H	VDDA X 0.550
28H	VDDA X 0.554
29H	VDDA X 0.558
(V5) 2AH	VDDA X 0.563
2BH	VDDA X 0.568
2CH	VDDA X 0.573
2DH	VDDA X 0.578
2EH	VDDA X 0.583
2FH	VDDA X 0.588
30H	VDDA X 0.593
31H	VDDA X 0.598
32H	VDDA X 0.603
33H	VDDA X 0.609
34H	VDDA X 0.615
35H	VDDA X 0.621
36H	VDDA X 0.626
37H	VDDA X 0.632
(V6) 38H	VDDA X 0.642
39H	VDDA X 0.648
3AH	VDDA X 0.656
3BH	VDDA X 0.665
3CH	VDDA X 0.677
3DH	VDDA X 0.693
3EH	VDDA X 0.719
(V7) 3FH	VDDA X 0.922

Data	VCOMOUT=L, POL=H
(V1) 00H	VDDA X 0.922
01H	VDDA X 0.893
02H	VDDA X 0.847
03H	VDDA X 0.799
04H	VDDA X 0.764
(V2) 05H	VDDA X 0.736
06H	VDDA X 0.712
07H	VDDA X 0.692
08H	VDDA X 0.675
09H	VDDA X 0.660
0AH	VDDA X 0.646
0BH	VDDA X 0.634
(V3) 0CH	VDDA X 0.623
0DH	VDDA X 0.612
0EH	VDDA X 0.602
0FH	VDDA X 0.592
10H	VDDA X 0.584
11H	VDDA X 0.576
12H	VDDA X 0.569
13H	VDDA X 0.562
14H	VDDA X 0.554
15H	VDDA X 0.547
16H	VDDA X 0.541
17H	VDDA X 0.535
18H	VDDA X 0.528
19H	VDDA X 0.522
(V4) 1AH	VDDA X 0.517
1BH	VDDA X 0.512
1CH	VDDA X 0.507
1DH	VDDA X 0.501
1EH	VDDA X 0.495
1FH	VDDA X 0.490
20H	VDDA X 0.486
21H	VDDA X 0.481
22H	VDDA X 0.475
23H	VDDA X 0.470
24H	VDDA X 0.465
25H	VDDA X 0.460
26H	VDDA X 0.455
27H	VDDA X 0.450
28H	VDDA X 0.446
29H	VDDA X 0.442
(V5) 2AH	VDDA X 0.437
2BH	VDDA X 0.432
2CH	VDDA X 0.427
2DH	VDDA X 0.422
2EH	VDDA X 0.417
2FH	VDDA X 0.412
30H	VDDA X 0.407
31H	VDDA X 0.402
32H	VDDA X 0.397
33H	VDDA X 0.391
34H	VDDA X 0.385
35H	VDDA X 0.379
36H	VDDA X 0.374
37H	VDDA X 0.368
(V6) 38H	VDDA X 0.358
39H	VDDA X 0.352
3AH	VDDA X 0.344
3BH	VDDA X 0.335
3CH	VDDA X 0.323
3DH	VDDA X 0.307
3EH	VDDA X 0.281
(V7) 3FH	VDDA X 0.078

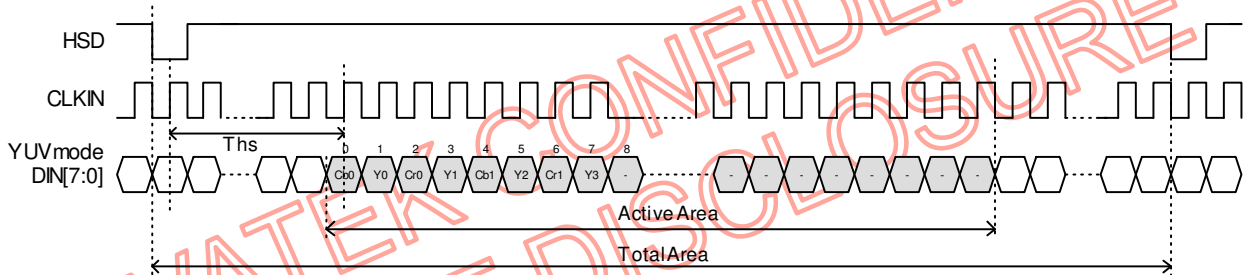
Note: Gamma Table will be difference for each custom. Contact to Novatek for the detail information, please.

## Data Input Format

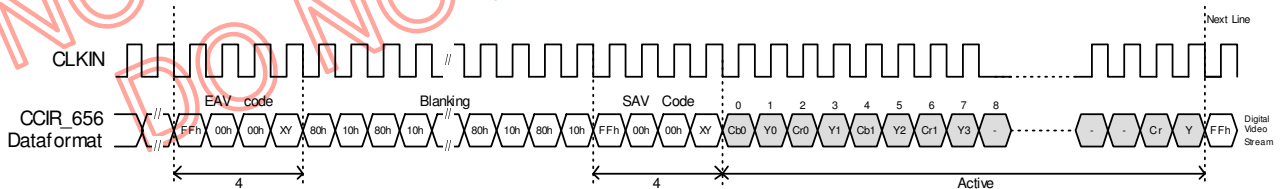
### 1. RGB input Data format



### 2. YUV input Data format



### 3. CCIR\_656 Mode Data format



### 4. Data Active Area

Input Format	Format Standard	CLKIN (MHz)	HSD (CLKIN)	Total Area (CLKIN)	Active Area (CLKIN)	Note
YUV	CCIR_601	27	1	1716	1440	
	CCIR_656			1728		
	CCIR_601	24.54	1	1560	1280	
8bit RGB	8 bit RGB	27	1	1716	960	960x240
24bit RGB	24 bit RGB	6.4	1	408	320	

**5. YUV\_601/656 to RGB conversion**

AVGY=0:

$$R_n = 1.164(Y_{2n-16}) + 1.596(C_{rn} - 128)$$

$$G_n = 1.164(Y_{2n-16}) - 0.813(C_{rn} - 128) - 0.392(C_{bn} - 128); [Y=16\sim 235, Cr \& Cb=16\sim 240]$$

$$B_n = 1.164(Y_{2n-16}) + 2.017(C_{bn} - 128)$$

AVGY=1:

$$R_n = 1.164((Y_{2n} + Y_{2n+1})/2 - 16) + 1.596(C_{rn} - 128)$$

$$G_n = 1.164((Y_{2n} + Y_{2n+1})/2 - 16) - 0.813(C_{rn} - 128) - 0.392(C_{bn} - 128); [Y=16\sim 235, Cr \& Cb=16\sim 240]$$

$$B_n = 1.164((Y_{2n} + Y_{2n+1})/2 - 16) + 2.017(C_{bn} - 128)$$

**6. Brightness / Contrast Adjustment**

Contrast:

$$G_n = G[7:0] \times \text{Contrast} (0 \text{ to } 3.875)$$

$$R_n = R[7:0] \times \text{Contrast} (0 \text{ to } 3.875) \times \text{Sub-Contrast } R (0.8 \text{ to } 1.175)$$

$$B_n = B[7:0] \times \text{Contrast} (0 \text{ to } 3.875) \times \text{Sub-Contrast } B (0.8 \text{ to } 1.175)$$

Brightness:

$$G_n = G[7:0] + \text{Brightness} (-128 \text{ to } +126)$$

$$R_n = R[7:0] + \text{Brightness} (-128 \text{ to } +126) + \text{Sub-Brightness } R (-32 \text{ to } +31)$$

$$B_n = B[7:0] + \text{Brightness} (-128 \text{ to } +126) + \text{Sub-Brightness } B (-32 \text{ to } +31)$$

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## Absolute Maximum Ratings

Logic supply voltage, VDD	-0.5V to +5V
Analog supply voltage, VDDA	-0.5V to +7.5V
Supply voltage, VDDP	-0.5V to +5.5V
Supply voltage, V1~ V6 VGH~VGL	-0.3 ~VDDA+0.3 -0.3~ +25V
Storage temperature	-55°C to +125°C
Operating temperature	-20°C to +85°C

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Electrical Characteristics

(For the digital circuit: Test Condition: VDD=VDDP=3.3V , VDDA=5.0V, GND=GND A=GNDP= 0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Digital Block Circuit</b>						
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	Digital power
Low Level Input Voltage	Vil	GND	-	0.2xVDD	V	Digital input pins TA=85°C
High Level Input Voltage	Vih	0.8xVDD	-	VDD	V	Digital input pins TA=85°C
Low Level Input Voltage	Vil	GND	-	0.2xVDD	V	Digital input pins TA=25°C
High Level Input Voltage	Vih	0.8xVDD	-	VDD	V	Digital input pins TA=25°C
Low Level Input Voltage	Vil	GND	-	0.1xVDD	V	Digital input pins TA= -20°C
High Level Input Voltage	Vih	0.9xVDD	-	VDD	V	Digital input pins TA= -20°C
Input Leakage Current	Ii	-	-	±1	µA	Digital input pins
Pull-high/low Impedance	Rin	-	200K	-	ohm	Digital control input pins
High Level Output Voltage	Voh	VDD-0.4	-	VDD	V	Digital output pins; loh = 400 uA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; lol = -400 uA
Digital Stand-by Current	Iddst	-	(50)	(100)	uA	No load, CLKIN/VSD/HSD stopped
Digital Operating Current	Idd1	-	2	-	mA	CLKIN = 27 MHz (CCIR601mode)
<b>Power Circuit</b>						
Charge Pump Supply Voltage	VDDP	3.0	3.3	3.6	V	For VGH/VGL power and Source Driver power, <b>must in this range</b>
VCOMAC output level	VCOMAC	4.6	-	6.1	V	By VCSL[2:0] setting VCOMAC = V(VCSL[2:0]) +- 100mV
VCOMDC output level	VCOMDC	1.0	-	2.26	V	By VCDCSL[5:0] setting VCOMDC = V(VCDCSL[5:0]) +- 50mV
Positive power supply	VGH	14.5	15	15.5	V	Gate driver load + procard load
Negative power supply	VGL	-9	-10	-11	V	Gate driver load + procard load
Base drive current	IDRV	-	-	10	mA	VDDP=3.3V, DRV=0.7 V
DRV output voltage	VDRV	GND +0.1	-	VDD -0.1	V	
Feed back voltage	VFB	0.55	0.6	0.65	V	DC/DC operating, VBL current=20 mA

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Analog Block Circuit</b>						
Analog Supply Voltage	VDDA	5.0	5.2	6.0	V	Analog circuit power from Power Block
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	Vo=0.1V ~ 0.5V & VDDA - 0.5 ~ VDDA - 0.1V
			±15	±25	mV	Vo=0.5V ~ VDDA-0.5V
Low-Level Output Current of VCOMOUT	IOLF	-	-10	-	mA	Force VCOMAC = 6.0V VCOMOUT output = 0V V.S. 0.9V
High-Level Output Current of VCOMOUT	IOHF	-	10	-	mA	Force VCOMAC = 6.0V VCOMOUT output = 6.0V V.S. 5.1V
Source Low-Level Output Current	I <sub>OLS</sub>	-	-30	-	uA	Son = Vo V.S. (Vo+0.9)
Source High-Level Output Current	I <sub>OHS</sub>	-	30	-	uA	Son = Vo V.S. (Vo-0.9)
Gate Low-Level Output Current	IOLG	-	-250	-	μA	GOn; Vo=VGL V.S. (VGL +0.5)
Gate High-Level Output Current	IOHG	-	250	-	μA	GOn; Vo=VGH V.S. (VGH -0.5)
Analog Stand-by Current	Iddast	-	-	100	μA	STBYB = "0", all function are shutdown
Analog Operating Current	Idda	-	10	-	mA	No load, CLKIN = 27MHz, Fld=15KHz

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## AC Electrical Characteristics

Test Condition: (VDD=VDDP=3.3V, VDDA=5.0V, GND=GND A=GNDP=0V, TA= 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>System Operation Timing</b>						
VDD power source slew time	T <sub>POR</sub>			1000	us	From 0V to 90% VDD
RSTB active pulse width	T <sub>RSTB</sub>	40			us	VDD = 3.3V
<b>Input Output Timing</b>						
CLKIN clock time	T <sub>clk</sub>	-		35.7	ns	CLKIN = 28MHz
HSD to CLKIN	T <sub>hc</sub>	-	-	1	CLKIN	
HSD width	T <sub>hwh</sub>	1	-	-	CLKIN	
VSD width	T <sub>vwh</sub>	1	-	-	Th	
HSD period time	T <sub>h</sub>	60	63.56	67	us	
VSD setup time	T <sub>vst</sub>	12	-	-	ns	
VSD hold time	T <sub>vhd</sub>	12	-	-	ns	
HSD setup time	T <sub>hst</sub>	12	-	-	ns	
HSD hold time	T <sub>hhd</sub>	12	-	-	ns	
Data set-up time	T <sub>dsu</sub>	12	-	-	ns	DIN[23:0] to CLKIN
Data hold time	T <sub>dhd</sub>	12	-	-	ns	DIN[23:0] to CLKIN
DEN setup time	T <sub>esd</sub>	12	-	-	ns	DEN to CLKIN
Time that VSD to 1 <sup>st</sup> line data input	T <sub>vs</sub>	2	13	127	Th	@CCIR601 / 8bit RGB HV mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Time that CCIR_V to 1 <sup>st</sup> line data input	T <sub>vs</sub>	12	20	28	Th	@CCIR656 NTSC mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Time that CCIR_V to 1 <sup>st</sup> line data input	T <sub>vs</sub>	17	25	33	Th	@CCIR656 PAL mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Time that VSD to 1 <sup>st</sup> line data input	T <sub>vs</sub>	2	13	127	Th	@24bit RGB HV mode Control by HDLY[6:0] setting T <sub>vs</sub> = HDLY[6:0]
Source output stable time 1	T <sub>st</sub>	-	25	30	us	96% final, CL=30pF, RL=2K
Gate output stable time	T <sub>gst</sub>	-	500	1000	ns	96% final, CL=40pF
VCOMOUT output stable time	T <sub>cst</sub>	-	4	8	us	96% final, CL=33nF, RL=100ohm
<b>3-wire serial communication AC timing</b>						
Serial clock	T <sub>spck</sub>	320	-	-	ns	
SPCK pulse duty	T <sub>scdut</sub>	40	50	60	%	
Serial data setup time	T <sub>isu</sub>	120	-	-	ns	
Serial data hold time	T <sub>ihd</sub>	120	-	-	ns	
Serial clock high/low	T <sub>ssw</sub>	120	-	-	ns	
Chip select distinguish	T <sub>cd</sub>	1	-	-	us	
SPENA to VSD	T <sub>cv</sub>	1	-	-	us	

## Timing Table

### CCIR601 Mode A/B \*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	24.54 /27		MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	40/37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from HSD to VCOMOUT	Thvcm	-	66	-	CLKIN	
Time from HSD to DATSEQ	Thseq	-	60	-	CLKIN	
Time from HSD to Gate output n line	Thgz		30	-	CLKIN	
Time from HSD to Gate output n+1 line	Thgo		100	-	CLKIN	
Time from HSD to 1'st data input (PAL)	Ths	128	264	-	CLKIN	DDLJ = 136, Offset = 128 (fixed)
Time from HSD to 1'st data input (NTSC)	Ths	128	244	-	CLKIN	DDLJ = 116, Offset = 128 (fixed)

### CCIR656 Mode A/B \*

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27		MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from EAV to VCOMOUT	Thvcm	-	66	-	CLKIN	
Time from EAV to DATSEQ	Thseq	-	60	-	CLKIN	
Time from HSD to Gate output n line	Thgz		30	-	CLKIN	
Time from HSD to Gate output n+1 line	Thgo		100	-	CLKIN	
Time from EAV to 1'st data input (PAL)	Ths	128	288	-	CLKIN	DDLJ = 152, Offset = 128 (fixed)
Time from EAV to 1'st data input (NTSC)	Ths	128	276	-	CLKIN	DDLJ = 140, Offset = 128 (fixed)

### 8 Bit RGB 960 CH Mode

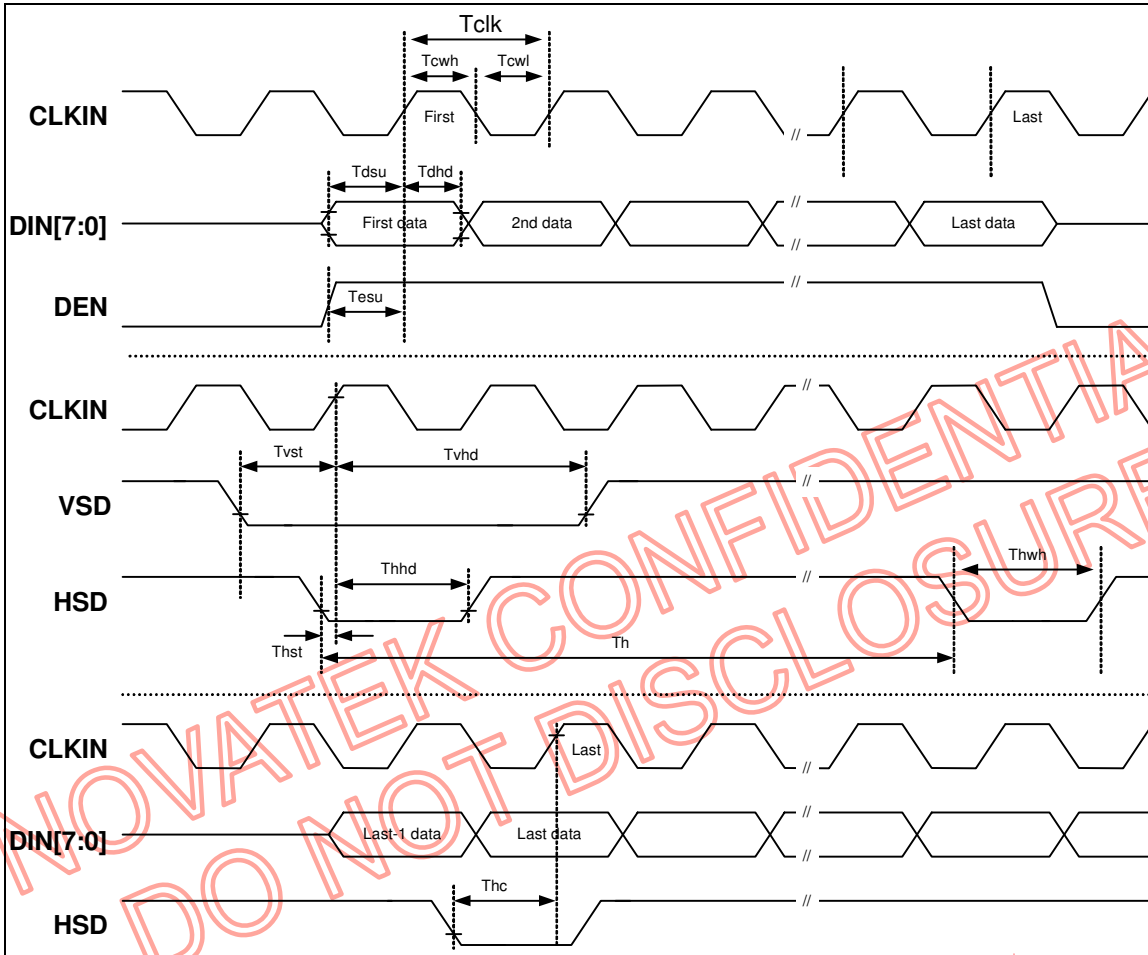
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	27		MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	37		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from HSD to VCOMOUT	Thvcm	-	25	-	CLKIN	
Time from HSD to DATSEQ	Thseq	-	20	-	CLKIN	
Time from HSD to Gate output n line	Thgz		5	-	CLKIN	
Time from HSD to Gate output n+1 line	Thgo		45	-	CLKIN	
Time that HSD to 1'st data input(NTSC)	Ths	35	70	255	CLKIN	DDLJ = 70, Offset = 0 (fixed)

### 24 Bit RGB Mode (@ SEL[3:0] = 1100 or 1101)

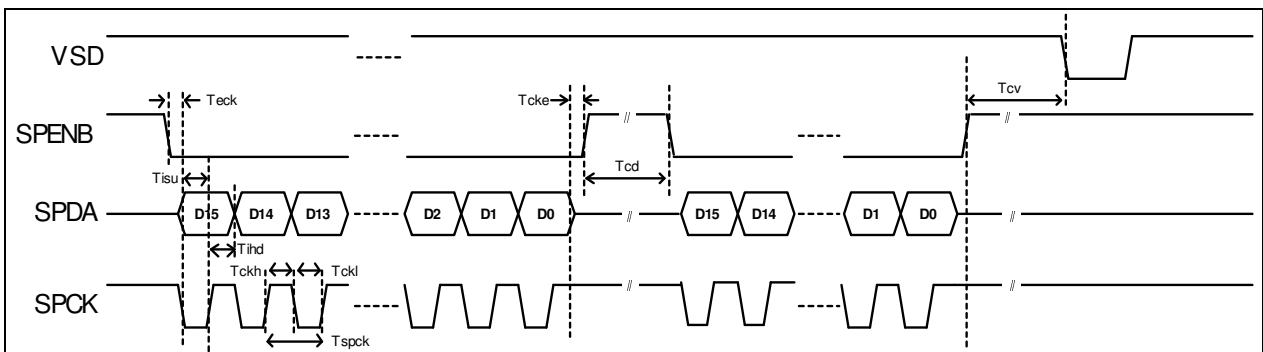
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLKIN frequency	Fclk	-	6.4		MHz	VDD = 3.0 ~3.6V
CLKIN cycle time	Tclk	-	156		ns	
CLKIN pulse duty	Tcwh	40	50	60	%	Tclk
Time from HSD to VCOMOUT	Thvcm	-	30	-	CLKIN	
Time from HSD to DATSEQ	Thseq	-	20	-	CLKIN	
Time from HSD to Gate output n line	Thgz		5	-	CLKIN	
Time from HSD to Gate output n+1 line	Thgo		45	-	CLKIN	
Time that HSD to 1'st data input(NTSC)	Ths	40	70	255	CLKIN	DDLJ = 70, Offset = 0 (fixed)

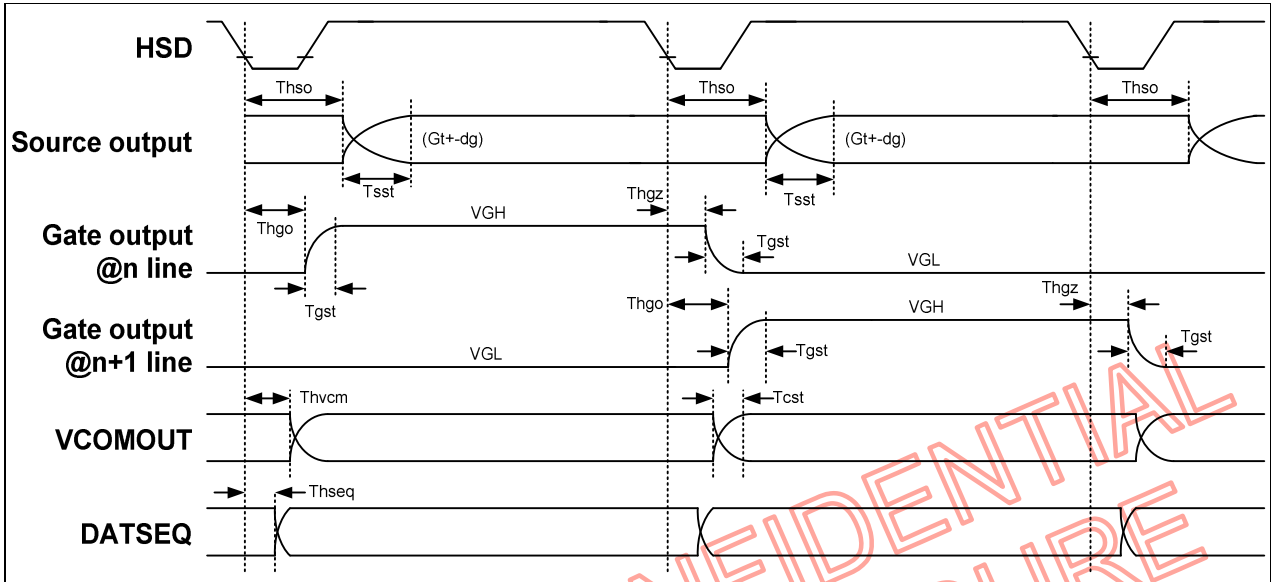
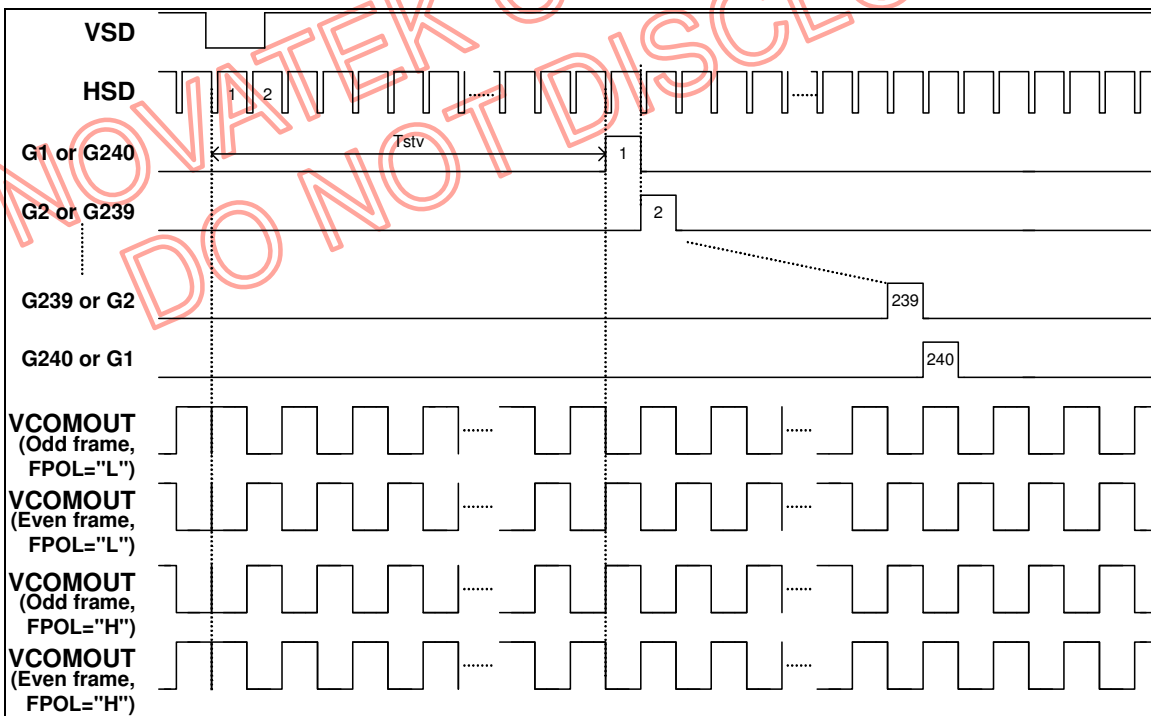
## Timing Diagram

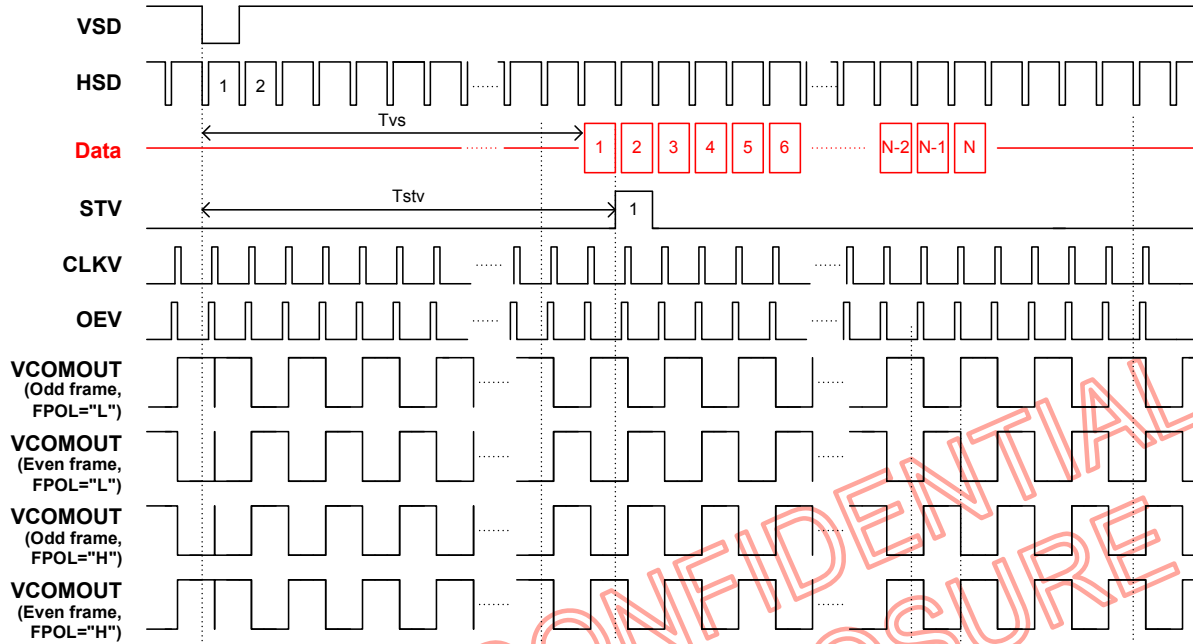
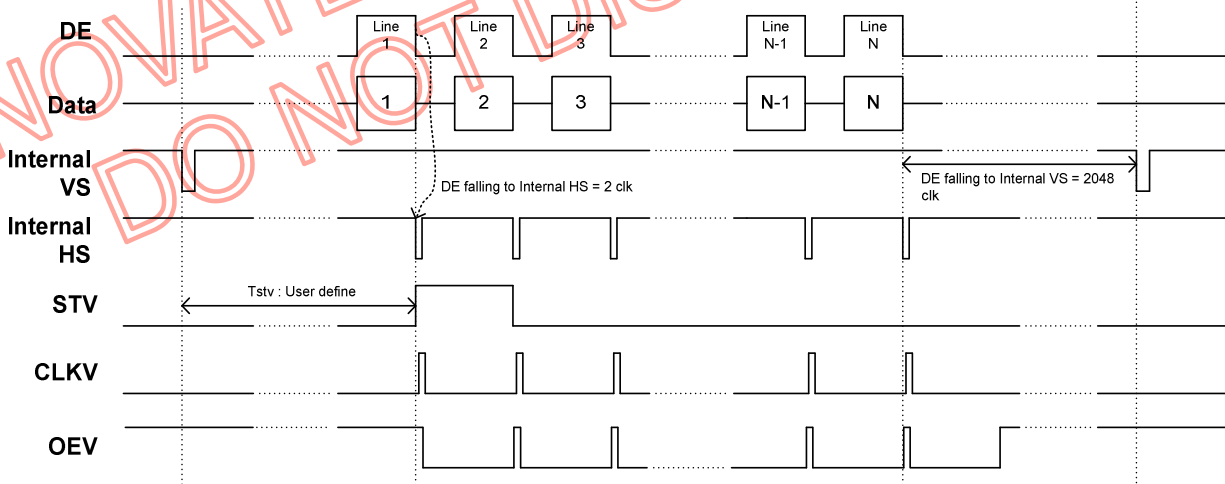
### Clock and Data Input Timing Diagram

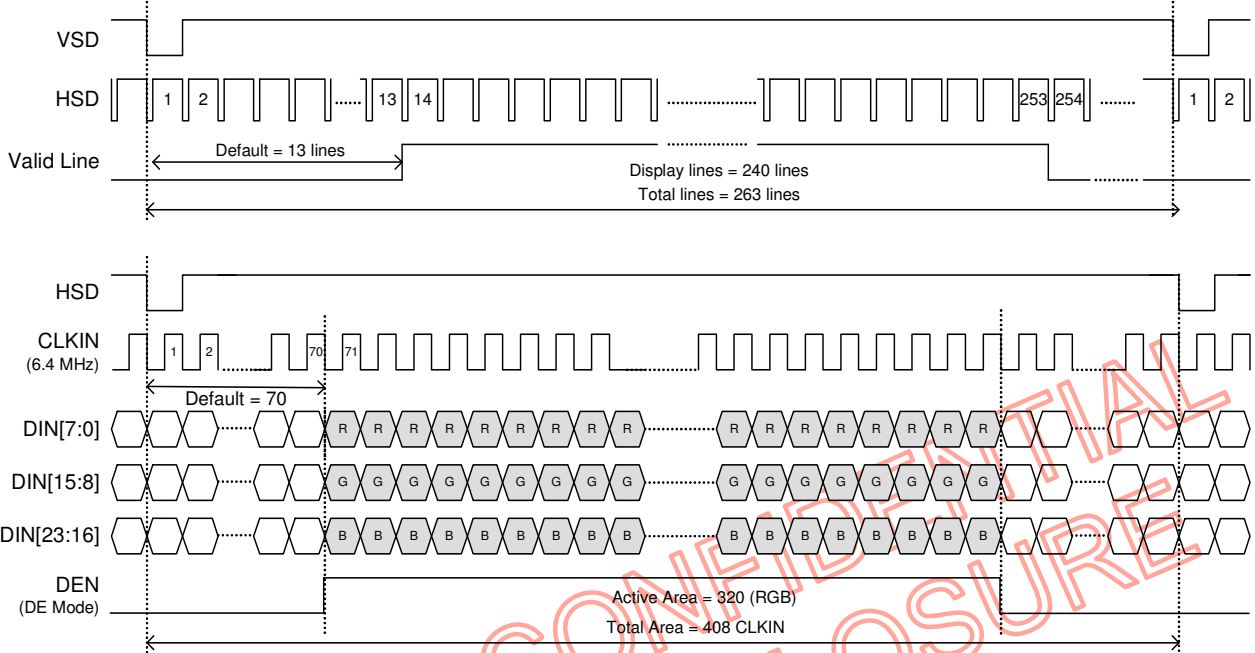


### 3-Wire Timing Diagram

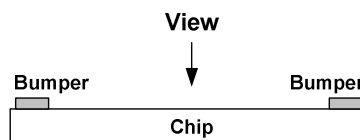
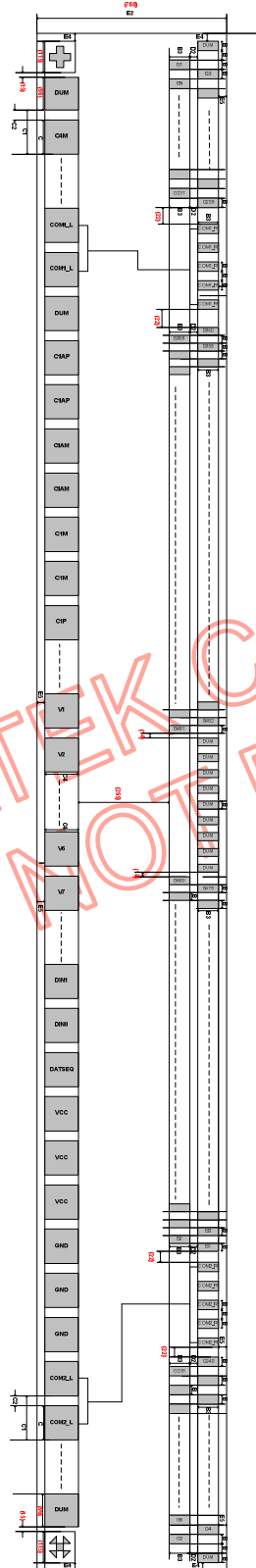


**Source Driver Output Timing Diagram**

**Gate Driver Output Timing Diagram**


**Vertical Timing Diagram (HV Mode)**

**Vertical Timing Diagram (DE Mode)**


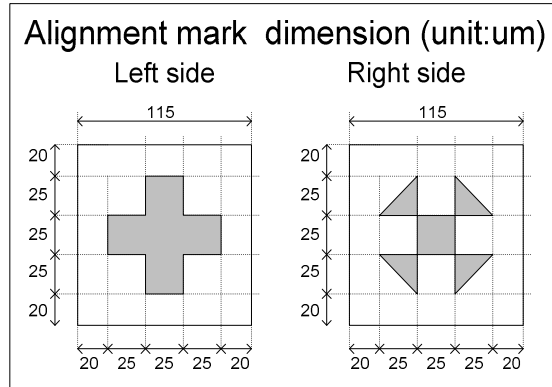
**Input Data Timing (24 bit RGB mode for 960 x 240 @ SEL[3:0] = 1100b)**


### Pad Location





### Alignment Mark



### Pad Information

Symbol	Dimension (um)
B	17
B3	110
C	100
C1	127
C2	27
C4	115
D2	30
E1	21310
E2	760
E4	65
E5	65

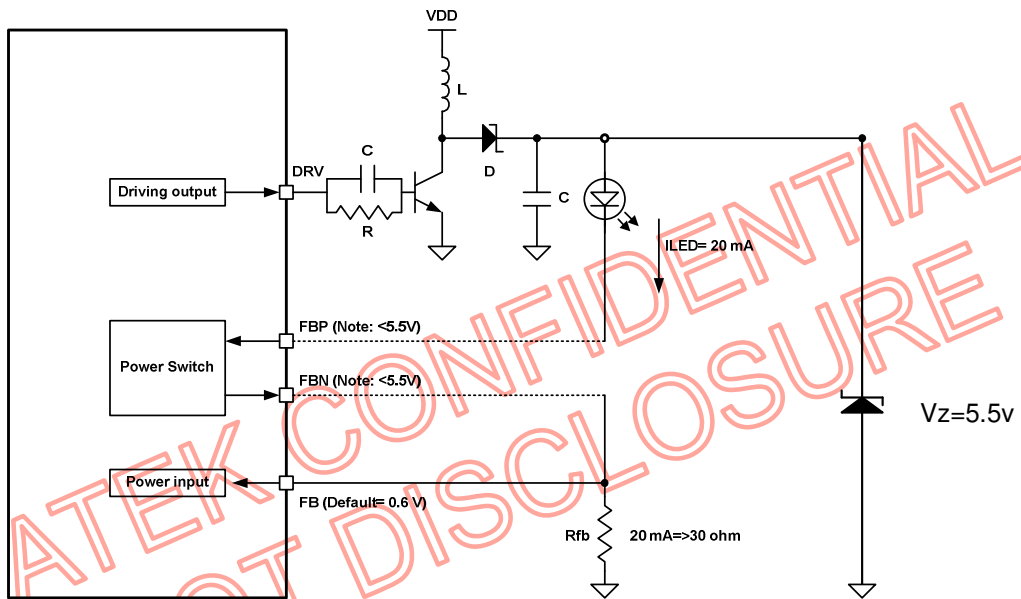
**\*Remark: Chip dimension include scribe line**

## Application Notes

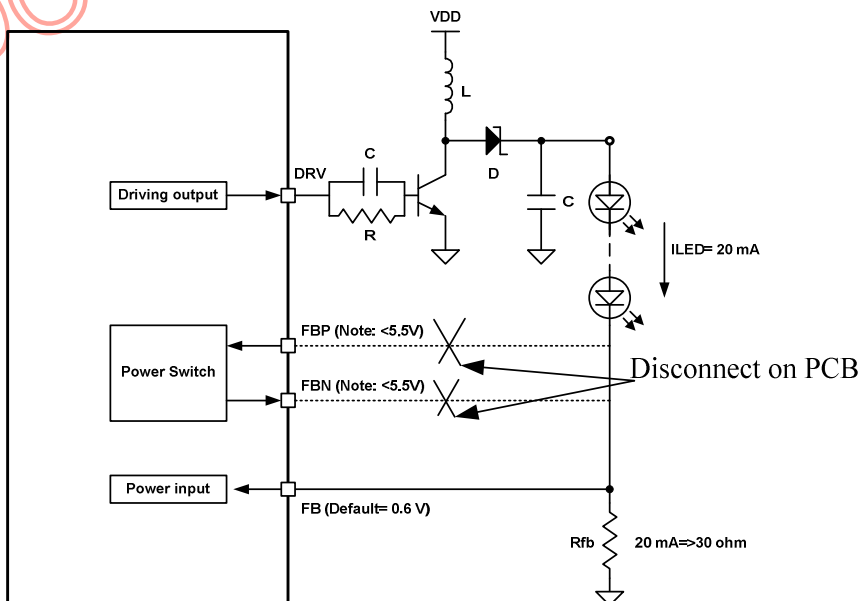
### PWM for LED Backlight Control

NT39016 using continuous analog type PWM control architecture for better performance. An auto protect detection feature was also integrated. The PWM circuit will enter power down state when the internal CKV signal is below 1KHz.

### Only one LED



### More than one LED



S







Preliminary Spec. for NT39016D  
TFT LCD Driver

Table with columns: Pad No., Name, X, Y, Pad No., Name, X, Y, Pad No., Name, X, Y, Pad No., Name, X, Y, Pad No., Name, X, Y. It lists various pad configurations for the NT39016D TFT LCD driver, including pad numbers, names, and X/Y coordinates.

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Pad No.	Name	X	Y
1321	GO133	-9425.5	120
1322	GO131	-9442.5	260
1323	GO129	-9459.5	120
1324	GO127	-9476.5	260
1325	GO125	-9493.5	120
1326	GO123	-9510.5	260
1327	GO121	-9527.5	120
1328	GO119	-9544.5	260
1329	GO117	-9561.5	120
1330	GO115	-9578.5	260
1331	GO113	-9595.5	120
1332	GO111	-9612.5	260
1333	GO109	-9629.5	120
1334	GO107	-9646.5	260
1335	GO105	-9663.5	120
1336	GO103	-9680.5	260
1337	GO101	-9697.5	120
1338	GO99	-9714.5	260
1339	GO97	-9731.5	120
1340	GO95	-9748.5	260
1341	GO93	-9765.5	120
1342	GO91	-9782.5	260
1343	GO89	-9799.5	120
1344	GO87	-9816.5	260
1345	GO85	-9833.5	120
1346	GO83	-9850.5	260
1347	GO81	-9867.5	120
1348	GO79	-9884.5	260
1349	GO77	-9901.5	120
1350	GO75	-9918.5	260
1351	GO73	-9935.5	120
1352	GO71	-9952.5	260
1353	GO69	-9969.5	120
1354	GO67	-9986.5	260
1355	GO65	-10003.5	120
1356	GO63	-10020.5	260
1357	GO61	-10037.5	120
1358	GO59	-10054.5	260
1359	GO57	-10071.5	120
1360	GO55	-10088.5	260
1361	GO53	-10105.5	120
1362	GO51	-10122.5	260
1363	GO49	-10139.5	120
1364	GO47	-10156.5	260
1365	GO45	-10173.5	120
1366	GO43	-10190.5	260
1367	GO41	-10207.5	120
1368	GO39	-10224.5	260
1369	GO37	-10241.5	120
1370	GO35	-10258.5	260
1371	GO33	-10275.5	120
1372	GO31	-10292.5	260
1373	GO29	-10309.5	120
1374	GO27	-10326.5	260
1375	GO25	-10343.5	120
1376	GO23	-10360.5	260
1377	GO21	-10377.5	120
1378	GO19	-10394.5	260
1379	GO17	-10411.5	120
1380	GO15	-10428.5	260
1381	GO13	-10445.5	120
1382	GO11	-10462.5	260
1383	GO9	-10479.5	120
1384	GO7	-10496.5	260
1385	GO5	-10513.5	120
1386	GO3	-10530.5	260
1387	GO1	-10547.5	120
1388	DUM	-10564.5	260

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