DATA SHEET

(DOC No. HX8353-D-DS)

HX8353-D

132RGB x 162 dots, 262K color,
with Internal GRAM,
TFT Mobile Single Chip Driver

Preliminary version 01 Apr, 2010

Himax Technologies, Inc.
http://www.himax.com.tw

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1. General Description

This manual is describes the Himax's HX8353-D 132RGB*162 dots resolution driving controller. The HX8353-D is designed to provide a single-chip solution that combined a gate driver, a source driver, power supply circuit, and internal graphics RAM for 262,144 colors to drive a TFT panel with 132RGB*162 dots at maximum.

The HX8353-D can be operated in low-voltage (1.65V) condition to the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8353-D also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8353-D is suitable for any small portable battery-driven product and requiring long-term driving capabilities, such as small PDAs, digital cellular phones and bi-directional pagers.

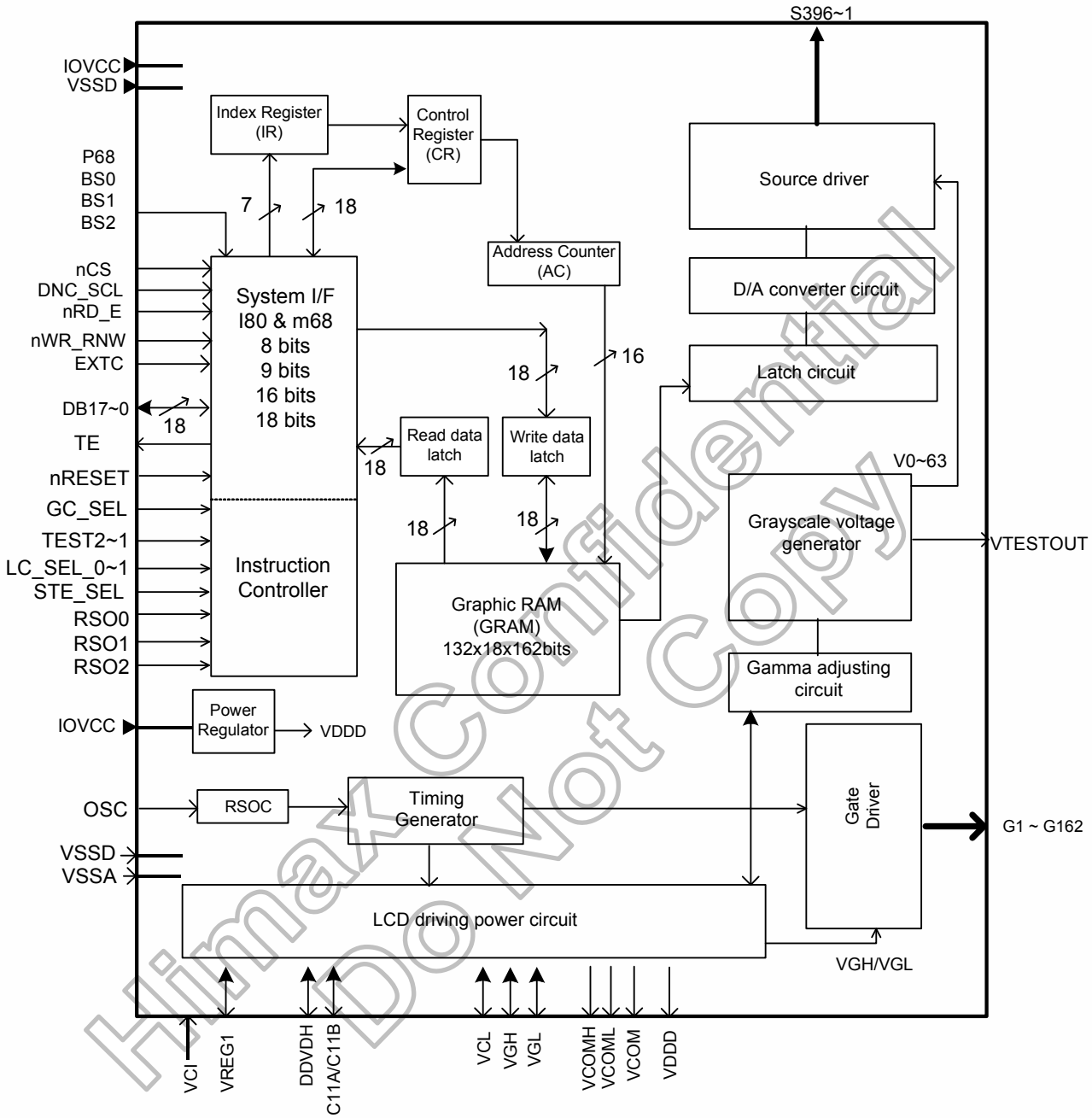
2. Features

- Single chip solution to drive a TFT panel
- 132RGB x 162-dot graphics display LCD controller/driver and 262,144 TFT colors
- Support resolution:
  - 132RGB x 162-dot: Display with 132 x 18-bits x 162 display RAM
  - 128RGB x 160-dot
    - Type 1: Display with 128 x 18-bits x 160 display RAM
    - Type 2: Display with 132 x 18-bits x 162 display RAM
  - 128RGB x 128-dot
  - 120RGB x 160-dot
  - 96RGB x 68-dot: Display with 96 x 18-bits x 68 display RAM
  - 96RGB x 64-dot
- Internal operation circuit of liquid crystal display:
  - Source channel: 396ch (132RGB)
  - Gate line: 162 Gate output
- Display mode (Color modes):
  - Full colors
    - 262k colors (18bit 6(R):6(G):6(B))
  - Reduce color mode:
    - 65k colors (16bit 5(R):6(G):5(B))
    - 4k colors (12bit 4(R):4(G):4(B))
    - 8 colors (Idle mode on): 8 colors (3 bit binary mode)
- Internal graphics RAM capacity: 132 x 162 x 18-bit = 0.38M bit:
- Support interface mode:
  - I80 System interface: 8-/9-/16-/18-bits bus
  - M68 System interface: 8-/9-/16- /18-bits bus
  - 3-/4- Wires Serial Data Transfer Interface
- Display features
  - Area scrolling
  - Partial display mode
  - Software programmable color depth mode
- On chip features:
  - DC/DC converter
  - OTP to store initialization register setting and MTP (Multi-time-programming)

non-volatile memory to store for VCM setting
- Oscillator for display clock generation
- Line inversion, frame inversion
- Support default value for factory use

- Low-power consumption architecture supports:
  - Logic supply voltage range for IOVCC to VSSD: 1.65 to 3.3V
  - Analog supply voltage range for VCI to VSSA: 2.5 to 3.3V
- Output voltage range:
  - DDVDH = 5.0 V for two time pump (Power supply for driver circuit range)
  - VREG1 = 3.3V to 4.8V (Source output voltage range)
  - VGH = +8.0 to +14.5V (Positive Gate output voltage range)
  - VGL = -5.0 to -12.5V (Negative Gate output voltage range)
  - VCOMH = 2.5V to 4.8V, 15mV/step (Common electrode output high voltage)
  - VCOML = -2.5V to 0.0V, 15mV/step (Common electrode output low voltage)
- Low power consumption, suitable for battery operated systems
- Suitable for all brand LCM module
  - Command set:
    - 128RGB x 160-dot
    - 132RGB x 162-dot
    - 120RGB x 160-dot
    - 96RGB x 68-dot
    - 96RGB x 64-dot
  - Himax defined command set
- CMOS compatible inputs
- Optimized layout for COG assembly
- Temperature range: -30℃ ~ 80℃

3. Block Diagram



4. Pin Description

4.1 Pin description

<table>
<tr><th colspan="5">Input Part</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>P68, BS2,BS1,BS0</td><td>I</td><td>4</td><td>VSSD/ IOVCC</td><td>Select the MPU interface mode as listed below
<table>
<tr><th>P68</th><th>BS2</th><th>BS1</th><th>BS0</th><th>Interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 80-system</td><td>DB17-DB8:Unused
DB7-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit bus interface, 80-system</td><td>DB17-DB16:Unused
DB15-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit bus interface, 80-system</td><td>DB17-DB9:Unused
DB8-DB0: Data</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>18-bit bus interface, 80-system</td><td>DB17-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>8-bit bus interface, 68-system</td><td>DB17-DB8:Unused
DB7-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>16-bit bus interface, 68-system</td><td>DB17-DB16:Unused
DB15-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>9-bit bus interface, 68-system</td><td>DB17-DB9:Unused
DB8-DB0: Data</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>18-bit bus interface, 68-system</td><td>DB17-DB0: Data</td></tr>
<tr><td>X</td><td>0</td><td>X</td><td>X</td><td>3-/4- wire serial interface</td><td>DB17-DB0:Unused
SDA: Data input/output</td></tr>
</table>
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>SPI_SEL</td><td>I</td><td>1</td><td>VSSD/ IOVCC</td><td>Interface format select pin
<table>
<tr><th>SPI_SEL</th><th>Serial Interface Format Selection</th></tr>
<tr><td>0</td><td>3-wire serial interface (default)</td></tr>
<tr><td>1</td><td>4-wire serial interface</td></tr>
</table>
If not used, connect it to VSSD.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed;
High: chip cannot be accessed.</td></tr>
<tr><td>DNC_SCL</td><td>I</td><td>1</td><td>MPU</td><td>The signal for command or parameter select under parallel mode(i.e. Not serial interface):
Low: command. High: parameter.
When under serial interface, it servers as SCL.</td></tr>
<tr><td>NRD_E</td><td>I</td><td>1</td><td>MPU</td><td>I80 system: Serves as a read signal and read data at the low level.
M68 system: 0: Read/Write disable, 1: Read/Write enable.
If not used, connected to IOVCC.</td></tr>
<tr><td>NWR_RNW</td><td>I</td><td>1</td><td>MPU</td><td>I80 system: Serves as a write signal and writes data at the rising edge.
M68 system: 0: Write, 1: Read.
4-wire SPI interface: 0: Command, 1: Data.
If not used, connected to IOVCC.</td></tr>
<tr><td>EXTC</td><td>I</td><td>1</td><td>VSSD/ IOVCC</td><td>Extended command set enable.
Low (VSSD): extended command set is discarded
High (IOVCC): extended command set is accepted
If not used, let it open or connected to VSSD.(weak pull low)</td></tr>
<tr><td>STE_SEL</td><td>I</td><td>1</td><td>VSSD/ IOVCC</td><td>This Pin is only valid for RSO[2:0]=3’b000.
Low (VSSD): Scrolling function enable and TE lines (162 lines)
High (IOVCC): Scrolling function disable and TE lines (160 lines)
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>GC_SEL</td><td>I</td><td>1</td><td>VSSD/ IOVCC</td><td>This signal is used to select gamma curve order.
Low (VSSD): GC0(1.0), GC1(2.5), GC2(2.2), GC3(1.8)
High (IOVCC): GC0(2.2), GC1(1.8), GC2(2.5), GC3(1.0)
Must be connected to VSSD or IOVCC.</td></tr>
</table>

<table>
<tr><th colspan="4">Input Part</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin Number</th><th>Connected with</th><th>Description</th></tr>
<tr><td>LC_SEL0~1</td><td>I</td><td>2</td><td>VSSD/ IOVCC</td><td>The selection pins of different liquid crystal type. Must be connected to VSSD or IOVCC.
<table>
<tr><th>LC_SEL1</th><th>LC_SEL0</th><th>Different liquid crystal type Selection</th></tr>
<tr><td>0</td><td>0</td><td>LC type 1</td></tr>
<tr><td>0</td><td>1</td><td>LC type 2</td></tr>
<tr><td>1</td><td>0</td><td>LC type 3</td></tr>
<tr><td>1</td><td>1</td><td>LC type 4</td></tr>
</table></td></tr>
<tr><td>RSO0~2</td><td>I</td><td>3</td><td>VSSD/ IOVCC</td><td>Resolution selection pins. RSO[2:0] is used for selecting resolution. Must be connected to VSSD or IOVCC.
<table>
<tr><th>RSO2</th><th>RSO1</th><th>RSO0</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GRAM resolution (Size): 132RGBX162
Display resolution:
Type1 :132RGBx162 (S1~S396 and G1~G162)
Type2 :128RGBx160 (S7~S390 and G2~G161)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GRAM resolution (Size): 128RGBx128
Display resolution:
128RGBx128 (S7~S390 and G2~G129)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>GRAM resolution (Size): 120RGBx160
Display resolution:
120RGBx160 (S7~S366, G2~G161)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>GRAM resolution (Size): 128RGBx160
Display resolution:
128RGBx160 (S7~S390 and G2~G161)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>GRAM resolution: 96RGBx68
Display resolution:
96RGBx68 (S55~S342, G1~G68)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>GRAM resolution: 96RGBx64
Display resolution:
96RGBx64 (S55~S342, G1~G64)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Setting disable</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Setting disable</td></tr>
</table></td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting this pin low initializes the LSI. Must be reset after power is supplied.</td></tr>
<tr><td>SS_PANEL</td><td>I</td><td>1</td><td>VSSD/ IOVCC</td><td>Input pin to select the source driver scan direction on panel module. Must be connected to VSSD or IOVCC.
<table>
<tr><th rowspan="2">SS_PANEL</th><th colspan="4">Module source output direction</th></tr>
<tr><th>RSO[2:0] =3’b100, 3’b101</th><th>RSO[2:0] =3’b010</th><th>RSO[2:0] =3’b000 (type2), 3’b001, 3’b011</th><th>RSO[2:0] =3’b000 (type1)</th></tr>
<tr><td>0</td><td>S55 -> S342</td><td>S7 -> S366</td><td>S7 -> S390</td><td>S1 -> S396</td></tr>
<tr><td>1</td><td>S342 -> S55</td><td>S366 -> S7</td><td>S390 -> S7</td><td>S396 -> S1</td></tr>
</table></td></tr>
<tr><td>GS_PANEL</td><td>I</td><td>1</td><td>VSSD/ IOVCC</td><td>Input pin to select the Gate driver scan direction on panel module. Must be connected to VSSD or IOVCC.
<table>
<tr><th rowspan="2">GS_PANEL</th><th colspan="5">Module Gate output direction</th></tr>
<tr><th>RSO[2:0] =3’b101</th><th>RSO[2:0] =3’b100</th><th>RSO[2:0] =3’b000 (type2), 3’b010, 3’b011</th><th>RSO[2:0] =3’b001</th><th>RSO[2:0] =3’b000 (type1)</th></tr>
<tr><td>0</td><td>G1 -> G64</td><td>G1 -> G68</td><td>G2 -> G161</td><td>G2 -> G129</td><td>G1 -> G162</td></tr>
<tr><td>1</td><td>G64 -> G1</td><td>G68 -> G1</td><td>G161 -> G2</td><td>G129 -> G2</td><td>G162 -> G1</td></tr>
</table></td></tr>
</table>

Input Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
REV_PANEL	I	1	VSSD/ IOVCC	Input pin to select the display reversion. Must be connected to VSSD or IOVCC. **REV_PANEL** / **Mapping data** 0 / "0" to maximum pixel voltage for normal white panel 1 / "0" to minimum pixel voltage for normal black panel
BGR_PANEL	I	1	VSSD/ IOVCC	Input pin to select the color mapping. Must be connected to VSSD or IOVCC. **BGR_PANEL** / **Color mapping** 0 / S1、S2、S3 filter order = R → G → B 1 / S1、S2、S3 filter order = B → G → R
TEST2-1	I	2	VSSD	Test pins. Let it open or connected to VSSD. (weak pull low)
OSC	I	1	Open or Connect to VSSD	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.

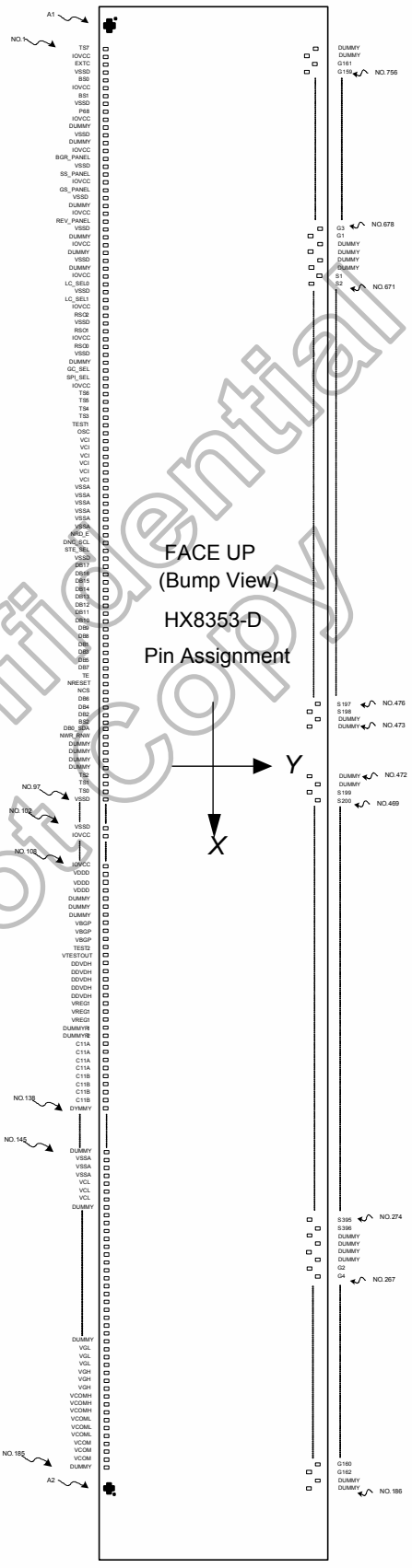
Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
S1~396	O	396	LCD	Output voltages applied to the liquid crystal. SS=0, ram address "0000" is output from S1. SS=1, ram address "0000" is output from S396. S1,S2,S3 ='R','G','B' (SS=0, BGR=0).
G1~162	O	162	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
VCOM	O	3	TFT common electrode	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. The alternation cycle can be set by the POL pin. Connect this pin to the common electrode in TFT panel.
VCOMH	O	3	Open	This pin indicates a high level of VCOM amplitude generated in driving the VCOM alternation. Let it open.
VCOML	O	3	Open	When the VCOM alternation is driven, this pin indicates a low level of VCOM amplitude. When the VCOMG bit is low, the VCOML output stops. Let it open.
VREG1	O	3	Open	Internal generated stable power for source driver. Let it open.
DDVDH	O	5	Stabilizing capacitor	An output from the step-up circuit1, of twice the VCI level. Connect to a stabilizing capacitor between VSSA and DDVDH.
VGH	O	3	Open	The step-up rate is determined with BT2-0 bits. Let it open.
VGL	O	3	Stabilizing capacitor	The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between VSSA and VGL.
VCL	O	3	Open	An output from the step-up circuit1. A negative voltage for VCOML circuit, VCL= -VCI. Let it open.
TE	O	1	MPU or open	A frame start pulse output (amplitude: IOVCC-VSSD). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it
VTESTOUT	O	1	Open	A test pin. Disconnect it.
VDDD	O	3	Open	Output from internal logic voltage. Let it open.
VBGP	O	3	Open	Reference voltage for power circuit. Let it open.
TS7~0	O	8	Open	Test pins. Let these pins open.

Input/Output Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
C11A,C11B	I/O	4,4	Stabilizing capacitor	Connect a pump capacitor between C11A and C11B.
Dummy35 ~ 40	I/O	3,3	Open	Dummy pads. Please open these pins.
Dummy23 ~ 34	I/O	3,3 3,3	Open	Dummy pads. Please open these pins.
DB0_SDA DB1~17	I/O	18	MPU	When Operates in system interface mode, it is used liked an 18-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0 For serial interface, this pin (SDA) is for serial data pin when operate on serial data transfer interface mode of Command-parameter Interface mode. Data would be latched on the rising edge of the SCL signal. Let unused data pins open or pulled Gnd or pulled IOVCC.
DUMMY	-	39	Open	Dummy pads. Disconnect them.
DUMMYR1~R2	-	2	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip.

Power Part				
Signals	**I/O**	**Pin Number**	**Connected with**	**Description**
IOVCC	P	17	Power supply	Power supply for interface pin. IOVCC = 1.65 ~3.3 V.
VSSD	P	17	Power supply	Ground for the logic side. VSSD = 0V
VSSA	P	9	Power supply	Analog ground. VSSA = 0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VCI	P	6	Power supply	A power supply for the analog circuit. VCI = 2.5 ~ 3.3V

4.2 Pin assignment

Chip size : 9900um x 675um
Including : Seal-ring : 4um * 2
Scribe line : 40um * 2
Chip thickness : 250um(typ.)/350um
Pad coordinate : PAD center
Coordinate Origin : Chip Center
Au Bump Size
Bump height tolerance +/- 3um
Bump size tolerance :
Output bump width : 16 +/- 2um
Output bump length : 98 +/- 3um
Input bump width : 35/40 +/- 3um
Input bump length : 90 +/- 3um
Au bump height : 12um +/- 3um
Numbers in the figure corresponds to pad coordinate numbers
Alignment Mark
Arrangement : Two places
A1 : Coordinate(X,Y)=(-4841,-220)
A2 : Coordinate(X,Y)=(4841,-220)



4.3 PAD coordinates

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	TS7	-4750	-231	61	VSSA	-1750	-231	121	DDVDH	1550	-231	181	VCOML	4550	-231
2	IOVCC	-4700	-231	62	VSSA	-1700	-231	122	DDVDH	1600	-231	182	VCOM	4600	-231
3	EXTC	-4650	-231	63	NRD_E	-1630	-231	123	DDVDH	1650	-231	183	VCOM	4650	-231
4	VSSD	-4600	-231	64	DNC_SCL	-1570	-231	124	DDVDH	1700	-231	184	VCOM	4700	-231
5	BS0	-4550	-231	65	STE_SEL	-1510	-231	125	VREG1	1750	-231	185	DUMMY	4750	-231
6	IOVCC	-4500	-231	66	VSSD	-1450	-231	126	VREG1	1800	-231	186	DUMMY	4772	110
7	BS1	-4450	-231	67	DB17	-1390	-231	127	VREG1	1850	-231	187	DUMMY	4756	227
8	VSSD	-4400	-231	68	DB16	-1330	-231	128	DUMMYR1	1900	-231	188	G162	4740	110
9	P68	-4350	-231	69	DB15	-1270	-231	129	DUMMYR2	1950	-231	189	G160	4724	227
10	IOVCC	-4300	-231	70	DB14	-1210	-231	130	C11A	2000	-231	190	G158	4708	110
11	DUMMY	-4250	-231	71	DB13	-1150	-231	131	C11A	2050	-231	191	G156	4692	227
12	VSSD	-4200	-231	72	DB12	-1090	-231	132	C11A	2100	-231	192	G154	4676	110
13	DUMMY	-4150	-231	73	DB11	-1030	-231	133	C11A	2150	-231	193	G152	4660	227
14	IOVCC	-4100	-231	74	DB10	-970	-231	134	C11B	2200	-231	194	G150	4644	110
15	BGR_PANEL	-4050	-231	75	DB9	-910	-231	135	C11B	2250	-231	195	G148	4628	227
16	VSSD	-4000	-231	76	DB8	-850	-231	136	C11B	2300	-231	196	G146	4612	110
17	SS_PANEL	-3950	-231	77	DB1	-790	-231	137	C11B	2350	-231	197	G144	4596	227
18	IOVCC	-3900	-231	78	DB3	-730	-231	138	DUMMY	2400	-231	198	G142	4580	110
19	GS_PANEL	-3850	-231	79	DB5	-670	-231	139	DUMMY	2450	-231	199	G140	4564	227
20	VSSD	-3800	-231	80	DB7	-610	-231	140	DUMMY	2500	-231	200	G138	4548	110
21	DUMMY	-3750	-231	81	TE	-550	-231	141	DUMMY	2550	-231	201	G136	4532	227
22	IOVCC	-3700	-231	82	NRESET	-490	-231	142	DUMMY	2600	-231	202	G134	4516	110
23	REV_PANEL	-3650	-231	83	NCS	-430	-231	143	DUMMY	2650	-231	203	G132	4500	227
24	VSSD	-3600	-231	84	DB6	-370	-231	144	DUMMY	2700	-231	204	G130	4484	110
25	DUMMY	-3550	-231	85	DB4	-310	-231	145	DUMMY	2750	-231	205	G128	4468	227
26	IOVCC	-3500	-231	86	DB2	-250	-231	146	VSSA	2800	-231	206	G126	4452	110
27	DUMMY	-3450	-231	87	BS2	-190	-231	147	VSSA	2850	-231	207	G124	4436	227
28	VSSD	-3400	-231	88	DB0_SDA	-130	-231	148	VSSA	2900	-231	208	G122	4420	110
29	DUMMY	-3350	-231	89	NWR_RNW	-70	-231	149	VCL	2950	-231	209	G120	4404	227
30	IOVCC	-3300	-231	90	DUMMY	0	-231	150	VCL	3000	-231	210	G118	4388	110
31	LC_SEL0	-3250	-231	91	DUMMY	50	-231	151	VCL	3050	-231	211	G116	4372	227
32	VSSD	-3200	-231	92	DUMMY	100	-231	152	DUMMY23	3100	-231	212	G114	4356	110
33	LC_SEL1	-3150	-231	93	DUMMY	150	-231	153	DUMMY24	3150	-231	213	G112	4340	227
34	IOVCC	-3100	-231	94	TS2	200	-231	154	DUMMY25	3200	-231	214	G110	4324	110
35	RSO2	-3050	-231	95	TS1	250	-231	155	DUMMY26	3250	-231	215	G108	4308	227
36	VSSD	-3000	-231	96	TS0	300	-231	156	DUMMY27	3300	-231	216	G106	4292	110
37	RSO1	-2950	-231	97	VSSD	350	-231	157	DUMMY28	3350	-231	217	G104	4276	227
38	IOVCC	-2900	-231	98	VSSD	400	-231	158	DUMMY29	3400	-231	218	G102	4260	110
39	RSO0	-2850	-231	99	VSSD	450	-231	159	DUMMY30	3450	-231	219	G100	4244	227
40	VSSD	-2800	-231	100	VSSD	500	-231	160	DUMMY31	3500	-231	220	G98	4228	110
41	DUMMY	-2750	-231	101	VSSD	550	-231	161	DUMMY32	3550	-231	221	G96	4212	227
42	GC_SEL	-2700	-231	102	VSSD	600	-231	162	DUMMY33	3600	-231	222	G94	4196	110
43	SPI_SEL	-2650	-231	103	IOVCC	650	-231	163	DUMMY34	3650	-231	223	G92	4180	227
44	IOVCC	-2600	-231	104	IOVCC	700	-231	164	DUMMY35	3700	-231	224	G90	4164	110
45	TS6	-2550	-231	105	IOVCC	750	-231	165	DUMMY36	3750	-231	225	G88	4148	227
46	TS5	-2500	-231	106	IOVCC	800	-231	166	DUMMY37	3800	-231	226	G86	4132	110
47	TS4	-2450	-231	107	IOVCC	850	-231	167	DUMMY38	3850	-231	227	G84	4116	227
48	TS3	-2400	-231	108	IOVCC	900	-231	168	DUMMY39	3900	-231	228	G82	4100	110
49	TEST1	-2350	-231	109	VDDD	950	-231	169	DUMMY40	3950	-231	229	G80	4084	227
50	OSC	-2300	-231	110	VDDD	1000	-231	170	VGL	4000	-231	230	G78	4068	110
51	VCI	-2250	-231	111	VDDD	1050	-231	171	VGL	4050	-231	231	G76	4052	227
52	VCI	-2200	-231	112	DUMMY	1100	-231	172	VGL	4100	-231	232	G74	4036	110
53	VCI	-2150	-231	113	DUMMY	1150	-231	173	VGH	4150	-231	233	G72	4020	227
54	VCI	-2100	-231	114	DUMMY	1200	-231	174	VGH	4200	-231	234	G70	4004	110
55	VCI	-2050	-231	115	VBGP	1250	-231	175	VGH	4250	-231	235	G68	3988	227
56	VCI	-2000	-231	116	VBGP	1300	-231	176	VCOMH	4300	-231	236	G66	3972	110
57	VSSA	-1950	-231	117	VBGP	1350	-231	177	VCOMH	4350	-231	237	G64	3956	227
58	VSSA	-1900	-231	118	TEST2	1400	-231	178	VCOMH	4400	-231	238	G62	3940	110
59	VSSA	-1850	-231	119	VTESTOUT	1450	-231	179	VCOML	4450	-231	239	G60	3924	227
60	VSSA	-1800	-231	120	DDVDH	1500	-231	180	VCOML	4500	-231	240	G58	3908	110

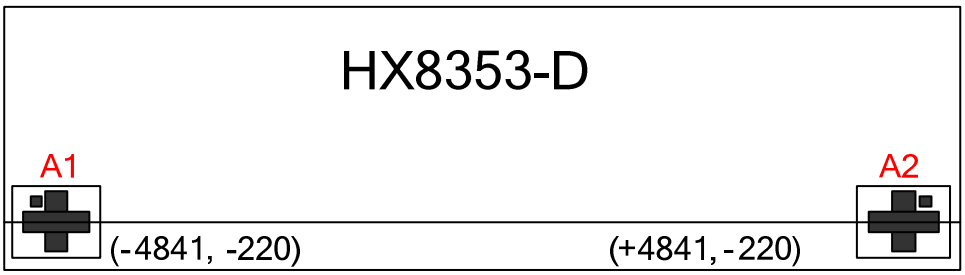
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
241	G56	3892	227	301	S368	2932	227	361	S308	1972	227	421	S248	1012	227
242	G54	3876	110	302	S367	2916	110	362	S307	1956	110	422	S247	996	110
243	G52	3860	227	303	S366	2900	227	363	S306	1940	227	423	S246	980	227
244	G50	3844	110	304	S365	2884	110	364	S305	1924	110	424	S245	964	110
245	G48	3828	227	305	S364	2868	227	365	S304	1908	227	425	S244	948	227
246	G46	3812	110	306	S363	2852	110	366	S303	1892	110	426	S243	932	110
247	G44	3796	227	307	S362	2836	227	367	S302	1876	227	427	S242	916	227
248	G42	3780	110	308	S361	2820	110	368	S301	1860	110	428	S241	900	110
249	G40	3764	227	309	S360	2804	227	369	S300	1844	227	429	S240	884	227
250	G38	3748	110	310	S359	2788	110	370	S299	1828	110	430	S239	868	110
251	G36	3732	227	311	S358	2772	227	371	S298	1812	227	431	S238	852	227
252	G34	3716	110	312	S357	2756	110	372	S297	1796	110	432	S237	836	110
253	G32	3700	227	313	S356	2740	227	373	S296	1780	227	433	S236	820	227
254	G30	3684	110	314	S355	2724	110	374	S295	1764	110	434	S235	804	110
255	G28	3668	227	315	S354	2708	227	375	S294	1748	227	435	S234	788	227
256	G26	3652	110	316	S353	2692	110	376	S293	1732	110	436	S233	772	110
257	G24	3636	227	317	S352	2676	227	377	S292	1716	227	437	S232	756	227
258	G22	3620	110	318	S351	2660	110	378	S291	1700	110	438	S231	740	110
259	G20	3604	227	319	S350	2644	227	379	S290	1684	227	439	S230	724	227
260	G18	3588	110	320	S349	2628	110	380	S289	1668	110	440	S229	708	110
261	G16	3572	227	321	S348	2612	227	381	S288	1652	227	441	S228	692	227
262	G14	3556	110	322	S347	2596	110	382	S287	1636	110	442	S227	676	110
263	G12	3540	227	323	S346	2580	227	383	S286	1620	227	443	S226	660	227
264	G10	3524	110	324	S345	2564	110	384	S285	1604	110	444	S225	644	110
265	G8	3508	227	325	S344	2548	227	385	S284	1588	227	445	S224	628	227
266	G6	3492	110	326	S343	2532	110	386	S283	1572	110	446	S223	612	110
267	G4	3476	227	327	S342	2516	227	387	S282	1556	227	447	S222	596	227
268	G2	3460	110	328	S341	2500	110	388	S281	1540	110	448	S221	580	110
269	DUMMY	3444	227	329	S340	2484	227	389	S280	1524	227	449	S220	564	227
270	DUMMY	3428	110	330	S339	2468	110	390	S279	1508	110	450	S219	548	110
271	DUMMY	3412	227	331	S338	2452	227	391	S278	1492	227	451	S218	532	227
272	DUMMY	3396	110	332	S337	2436	110	392	S277	1476	110	452	S217	516	110
273	S396	3380	227	333	S336	2420	227	393	S276	1460	227	453	S216	500	227
274	S395	3364	110	334	S335	2404	110	394	S275	1444	110	454	S215	484	110
275	S394	3348	227	335	S334	2388	227	395	S274	1428	227	455	S214	468	227
276	S393	3332	110	336	S333	2372	110	396	S273	1412	110	456	S213	452	110
277	S392	3316	227	337	S332	2356	227	397	S272	1396	227	457	S212	436	227
278	S391	3300	110	338	S331	2340	110	398	S271	1380	110	458	S211	420	110
279	S390	3284	227	339	S330	2324	227	399	S270	1364	227	459	S210	404	227
280	S389	3268	110	340	S329	2308	110	400	S269	1348	110	460	S209	388	110
281	S388	3252	227	341	S328	2292	227	401	S268	1332	227	461	S208	372	227
282	S387	3236	110	342	S327	2276	110	402	S267	1316	110	462	S207	356	110
283	S386	3220	227	343	S326	2260	227	403	S266	1300	227	463	S206	340	227
284	S385	3204	110	344	S325	2244	110	404	S265	1284	110	464	S205	324	110
285	S384	3188	227	345	S324	2228	227	405	S264	1268	227	465	S204	308	227
286	S383	3172	110	346	S323	2212	110	406	S263	1252	110	466	S203	292	110
287	S382	3156	227	347	S322	2196	227	407	S262	1236	227	467	S202	276	227
288	S381	3140	110	348	S321	2180	110	408	S261	1220	110	468	S201	260	110
289	S380	3124	227	349	S320	2164	227	409	S260	1204	227	469	S200	244	227
290	S379	3108	110	350	S319	2148	110	410	S259	1188	110	470	S199	228	110
291	S378	3092	227	351	S318	2132	227	411	S258	1172	227	471	DUMMY	212	227
292	S377	3076	110	352	S317	2116	110	412	S257	1156	110	472	DUMMY	196	110
293	S376	3060	227	353	S316	2100	227	413	S256	1140	227	473	DUMMY	-196	110
294	S375	3044	110	354	S315	2084	110	414	S255	1124	110	474	DUMMY	-212	227
295	S374	3028	227	355	S314	2068	227	415	S254	1108	227	475	S198	-228	110
296	S373	3012	110	356	S313	2052	110	416	S253	1092	110	476	S197	-244	227
297	S372	2996	227	357	S312	2036	227	417	S252	1076	227	477	S196	-260	110
298	S371	2980	110	358	S311	2020	110	418	S251	1060	110	478	S195	-276	227
299	S370	2964	227	359	S310	2004	227	419	S250	1044	227	479	S194	-292	110
300	S369	2948	110	360	S309	1988	110	420	S249	1028	110	480	S193	-308	227

No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
481	S192	-324	110	541	S132	-1284	110	601	S72	-2244	110	661	S12	-3204	110
482	S191	-340	227	542	S131	-1300	227	602	S71	-2260	227	662	S11	-3220	227
483	S190	-356	110	543	S130	-1316	110	603	S70	-2276	110	663	S10	-3236	110
484	S189	-372	227	544	S129	-1332	227	604	S69	-2292	227	664	S9	-3252	227
485	S188	-388	110	545	S128	-1348	110	605	S68	-2308	110	665	S8	-3268	110
486	S187	-404	227	546	S127	-1364	227	606	S67	-2324	227	666	S7	-3284	227
487	S186	-420	110	547	S126	-1380	110	607	S66	-2340	110	667	S6	-3300	110
488	S185	-436	227	548	S125	-1396	227	608	S65	-2356	227	668	S5	-3316	227
489	S184	-452	110	549	S124	-1412	110	609	S64	-2372	110	669	S4	-3332	110
490	S183	-468	227	550	S123	-1428	227	610	S63	-2388	227	670	S3	-3348	227
491	S182	-484	110	551	S122	-1444	110	611	S62	-2404	110	671	S2	-3364	110
492	S181	-500	227	552	S121	-1460	227	612	S61	-2420	227	672	S1	-3380	227
493	S180	-516	110	553	S120	-1476	110	613	S60	-2436	110	673	DUMMY	-3396	110
494	S179	-532	227	554	S119	-1492	227	614	S59	-2452	227	674	DUMMY	-3412	227
495	S178	-548	110	555	S118	-1508	110	615	S58	-2468	110	675	DUMMY	-3428	110
496	S177	-564	227	556	S117	-1524	227	616	S57	-2484	227	676	DUMMY	-3444	227
497	S176	-580	110	557	S116	-1540	110	617	S56	-2500	110	677	G1	-3460	110
498	S175	-596	227	558	S115	-1556	227	618	S55	-2516	227	678	G3	-3476	227
499	S174	-612	110	559	S114	-1572	110	619	S54	-2532	110	679	G5	-3492	110
500	S173	-628	227	560	S113	-1588	227	620	S53	-2548	227	680	G7	-3508	227
501	S172	-644	110	561	S112	-1604	110	621	S52	-2564	110	681	G9	-3524	110
502	S171	-660	227	562	S111	-1620	227	622	S51	-2580	227	682	G11	-3540	227
503	S170	-676	110	563	S110	-1636	110	623	S50	-2596	110	683	G13	-3556	110
504	S169	-692	227	564	S109	-1652	227	624	S49	-2612	227	684	G15	-3572	227
505	S168	-708	110	565	S108	-1668	110	625	S48	-2628	110	685	G17	-3588	110
506	S167	-724	227	566	S107	-1684	227	626	S47	-2644	227	686	G19	-3604	227
507	S166	-740	110	567	S106	-1700	110	627	S46	-2660	110	687	G21	-3620	110
508	S165	-756	227	568	S105	-1716	227	628	S45	-2676	227	688	G23	-3636	227
509	S164	-772	110	569	S104	-1732	110	629	S44	-2692	110	689	G25	-3652	110
510	S163	-788	227	570	S103	-1748	227	630	S43	-2708	227	690	G27	-3668	227
511	S162	-804	110	571	S102	-1764	110	631	S42	-2724	110	691	G29	-3684	110
512	S161	-820	227	572	S101	-1780	227	632	S41	-2740	227	692	G31	-3700	227
513	S160	-836	110	573	S100	-1796	110	633	S40	-2756	110	693	G33	-3716	110
514	S159	-852	227	574	S99	-1812	227	634	S39	-2772	227	694	G35	-3732	227
515	S158	-868	110	575	S98	-1828	110	635	S38	-2788	110	695	G37	-3748	110
516	S157	-884	227	576	S97	-1844	227	636	S37	-2804	227	696	G39	-3764	227
517	S156	-900	110	577	S96	-1860	110	637	S36	-2820	110	697	G41	-3780	110
518	S155	-916	227	578	S95	-1876	227	638	S35	-2836	227	698	G43	-3796	227
519	S154	-932	110	579	S94	-1892	110	639	S34	-2852	110	699	G45	-3812	110
520	S153	-948	227	580	S93	-1908	227	640	S33	-2868	227	700	G47	-3828	227
521	S152	-964	110	581	S92	-1924	110	641	S32	-2884	110	701	G49	-3844	110
522	S151	-980	227	582	S91	-1940	227	642	S31	-2900	227	702	G51	-3860	227
523	S150	-996	110	583	S90	-1956	110	643	S30	-2916	110	703	G53	-3876	110
524	S149	-1012	227	584	S89	-1972	227	644	S29	-2932	227	704	G55	-3892	227
525	S148	-1028	110	585	S88	-1988	110	645	S28	-2948	110	705	G57	-3908	110
526	S147	-1044	227	586	S87	-2004	227	646	S27	-2964	227	706	G59	-3924	227
527	S146	-1060	110	587	S86	-2020	110	647	S26	-2980	110	707	G61	-3940	110
528	S145	-1076	227	588	S85	-2036	227	648	S25	-2996	227	708	G63	-3956	227
529	S144	-1092	110	589	S84	-2052	110	649	S24	-3012	110	709	G65	-3972	110
530	S143	-1108	227	590	S83	-2068	227	650	S23	-3028	227	710	G67	-3988	227
531	S142	-1124	110	591	S82	-2084	110	651	S22	-3044	110	711	G69	-4004	110
532	S141	-1140	227	592	S81	-2100	227	652	S21	-3060	227	712	G71	-4020	227
533	S140	-1156	110	593	S80	-2116	110	653	S20	-3076	110	713	G73	-4036	110
534	S139	-1172	227	594	S79	-2132	227	654	S19	-3092	227	714	G75	-4052	227
535	S138	-1188	110	595	S78	-2148	110	655	S18	-3108	110	715	G77	-4068	110
536	S137	-1204	227	596	S77	-2164	227	656	S17	-3124	227	716	G79	-4084	227
537	S136	-1220	110	597	S76	-2180	110	657	S16	-3140	110	717	G81	-4100	110
538	S135	-1236	227	598	S75	-2196	227	658	S15	-3156	227	718	G83	-4116	227
539	S134	-1252	110	599	S74	-2212	110	659	S14	-3172	110	719	G85	-4132	110
540	S133	-1268	227	600	S73	-2228	227	660	S13	-3188	227	720	G87	-4148	227

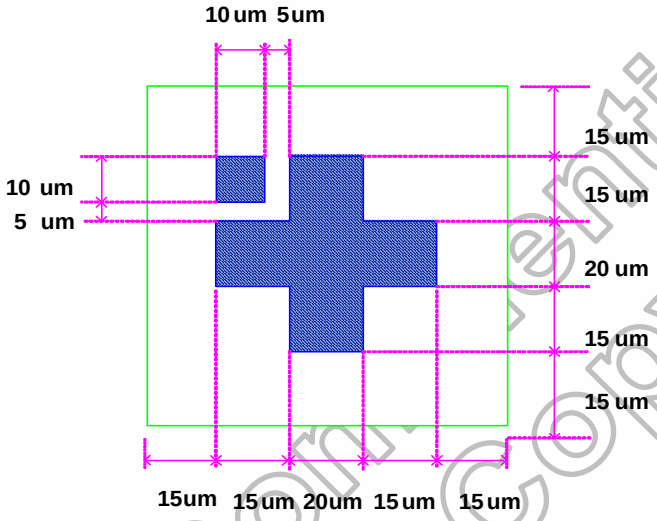
No.	Name	X	Y
721	G89	-4164	110
722	G91	-4180	227
723	G93	-4196	110
724	G95	-4212	227
725	G97	-4228	110
726	G99	-4244	227
727	G101	-4260	110
728	G103	-4276	227
729	G105	-4292	110
730	G107	-4308	227
731	G109	-4324	110
732	G111	-4340	227
733	G113	-4356	110
734	G115	-4372	227
735	G117	-4388	110
736	G119	-4404	227
737	G121	-4420	110
738	G123	-4436	227
739	G125	-4452	110
740	G127	-4468	227
741	G129	-4484	110
742	G131	-4500	227
743	G133	-4516	110
744	G135	-4532	227
745	G137	-4548	110
746	G139	-4564	227
747	G141	-4580	110
748	G143	-4596	227
749	G145	-4612	110
750	G147	-4628	227
751	G149	-4644	110
752	G151	-4660	227
753	G153	-4676	110
754	G155	-4692	227
755	G157	-4708	110
756	G159	-4724	227
757	G161	-4740	110
758	DUMMY	-4756	227
759	DUMMY	-4772	110

Alignment mark	X	Y
A1	-4841	-220
A2	4841	-220

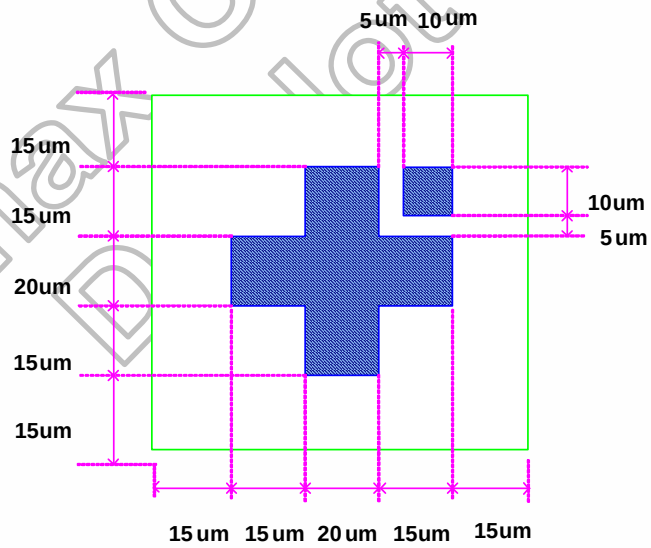
4.4 Alignment mark



A_MARK (A1)

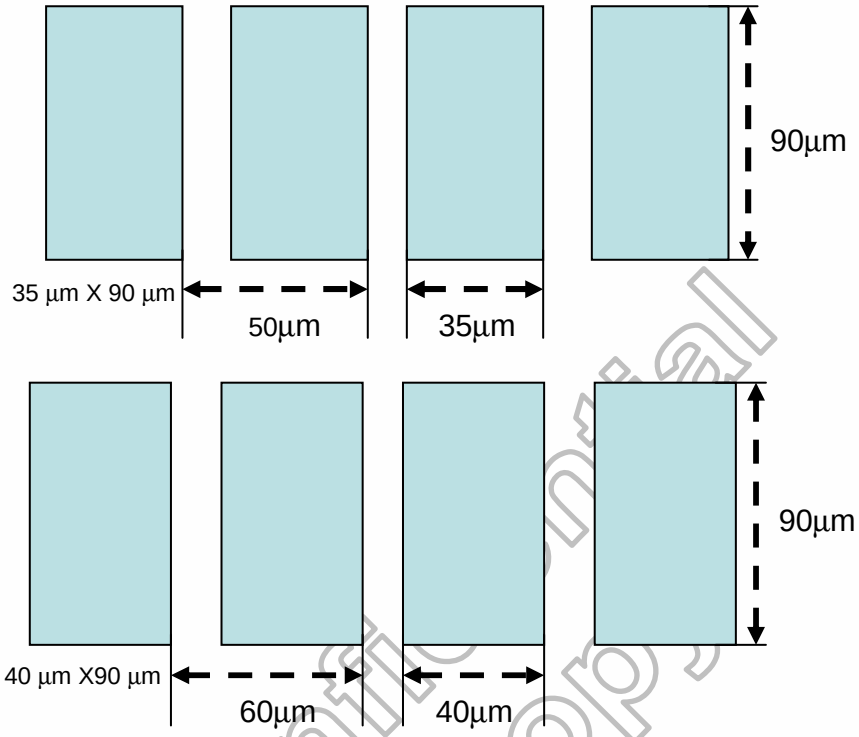


A_MARK (A2)



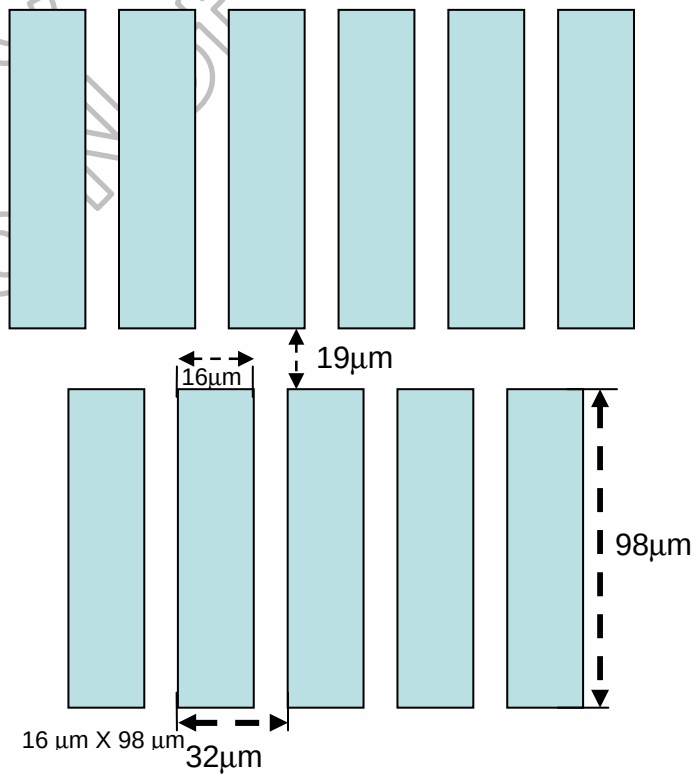
4.5 Bump size

Input/Output PAD



Note: 35µmX90µm : Pad no. 1~62
Pad no. 90~185
40µmX90µm: Pad no. 63~89

Output PAD



Note: 16µmX98µm : Pad no.186~759

5. Interface

5.1 System interface

The HX8353-D supports parallel 80-system and 68-system 18-/16-/9-/8-bits bus interface mode and 3-/4- wires serial interface mode. When NCS = “L”, the parallel and serial bus system interface of the HX8353-D become active and data transfer through the interface circuit is available. The DNC_SCL pin specifies whether the system interface circuit access is to the register command or to the GRAM. The input bus width format of system interface circuit is selected by external pins BS2-0. For selecting the format of input bus, please refer to Table 5.1 and Table 5.2.

The HX8353-D includes command code and the following parameter and GRAM data. The command code can be written through data bus by setting DNC_SCL=0. Then the command or GRAM data can be written to register at which that index pointer pointed by setting DNC_SCL=1.

Furthermore, there are two 18-bit bus control registers used to temporarily store the data written to or read from the GRAM. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM. Therefore, the first read data operation is invalid and the following read data operations are valid.

SPI_SEL	P68	BS2	BS1	BS0	Interface
x	0	1	0	0	80-system 8-bit Parallel
x	0	1	0	1	80-system 16-bit Parallel
x	0	1	1	0	80-system 9-bit Parallel
x	0	1	1	1	80-system 18-bit Parallel
x	1	1	0	0	68-system 8-bit Parallel
x	1	1	0	1	68-system 16-bit Parallel
x	1	1	1	0	68-system 9-bit Parallel
x	1	1	1	1	68-system 18-bit Parallel
0	x	0	x	x	3 wire serial Interface only
1	x	0	x	x	4 wire serial Interface only

Table 5.1 Interface selection

Interface	NRD_E	NWR_RNW	DNC_SCL	DB17 – DB0	
				Command/Parameter	GRAM
80-system 8-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB7-DB0
80-system 9-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB8-DB0
80-system 16-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB15-DB0
80-system 18-bit Parallel	NRD	NWR	DNC	DB7-DB0	DB17-DB0
3 wire serial Interface	-	-	SCL	DB0 as SDA	
68-system 8-bit Parallel	E	RW	DNC	DB7-DB0	DB7-DB0
68-system 9-bit Parallel	E	RW	DNC	DB7-DB0	DB8-DB0
68-system 16-bit Parallel	E	RW	DNC	DB7-DB0	DB15-DB0
68-system 18-bit Parallel	E	RW	DNC	DB7-DB0	DB17-DB0
4 wire serial Interface	-	DNC	SCL	DB0 as SDA	

Table 5.2 Interface mode selection

5.1.1 Parallel bus system interface

The input / output data from data pins (DB17-0) and signal operation of the I80/M68 series parallel bus interface as listed in Table 5.3 and Table 5.4.

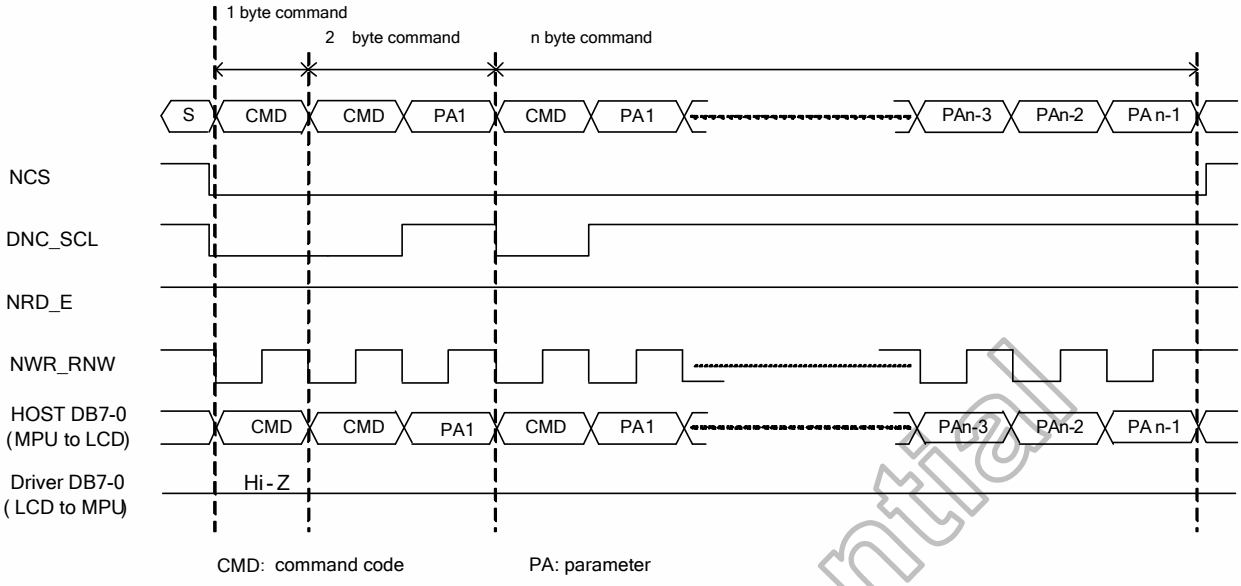
Operations	NWR_RNW	NRD_E	DNC_SCL
Writes command code	0	1	0
Reads internal status	1	0	0
Writes parameter into command or data into GRAM	0	1	1
Reads parameter from command or data from GRAM	1	0	1

Table 5.3 Data pin function for I80 series CPU

Operations	NWR_RNW	NRD_E	DNC_SCL
Writes command code	0	1	0
Reads internal status	1	1	0
Writes parameter into command or data into GRAM	0	1	1
Reads parameter from command or data from GRAM	1	1	1

Table 5.4 Data pin function for M68 series CPU

Write to register



Read from register

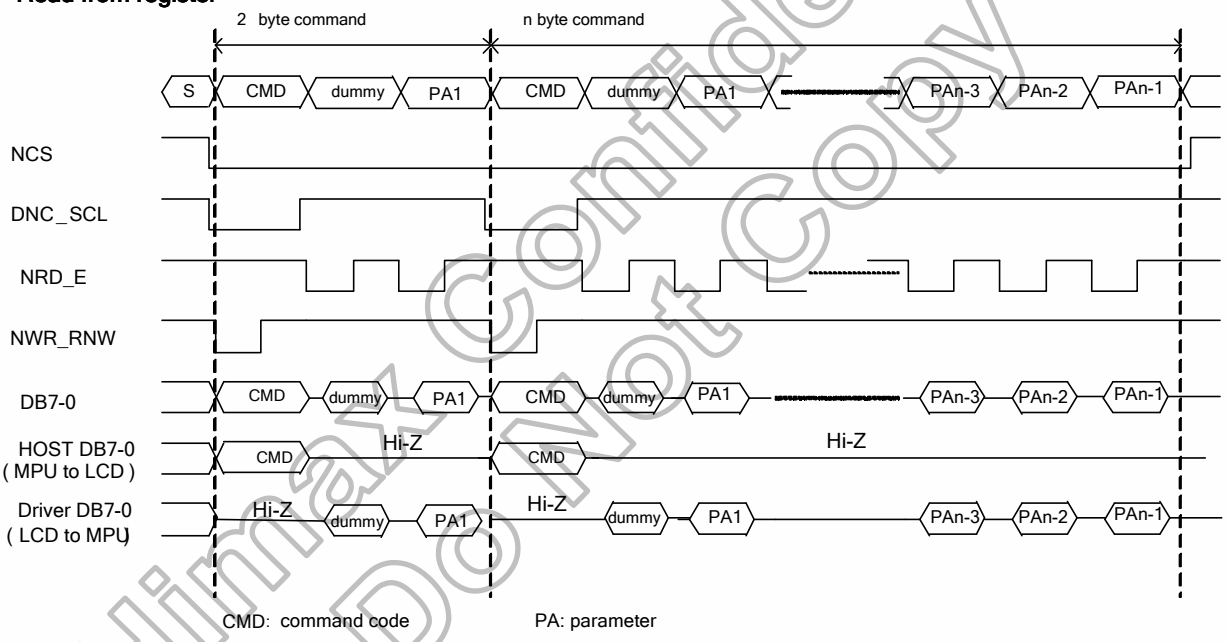
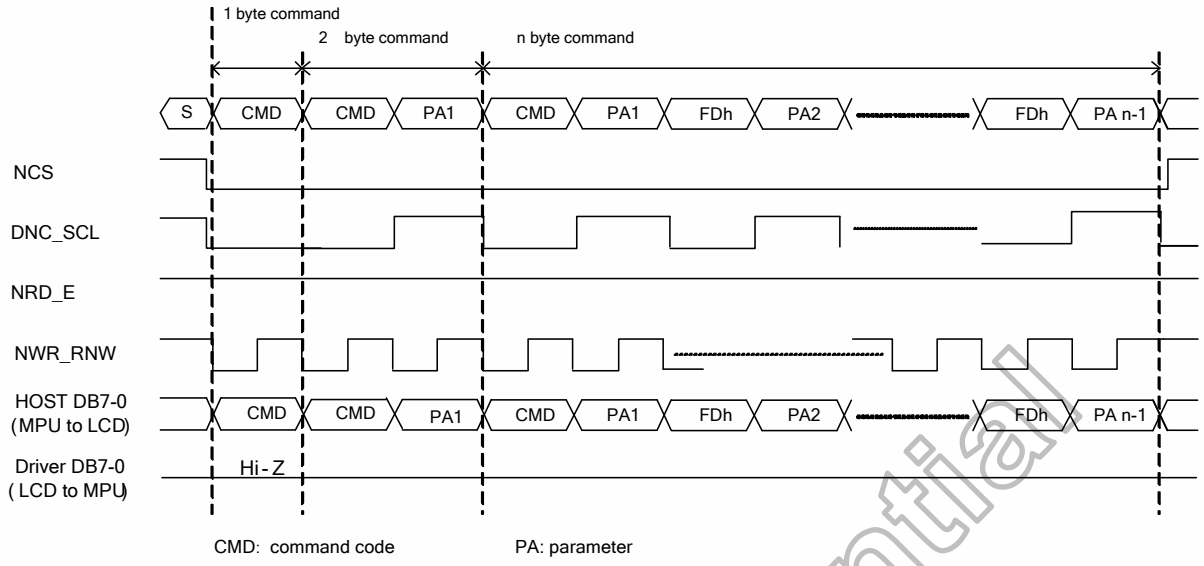


Figure 5.1 Register read/write timing in parallel bus system interface (for I80 series MPU)-1

Write to register



Read from register

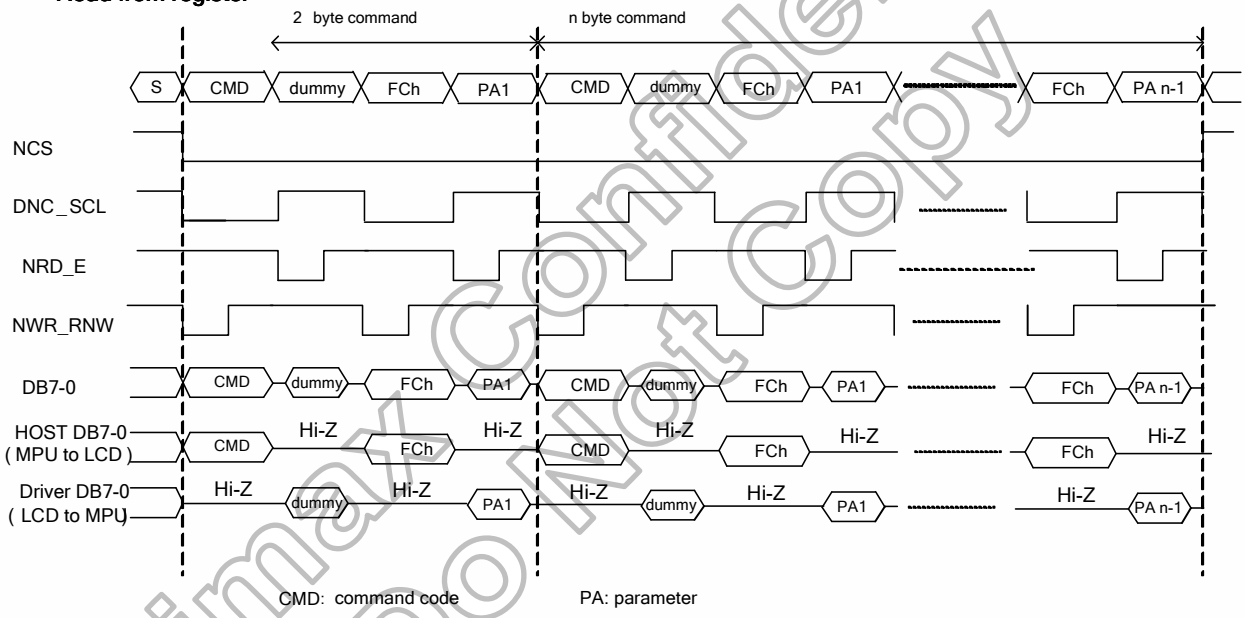
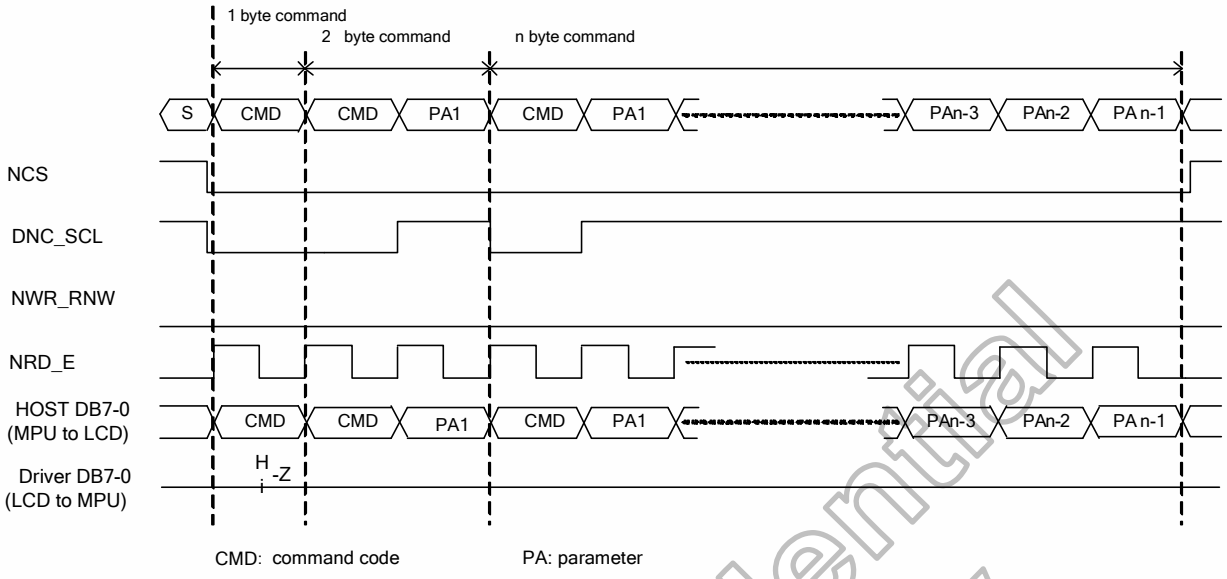


Figure 5.2 Register read/write timing in parallel bus system interface (for I80 series MPU)-2

Write to register



Read from register

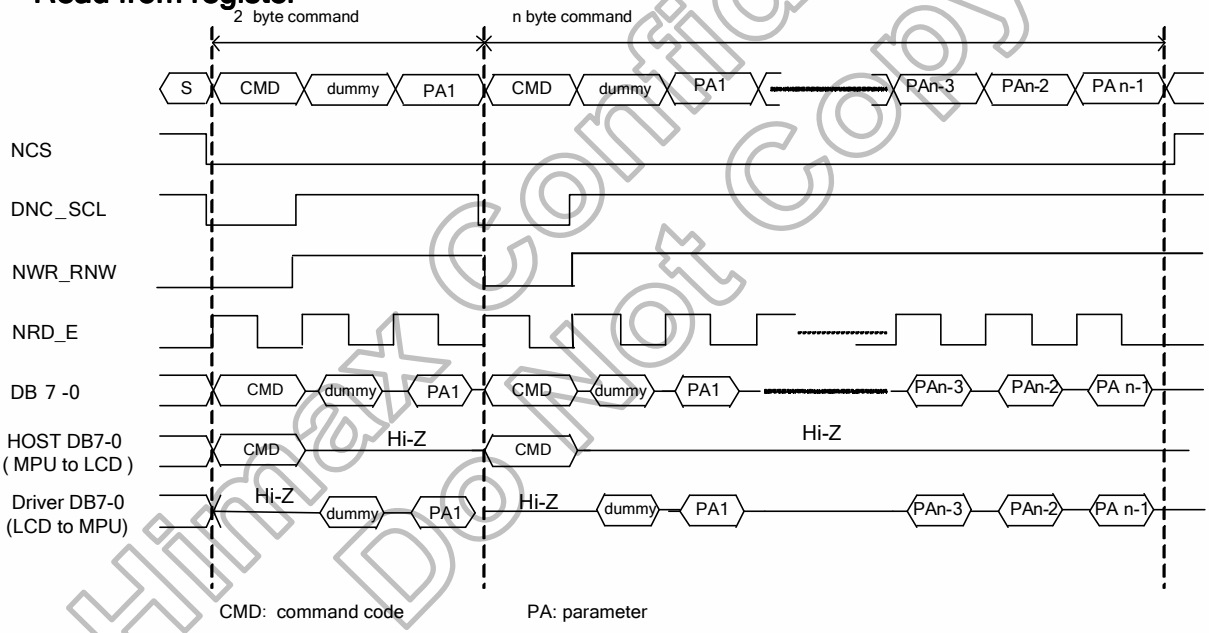
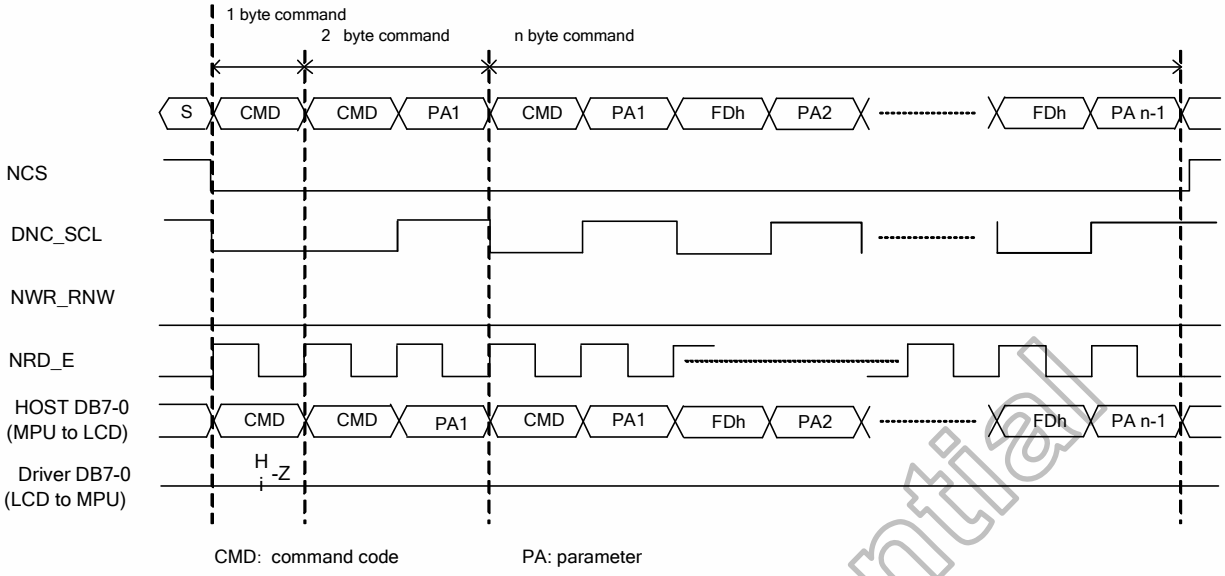


Figure 5.3 Register read/write timing in parallel bus system interface (for M68 series MPU)-1

Write to register



Read from register

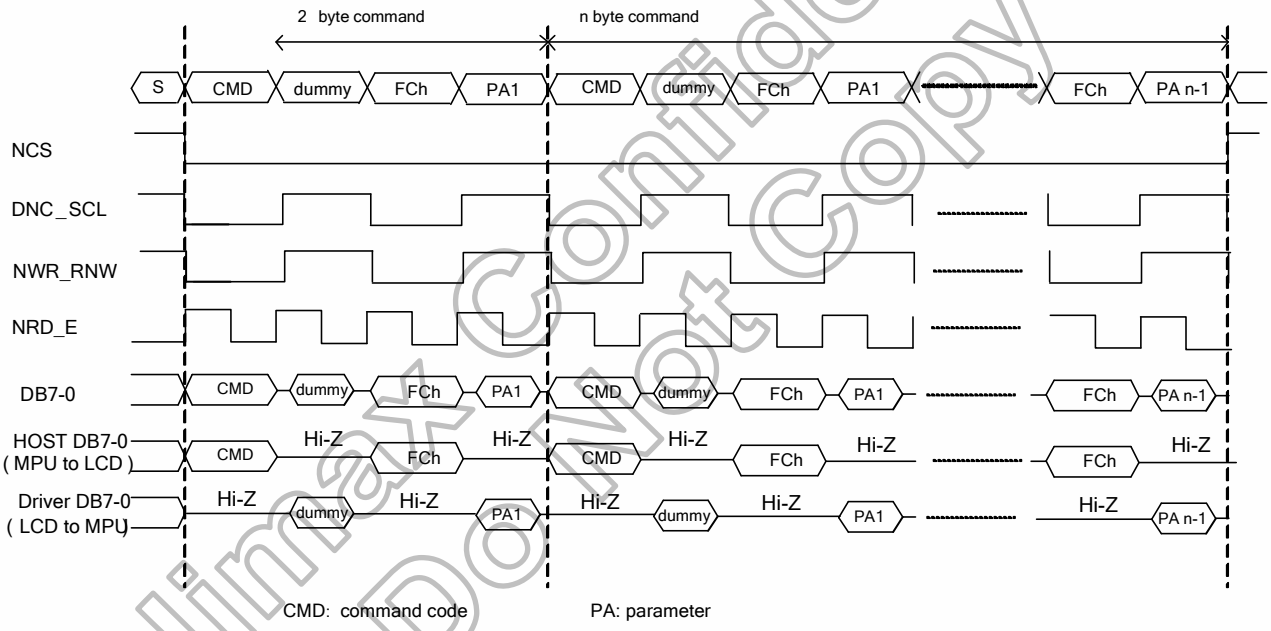
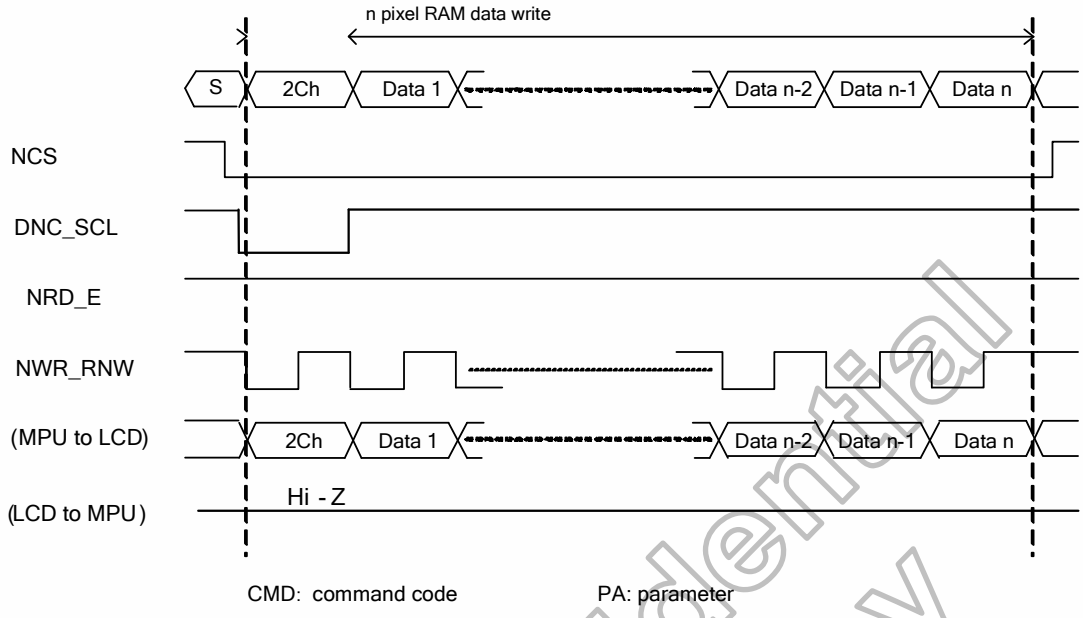


Figure 5.4 Register read/write timing in parallel bus system interface (for M68 series MPU)-2

Write to GRAM



Read from GRAM

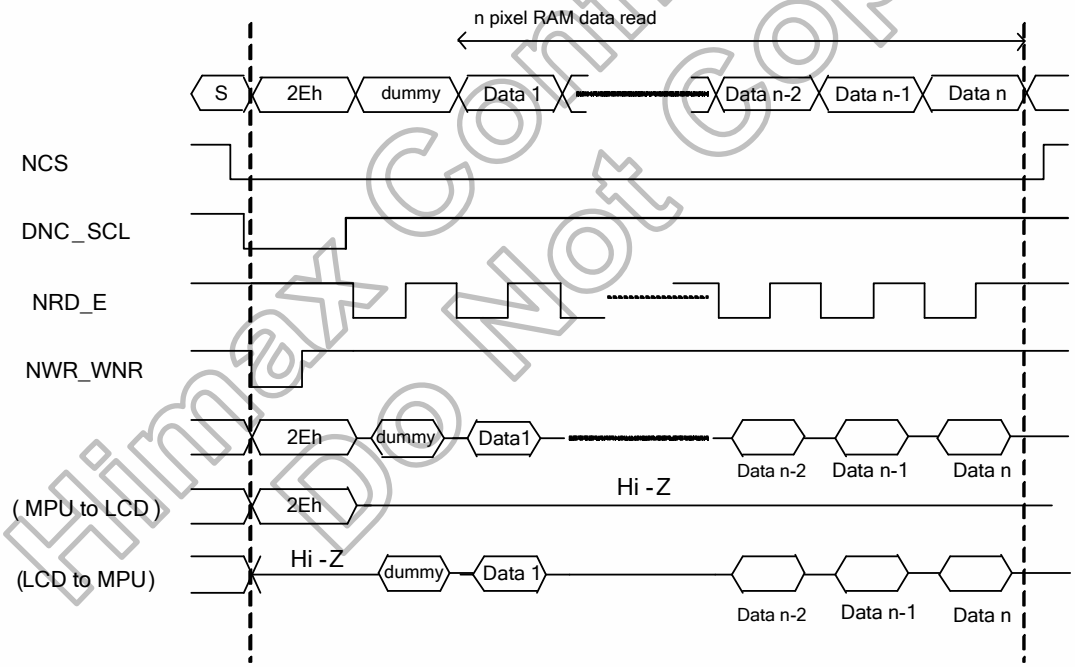
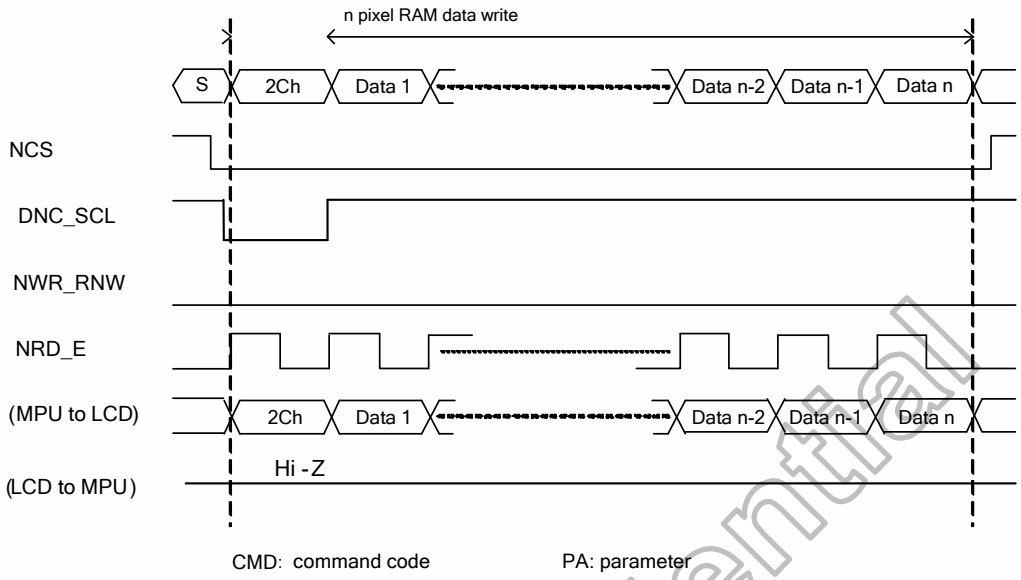


Figure 5.5 GRAM read/write timing in parallel bus system interface (for I80 series MPU)

Write to GRAM



Read from GRAM

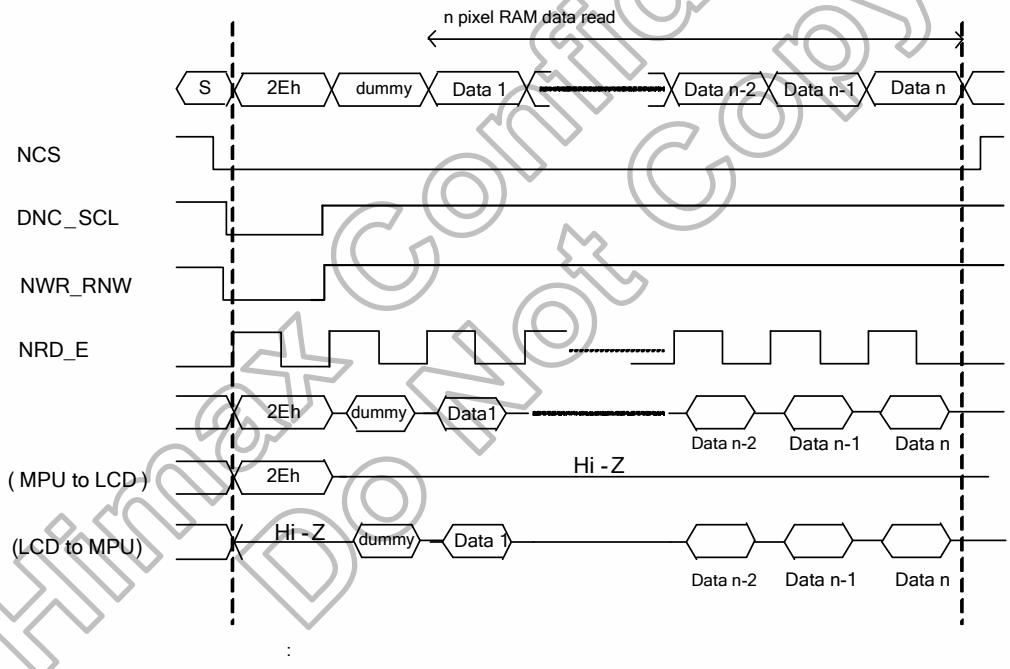


Figure 5.6 GRAM read/write timing in parallel bus system interface (for M68 series MPU)

5.1.2 MCU data color coding

MCU Data Color Coding for RAM data ***Write***

- Parallel 8-Bit Bus Interface (BS2,BS1,BS0="100")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	X	X	X	X	X	X	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	4K-Color (2-pixel/ 3-bytes)
	X	X	X	X	X	X	X	X	X	X	B3	B2	B1	B0	R3	R2	R1	R0	
	X	X	X	X	X	X	X	X	X	X	G3	G2	G1	G0	B3	B2	B1	B0	
05h	X	X	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	65K-Color (1-pixel/ 2-bytes)
	X	X	X	X	X	X	X	X	X	X	G2	G1	G0	B4	B3	B2	B1	B0	
06h	X	X	X	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	X	X	X	X	X	X	X	X	X	X	G5	G4	G3	G2	G1	G0	x	x	
	X	X	X	X	X	X	X	X	X	X	B5	B4	B3	B2	B1	B0	x	x	

Table 5.5 8-bit parallel interface GRAM write table

- Parallel 16-Bit Bus Interface (BS2,BS1,BS0="101")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
03h	X	X	X	X	X	X	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0	4K-Color
05h	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	65K-Color
06h	X	X	R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X	262K-Color (2-pixel/ 3bytes)
	X	X	B5	B4	B3	B2	B1	B0	X	X	R5	R4	R3	R2	R1	R0	X	X	
	X	X	G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X	

Table 5.6 16-bit parallel interface GRAM write table

- Parallel 9-Bit Bus Interface (BS2,BS1,BS0="110")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
06h	X	X	X	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	X	X	X	X	X	X	X	X	X	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.7 9-bit parallel interface GRAM write table

- Parallel 18-Bit Bus Interface (BS2,BS1,BS0="111")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	X	X	X	X	X	X	X	X	X	X	0	0	1	0	1	1	0	0	**2CH**
3AH	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.8 18-bit parallel interface GRAM write table

8-bit bus interface

The I80-system 8-bit parallel bus interface can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0100”. And the M68-system 8-bit parallel bus interface can be used by setting “P68, BS2, BS1, and BS0” pins to “1100”. Figure 5.7 is the example of interface with I80/M68 microcomputer system interface and Figure 5.8 ~Figure 5.10 is bit format per pixel color order.

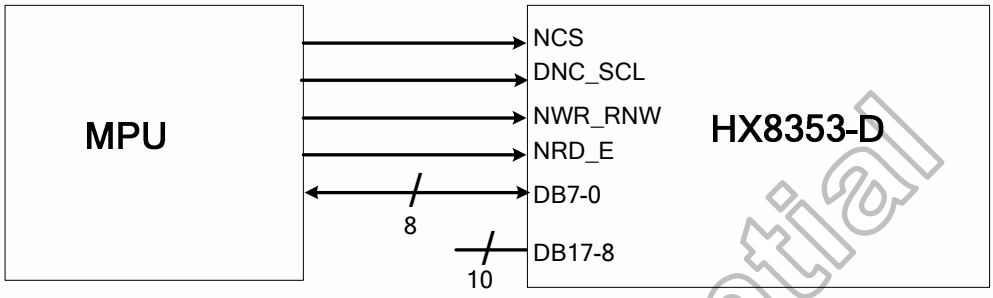


Figure 5.7 Example of 80- / 68- system 8-bit bus interface

262k Color Data	DNC_ SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R15	R14	R13	R12	R11	R10	x	x	-
2nd write	1	G15	G14	G13	G12	G11	G10	x	x	-
3rd write	1	B15	B14	B13	B12	B11	B10	x	x	1st pixel (R1/G1/B1)
4th write	1	R25	R24	R23	R22	R21	R20	x	x	-
5th write	1	G25	G24	G23	G22	G21	G20	x	x	-
6th write	1	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

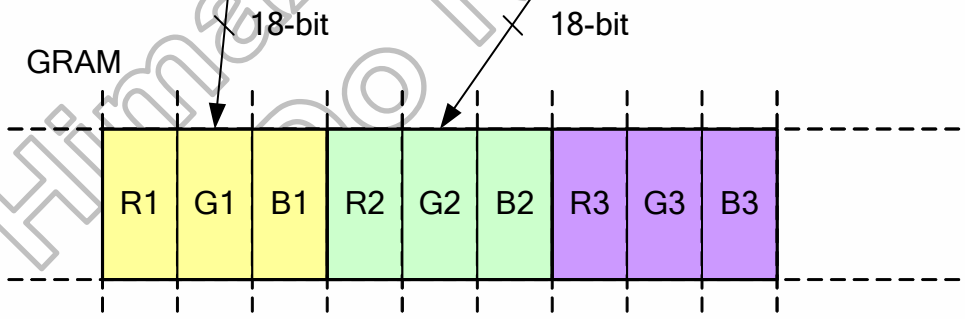
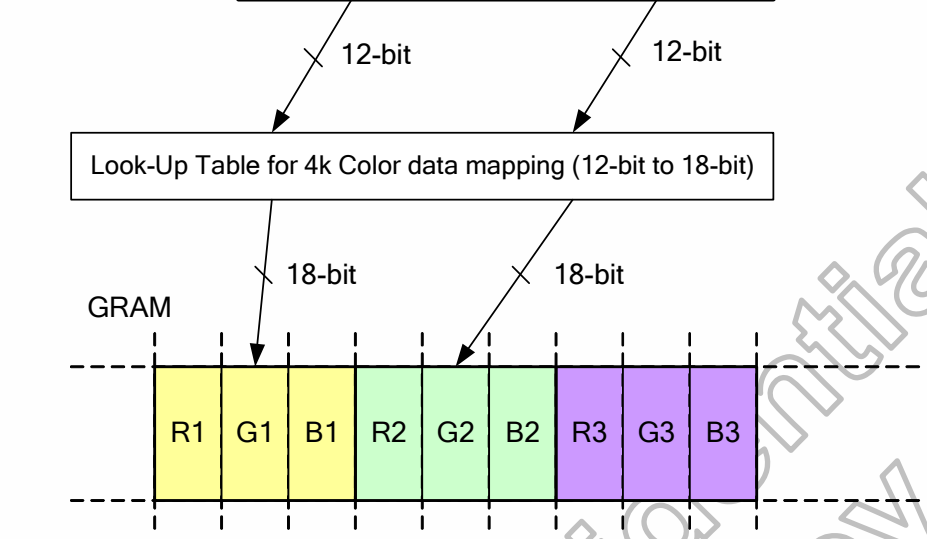


Figure 5.8 Write data for RGB 6-6-6-bit input

4k Color Data	DNC_ SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R13	R12	R11	R10	G13	G12	G11	G10	-
2nd write	1	B13	B12	B11	B10	R23	R22	R21	R20	1st pixel (R1/G1/B1)
3rd write	1	G23	G22	G21	G20	B23	B22	B21	B20	2nd pixel (R2/G2/B2)



4k Color Data	DNC_ SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R13	R12	R11	R10	G13	G12	G11	G10	-
2nd write	1	B13	B12	B11	B10	R23	R22	R21	R20	1st pixel (R1/G1/B1)
MEMWR	0	The other command								-
MEMWR	0	GRAM Write command code								-
1st write	1	R23	R22	R21	R20	G23	G22	G21	G20	-
2nd write	1	B23	B22	B21	B20	R33	R32	R31	R30	2nd pixel (R2/G2/B2)
3rd write	1	G33	G32	G31	G30	B33	B32	B31	B30	3rd pixel (R3/G3/B3)

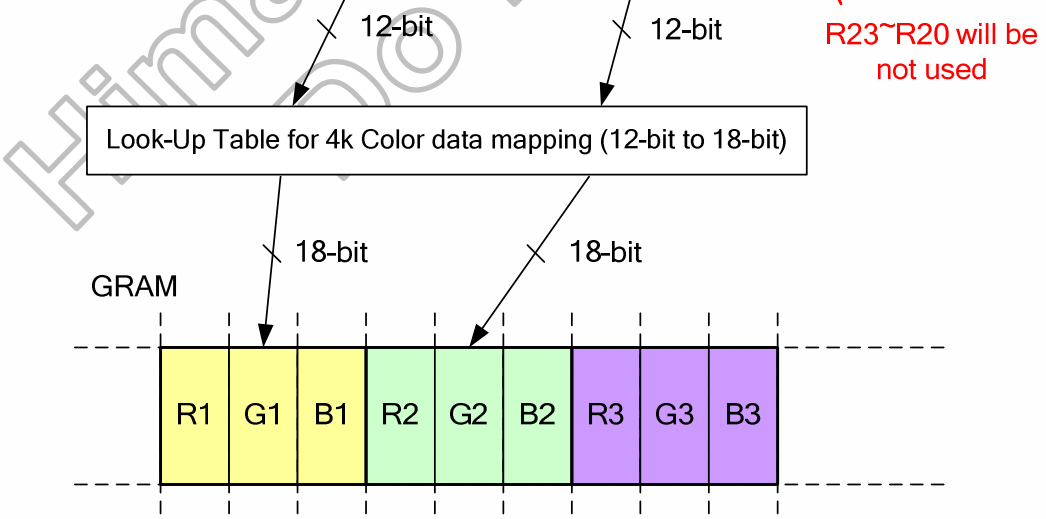


Figure 5.9 Write data for RGB 4-4-4-bit input

65k Color Data	DNC_SCL	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code								-
1st write	1	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

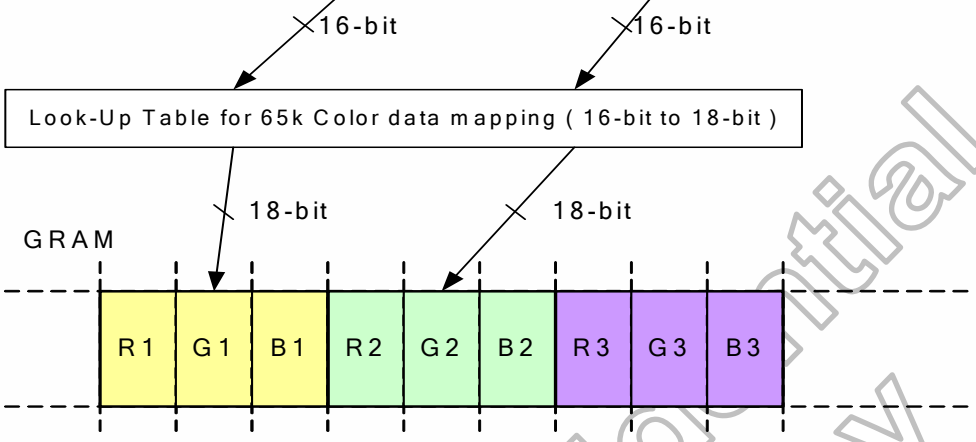


Figure 5.10 Write data for RGB 5-6-5-bit input

16-bit parallel bus system interface

The I80-system 16-bit parallel bus interface in command-parameter interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0101”. And the M68-system 16-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1” pins to “1101”. The Figure 5.11 is the example of interface with I80/M68 microcomputer system interface. There are three types of data format to write display data at 18-bit bus Interface. See Figure 5.12 ~ Figure 5.14.

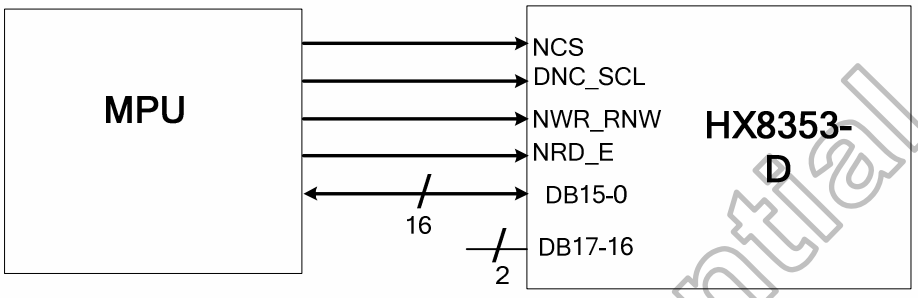


Figure 5.11 Example of I80- / M68- system 16-bit parallel bus interface

	DNC_SCL	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	x	x	x	x	x	x	x	x	GRAM Write command code (2Ch)								-
1 st write	1	R15	R14	R13	R12	R11	R10	x	x	G15	G14	G13	G12	G11	G10	x	x	-
2 nd write	1	B15	B14	B13	B12	B11	B10	x	x	R25	R24	R23	R22	R21	R20	x	x	1st pixel (R1/G1/B1)
3 rd write	1	G25	G24	G23	G22	G21	G20	x	x	B25	B24	B23	B22	B21	B20	x	x	2nd pixel (R2/G2/B2)

X : Don’t care

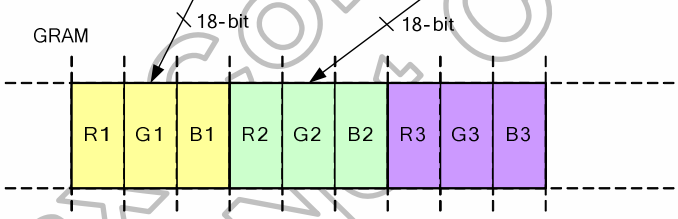


Figure 5.12 GRAM write data for RGB 6-6-6-(262k colors) bit input

4k Color Data	DNC_SCL	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code																-
1st write	1	x	x	x	x	R13	R12	R11	R10	G13	G12	G11	G10	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	x	x	x	x	R23	R22	R21	R20	G23	G22	G21	G20	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

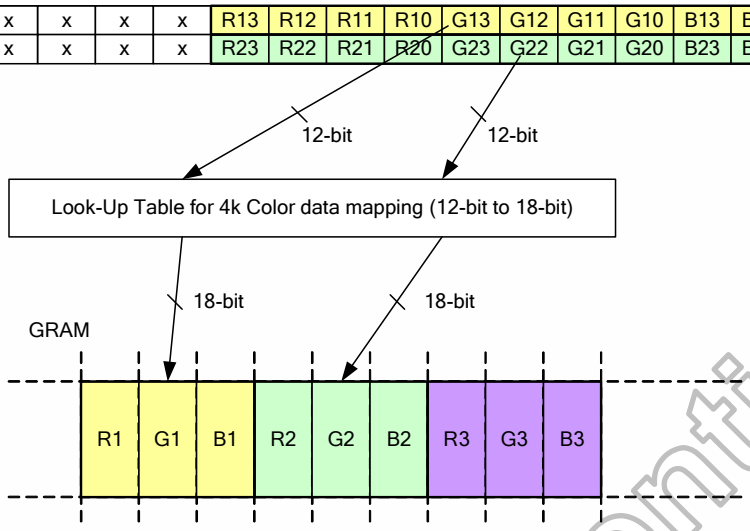


Figure 5.13 Write data for RGB 4-4-4 (4k colors) bit input on 16-bit parallel interface

65k Color Data	DNC_SCL	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	x	x	x	x	x	x	x	x	GRAM Write command code								-
1st write	1	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

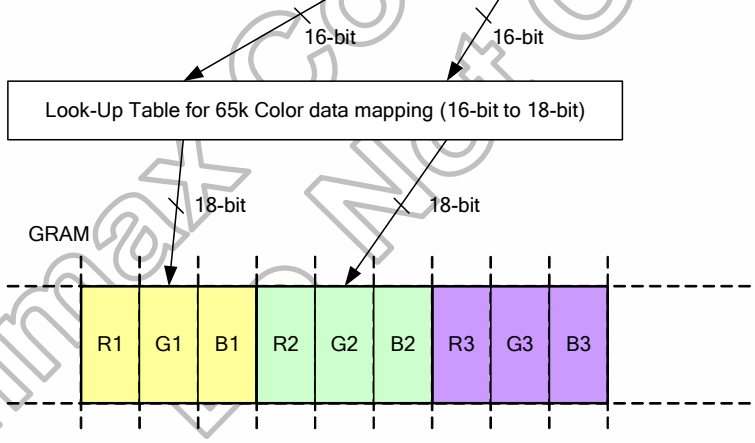


Figure 5.14 Write data for RGB 5-6-5 (65k colors) bit input on 16-bit parallel interface

18-bit parallel bus system interface

The I80-system 18-bit parallel bus interface in MPU interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0111”. And the M68-system 18-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1111”. The Figure5.15 is the example of interface with I80/M68 microcomputer system interface.

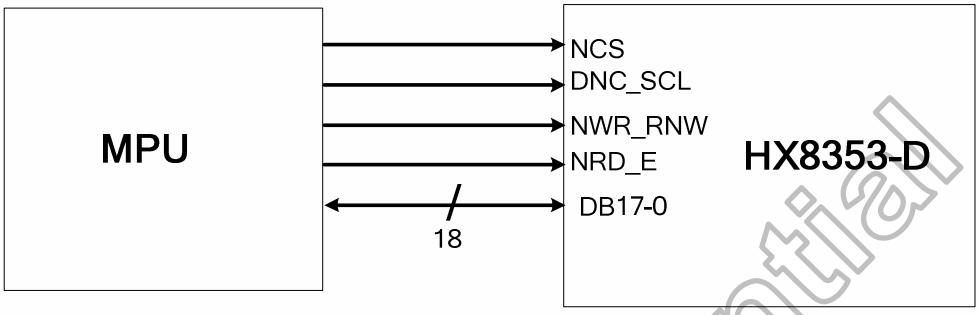


Figure 5.15 Example of I80- / M68- system 18-bit parallel bus interface

There is one type of data format to write display data at 18-bit bus Interface. See Figure 5.16.

262k Color Data	DNC_SCL	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code																		-
1st write	1	R15	R14	R13	R12	R11	R10	G15	G14	G13	G12	G11	G10	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
2nd write	1	R25	R24	R23	R22	R21	R20	G25	G24	G23	G22	G21	G20	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

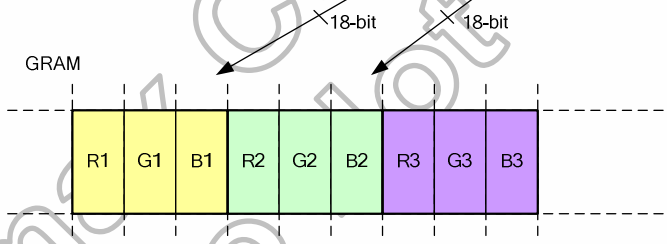


Figure 5.16 Write data for RGB 6-6-6(262k colors) bit input in 18-bit parallel interface

9-bit bus interface

The I80-system 9-bit parallel bus interface in MPU interface mode can be used by setting external pins “P68, BS2, BS1, BS0” pins to “0110”. And the M68-system 9-bit parallel bus interface in MPU interface mode can be used by setting “P68, BS2, BS1, BS0” pins to “1110”. The Figure5.17 is the example of interface with I80/M68 microcomputer system interface.

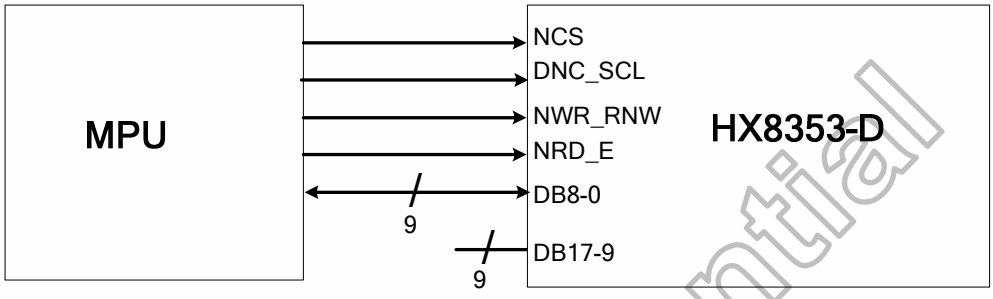


Figure 5.17 Example of 80- / 68- system 9-bit bus interface

There is one type of data format to write display data at 9-bit bus Interface. See Figure 5.18.

262k Color Data	DNC_SCL	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	GRAM Write
MEMWR	0	GRAM Write command code									-
1st write	1	R15	R14	R13	R12	R11	R10	G15	G14	G13	-
2nd write	1	G12	G11	G10	B15	B14	B13	B12	B11	B10	1st pixel (R1/G1/B1)
3rd write	1	R25	R24	R23	R22	R21	R20	G25	G24	G23	-
4th write	1	G22	G21	G20	B25	B24	B23	B22	B21	B20	2nd pixel (R2/G2/B2)

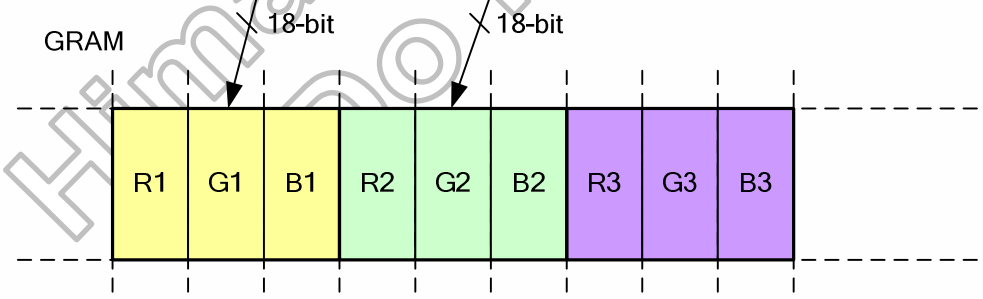


Figure 5.18 Write data for RGB 6-6-6-bit (262k colors) input in 9-bit parallel interface

MCU Data Color Coding for RAM data ***Read***

- Parallel 8-Bit Bus Interface (BS2,BS1,BS0="100")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	262K-Color (1-pixel/ 3bytes)
	x	x	x	x	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	
	x	x	x	x	x	x	x	x	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.9 8-bit parallel interface GRAM read table

- Parallel 16-Bit Bus Interface (BS2,BS1,BS0="101")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Command
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	262K-Color (2-pixel/ 3bytes)
	x	x	B5	B4	B3	B2	B1	B0	x	x	R5	R4	R3	R2	R1	R0	x	x	
	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0	x	x	

Table 5.10 16-bit parallel interface GRAM read table

- Parallel 9-Bit Bus Interface (BS2,BS1,BS0="110")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	x	x	x	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	262K-Color (1-pixel/ 2bytes)
	x	x	x	x	x	x	x	x	x	G2	G1	G0	B5	B4	B3	B2	B1	B0	

Table 5.11 9-bit parallel interface GRAM read table

- Parallel 18-Bit Bus Interface (BS2,BS1,BS0="111")

Register Command	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register
	x	x	x	x	x	x	x	x	x	x	0	0	1	0	1	1	1	0	**2EH**
Read Data Format	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 5.12 18-bit parallel interface GRAM read table

5.1.3 Serial Interface

The HX8353-D supports serial data transfer interface. The interface selection by setting BS2=0 for serial interface mode. The 3-wires serial bus and 4-wires serial bus is select by SPI_SEL pin. When SPI_SEL pin is low (VSSD), it is selected by 3-wires serial bus and use: chip select line (NCS), serial input/output data (SDA), and the serial transfer clock line (DNC_SCL). When SPI_SEL pin is high (IOVCC), it is selected by 4-wires serial bus and use: chip select line (NCS), serial input/output data (SDA), and the serial transfer clock line (DNC_SCL) and the command or data transfer signal (NWR_RNW).

Serial data write mode

The 3-wires serial data packet contains a control bit DNC and a transmission byte, and in 4-wires serial case data packet contains just transmission byte and control bit DNC is transferred by NWR_RNW pin. If NWR_RNW is low, the transmission byte is command byte. If NWR_RNW is high, the transmission byte is stored to command register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, DNC_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

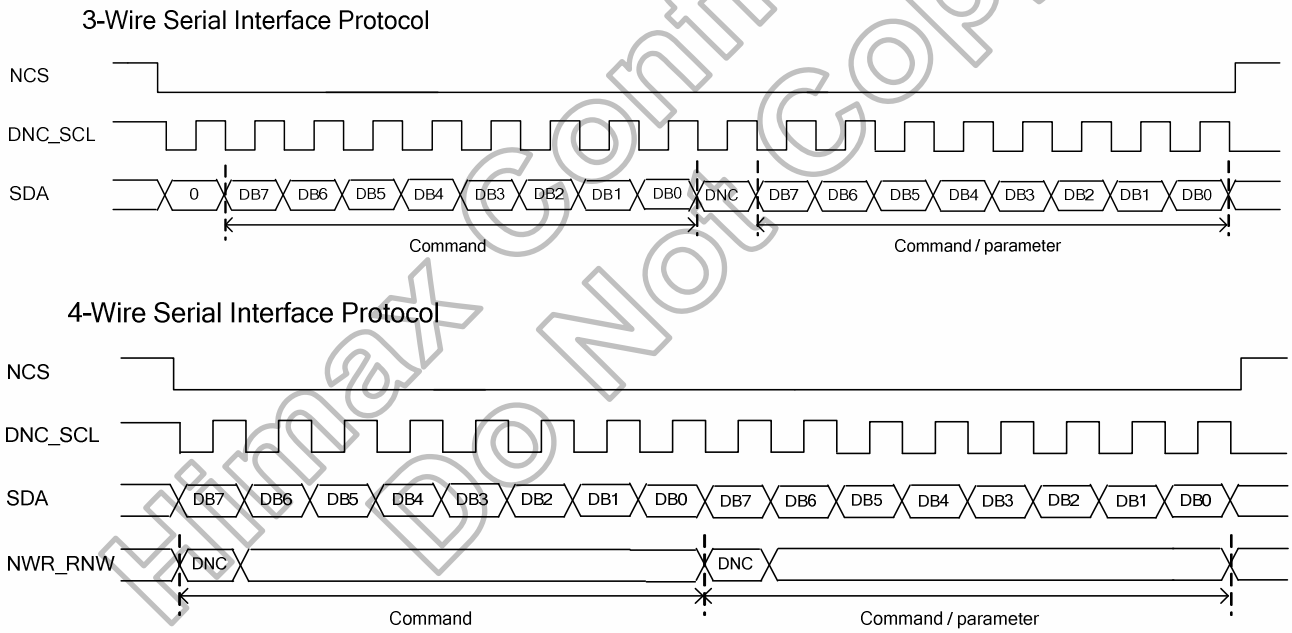


Figure 5.19 Serial interface protocol 3-/4- wire, write mode

Serial data read mode

The microcontroller first has to send a command and then the following byte is transmitted in the opposite direction. The read mode has three type command data transmitted (8- / 24- / 32-bit) is according command code.

3-Wire Serial Interface Protocol

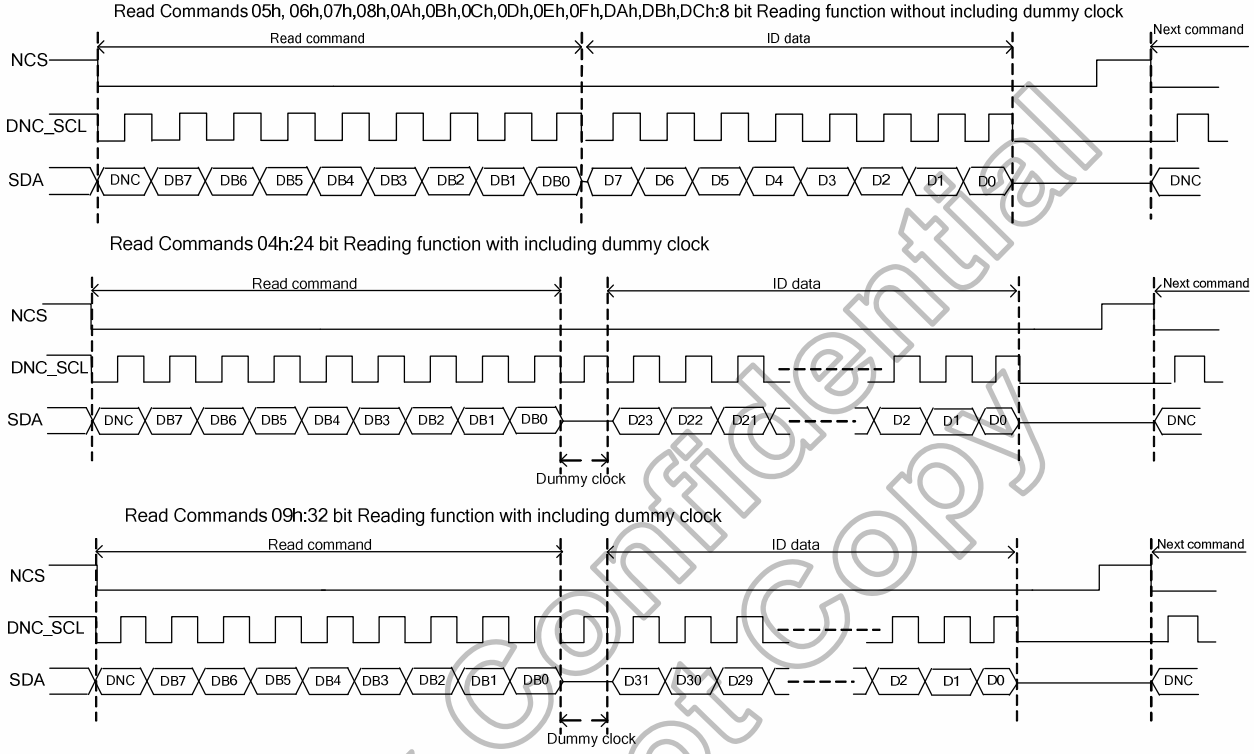


Figure 5.20 3-wire serial interface protocol, read mode

4-Wire Serial Interface Protocol

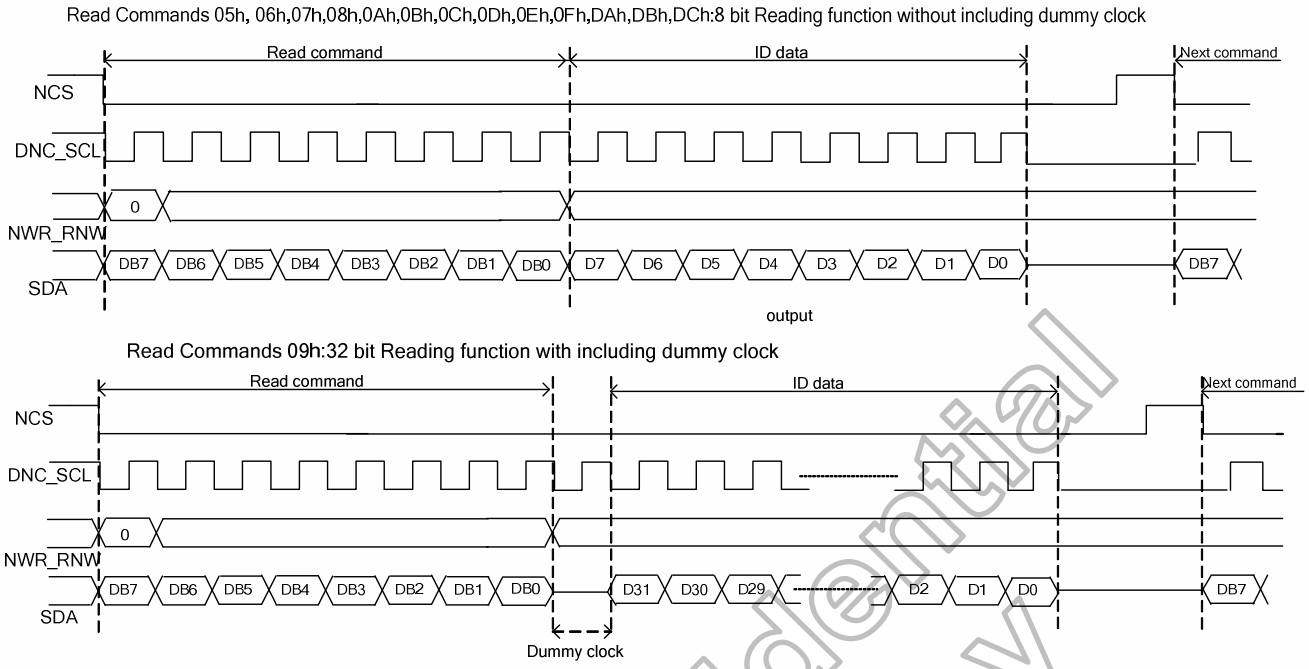


Figure 5.21 4-wire serial interface protocol, read mode

The data format that write display data to SRAM at Serial data bus Interface is shown as Figure5. 22 ~ Figure5. 27.

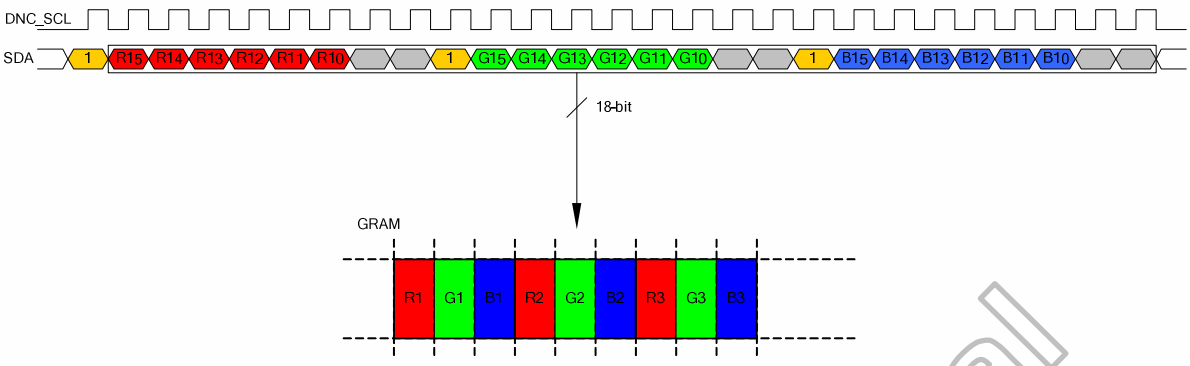


Figure 5.22 3-wire serial write data for RGB (6-6-6) bit input

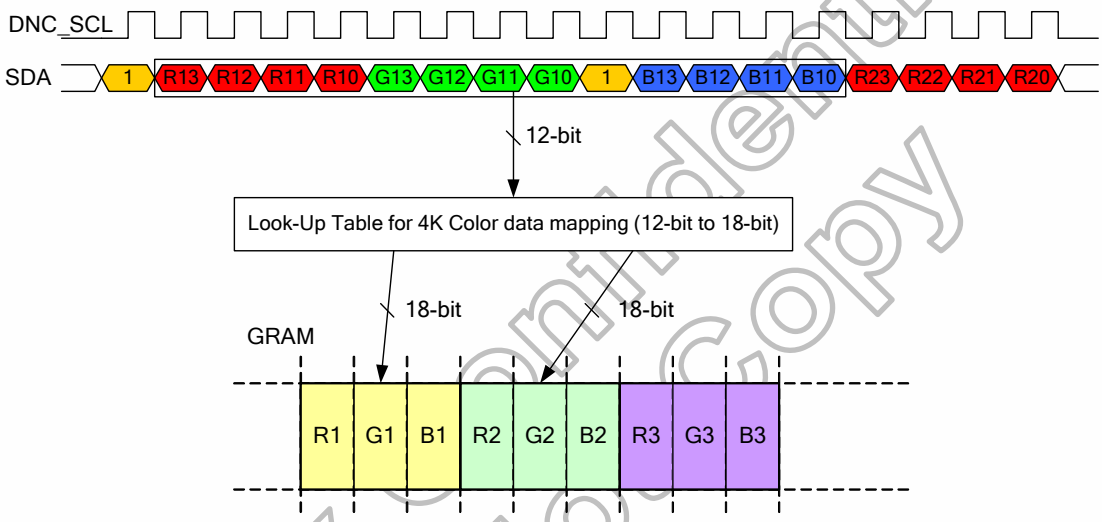


Figure 5.23 3-wire serial write data for RGB 4-4-4-bit input

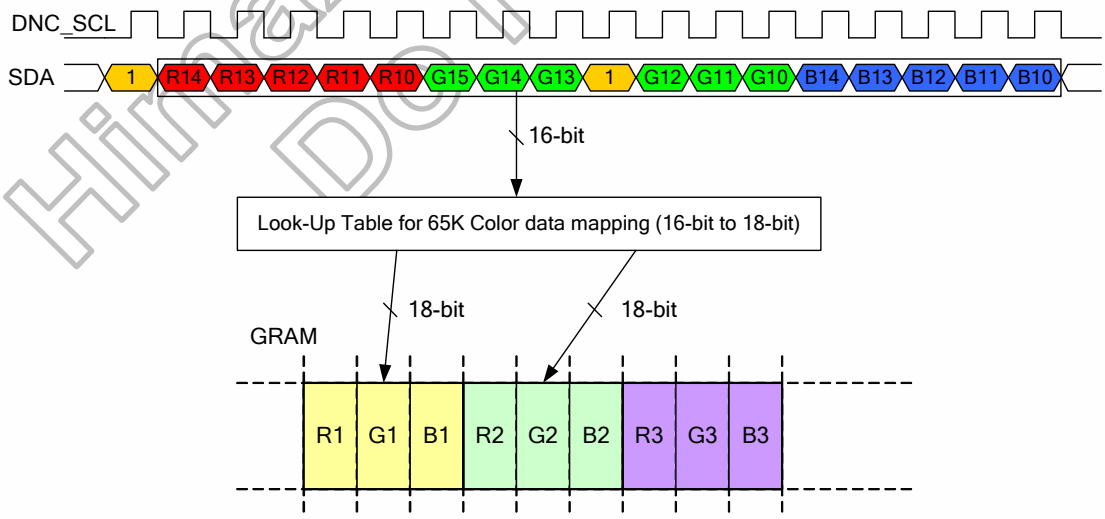


Figure 5.24 3-wire serial write data for RGB 5-6-5-bit input

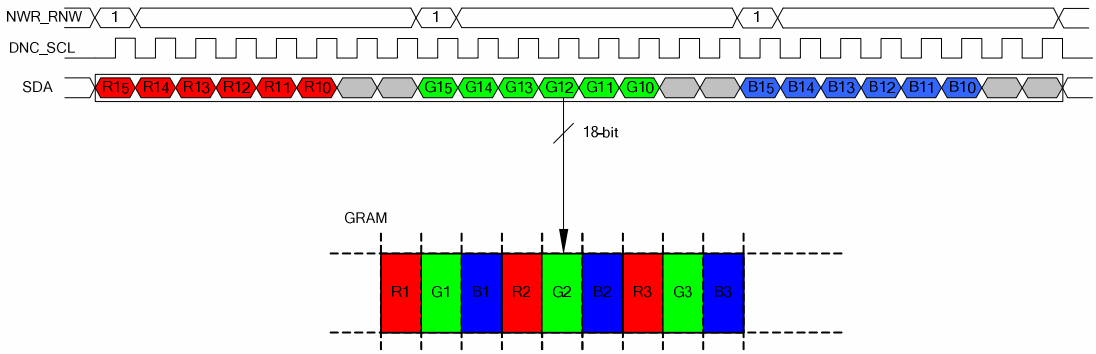


Figure 5.25 4-wire serial write data for RGB (6-6-6) bit input

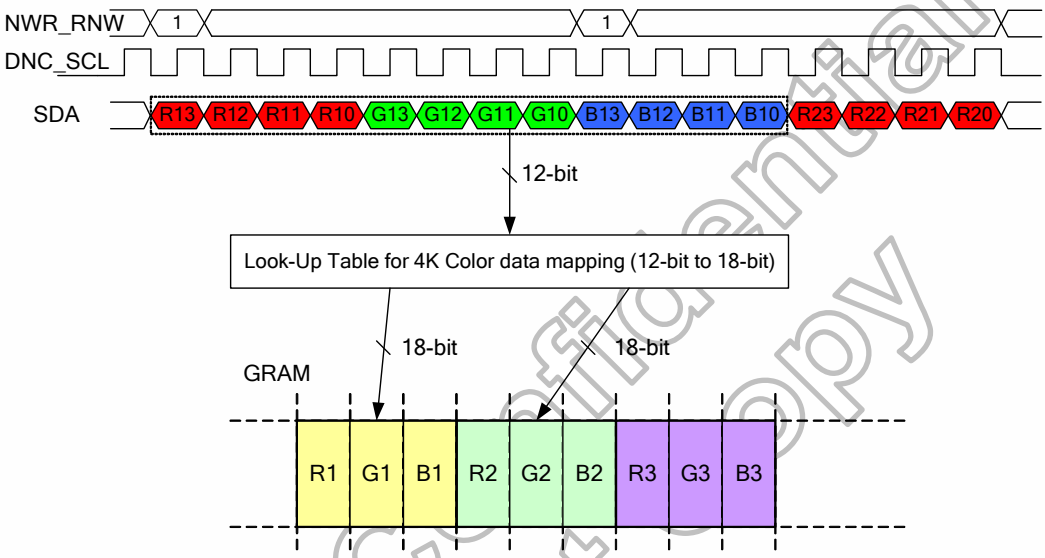


Figure 5.26 4-wire serial write data for RGB 4-4-4-bit input

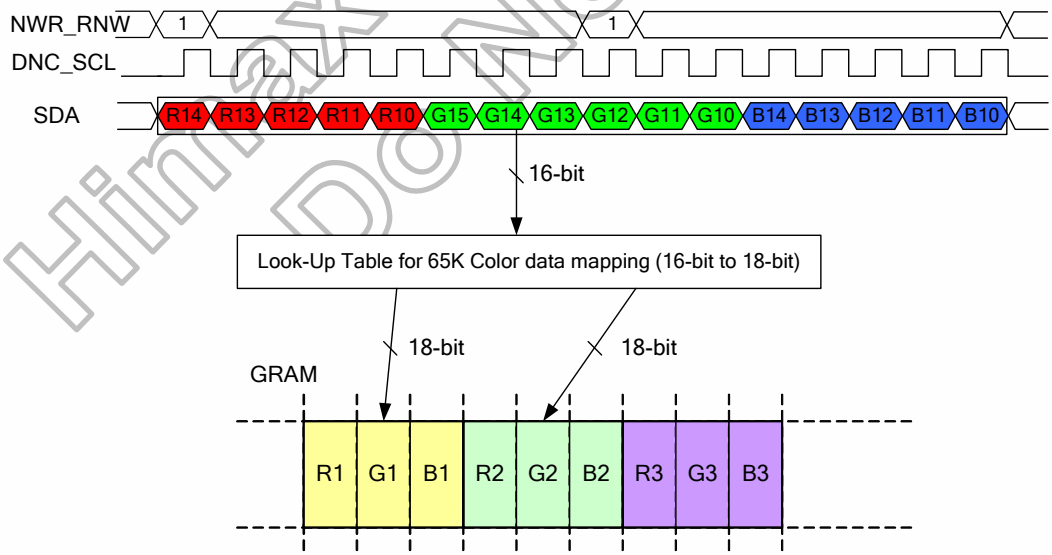


Figure 5.27 4-wire serial write data for RGB 5-6-5-bit input

5.1.4 Display module data transfer recovery

If there is a break on data transmission when transmitting a command before a whole byte has been completed, then the display module will reset the interface so that it will be ready to receive the same byte re-transmitted when the chip select line (NCS) is next activated. See the following figure.

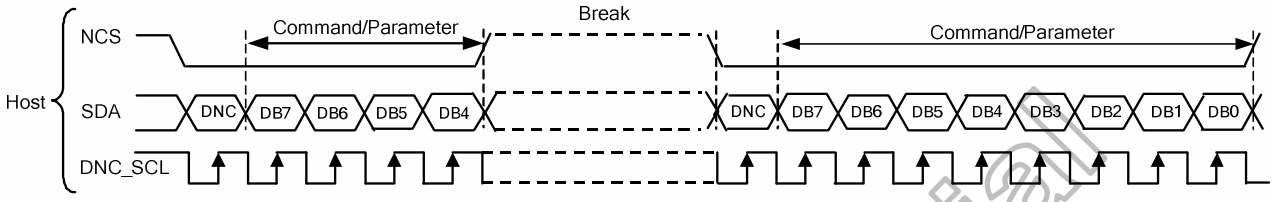
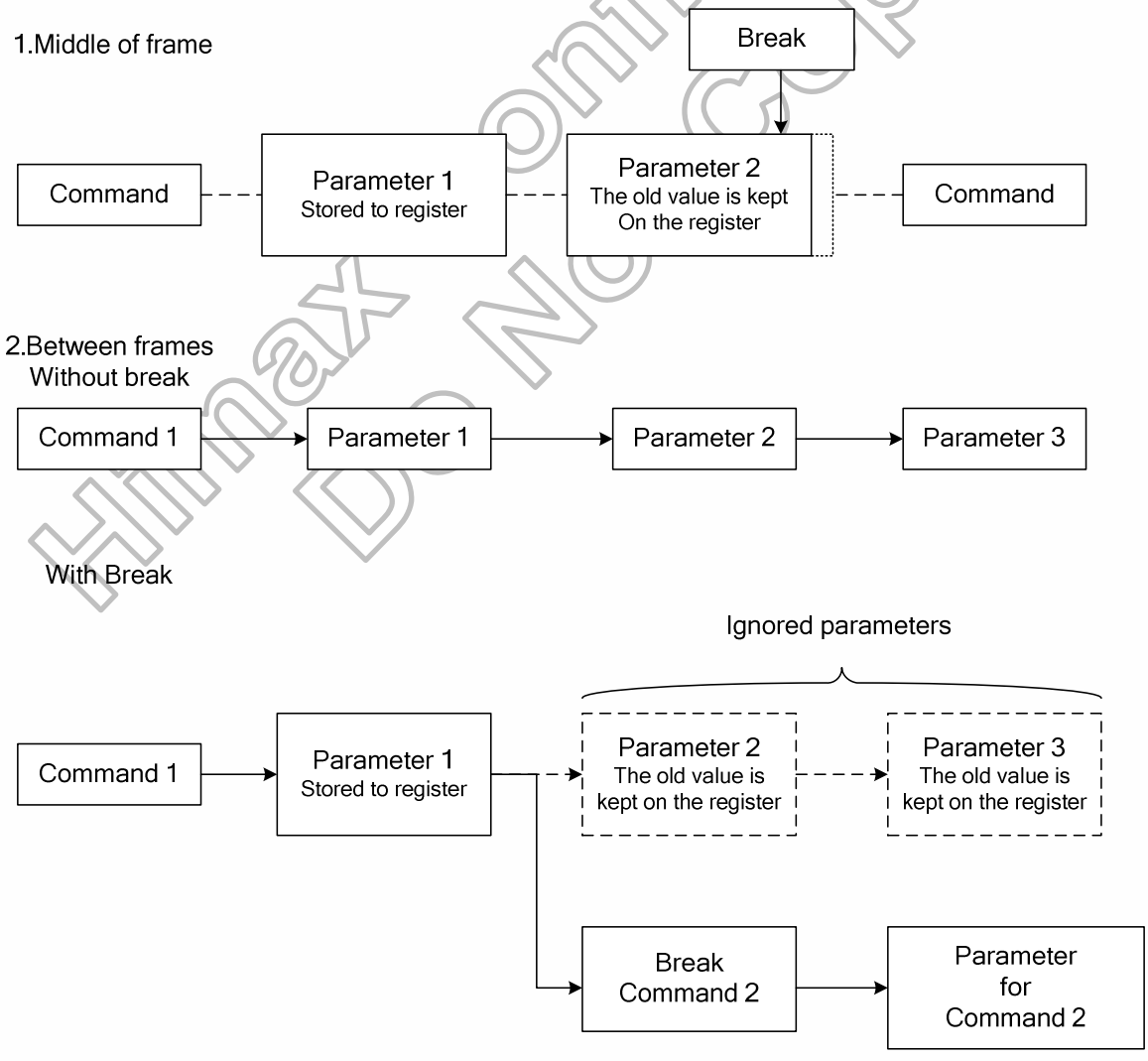


Figure 5.28 Display module data transfer recovery

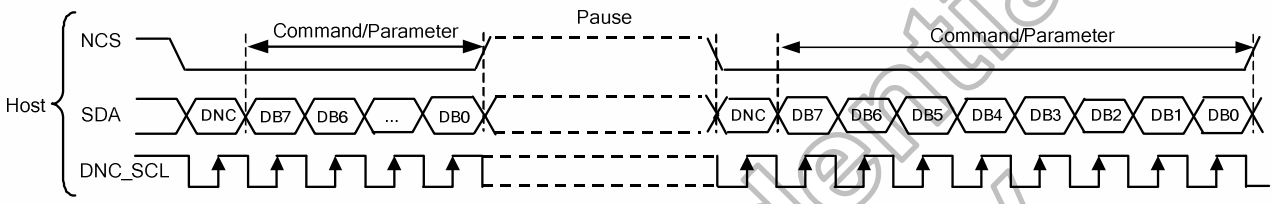
If 1 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:



5.1.5 Display module data transfer pause

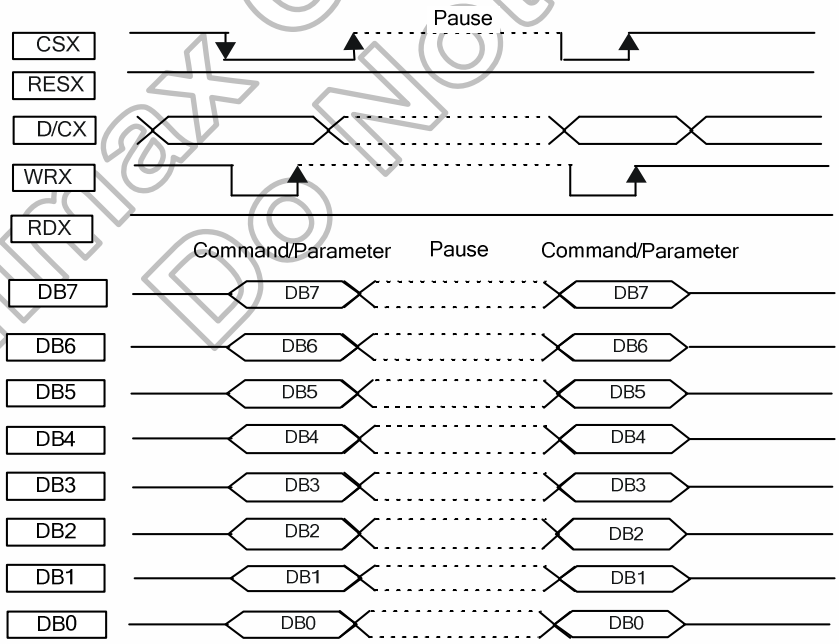
It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:

Serial interface pause



This applies to the following 4 conditions:
a. Command-Pause-Command
b. Command-Pause-Parameter
c. Parameter-Pause-Parameter
d. Parameter-Pause-Parameter

Parallel interface pause



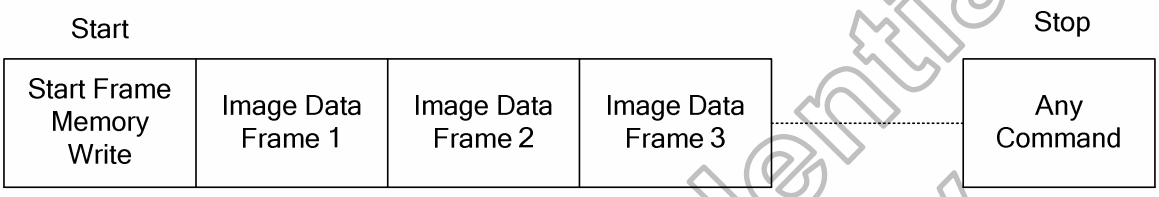
This applies to the following 4 conditions:
a. Command-Pause-Command
b. Command-Pause-Parameter
c. Parameter-Pause-Command

d. Parameter-Pause-Parameter

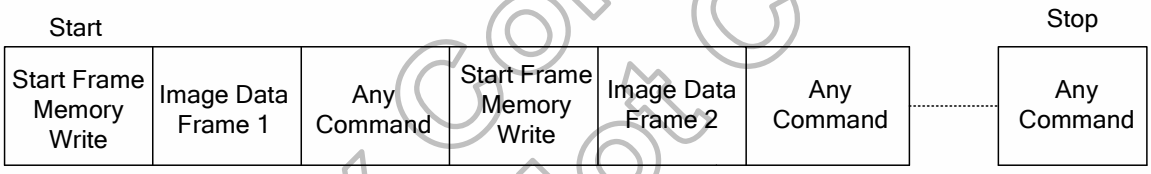
5.1.6 Display module data transfer modes

The Module has three colour modes for transferring data to the display RAM. These are 12-bit colour per pixel, 16-bit colour per pixel and 18-bit colour per pixel. The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method 1:
The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.



Method 2:
Image Data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloaded.



Note: (1) These apply to all Data Transfer Colour modes on both Serial and Parallel interfaces.
(2) The Frame Memory can contain both odd and even number of pixels for both Methods. Only complete pixel data will be stored in the Frame Memory.

5.2 Color depth conversion

R input (4bit) 12 bit/pixel -mode 4,096 colors	R input (5 bit) 16 bit/pixel -mode 65,536 colors	R output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
0000	00000	R005 R004 R003 R002 R001 R000	1
0001	00001	R015 R014 R013 R012 R011 R010	2
0010	00010	R025 R024 R023 R022 R021 R020	3
0011	00011	R035 R034 R033 R032 R031 R030	4
0100	00100	R045 R044 R043 R042 R041 R040	5
0101	00101	R055 R054 R053 R052 R051 R050	6
0110	00110	R065 R064 R063 R062 R061 R060	7
0111	00111	R075 R074 R073 R072 R071 R070	8
1000	01000	R085 R084 R083 R082 R081 R080	9
1001	01001	R095 R094 R093 R092 R091 R090	10
1010	01010	R105 R104 R103 R102 R101 R100	11
1011	01011	R115 R114 R113 R112 R111 R110	12
1100	01100	R125 R124 R123 R122 R121 R120	13
1101	01101	R135 R134 R133 R132 R131 R130	14
1110	01110	R145 R144 R143 R142 R141 R140	15
1111	01111	R155 R154 R153 R152 R151 R150	16
No Input	10000	R165 R164 R163 R162 R161 R160	17
No Input	10001	R175 R174 R173 R172 R171 R170	18
No Input	10010	R185 R184 R183 R182 R181 R180	19
No Input	10011	R195 R194 R193 R192 R191 R190	20
No Input	10100	R205 R204 R203 R202 R201 R200	21
No Input	10101	R215 R214 R213 R212 R211 R210	22
No Input	10110	R225 R224 R223 R222 R221 R220	23
No Input	10111	R235 R234 R233 R232 R231 R230	24
No Input	11000	R245 R244 R243 R242 R241 R240	25
No Input	11001	R255 R254 R253 R252 R251 R250	26
No Input	11010	R265 R264 R263 R262 R261 R260	27
No Input	11011	R275 R274 R273 R272 R271 R270	28
No Input	11100	R285 R284 R283 R282 R281 R280	29
No Input	11101	R295 R294 R293 R292 R291 R290	30
No Input	11110	R305 R304 R303 R302 R301 R300	31
No Input	11111	R315 R314 R313 R312 R311 R310	32

G input (4bit) 12 bit/pixel -mode 4,096 colors	G input (6 bit) 16 bit/pixel -mode 65,536 colors	G output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
0000	000000	G005 G004 G003 G002 G001 G000	33
0001	000001	G015 G014 G013 G012 G011 G010	34
0010	000010	G025 G024 G023 G022 G021 G020	35
0011	000011	G035 G034 G033 G032 G031 G030	36
0100	000100	G045 G044 G043 G042 G041 G040	37
0101	000101	G055 G054 G053 G052 G051 G050	38
0110	000110	G065 G064 G063 G062 G061 G060	39
0111	000111	G075 G074 G073 G072 G071 G070	40
1000	001000	G085 G084 G083 G082 G081 G080	41
1001	001001	G095 G094 G093 G092 G091 G090	42
1010	001010	G105 G104 G103 G102 G101 G100	43
1011	001011	G115 G114 G113 G112 G111 G110	44
1100	001100	G125 G124 G123 G122 G121 G120	45
1101	001101	G135 G134 G133 G132 G131 G130	46
1110	001110	G145 G144 G143 G142 G141 G140	47
1111	001111	G155 G154 G153 G152 G151 G150	48
No Input	010000	G165 G164 G163 G162 G161 G160	49
No Input	010001	G175 G174 G173 G172 G171 G170	50
No Input	010010	G185 G184 G183 G182 G181 G180	51
No Input	010011	G195 G194 G193 G192 G191 G190	52
No Input	010100	G205 G204 G203 G202 G201 G200	53
No Input	010101	G215 G214 G213 G212 G211 G210	54
No Input	010110	G225 G224 G223 G222 G221 G220	55
No Input	010111	G235 G234 G233 G232 G231 G230	56
No Input	011000	G245 G244 G243 G242 G241 G240	57
No Input	011001	G255 G254 G253 G252 G251 G250	58
No Input	011010	G265 G264 G263 G262 G261 G260	59
No Input	011011	G275 G274 G273 G272 G271 G270	60
No Input	011100	G285 G284 G283 G282 G281 G280	61
No Input	011101	G295 G294 G293 G292 G291 G290	62
No Input	011110	G305 G304 G303 G302 G301 G300	63
No Input	011111	G315 G314 G313 G312 G311 G310	64

G input (4bit) 12 bit/pixel -mode 4,096 colors	G input (6 bit) 16 bit/pixel -mode 65,536 colors	G output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
No Input	100000	G325 G324 G323 G322 G321 G320	65
No Input	100001	G335 G334 G333 G332 G331 G330	66
No Input	100010	G345 G344 G343 G342 G341 G340	67
No Input	100011	G355 G354 G353 G352 G351 G350	68
No Input	100100	G365 G364 G363 G362 G361 G360	69
No Input	100101	G375 G374 G373 G372 G371 G370	70
No Input	100110	G385 G384 G383 G382 G381 G380	71
No Input	100111	G395 G394 G393 G392 G391 G390	72
No Input	101000	G405 G404 G403 G402 G401 G400	73
No Input	101001	G415 G414 G413 G412 G411 G410	74
No Input	101010	G425 G424 G423 G422 G421 G420	75
No Input	101011	G435 G434 G433 G432 G431 G430	76
No Input	101100	G445 G444 G443 G442 G441 G440	77
No Input	101101	G455 G454 G453 G452 G451 G450	78
No Input	101110	G465 G464 G463 G462 G461 G460	79
No Input	101111	G475 G474 G473 G472 G471 G470	80
No Input	110000	G485 G484 G483 G482 G481 G480	81
No Input	110001	G495 G494 G493 G492 G491 G490	82
No Input	110010	G505 G504 G503 G502 G501 G500	83
No Input	110011	G515 G514 G513 G512 G511 G510	84
No Input	110100	G525 G524 G523 G522 G521 G520	85
No Input	110101	G535 G534 G533 G532 G531 G530	86
No Input	110110	G545 G544 G543 G542 G541 G540	87
No Input	110111	G555 G554 G553 G552 G551 G550	88
No Input	111000	G565 G564 G563 G562 G561 G560	89
No Input	111001	G575 G574 G573 G572 G571 G570	90
No Input	111010	G585 G584 G583 G582 G581 G580	91
No Input	111011	G595 G594 G593 G592 G591 G590	92
No Input	111100	G605 G604 G603 G602 G601 G600	93
No Input	111101	G615 G614 G613 G612 G611 G610	94
No Input	111110	G625 G624 G623 G622 G621 G620	95
No Input	111111	G635 G634 G533 G632 G631 G630	96

B input (4bit) 12 bit/pixel -mode 4,096 colors	B input (5 bit) 16 bit/pixel -mode 65,536 colors	B output (6bit) 18 bit/pixel -mode 262,144 colors	RGBSET Parameter
0000	00000	B005 B004 B003 B002 B001 B000	97
0001	00001	B015 B014 B013 B012 B011 B010	98
0010	00010	B025 B024 B023 B022 B021 B020	99
0011	00011	B035 B034 B033 B032 B031 B030	100
0100	00100	B045 B044 B043 B042 B041 B040	101
0101	00101	B055 B054 B053 B052 B051 B050	102
0110	00110	B065 B064 B063 B062 B061 B060	103
0111	00111	B075 B074 B073 B072 B071 B070	104
1000	01000	B085 B084 B083 B082 B081 B080	105
1001	01001	B095 B094 B093 B092 B091 B090	106
1010	01010	B105 B104 B103 B102 B101 B100	107
1011	01011	B115 B114 B113 B112 B111 B110	108
1100	01100	B125 B124 B123 B122 B121 B120	109
1101	01101	B135 B134 B133 B132 B131 B130	110
1110	01110	B145 B144 B143 B142 B141 B140	111
1111	01111	B155 B154 B153 B152 B151 B150	112
No Input	10000	B165 B164 B163 B162 B161 B160	113
No Input	10001	B175 B174 B173 B172 B171 B170	114
No Input	10010	B185 B184 B183 B182 B181 B180	115
No Input	10011	B195 B194 B193 B192 B191 B190	116
No Input	10100	B205 B204 B203 B202 B201 B200	117
No Input	10101	B215 B214 B213 B212 B211 B210	118
No Input	10110	B225 B224 B223 B222 B221 B220	119
No Input	10111	B235 B234 B233 B232 B231 B230	120
No Input	11000	B245 B244 B243 B242 B241 B240	121
No Input	11001	B255 B254 B253 B252 B251 B250	122
No Input	11010	B265 B264 B263 B262 B261 B260	123
No Input	11011	B275 B274 B273 B272 B271 B270	124
No Input	11100	B285 B284 B283 B282 B281 B280	125
No Input	11101	B295 B294 B293 B292 B291 B290	126
No Input	11110	B305 B304 B303 B302 B301 B300	127
No Input	11111	B315 B314 B313 B312 B311 B310	128

6. Display Data GRAM

The display data RAM stores display dots and consists of 384,912 bits (132x18x162 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

6.1 Display data GRAM mapping

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **CASET's SC, EC** and **PASET's SP, EP**, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

0000H	0001H	0002H	0003H	---------	0080H	0081H	0082H	0083H
0100H	0101H	0102H	0103H	---------	0180H	0181H	0182H	0183H
0200H	0201H	0202H	0203H	---------	0280H	0281H	0282H	0283H
0300H	0301H	0302H	0303H	---------	0380H	0381H	0382H	0383H
0400H	0401H	0402H	0403H	---------	0480H	0481H	0482H	0483H
0500H	0501H	0502H	0503H	---------	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮
9C00H	9C01H	9C02H	9C03H	---------	9C80H	9C81H	9C82H	9C83H
9D00H	9D01H	9D02H	9D03H	---------	9D80H	9D81H	9D82H	9D83H
9E00H	9E01H	9E02H	9E03H	---------	9E80H	9E81H	9E82H	9E83H
9F00H	9F01H	9F02H	9F03H	---------	9F80H	9F81H	9F82H	9F83H
A000H	A001H	A002H	A003H	---------	A080H	A081H	A082H	A083H
A100H	A101H	A102H	A103H	---------	A180H	A181H	A182H	A183H

Table 6.1 GRAM address for display panel position

6.2 Address counter (AC) of GRAM

The HX8353-D contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MADTCL's MV(B5), MX(B6)** and **MY(B7)** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the **CASET** (start: **SC**, end: **EC**) and the PASET (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

6.2.1 System interface to GRAM write direction

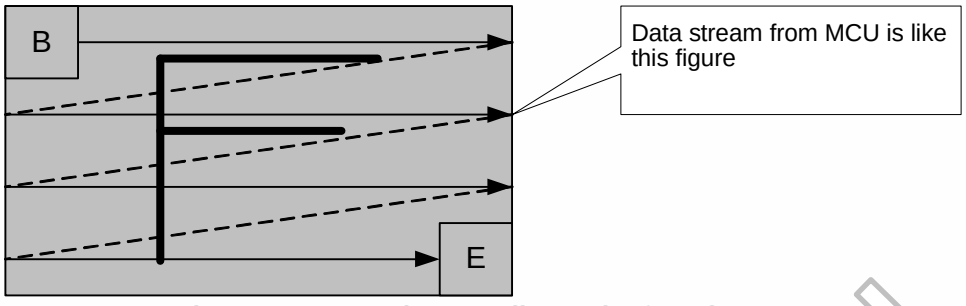


Figure 6.1 Image data sending order from host

The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MADTCL's MV(B5), MX(B6)** and **MY(B7)** bits setting

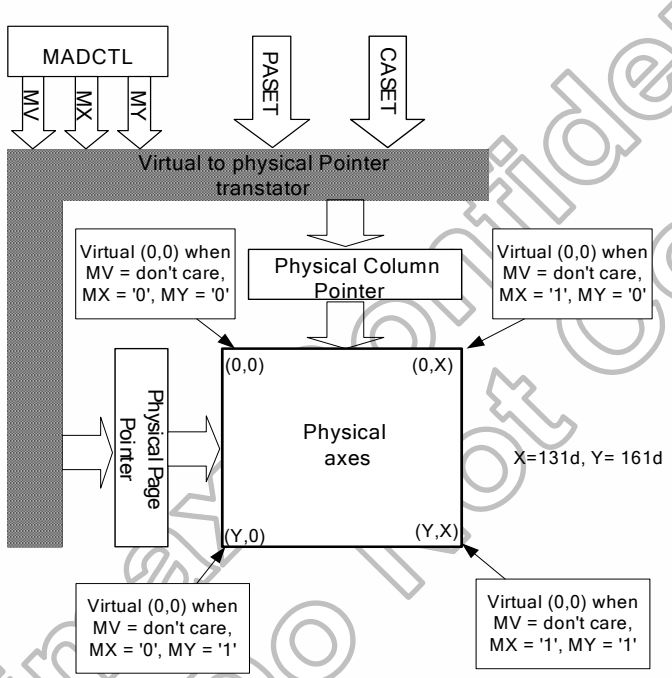


Figure 6.2 Image data writing control

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (Y - Physical Page Pointer)
0	1	0	Direct to (X-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (X - Physical Column Pointer)	Direct to (Y - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (Y - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (X-Physical Column Pointer)
1	1	1	Direct to (Y - Physical Page Pointer)	Direct to (X - Physical Column Pointer)

Table 6.2 CASET and PASET control for physical column/page pointers

For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted.	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start Column"	Return to "Start Page"

Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5.

Table 6.3 Rules for updating GRAM order

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

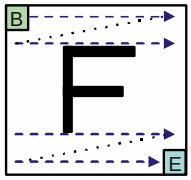
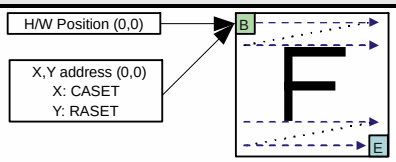
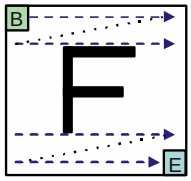
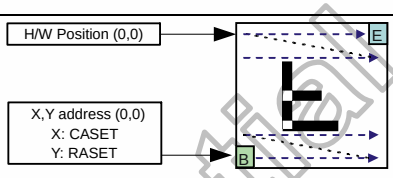
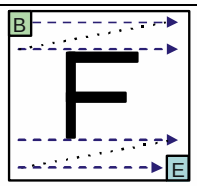
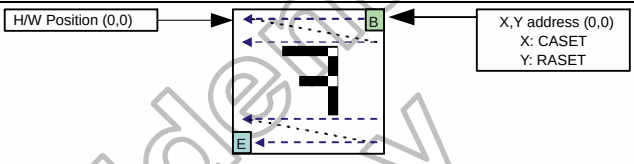
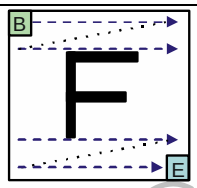
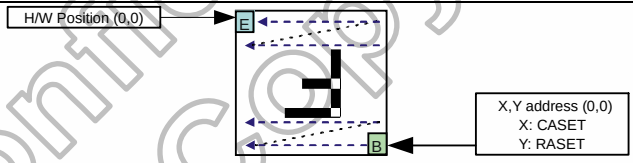
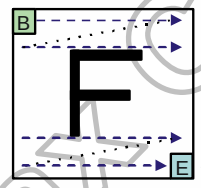
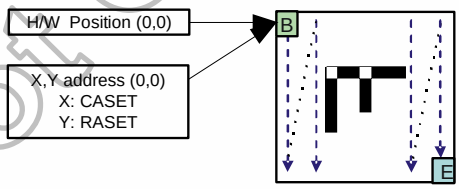
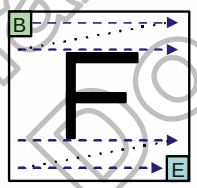
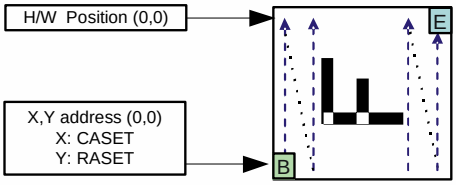
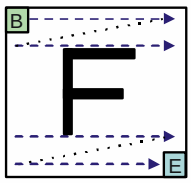
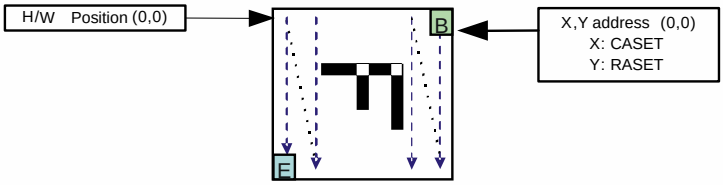
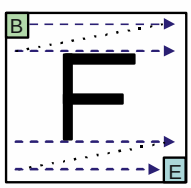
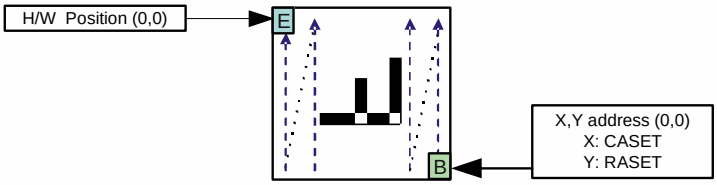
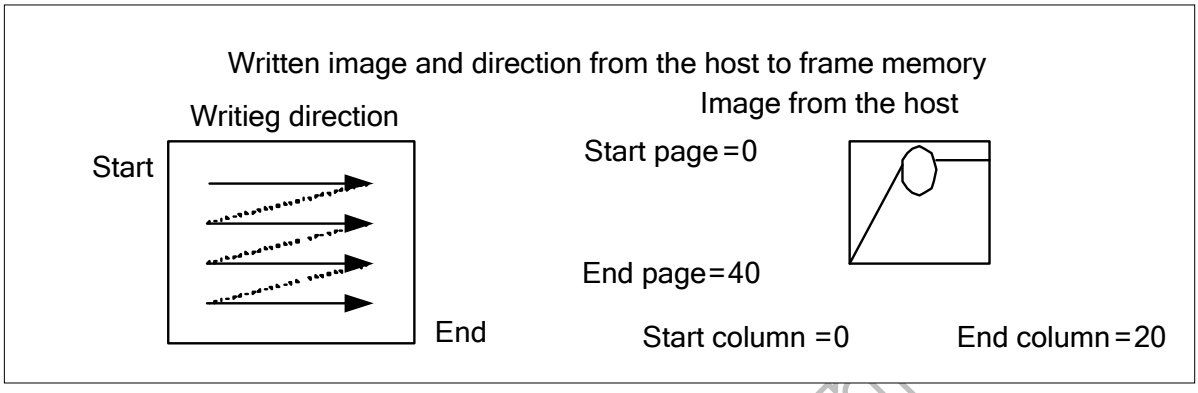
Display Data Direction	MADCTR parameter MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
Normal	0	0	0		
Y-Invert	0	0	1		
X-Invert	0	1	0		
X-Invert Y-Invert	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange X-invert	1	0	1		
X-Y Exchange Y-invert	1	1	0		
X-Y Exchange X-invert Y-invert	1	1	1		

Table 6.4 Address direction settings

Example for rotation with MY, MX and MV

This example is using following values: start page=0, end page=40, start column=0 and end column=20=> commands: page address set (0, 40) and column address set (0, 20). The sent figure is as follows and its sending order is as follows.



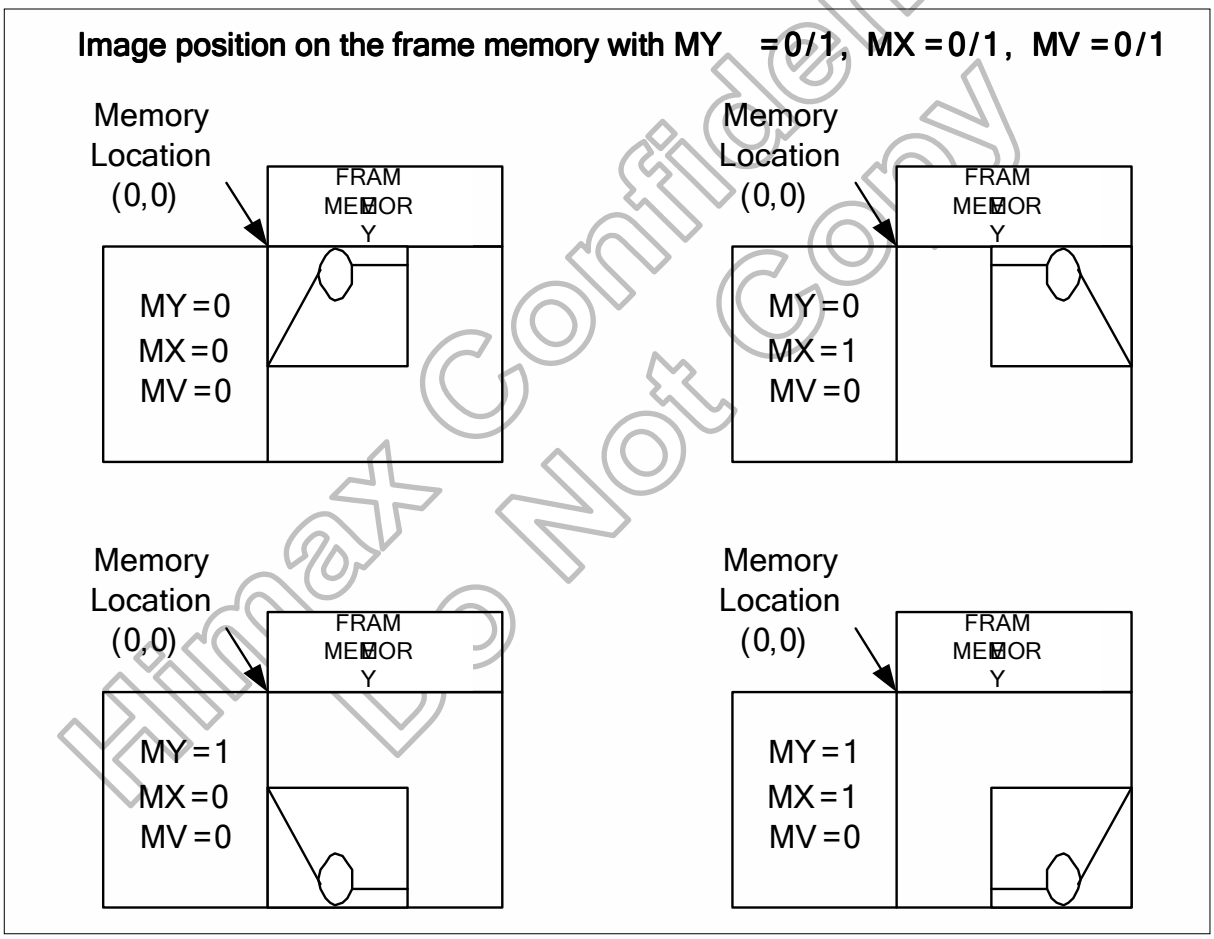
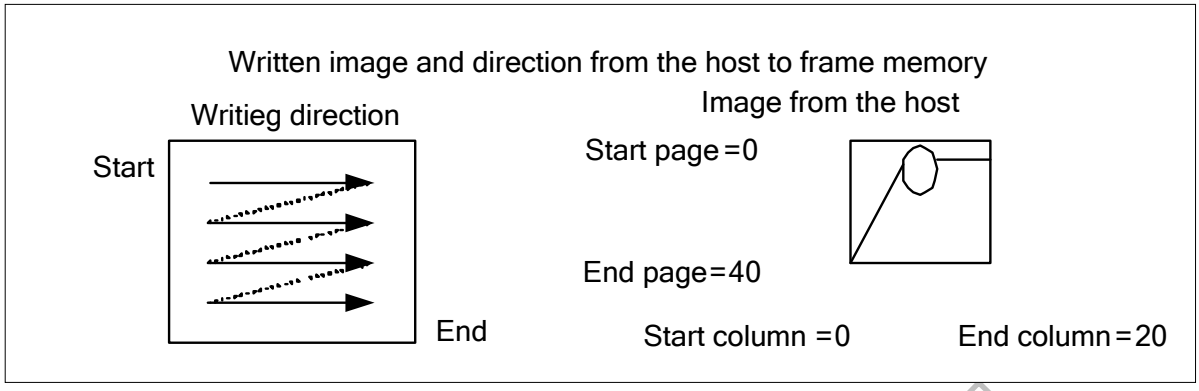


Figure 6.3 Example for rotation with MY, MX and MV – 1



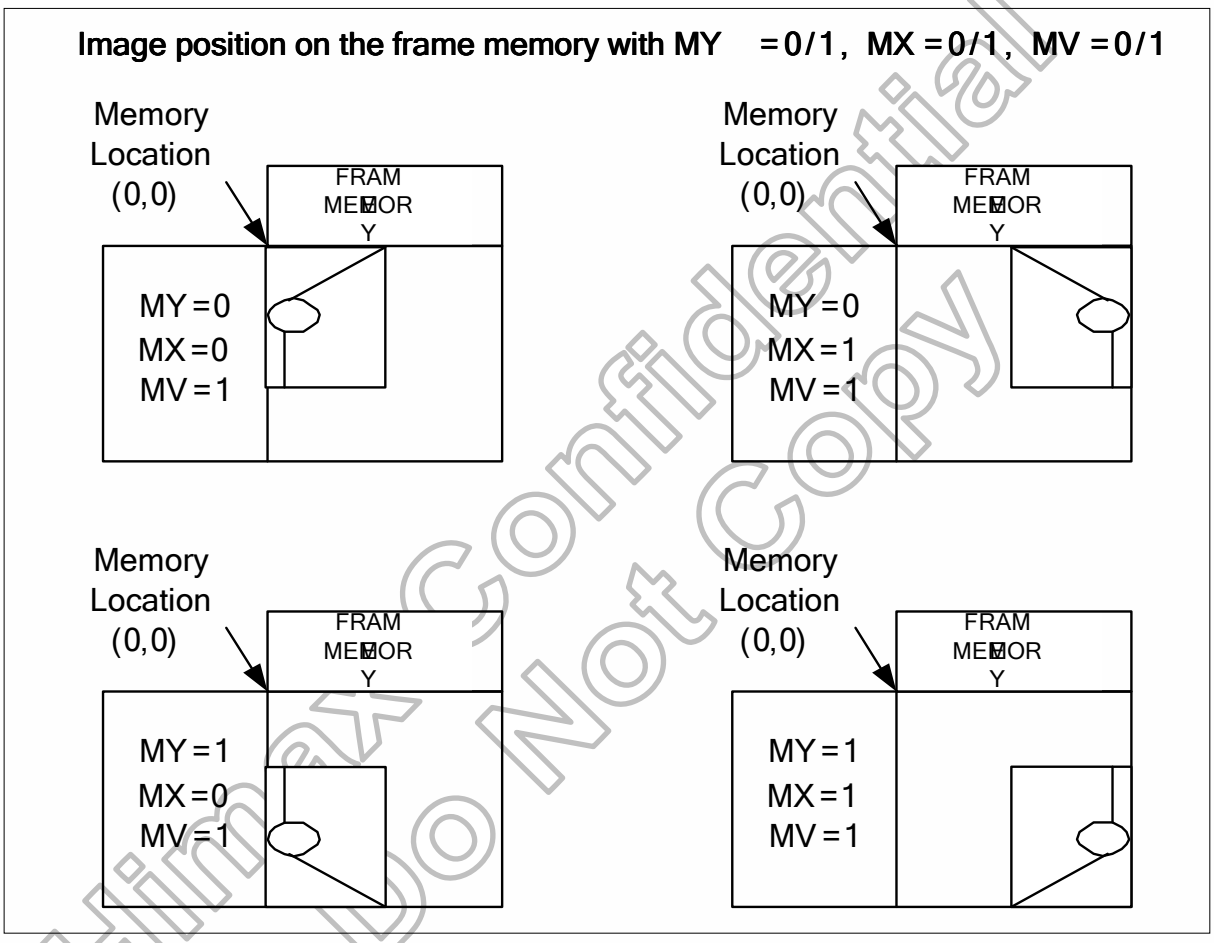


Figure 6.4 Example for rotation with MY, MX and MV – 2

6.3 Source, gate and memory map

6.3.1 When using 132 x 162 GRAM resolution, display resolution 132RGB x 162 (RSO[2:0]=3'b000 & STE_SEL=0)

Source Out	S1	S2	S3	S4	S5	S6	RGB Order —— :RGB=0 ----- :RGB=1	S391	S392	S393	S394	S395	S396
RA MY=0	RA MY=1													
0	161	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	–	$R130_{5-0}$	$G130_{5-0}$	$B130_{5-0}$	$R131_{5-0}$	$G131_{5-0}$	$B131_{5-0}$
1	160							–						
2	159							–						
3	158							–						
4	157							–						
5	156							–						
6	155							–						
7	154							–						
8	153							–						
9	152							–						
10	151							–						
11	150							–						
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:
154	7							–						
155	6							–						
156	5							–						
157	4							–						
158	3							–						
159	2							–						
160	1							–						
161	0							–						
CA MX=0		0			1				130			131		
CA MX=1		131			130				1			0		

SA ML=0	SA ML=1	Gate ML=0	Gate ML=1
0	161	G1	G162
1	160	G2	G161
2	159	G3	G160
3	158	G4	G159
4	157	G5	G158
5	156	G6	G157
6	155	G7	G156
7	154	G8	G155
8	153	G9	G154
9	152	G10	G153
10	151	G11	G152
11	150	G12	G151
:	:	:	:
154	7	G155	G8
155	6	G156	G7
156	5	G157	G6
157	4	G158	G5
158	3	G159	G4
159	2	G160	G3
160	1	G161	G2
161	0	G162	G1

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.5 Memory map, 132 x 162 GRAM resolution, display resolution 132RGB x 162

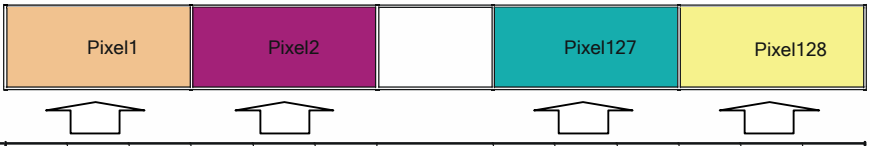
6.3.2 When using 132 x 162 GRAM resolution, display resolution 128RGB x 160 (RSO[2:0]=3'b000 & STE_SEL=1)

Source Out		S7	S8	S9	S10	S11	S12	RGB Order —— :RGB=0 ----- :RGB=1	S385	S386	S387	S388	S389	S390	SA		Gate	
RA															ML=0	ML=1	ML=0	ML=1
MY=0	MY=1																	
0	161	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	–	$R126_{5-0}$	$G126_{5-0}$	$B126_{5-0}$	$R127_{5-0}$	$G127_{5-0}$	$B127_{5-0}$	0	161	--	--
1	160							–							1	160	G2	G161
2	159							–							2	159	G3	G160
3	158							–							3	158	G4	G159
4	157							–							4	157	G5	G158
5	156							–							5	156	G6	G157
6	155							–							6	155	G7	G156
7	154							–							7	154	G8	G155
8	153							–							8	153	G9	G154
9	152							–							9	152	G10	G153
10	151							–							10	151	G11	G152
11	150							–							11	150	G12	G151
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
154	7							–							154	7	G155	G8
155	6							–							155	6	G156	G7
156	5							–							156	5	G157	G6
157	4							–							157	4	G158	G5
158	3							–							158	3	G159	G4
159	2							–							159	2	G160	G3
160	1							–							160	1	G161	G2
161	0							–							161	0	--	--
CA	MX=0	0			1				126			127						
	MX=1	127			126				1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.6 Memory map, 132 x 162 GRAM resolution, display resolution 128RGB x 160

6.3.3 When using 128 x 128 GRAM resolution, display resolution 128RGB x 128 (RSO[2:0]=3'b001)

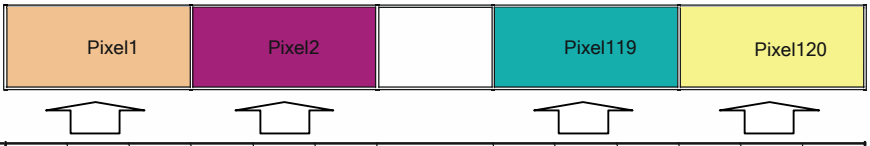


Source Out		S7	S8	S9	S10	S11	S12		S385	S386	S387	S388	S389	S390	SA		Gate	
RA								RGB Order —— :RGB=0 ----- :RGB=1										
MY=0	MY=1														ML=0	ML=1	ML=0	ML=1
0	127	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	–	$R126_{5-0}$	$G126_{5-0}$	$B126_{5-0}$	$R127_{5-0}$	$G127_{5-0}$	$B127_{5-0}$	0	127	G2	G129
1	126							–							1	126	G3	G128
2	125							–							2	125	G4	G127
3	124							–							3	124	G5	G126
4	123							–							4	123	G6	G125
5	122							–							5	122	G7	G124
6	121							–							6	121	G8	G123
7	120							–							7	120	G9	G122
8	119							–							8	119	G10	G121
9	118							–							9	118	G11	G120
10	117							–							10	117	G12	G119
11	116							–							11	116	G13	G118
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
120	7							–							120	7	G122	G9
121	6							–							121	6	G123	G8
122	5							–							122	5	G124	G7
123	4							–							123	4	G125	G6
124	3							–							124	3	G126	G5
125	2							–							125	2	G127	G4
126	1							–							126	1	G128	G3
127	0							–							127	0	G129	G2
CA	MX=0	0			1				126			127						
	MX=1	127			126				1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.7 Memory map, 128 x 128 GRAM resolution, display resolution 128RGB x 128

6.3.4 When using 120 x 160 GRAM resolution, display resolution 120RGB x 160 (RSO[2:0]=3'b010)



Source Out	S7	S8	S9	S10	S11	S12	RGB Order ——:RGB=0 ------:RGB=1	S361	S362	S363	S364	S365	S366	SA		Gate	
RA MY=0	RA MY=1													ML=0	ML=1	ML=0	ML=1
0	159	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	–	$R118_{5-0}$	$G118_{5-0}$	$B118_{5-0}$	$R119_{5-0}$	$G119_{5-0}$	$B119_{5-0}$	0	159	G2	G161
1	158							–							1	158	G3	G160
2	157							–							2	157	G4	G159
3	156							–							3	156	G5	G158
4	155							–							4	155	G6	G157
5	154							–							5	154	G7	G156
6	153							–							6	153	G8	G155
7	152							–							7	152	G9	G154
8	151							–							8	151	G10	G153
9	150							–							9	150	G11	G152
10	149							–							10	149	G12	G151
11	148							–							11	148	G13	G150
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
152	7							–							152	7	G154	G9
153	6							–							153	6	G155	G8
154	5							–							154	5	G156	G7
155	4							–							155	4	G157	G6
156	3							–							156	3	G158	G5
157	2							–							157	2	G159	G4
158	1							–							158	1	G160	G3
159	0							–							159	0	G161	G2
CA MX=0		0			1				118			119						
CA MX=1		119			118				1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.8 Memory map, 120 x 160 GRAM resolution, display resolution 120RGB x 160

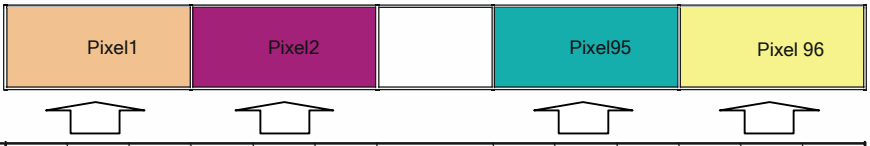
6.3.5 When using 128 x 160 GRAM resolution, display resolution 128RGB x 160 (RSO[2:0]=3'b011)

Source Out		S7	S8	S9	S10	S11	S12	RGB Order ——:RGB=0 -----:RGB=1	S385	S386	S387	S388	S389	S390	SA		Gate	
RA																		
MY=0	MY=1														ML=0	ML=1	ML=0	ML=1
0	159	$R0_{5-0}$	$G0_{5-0}$	$B0_{5-0}$	$R1_{5-0}$	$G1_{5-0}$	$B1_{5-0}$	–	$R126_{5-0}$	$G126_{5-0}$	$B126_{5-0}$	$R127_{5-0}$	$G127_{5-0}$	$B127_{5-0}$	0	159	G2	G161
1	158							–							1	158	G3	G160
2	157							–							2	157	G4	G159
3	156							–							3	156	G5	G158
4	155							–							4	155	G6	G157
5	154							–							5	154	G7	G156
6	153							–							6	153	G8	G155
7	152							–							7	152	G9	G154
8	151							–							8	151	G10	G153
9	150							–							9	150	G11	G152
10	149							–							10	149	G12	G151
11	148							–							11	148	G13	G150
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
152	7							–							152	7	G154	G9
153	6							–							153	6	G155	G8
154	5							–							154	5	G156	G7
155	4							–							155	4	G157	G6
156	3							–							156	3	G158	G5
157	2							–							157	2	G159	G4
158	1							–							158	1	G160	G3
159	0							–							159	0	G161	G2
CA	MX=0	0			1				126			127						
	MX=1	127			126				1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.9 Memory map, 128 x 160 GRAM resolution, display resolution 128RGB x 160

6.3.6 When using 96 x 68 GRAM resolution, display resolution 96RGB x 68 (RSO[2:0]=3'b100)

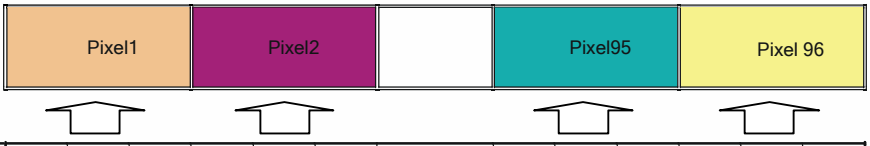


Source Out		S55	S56	S57	S58	S59	S60		S337	S338	S339	S340	S341	S342	SA		Gate	
RA								RGB Order										
MY=0	MY=1							—— :RGB=0 ----- :RGB=1							ML=0	ML=1	ML=0	ML=1
0	67	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	–	R94 5-0	G94 5-0	B94 5-0	R95 5-0	G95 5-0	B95 5-0	0	67	G1	G68
1	66							–							1	66	G2	G67
2	65							–							2	65	G3	G66
3	64							–							3	64	G4	G65
4	63							–							4	63	G5	G64
5	62							–							5	62	G6	G63
6	61							–							6	61	G7	G62
7	60							–							7	60	G8	G61
8	59							–							8	59	G9	G60
9	58							–							9	58	G10	G59
10	57							–							10	57	G11	G58
11	56							–							11	56	G12	G57
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
60	7							–							60	7	G61	G8
61	6							–							61	6	G62	G7
62	5							–							62	5	G63	G6
63	4							–							63	4	G64	G5
64	3							–							64	3	G65	G4
65	2							–							65	2	G66	G3
66	1							–							66	1	G67	G2
67	0							–							67	0	G68	G1
CA	MX=0	0			1				94			95						
	MX=1	95			94				1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.10 Memory map, 96 x 68 GRAM resolution, display resolution 96RGB x 68

6.3.7 When using 96 x 64 GRAM resolution, display resolution 96RGB x 64 (RSO[2:0]=3'b101)



Source Out		S55	S56	S57	S58	S59	S60		S337	S338	S339	S340	S341	S342	SA		Gate	
RA								RGB Order —— :RGB=0 ----- :RGB=1										
MY=0	MY=1														ML=0	ML=1	ML=0	ML=1
0	63	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	–	R94 5-0	G94 5-0	B94 5-0	R95 5-0	G95 5-0	B95 5-0	0	63	G1	G64
1	62							–							1	62	G2	G63
2	61							–							2	61	G3	G62
3	60							–							3	60	G4	G61
4	59							–							4	59	G5	G60
5	58							–							5	58	G6	G59
6	57							–							6	57	G7	G58
7	56							–							7	56	G8	G57
8	55							–							8	55	G9	G56
9	54							–							9	54	G10	G55
10	53							–							10	53	G11	G54
11	52							–							11	52	G12	G53
:	:	:	:	:	:	:	:	--	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:		:	:	:	:	:	:	:	:	:	:
56	7							–							56	7	G57	G8
57	6							–							57	6	G58	G7
58	5							–							58	5	G59	G6
59	4							–							59	4	G60	G5
60	3							–							60	3	G61	G4
61	2							–							61	2	G62	G3
62	1							–							62	1	G63	G2
63	0							–							63	0	G64	G1
CA	MX=0	0			1				94			95						
	MX=1	95			94				1			0						

Note: RA = Row Address,
CA = Column Address,
SA = Scan Address,
MX = Mirror X-axis (Column address direction parameter), DB6 parameter of MADCTL command
MY = Mirror Y-axis (Row address direction parameter), DB7 parameter of MADCTL command
ML = Scan direction parameter, DB4 parameter of MADCTL command
RGB= Red, Green and Blue pixel position change, DB3 parameter of MADCTL command

Figure 6.11 Memory map, 96 x 64 GRAM resolution, display resolution 96RGB x 64

6.3.8 Normal display on or partial display on

The HX8353-D has an internal GRAM that store 48,114 bytes pattern data, where one pixel is expressed by 18 bits.

6.3.8.1 132X162 GRAM resolution (size) (display resolution 132RGB x 162 (RSO[2:0]=3'b000 & STE_SEL=0)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--------- ---------	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A180H	A181H	A182H	A183H

LCD panel S/G pins	S1	S2	S3	---------	S394	S395	S396
G1	0000H			---------	0083H		
G2	0100H			---------	0183H		
G3	0200H			---------	0283H		
G4	0300H			---------	0383H		
G5	0400H			---------	0483H		
G6	0500H			---------	0583H		
⋮	⋮			---------	⋮		
G157	9C00H			---------	9C83H		
G158	9D00H			---------	9D83H		
G159	9E00H			---------	9E83H		
G160	9F00H			---------	9F83H		
G161	A000H			---------	A083H		
G162	A100H			---------	A183H		

Table 6.5 132X162 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=9Fh, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--------- ---------	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S1	S2	S3	---------	S394	S395	S396
Non-displa y area 2	**G1**	0000H			---------	0083H		
	G2	0100H			---------	0183H		
Display area 158 lines	**G3**	0200H			---------	0283H		
	G4	0300H			---------	0383H		
	G5	0400H			---------	0483H		
	G6	0500H			---------	0583H		
	⋮	⋮			---------	⋮		
	G157	9C00H			---------	9C83H		
	G158	9D00H			---------	9D83H		
	G159	9E00H			---------	9E83H		
	G160	9F00H			---------	9F83H		
Non-display area 2 lines	**G161**	A000H			---------	A083H		
	G162	A100H			---------	A183H		

Table 6.6 Partial area of 132X162 GRAM resolution

6.3.8.2 132X162 GRAM resolution (size) (display resolution 128RGB x 160 (RSO[2:0]=3'b000 & STE_SEL=1)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	---------	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A180H	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	---------	S388	S389	S390
G2	0000H			---------	0181H		
G3	0100H			---------	0281H		
G4	0200H			---------	0381H		
G5	0300H			---------	0481H		
G6	0400H			---------	0581H		
G7	0500H			---------	0681H		
⋮	⋮			---------	⋮		
G158	9C00H			---------	9D81H		
G159	9D00H			---------	9E81H		
G160	9E00H			---------	9F81H		
G161	9F00H			---------	A081H		

Table 6.7 132X162 GRAM resolution and 128X160 display resolution

(b) Partial display on

PSL[15:0]=03h, PEL[15:0]=9Eh, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--------- ---------	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	---------	S388	S389	S390
Non-display area 2 lines	**G2**	0102H			---------	0181H		
	G3	0202H			---------	0281H		
Display area 156 lines	**G4**	0302H			---------	0381H		
	G5	0402H			---------	0481H		
	G6	0502H			---------	0581H		
	G7	0602H			---------	0681H		
	⋮	⋮			---------	⋮		
	G158	9D02H			---------	9D81H		
	G159	9E02H			---------	9E81H		
Non-display area 2 lines	**G160**	9F02H			---------	9F81H		
	G161	A002H			---------	A081H		

Table 6.8 Partial area of 132X162 GRAM resolution and 128X160 display resolution

6.3.8.3 128X128 GRAM resolution (size) (display resolution 128RGB x 128 → RSO[2:0]=3'b001)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 7Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	---------	7Fh DB---DB 17 ---0	---------	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	007FH	---------	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	017FH	---------	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	027FH	---------	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	037FH	---------	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	047FH	---------	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	057FH	---------	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	---------	⋮	⋮	⋮
7Eh	7E00H	7E01H	7E02H	7E03H	---------	7E7FH	---------	7E81H	7E82H	7E83H
7Fh	7F00H	7F01H	7F02H	7F03H	---------	7E7FH	---------	7F81H	7F82H	7F83H
⋮	⋮	⋮	⋮	⋮	---------	⋮	---------	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C7FH	---------	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D7FH	---------	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E7FH	---------	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F7FH	---------	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A07FH	---------	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A17FH	---------	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	---------	S388	S389	S390
G2	0000H			---------	007FH		
G3	0100H			---------	017FH		
G4	0200H			---------	027FH		
G5	0300H			---------	037FH		
G6	0400H			---------	047FH		
G7	0500H			---------	057FH		
⋮	⋮			---------	⋮		
G126	7C00H			---------	7C7FH		
G127	7D00H			---------	7D7FH		
G128	7E00H			---------	7E7FH		
G129	7F00H			---------	7F7FH		

Table 6.9 128X128 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=7Dh, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	---------	7Fh DB---DB 17 ---0	---------	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	007FH	---------	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	017FH	---------	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	027FH	---------	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	037FH	---------	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	047FH	---------	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	057FH	---------	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	---------	⋮	⋮	⋮
7Eh	7E00H	7E01H	7E02H	7E03H	---------	7E7FH	---------	7E81H	7E82H	7E83H
7Fh	7F00H	7F01H	7F02H	7F03H	---------	7E7FH	---------	7F81H	7F82H	7F83H
⋮	⋮	⋮	⋮	⋮	---------	⋮	---------	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C7FH	---------	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D7FH	---------	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E7FH	---------	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F7FH	---------	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A07FH	---------	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A17FH	---------	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	---------	S387	S389	S390
Non-display area 2 lines	G2	0000H			---------	007FH		
	G3	0100H			---------	017FH		
Display area 124 lines	G4	0200H			---------	027FH		
	G5	0300H			---------	037FH		
	G6	0400H			---------	047FH		
	G7	0500H			---------	057FH		
	⋮	⋮			---------	⋮		
	G126	7C00H			---------	7C7FH		
	G127	7D00H			---------	7D7FH		
Non-display area 2 lines	G128	7E00H			---------	7E7FH		
	G129	7F00H			---------	7F7FH		

Table 6.10 Partial area of 128X128 GRAM resolution

6.3.8.4 120X160 GRAM resolution (size) (display resolution 120RGB x 160 → RSO[2:0]=3'b010)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 77h and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	---------	77h DB---DB 17 ---0	---------	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	0077H	---------	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	0177H	---------	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	0277H	---------	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	0377H	---------	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	0477H	---------	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	0577H	---------	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	---------	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C77H	---------	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D77H	---------	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E77H	---------	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F77H	---------	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A077H	---------	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A177H	---------	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	---------	S364	S365	S366
G2	0000H			---------	0077H		
G3	0100H			---------	0177H		
G4	0200H			---------	0277H		
G5	0300H			---------	0377H		
G6	0400H			---------	0477H		
G7	0500H			---------	0577H		
⋮	⋮			---------	⋮		
G158	9C00H			---------	9C77H		
G159	9D00H			---------	9D77H		
G160	9E00H			---------	9E77H		
G161	9F00H			---------	9F77H		

Table 6.11 120X160 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=9Dh, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	-------- --------	77h DB---DB 17 ---0	-------- --------	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	0077H	---------	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	0177H	---------	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	0277H	---------	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	0377H	---------	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	0477H	---------	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	0577H	---------	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	---------	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C77H	---------	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D77H	---------	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E77H	---------	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F77H	---------	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A077H	---------	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A177H	---------	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	---------	S364	S365	S366
Non-display area 2 lines	G2	0000H			---------	0077H		
	G3	0100H			---------	0177H		
Display area 156 lines	G4	0200H			---------	0277H		
	G5	0300H			---------	0377H		
	G6	0400H			---------	0477H		
	G7	0500H			---------	0577H		
	⋮	⋮			---------	⋮		
	G158	9C00H			---------	9C77H		
	G159	9D00H			---------	9D77H		
Non-display area 2 lines	G160	9E00H			---------	9E77H		
	G161	9F00H			---------	9F77H		

Table 6.12 Partial area of 120X160 GRAM resolution

6.3.8.5 128X160 GRAM resolution (size) (display resolution 128RGB x 160 (RSO[2:0]=3'b011)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--------- ---------	7Fh DB---DB 17 ---0	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	007FH	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	017FH	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	027FH	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	037FH	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	047FH	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	057FH	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C7FH	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D7FH	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E7FH	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F7FH	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A07FH	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A17FH	A180H	A181H	A182H	A183H

LCD panel S/G pins	S7	S8	S9	---------	S388	S389	S390
G2	0000H			---------	007FH		
G3	0100H			---------	017FH		
G4	0200H			---------	027FH		
G5	0300H			---------	037FH		
G6	0400H			---------	047FH		
G7	0500H			---------	057FH		
⋮	⋮			---------	⋮		
G158	9C00H			---------	9C7FH		
G159	9D00H			---------	9D7FH		
G160	9E00H			---------	9E7FH		
G161	9F00H			---------	9F7FH		

Table 6.13 128X160 GRAM resolution

(b) Partial display on

PSL[15:0]=02h, PEL[15:0]=9Dh, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--------- ---------	7Fh DB---DB 17 ---0	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---------	007FH	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---------	017FH	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---------	027FH	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---------	037FH	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---------	047FH	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---------	057FH	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---------	⋮	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---------	9C7FH	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---------	9D7FH	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---------	9E7FH	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---------	9F7FH	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---------	A07FH	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---------	A17FH	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S7	S8	S9	---------	S388	S389	S390
Non-display area 2 lines	G2	0000H			---------	007FH		
	G3	0100H			---------	017FH		
Display area 156 lines	G4	0200H			---------	027FH		
	G5	0300H			---------	037FH		
	G6	0400H			---------	047FH		
	G7	0500H			---------	057FH		
	⋮	⋮			---------	⋮		
	G158	9C00H			---------	9C7FH		
	G159	9D00H			---------	9D7FH		
Non-display area 2 lines	G160	9E00H			---------	9E7FH		
	G161	9F00H			---------	9F7FH		

Table 6.14 Partial area of 128X160 GRAM resolution

6.3.8.6 96x68 Resolution (RSO[2:0]=3'b100)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 5Fh and page pointer is 00h to 43h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	---	5Dh DB---DB 17 ---0	5Eh DB---DB 17 ---0	5Fh DB---DB 17 ---0	---	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
42h	4200H	4201H	4102H	4103H	---	425DH	425EH	425FH	---	4280H	4281H	4282H	4283H
43h	4300H	4301H	4302H	4303H	---	435DH	435EH	435FH	---	4380H	4381H	4382H	4383H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

LCD panel S/G pins	S55	S56	S57		S340	S341	S342
G1	0000H		---------		005FH		
G2	0100H		---------		015FH		
G3	0200H		---------		025FH		
G4	0300H		---------		035FH		
G5	0400H		---------		045FH		
G6	0500H		---------		055FH		
⋮	⋮		⋮		⋮		
G67	4200H		---------		425FH		
G68	4300H		---------		435FH		

Table 6.15 96X68 GRAM resolution

(b) Partial display on

PSL[15:0]=02, PEL[15:0]=41, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--- ---	5Dh DB---DB 17 ---0	5Eh DB---DB 17 ---0	5Fh DB---DB 17 ---0	--- ---	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
42h	4200H	4201H	4202H	4203H	---	425DH	425EH	425FH	---	4280H	4281H	4282H	4283H
43h	4300H	4301H	4302H	4303H	---	435DH	435EH	435FH	---	4380H	4381H	4382H	4383H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S55	S56	S57		S340	S341	S342
Non-display area 2 lines	G1	0000H			---------			005FH
	G2	0100H			---------			015FH
Display area 64 lines	G3	0200H			---------			025FH
	G4	0300H			---------			035FH
	G5	0400H			---------			045FH
	G6	0500H			---------			055FH
	⋮	⋮			⋮			⋮
	G66	4100H			---------			415FH
Non-display area 2 lines	G67	4200H			---------			425FH
	G68	4300H			---------			435FH

Table 6.16 Partial area of 96X68 GRAM resolution

6.3.8.7 96x64 resolution (RSO[2:0]=3'b101)

(a) Normal display on

In this mode, contents of the frame memory within an area where column pointer is 00h to 5Fh and page pointer is 00h to 43h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	--- ---	5Dh DB---DB 17 ---0	5Eh DB---DB 17 ---0	5Fh DB---DB 17 ---0	--- ---	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
3Fh	3F00H	3F01H	3F02H	3F03H	---	3F5DH	3F5EH	3F5FH	---	3F80H	3F81H	3F82H	3F83H
40h	4000H	4001H	4002H	4003H	---	405DH	405EH	405FH	---	4080H	4081H	4082H	4083H
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

LCD panel S/G pins	S55	S56	S57		S340	S341	S342
G1	0000H		---------		005FH		
G2	0100H		---------		015FH		
G3	0200H		---------		025FH		
G4	0300H		---------		035FH		
G5	0400H		---------		045FH		
G6	0500H		---------		055FH		
⋮	⋮		⋮		⋮		
G63	3E00H		---------		3E5FH		
G64	3F00H		---------		3F5FH		

Table 6.17 96X64 GRAM resolution

(b) Partial display on

PSL[15:0]=02, PEL[15:0]=3D, ML=0.

GRAM	00h DB---DB 17 ---0	01h DB---DB 17 ---0	02h DB---DB 17 ---0	03h DB---DB 17 ---0	---	5Dh DB---DB 17 ---0	5Eh DB---DB 17 ---0	5Fh DB---DB 17 ---0	---	80h DB---DB 17 ---0	81h DB---DB 17 ---0	82h DB---DB 17 ---0	83h DB---DB 17 ---0
00h	0000H	0001H	0002H	0003H	---	005DH	005EH	005FH	---	0080H	0081H	0082H	0083H
01h	0100H	0101H	0102H	0103H	---	015DH	015EH	015FH	---	0180H	0181H	0182H	0183H
02h	0200H	0201H	0202H	0203H	---	025DH	025EH	025FH	---	0280H	0281H	0282H	0283H
03h	0300H	0301H	0302H	0303H	---	035DH	035EH	035FH	---	0380H	0381H	0382H	0383H
04h	0400H	0401H	0402H	0403H	---	045DH	045EH	045FH	---	0480H	0481H	0482H	0483H
05h	0500H	0501H	0502H	0503H	---	055DH	055EH	055FH	---	0580H	0581H	0582H	0583H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
3Fh	3F00H	3F01H	3F02H	3F03H	---	3F5DH	3F5EH	3F5FH	---	3F80H	3F81H	3F82H	3F83H
40h	4000H	4001H	4002H	4003H	---	405DH	405EH	405FH	---	4080H	4081H	4082H	4083H
41h	4100H	4101H	4102H	4103H	---	415DH	415EH	415FH	---	4180H	4181H	4182H	4183H
⋮	⋮	⋮	⋮	⋮	---	⋮	⋮	⋮	---	⋮	⋮	⋮	⋮
9Ch	9C00H	9C01H	9C02H	9C03H	---	9C5DH	9C5EH	9C5FH	---	9C80H	9C81H	9C82H	9C83H
9Dh	9D00H	9D01H	9D02H	9D03H	---	9D5DH	9D5EH	9D5FH	---	9D80H	9D81H	9D82H	9D83H
9Eh	9E00H	9E01H	9E02H	9E03H	---	9E5DH	9E5EH	9E5FH	---	9E80H	9E81H	9E82H	9E83H
9Fh	9F00H	9F01H	9F02H	9F03H	---	9F5DH	9F5EH	9F5FH	---	9F80H	9F81H	9F82H	9F83H
A0h	A000H	A001H	A002H	A003H	---	A05DH	A05EH	A05FH	---	A080H	A081H	A082H	A083H
A1h	A100H	A101H	A102H	A103H	---	A15DH	A15EH	A15FH	---	A180H	A181H	A182H	A183H

	LCD panel S/G pins	S55	S56	S57		S340	S341	S342
Non-display area 2 lines	G1	0000H		---------		005FH		
	G2	0100H		---------		015FH		
Display area 60 lines	G3	0200H		---------		025FH		
	G4	0300H		---------		035FH		
	G5	0400H		---------		045FH		
	G6	0500H		---------		055FH		
	⋮	⋮		⋮		⋮		
Non-display area 2 lines	G63	3E00H		---------		3E5FH		
	G64	3F00H		---------		3F5FH		

Table 6.18 Partial area of 96X64 GRAM resolution

6.4 Vertical scrolling display

The vertical scrolling display is specified by SCRLAR instruction (R33h) and VSCSAD instruction (R37h). The Vertical scrolling is only enable when using 132 x 162 GRAM resolution, display resolution 132RGB x 162
(RSO[2:0]=3'b000 & STE_SEL=0) and display resolution 128RGB x 160
(RSO[2:0]=3'b011)

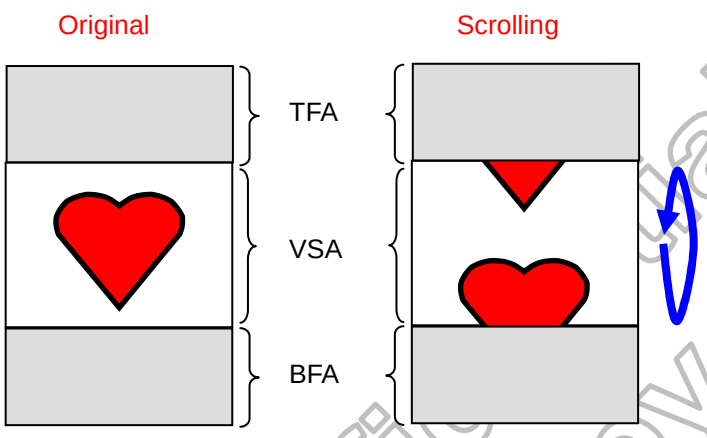


Figure 6.12 Vertical scrolling display

When RSO[2:0]=3'b000(132RGB x 162) and Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=162 (other setting is prohibited). In this case, scrolling is applied as shown below.

Example 1: RSO=3'b000(132RGB x 162), TFA =3, VSA=157, BFA=2, VSP=4, MADCTR(ML)=0: Scrolling

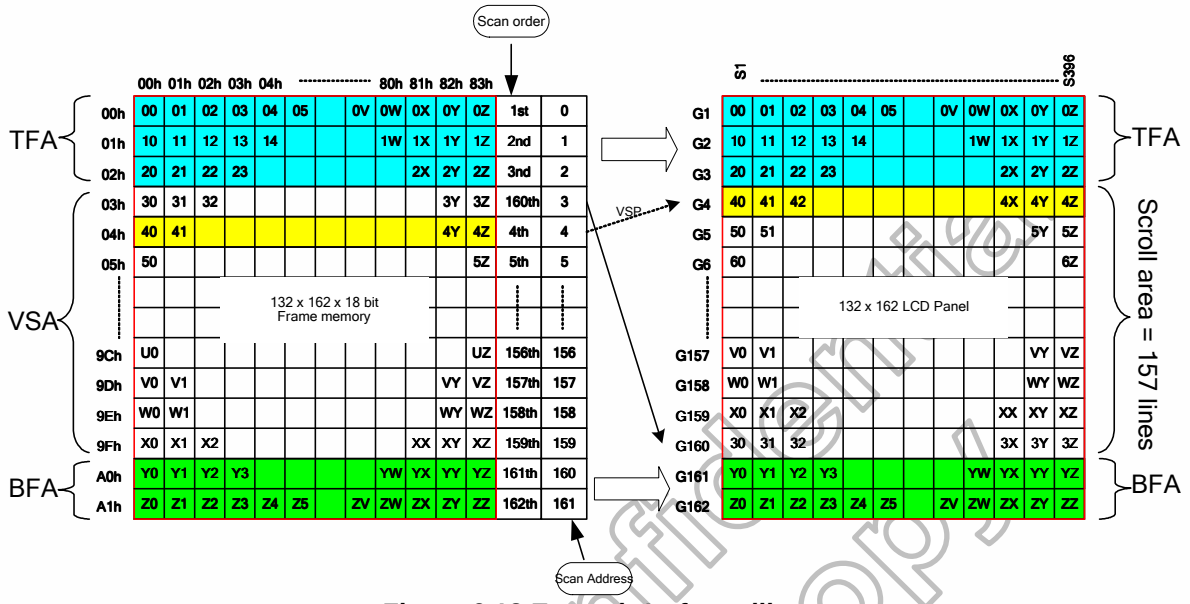


Figure 6.13 Example1 of scrolling

Example 2: RSO=3'b000(132RGB x 162), TFA =3, VSA=157, BFA=2, VSP=4, MADCTR (ML)=1: Scrolling (TFA and BFA are exchanged)

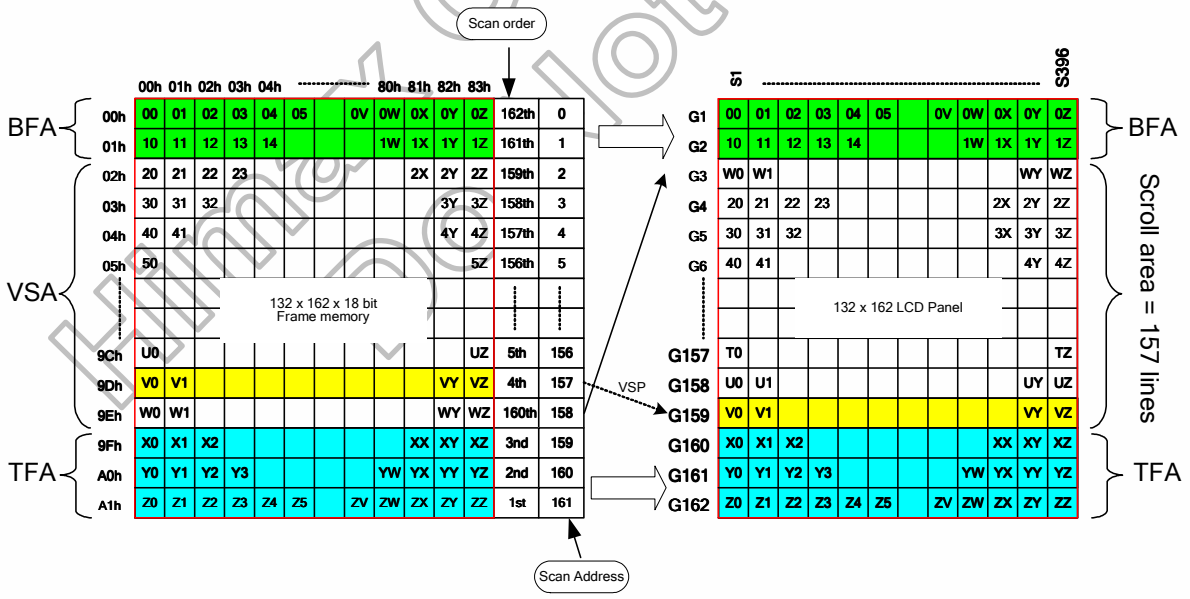


Figure 6.14 Example2 of scrolling

7. Functional Description

7.1 Internal Oscillator

The HX8353-D can oscillate an internal R-C oscillator for internal operation. Because the tolerance of internal oscillator frequency is ±5%, it can be adjusted by the **RADJ [1:0]** bits for initial 1.46MHz internal clock generation. With other dividers setting, the 1.46MHz internal clock can be used to generate clock for other part of the chip using.

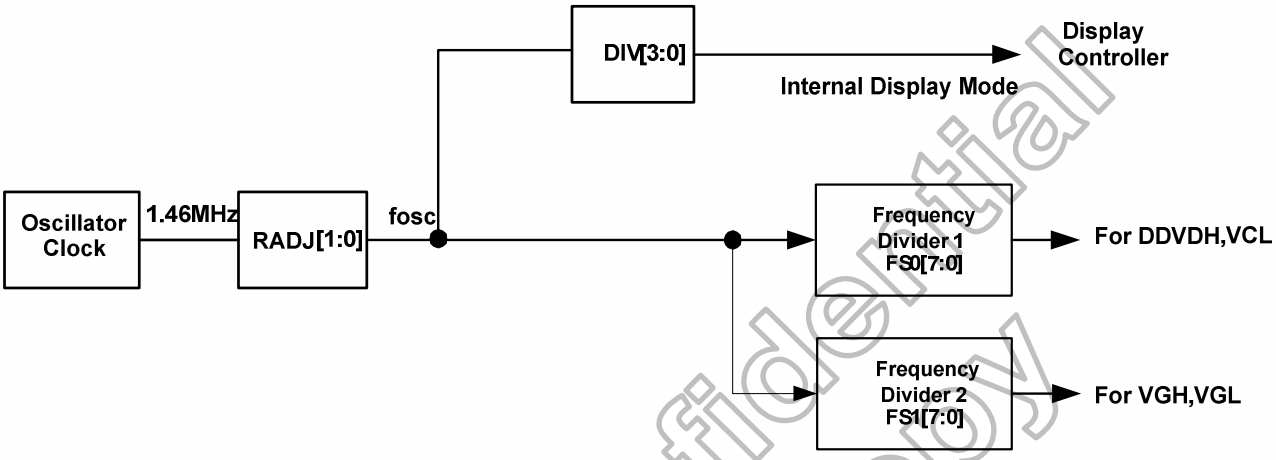


Figure 7.1 HX8353-D internal clock circuit

7.2 Gamma characteristic correction function

The HX8353-D incorporates gamma adjustment function for the 262,144-color display (64 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. These registers are available for both polarities.

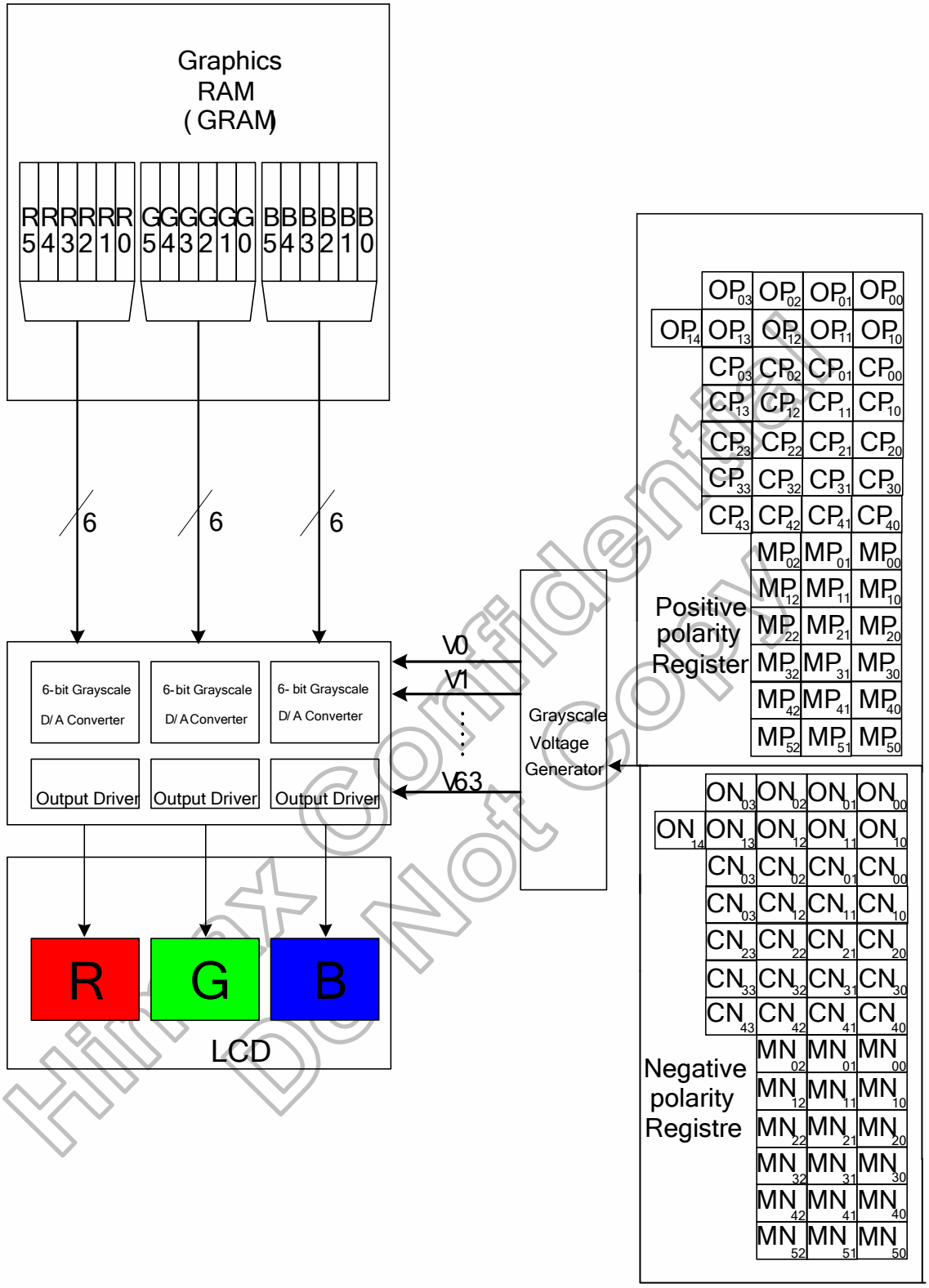


Figure 7.2 Grayscale control

7.2.1 Structure of grayscale voltage generator

Eight reference gamma voltages VgP/N(0, 1, 8, 20, 43, 55, 62, 63) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltage injected into specified node of grayscale voltage generator, totally 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel.

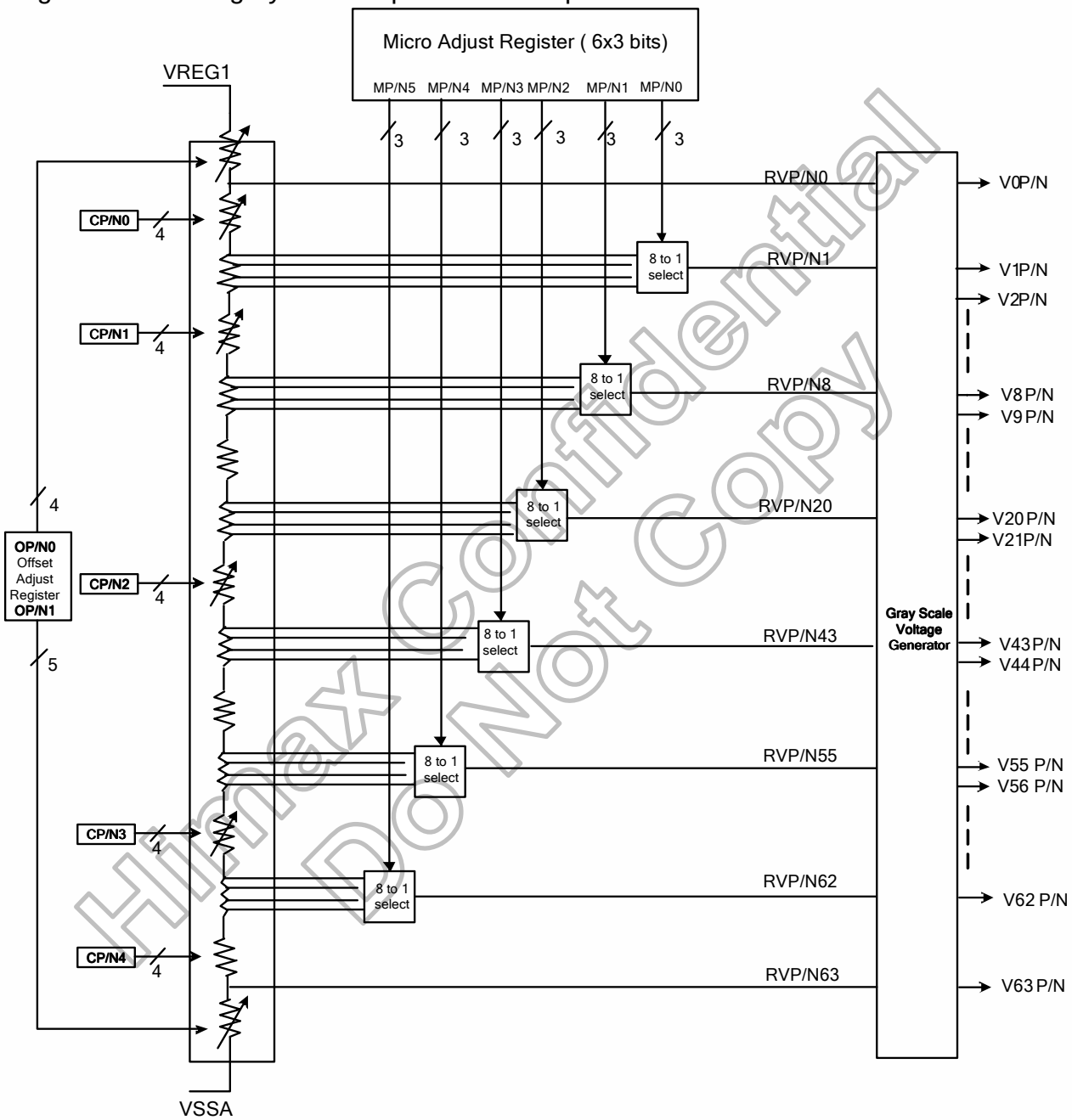


Figure 7.3 Structure of grayscale voltage generator

7.2.2 Gamma-characteristics adjustment register

This HX8353-D has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently. (R, G, and B are common.)

7.2.2.1 Offset adjustment registers 0/1

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities

7.2.2.2 Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by controlling these variable resisters in center of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

7.2.2.3 Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (MP/N0~5), each of which has 8 inputs and generate one reference voltage output (RVP/N 0, 1, 8, 20, 44, 56, 63, 64). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Description
Center Adjustment	CP/N0 3-0	Variable resistor (VRTP/N) for center adjustment
	CP/N1 3-0	Variable resistor (VRCP/N0)for center adjustment
	CP/N2 3-0	Variable resistor (VRMP/N) for center adjustment
	CP/N3 3-0	Variable resistor (VRCP/N1)for center adjustment
	CP/N4 3-0	Variable resistor (VRBP/N)for center adjustment
Macro Adjustment	MP/N0 2-0	8-to-1 selector (reference voltage level of grayscale 1)
	MP/N1 2-0	8-to-1 selector (reference voltage level of grayscale 8)
	MP/N2 2-0	8-to-1 selector (reference voltage level of grayscale 20)
	MP/N3 2-0	8-to-1 selector (reference voltage level of grayscale 43)
	MP/N4 2-0	8-to-1 selector (reference voltage level of grayscale 55)
	MP/N5 2-0	8-to-1 selector (reference voltage level of grayscale 62)
Offset Adjustment	OP/N0 3-0	Variable resistor (VRP/N0)for offset adjustment
	OP/N1 4-0	Variable resistor (VRP/N1)for offset adjustment

Table 7.1 Gamma-adjustment registers

7.2.3 Gamma resister stream and 8 to 1 selector

The block consists of two gamma resister streams, one is for positive polarity and the other is for negative polarity, each one includes eight gamma reference voltages (Vg(P/N)0, 1, 8, 20, 43, 55, 62, 63).

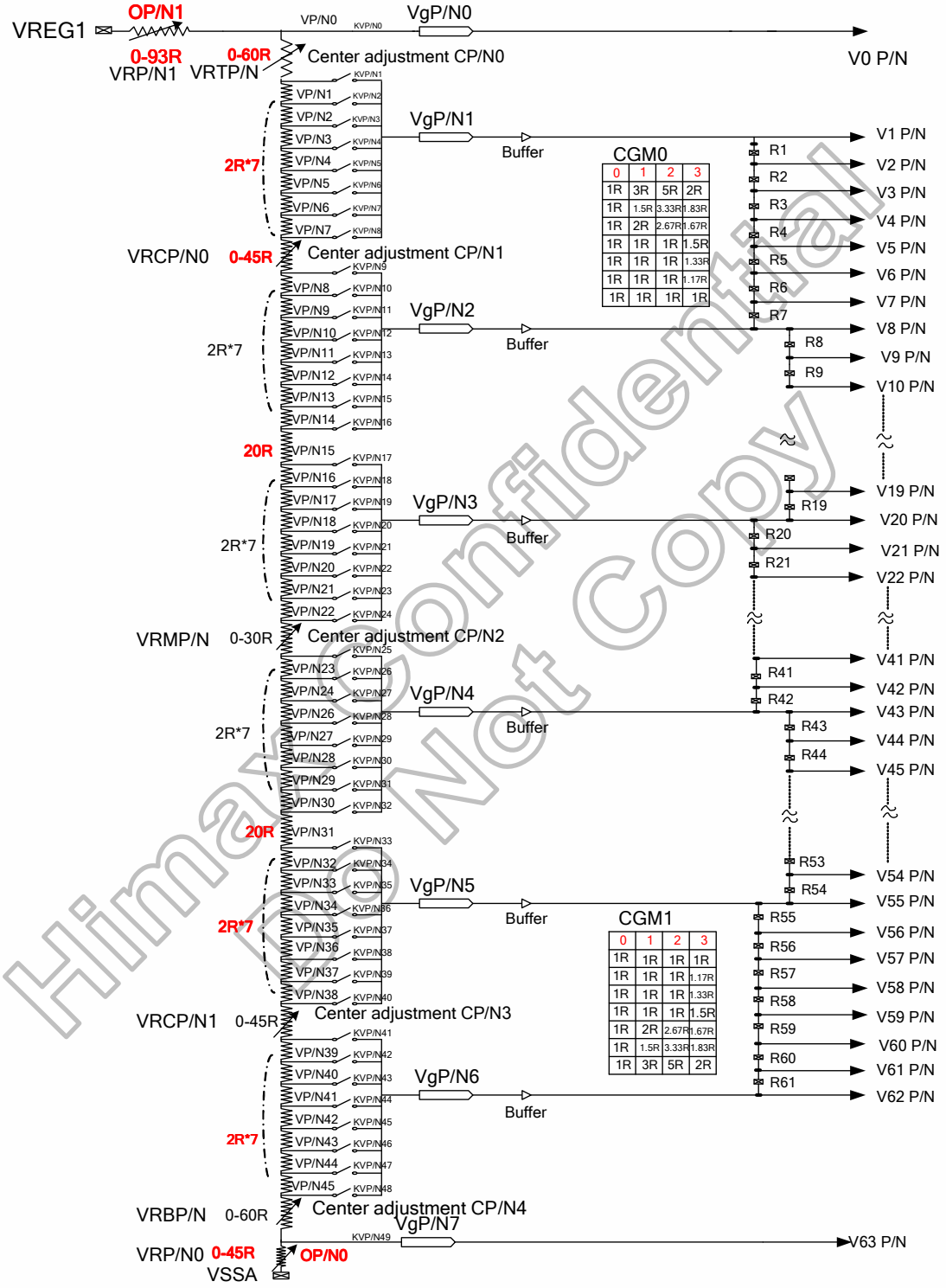


Figure 7.4 Gamma resister stream and gamma reference voltage

7.2.4 Variable resister

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationship is shown as below.

Value in Register OP/N0 3-0	Resistance VRP/N0
0000	**0R**
0001	**3R**
0010	**6R**
• •	
1101	**39R**
1110	**42R**
1111	**45R**

Value in Register OP/N1 4-0	Resistance VRP/N1
00000	**0R**
00001	**3R**
00010	**6R**
• •	
11101	**87R**
11110	**90R**
11111	**93R**

Table 7.2 Offset adjustment

Value in Register CP/N0 3-0	Resistance VRTP/N	Value in Register CP/N4 3-0	Resistance VRBP/N	Value in Register CP/N2 3-0	Resistance VRMP/N0
0000	**0R**	0000	0R	0000	0R
0001	**4R**	0001	4R	0001	2R
0010	**8R**	0010	8R	0010	4R
• •		• •	• •	• •	• •
1100		1100	48R	1100	24R
1101	**52R**	1101	52R	1101	26R
1110	**56R**	1110	56R	1110	28R
1111	**60R**	1111	60R	1111	30R

Value in Register CP/N3 3-0	Resistance VRCP/N1	Value in Register CP/N1 3-0	Resistance VRCP/N0
0000	0R	0000	0R
0001	3R	0001	3R
0010	6R	0010	6R
• •	• •	• •	• •
1100	36R	1100	36R
1101	39R	1101	39R
1110	42R	1110	42R
1111	45R	1111	45R

Table 7.3 Center adjustment

8 to 1 selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream, and outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. There are six 8 to 1 selectors and the relationship is shown as below.

Value in Register	Voltage level					
M(P/N) 2-0	Vg(P/N) 1	Vg(P/N) 2	Vg(P/N) 3	Vg(P/N) 4	Vg(P/N) 5	Vg(P/N) 6
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 7.4 Output voltage of 8 to 1 selector

The grayscale levels are determined by the following formulas.

Reference Voltage	Formula	
VgP/N0	-	VREG1-VD*VRP/N1 /sumRP/N
VgP1/VgN7	MP/N0 2-0=000	VREG1 –VD((VRP/N1+VRTP/N) /sumRP/N
	MP/N0 2-0=001	VREG1 –VD((VRP/N1+ VRTP/N +2R) /sumRP/N
	MP/N0 2-0=010	VREG1 –VD((VRP/N1+ VRTP/N +4R) /sumRP/N
	MP/N0 2-0=011	VREG1 –VD((VRP/N1+ VRTP/N +6R) /sumRP/N
	MP/N0 2-0=100	VREG1 –VD((VRP/N1+ VRTP/N +8R) /sumRP/N
	MP/N0 2-0=101	VREG1 –VD((VRP/N1+ VRTP/N +10R) /sumRP/N
	MP/N0 2-0=110	VREG1 –VD((VRP/N1+ VRTP/N +12R) /sumRP/N
	MP/N0 2-0=111	VREG1 –VD((VRP/N1+ VRTP/N +14R) /sumRP/N
VgP2/VgN2	MP/N1 2-0=000	VREG1 –VD((VRP/N1+ VRTP/N +14R+VRCP/N0) /sumRP/N
	MP/N1 2-0=001	VREG1 –VD((VRP/N1+ VRTP/N +16R+VRCP/N0) /sumRP/N
	MP/N1 2-0=010	VREG1 –VD((VRP/N1+ VRTP/N +18R+VRCP/N0) /sumRP/N
	MP/N1 2-0=011	VREG1 –VD((VRP/N1+ VRTP/N +20R+VRCP/N0) /sumRP/N
	MP/N1 2-0=100	VREG1 –VD((VRP/N1+ VRTP/N +22R+VRCP/N0) /sumRP/N
	MP/N1 2-0=101	VREG1 –VD((VRP/N1+ VRTP/N +24R+VRCP/N0) /sumRP/N
	MP/N1 2-0=110	VREG1 –VD((VRP/N1+ VRTP/N +26R+VRCP/N0) /sumRP/N
	MP/N1 2-0=111	VREG1 –VD((VRP/N1+ VRTP/N +28R+VRCP/N0) /sumRP/N
VgP3/VgN3	MP/N2 2-0=000	VREG1 –VD((VRP/N1+ VRTP/N+48R+VRCP/N0) /sumRP/N
	MP/N2 2-0=001	VREG1 –VD((VRP/N1+ VRTP/N+50R+VRCP/N0) /sumRP/N
	MP/N2 2-0=010	VREG1 –VD((VRP/N1+ VRTP/N+52R+VRCP/N0) /sumRP/N
	MP/N2 2-0=011	VREG1 –VD((VRP/N1+ VRTP/N+54R+VRCP/N0) /sumRP/N
	MP/N2 2-0=100	VREG1 –VD((VRP/N1+ VRTP/N+56R+VRCP/N0) /sumRP/N
	MP/N2 2-0=101	VREG1 –VD((VRP/N1+ VRTP/N+58R+VRCP/N0) /sumRP/N
	MP/N2 2-0=110	VREG1 –VD((VRP/N1+ VRTP/N+60R+VRCP/N0) /sumRP/N
	MP/N2 2-0=111	VREG1 –VD((VRP/N1+ VRTP/N+62R+VRCP/N0) /sumRP/N
VgP4/VgN4	MP/N3 2-0=000	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +62R+VRCP/N0) /sumRP/N
	MP/N3 2-0=001	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +64R+VRCP/N0) /sumRP/N
	MP/N3 2-0=010	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +66R+VRCP/N0) /sumRP/N
	MP/N3 2-0=011	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +68R+VRCP/N0) /sumRP/N
	MP/N3 2-0=100	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +70R+VRCP/N0) /sumRP/N
	MP/N3 2-0=101	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +72R+VRCP/N0) /sumRP/N
	MP/N3 2-0=110	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +74R+VRCP/N0) /sumRP/N
	MP/N3 2-0=111	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +76R+VRCP/N0) /sumRP/N
VgP5/VgN5	MP/N4 2-0=000	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +96R+VRCP/N0) /sumRP/N
	MP/N4 2-0=001	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +98R+VRCP/N0) /sumRP/N
	MP/N4 2-0=010	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +100R+VRCP/N0) /sumRP/N
	MP/N4 2-0=011	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +102R+VRCP/N0) /sumRP/N
	MP/N4 2-0=100	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +104R+VRCP/N0) /sumRP/N
	MP/N4 2-0=101	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +106R+VRCP/N0) /sumRP/N
	MP/N4 2-0=110	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +108R+VRCP/N0) /sumRP/N
	MP/N4 2-0=111	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +110R+VRCP/N0) /sumRP/N
VgP6/VgN6	MP/N5 2-0=000	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N+110R+VRCP/N0 +VRCP/N1) /sumRP/N
	MP/N5 2-0=001	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +112R+VRCP/N0+VRCP/N1) /sumRP/N
	MP/N5 2-0=010	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +114R+VRCP/N0+VRCP/N1) /sumRP/N
	MP/N5 2-0=011	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +116R+VRCP/N0+VRCP/N1) /sumRP/N
	MP/N5 2-0=100	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +118R+VRCP/N0+VRCP/N1) /sumRP/N
	MP/N5 2-0=101	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +120R+VRCP/N0+VRCP/N1) /sumRP/N
	MP/N5 2-0=110	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +122R+VRCP/N0+VRCP/N1) /sumRP/N
	MP/N5 2-0=111	VREG1 –VD((VRP/N1+ VRTP/N+ VRMP/N +124R+VRCP/N0+VRCP/N1) /sumRP/N
VgP7/VgN7	-	VREG1 –VD((VRP/N1+ VRBP/N+ VRTP/N+ VRMP/N +104R+VRCP/N0+VRCP/N1) /sumRP/N

SumRP=124R+VRP0+ VRP1+ VRTP+ VRCP0+VRMP+VRCP1+VRBP
SumRN=124R+ VRN0+ VRN1+ VRTN+ VRCN0+VRMN+VRCN1+VRBN
VD=(VREG1–VSSA)

Table 7.5 Voltage calculation formula

Grayscale Voltage	Formula
V0P/V63N	VgP/N0
V1P/V62N	VgP/N1
V2P/V61N	VgP/N2+(VgP/N1-VgP/N2)*CT1
V3P/V60N	VgP/N2+(VgP/N1-VgP/N2)*CT2
V4P/V59N	VgP/N2+(VgP/N1-VgP/N2)*CT3
V5P/V58N	VgP/N2+(VgP/N1-VgP/N2)*CT4
V6P/V57N	VgP/N2+(VgP/N1-VgP/N2)*CT5
V7P/V56N	VgP/N2+(VgP/N1-VgP/N2)*CT6
V8P/V55N	VgP/N2
V9P/V54N	VgP/N3+(VgP/N2-VgP/N3)*(22/24)
V10P/V53N	VgP/N3+(VgP/N2-VgP/N3)*(20/24)
V11P/V52N	VgP/N3+(VgP/N2-VgP/N3)*(18/24)
V12P/V51N	VgP/N3+(VgP/N2-VgP/N3)*(16/24)
V13P/V50N	VgP/N3+(VgP/N2-VgP/N3)*(14/24)
V14P/V49N	VgP/N3+(VgP/N2-VgP/N3)*(12/24)
V15P/V48N	VgP/N3+(VgP/N2-VgP/N3)*(10/24)
V16P/V47N	VgP/N3+(VgP/N2-VgP/N3)*(8/24)
V17P/V46N	VgP/N3+(VgP/N2-VgP/N3)*(6/24)
V18P/V45N	VgP/N3+(VgP/N2-VgP/N3)*(4/24)
V19P/V44N	VgP/N3+(VgP/N2-VgP/N3)*(2/24)
V20P/V43N	VgP/N3
V21P/V42N	VgP/N4+(VgP/N3-VgP/N4)*(22/23)
V22P/V41N	VgP/N4+(VgP/N3-VgP/N4)*(21/23)
V23P/V40N	VgP/N4+(VgP/N3-VgP/N4)*(20/23)
V24P/V39N	VgP/N4+(VgP/N3-VgP/N4)*(19/23)
V25P/V38N	VgP/N4+(VgP/N3-VgP/N4)*(18/23)
V26P/V37N	VgP/N4+(VgP/N3-VgP/N4)*(17/23)
V27P/V36N	VgP/N4+(VgP/N3-VgP/N4)*(16/23)
V28P/V35N	VgP/N4+(VgP/N3-VgP/N4)*(15/23)
V29P/V34N	VgP/N4+(VgP/N3-VgP/N4)*(14/23)
V30P/V33N	VgP/N4+(VgP/N3-VgP/N4)*(13/23)
V31P/V32N	VgP/N4+(VgP/N3-VgP/N4)*(12/23)

Grayscale Voltage	Formula
V32P/V31N	VgP/N4+(VgP/N3-VgP/N4)*(11/23)
V33P/V30N	VgP/N4+(VgP/N3-VgP/N4)*(10/23)
V34P/V29N	VgP/N4+(VgP/N3-VgP/N4)*(9/23)
V35P/V28N	VgP/N4+(VgP/N3-VgP/N4)*(8/23)
V36P/V27N	VgP/N4+(VgP/N3-VgP/N4)*(7/23)
V37P/V26N	VgP/N4+(VgP/N3-VgP/N4)*(6/23)
V38P/V25N	VgP/N4+(VgP/N3-VgP/N4)*(5/23)
V39P/V24N	VgP/N4+(VgP/N3-VgP/N4)*(4/23)
V40P/V23N	VgP/N4+(VgP/N3-VgP/N4)*(3/23)
V41P/V22N	VgP/N4+(VgP/N3-VgP/N4)*(2/23)
V42P/V21N	VgP/N4+(VgP/N3-VgP/N4)*(1/23)
V43P/V20N	VgP/N4
V44P/V19N	VgP/N5+(VgP/N4-VgP/N5)*(22/24)
V45P/V18N	VgP/N5+(VgP/N4-VgP/N5)*(20/24)
V46P/V17N	VgP/N5+(VgP/N4-VgP/N5)*(18/24)
V47P/V16N	VgP/N5+(VgP/N4-VgP/N5)*(16/24)
V48P/V15N	VgP/N5+(VgP/N4-VgP/N5)*(14/24)
V49P/V14N	VgP/N5+(VgP/N4-VgP/N5)*(12/24)
V50P/V13N	VgP/N5+(VgP/N4-VgP/N5)*(10/24)
V51P/V12N	VgP/N5+(VgP/N4-VgP/N5)*(8/24)
V52P/V11N	VgP/N5+(VgP/N4-VgP/N5)*(6/24)
V53P/V10N	VgP/N5+(VgP/N4-VgP/N5)*(4/24)
V54P/V9N	VgP/N5+(VgP/N4-VgP/N5)*(2/24)
V55P/V8N	VgP/N5
V56P/V7N	VgP/N6+(VgP/N5-VgP/N6)*CB1
V57P/V6N	VgP/N6+(VgP/N5-VgP/N6)*CB2
V58P/V5N	VgP/N6+(VgP/N5-VgP/N6)*CB3
V59P/V4N	VgP/N6+(VgP/N5-VgP/N6)*CB4
V60P/V3N	VgP/N6+(VgP/N5-VgP/N6)*CB5
V61P/V2N	VgP/N6+(VgP/N5-VgP/N6)*CB6
V62P/V1N	VgP/N6
V63P/V0N	VgP/N7

Table 7.6 Voltage calculation formula of grayscale voltage

CGM0[1:0]	"00"	"01"	"10"	"11"
CT1	6/7	7.5/10.5	10/15	8.5/10.5
CT2	5/7	6/10.5	6.67/15	6.67/10.5
CT3	4/7	4/10.5	4/15	5.0/10.5
CT4	3/7	3/10.5	3/15	3.5/10.5
CT5	2/7	2/10.5	2/15	2.17/10.5
CT6	1/7	1/10.5	1/15	1/10.5

CGM1[1:0]	"00"	"01"	"10"	"11"
CB1	6/7	9.5/10.5	14/15	9.5/10.5
CB2	5/7	8.5/10.5	13/15	8.33/10.5
CB3	4/7	7.5/10.5	12/15	7.0/10.5
CB4	3/7	6.5/10.5	11/15	5.5/10.5
CB5	2/7	4.5/10.5	8.33/15	3.83/10.5
CB6	1/7	3.0/10.5	5/15	2.0/10.5

Note: Negative gamma don't have CGM0/CGM1 setting, the ratio V2~V7 and V56~V61 is automatically mapping from positive side.

Table 7.7 Voltage calculation formula of grayscale voltage V2~V7 and V56~V61

Relationship between GRAM Data and Output Level (“Normally White Panel”, GRAM data=0)

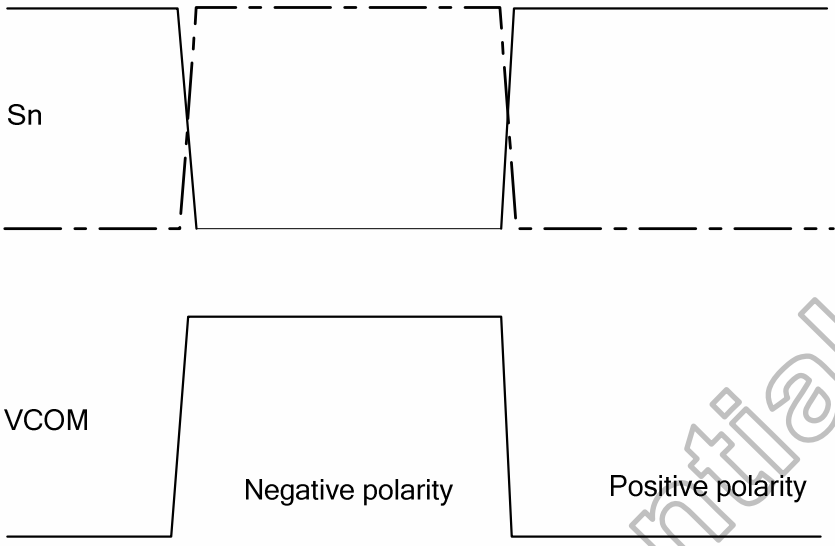


Figure 7.5 Relationship between source output and VCOM

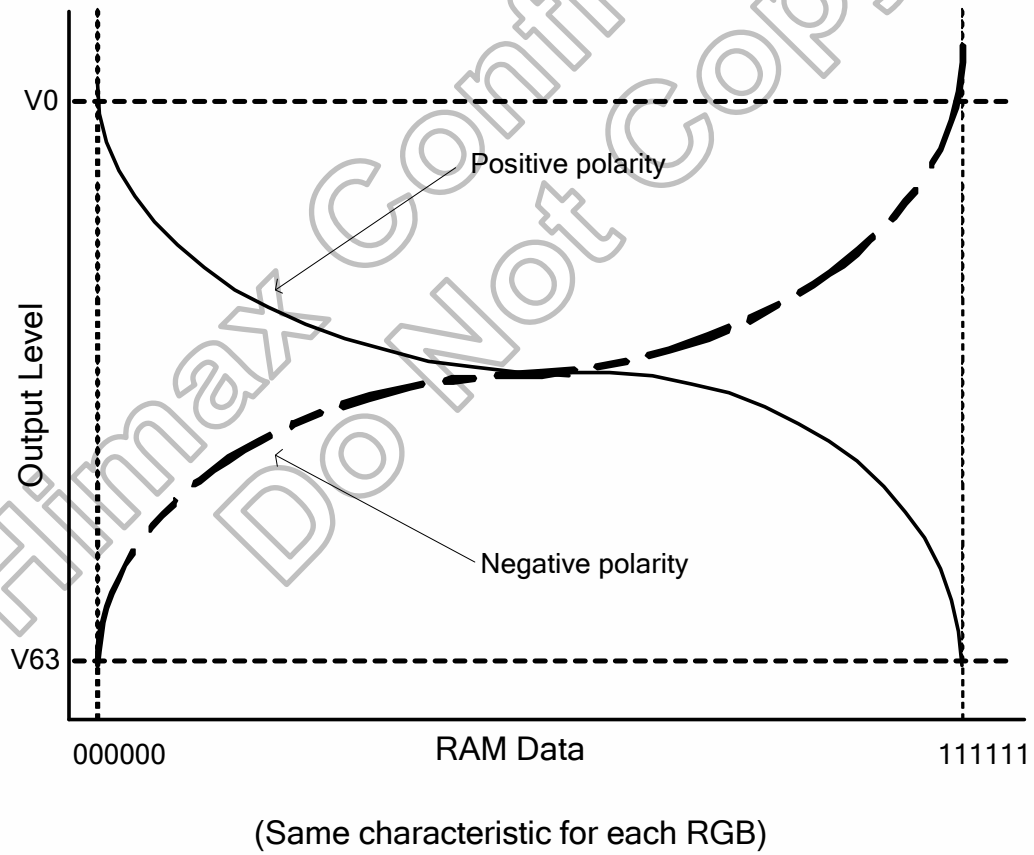


Figure 7.6 Relationship between GRAM data and output level (normal white panel REV_Panel=“0”)

Four-characteristic gamma curve selection

There are four kind of Gamma Curve is selected by GAMSET command. The parameter GC[7:0] is stored in internal register and used to select one set of gamma correction register.

GC_SEL="L":

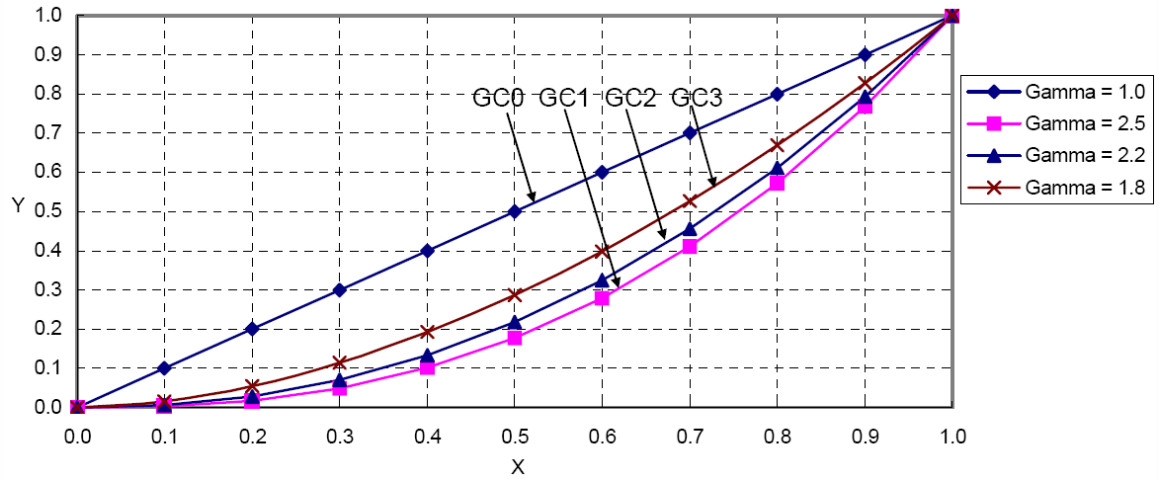


Figure 7.7 Gamma curve according to GC0 to GC3 bit (GC_SEL="L")

GC_SEL="H":

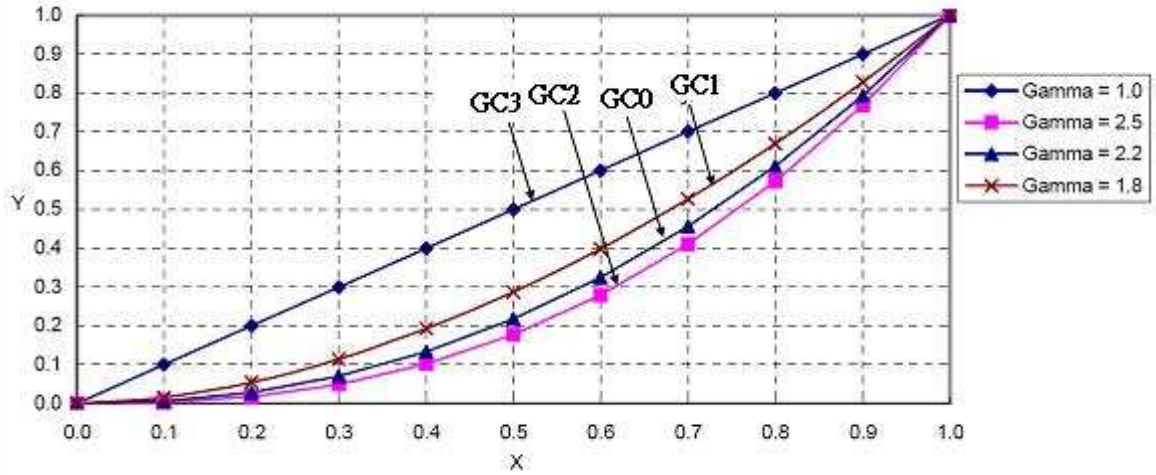


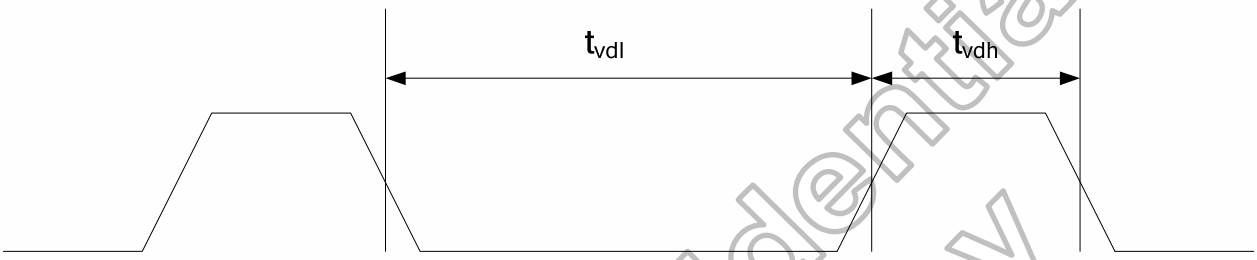
Figure 7.8 Gamma curve according to GC0 to GC3 bit (GC_SEL="H")

7.3 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line off & on commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

7.3.1 Tearing effect line modes

Mode 1: The Tearing Effect Output signal consists of V-Blanking Information only:

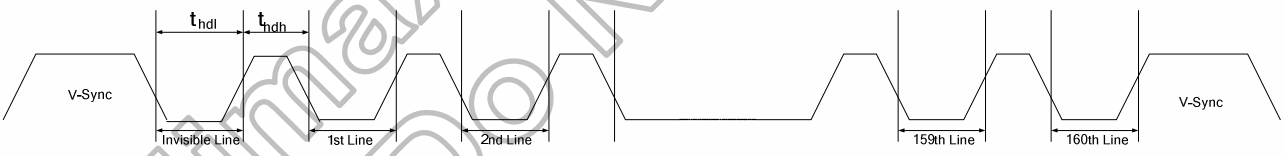


t_{vdh}= The LCD display is not updated from the Frame Memory
t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

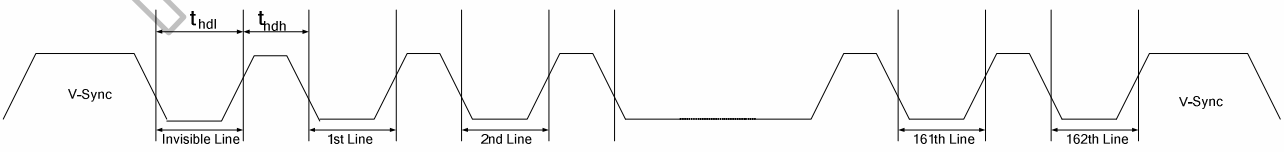
Figure 7.9 TE mode 1 output

Mode 2: The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and N H-sync pulses per field on different resolution.

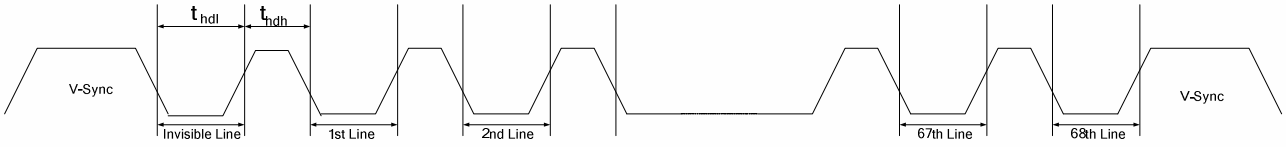
128RGBx160: N=160



132RGBx162: N=162



96x68: N=68



96x64: N=64

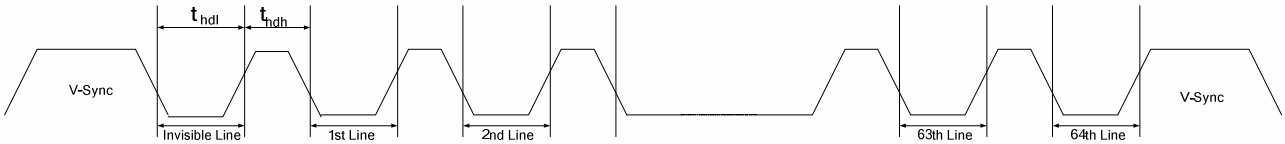
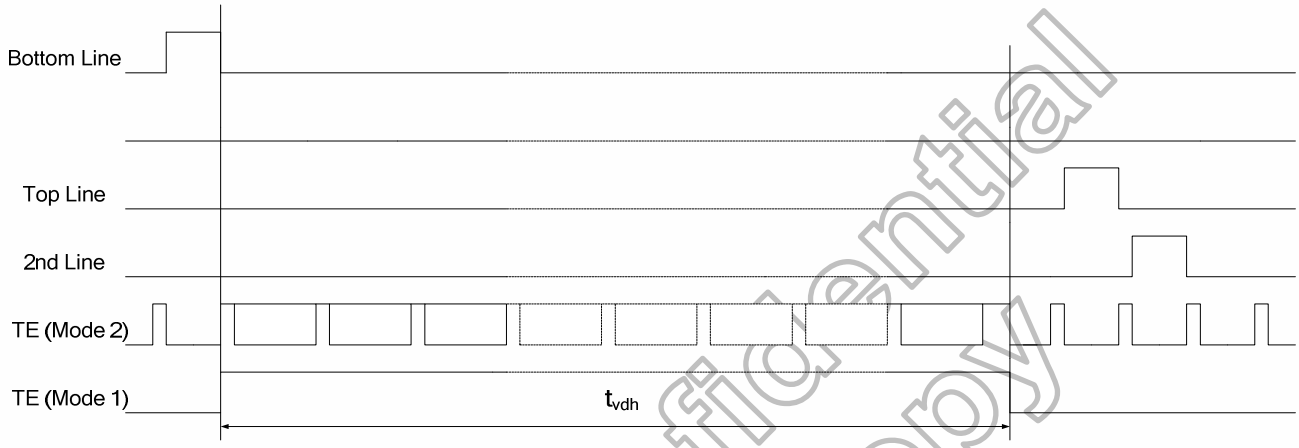


Figure 7.10 TE mode 2 output

t_{hdh}= The LCD display is not updated from the Frame Memory
t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above.)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

Figure 7.11 TE output waveform

7.3.2 Tearing effect line timing

The Tearing Effect signal is described below.

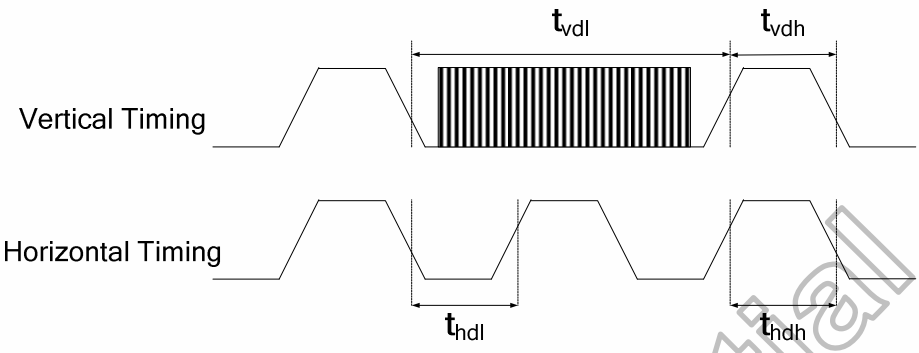


Figure 7.12 Waveform of tearing effect signal

Idle Mode Off (Frame Rate=60Hz)

Symbol	Parameter	Min.	Max.	Unit	Description
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	µs	-
thdl	Horizontal Timing Low Duration	TBD	-	µs	-
thdh	Horizontal Timing High Duration	TBD	500	µs	-

Table 7.8 AC characteristics of tearing effect signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

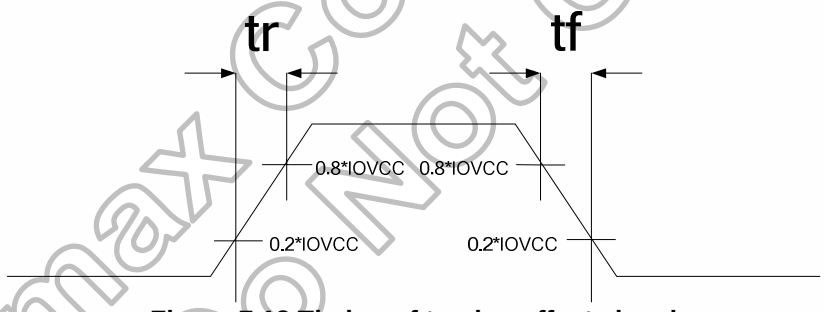


Figure 7.13 Timing of tearing effect signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

7.3.3 Example 1: MPU write is faster than panel read

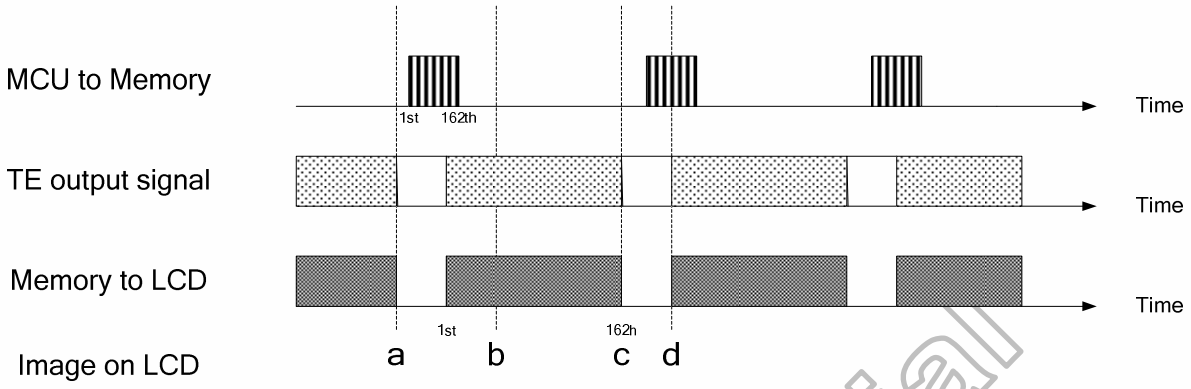


Figure 7.14 Timing of MPU write is faster than panel read

Data write to frame memory is now synchronized to the panel scan. It should be written during the vertical sync pulse of the tearing effect output line. This ensures that data is always written ahead of the panel scan and each panel frame refresh has a complete new image:

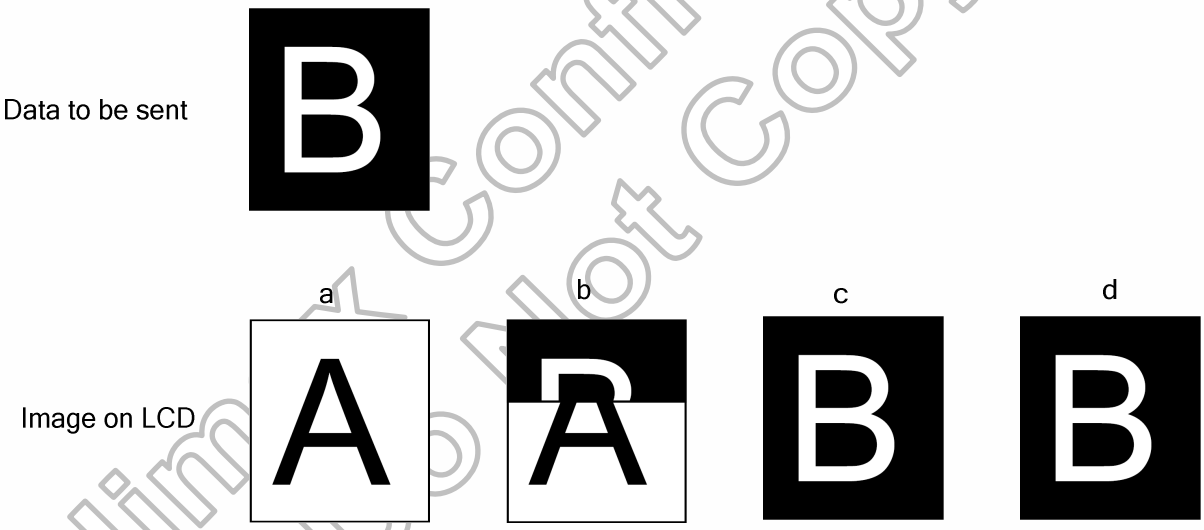


Figure 7.15 Display of MPU write is faster than panel read

7.3.4 Example 2: MPU write is slower than panel read

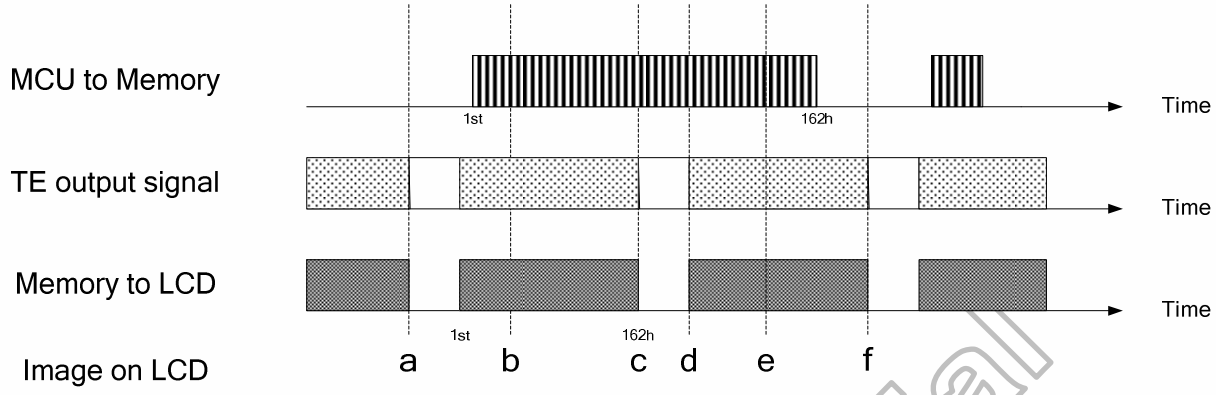


Figure 7.16 Timing of MPU write is slower than panel read

The MPU to frame memory write begins just after panel read has commenced i.e. after one horizontal sync pulse of the tearing effect output line. This allows time for the image to download behind the panel read pointer and finishing download during the subsequent frame before the read pointer "catches" the MPU to frame memory write position.

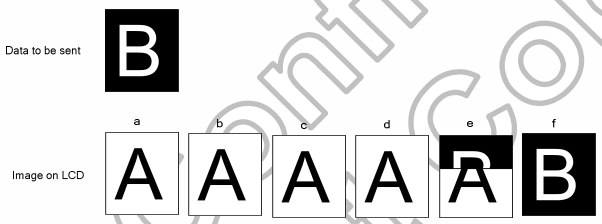


Figure 7.17 Display of MPU write is slower than panel read

7.4 Scan Mode Setting

HX8353-D can set internal register GS_PANEL bit to determine the pin assignment of gate. The GS_PANEL setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8353-D.

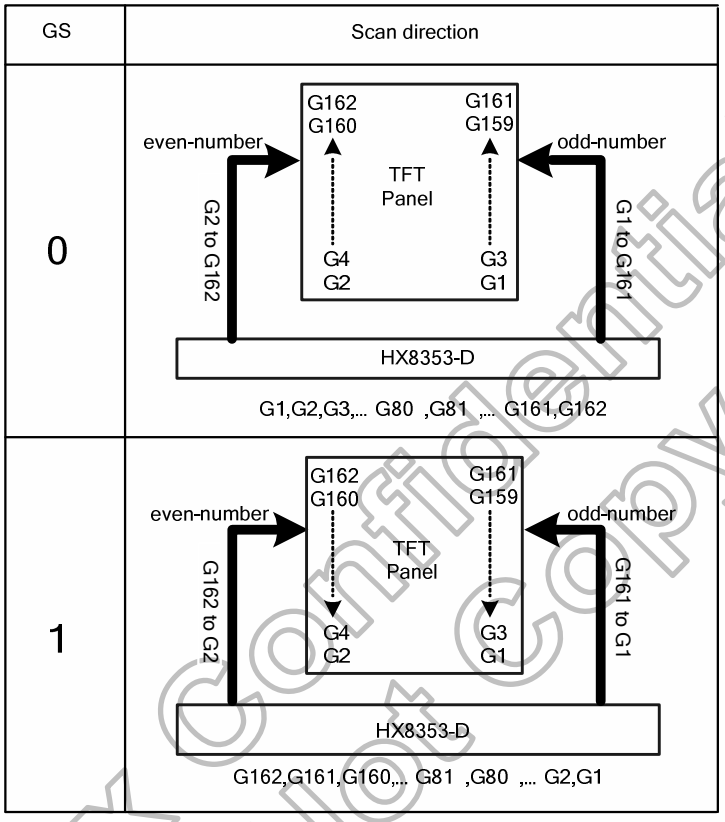


Figure 7.18 Gate Scan Mode

7.5 LCD power generation circuit

7.5.1 Power supply circuit

The power circuit of HX8353-D is used to generate supply voltages for LCD panel driving.

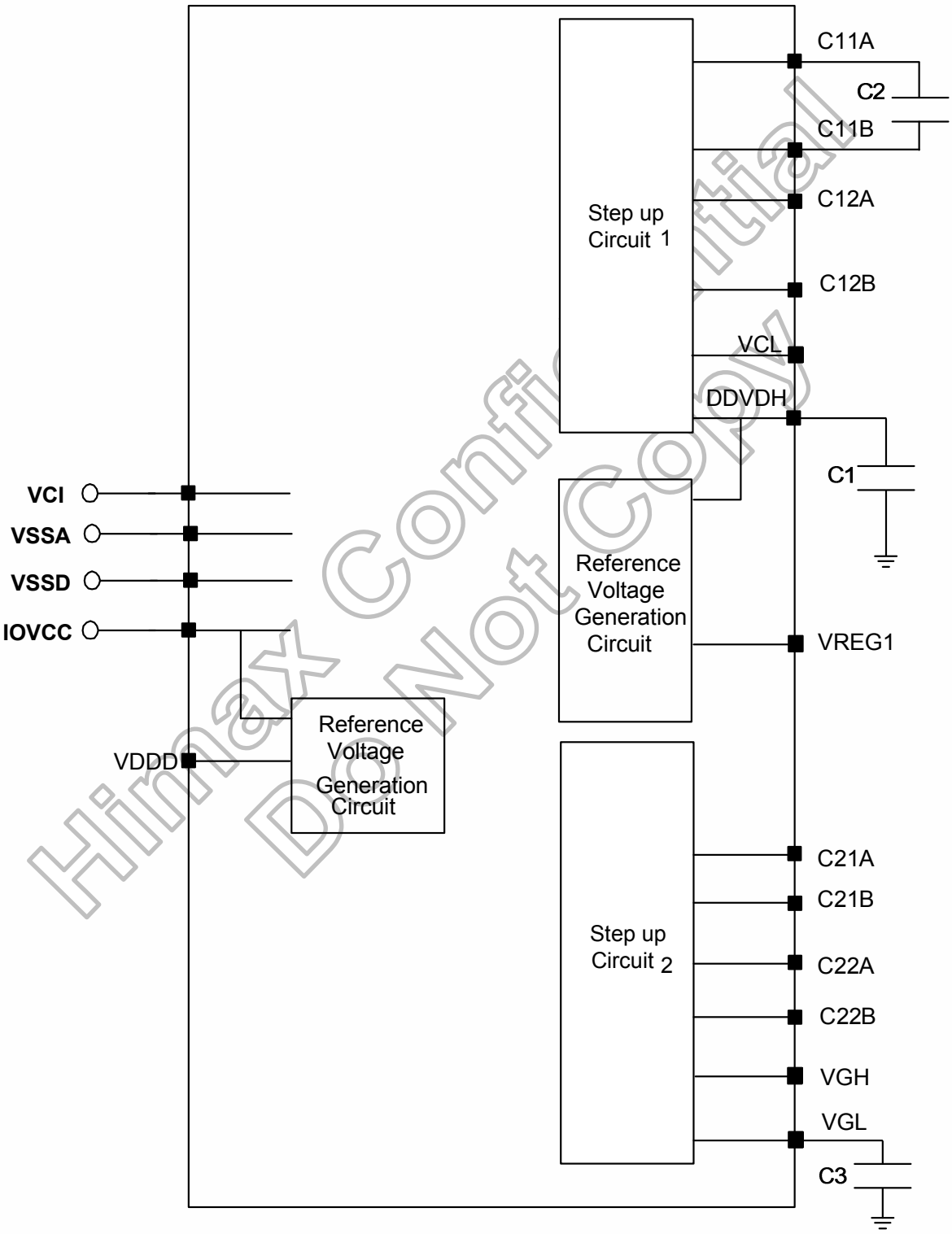


Figure 7.19 Block diagram of HX8353-D power circuit

Specification of Connected Passive Component

Capacitor	Recommended voltage	Capacity
C1 (DDVDH)	6.3V	1 µF (B characteristics)
C2 (C11)	6.3V	1 µF (B characteristics)
C3 (VGL)	16V	1 µF (B characteristics)

Table 7.9 The adoptability of Capacitor

7.5.2 LCD power generation scheme

The boost voltage generated is shown as below.

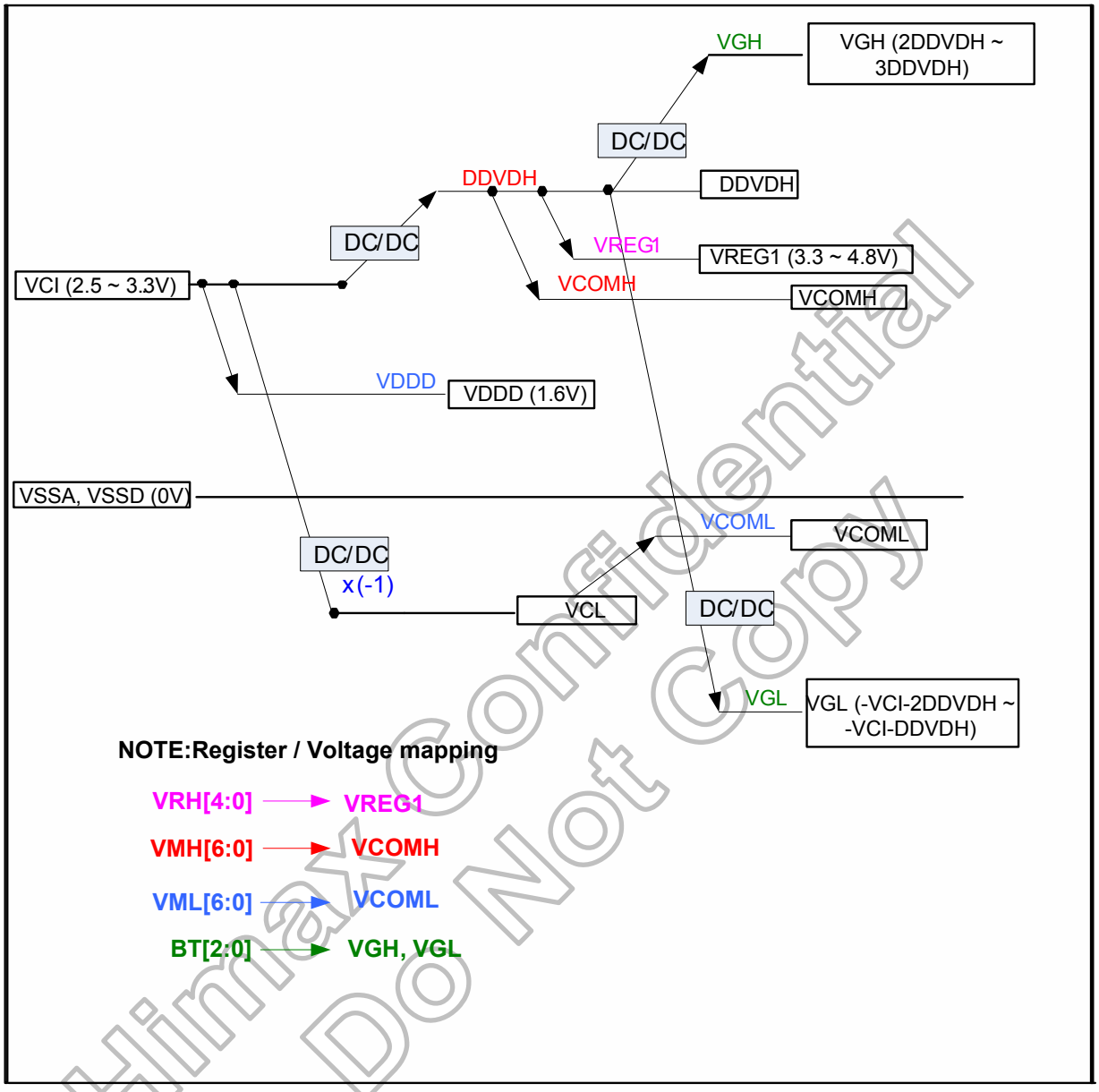


Figure 7.20 LCD power generation scheme

7.6 Power function

7.6.1 Power on/off sequence

Power source IOVCC, VCI can be applied and powered down in any order.
IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

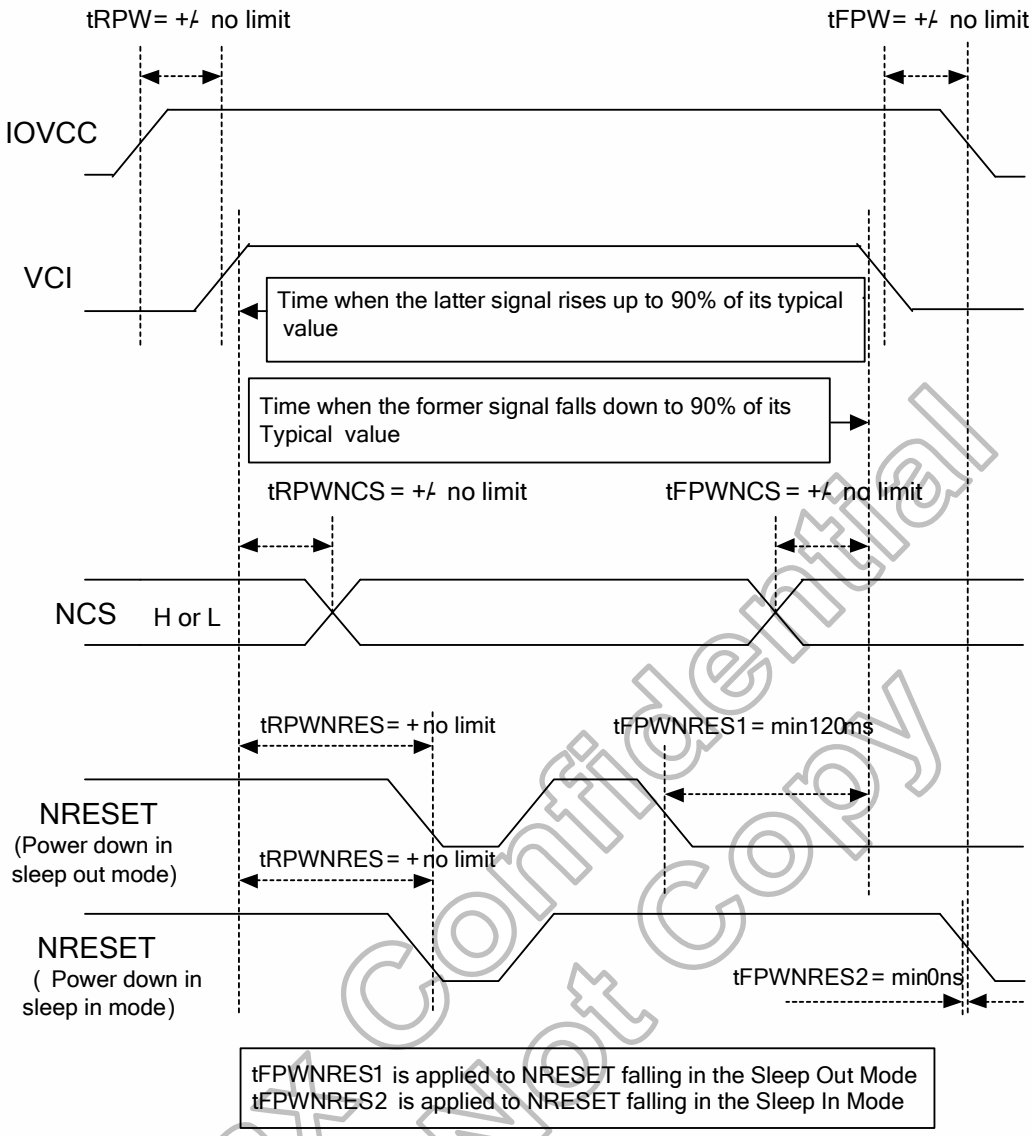
NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.

Note: (1) There will be no damage to the display module if the power sequences are not met.
(2) There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
(3) There will be no abnormal visible effects on the display between end of Power on Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
(4) If NRESET line is not held stable by host during Power on Sequence as defined in Sections 7.5.1.1 and 7.5.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence to ensure correct operation. Otherwise correct function is not guaranteed.

If NRESET line is not held stable by host during Power on Sequence as defined in Sections 7.5.1.1 and 7.5.1.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power on Sequence is complete to ensure correct operation, otherwise correct functionality is not guaranteed. The power on/off sequence is illustrated as below.

7.6.1.1 Case 1 – NRESET line is held high or unstable by host at power on

If NRESET line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both IOVCC, VCI have been applied, otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

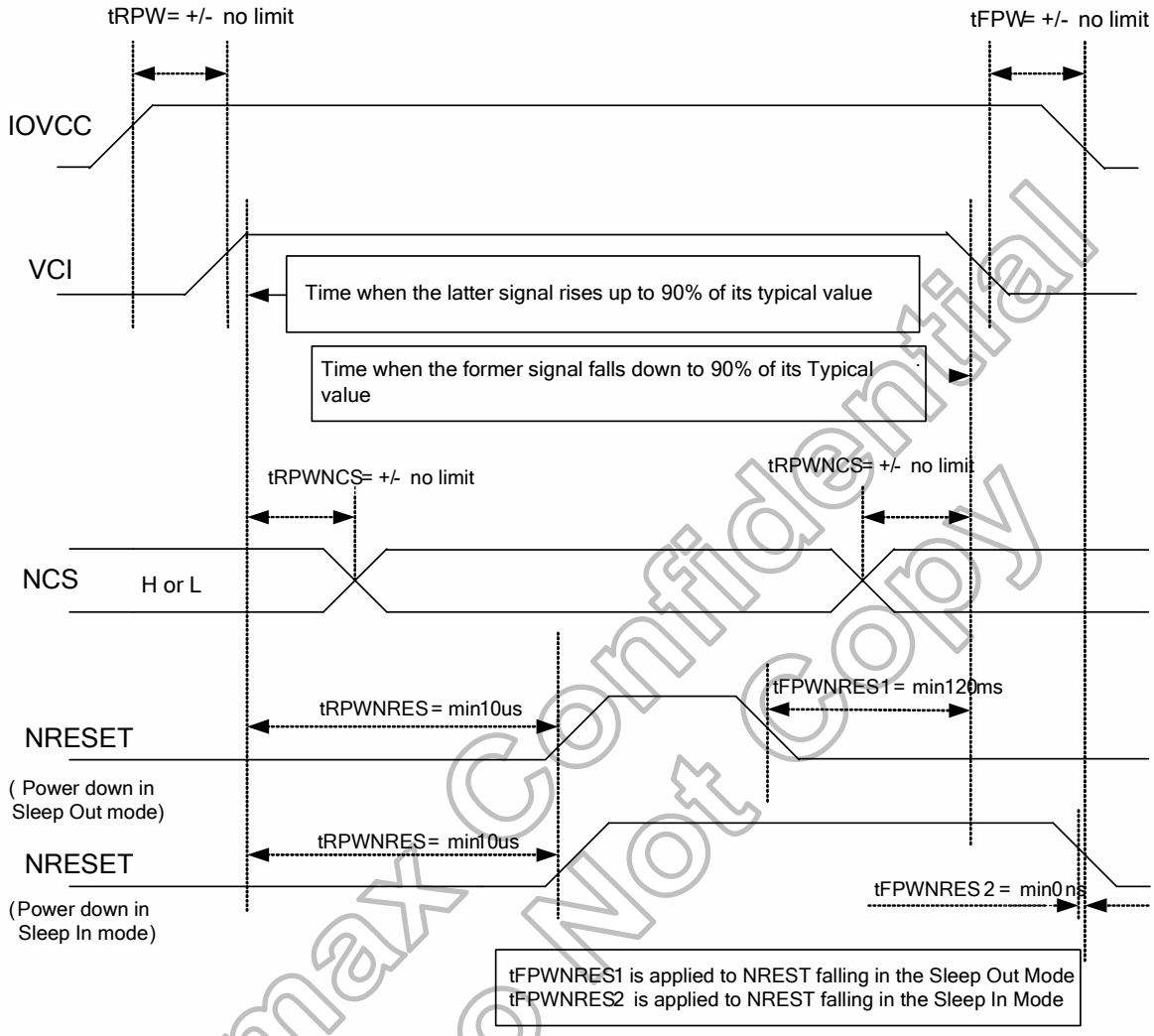


Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 7.21 Case 1 – NRESET line is held high or unstable by host at power on

7.6.1.2 Case 2 – NRESET line is held low by host at power on

If NRESET line is held Low (and stable) by the host during Power On, then the NRESET must be held low for minimum 10µsec after VCI have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Figure 7.22 NRESET Line is Held Low by Host at Power On

7.6.2 Power levels definition

7.6.2.1 General definition for power levels on system interface

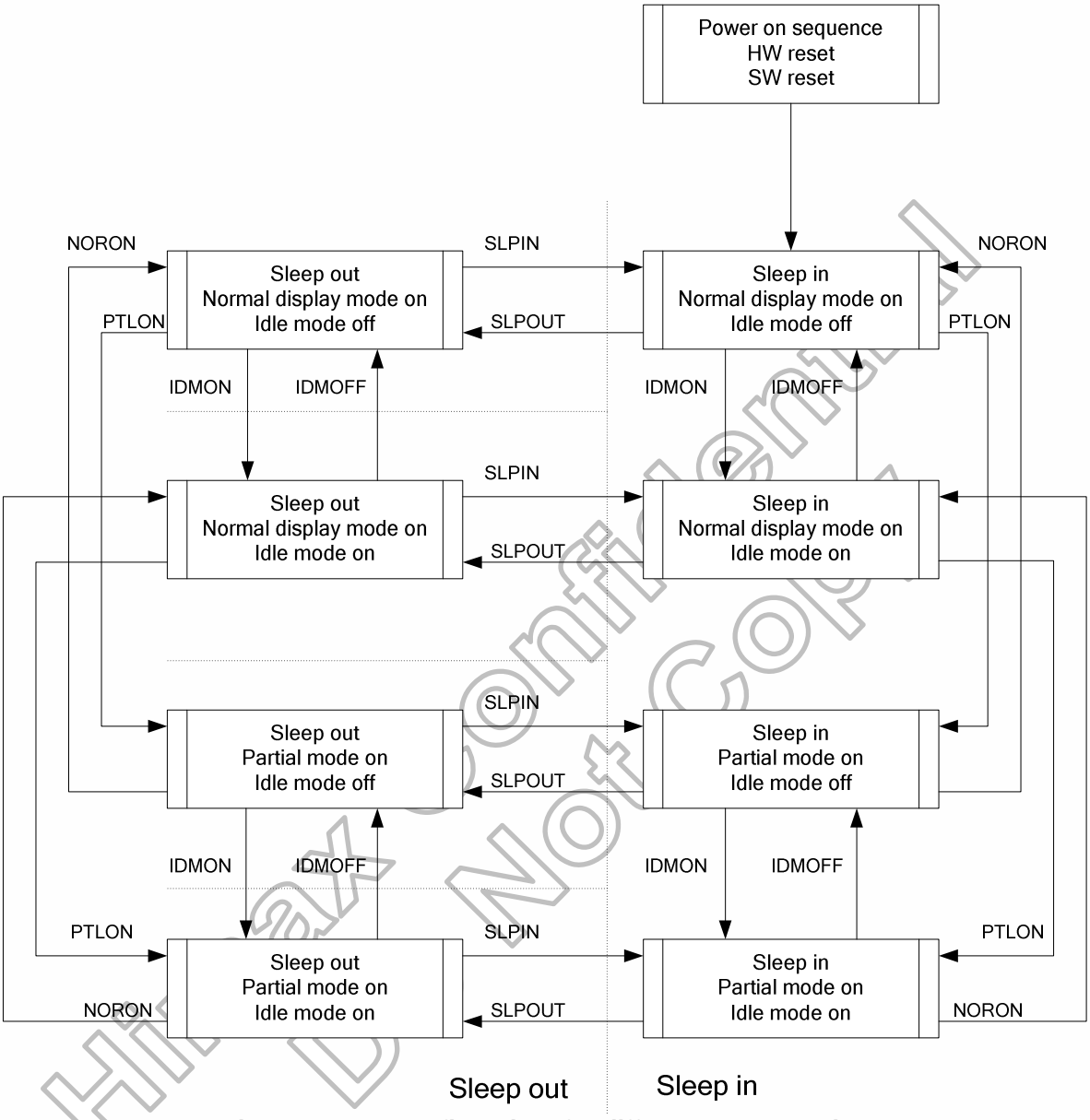


Figure 7.23 Power flow chart for different power modes

7.6.3 Deep standby mode set up flow

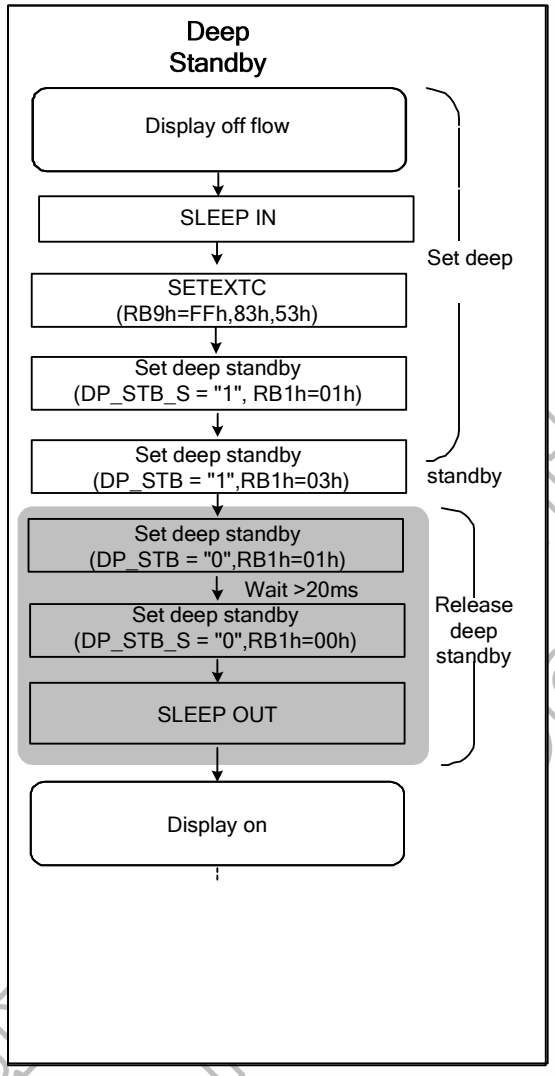


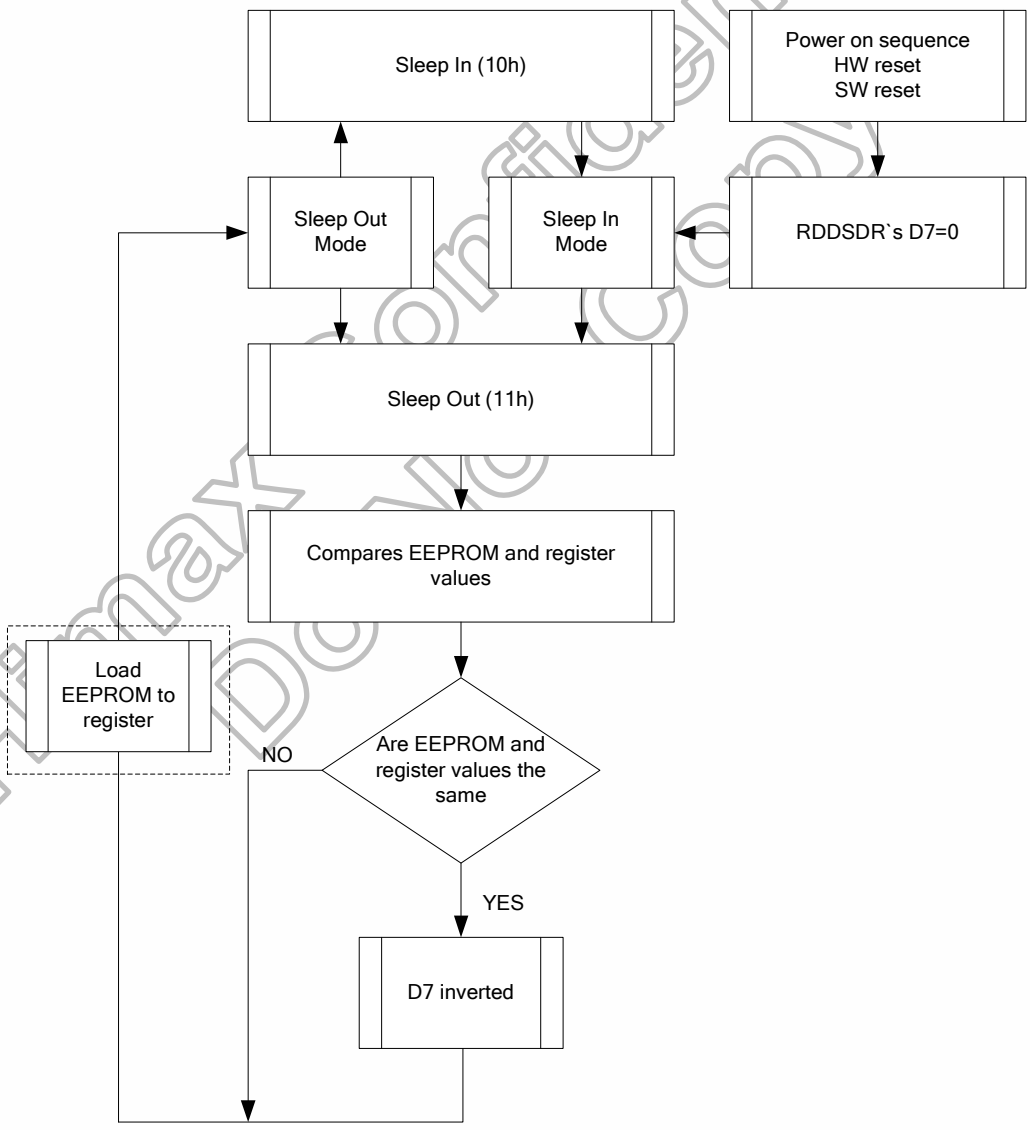
Figure 7.24 Deep standby mode setting flow

7.7 Sleep out – command and self-diagnostic functions of display module

7.7.1 Register loading detection

Sleep Out-command (See section 8.2.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller. If those both values (EEPROM and register values) are the same, there is an inverted (=increased by 1) bit, which is defined in section 8.2.10 “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The bit used for this command is D7). If those both values are not the same, this bit (D7) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



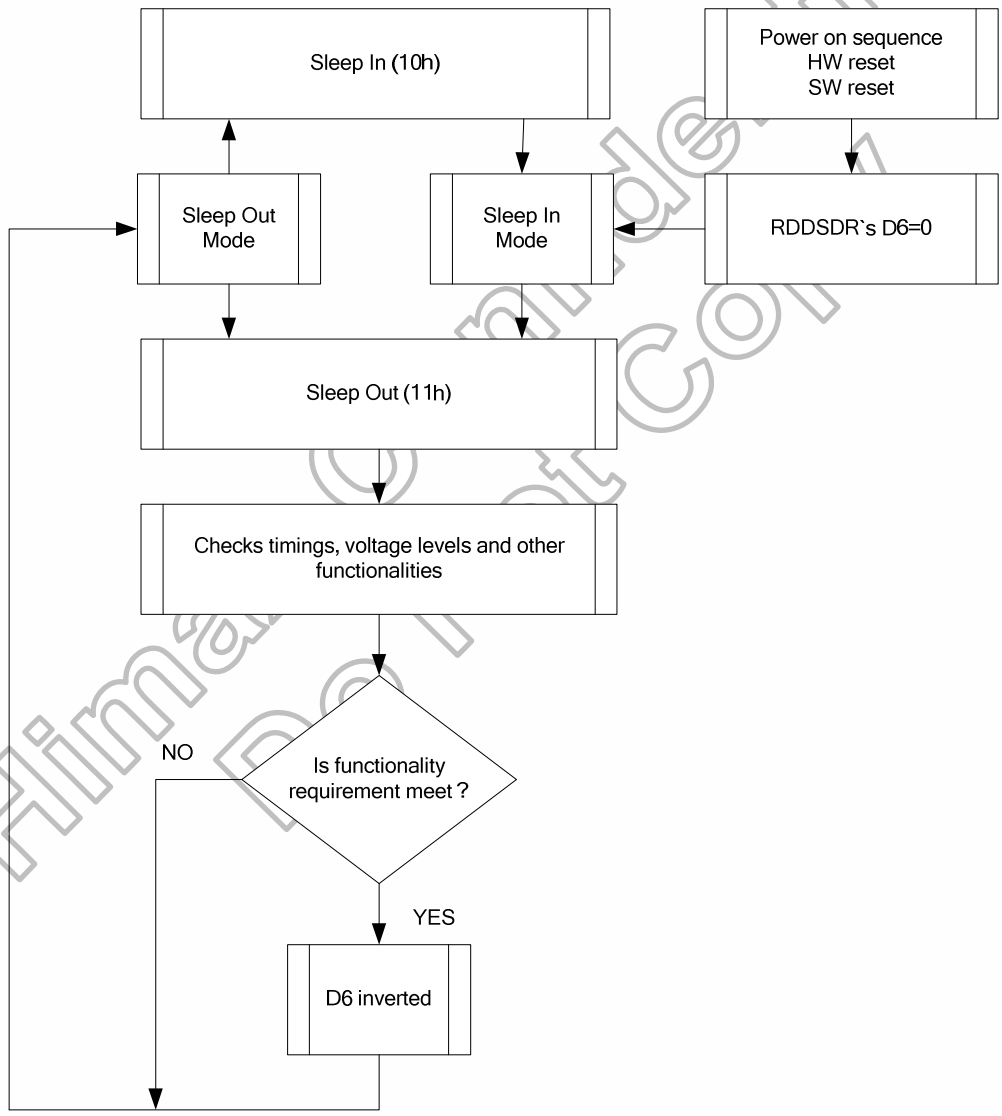
Note: There is not compared and loaded register values, which can be changed by User (User area commands: 00h to AFh and DAh to DDh), by the display module.

Figure 7.25 RDDSDR register loading detection flow

7.7.2 Functionality detection

Sleep Out-command (See section 8.2.12 “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in section 8.2.10 “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 7.26 Functionality detection flow

7.8 Input / output pin state

7.8.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
VTESTOUT	Low	Low	Low

Table 7.10 Characteristics of output pins

7.8.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
NRESET	Input valid	Input valid	Input valid	Input valid	Input valid
NCS	Input valid	Input valid	Input valid	Input valid	Input valid
SPI_SEL	Input valid	Input valid	Input valid	Input valid	Input valid
GC_SEL	Input valid	Input valid	Input valid	Input valid	Input valid
LC_SEL0, LC_SEL1	Input valid	Input valid	Input valid	Input valid	Input valid
DNC_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
NWR_RNW	Input valid	Input valid	Input valid	Input valid	Input valid
NRD_E	Input valid	Input valid	Input valid	Input valid	Input valid
DB17 to DB0	Input valid	Input valid	Input valid	Input valid	Input valid
OSC,P68,BS1,BS2,BS0	Input valid	Input valid	Input valid	Input valid	Input valid
EXTC	Input valid	Input valid	Input valid	Input valid	Input valid
TEST1	Input valid	Input valid	Input valid	Input valid	Input valid
TEST2	Input valid	Input valid	Input valid	Input valid	Input valid
RSO0	Input valid	Input valid	Input valid	Input valid	Input valid
RSO1	Input valid	Input valid	Input valid	Input valid	Input valid
RSO2	Input valid	Input valid	Input valid	Input valid	Input valid

Table 7.11 Characteristics of input pins

8. Command Set

8.1 Command set list

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
00	NOP	0	↑	1	0	0	0	0	0	0	0	0	No operation
01	SWRESET	0	↑	1	0	0	0	0	0	0	0	1	Software reset
04	RDDIDIF	0	↑	1	0	0	0	0	0	1	0	0	Read display identification information
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	ID1[7:0]								ID1 read
		1	1	↑	ID2[7:0]								ID2 read
		1	1	↑	ID3[7:0]								ID3 read
09	RDDST	0	↑	1	0	0	0	0	1	0	0	1	Read display status
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D31	D30	D29	D28	D27	D26	D25	0	
		1	1	↑	0	D22	D21	D20	D19	D18	D17	D16	
		1	1	↑	D15	0	D13	0	0	D10	D9	D8	
		1	1	↑	D7	D6	D5	0	0	0	0	0	
0A	RDDPM	0	↑	1	0	0	0	0	1	0	1	0	Read display power mode
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	D3	D2	0	0	
0B	RDDMADCTL	0	↑	1	0	0	0	0	1	0	1	1	Read display MADCTL
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	D3	D2	0	0	
0C	RDDCOLMOD	0	↑	1	0	0	0	0	1	1	0	0	Read display pixel format
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	0	0	0	0	0	D2	D1	D0	
0D	RDDIM	0	↑	1	0	0	0	0	1	1	0	1	Read display image mode
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	0	D5	0	0	D2	D1	D0	
0E	RDDSM	0	↑	1	0	0	0	0	1	1	1	0	Read display signal mode
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	0	0	0	0	0	0	
0F	RDDSDR	0	↑	1	0	0	0	0	1	1	1	1	Read display self-diagnostic result
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D7	D6	D5	D4	0	0	0	0	
10	SLPIN	0	↑	1	0	0	0	1	0	0	0	0	Sleep in and charge-pump off
11	SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	Sleep out and charge-pump on
12	PTLON	0	↑	1	0	0	0	1	0	0	1	0	Partial mode on
13	NORON	0	↑	1	0	0	0	1	0	0	1	1	Normal display mode on
20	INVOFF	0	↑	1	0	0	1	0	0	0	0	0	Display inversion off
21	INVON	0	↑	1	0	0	1	0	0	0	0	1	Display inversion on

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
26	GAMSET	0	↑	1	0	0	1	0	0	1	1	0	Gamma set
		1	↑	1	GC[7:0]								
28	DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	Display off
29	DISPON	0	↑	1	0	0	1	0	1	0	0	1	Display on
2A	CASET	0	↑	1	0	0	1	0	1	0	1	0	Column setting
		1	↑	1	SC[15:8]								Column address start
		1	↑	1	SC[7:0]								Column address start
		1	↑	1	EC[15:8]								Column address end
		1	↑	1	EC[7:0]								Column address end
2B	PASET	0	↑	1	0	0	1	0	1	0	1	1	Row address set
		1	↑	1	SP[15:8]								Row address start
		1	↑	1	SP[7:0]								Row address start
		1	↑	1	EP[15:8]								Row address end
		1	↑	1	EP[7:0]								Row address end
2C	RAMWR	0	↑	1	0	0	1	0	1	1	0	0	Memory write
		1	↑	1	D[17:0]								Write GRAM data
2D	RGBSET	0	↑	1	0	0	1	0	1	1	0	1	LUT parameter
		1	↑	1	-	-	R005	R004	R003	R002	R001	R000	Red tone
					:	:	:	:	:	:	:	:	
		1	↑	1	-	-	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	Red tone
		1	↑	1	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	R315	R314	R313	R312	R311	R310	Red tone
		1	↑	1	-	-	G005	G004	G003	G002	G001	G000	Green tone
		1	↑	1	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	Green tone
		1	↑	1	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	G635	G634	G633	G632	G631	G630	Green tone
		1	↑	1	-	-	B005	B004	B003	B002	B001	B000	Blue tone
		1	↑	1	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	Blue tone
		1	↑	1	:	:	:	:	:	:	:	:	
		1	↑	1	-	-	B315	B314	B313	B312	B311	B310	Blue tone
2E	RAMRD	0	↑	1	0	0	1	0	1	1	1	0	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	D[15:0]								Read GRAM data
30	PLTAR	0	↑	1	0	0	1	1	0	0	0	0	Partial start end address set
		1	↑	1	SR[15:8]								Start row
		1	↑	1	SR[7:0]								Start row
		1	↑	1	ER[15:8]								End row
		1	↑	1	ER[7:0]								End row
33	VSCRDEF	0	↑	1	0	0	1	1	0	0	1	1	Vertical Scrolling Definition
		1	↑	1	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8	
		1	↑	1	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	
		1	↑	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA9	VSA8	
		1	↑	1	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
		1	↑	1	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8	
		1	↑	1	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	
34	TEOFF	0	↑	1	0	0	1	1	0	1	0	0	Tear effect Off
35	TEON	0	↑	1	0	0	1	1	0	1	0	1	Tear effect mode
		1	↑	1	-	-	-	-	-	-	-	TEMODE	

(Hex)	Operation Code	DNC	NWR	NRD	D7	D6	D5	D4	D3	D2	D1	D0	Function
36	MADCTL	0	↑	1	0	0	1	1	0	1	1	0	Memory access control
		1	↑	1	MY	MX	MV	ML	BGR	SS	0	0	
37	VSCRSADD	0	↑	1	0	0	1	1	0	1	1	1	Vertical scrolling start address
		1	↑	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP9	VSP8	
		1	↑	1	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	
38	IDMOFF	0	↑	1	0	0	1	1	1	0	0	0	Idle mode off
39	IDMON	0	↑	1	0	0	1	1	1	0	0	1	Idle mode on
3A	COLMOD	0	↑	1	0	0	1	1	1	0	1	0	Interface pixel format
		1	↑	1	0	0	0	0	0	D2	D1	D0	
DA	RDID1	0	↑	1	1	1	0	1	1	0	1	0	Read ID1
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	module's manufacturer[7:0]								
DB	RDID2	0	↑	1	1	1	0	1	1	0	1	1	Read ID2
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	1	LCD module/driver version [6:0]							
DC	RDID3	0	↑	1	1	1	0	1	1	1	0	0	Read ID3
		1	1	↑	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	LCD module/driver ID[7:0]								

Table 8.1 System interface command set

Extended command set

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
B0	SETOSC	0	↑	1	-	1	0	1	1	0	0	0	0	Set internal Oscillator
		1	↑	1	-	I_RADJ[1:0] (11)	-	-	N_RADJ[1:0] (10)	-	-			
		1	↑	1	-	-	-	-	-	-	-	-	OSC_EN (0)	
B1	SETPWCTR	0	↑	1	-	1	0	1	1	0	0	0	1	Set power control
		1	↑	1	-	-	-	-	-	-	-	DP_STB (0)	DP_STB_S (0)	
		1	↑	1	-	-	-	-	-	-	BT[2:0](001)			
		1	↑	1	-	-	-	VRH[5:0](01_1011)						
		1	↑	1	-	-	-	-	-	-	AP[2:0](011)			
		1	↑	1	-	FS0[7:0](0000_0100)								
		1	↑	1	-	FS1[7:0](0000_1000)								
		1	↑	1	-	-	-	-	-	-	-	-	-	
		1	↑	1	-	GASEN(1)	VCOMG(0)	-	PON (0)	DK(1)	-	-	STB (1)	
B2	SETDISPLAY	0	↑	1	-	1	0	1	1	0	0	1	0	Set display control
		1	↑	1	-	-	-	-	-	ISC[3:0] (0001)				
		1	↑	1	-	PT[1:0] (10)		PTV[1:0](01)		-	-	PTG (1)	REF (1)	
		1	↑	1	-	-	-	GON (1)	DTE (0)	D[1:0] (00)		-	-	
B4	SETCYC	0	↑	1	-	1	0	1	1	0	1	0	0	Set display cycle
		1	↑	1	-	-	I_NW[2:0](000)			-	N_NW[2:0](001)			
		1	↑	1	-	I_RTN[3:0](0000)				N_RTN[3:0](0100)				
		1	↑	1	-	I_DIV[3:0](1111)				N_DIV[3:0](1111)				
		1	↑	1	-	N_DUM[7:0] (0000_1100)								
		1	↑	1	-	I_DUM[7:0] (0000_1100)								
		1	↑	1	-	GDON[7:0] (0000_1101)								
		1	↑	1	-	GDOF[7:0] (0101_0011)								
		1	↑	1	-	L_BASE[7:0](0101_1001)								
B5	SETBGP	0	↑	1	-	1	0	1	1	0	1	0	1	Set power control
		1	↑	1	-	FBOFF(0)	-	-	DDVDH_TRI (0)	VVDHS_SEL[3:0] (1011)				
		1	↑	1	-	-	-	-	-	VREF[3:0] (1011)				
		1	↑	1	-	-	-	-	-	VR_TRIM[3:0] (1000)				
B6	SETVCOM	0	↑	1	-	1	0	1	1	0	1	1	0	Set VCOM voltage
		1	↑	1	-	VMF[7:0](1001_1110)								
		1	↑	1	-	VMH[7:0](0110_1100)								
		1	↑	1	-	VML[7:0](0101_0100)								
B9	SETEXTC	0	↑	1	-	1	0	1	1	1	0	0	1	Enter extension command
		1	↑	1	-	EXTC1[7:0] (0000_0000)								
		1	↑	1	-	EXTC2[7:0] (0000_0000)								
		1	↑	1	-	EXTC3[7:0] (0000_0000)								
BB	SETOTP	0	↑	1	-	1	0	1	1	1	0	1	1	Set OTP
		1	↑	1	-	OTP_MASK[7:0] (0000_0000)								
		1	↑	1	-	OTP_INDEX[7:0] (0000_0000)								
		1	↑	1	-	OTP_LOAD_DISABLE (0)	DCCLK_DISABLE (0)	OTP_POR (0)	OTP_PWE (0)	OTP_EN (0)	OTPTEST_EN (0)	VPP_SEL(0)	OTP_PROG(0)	
		1	↑	1	-	-	-	-	-	OTP_PTM [1:0](00)		OTP_VRADJ [1:0](00)		
		1	1	↑		OTP_DATA[7:0] (0000_0000)								

(Hex)	Operation Code	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	Function
C0	SETSTBA	0	↑	1	-	1	1	0	0	0	0	0	0	Set Source option
		1	↑	1	-	N_OPON[7:0] (0001_1000)								
		1	↑	1	-	I_OPON[7:0] (0000_1000)								
		1	↑	1	-	STBA[15:8] (0000_1100)								
		1	↑	1	-	STBA[7:0] (1100_0100)								
		1	↑	1	-	GENON[7:0] (0001_0000)								
		1	↑	1	-	-	-	-	-	-	-	-	OTPS 1B (0)	
C3	SETID	0	↑	1	-	1	1	0	0	0	0	1	1	Set ID
		1	↑	1	-	ID1[7:0] (0000_0000)								
		1	↑	1	-	ID2[7:0] (1000_0000)								
		1	↑	1	-	ID3[7:0] (0000_0000)								
C6	SETUADJ	0	↑	1		1	1	0	0	0	1	1	0	Set UADJ to trimming Freq
		1	↑	1		-	I_UADJ[2:0](011)			-	N_UADJ[2:0](001)			
CB	SETCLOCK	0	↑	1		1	1	0	0	1	0	1	1	
		1	↑	1		CADJ[3:0] (0010)				-	-	-	-	
		1	↑	1		-	-	-	-	-	-	-	DCCLK_SYNC(1)	
CC	SETPANEL	0	↑	1	-	1	1	0	0	1	1	0	0	Set Panel characteristics
		1	↑	1	-	-	-	-	-	SS_PANEL (0)	GS_PANEL (0)	REV_PANEL(0)	BGR_PANEL(0)	
D0	GETHID	0	1	↑		1	1	0	1	0	0	0	0	Read Product ID
		1	1	↑		Dummy Read								
		1	1	↑		Product ID[7:0] (0110_0100)								
E0	SETGAMMA	0	↑	1	-	1	1	1	0	0	0	0	0	Set Gamma
		1	↑	1	-	-	MP1[2:0](000)			-	MP0[2:0](000)			
		1	↑	1	-	-	MP3[2:0](110)			-	MP2[2:0](101)			
		1	↑	1	-	-	MP5[2:0](111)			-	MP4[2:0](001)			
		1	↑	1	-	-	-	-	-	CP0[3:0](1010)				
		1	↑	1	-	CP2[3:0](1111)				CP1[3:0](0111)				
		1	↑	1	-	-	-	-	-	CP3[3:0](0001)				
		1	↑	1	-	-	-	-	-	CP4[3:0](1100)				
		1	↑	1	-	-	-	-	-	OP0[3:0](1111)				
		1	↑	1	-	-	-	-	OP1[4:0](0_0000)					
		1	↑	1	-	-	-	-	-	**CGM1[1:0](11)**		**CGM0[1:0](00)**		
		1	↑	1	-	-	MN1[2:0](101)			-	MN0[2:0](000)			
		1	↑	1	-	-	MN3[2:0](010)			-	MN2[2:0](001)			
		1	↑	1	-	-	MN5[2:0](111)			-	MN4[2:0](111)			
		1	↑	1	-	-	-	-	-	CN0[3:0](1100)				
		1	↑	1	-	CN2[3:0](1111)				CN1[3:0](0001)				
		1	↑	1	-	-	-	-	-	CN3[3:0](0111)				
		1	↑	1	-	-	-	-	-	CN4[3:0](1010)				
		1	↑	1	-	-	-	-	-	ON0[3:0](0000)				
		1	↑	1	-	-	-	-	ON1[4:0](0_1111)					
E3	SETEQ	0	↑	1	-	1	1	1	0	0	0	1	1	Set EQ
		1	↑	1	-	EQVCI_M1[7:0] (0001_0000)								
		1	↑	1	-	EQGND_M1[7:0](0000_1000)								
		1	↑	1	-	EQVCI_M0[7:0](0000_1000)								
		1	↑	1	-	EQGND_M0[7:0](0001_0000)								
		1	↑	1	-	PREOE_M0[7:0](0000_0000)								
		1	↑	1	-	PREOE_M1[7:0](0000_0000)								

Table 8.2 System Interface In-House Command Set

8.2 Command description

8.2.1 NOP

<table>
<tr><td>00 H</td><td colspan="13">NOP (No Operation)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR (Memory Write) or RAMRD (Memory Read) command.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">-</td></tr>
</table>

8.2.2 Software reset (01h)

01 H	SWRESET (Software Reset)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	0	0	1	01
Parameter	NO PARAMETER												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately. Note: The GRAM contents are unaffected by this command.												
Restriction	It will be necessary to wait 5m sec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.												

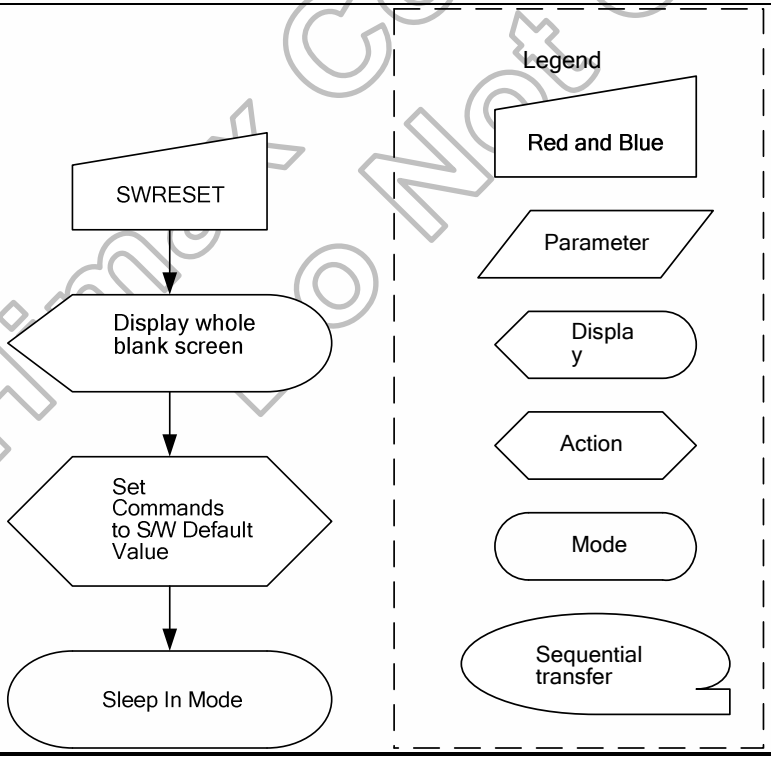
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



8.2.3 Read display identification information (04h)

04 H	RDDIDIF (Read Display Identification Information)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	0	1	0	0	04
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-
3rd parameter	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-
4th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-

Description

This read byte returns 24-bit display identification information.
The 1st Parameter is dummy read. The 2nd ~ 4th Parameter identifies the LCD module's manufacturer.
It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table:

ID Byte Value ID2[7:0]	Version	Changes
80h	-	-
81h	-	-
82h	-	-
83h	-	-
84h	-	-
85h	-	-

The 4th parameter identifies the LCD module/driver.

Restriction

-

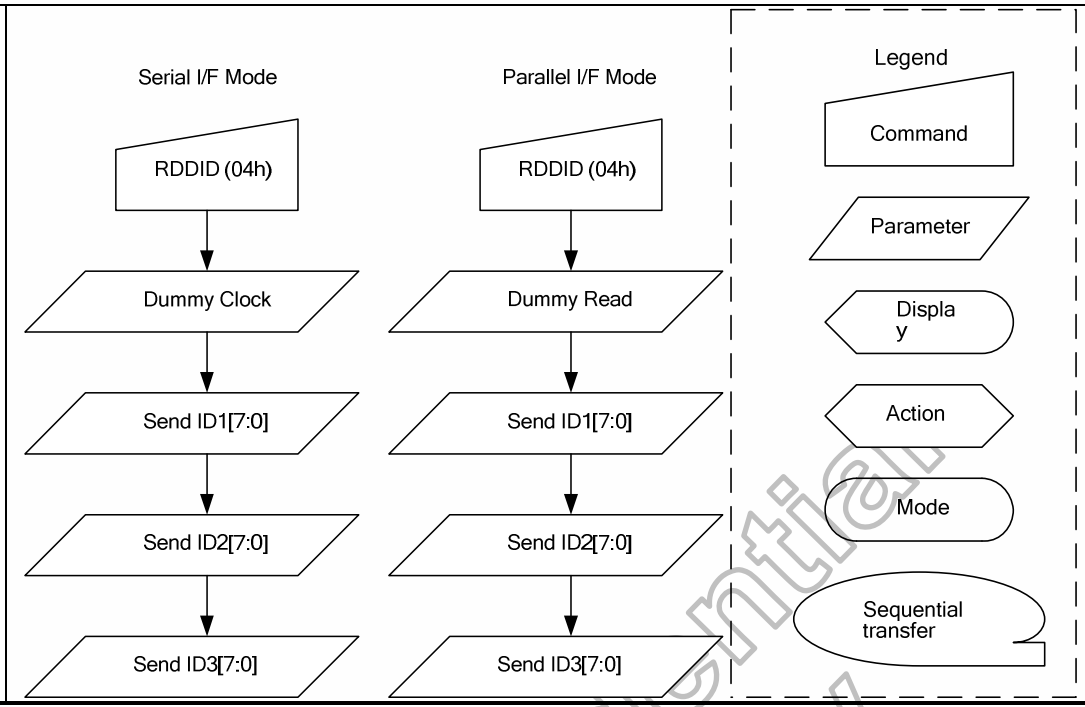
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	See Description
S/W Reset	See Description
H/W Reset	See Description

Flow Chart



8.2.4 Read display status (09h)

09 H	RDDST (Read Display Status)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	0	1	09
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D31	D30	D29	D28	D27	D26	D25	0	-
3rd parameter	1	1	↑	-	0	D22	D21	D20	D19	D18	D17	D16	-
4th parameter	1	1	↑	-	D15	0	D13	0	0	D10	D9	D8	-
5th parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	0	-

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D31	Booster Voltage Status	-
D30	Page Address Order (MY)	-
D29	Column Address Order (MX)	-
D28	Page/Column Order (MV)	-
D27	Line Address Order (ML)	-
D26	RGB/BGR Order	-
D25	Display Data Latch Order	-
D24	Switching between Segment outputs and RAM	Set to '0'
D23	Switching between Common outputs and RAM	Set to '0'
D22	Interface Color Pixel Format Definition	-
D21		-
D20		-
D19	Idle Mode On/Off	-
D18	Partial Mode On/Off	-
D17	Sleep In/Out	-
D16	Display Normal Mode On/Off	-
D15	Vertical Scrolling Status	-
D14	Horizontal Scrolling Status	Set to '0'
D13	Inversion Status	-
D12	All Pixels On	Set to '0'
D11	All Pixels Off	Set to '0'
D10	Display On/Off	-
D9	Tearing Effect Line On/Off	-
D8	Gamma Curve Selection	-
D7		-
D6		-
D5	Tearing Effect Output Line Mode	-
D4	Horizontal Sync. (HS, RGB I/F)	Set to '0'
D3	Vertical Sync. (VS,RGB I/F)	Set to '0'
D2	Pixel Clock (DOTCLK,RGB I/F))	Set to '0'
D1	Data Enable (DE,RGB I/F)	Set to '0'
D0	Parity Error	Set to '0'

Bit Values are explained overleaf.

Bit D31 – Booster Voltage Status
'0' = Booster Off or has a fault.
'1' = Booster On and working OK.

Bit D30 – Page Address Order
'0' = Top to Bottom (When MADCTL B7(MY) = '0').
'1' = Bottom to Top (When MADCTL B7(MY) ='1').

Bit D29 – Column Address Order
'0' = Left to Right (When MADCTL B6(MX) = '0').
'1' = Right to Left (When MADCTL B6(MX) = '1').

Bit D28 –Page / Column Order
'0' = Normal Mode (When MADCTL B5(MV) = '0').

'1' = Reverse Mode (When MADCTL B5(MV) = '1').

Bit D27 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').

Bit D26 – RGB/BGR Order
'0' = RGB (When MADCTL B3 = '0').
'1' = BGR (When MADCTL B3 = '1').

Bit D25 – Display Data Latch Order
'0' = LCD Refresh Left to Right (When MADCTL B2 = '0').
'1' = LCD Refresh Right to Left (When MADCTL B2 = '1').

Note : For bits D27, D26 and D25 also refer to 8.3.29 Memory Access Control (R36h)

Bit D24 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.

Bit D23 – Switching Between Common Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.

Bits D22, D21, D20 –Interface Color Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 bit/pixel	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

Bit D19 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.

Bit D18 – Partial Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.

Bit D17 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.

Bit D16 – Display Normal Mode On/Off
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.

Bit D15 – Vertical Scrolling On/Off
'0' = Vertical Scrolling is Off.
'1' = Vertical Scrolling is On.

Bit D14 – Horizontal Scrolling Status
This bit is not applicable for this project, so it is set to '0'.

Bit D13 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.

Bit D12 – All Pixels On
This bit is not applicable for this project, so it is set to '0'.

Bit D11 – All Pixels Off
This bit is not applicable for this project, so it is set to '0'.

Bit D10 – Display On/Off
'0' = Display is Off.
'1' = Display is On.

Bit D9 – Tearing Effect Line On/Off
'0' =Tearing Effect Line Off.
'1' = Tearing Effect On.

Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Bit D5 – Tearing Effect Line Output Mode.
'0' = Mode 1, V-Blanking only.
'1' = Mode 2, both H-Blanking and V-Blanking.
Bit D4 – Horizontal Sync. (HS) RGB I/F On/Off, Note
This bit is not applicable for this project, so it is set to '0'.
Bit D3 – Vertical Sync. (VS) RGB I/F On/Off, Note
This bit is not applicable for this project, so it is set to '0'.
Bit D2 – Pixel Clock (DOTCLK) RGB I/F On/Off, Note
This bit is not applicable for this project, so it is set to '0'.
Bit D1 – Data Enable (DE) RGB I/F On/Off, Note
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Parity Error
This bit is not applicable for this project, so it is set to '0'.

Restriction

-

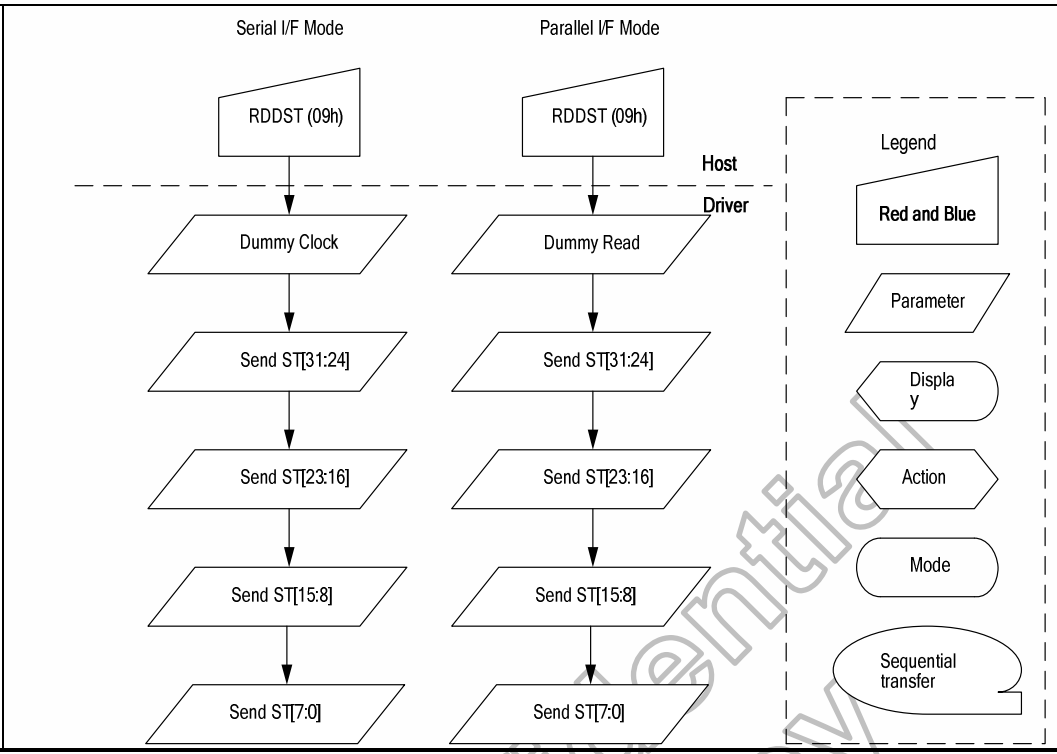
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	See Description
S/W Reset	See Description
H/W Reset	See Description

Flow Chart



8.2.5 Read display power mode (0Ah)

0A H	RDDPM (Read Display Power Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	0	0A
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Booster Voltage Status	-
D6	Idle Mode On/Off	-
D5	Partial Mode On/Off	-
D4	Sleep In/Out	-
D3	Display Normal Mode On/Off	-
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D7 – Booster Voltage Status
'0' = Booster Off or has a fault.
'1' = Booster On and working OK (Meets display supplier's optical requirements).
Bit D6 – Idle Mode On/Off
'0' = Idle Mode Off.
'1' = Idle Mode On.
Bit D5 – Partial Display Mode On/Off
'0' = Partial Mode Off.
'1' = Partial Mode On.
Bit D4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D3 – Normal Display Mode On/Off
'0' = Display Normal Mode Off.
'1' = Display Normal Mode On.
Bit D2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D1 – Not Defined
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Not Defined
This bit is not applicable for this project, so it is set to '0'.

Restrictions

-

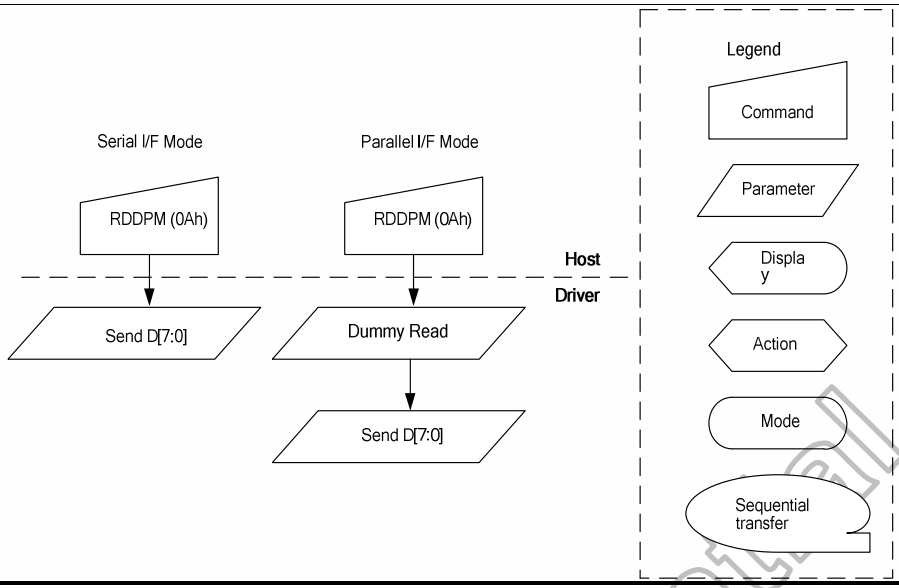
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



8.2.6 Read display MADCTL (0Bh)

0B H	RDDMADCTL (Read Display MADCTL)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	0	1	1	0B
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Page Address Order	-
D6	Column Address Order	-
D5	Page/Column Order	-
D4	Line Address Order	-
D3	RGB/BGR Order	-
D2	Display Data Latch Order	-
D1	Switching between Segment outputs and RAM	Set to '0'
D0	Switching between Common outputs and RAM	Set to '0'

Bit D7 – Page Address Order
'0' = Top to Bottom (When MADCTL B7(MY) = '0').
'1' = Bottom to Top (When MADCTL B7(MY) ='1').
Bit D6 – Column Address Order
'0' = Left to Right (When MADCTL B6(MX) = '0').
'1' = Right to Left (When MADCTL B6(MX) = '1').
Bit D5 –Page / Column Order
'0' = Normal Mode (When MADCTL B5(MV) = '0').
'1' = Reverse Mode (When MADCTL B5(MV) = '1').
Bit D4 – Line Address Order
'0' = LCD Refresh Top to Bottom (When MADCTL B4(ML) = '0').
'1' = LCD Refresh Bottom to Top (When MADCTL B4(ML) = '1').
Bit D3 – RGB/BGR Order
'0' = RGB (When MADCTL B3 = '0').
'1' = BGR (When MADCTL B3 = '1').
Note: For bits D4, D3 and D2 also refer to 8.2.29 Memory Access Control (R36h)
Bit D2 – Display Data Latch Order
Display Data Latch Data Order
'0' = LCD Refresh Left to Right (When MADCTL B2='0').
'1' = LCD Refresh Right to Left (When MADCTL B2='1').
Bit D1 – Switching Between Segment Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.
Bit D0 – Switching Between Common Outputs and RAM
This bit is not applicable for this project, so it is set to '0'.

Restrictions

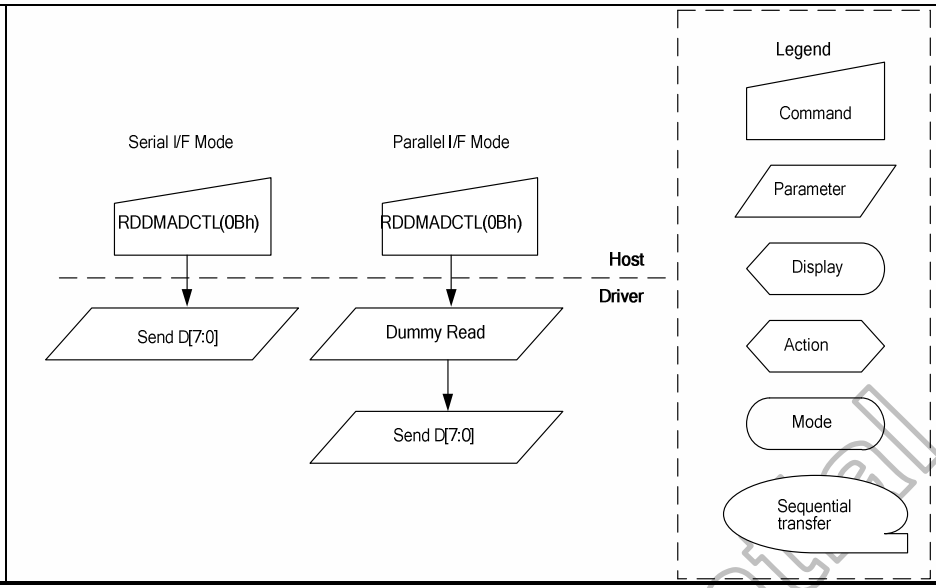
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

Flow Chart	

8.2.7 Read display pixel format (0Ch)

0C H	RDDCOLMOD (Read Display COLMOD)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	0	0C
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	RGB Interface Color Format	Set to '0'
D6		Set to '0'
D5		Set to '0'
D4		Set to '0'
D3	System Interface Color Format	Set to '0'
D2		-
D1		-
D0		-

Bit D7 – RGB Interface Color Format Selection
This bit is not applicable for this project, so it is set to '0'.
Bits D6, D5, D4 – RGB Interface Color Pixel Format Definition
These bits are not applicable for this project, so they are set to '0's.
Bit D3 – System Interface Color Format Selection
This bit is not applicable for this project, so it is set to '0'.
Bit D2, D1, D0 – Control Interface Color Pixel Format Definition.
See section"8.2.33 Interface Pixel Format (R3Ah)".

System Interface Color Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
Not Defined	1	1	1

Restrictions

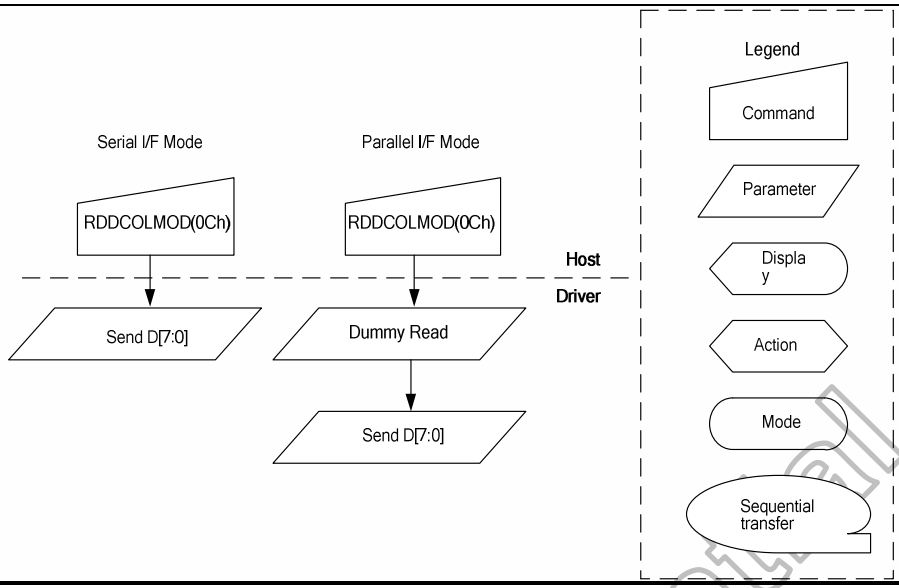
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	18-bit/pixel
S/W Reset	No Change
H/W Reset	18-bit/pixel

Flow Chart	

8.2.8 Read display image mode (0Dh)

0D H	RDDIM (Read Display Image Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	0	1	0D
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	0	D5	0	0	D2	D1	D0	xx

Description

This command indicates the current status of the display as described in the table below:
Bit D7 – Vertical Scrolling On/Off
'0' = Vertical Scrolling is Off.
'1' = Vertical Scrolling is On.
Bit D6 – Horizontal Scrolling Status
This bit is not applicable for this project, so it is set to '0'
Bit D5 – Inversion On/Off
'0' = Inversion is Off.
'1' = Inversion is On.
This bit is not applicable for this project, so it is set to '0'
Bit D4 – All Pixels On
This bit is not applicable for this project, so it is set to '0'
Bit D3 – All Pixels Off
This bit is not applicable for this project, so it is set to '0'
Bits D2, D1, D0 – Gamma Curve Selection

Gamma Curve Selected	D2	D1	D0	Gamma Set (R26h) Parameter
Gamma Curve 1	0	0	0	GC0
Gamma Curve 2	0	0	1	GC1
Gamma Curve 3	0	1	0	GC2
Gamma Curve 4	0	1	1	GC3
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Restrictions

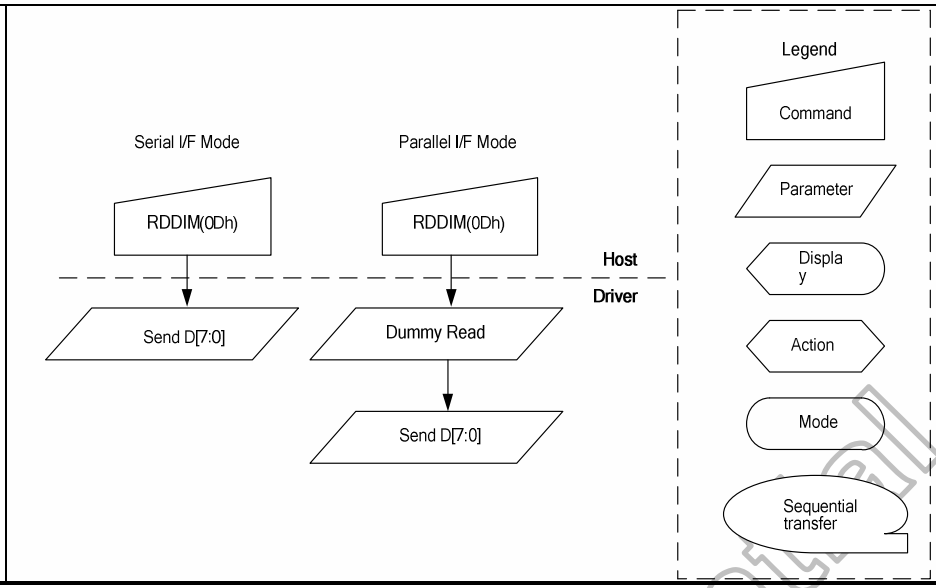
-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

8.2.9 Read display signal mode (0Eh)

0E H	RDDSM (Read Display Signal Mode)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	0	0E
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	D3	D2	0	0	xx
Description	This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 7.3 for mode definitions. '0' = Mode 1. '1' = Mode 2. Bit D5 – Horizontal Sync. (VSYNC, RGB I/F) On/Off This bit is not applicable for this project, so it is set to '0' Bit D4 – Vertical Sync. (HSYNC, RGB I/F) On/Off This bit is not applicable for this project, so it is set to '0' Bit D3 – Pixel Clock (DCLK, RGB I/F) On/Off This bit is not applicable for this project, so it is set to '0' Bit D2 – Data Enable (ENABLE, RGB I/F)) On/Off This bit is not applicable for this project, so it is set to '0' D1 are D0 - are for future use and are set to '0'.												
Restrictions	-												

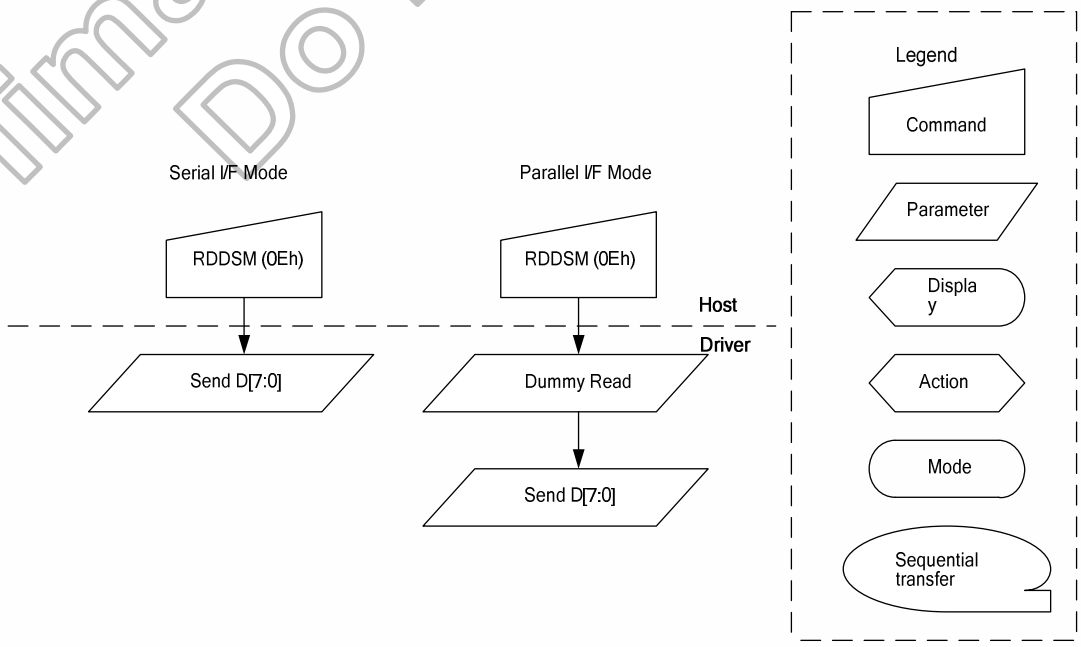
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.10 Read display self-diagnostic result (0Fh)

0F H	RDDSDR (Read Display Self-Diagnostic Result)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	0	1	1	1	1	0F
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	D7	D6	D5	D4	0	0	0	0	-
Description	This command indicates the status of the display self-diagnostic results after Sleep Out -command as described in the table below: Bit D7 – Register Loading Detection See section 7.6.1. Bit D6 – Functionality Detection See section 7.6.2. Bit D5 – Chip Attachment Detection Set bit D5 to '0', if this function is not implemented. Bit D4 – Display Glass Break Detection Set bit D4 to '0', if this function is not implemented. Bits D3, D2, D1 and D0 are for future use and are set to '0'.												
Restrictions	-												

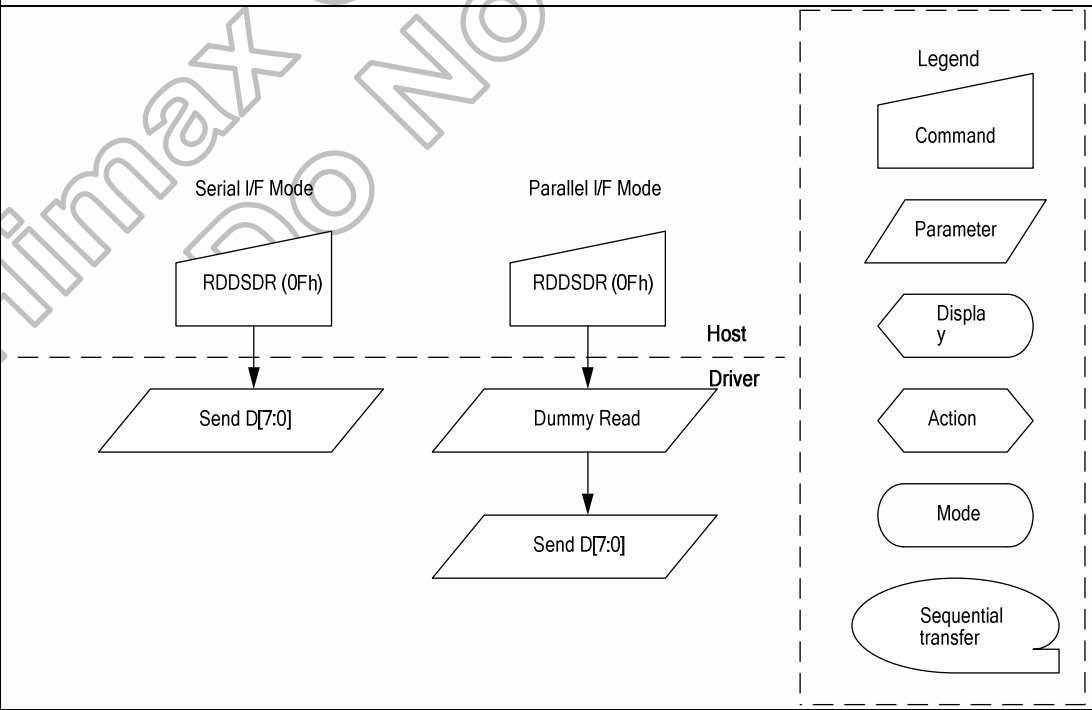
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

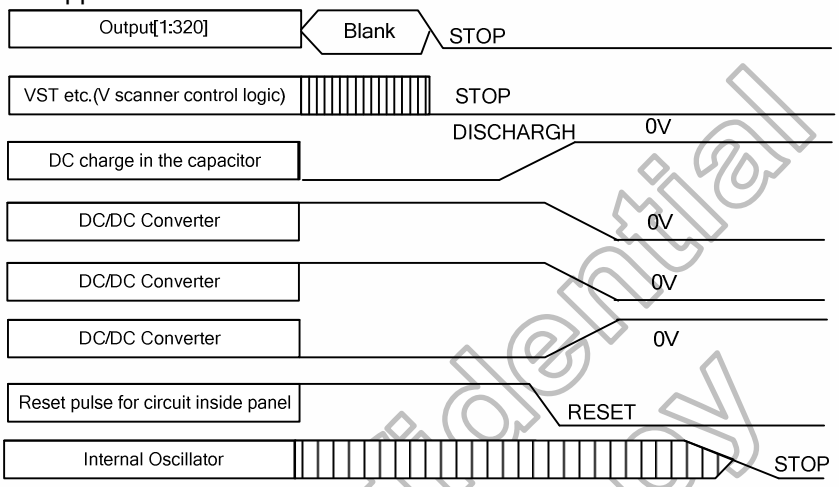
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



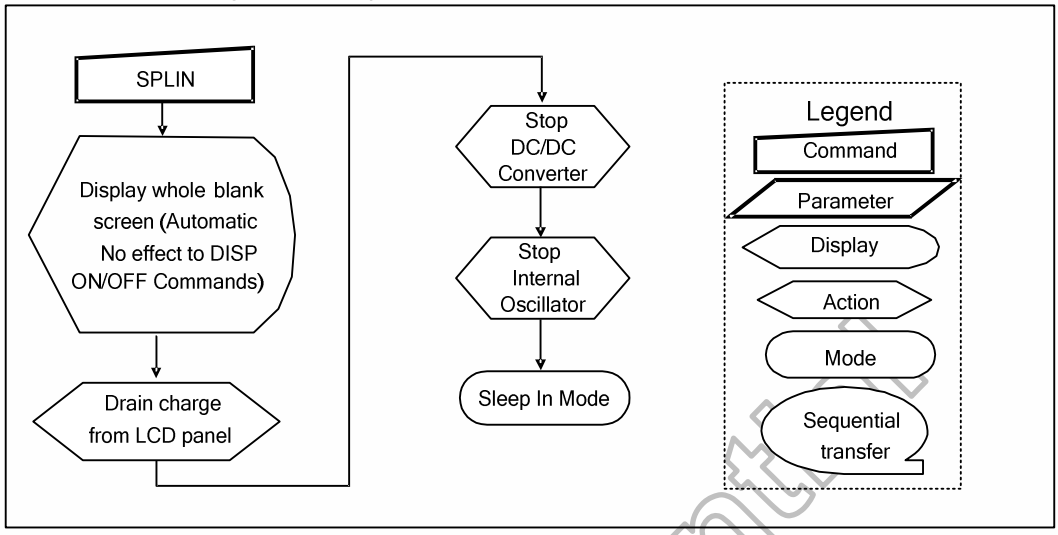
8.2.11 Sleep in (10h)

<table>
<tr><td>10 H</td><td colspan="13">SLPIN (Sleep In)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.
 

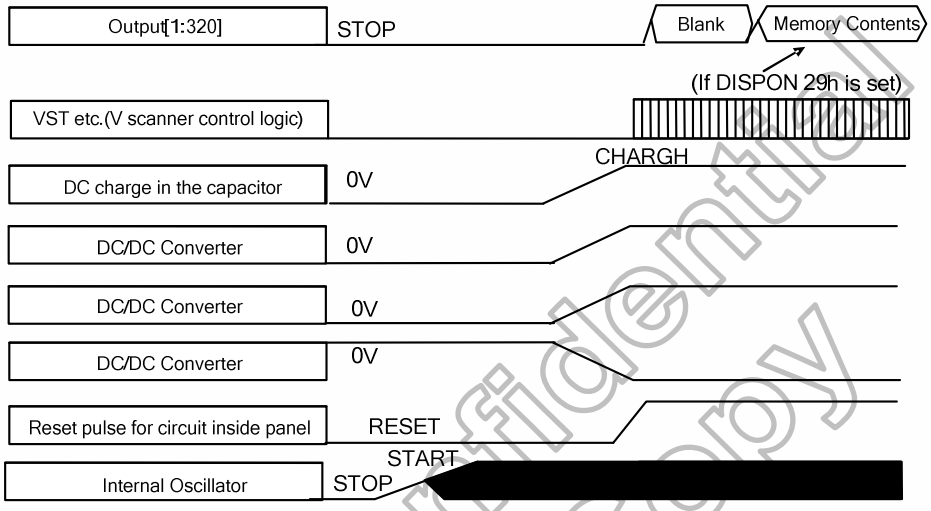
MCU interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr>
<tr><td>S/W Reset</td><td>Sleep In Mode</td></tr>
<tr><td>H/W Reset</td><td>Sleep In Mode</td></tr>
</table></td></tr>
</table>

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.

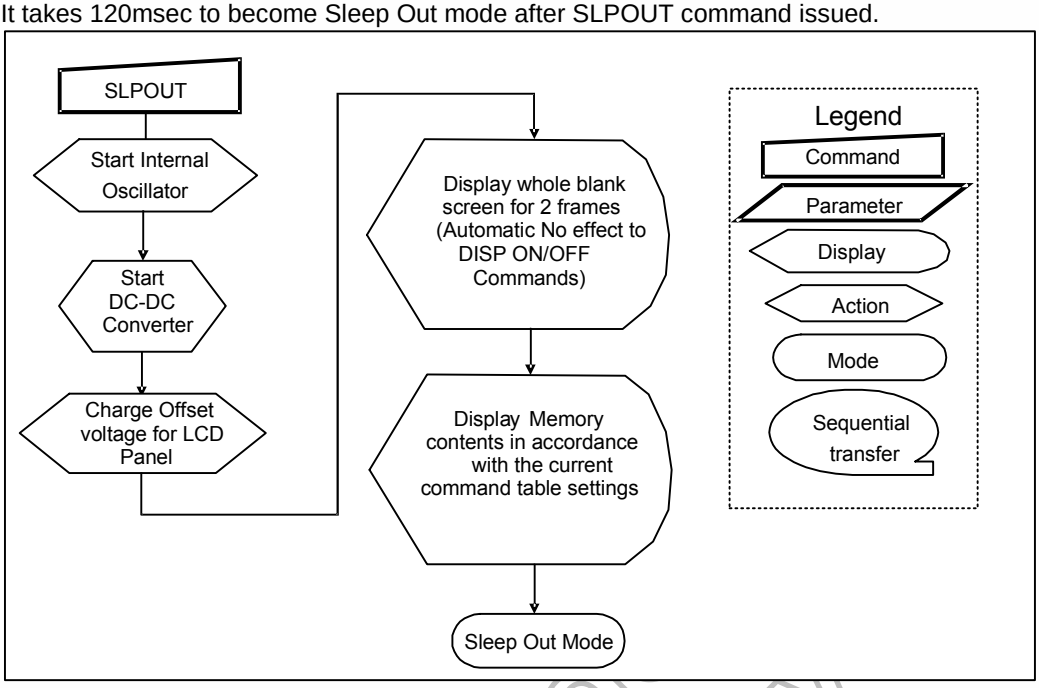


8.2.12 Sleep out (11h)

11 H	SLPOUT (Sleep Out)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	0	1	11
Parameter	NO PARAMETER												
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  												
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display suppliers' factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image. If factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.												
Register Availability	Status	Availability											
	Normal Mode On, Idle Mode Off, Sleep Out	Yes											
	Normal Mode On, Idle Mode On, Sleep Out	Yes											
	Partial Mode On, Idle Mode Off, Sleep Out	Yes											
	Partial Mode On, Idle Mode On, Sleep Out	Yes											
	Sleep In or Booster Off	Yes											
Default	Status	Default Value											
	Power On Sequence	Sleep In Mode											
	S/W Reset	Sleep In Mode											
	H/W Reset	Sleep In Mode											

Flow Chart

It takes 120msec to become Sleep Out mode after SLPOUT command issued.



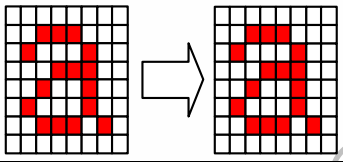
8.2.13 Partial mode on (12h)

12 H	PTLON (Partial Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	0	1	0	0	1	0	12
Parameter	NO PARAMETER												
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. See also section 6.3.8												
Restrictions	This command has no effect when Partial mode is active.												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	Status / Default Value Power On Sequence: Normal Display Mode On S/W Reset: Normal Display Mode On H/W Reset: Normal Display Mode On												
Flow Chart	See Partial Area (30h)												

8.2.14 Normal display mode on (13h)

<table>
<tr><td>13 H</td><td colspan="13">NORON (Normal Display Mode On)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D15-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="13">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode. Normal display mode on means Partial mode off, Scroll mode Off.
See also section 6.2.1.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.</td></tr>
</table>

8.2.15 Display inversion off (20h)

20 H	INVOFF (Display Inversion Off)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20
Parameter	NO PARAMETER												
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 												
Restriction	-												

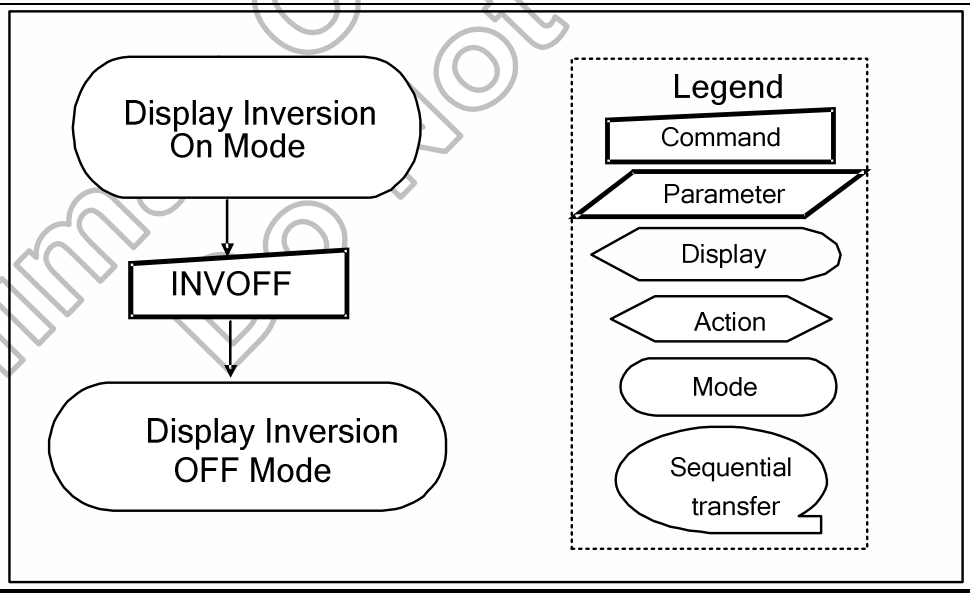
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

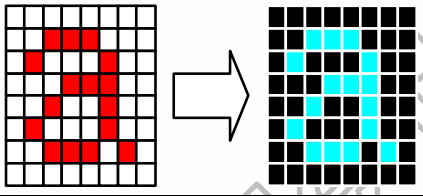
Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



8.2.16 Display inversion on (21h)

21 H	INVON (Display Inversion On)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21
Parameter	NO PARAMETER												
Description	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example) memory display 												
Restriction													

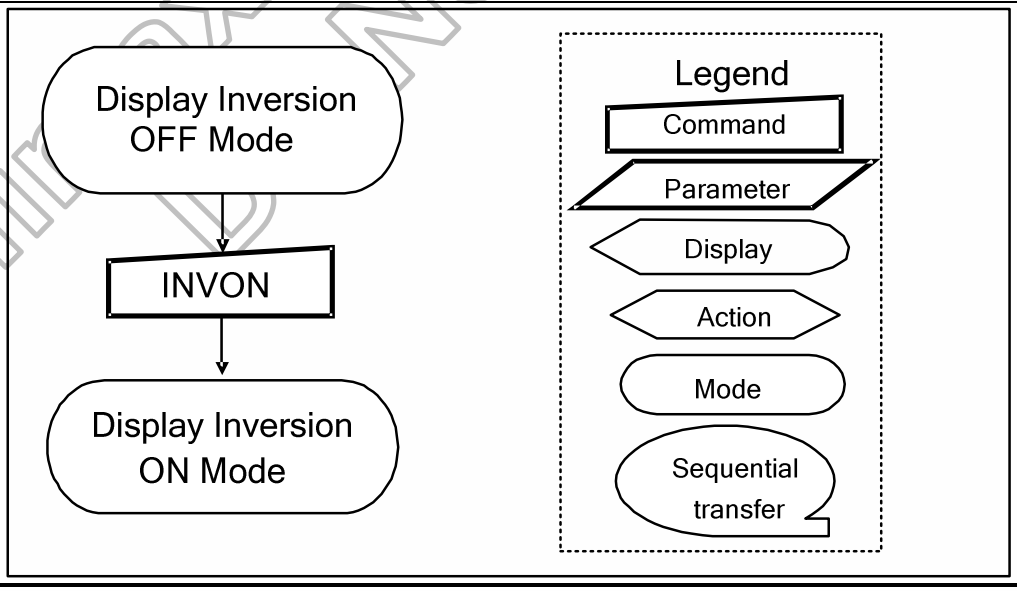
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



8.2.17 Gamma set (26h)

26 H	GAMSET (Gamma Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	0	1	1	0	26
Parameter	1	↑	1	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	-

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the table:

GC[7..0]	Parameter	Curve Selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

Note: All other values are undefined.

Restriction

Values of GC[7..0] not shown in table above are invalid and will not change the Current selected Gamma curve until valid value is received.

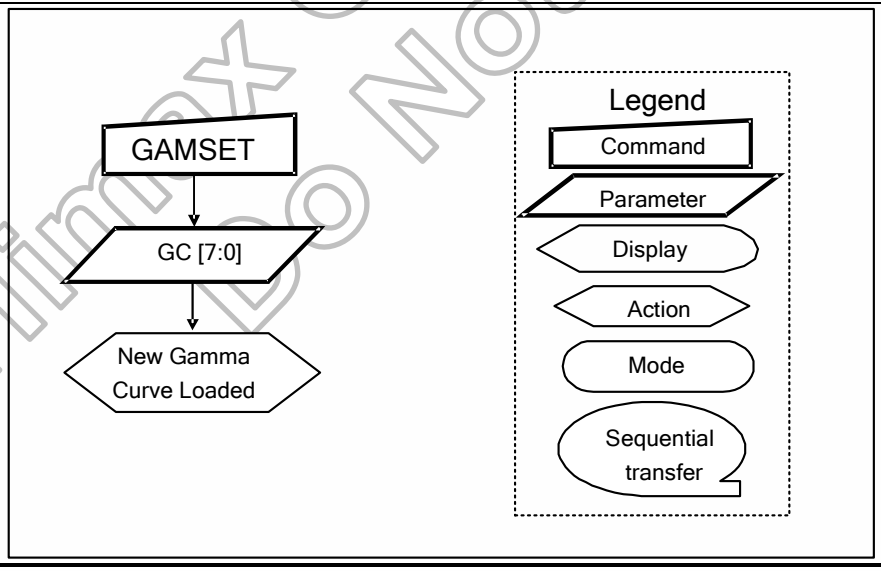
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

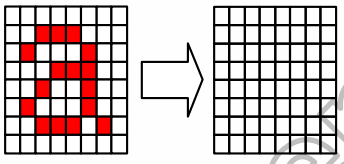
Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



8.2.18 Display off (28h)

28 H	DISPOFF (Display Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	0	28
Parameter	NO PARAMETER												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) memory display 												
Restriction	This command has no effect when module is already in display off mode.												

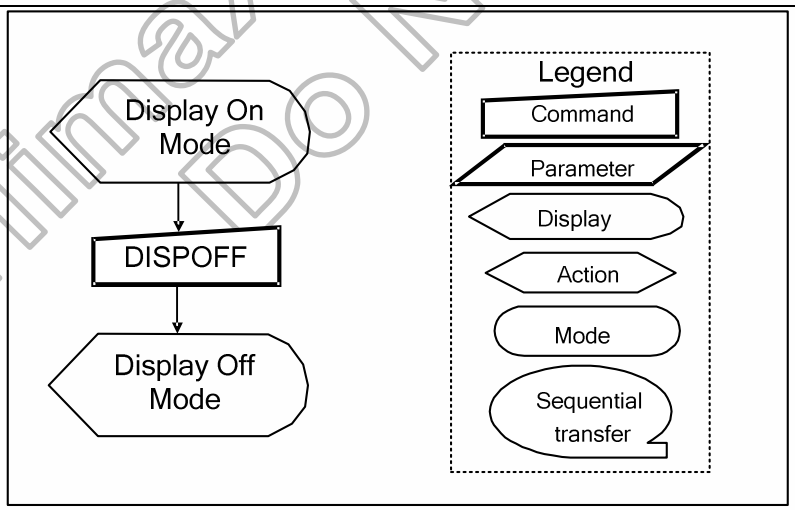
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

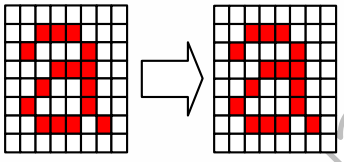
Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



8.2.19 Display on (29h)

29 H	DISPON (Display On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	0	1	29
Parameter	NO PARAMETER												
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 												
Restriction	This command has no effect when module is already in display on mode.												

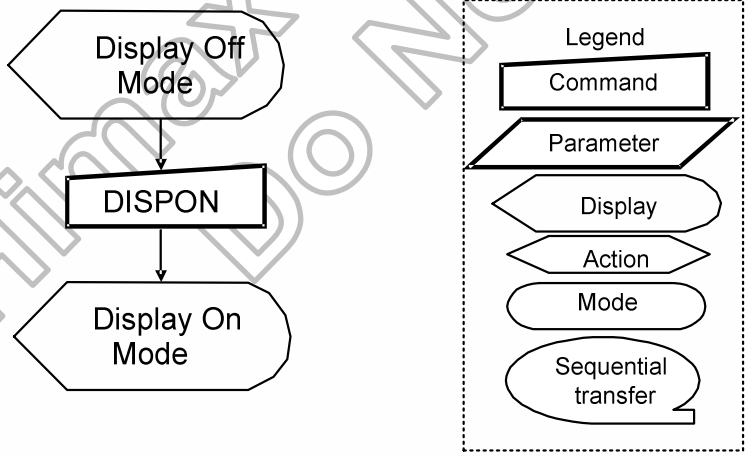
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



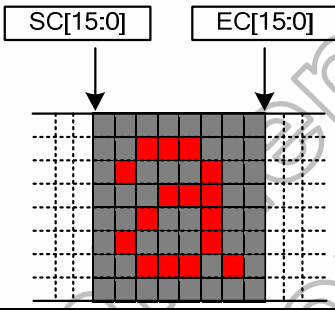
8.2.20 Column address set (2Ah)

2A H	CASET (Column Address Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	0	2A
1st parameter	1	↑	1	-	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note
2nd parameter	1	↑	1	-	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd parameter	1	↑	1	-	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note
4th parameter	1	↑	1	-	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SC[15:0] and EC[15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.

(Example)



Restriction

SC[15:0] always must be equal to or less than EC[15:0]
Note: When SC[15:0] or EC[15:0] is greater than maximum address like below, data out of range will be ignored
0000h<=SC[15:0]<=EC[15:0] <=0083h ,when MADCTL's B5=0
0000h<=SC[15:0]<=EC[15:0] <=00A1h ,when MADCTL's B5=1

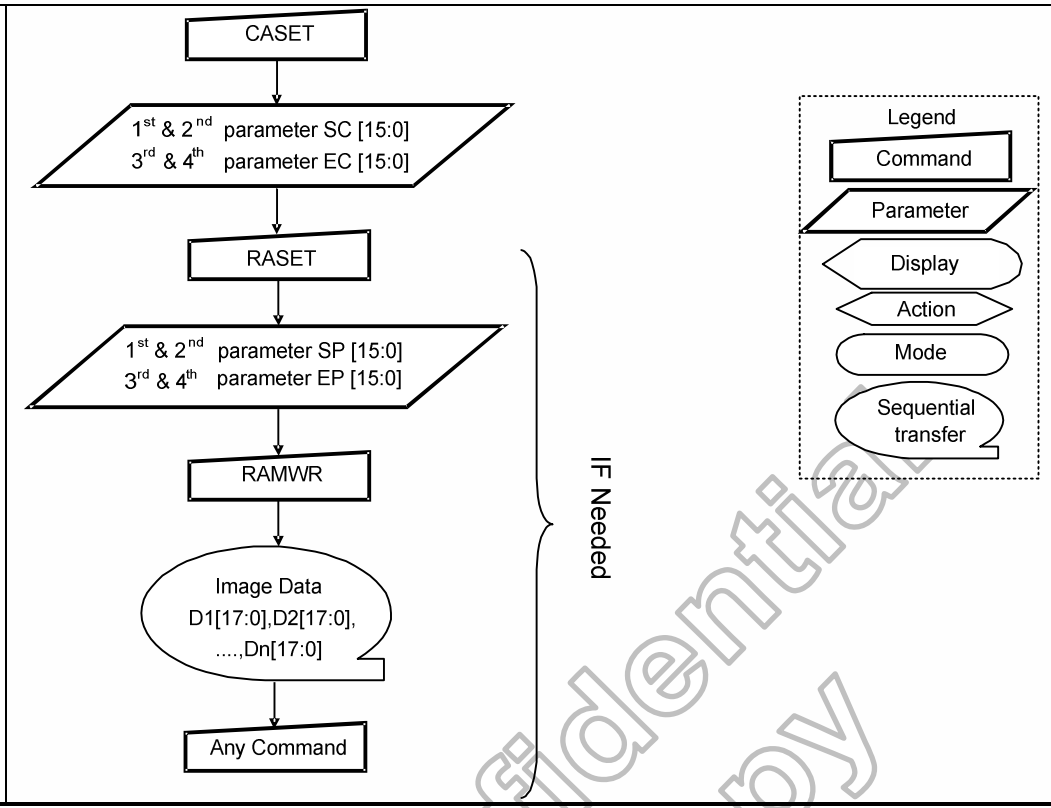
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SC[15:0]=0000h	EC[15:0]=0083h
S/W Reset	When MADCTL's B5=0:	
	SC[15:0]=0000h	EC[15:0]=0083h
	When MADCTL's B5=1:	
	SC[15:0]=0000h	EC[15:0]=00A1h
H/W Reset	SC[15:0]=0000h	EC[15:0]=0083h

Flow Chart



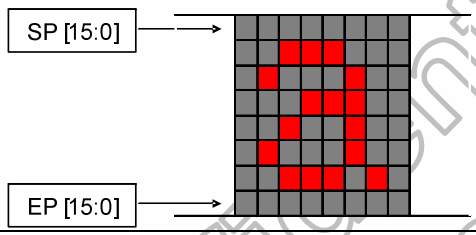
8.2.21 Page address set (2Bh)

2B H	PASET (Page Address Set)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	0	1	1	2B
1st parameter	1	↑	1	-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note
2nd parameter	1	↑	1	-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd parameter	1	↑	1	-	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note
4th parameter	1	↑	1	-	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access.
This command makes no change on the other driver status.
The values of SP[15:0] and EP[15:0] are referred when RAMWR command comes.
Each value represents one Page line in the Frame Memory.

(Example)



Restriction

SP[15:0] always must be equal to or less than EP[15:0]
Note: When SP[15:0] or EP[15:0] is greater than maximum row address like below, data of out of range will be ignored
0000h<=SP[15:0]<=EP[15:0]<=00A1h (When MADCTL's B5=0)
0000h<=SP[15:0]<=EP[15:0]<=0083h (When MADCTL's B5=1)

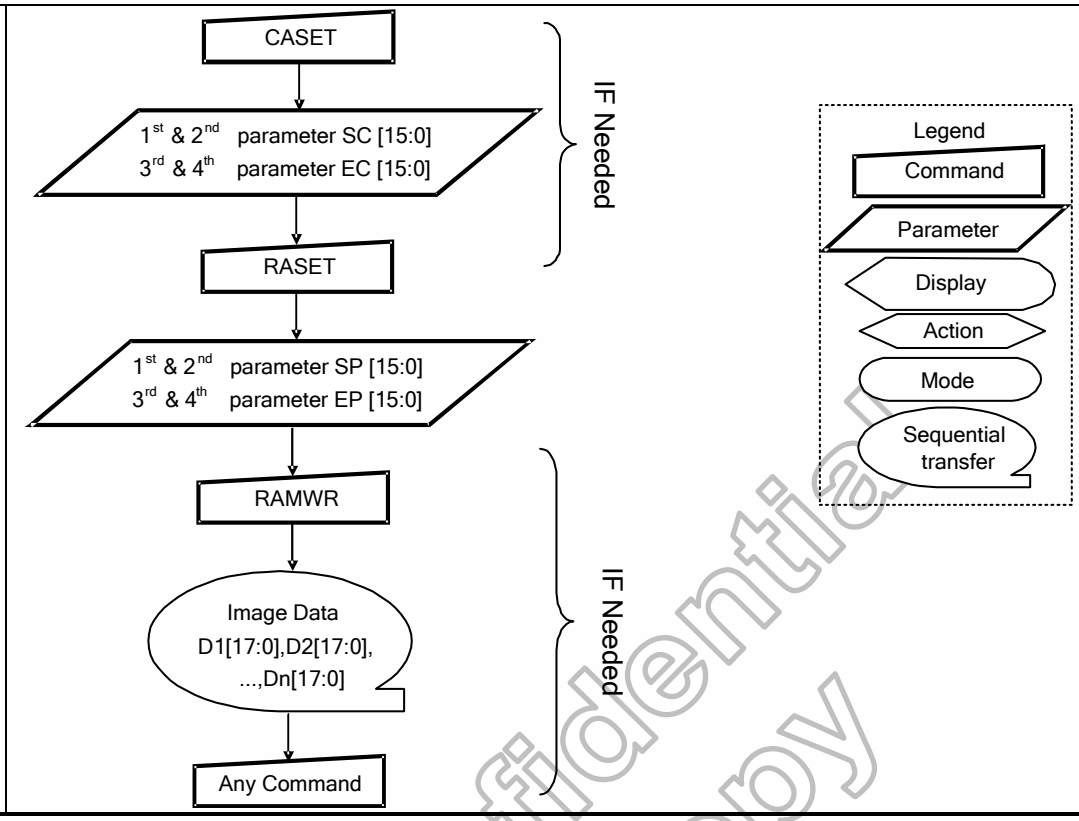
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value	
Power On Sequence	SP[15:0]=0000h	EP[15:0]=00A1h
S/W Reset	When MADCTL's B5=0:	
	SP[15:0]=0000h	EP[15:0]=00A1h
	When MADCTL's B5=1:	
	SP[15:0]=0000h	EP[15:0]=0083h
H/W Reset	SP[15:0]=0000h	EP[15:0]=00A1h

Flow Chart



8.2.22 Memory write (2Ch)

2C H	RAMWR (Memory Write)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	0	0	2C
1st parameter	1	↑	1	D1[15:0]									00..FF
:	1	↑	1	Dx[15:0]									00..FF
nth parameter	1	↑	1	Dn[15:0]									00..FF

Description

This command is used to transfer data from MCU to frame memory.
This command makes no change to the other driver status.
When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions.
The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 6.2)
Then D[7:0] is stored in frame memory and the column register and the page register incremented.
Sending any other command can stop frame Write.

Restriction

In all color modes, there is no restriction on length of parameters.

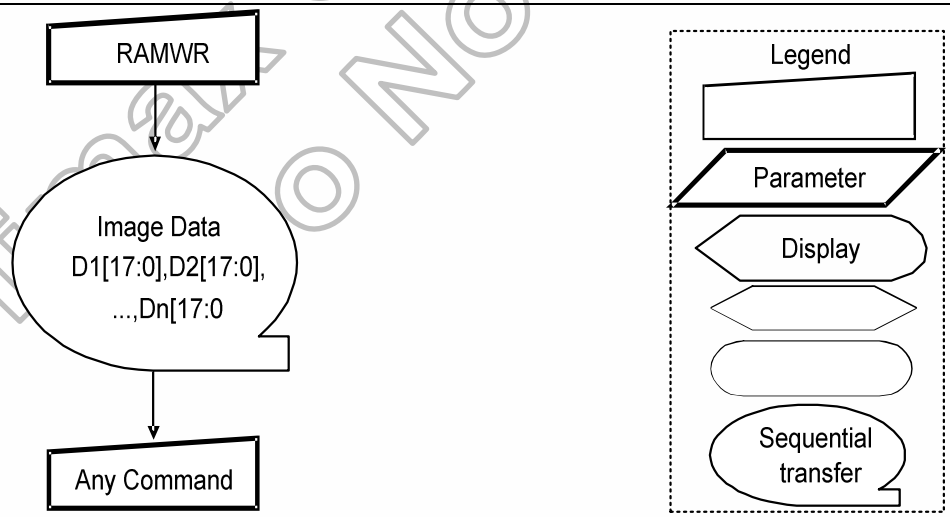
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



8.2.23 Color set (2Dh)

2D H	RGBSET (Color Set)											
	DNC	NRD	NWR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	HEX
Command	0	1	↑	0	0	1	0	1	1	0	1	2D
1st parameter	1	1	↑	X	X	R005	R004	R003	R002	R001	R000	00..FF
:	1	1	↑	X	X	Rnn5	Rnn4	Rnn3	Rnn2	Rnn1	Rnn0	00..FF
32th parameter	1	1	↑	X	X	R315	R314	R313	R312	R311	R310	00..FF
33rd parameter	1	1	↑	X	X	G005	G004	G003	G002	G001	G000	00..FF
:	1	1	↑	X	X	Gnn5	Gnn4	Gnn3	Gnn2	Gnn1	Gnn0	00..FF
96th parameter	1	1	↑	X	X	G635	G634	G633	G632	G631	G630	00..FF
97th parameter	1	1	↑	X	X	B005	B004	B003	B002	B001	B000	00..FF
:	1	1	↑	X	X	Bnn5	Bnn4	Bnn3	Bnn2	Bnn1	Bnn0	00..FF
128th parameter	1	1	↑	X	X	B315	B314	B313	B312	B311	B310	00..FF
Description	This command is used to define the LUT for 12bit-to-18bit/16bit-to-18bit color depth conversions. (See also section 5.2) 128 bytes must be written to the LUT regardless of the color mode. This command has no effect on other commands/parameters and Contents of frame memory. Visible change takes effect next time the Frame Memory is written to.											
Restriction	-											

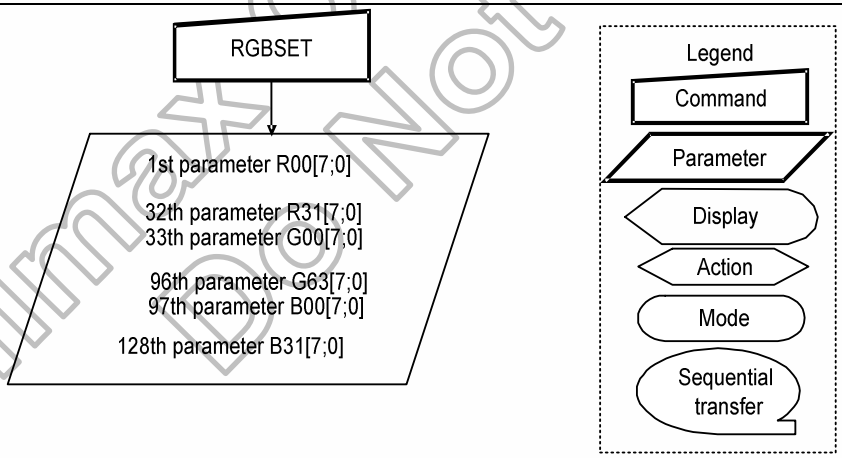
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Random values
S/W Reset	Contents of the look-up table protected
H/W Reset	Random values

Flow Chart



8.2.24 Memory read (2Eh)

2E H	RAMRD (Memory Read)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	0	1	1	1	0	2E
1st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	↑	1	D1[15:0]									00..FF
:	1	↑	1	Dx[15:0]									00..FF
(n+1)th parameter	1	↑	1	Dn[15:0]									00..FF
Description	This command is used to transfer data from frame memory to MCU. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting. (See 6.2) Then D[7:0] is read back from the frame memory and the column register and the page register incremented Frame Read can be stopped by sending any other command.												
Restriction	-												

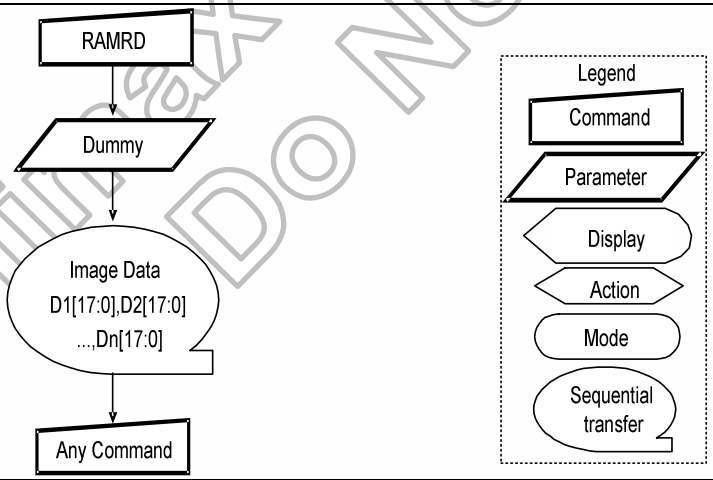
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

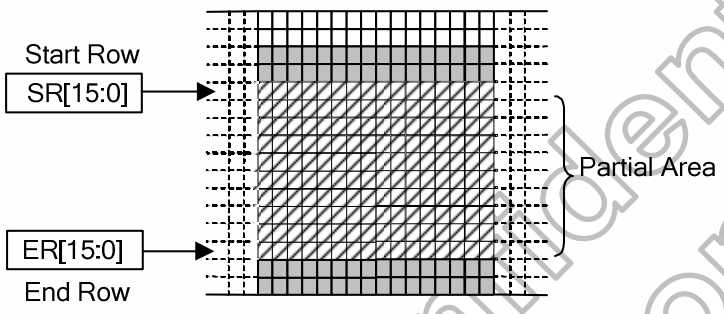
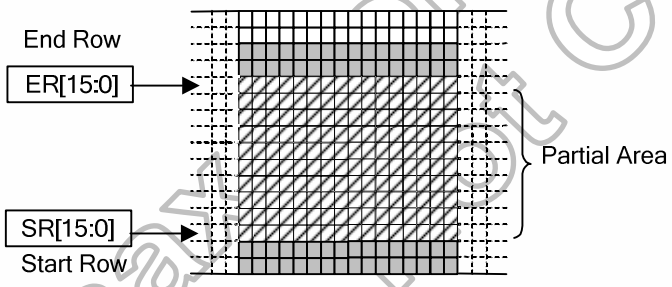
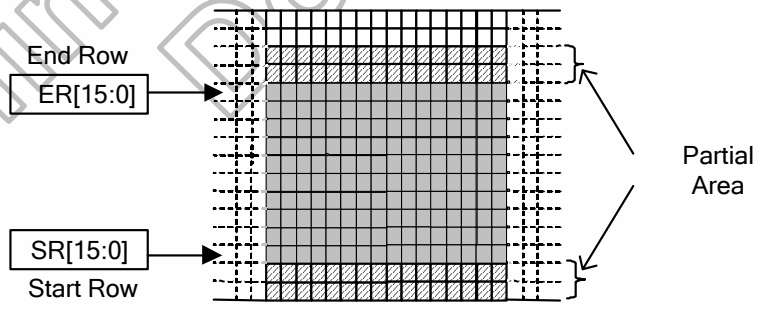
Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
S/W Reset	Contents of memory is not cleared
H/W Reset	Contents of memory is not cleared

Flow Chart



8.2.25 Partial area (30h)

30 H	PLTAR (Partial Area)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	0	0	30
1st parameter	1	↑	1	-	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	0000: 013F
2nd parameter	1	↑	1	-	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
3rd parameter	1	↑	1	-	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	0000: 013F
4th parameter	1	↑	1	-	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	
Description	This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row > Start Row when MADCTL B4(ML) = 0:  If End Row > Start Row when MADCTL B4(ML) = 1:  If End Row<Start Row when MADCTL's B4(ML) = 0:  If End Row = Start Row then the Partial Area will be one row deep.												
Restriction	SR[15:0] and ER[15:0] cannot be exceeding than 00A1h.												

Register Availability

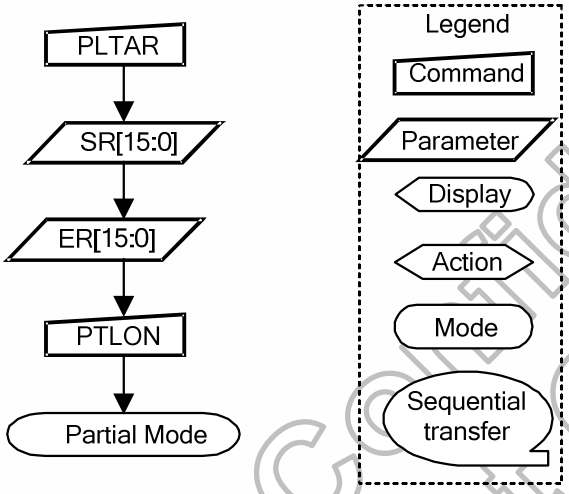
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

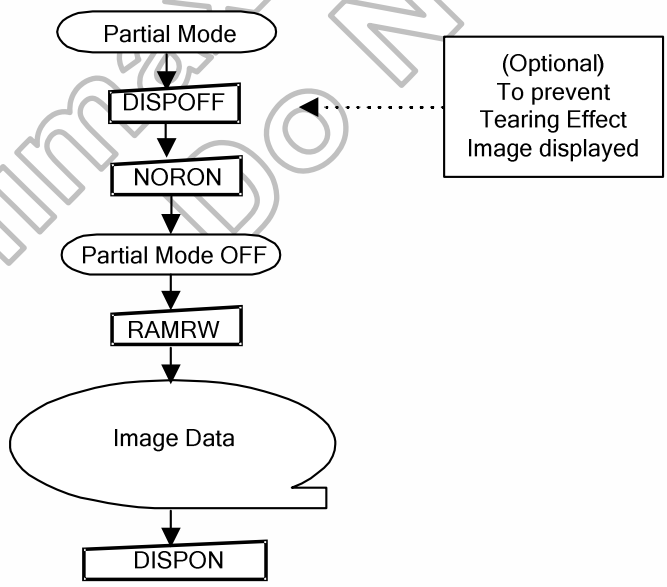
Status	Default Value	
Power On Sequence	SR[15:0]=0000h	ER[15:0]=00A1h
S/W Reset	SR[15:0]=0000h	ER[15:0]=00A1h
H/W Reset	SR[15:0]=0000h	ER[15:0]=00A1h

Flow Chart

1. To Enter Partial Display Mode:

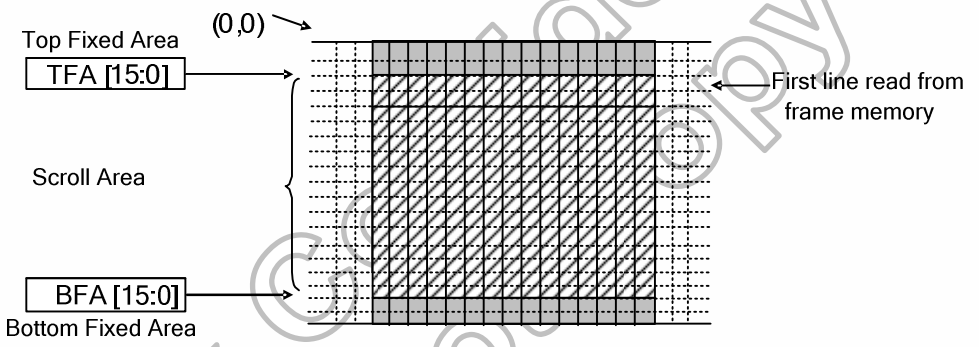


2. To Leave Partial Display Mode

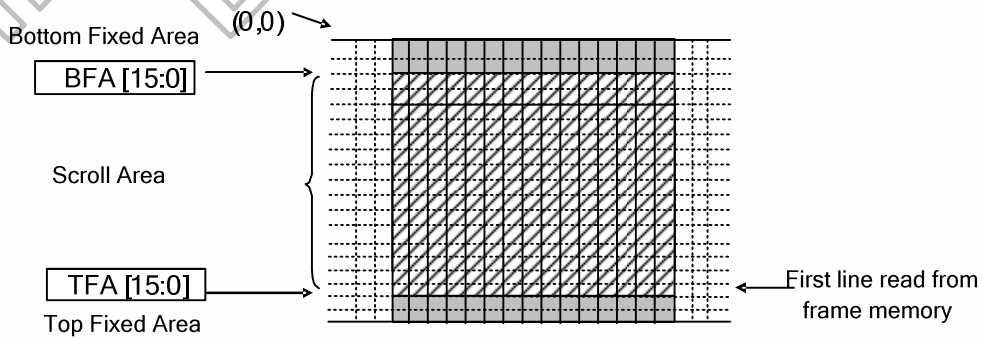


8.2.26 Vertical scrolling definition (33h)

33 H	VSCRDEF (Vertical Scrolling Definition)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	0	1	1	33
1st parameter	1	↑	1	-	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8	0000:
2nd parameter	1	↑	1	-	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0	00A2
3rd parameter	1	↑	1	-	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8	0000:
4th parameter	1	↑	1	-	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0	00A2
5th parameter	1	↑	1	-	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8	0000:
6th parameter	1	↑	1	-	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0	00A2
Description	This command defines the Vertical Scrolling Area of the display. When MADCTL B4=0, the 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from top of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.
Restriction	The condition is (TFA+VSA+BFA)=162, otherwise Scrolling mode is undefined. In Vertical Scroll Mode, MADCTL B5 should be set to '0' – this only affects the Frame Memory Write.



When MADCTL B4=1
The 1st & 2nd parameter TFA[15:0] describes the Top Fixed Area (in No. of lines from bottom of the Frame Memory and Display). The 3rd & 4th parameter VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area. The 5th & 6th parameter BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



Register Availability

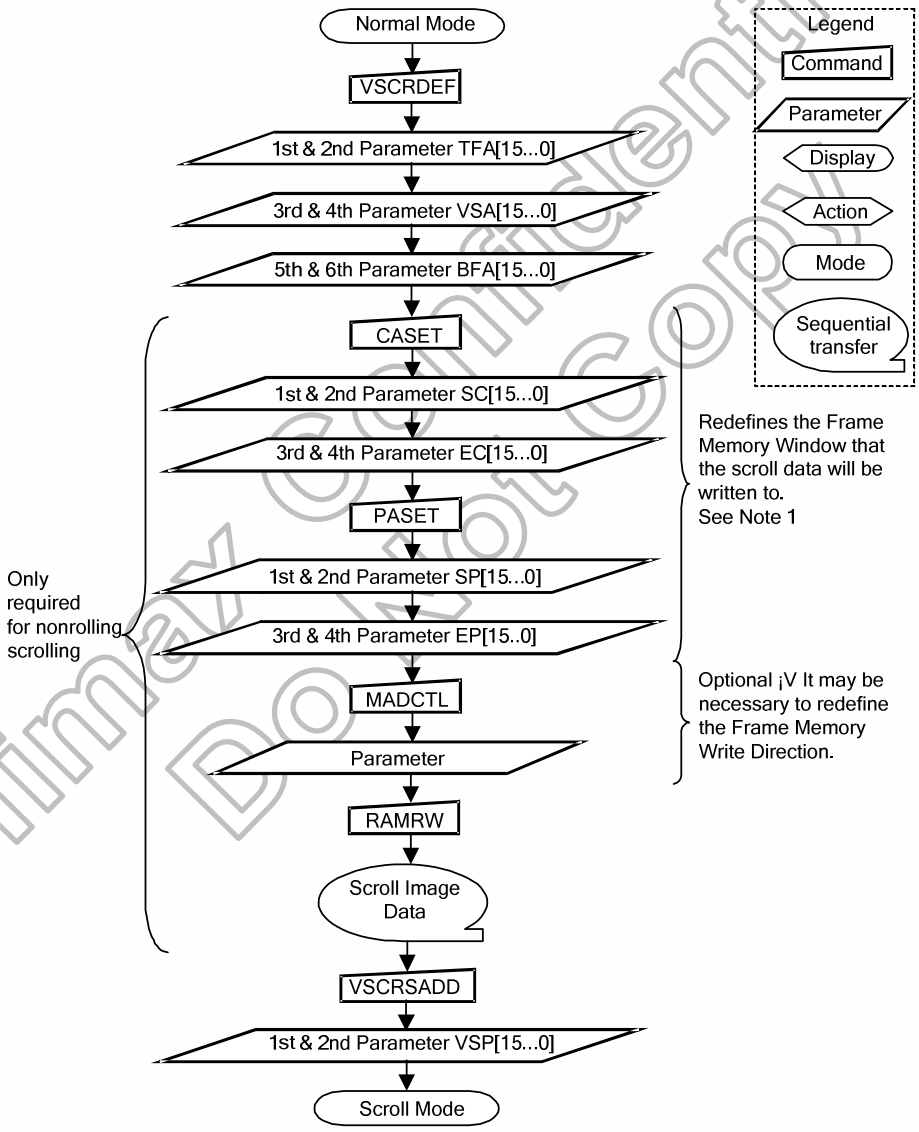
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value		
Power On Sequence	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000
S/W Reset	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000
H/W Reset	TFA[15:0]=0000	VSA[15:0]=00A2h	BFA[15:0]=0000

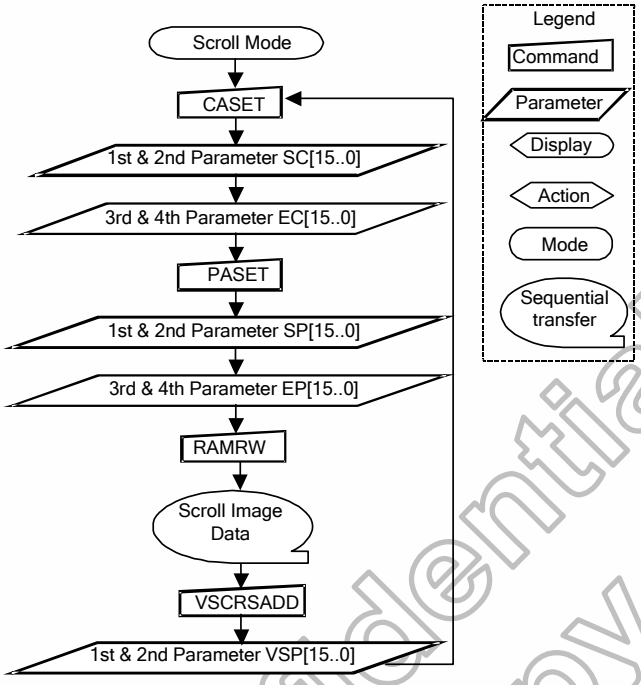
Flow Charts

1. To enter Vertical Scroll Mode:

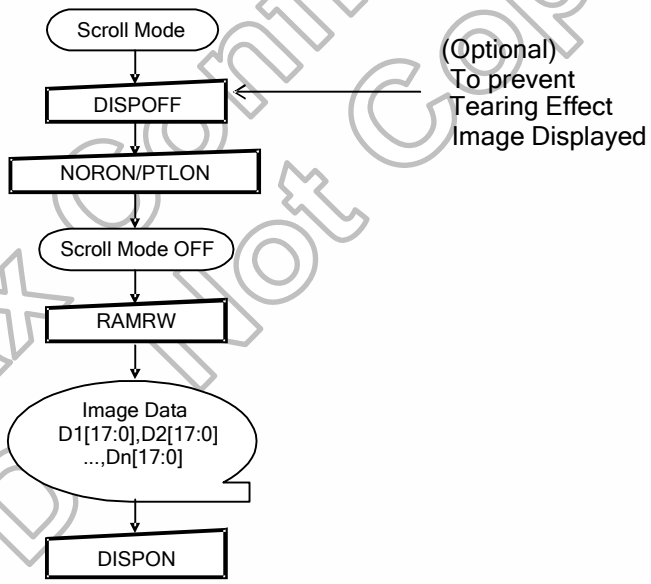


Note: The Frame Memory Window size must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll:



3. To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode On (13h) and Partial Mode On (12h) commands.

8.2.27 Tearing effect line off (34h)

34 H	TEOFF (Tearing Effect Line OFF)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	0	34
Parameter	No Parameter												
Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

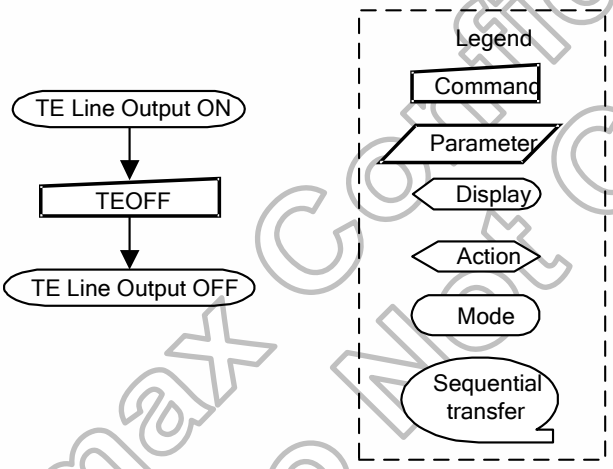
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



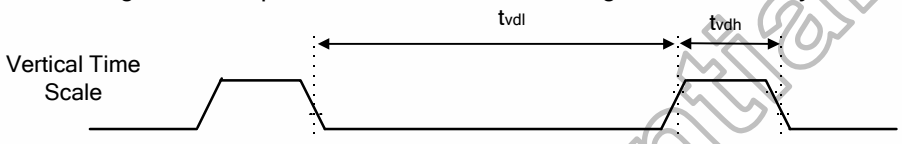
8.2.28 Tearing effect line on (35h)

35 H	TEON (Tearing Effect Line ON)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	0	1	35
1stparameter	0	↑	1	-	-	-	-	-	-	-	-	TEMODE	-

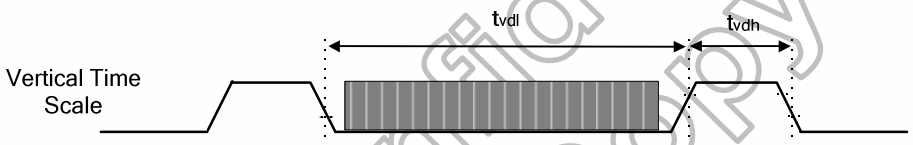
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).

When TEMODE=0:
The Tearing Effect Output line consists of V-Blanking information only:



When TEMODE=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

Restriction

This command has no effect when Tearing Effect output is already ON.

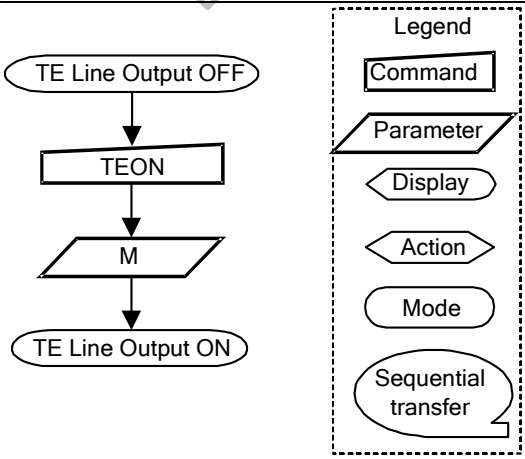
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



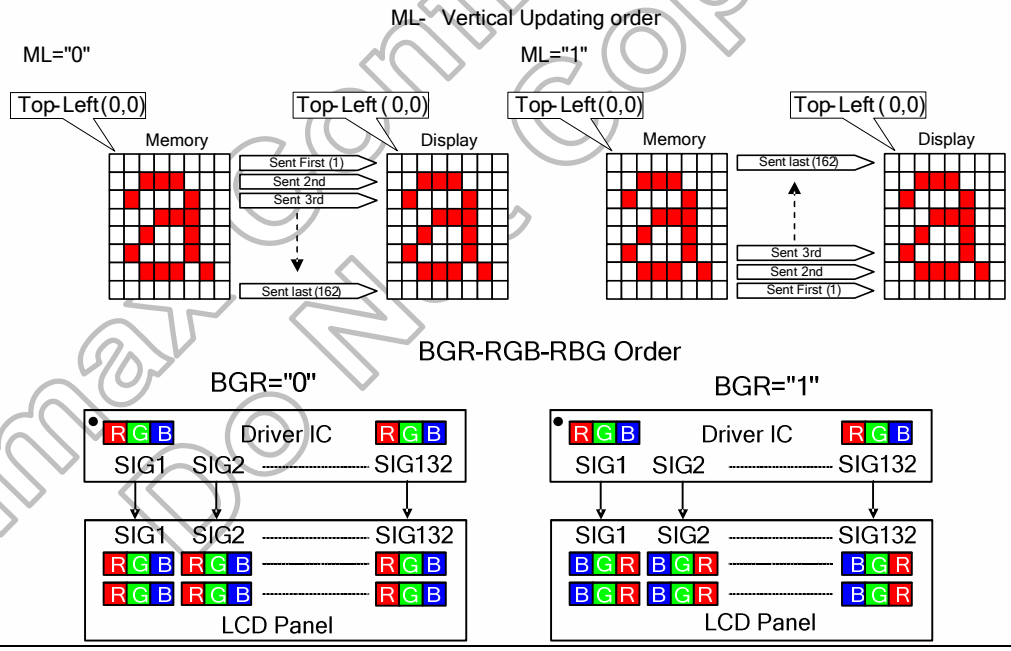
8.2.29 Memory access control (36h)

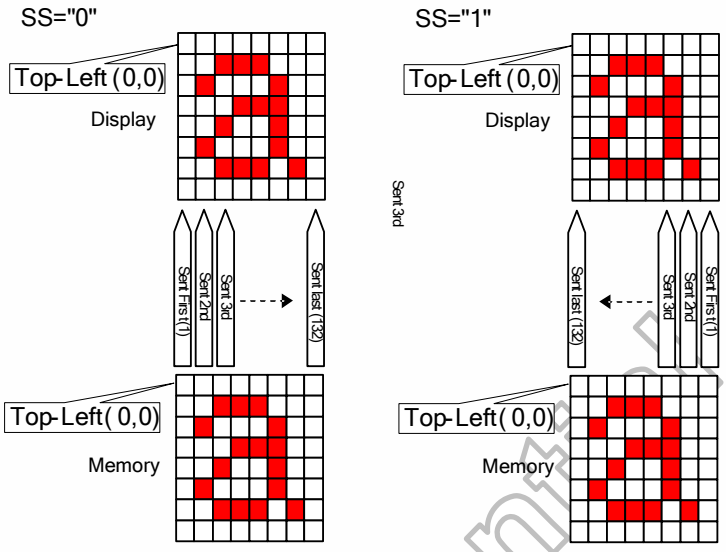
36 H	MADCTL (Memory Access Control)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	0	1	1	0	36
1st parameter	1	↑	1	-	MY	MX	MV	ML	BGR	SS	-	-	-

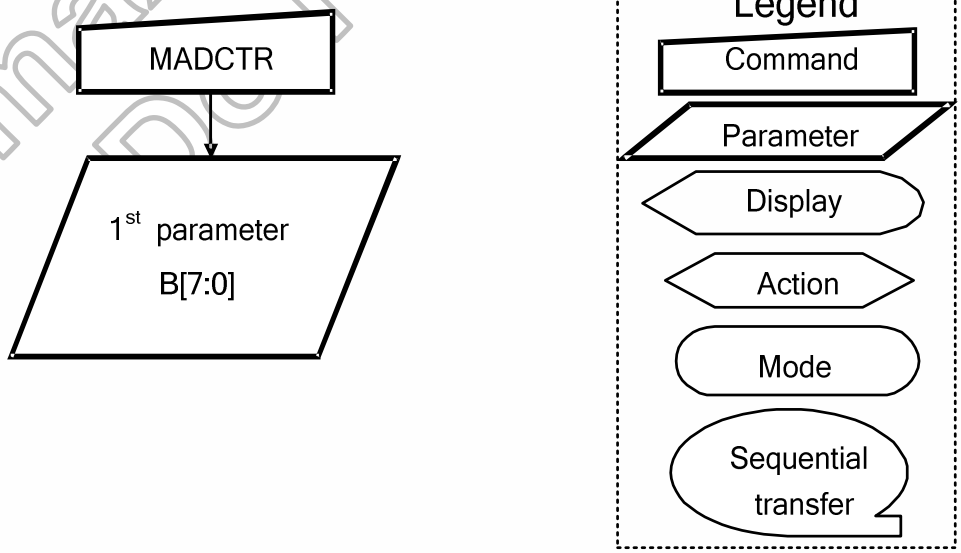
Description

This command defines read/write sc oning direction of frame memory.
This command makes no change on the other driver status.
Bit Assignment

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write/read direction. See Section 6.2.1 “MCU to memory write/read direction”
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
ML	Vertical ORDER	LCD vertical refresh direction control
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
SS	Horizontal ORDER	LCD horizontal refresh direction control



<table>
<tr><td></td><td>SS- Horizontal Updating order
 

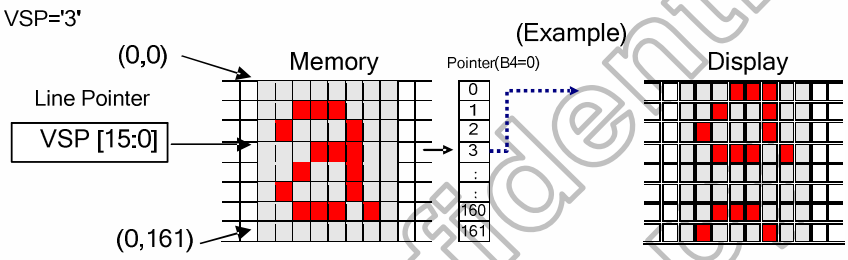
Note: Top-Left (0,0) means a physical memory location.</td></tr>
<tr><td>Restriction</td><td>D1 and D0 are set to ‘00’ internally. D2 is implemented if the LCD is updating pixel-by pixel. D2 is set to ‘0’ internally if the LCD is updating line-by-line.</td></tr>
<tr><td>Register Availability</td><td><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

8.2.30 Vertical scrolling start address (37h)

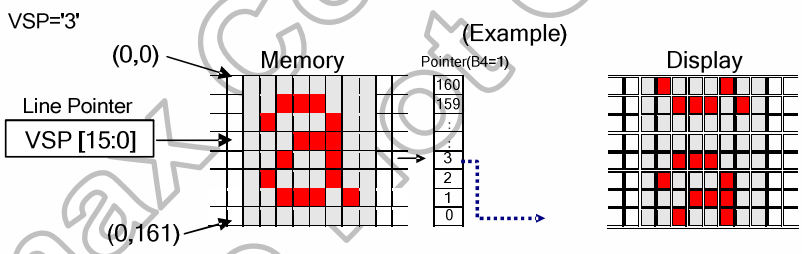
37 H	VSCRSADD (Vertical Scrolling Start Address)												
	DNC	NRD	NWR	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	-	0	0	1	1	0	1	1	1	37
1st parameter	1	1	↑	-	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8	01.
2nd parameter	1	1	↑	-	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0	3F

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

When MADCTL B4='0'
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and



When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.
VSP refers to the Frame Memory line Pointer.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the Frame Memory), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h) – otherwise undesirable image will be displayed on the Panel.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart

See Vertical Scrolling Definition (33h) description.

8.2.31 Idle mode off (38h)

38 H	IDMOFF (Idle Mode Off)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	0	38
Parameter	NO PARAMETER												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors.												
Restriction	1. This command has no effect when module is already in idle off mode. 2. RGB I/F enable, this command is working as a NOP (00h) command.												

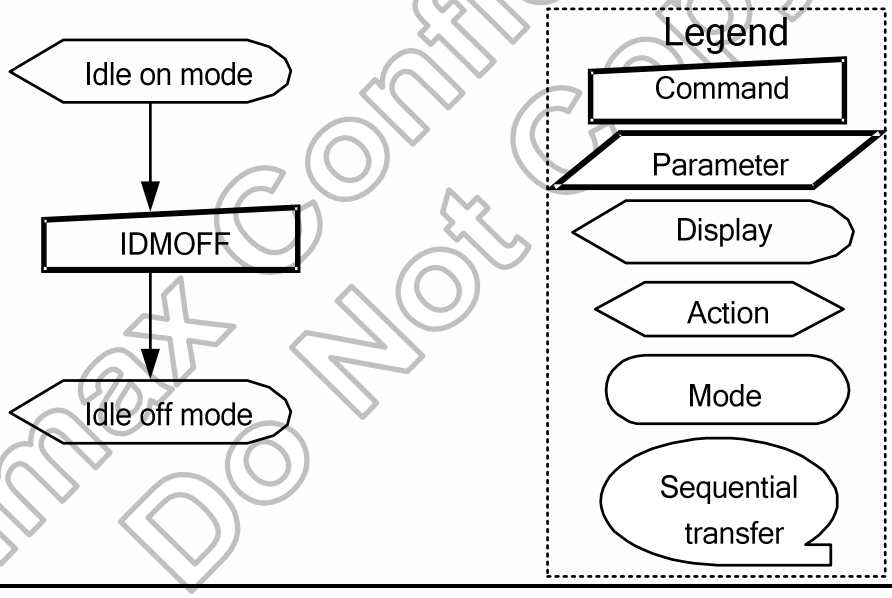
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

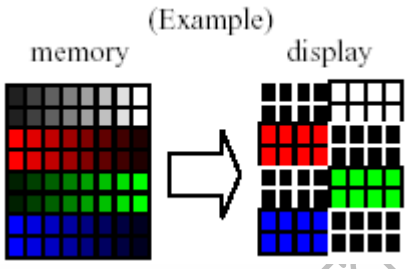


8.2.32 Idle mode on (39h)

39 H	IDMON (Idle Mode On)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	0	1	39
Parameter	NO PARAMETER												

Description

This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory contents vs. Display Color			
	$R_5 R_4 R_3 R_2 R_1 R_0$	$G_5 G_4 G_3 G_2 G_1 G_0$	$B_5 B_4 B_3 B_2 B_1 B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

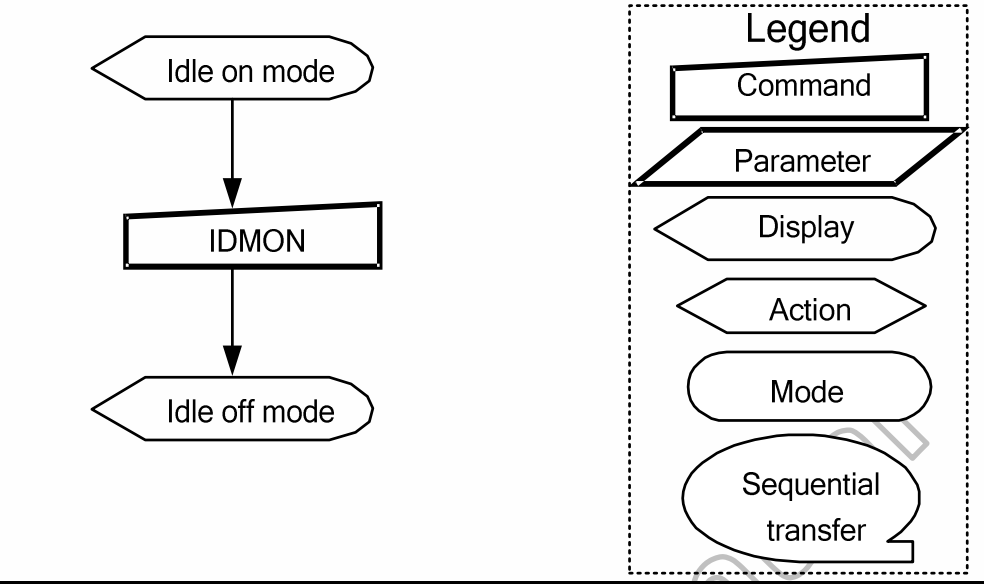
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart	

8.2.33 Interface pixel format (3Ah)

3A H	COLMOD (Interface Pixel Format)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	0	0	1	1	1	0	1	0	3A
1st parameter	1	↑	1	-	-	-	-	-	-	D2	D1	D0	011, 101, 110

Description

This command is used to define the format of RGB picture data, which is to be transfer via the system interface. The formats are shown in the table:

Interface Format	D2	D1	D0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
12 Bit/Pixel	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

Restriction

-

Register Availability

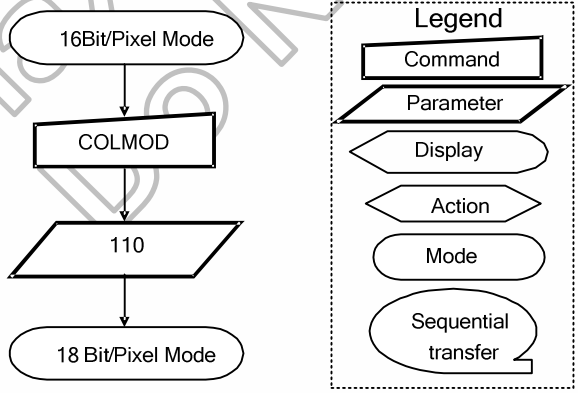
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	18-bit/pixel
S/W Reset	No Change
H/W Reset	18-bit/pixel

Flow Chart

Example:



8.2.34 Read ID1 (DAh)

DA H	RDID1 (Read ID1)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	0	DA
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	module's manufacturer m[7:0]								-
Description	This read byte identifies the LCD module's manufacturer.												
Restriction	-												

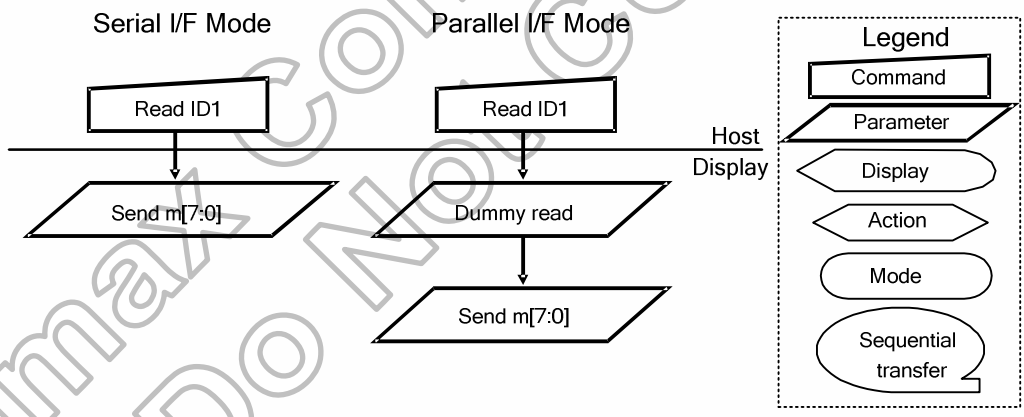
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



8.2.35 Read ID2 (DBh)

DB H	RDID2 (Read ID2)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	0	1	1	DB
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	1	V6	V5	V4	V3	V2	V1	V0	-

Description

This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See the following table.

ID Byte Value V[7:0]	Version	Changes
80h	-	-
81h	-	-
82h	-	-
83h	-	-
84h	-	-
85h	-	-

Restrictions

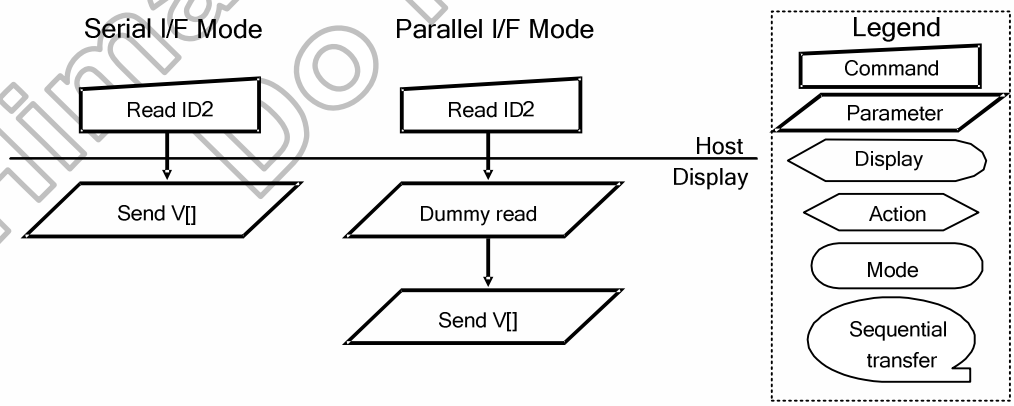
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	See Description
S/W Reset	See Description
H/W Reset	See Description

Flow Chart



8.2.36 Read ID3 (DCh)

DC H	RDID3 (Read ID3)												
	DNC	NWR	NRD	D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	1	1	1	0	0	DC
1st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-
2nd parameter	1	1	↑	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	-
Description	This read byte identifies the LCD module/driver.												
Restrictions													

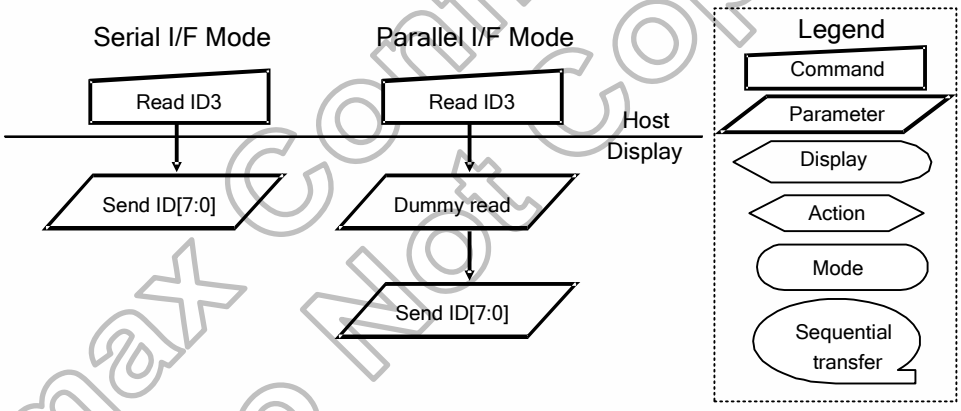
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	xxHEX
S/W Reset	xxHEX
H/W Reset	xxHEX

Flow Chart



8.2.37 SETOSC: set internal oscillator (B0h)

B0 H	SETOSC(Set Internal Oscillator)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	0	0	B0
1st parameter	1	↑	1	-	I_RADJ[1:0]				N_RADJ[1:0]				C4
2nd parameter	1	↑	1	-	-	-	-	-	-	-	-	OSC_EN	00

Description

These command is used to set internal oscillator related setting
OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop.
N_RADJ[1:0]: Internal oscillator frequency adjusts in Normal / Partial mode.
I_RADJ[1:0]: Internal oscillator frequency adjusts in Idle(8-color) / Partial Idle mode.

For details, please refer to "7.1 Internal Oscillator" section.

RADJ1	RADJ0	Internal Oscillator Frequency
0	0	147.4%
0	1	127.1%
1	0	111.7%
1	1	100%

Restrictions

If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	I_RADJ[1:0]=11, N_RADJ[1:0]=10, OSC_EN=0
S/W Reset	OSC_EN=0, others no change
H/W Reset	I_RADJ[1:0]=11, N_RADJ[1:0]=10, OSC_EN=0

Flow Chart

-

8.2.38 SETPOWER: set power (B1h)

B1 H	SETPOWER (Set Power)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	0	1	B1
1st parameter	1	↑	1	-	-	-	-	-	-	-	DP_STB	DP_STB_S	00
2nd parameter	1	↑	1	-	-	-	-	-	-	BT[2:0]			01
3rd parameter	1	↑	1	-	-	-	VRH[5:0]						1B
4th parameter	1	↑	1	-	-	-	-	-	-	AP[2:0]			03
5th parameter	1	↑	1	-	FS0[7:0]								04
6th parameter	1	↑	1	-	FS1[7:0]								04
7th parameter	1	↑	1	-	-	-	-	-	-	-	-	-	11
8th parameter	1	↑	1	-	GASEN	VCOMG	-	PON	DK	-	-	STB	89

Description

DP_STB, DP_STB_S : These two bits can let the driver into the deep standby mode. And when into deep standby, all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained.

VRH[5:0]: Specify the VREG1 voltage adjusting. VREG1 voltage is for gamma voltage setting.VREG1=Decimal(VRH[5:0])x0.05+3.3.

VRH5	VRH4	VRH3	VRH2	VRH1	VRH0	VREG1
0	0	0	0	0	0	3.30
0	0	0	0	0	1	3.35
0	0	0	0	1	0	3.40
0	0	0	0	1	1	3.45
0	0	0	1	0	0	3.50
0	0	0	1	0	1	3.55
:	:	:	:	:	:	:
0	1	1	1	0	1	4.75
0	1	1	1	1	0	4.80
0	1	1	1	1	1	STOP
1	0	0	0	0	0	STOP
:	:	:	:	:	:	:
1	1	0	0	0	0	STOP
1	1	0	0	0	1	STOP
1	1	0	0	1	0	STOP
1	1	0	0	1	1	STOP
:	:	:	:	:	:	:
1	1	1	1	1	0	STOP
1	1	1	1	1	1	Internal circuit operations stop. The gamma voltage can be adjusted from external VREG1 input.

Note: (1) Internal reference voltage VREF=4.8V (Please set DDVDH_TRI=0)
(2) Internal VREF can be modified by Custom' s special request.
VREG1={Decimal(VRH[5:0])x0.05+3.3 }*(VREF/4.8) (Please set DDVDH_TRI=0)

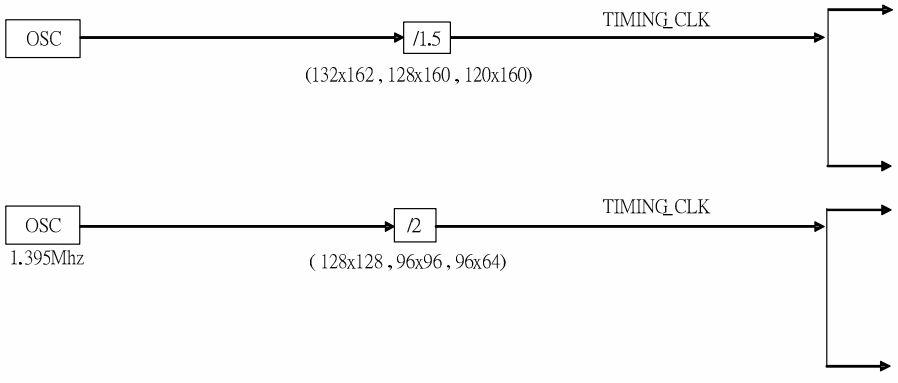
BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	5.0V	-VCI	11V ~ 14.5V	-8V ~ -12.5V
0	0	1	5.0V	-VCI	11V ~ 14.5V	-6V ~ -10V
0	1	0	5.0V	-VCI	11V ~ 14.5V	-5V ~ -7V
0	1	1	5.0V	-VCI	9V ~ 12.5V	-8V ~ -12.5V
1	0	0	5.0V	-VCI	9V ~ 12.5V	-6V ~ -10V
1	0	1	5.0V	-VCI	9V ~ 12.5V	-5V ~ -7V
1	1	0	5.0V	-VCI	8V ~ 10V	-6V ~ -10V
1	1	1	5.0V	-VCI	8V ~ 10V	-5V ~ -7V

Note1: When VCI = 2.8V and DDVDH_TRI=0
Note2: The "VGH" & "VGL" value depend on panel
Note3: The VGH v.s Ivgh and VGL v.s. Ivgl ,please reference the chapter 11.3 DC characteristic

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Small
0	1	1	Small
1	0	0	Medium
1	0	1	Medium High
1	1	0	Large
1	1	1	Small



FS0[7:0]: Set the operating frequency for DDVDH and VCL voltage generation.
For details, please refer to "7.1 Internal Oscillator" section.

FS07	FS06	FS05	FS04	FS03	FS02	FS01	FS00	Operation Frequency for DDVDH and VCL
0	0	0	0	0	0	0	0	TIMING_CLK/2
0	0	0	0	0	0	0	1	TIMING_CLK/2
0	0	0	0	0	0	1	0	TIMING_CLK/4
0	0	0	0	0	0	1	1	TIMING_CLK/6
0	0	0	0	0	1	0	0	TIMING_CLK/8
0	0	0	0	0	1	0	1	TIMING_CLK/10
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	TIMING_CLK/508
1	1	1	1	1	1	1	1	TIMING_CLK/510

Note : TIMING_CLK = TIMING_CLK/(2*X) ; X = FS0's Value.

FS1[7:0]: Set the operating frequency for VGH and VGL voltage generation.
For details, please refer to "7.1 Internal Oscillator" section.

FS17	FS16	FS15	FS14	FS13	FS12	FS11	FS10	Operation Frequency for VGH and VGL
0	0	0	0	0	0	0	0	TIMING_CLK/1
0	0	0	0	0	0	0	1	TIMING_CLK/1
0	0	0	0	0	0	1	0	TIMING_CLK/2
0	0	0	0	0	0	1	1	TIMING_CLK/3
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	TIMING_CLK/253
1	1	1	1	1	1	1	0	TIMING_CLK/254
1	1	1	1	1	1	1	1	TIMING_CLK/255

Note: TIMING_CLK = TIMING_CLK/X ; X = FS1's Value.
Ensure that the operation frequency of FS0 ≧ FS1.

STB: When STB = "1", the HX8353-D into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed.

a. Exit the Standby mode (STB = "0") ,
b. Start the oscillation

In the standby mode, the GRAM data and register content will be keeping.

GASEN: This stands for abnormal power-off monitor function when the power is off.
DK: Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

PON: Specify on/off control of step-up circuit 2 for VCL, VGL voltage generation.
For detail, see the Power Supply Setting Sequence.

PON	Operation of step-up circuit 2
0	OFF
1	ON

VCOMG: When VCOMG = '1', VCOML voltage can output to negative voltage. When

<table>
<tr><td></td><td>VCOMG = ‘0’, VCOML = GND.

DK: set “0” => DDVDH Enable, set “1” => DDVDH Disable.</td></tr>
<tr><td>Restrictions</td><td>If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>DP_STB=0, DP_STB_S=0, BT[2:0]=3’b011, VRH[5:0]=6’b011011, AP[2:0]=3’b011, FS0[7:0]=8’h01, FS1[7:0]=8’h10, BLANK_FS0[3:0]=4’b0001, BLANK_FS1[3:0]= 4’b0001, GASEN=1, VCOMG=0, PON=0, DK=1, STB=1</td></tr>
<tr><td>S/W Reset</td><td>VCOMG=0, PON=0, DK=1, STB=1, others no change</td></tr>
<tr><td>H/W Reset</td><td>DP_STB=0, DP_STB_S=0, BT[2:0]=3’b011, VRH[5:0]=6’b011011, AP[2:0]=3’b011, FS0[7:0]=8’h01, FS1[7:0]=8’h10, BLANK_FS0[3:0]=4’b0001, BLANK_FS1[3:0]= 4’b0001, GASEN=1, VCOMG=0, PON=0, DK=1, STB=1</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

8.2.39 SETDISPLAY: set display related register (B2h)

B2H	SETDISPLAY(Set Display Control)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	0	1	0	B2
1st parameter	1	↑	1	-	-	-	-	-	ISC[3:0]				01
2nd parameter	1	↑	1	-	PT[1:0]		PTV[1:0]		-	-	PTG	REF	93
3rd parameter	1	↑	1	-	-	-	GON	DTE	D1	D0	-	-	20

Description

This command is used to set display related register

D[1:0]: When D1 = '1', display is on; when D1 = '0', display is off. When display is off, the display data is retained in the GRAM and the entire source outputs are set to the VSSD level.
When D[1:0]= '01', the internal display of the HX8353-D is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PT(0,0)	Operate	Operate
1	1	Display	Operate	Operate

GON, DTE:

GON	DTE	Gate Output
1	0	Fixed to VGL
1	1	Normal Operation

PT[1:0] : Specify the Non-display area source output in partial display mode.

		Source Output Level							
REV_Panel	GRAM Data	Display area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"	VCOM = "L"	VCOM = "H"
1 (Normally Black Panel)	18'h00000 : 18'h3FFFF	V63P : V0P	V0N : V63N	V63P	V0N	GND	GND	Hi-z	Hi-z
0 (Normally White Panel)	18'h00000 : 18'h3FFFF	V0P : V63P	V63N : V0N	V63P	V0N	GND	GND	Hi-z	Hi-z

REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

PTG: Specify the scan mode of gate driver in non-display area.

PTG	Gate Outputs in Non-display Area
0	Normal Drive
1	Fixed VGL

PTV[1:0]: Specify the scan mode of VCOM in non-display area.

PTV1	PTV0	VCOM Outputs in Non-display Area
0	0	Normal Drive
0	1	Fixed to VCOML
1	0	Fixed to GND
1	1	Setting Inhibited

ISC[3:0]: Specify the scan cycle of gate driver when REF = '1' in non-display area. Then scan cycle is set to Decimal(ISC[3:0])x4+1.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	1 frame	17ms
0	0	0	1	5 frames	83ms
0	0	1	0	9 frames	150ms
0	0	1	1	13 frames	217ms
0	1	0	0	17 frames	283ms
0	1	0	1	21 frames	350ms
0	1	1	0	25 frames	417ms
0	1	1	1	29 frames	483ms
1	0	0	0	33 frames	550ms
1	0	0	1	37 frames	616ms
1	0	1	0	41 frames	683ms
1	0	1	1	45 frames	750ms
1	1	0	0	49 frames	816ms
1	1	0	1	53 frames	883ms
1	1	1	0	57 frames	950ms
1	1	1	1	61 frames	1017ms

PT1	PT0	REF	ISC[3:0]	Source Output	VCOM Output	Gate Output
0	x	x	--	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving
1	0	0	--	GND	PTV[1:0]	PTG
		1	Non-refresh cycle	GND	PTV[1:0]	PTG
			Refresh cycle	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving
1	1	0	--	Hi-z	PTV[1:0]	PTG
		1	Non-refresh cycle	Hi-z	PTV[1:0]	PTG
			Refresh cycle	Black Display (REV_PANEL = '1') White Display (REV_PANEL = '0')	Normal Driving	Normal Driving

Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>ISC[3:0]=4’b0001, PT[1:0]=2’b10, PTV[1:0]=2’b01, PTG=1, REF=1, GON=1, DTE=0, D[1:0]=2’b00</td></tr>
<tr><td>S/W Reset</td><td>GON=1, D0=0, others no change</td></tr>
<tr><td>H/W Reset</td><td>ISC[3:0]=4’b0001, PT[1:0]=2’b10, PTV[1:0]=2’b10, PTG=1, REF=1, GON=1, DTE=0, D[1:0]=2’b00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>-</td></tr>
</table>

8.2.40 SETCYC: set display cycle register (B4h)

B4 H	SETCYC (Set display cycle)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	0	0	B4
1st parameter	1	↑	1	-	-	I/_NW[2:0]			-	N_NW[2:0]			01
2nd parameter	1	↑	1	-	I_RTN[3:0]				N_RTN[3:0]				04
3rd parameter	1	↑	1	-	I_DIV[3:0]				N_DIV[3:0]				FF
4th parameter	1	↑	1	-	N_DUM[7:0]								0C
5th parameter	1	↑	1	-	I_DUM[7:0]								0C
6th parameter	1	↑	1	-	GDON[7:0]								0D
7th parameter	1	↑	1	-	GDOF[7:0]								53
8th parameter	1	↑	1	-	L_BASE[7:0]								59

Description

This command is used to set display related register

N_ NW[2:0]: Specify LCD driving inversion type in Normal/ Partial mode.
I_ NW[2:0]: Specify LCD driving inversion type in Idle / Partial Idle mode.

NW[2:0]	LCD driving Inversion Type
0d	Frame inversion
1d	1-line inversion
2d	2-line inversion
3d	3-line inversion
:	:
6d	6-line inversion
7d	7-line inversion

N_DIV[3:0]: Specify the division ratio of internal clocks in Normal / Partial mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the N_RTN[3:0] bits (1H period clock cycle), N_DIV[3:0], and N_DUM[7:0] bits.

I_DIV[3:0]: Specify the division ratio of internal clocks in Idle (8-color) / Partial Idle mode for internal operation. When used internal clock for the display operation, frame frequency can be adjusted with the I_RTN[3:0] bits(1H period clock cycle), I_DIV[3:0], and I_DUM[7:0] bits.

fosc = R-C oscillation frequency

DIV3	DIV2	DIV1	DIV0	Division Ratio	Internal Display Operation Clock Frequency
0	0	0	0	1	fosc / 1
0	0	0	1	1	fosc / 1
0	0	1	0	1.5	fosc / 1.5
0	0	1	1	2	fosc / 2
0	1	0	0	2.5	fosc / 2.5
0	1	0	1	3	fosc / 3
0	1	1	0	3.5	fosc / 3.5
:	:	:	:	:	:
1	1	0	1	7	fosc / 7
1	1	1	0	7.5	fosc / 7.5
1	1	1	1	1.5	fosc / 1.5 (defaule)

N_RTN[3:0]: Specify clock number of one line period in Normal / Partial mode for internal operation.

I_ RTN[3:0]: Specify clock number of one line period in Idle (8-color) / Partial Idle mode for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN[3:0]	Clock number per Line
4'b0000	89
4'b0001	90
4'b0010	91
4'b0011	92
4'b0100	93
:	:
4'b1110	103
4'b1111	104

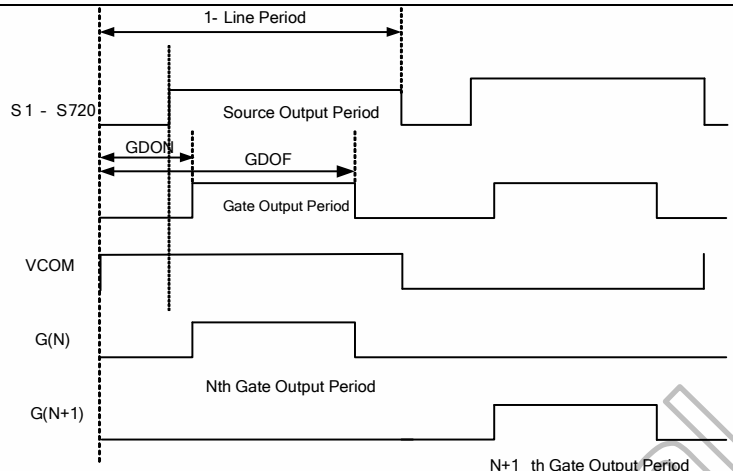
N_DUM[7:0]: Specify dummy line number in blanking area of one frame in Normal / Partial mode for internal operation.
I_DUM[7:0]: Specify dummy line number in blanking area of one frame in Idle (8-color) / Partial Idle mode for internal operation.

DUM[7:0]	Line number in blanking period
000d	Setting Inhibited
001d	Setting Inhibited
002d	2
003d	3
004d	4
:	:
190d	190
others	Setting Inhibited

Formula for the Frame Frequency during internal display mode:
Frame frequency = fosc/(RTN × DIV × (162+DUM)) [Hz]
fosc: RC oscillation frequency

GDON[7:0]: Specify the valid gate output start time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the setting "00h", "01h", "02h" is inhibited).

GDOF[7:0]: Specify the gate output end time in 1-line driving period. The period time value is defined as SYSCLK number in internal clock display mode. The period time value is defined as DOTCLK number in 18/16-bit bus width RGB display mode and is defined as DOTCLK/3 number in 6-bit bus width RGB display mode. (Please note that the GDON[7:0] + 1≤ GDOF[7:0] ≤ RTN-1).



L_BASE[7:0]: Basic line clock number. Internal line clock=L_BASE[7:0] + RTN[3:0].

Restrictions

If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	I_NW[2:0]=3'b000, N_NW[2:0]=3'b001, I_RTN[3:0]=4'b0000, N_RTN[3:0]=4'b0000, N_DUM[7:0]=8'b00001100, I_DUM[7:0]=8'b00001100, GDON[7:0]=8'b00001101, GDOF[7:0]=8'b01110000, RSO[2:0]=000: I_DIV[3:0]=N_DIV[3:0]=4'b0110, L_BASE[7:0]=8'h59 RSO[2:0]=001: I_DIV[3:0]=N_DIV[3:0]=4'b1000, L_BASE[7:0]=8'h53 RSO[2:0]=010: I_DIV[3:0]=N_DIV[3:0]=4'b0110, L_BASE[7:0]=8'h5A RSO[2:0]=011: I_DIV[3:0]=N_DIV[3:0]=4'b0110, L_BASE[7:0]=8'h5A RSO[2:0]=100: I_DIV[3:0]=N_DIV[3:0]=4'b1000, L_BASE[7:0]=8'h91 RSO[2:0]=011: I_DIV[3:0]=N_DIV[3:0]=4'b1000, L_BASE[7:0]=8'h98
S/W Reset	No change
H/W Reset	I_NW[2:0]=3'b000, N_NW[2:0]=3'b001, I_RTN[3:0]=4'b0000, N_RTN[3:0]=4'b0000, N_DUM[7:0]=8'b00001100, I_DUM[7:0]=8'b00001100, GDON[7:0]=8'b00001101, GDOF[7:0]=8'b01110000, RSO[2:0]=000: I_DIV[3:0]=N_DIV[3:0]=4'b0110, L_BASE[7:0]=8'h59 RSO[2:0]=001: I_DIV[3:0]=N_DIV[3:0]=4'b1000, L_BASE[7:0]=8'h53 RSO[2:0]=010: I_DIV[3:0]=N_DIV[3:0]=4'b0110, L_BASE[7:0]=8'h5A RSO[2:0]=011: I_DIV[3:0]=N_DIV[3:0]=4'b0110, L_BASE[7:0]=8'h5A RSO[2:0]=100: I_DIV[3:0]=N_DIV[3:0]=4'b1000, L_BASE[7:0]=8'h91 RSO[2:0]=011: I_DIV[3:0]=N_DIV[3:0]=4'b1000, L_BASE[7:0]=8'h98

Flow Chart

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8.2.41 SETBGP: set BGP voltage related register (B5h)

B5 H	SETBGP(Set VBGP Voltage)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	0	1	B5
1st parameter	1	↑	1	-	FBOFF	-	-	DDVDH_TRI	VVDHS_SEL[3:0]				0B
2nd parameter	1	↑	1	-	-	-	-	-	VREF[3:0]				0B
3rd parameter	1	↑	1	-	-	-	-	-	VR_TRIM[3:0]				07

Description

The DDVDH setting table:

Set VREF @	DDVDH_TRI=0				
	VVDHS_SEL[3:0]				DDVDH
1.8 V	0	0	0	0	4.068
	0	0	0	1	4.176
	0	0	1	0	4.284
	0	0	1	1	4.392
	0	1	0	0	4.5
	0	1	0	1	4.608
	0	1	1	0	4.716
	0	1	1	1	4.824
	1	0	0	0	4.932
	1	0	0	1	5.04
	1	0	1	0	5.148
	1	0	1	1	5.256
	1	1	0	0	5.364
	1	1	0	1	5.472
	1	1	1	0	5.58
	1	1	1	1	5.688

The VREF setting table:

DDVDH_TRI=0				
VREF[3:0]				VREF
0	0	0	0	4.1
0	0	0	1	4.2
0	0	1	0	4.3
0	0	1	1	4.4
0	1	0	0	4.45
0	1	0	1	4.5
0	1	1	0	4.55
0	1	1	1	4.6
1	0	0	0	4.65
1	0	0	1	4.7
1	0	1	0	4.75
1	0	1	1	4.8
1	1	0	0	4.85
1	1	0	1	4.9
1	1	1	0	4.95
1	1	1	1	5

The VR_TRIM setting table:

VR_TRIM[3:0]				VR
0	0	0	0	2.04
0	0	0	1	2
0	0	1	0	1.96
0	0	1	1	1.93
0	1	0	0	1.9
0	1	0	1	1.86
0	1	1	0	1.83
0	1	1	1	1.8
1	0	0	0	1.77
1	0	0	1	1.74
1	0	1	0	1.71
1	0	1	1	1.69
1	1	0	0	1.66
1	1	0	1	1.64
1	1	1	0	1.61
1	1	1	1	1.59

The DDVDH_TRI is setting to “0“ only .

Restrictions

If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	FBOFF=0, DDVDH_TRI=0, VVDHS_SEL[3:0]=4’b1001, VREF[3:0]=4’b1011, VR_TRIM[5:0]=6’b001000
S/W Reset	No change
H/W Reset	FBOFF=0, DDVDH_TRI=0, VVDHS_SEL[3:0]=4’b1001, VREF[3:0]=4’b1011, VR_TRIM[5:0]=6’b001000

Flow Chart

-

8.2.42 SETCOM: set VCOM voltage related register (B6h)

B6 H	SETCOM (Set VCOM Voltage)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	0	1	1	0	B6
1st parameter	1	↑	1	-	VMF7	VMF6	VMF5	VMF4	VMF3	VMF2	VMF1	VMF0	9E
2nd parameter	1	↑	1	-	VMH7	VMH6	VMH5	VMH4	VMH3	VMH2	VMH1	VMH0	6C
3rd parameter	1	↑	1	-	VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	54

Description

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

VMH[7:0]: Set the VCOMH voltage (High level voltage of VCOM). VCOM High voltage = Decimal(VMH[7:0])x0.015+2.5.

VMH 7	VMH 6	VMH 5	VMH 4	VMH 3	VMH 2	VMH 1	VMH 0	VCOMH (DDVDH_TRI=0)
0	0	0	0	0	0	0	0	2.500
0	0	0	0	0	0	0	1	2.515
0	0	0	0	0	0	1	0	2.530
0	0	0	0	0	0	1	1	2.545
0	0	0	0	0	1	0	0	2.560
0	0	0	0	0	1	0	1	2.575
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	0	0	1	0	0	1	1	4.705
1	0	0	1	0	1	0	0	4.720
1	0	0	1	0	1	0	1	4.735
1	0	0	1	0	1	1	0	4.750
1	0	0	1	0	1	1	1	4.765
1	0	0	1	1	0	0	0	4.780
1	0	0	1	1	0	0	1	4.795
1	0	0	1	1	0	1	0	4.800
1	0	0	1	1	0	1	1	4.800
1	0	0	1	1	1	0	0	4.800
1	0	0	1	1	1	0	1	4.800
:	:	:	:	:	:	:	:	4.800
1	1	0	1	1	0	1	1	4.800
1	1	0	1	1	1	0	0	4.800
:	:	:	:	:	:	:	:	4.800
1	1	1	1	1	1	1	0	4.800
1	1	1	1	1	1	1	1	Setting inhibited

Note: Internal VREF can be modified by customer's request. default VREF=4.8V (DDVDH_TRI=0)
VCOMH= {Decimal(VMH[7:0])x0.015+2.5 }*(VREF/4.8) (DDVDH_TRI=0)

VML[7:0]: Set the VCOML voltage (Low level voltage of VCOM). VCOM Low voltage = Decimal(VML[7:0])x0.015-2.5.

VML7	VML6	VML5	VML4	VML3	VML2	VML1	VML0	VCOML
0	0	0	0	0	0	0	0	-2.500
0	0	0	0	0	0	0	1	-2.485
0	0	0	0	0	0	1	0	-2.470
0	0	0	0	0	1	0	1	-2.455
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	1	1	-0.055
1	0	1	0	0	1	0	0	-0.040
1	0	1	0	0	1	0	1	-0.025
1	0	1	0	0	1	1	0	-0.010
1	0	1	0	0	1	1	1	VSSA
	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	VSSA

Note: Internal VREF can be modified by customer's request. default VREF=4.8V (DDVDH_TRI=0)
VCOML= { Decimal(VML[7:0])x0.015-2.5 }*(VREF/4.8) (DDVDH_TRI=0)

VMF[7:0]: Set the VCOM offset voltage. VMH+1d/VML+1d means VMH/VML from original setting move up one step (15mV). VMH-1d/VML-1d means VMH/VML from original setting move down one step (15mV)

VMF[7:0]	VCOMH	VCOML
0	"VMH" – 128d	"VMH" – 128d
1	"VMH" – 127d	"VMH" – 127d
2	"VMH" – 126d	"VMH" – 126d
3	"VMH" – 125d	"VMH" – 125d
:	:	:
126	"VMH" – 2d	"VMH" – 2d
127	"VMH" – 1d	"VMH" – 1d
128	"VMH"	"VML"
129	"VMH" + 1d	"VMH" + 1d
130	"VMH" + 2d	"VMH" + 2d
:	:	:
254	"VMH" + 126d	"VMH" + 126d
255	"VMH" + 127d	"VMH" + 127d

Note1 : VMH[7:0]-128+VMF[7:0]>=0 and VML[7:0]-128+VMF[7:0]>=0
Note2 : When Setting the VMF, be careful the VCOMH & VCOML voltage's range.

Restrictions

If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	OTP value
S/W Reset	No change
H/W Reset	OTP value

Flow Chart

-

8.2.43 SETEXTC: enable extension command (B9h)

B9 H	SETEXTC (Set Extended Command Set)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	1	0	0	1	B9
1st parameter	1	↑	1	-	EXTC1[7:0]								00
2nd parameter	1	↑	1	-	EXTC2[7:0]								00
3rd parameter	1	↑	1	-	EXTC3[7:0]								00

Description

This command is used to set extended command set access enable.

Extend cmd	Command description
Enable	After command (B9h), must write 3 parameters (FFh,83h,53h) by order
Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh,83h,53h)

Restrictions

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	EXTC1[7:0]=8'h00, EXTC2[7:0]=8'h00, EXTC3[7:0]=8'h00
S/W Reset	No change
H/W Reset	EXTC1[7:0]=8'h00, EXTC2[7:0]=8'h00, EXTC3[7:0]=8'h00

Flow Chart

-

8.2.44 SETOTP: set OTP setting (BBh)

BB H	SETOTP (Set OTP related setting)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	0	1	1	1	0	1	1	BB
1st parameter	1	↑	1	-	OTP_MASK[7:0]								00
2nd parameter	1	↑	1	-	OTP_INDEX[7:0]								00
3rd parameter	1	↑	1	-	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_EN	OTPTEST_EN	VPP_SEL	OTP_PROG	00
4th parameter	1	↑	1	-	-	-	-	-	OTP_PTM[1:0]		OTP_VRADJ[1:0]		00
5th parameter	1	1	↑	-	OTP_DATA[7:0]								00
Description	This command is used to set the OTP related setting. **OTP_MASK7~OTP_MASK0:** Bit programming mask, if 1, means don't programming this bit **OTP_INDEX7~OTP_INDEX0:** Set location of OTP to be programmed **OTP_EN:** When written to 1, internal register begin written to OTP **VPP_SEL:** When written to 1, PVSS voltage is fed to OTP **OTP_LOAD_DISABLE**: When written to 1, auto load from OTP to internal register when SLPOUT command received is disabled, this is used when OTP is not yet programmed **DCCLK_DISABLE:** Disable Pumping Clock **OTPTEST_EN:** 0 : normal mode, automatic OTP programming mode (by internal state machine) 1 : manual mode 0 is the default value **OTP_POR:** for OTP read/write timing control **OTP_PPROG :** 1'b1 to turn on OTP write mode. **OTP_PWE :** 1'b1 to write OTP. **OTP_PTM[1:0] :** OTP Test mode register, In-house use. **OTP_VRADJ[1:0] :** OTP VPP2 adjusts register, In-house use. **OTP_DATA[7:0] :** OTP read data.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In or Booster Off: Yes												
Default	Status / Default Value Power On Sequence: OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00 S/W Reset: OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00 H/W Reset: OTP_MASK[7:0]=8'h00, OTP_INDEX[7:0]=8'h00, OTP_LOAD_DISABLE=0, DCCLK_DISABLE=0, OTP_POR=0, OTP_PWE=0, OTP_EN=0, OTPTEST_EN=0, VPP_SEL=0, OTP_PROG=0, OTP_PTM[1:0]=2'b00, OTP_VRADJ[1:0]=2'b00												
Flow Chart	-												

8.2.45 SETVDC: set internal digital and GRAM voltage (BCh)

<table>
<tr><td>BC H</td><td colspan="13">SETVDC (set internal digital and GRAM voltage)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>BC</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td></td><td></td><td></td><td></td><td colspan="3">VDC_SEL[2:0] (100)</td><td></td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to set internal digital and GRAM voltage.
The VDC_SEL setting table:
<table>
<tr><td>Set VREF @</td><td colspan="3">VDC_SEL[2:0]</td><td>VDDD</td></tr>
<tr><td rowspan="8">1.8 V</td><td>0</td><td>0</td><td>0</td><td>1.28</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1.34</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1.38</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1.44</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1.5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1.6</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.7</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1.8</td></tr>
</table></td></tr>
<tr><td>Restrictions</td><td colspan="13">If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In or Booster Off</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>Power On Sequence</td><td>VDC_SEL[2:0]=100</td></tr>
<tr><td>S/W Reset</td><td>No change</td></tr>
<tr><td>H/W Reset</td><td>VDC_SEL[2:0]=100</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">-</td></tr>
</table>

8.2.46 SETSTBA: set source option (C0h)

C0 H	SETSTBA (Set Source Option)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	0	0	0	0	C0
1st parameter	1	↑	1	-	N_OPON[7:0]								18
2nd parameter	1	↑	1	-	I_OPON[7:0]								08
3rd parameter	1	↑	1	-	STBA[15:8]								0C
4th parameter	1	↑	1	-	STBA[7:0]								C4
5th parameter	1	↑	1	-	GENON[7:0]								10
6th parameter	1	↑	1	-	-	-	-	-	-	-	-	**OTP_S1B**	00
Description	This command is used to set source option setting. Internal used, not open.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	N_OPON[7:0]=8'h20, I_OPON[7:0]=8'h10, STBA[15:0]=16'h0000, GENON[7:0]=8'h16, OTP_S1B=0
S/W Reset	No change
H/W Reset	N_OPON[7:0]=8'h20, I_OPON[7:0]=8'h10, STBA[15:0]=16'h0000, GENON[7:0]=8'h16, OTP_S1B=0

Flow Chart: -

8.2.47 SETTID: set ID (C3h)

C3 H	SETID (Set ID)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	0	0	1	1	C3
1st parameter	1	↑	1	-	ID1[7:0]								00
2nd parameter	1	↑	1	-	ID2[7:0]								80
3rd parameter	1	↑	1	-	ID3[7:0]								00
Description	This command is used to set ID.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	OTP value
S/W Reset	No Change
H/W Reset	OTP value

Flow Chart: -

8.2.48 SETUADJ: (C6h)

C6 H	SETUADJ												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	0	1	1	0	C6
1st parameter	1	↑	1	-	-	I_UADJ[2:0]			-	N_UADJ[2:0]			33
Description	This command is used to set UADJ.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	I_UADJ[2:0]=03 ; N_UADJ[2:0]=03
S/W Reset	No Change
H/W Reset	I_UADJ[2:0]=03 ; N_UADJ[2:0]=03

Flow Chart: -

UADJ			Trimming Freq
0	0	0	228.6%
0	0	1	123.9%
0	1	0	112.0%
0	1	1	100.0%
1	0	0	87.9%
1	0	1	75.8%
1	1	0	63.6%
1	1	1	51.3%

8.2.49 SETCLOCK: (CBh)

CB H	SETECO												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	1	0	1	1	CB
1st parameter	1	↑	1	-	CADJ[3:0]				-	-	-	-	20
2nd parameter	1	↑	1	-	-	-	-	-	-	-	-	DCCLK_SYNC	01
Description	This command is used to set CLOCK.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	CADJ[3:0] (1000) ; DCCLK_SYNC(1)
S/W Reset	No Change
H/W Reset	CADJ[3:0] (1000) ; DCCLK_SYNC(1)

Flow Chart: -

CADJ[3:0]	Trimming Freq
0000	111.9%
0001	110.3%
0010	108.7%
0011	107.1%
0100	105.7%
0101	104.1%
0110	102.7%
0111	101.3%
1000	100.0%
1001	98.6%
1010	97.4%
1011	96.2%
1100	94.9%
1101	93.7%
1110	92.6%
1111	91.5%

8.2.50 SETPANEL: set panel characteristic (CCh)

CCH	SETPANEL(Set Panel Characteristic Register)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	0	0	1	1	0	0	CC
1st parameter	1	↑	1	-	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL	00
Description	This command is used to set Panel characteristic related register **REV_PANEL:** The source output data polarity selected. When REV_PANEL=0, normally white panel is selected. When REV_PANEL = 1, normally black panel is selected. **BGR_PANEL:** The color filter order direction selected. When BGR_PANEL=0, don't reverse the SRGB setting. When BGR_PANEL = 1, the color filter order will be reversed. **GS_PANEL:** The gate driver output shift direction selected. When GS_PANEL=0, the shift direction don't reverse. When GS_PANEL = 1, the shift direction will be reversed. **SS_PANEL:** The source driver output shift direction selected. When SS_PANEL=0, the shift direction don't reverse. When SS_PANEL = 1, the shift direction will be reversed.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Partial Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In or Booster Off — Availability: Yes												
Default	Status: Power On Sequence — Default Value: SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0 Status: S/W Reset — Default Value: No change Status: H/W Reset — Default Value: SS_PANEL=0, GS_PANEL=0, REV_PANEL=0, BGR_PANEL=0												
Flow Chart	-												

8.2.51 GETHID: Read Product ID (D0h)

<table>
<tr><td>D0H</td><td colspan="13">GETHID (Read Product ID)</td></tr>
<tr><td></td><td>DNC</td><td>NWR</td><td>NRD</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>↑</td><td>1</td><td>-</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D0</td></tr>
<tr><td>1st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td colspan="8">Dummy Read</td><td>xx</td></tr>
<tr><td>2st parameter</td><td>1</td><td>↑</td><td>1</td><td>-</td><td colspan="8">Product ID [7:0] (0110_0100)</td><td>64</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to Read Product ID</td></tr>
<tr><td>Restrictions</td><td colspan="13">If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>Power On Sequence</td><td>Product ID [7:0]=64H</td></tr><tr><td>S/W Reset</td><td>No change</td></tr><tr><td>H/W Reset</td><td>Product ID [7:0]=64H</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">-</td></tr>
</table>

8.2.52 SETGAMMA: set gamma curve (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	0	0	0	0	0	E0
1st parameter	1	↑	1	-	-	MP1[2:0]			-	MP0[2:0]			77
2nd parameter	1	↑	1	-	-	MP3[2:0]			-	MP2[2:0]			73
3rd parameter	1	↑	1	-	-	MP5[2:0]			-	MP4[2:0]			00
4th parameter	1	↑	1	-	-	-	-	-	CP0[3:0]				0D
5th parameter	1	↑	1	-	CP2[3:0]				CP1[3:0]				4F
6th parameter	1	↑	1	-	-	-	-	-	CP3[3:0]				08
7th parameter	1	↑	1	-	-	-	-	-	CP4[3:0]				09
8th parameter	1	↑	1	-	-	-	-	-	OP0[3:0]				00
9th parameter	1	↑	1	-	-	-	-	OP1[4:0]					0F
10th parameter	1	↑	1	-	-	-	-	-	CGM1[1:0]		CGM0[1:0]		0A
11st parameter	1	↑	1	-	-	MN1[2:0]			-	MN0[2:0]			77
12nd parameter	1	↑	1	-	-	MN3[2:0]			-	MN2[2:0]			40
13rd parameter	1	↑	1	-	-	MN5[2:0]			-	MN4[2:0]			00
14th parameter	1	↑	1	-	-	-	-	-	CN0[3:0]				09
15th parameter	1	↑	1	-	CN2[3:0]				CN1[3:0]				48
16th parameter	1	↑	1	-	-	-	-	-	CN3[3:0]				0F
17th parameter	1	↑	1	-	-	-	-	-	CN4[3:0]				0D
18th parameter	1	↑	1	-	-	-	-	-	ON0[3:0]				0F
19th parameter	1	↑	1	-	-	-	-	ON1[4:0]					00

Description	This command is used for Gamma Curve related Setting. For details, please refer to Section 7.2.
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	GC0 value
S/W Reset	No change
H/W Reset	GC0 value

Flow Chart	-

8.2.53 SETEQ: set EQ (E3h)

E3H	SETEQ(Set EQ)												
	DNC	NWR	NRD	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	↑	1	-	1	1	1	0	0	0	1	1	E3
1st parameter	1	↑	1	-	EQVCI_M1[7:0]								18
2nd parameter	1	↑	1	-	EQGND_M1[7:0]								08
3rd parameter	1	↑	1	-	EQVCI_M0[7:0]								00
4th parameter	1	↑	1	-	EQGND_M0[7:0]								08
5th parameter	1	↑	1	-	PREOE_M0[7:0]								00
6th parameter	1	↑	1	-	PREOE_M1[7:0]								00
Description	Internal used, not open.												
Restrictions	If EXTC is high or enable SETEXTC command (even EXTC = low) can enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In or Booster Off	Yes

Default

Status	Default Value
Power On Sequence	EQVCI_M1[7:0]=8'h10, EQGND_M1[7:0]=8'h08, EQVCI_M0[7:0]=8'h08, EQGND_M0[7:0]=8'h10, PREOE_M0[7:0]=8'h00, PREOE_M1[7:0]=8'h00
S/W Reset	No change
H/W Reset	EQVCI_M1[7:0]=8'h10, EQGND_M1[7:0]=8'h08, EQVCI_M0[7:0]=8'h08, EQGND_M0[7:0]=8'h10, PREOE_M0[7:0]=8'h00, PREOE_M1[7:0]=8'h00

Flow Chart: -

9. Layout Recommendation

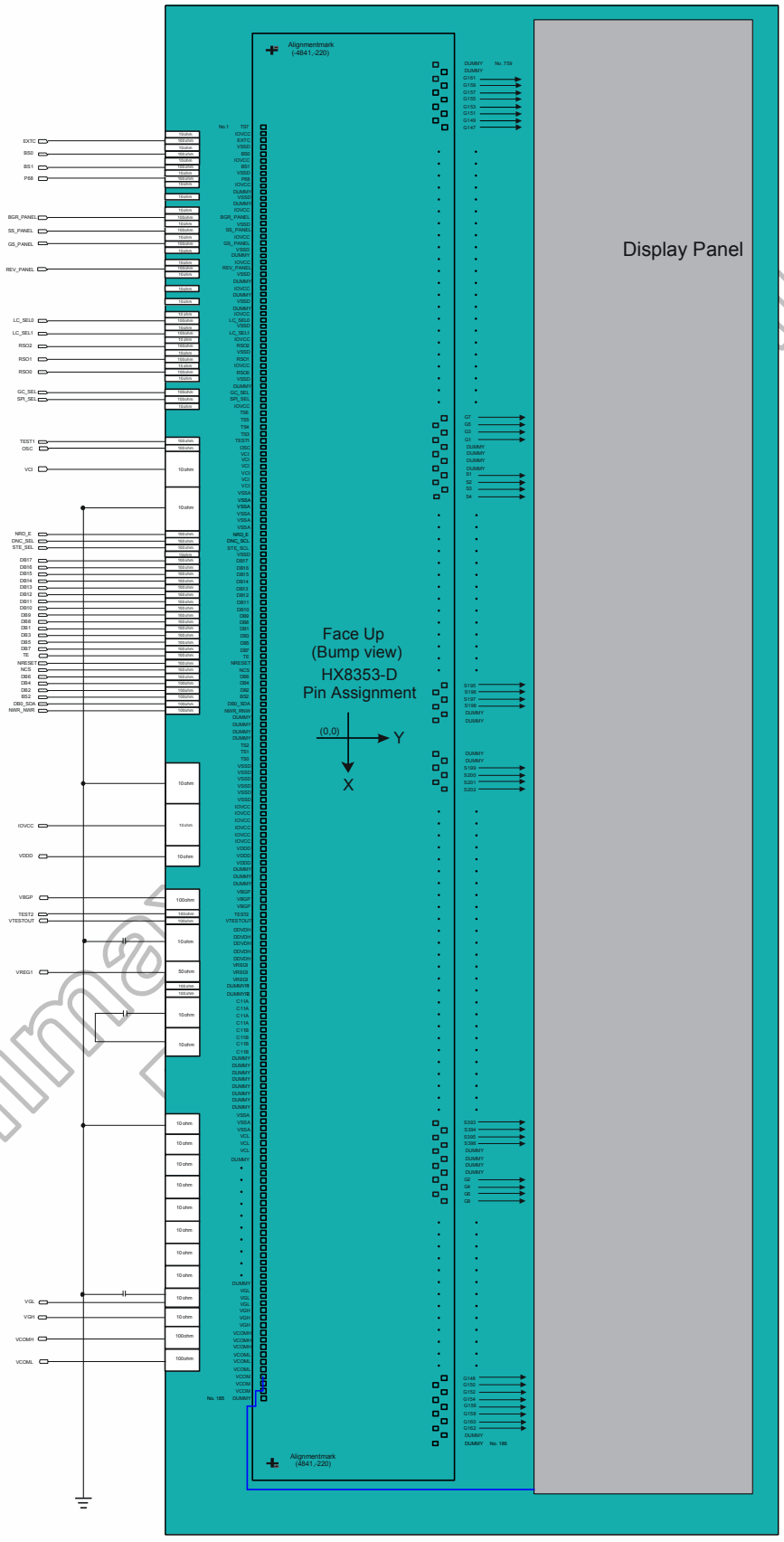


Figure 9.1 Layout recommendation of HX8353-D

Maximum layout resistance

Name	Type	Maximum Series Resistance	Unit
VCI	Power supply	10	Ω
IOVCC	Power supply	10	Ω
VSSA	Power supply	10	Ω
VSSD	Power supply	10	Ω
OSC	Input	100	Ω
EXTC	Input	100	Ω
P68, BS2, BS1, BS0	Input	100	Ω
STE_SEL, GC_SEL, SPI_SEL	Input	100	Ω
RSO0, RSO1, RSO2	Input	100	Ω
LC_SEL0, LC_SEL1	Input	100	Ω
NRESET, NCS, DNC_SCL	Input	100	Ω
NWR_RNW, NRD_E	Input	100	Ω
TEST2, TEST1	Input	100	Ω
SS_PANEL, GS_PANEL, REV_PANEL, BGR_PANEL	Input	100	Ω
DUMMYR1,DUMMYR2,	Input	100	Ω
DB0_SDA, DB17 ~ DB1	Input / Output	100	Ω
VGH	Output	10	Ω
VGL	Output	10	Ω
C11A, C11B	Output	10	Ω
C12A, C12B	Output	10	Ω
C22A, C22B	Output	10	Ω
C21A, C21B	Output	10	Ω
VDDD	Output	10	Ω
DDVDH	Output	10	Ω
VCL	Output	10	Ω
TE	Output	100	Ω
VCOMH, VCOML	Output	100	Ω
VREG1	Output	100	Ω
VBGP	Output	100	Ω
VTESTOUT	Output	100	Ω

Table 9.1 Maximum layout resistance

10. OTP Programming

OTP_INDEX	D7	D6	D5	D4	D3	D2	D1	D0	Non-Program
00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	00h
01h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	00h
02h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	00h
03h	VMF17	VMF16	VMF15	VMF14	VMF13	VMF12	VMF11	VMF10	00h
04h	VMF27	VMF26	VMF25	VMF24	VMF23	VMF22	VMF21	VMF20	00h
05h	VMF37	VMF36	VMF35	VMF34	VMF33	VMF32	VMF31	VMF30	00h
06h	-	-	-	-	-	Valid_VMF3	Valid_VMF2	Valid_VMF1	00h
07h	Valid_ID	-	-	-	-	-	-	-	00h

Table 10.1 OTP address mapping

Note: (1) The default value of OTP memory bits are all "0".

(2) "Valid_ID" bit decide the OTP reload Enable/Disable, the default value is "0". If the OTP index of Valid bit had been programmed, the Valid bit will be changed to "1" automatically and execute the OTP reload.

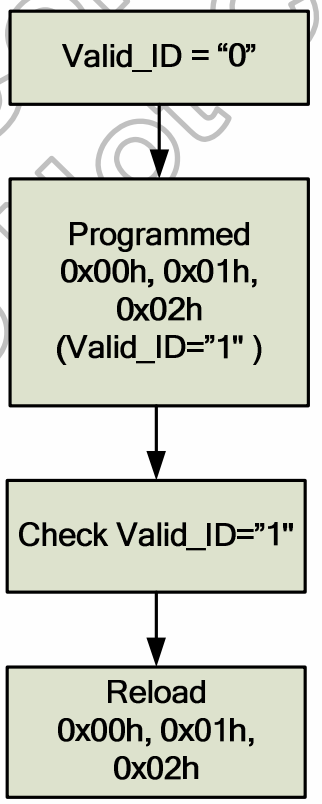
(3) Please set the 00h(ID1) & 01h(ID2) & 02h(ID3) at the same time.

(4) VMF can be programmed three times. When programming index 03h first time, VMF1 and Valid_VMF1 will be programmed automatically. If programming index 03h second time, VMF2 and Valid_VMF2 will be programmed automatically. If programming index 03h third time, VMF3 and Valid_VMF3 will be programmed automatically.

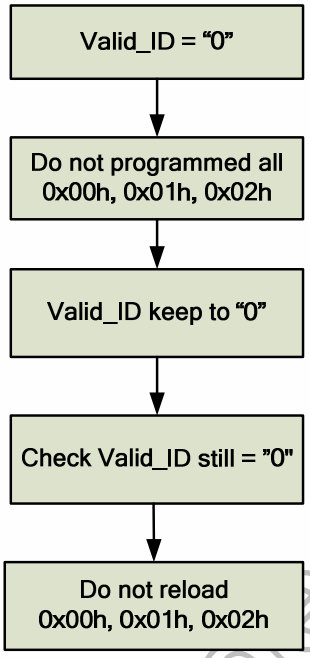
(5) The OTP programming (External 6.5V to VGH) current limit must ≧20mA.

For example:

Condition 1: Programmed all index of 0X00h, 0X01h and 0X02h



Condition 2: Do not program all index of 0X00h, 0X01h and 0X02h

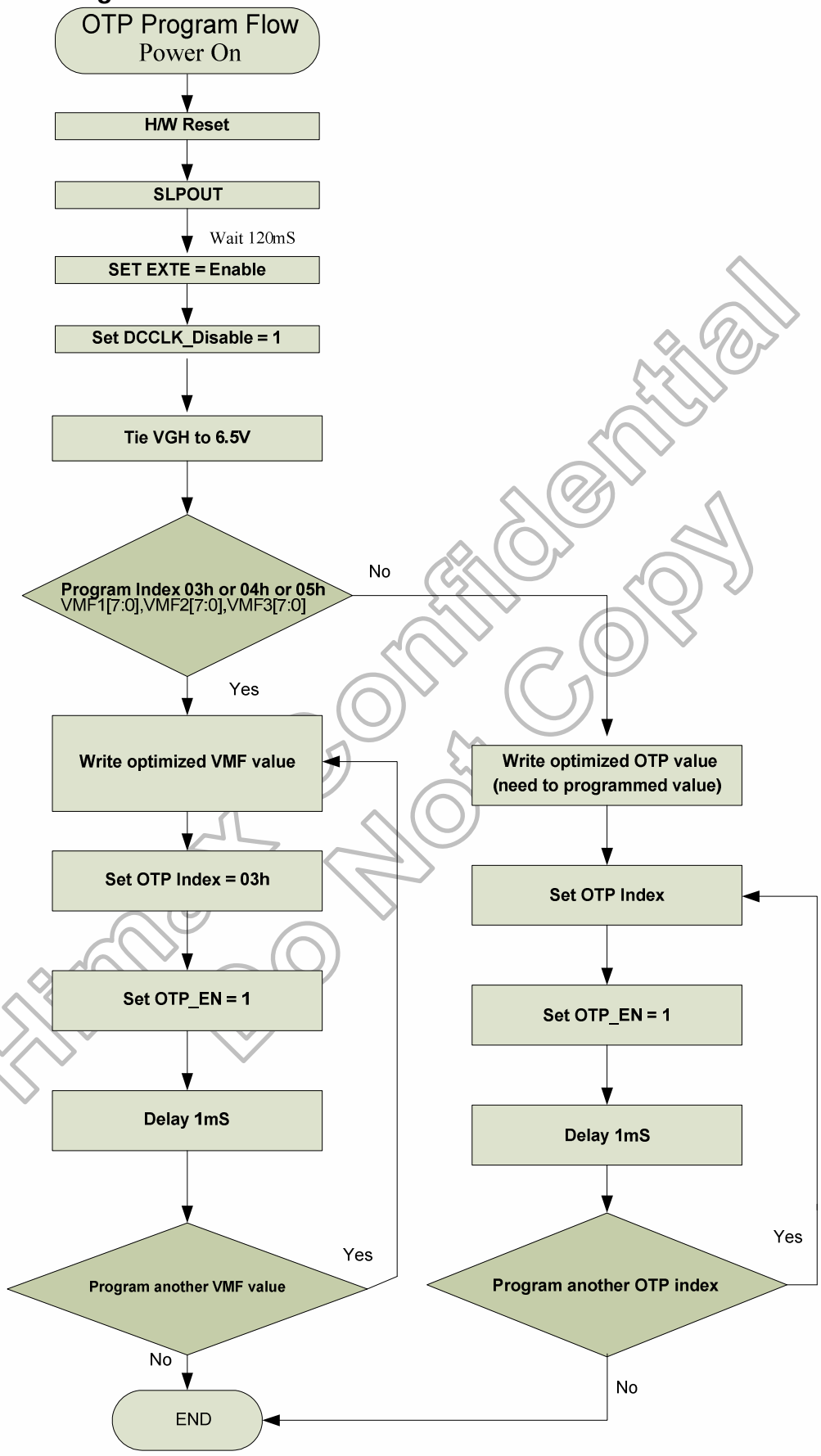


(4) There are some conditions that HX8353-D can reload OTP.
1.Hardware reset
2.Software reset
3.SLPOUT command.

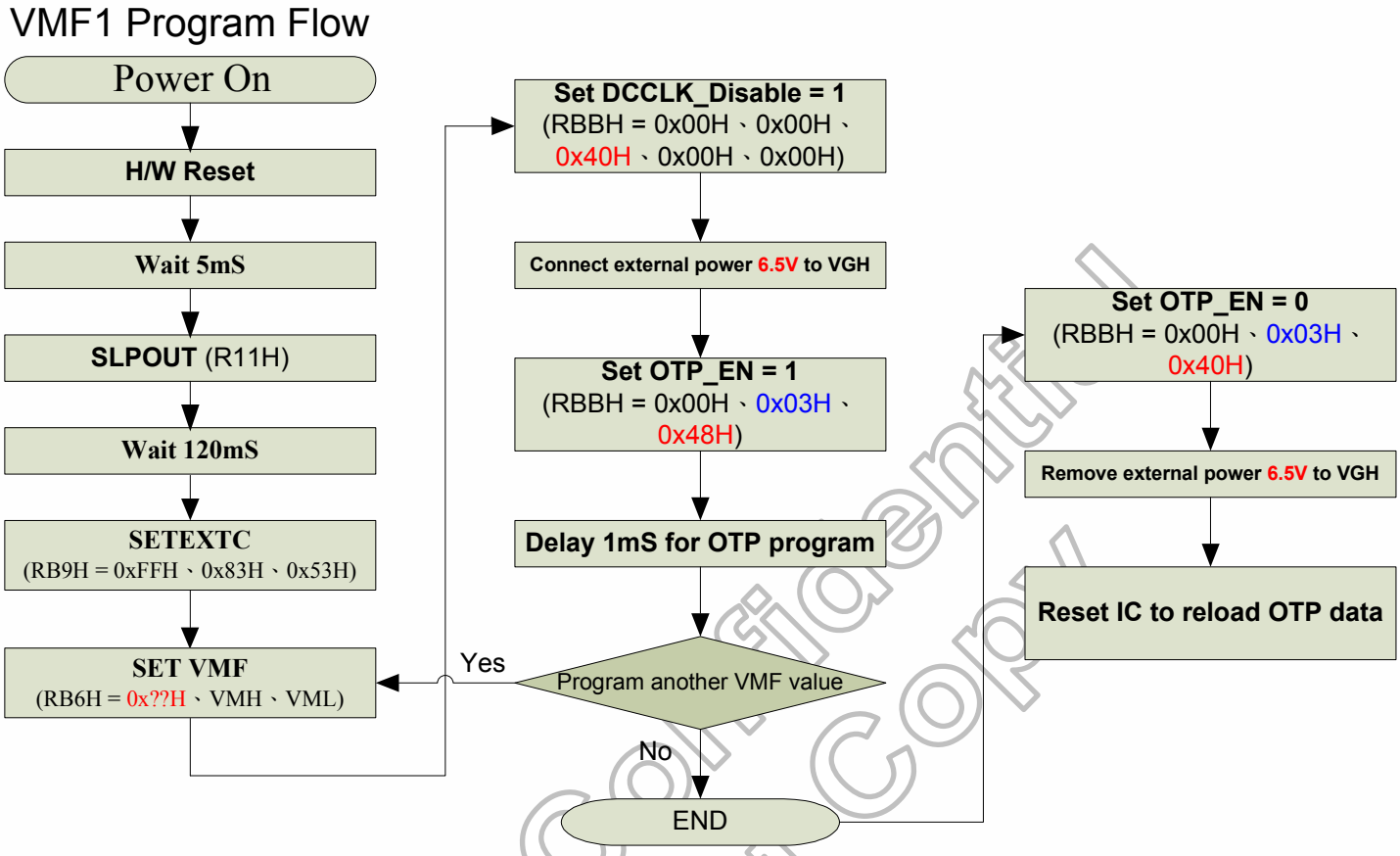
(5) User can use GETOTP command to read back the OTP values. Similarly, the user also can use GETOTP to read the index 0x06h that is defined the VALID bit for VMF1, VMF2 and VMF3 (Valid_VMF1, Valid_VMF2 and Valid_VMF3) to know how many times of VMF had programmed on OTP.

	Valid_VMF3	Valid_VMF2	Valid_VMF1
Programmed 0 time	0	0	0
Programmed 1 time	0	0	1
Programmed 2 times	0	1	1
Programmed 3 times	1	1	1

10.1 Programming flow



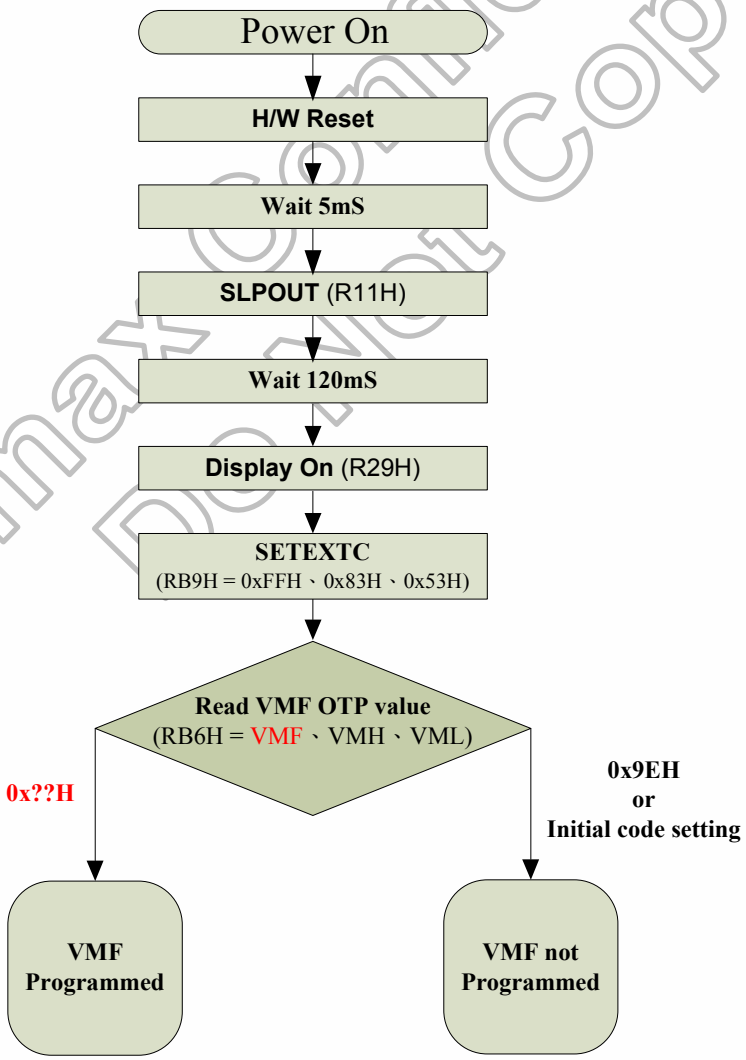
10.2 OTP Programming example for VMF1



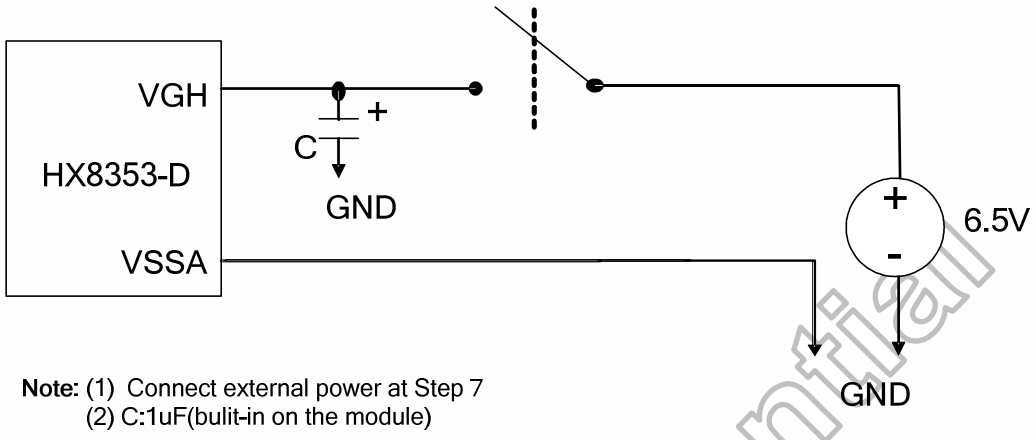
10.3 Programming sequence

Step	Operation
1	Power on and reset the module
2	Set OTP_LOAD_DISABLE=1, disable the auto-loading function.
3	SLPOUT command (11h)
4	Wait 120ms
5	Write optimized value to related register.
6	Set OSC_EN=0, disable internal pumping clock.
7	Connect external power 6.5V to VGH pin
8	Wait 100ms for external power 6.5V to stabilize.
9	Specify OTP_index. Reference OTP address mapping table
10	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
11	Set OTP_EN=1, Internal register begin write to OTP according to OTP_index.
12	Wait 1 ms
13	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (9). Otherwise, power off the module and remove the external power on VGH pin.

10.4 OTP Read flow and example



10.5 Programming circuitry



Note: (1) Connect external power at Step 7
(2) C:1uF(bulit-in on the module)

11. Electrical Characteristic

11.1 Absolute maximum ratings

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~VSSD	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.6	Note(3)
Power Supply Voltage 3	DDVDH ~ VSSA	V	-0.3 to +6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to +4.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3 to +9	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to +18.5	Note(7)
Power Supply Voltage 7	VSSA ~ VGL	V	0 to -16	Note(8)
Logic Input Voltage	V_{IN}	V	-0.3 to IOVCC+0.5	-
Logic Output Voltage	Vo	V	-0.3 to IOVCC+0.5	-
Operating Temperature	Topr	℃	-30 to +80	Note(9),(10)
Storage Temperature	Tstg	℃	-55 to +110	Note(9),(10)

Note: (1) IOVCC, VSSD must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL.
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +80℃.

Table 11.1 Absolute maximum ratings

11.2 ESD protection level

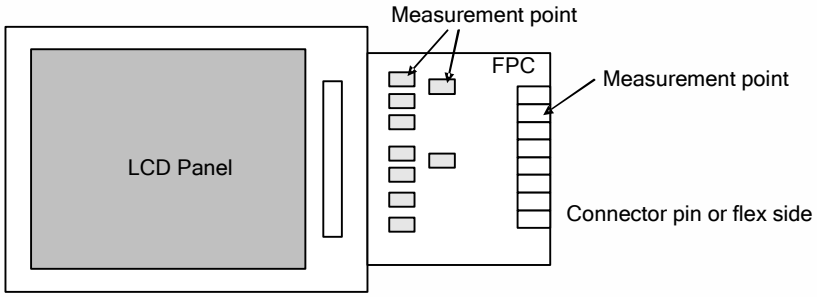
Mode	Test Condition	Protection Level	Unit
Human Body Model	C=100pF, R=1.5kΩ	±2.0K	V
Machine Model	C=200pF, R=0.0Ω	±200	V

Table 11.2 ESD protection level

11.3 DC characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Power & Operating Voltages						
IO Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.3	V
Driver Operating voltage	VCI	Operation voltage	2.5	2.8	3.3	
Source Drive Voltage	VREG1	Dual Pump	3.3	4.65	4.8	
Gate Drive High Voltage	VGH	VCI=2.8 Dual Pump (Typ:BT=000)	-	-	-	
		IVGH=30μA	9.5	10	10.5	
		IVGH=25μA	10.3	10.8	11.3	
		IVGH=20μA	11.25	11.5	11.75	
		IVGH=15μA	11.75	12	12.25	
		IVGH=10μA	12.25	12.5	12.75	
		IVGH=5μA	13	13.25	13.5	
Gate Drive Low Voltage	VGL	VCI=2.8 Dual Pump (Typ:BT=000)	-	-	-	
		IVGL=30μA	-8.05	-8.2	-8.35	
		IVGL=25μA	-8.75	-8.9	-9.05	
		IVGL=20μA	-9.25	-9.4	-9.55	
		IVGL=15μA	-9.75	-9.9	-10.05	
		IVGL=10μA	-10.35	-10.5	-10.65	
		IVGL=5μA	-10.85	-11	-11.15	
Drive Supply Voltage	|VGH-VGL|	-	-	-	30	
Input / Output						
High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V
Low level input voltage	VIL	-	VSSD	-	0.3*IOVCC	
High level output voltage	VOH	IOH = -1.0mA	0.8*IOVCC	-	IOVCC	
Low level output voltage	VOL	IOL = +1.0mA	VSSD	-	0.2*IOVCC	
Input leakage current	IIL	-	-1	-	1	μA
Oscillator frequency	fOSC	Frame rate at 75hz,default Vs and Hs setting T_A=25℃	1.387	1.46	1.533	MHz
Booster (VCI=2.8V)						
DDVDH boost voltage1	DDVDH	Dual Pump IDDVDH=300μA	4.8	5.0	5.2	V
VCL boost voltage	VCL	ICL=-100μA	-2.5	-2.65	2.75	
VCOM Generator (VCI=2.8V)						
VCOM amplitude	VCOM	No load, Dual Pump	2.5	4.4	7.3	V
VCOM high level	VCOMH	No load, Dual Pump	2.5	3.205	4.8	V
VCOM low level	VCOML	No load	-2.5	-1.195	VSSD	V
Source Driver (Typ:T_A=25℃ VCI=2.8V)						
Output voltage deviation (mean value)	DVOS	VSSD+1.0 ~ VREG1-1.0	-	+/- 10	+/- 20	mV
		VSSD+0.1V ~ VSSD+1.0 VREG1-1.0 ~ VREG1-0.1V	-	+/- 30	+/- 50	mV
Output voltage range	VOS	-	0.1	-	DDVDH-0.1	V
Output offset voltage	Voff	-		+/-30	+/-50	mV

Note: VREG1/VCOMH/VCOML conditions: When Internal Voltage VREF=4.8V for dual pump



11.3.1 Current consumption

Host I/F	Mode of operation	Frame Frequency	Inversion Mode	Image	Memory Data Access Control (MY:MX:MV)	Current consumption			
						Typical		Worst case	
						VCI (mA)	IOVCC (uA)	VCI (mA)	IOVCC(uA)
Host interface NOT active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	1-line	Black	X;X;X	1.2	2.5	1.48	3
			1-line	1x1 checker board	X;X;X	1.17	2.5	1.45	3
			1-line	4x4 checker board	X;X;X	1.25	2.5	1.46	3
			1-line	Grayscale Top to Bottom	X;X;X	1.18	2.5	1.4	3
			1-line	20B80W	X;X;X	1.14	2.5	1.3	3
	- Normal Mode On - Partial Mode Off - Idle Mode On - Sleep Out Mode	60Hz	1-line	20B80W	X;X;X	0.67	2.5	0.77	3
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode Off - Sleep Out Mode	60Hz	1-line	Grey Levels	X;X;X	0.72	2.5	0.82	3
	- Normal Mode Off - Partial Mode On (32 lines) - Idle Mode On - Sleep Out Mode	60Hz	1-line	8x8 checker board	X;X;X	0.52	2.5	0.58	3
			1-line	Worst pattern	X;X;X	0.55	2.5	0.62	3
	- Sleep In Mode	N/A	N/A	N/A	X;X;X	2µA	2.5	80µA	10
	- Deep Sleep In Mode	N/A	N/A	N/A	X;X;X	0.1µA	0.1	1µA	1
Host interface active	- Normal Mode On - Partial Mode Off - Idle Mode Off - Sleep Out Mode	60Hz	1-line	262k Colors Worst pattern CPU Access @ 15fps	0;0;0	1.28	3	1.5	7
					0;0;1	1.28	3	1.5	7
					0;1;0	1.28	3	1.5	7
					0;1;1	1.28	3	1.5	7
					1;0;0	1.28	3	1.5	7
					1;0;1	1.28	3	1.5	7
					1;1;0	1.28	3	1.5	7
					1;1;1	1.28	3	1.5	7
				262k Colors Worst pattern CPU Access @ 25fps	0;0;0	1.3	3	1.55	12
					0;0;1	1.3	3	1.55	12
					0;1;0	1.3	3	1.55	12
					0;1;1	1.3	3	1.55	12
					1;0;0	1.3	3	1.55	12
					1;0;1	1.3	3	1.55	12
					1;1;0	1.3	3	1.55	12
					1;1;1	1.3	3	1.55	12

Table 11.3 Current consumption

Typical Case:
T_A = 25°C
IOVCC=1.8V
VCI = 2.8V

Worst Case:
T_A = -30 to80°C
IOVCC = 1.65V to 1.95V
VCI = 2.5V to 3.3V
Includes Process Variance.

11.4 AC characteristics

11.4.1 Parallel interface characteristics (8080-series MPU)

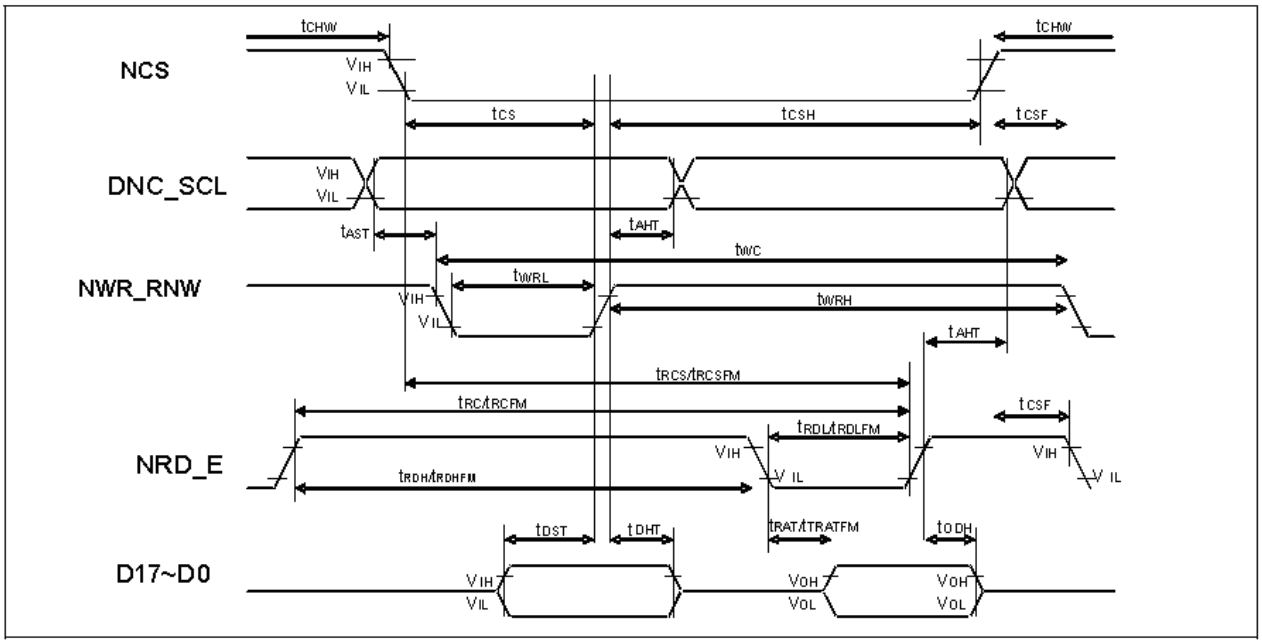


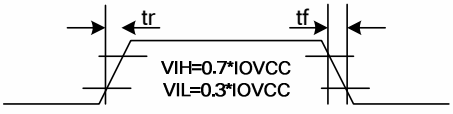
Figure 11.1 Parallel interface characteristics (8080-series MPU)

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3 V, T_A = -30 to 70℃)

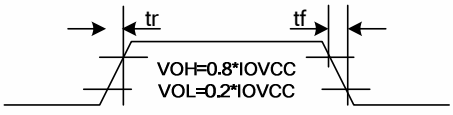
Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NCS	t_{CHW}	Chip select "H" pulse width	0	-	ns	-
	t_{CS}	Chip select setup time (Write)	15	-		
	t_{RCS}	Chip select setup time (Read ID)	45	-		
	t_{RCSFM}	Chip select setup time (Read FM)	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
	t_{CSH}	Chip select hold time	10	-		
NWR_SCL	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse "H" duration	15	-		
	t_{WRL}	Control pulse "L" duration	15	-		
NRD_E (ID)	t_{RC}	Read cycle (ID)	160	-	ns	When read ID data
	t_{RDH}	Control pulse "H" duration (ID)	90	-		
	t_{RDL}	Control pulse "L" duration (ID)	45	-		
NRD_E (FM)	t_{RCFM}	Read cycle (FM)	450	-	ns	When read from frame memory
	t_{RDHFM}	Control pulse "H" duration (FM)	90	-		
	t_{RDLFM}	Control pulse "L" duration (FM)	355	-		
D17 to D0	t_{DST}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DHT}	Data hold time	10	-		
	t_{RAT}	Read access time (ID)	-	40		
	t_{RATFM}	Read access time (FM)	-	340		
	t_{ODH}	Output disable time	20	80		

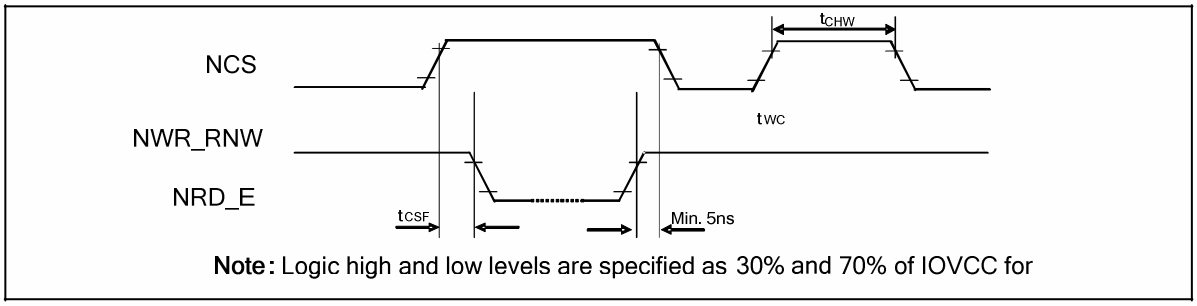
Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



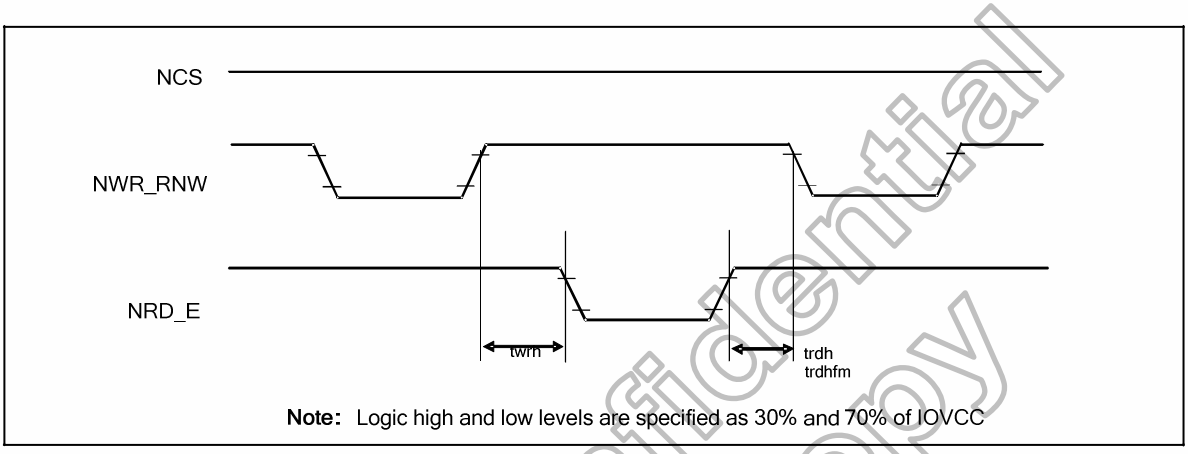
Output Signal Slope





Note: Logic high and low levels are specified as 30% and 70% of IOVCC for

Figure 11.2 Chip select timing



Note: Logic high and low levels are specified as 30% and 70% of IOVCC

Figure 11.3 Write to read and read to write timing

11.4.2 Serial interface characteristics

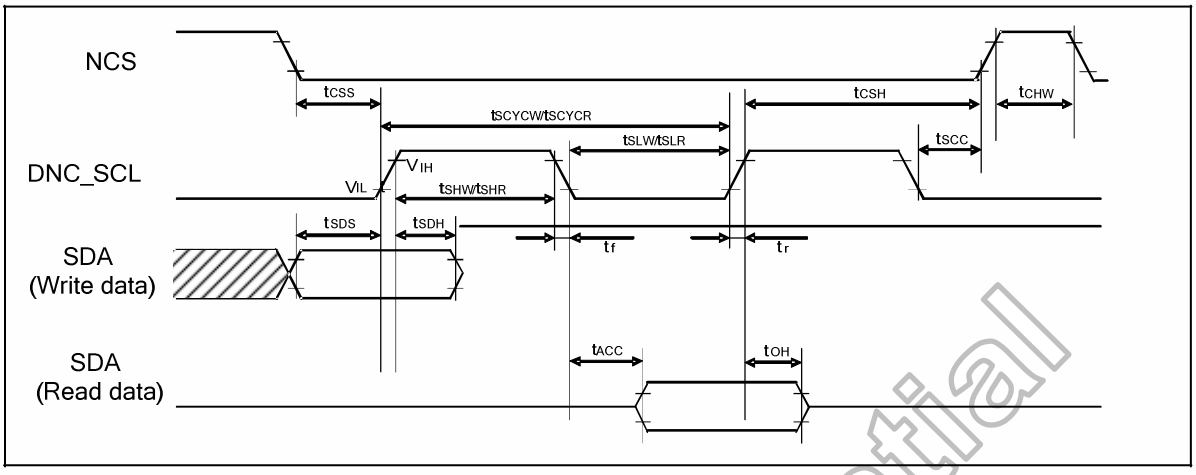


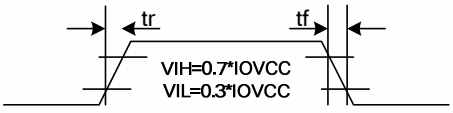
Figure 11.4 Serial interface characteristics

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3 V, T_A= -30 to 70°C)

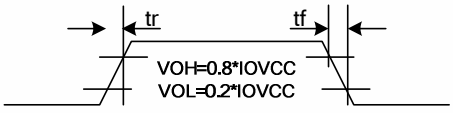
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial clock cycle (Write) DNC_SCL "H" pulse width (Write) DNC_SCL "L" pulse width (Write)	tSCYCW tSHW tSLW	DNC_SCL	66 15 15	-	- - -	ns
Data setup time (Write) Data hold time (Write)	tSDS tSDH	SDA	10 10	-	- -	ns
Serial clock cycle (Read) DNC_SCL "H" pulse width (Read) DNC_SCL "L" pulse width (Read)	tSCYCR tSHR tSLR	DNC_SCL	150 60 60	-	- - -	ns
Access Time	tACC	SDI for maximum CL=30pF For minimum CL=8pF	10	-	50	ns
Output disable time	tOH	SDO For maximum CL=30pF For minimum CL=8pF	15	-	50	ns
DNC_SCL to Chip select	tSCC	DNC_SCL, NCS	15	-	-	ns
NCS "H" pulse width	tCHW	NCS	40	-	-	ns
Chip select setup time Chip select hold time	tCSS tCSH	NCS	60 65	-	- -	ns

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Input Signal Slope



Output Signal Slope



11.4.3 Reset input timing

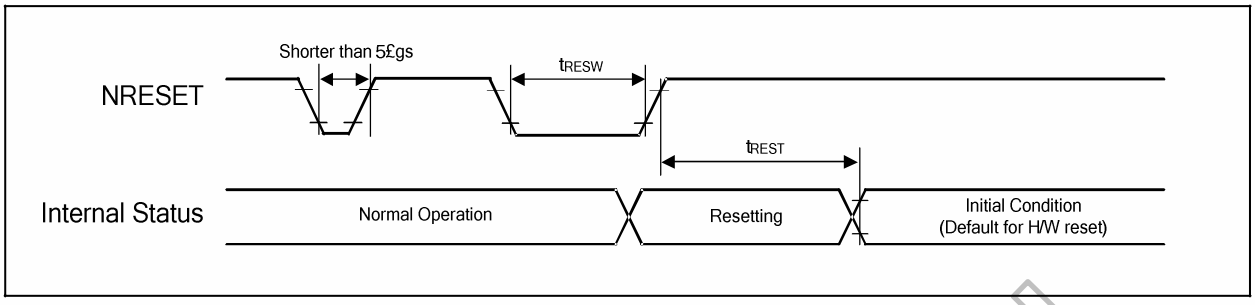


Figure 11.5 Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during Sleep In mode	ms
		-	-	-	120	When reset applied during Sleep Out mode	ms

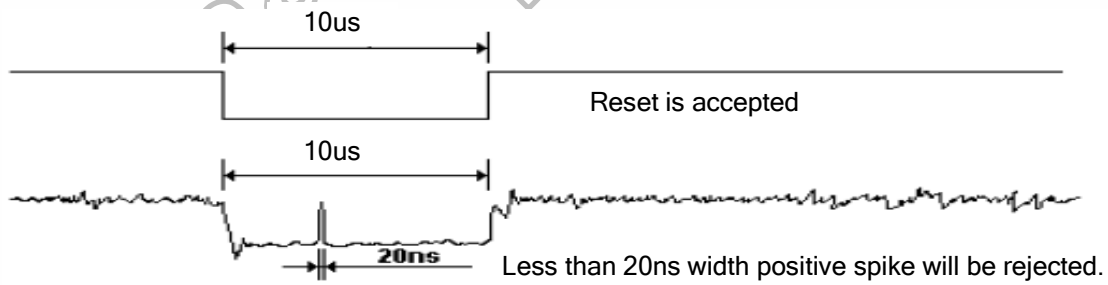
Note: (1) Spike due to an electrostatic discharge on !RES line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 and VCOMOF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.

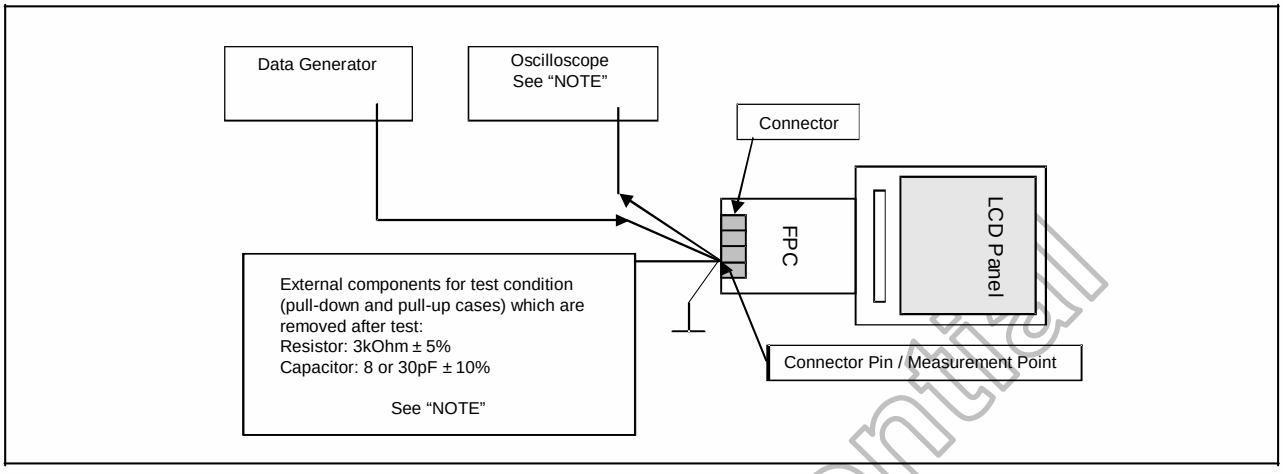
(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

11.5 tACC, tOH Measurement Condition

Measurement condition set-up



Note: Capacitances and resistances of the oscilloscope's probe must be included externals components in these measurements

Figure 11.6 tACC and tOH measurement condition set-up

Minimum value measurement

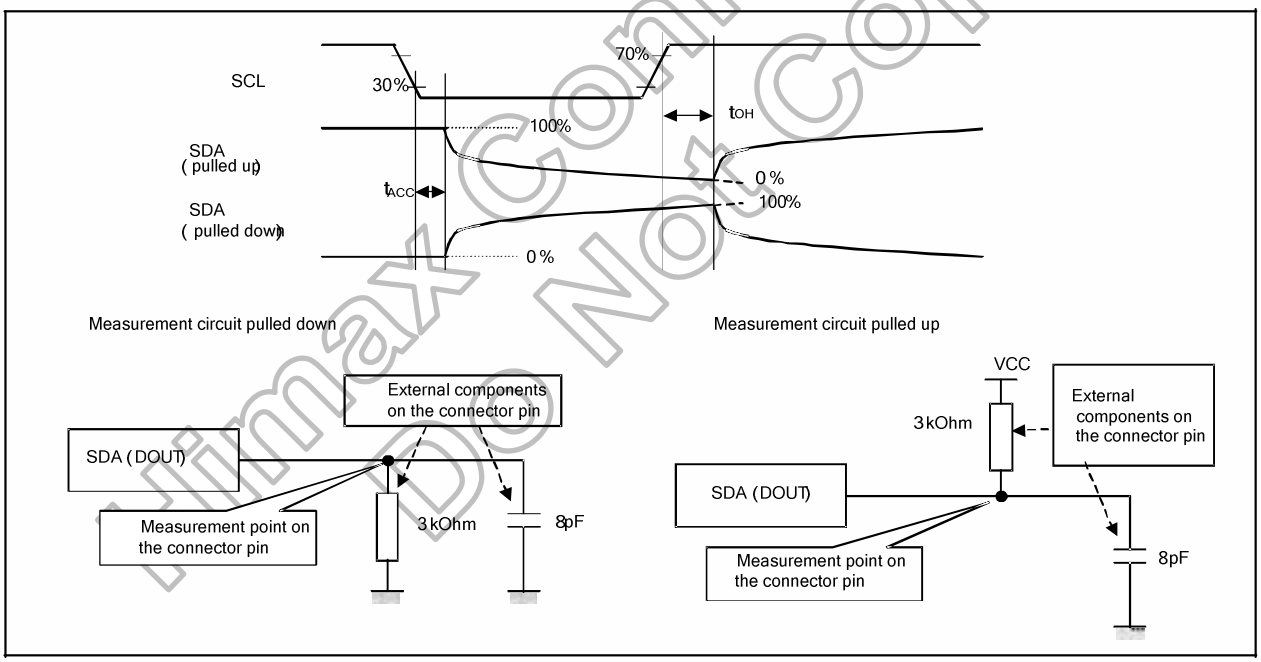


Figure 11.7 tACC and tOH minimum value measurement

Maximum value measurement

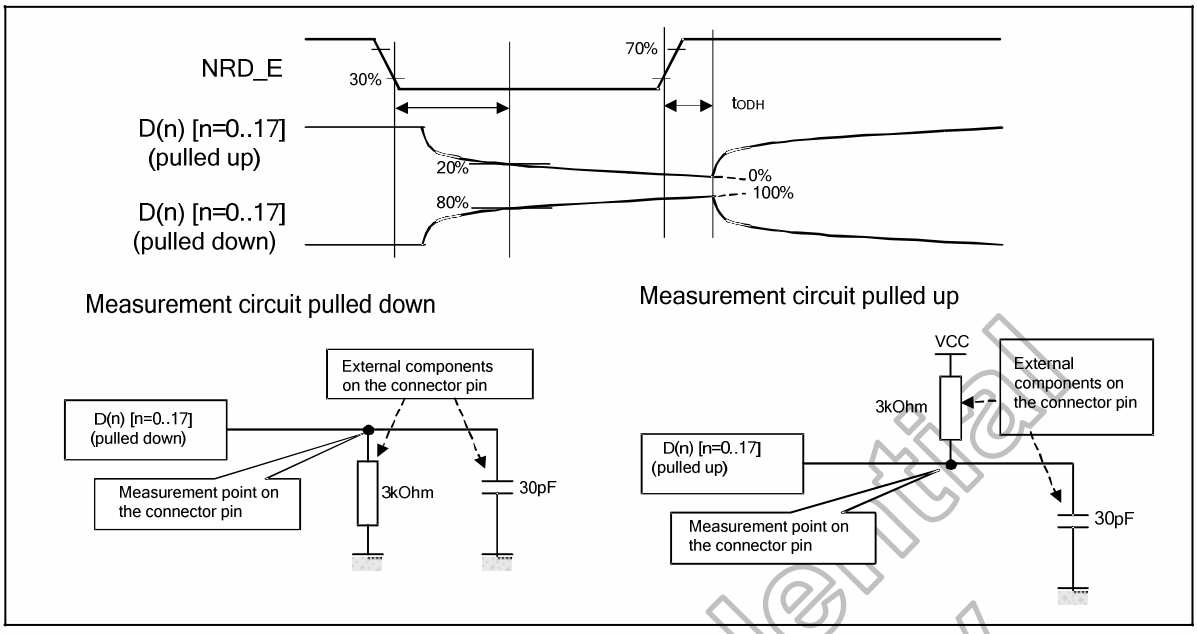
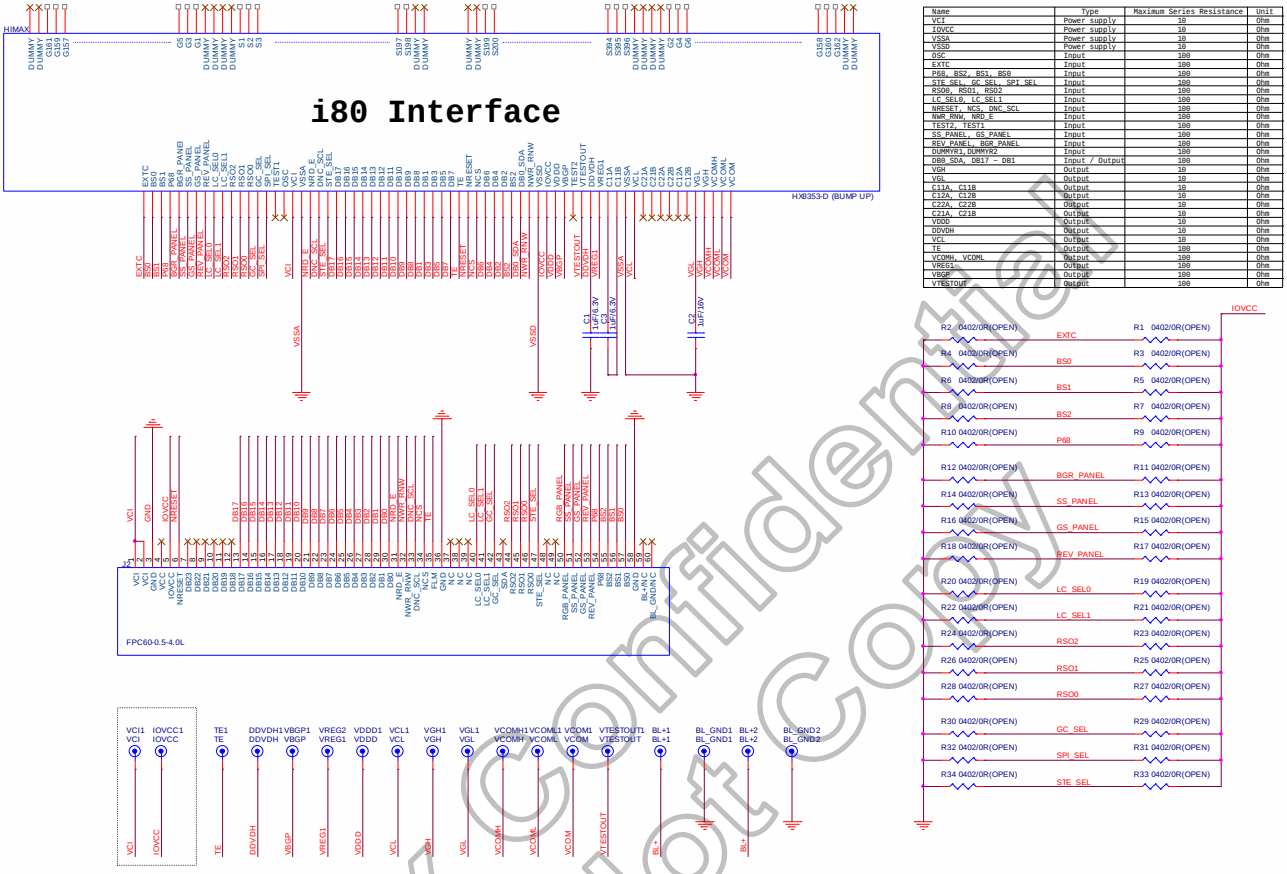


Figure 11.8 tACC and tOH maximum value measurement

12. Reference Application

12.1 I80 system



Name	Type	Maximum Series Resistance	Unit
VCI	Power supply	10	Ohm
IOVCC	Power supply	10	Ohm
VSSA	Power supply	10	Ohm
VSSD	Power supply	10	Ohm
OSC	Input	100	Ohm
EXTC	Input	100	Ohm
P68, BS2, BS1, BS0	Input	100	Ohm
STE_SEL, GC_SEL, SPI_SEL	Input	100	Ohm
RSO0, RSO1, RSO2	Input	100	Ohm
LC_SEL0, LC_SEL1	Input	100	Ohm
NRESET, NCS, DNC_SCL	Input	100	Ohm
NWR_RNW, NRD_E	Input	100	Ohm
TEST2, TEST1	Input	100	Ohm
SS_PANEL, GS_PANEL	Input	100	Ohm
REV_PANEL, BGR_PANEL	Input	100	Ohm
DUMMYR1,DUMMYR2	Input	100	Ohm
DB0_SDA, DB17 ~ DB1	Input / Output	100	Ohm
VGH	Output	10	Ohm
VGL	Output	10	Ohm
C11A, C11B	Output	10	Ohm
C12A, C12B	Output	10	Ohm
C22A, C22B	Output	10	Ohm
C21A, C21B	Output	10	Ohm
VDDD	Output	10	Ohm
DDVDH	Output	10	Ohm
VCL	Output	10	Ohm
TE	Output	100	Ohm
VCOMH, VCOML	Output	100	Ohm
VREG1	Output	100	Ohm
VREGP	Output	100	Ohm
VTESTOUT	Output	100	Ohm

P68	BS2	BS1	BS0	Interface mode
0	1	0	0	I80 MCU 8-bits Parallel Bus
0	1	0	1	I80 MCU 16-bits Parallel Bus
0	1	1	0	I80 MCU 9-bits Parallel Bus
0	1	1	1	I80 MCU 18-bits Parallel Bus
1	1	0	0	M68 MCU 8-bits Parallel Bus
1	1	0	1	M68 MCU 16-bits Parallel Bus
1	1	1	0	M68 MCU 9-bits Parallel Bus
1	1	1	1	M68 MCU 18-bits Parallel Bus
X	0	X	X	3W/4W Serial Interface

RSO2	RSO1	RSO0	STE_SEL	GRAM Resolution
0	0	0	0	132RGB X 162 (Display 132RGB X 162)
0	0	0	1	132RGB X 162 (Display 128RGB X 160)
0	0	1	X	128RGB X 128 (Display 128RGB X 128)
0	1	0	X	120RGB X 160(Display 120RGB X 160)
0	1	1	X	128RGB X 160(Display 128RGB X 160)
1	0	0	X	96RGB X 68(Display 96RGB X 68)
1	0	1	X	96RGB X 64(Display 96RGB X 64)

	0	1
BGR_PANEL	R -> G -> B	B -> G -> R
SS_PANEL	S1 -> S396	S396 -> S1
GS_PANEL	G1 -> G162	G162 -> G1
REV_PANEL	Normally White Panel	Normally Black Panel

Note: SS_PANEL and GS_PANEL is base on RSO[2:0]="000", other RSO[2:0] setting please reference "Pin Description"

Figure 12.1 80-/68- system FPC reference circuit

12.2 SPI system

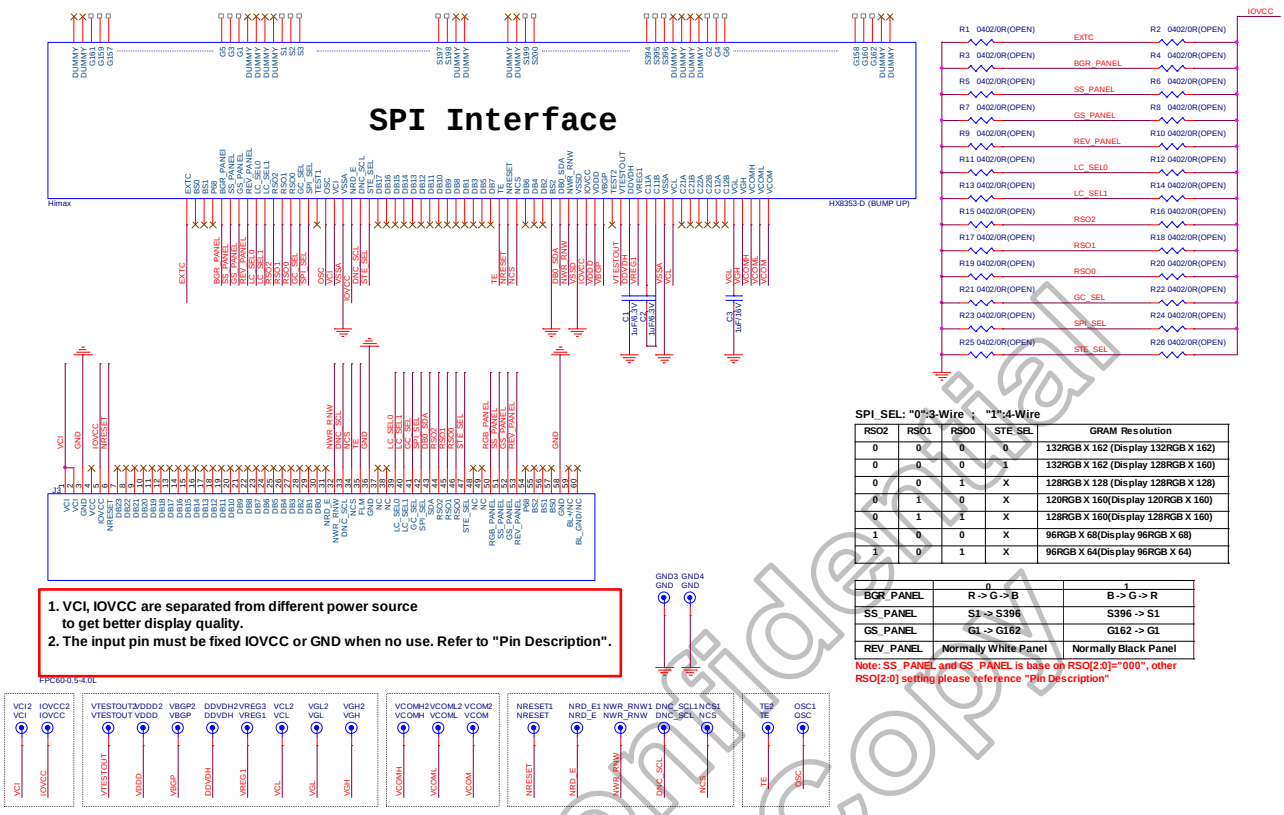
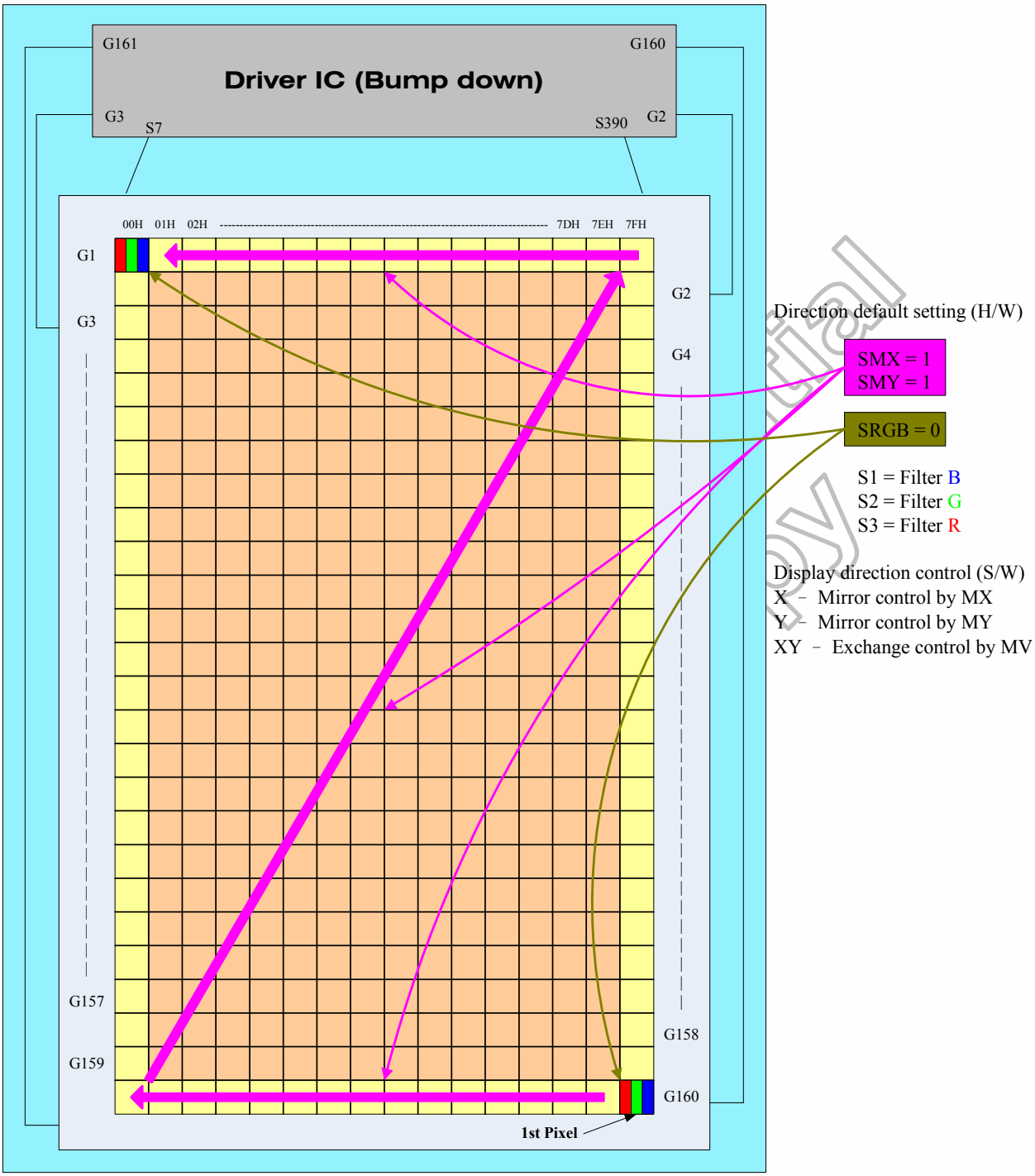
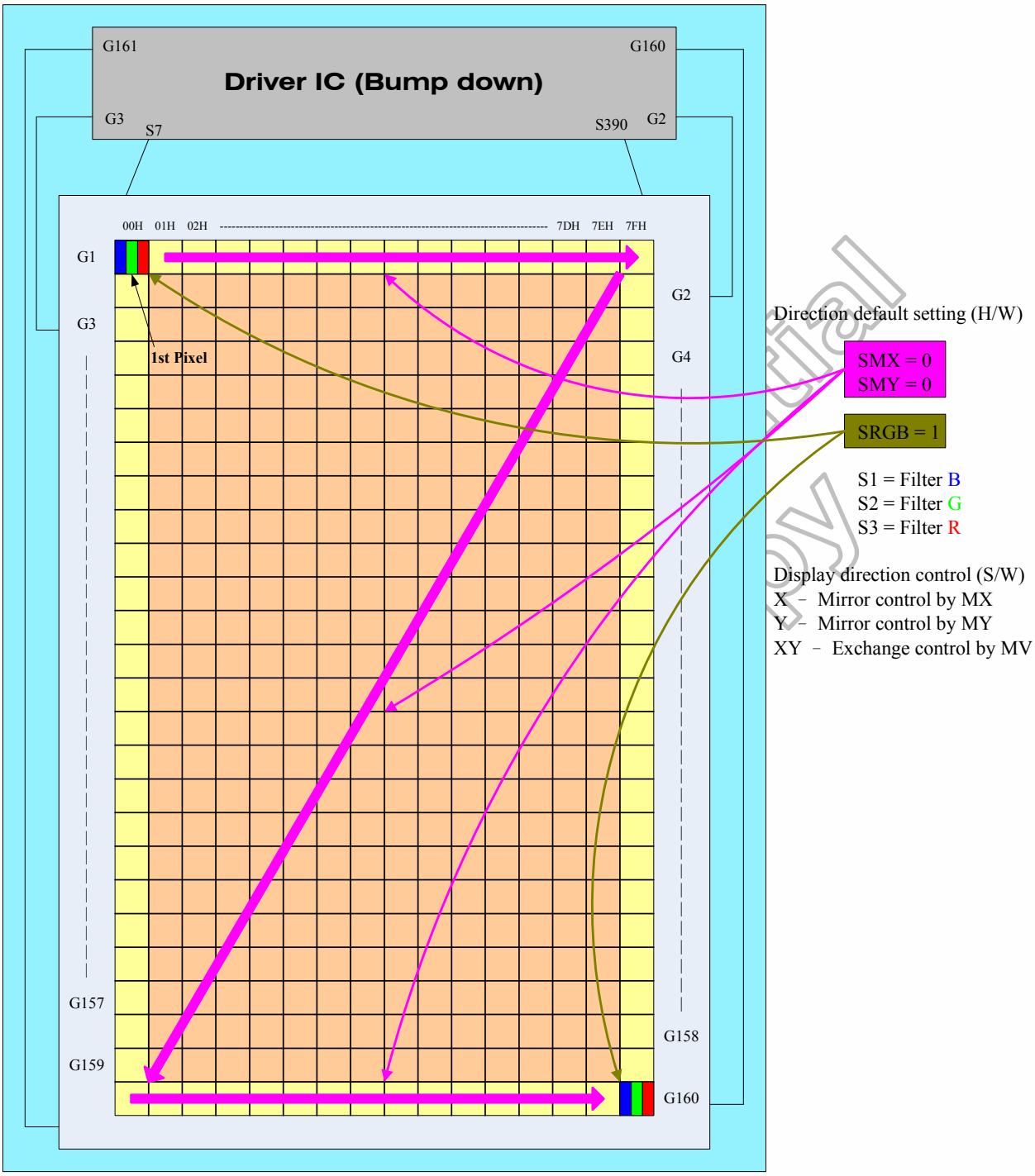


Figure 12.2 SPI FPC reference circuit

12.3 1st Pixel is at right-bottom of the panel & RGB filter order = RGB



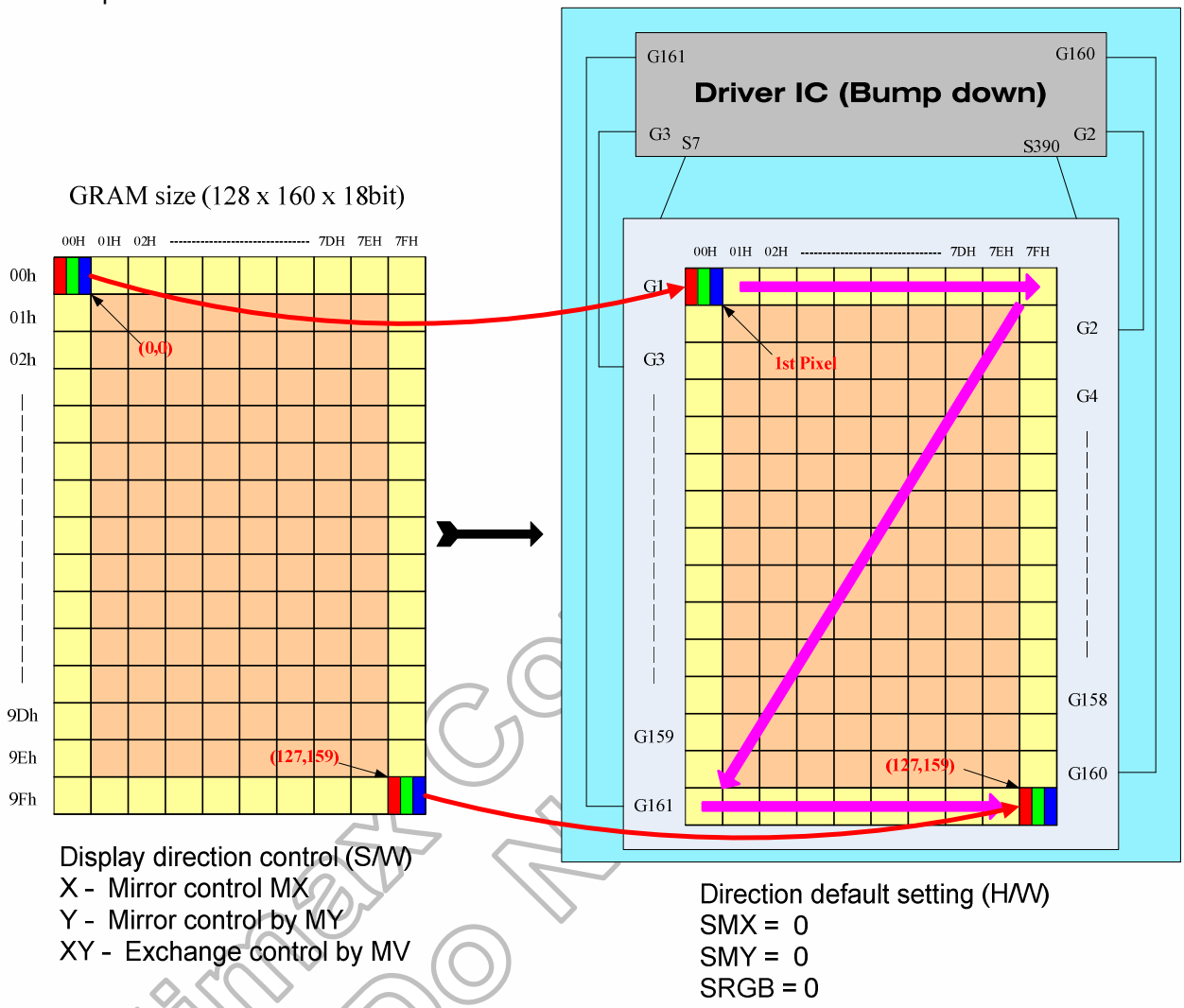
12.4 1st Pixel is at left-top of the panel & RGB filter order = BGR



12.5 Application of connection with Different resolution

Case 1 of resolution (128RGB x 160) (RSO[2:0] = 011) RAM size = 128 x 160 x 18-bits (Used)
Display size = 128RGB x 160

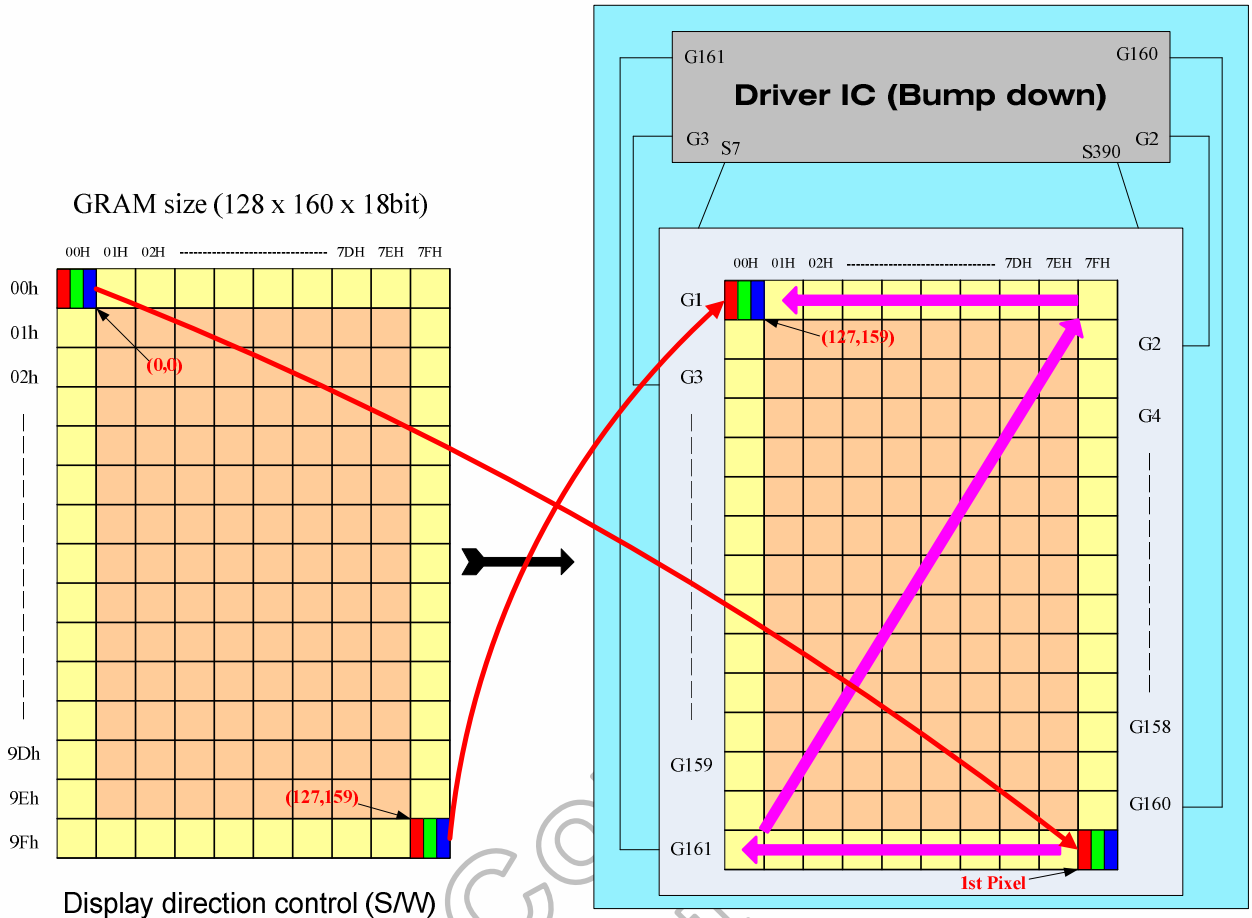
Example for SMX = SMY = 0



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Example for SMX = SMY = 1

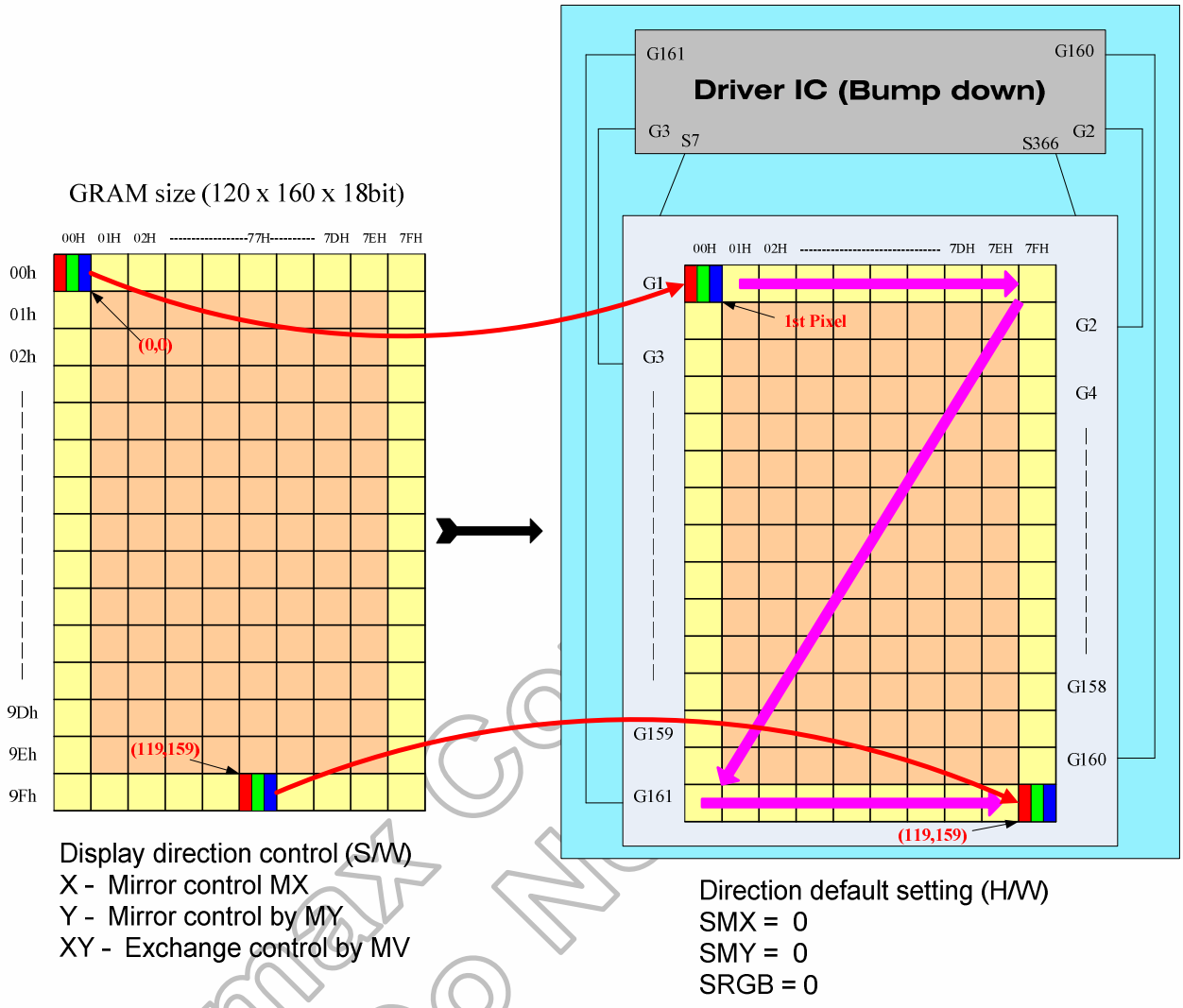


Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

Case 2 of resolution (120RGB x 160) (RSO[2:0] = 010) RAM size = 120 x 160 x 18-bits (Used)
Display size = 120RGB x 160

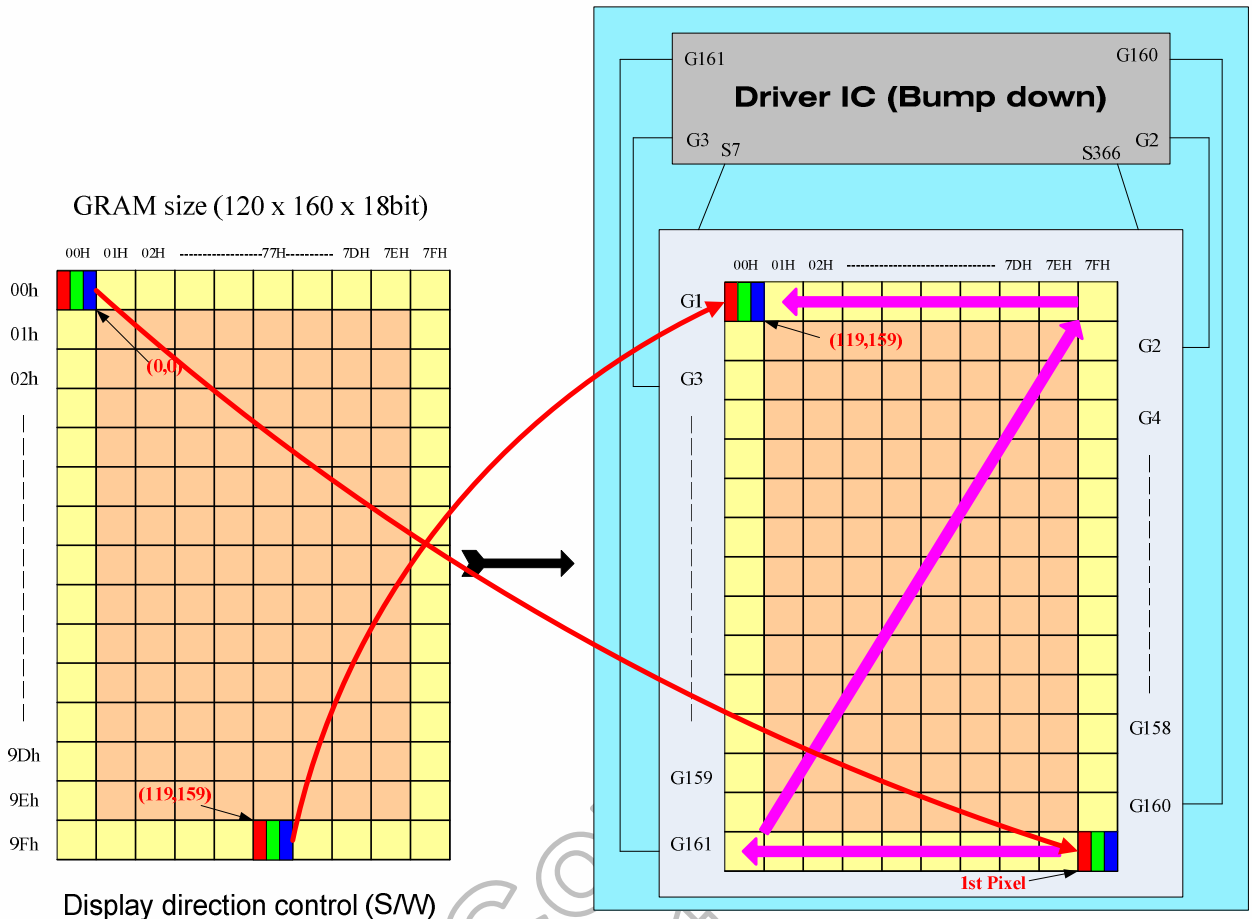
Example for SMX = SMY = 0



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Example for SMX = SMY = 1

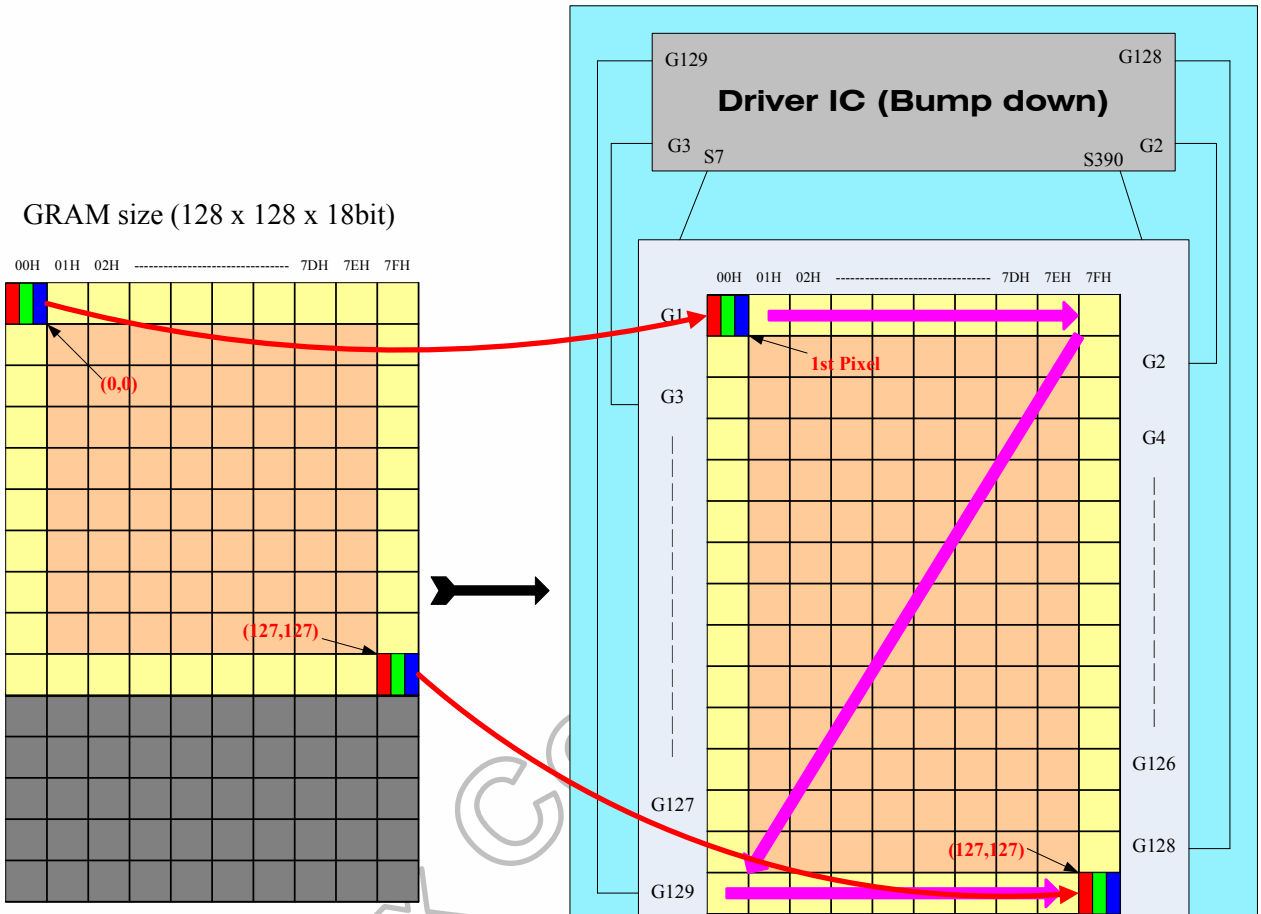


Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

Case 3 of resolution (128RGB x 128) (RSO[2:0] = 001) RAM size = 128 x 128 x 18-bits (Used)
Display size = 128RGB x 128

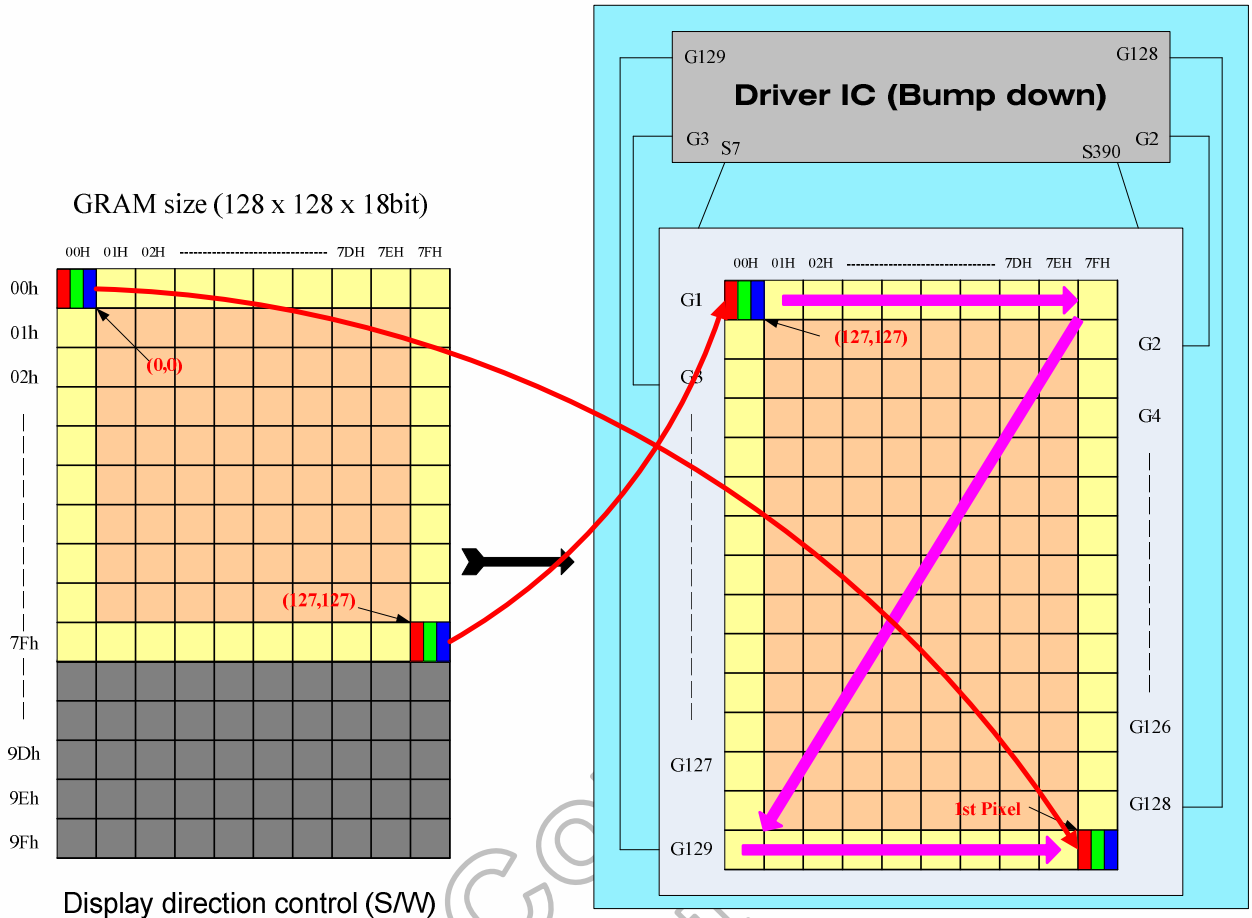
Example for SMX = SMY = 0



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Example for SMX = SMY = 1

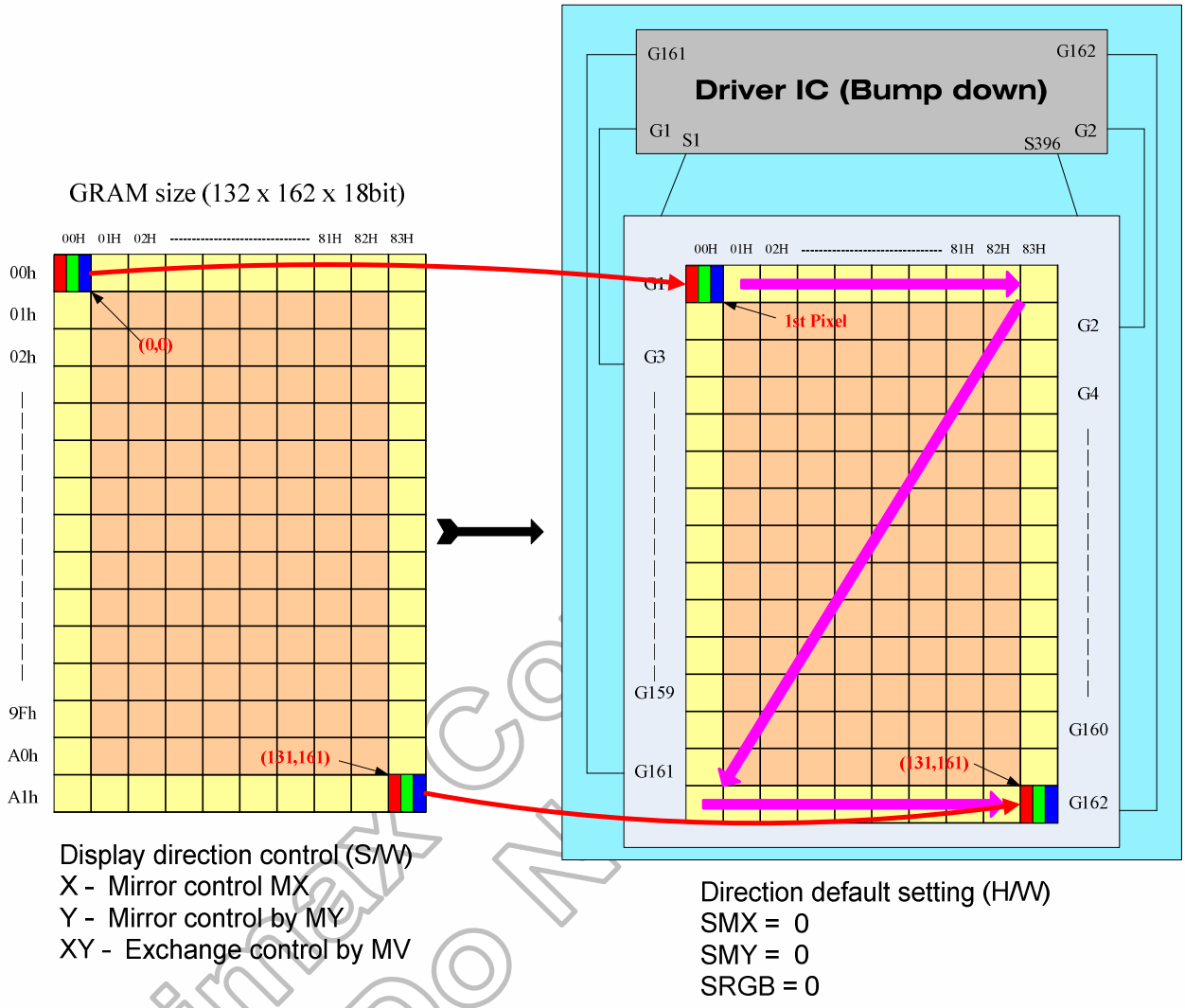


Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

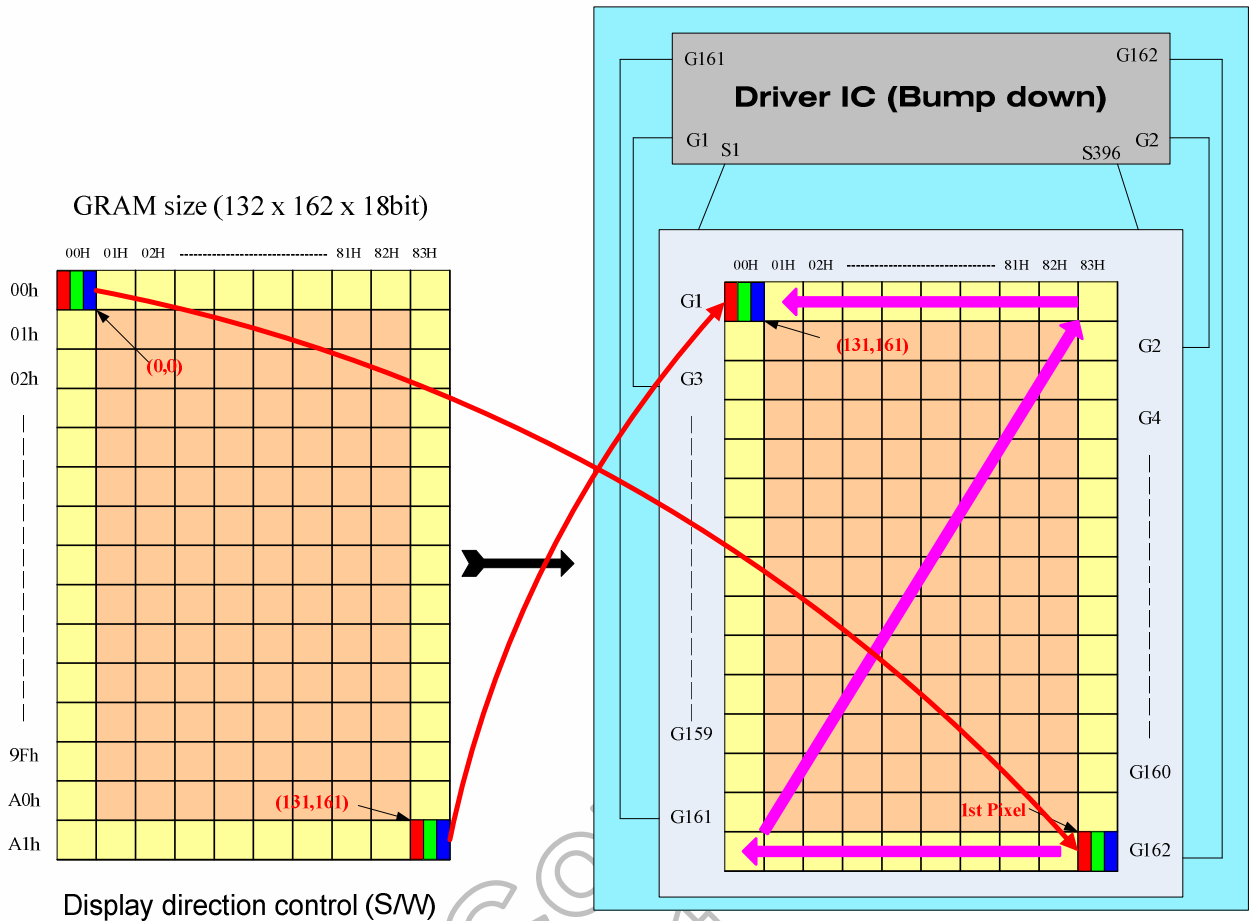
Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

Case 4 of resolution (132RGB x 162) (RSO[2:0] = 000) RAM size = 132 x 162 x 18-bits (Used)
Display size = 132RGB x 162 ~ Type 1
(P.S : STE_SEL = 0 ➔ Type1 ; STE_SEL = 1 ➔ Type 2)

Example for SMX = SMY = 0



Example for SMX = SMY = 1

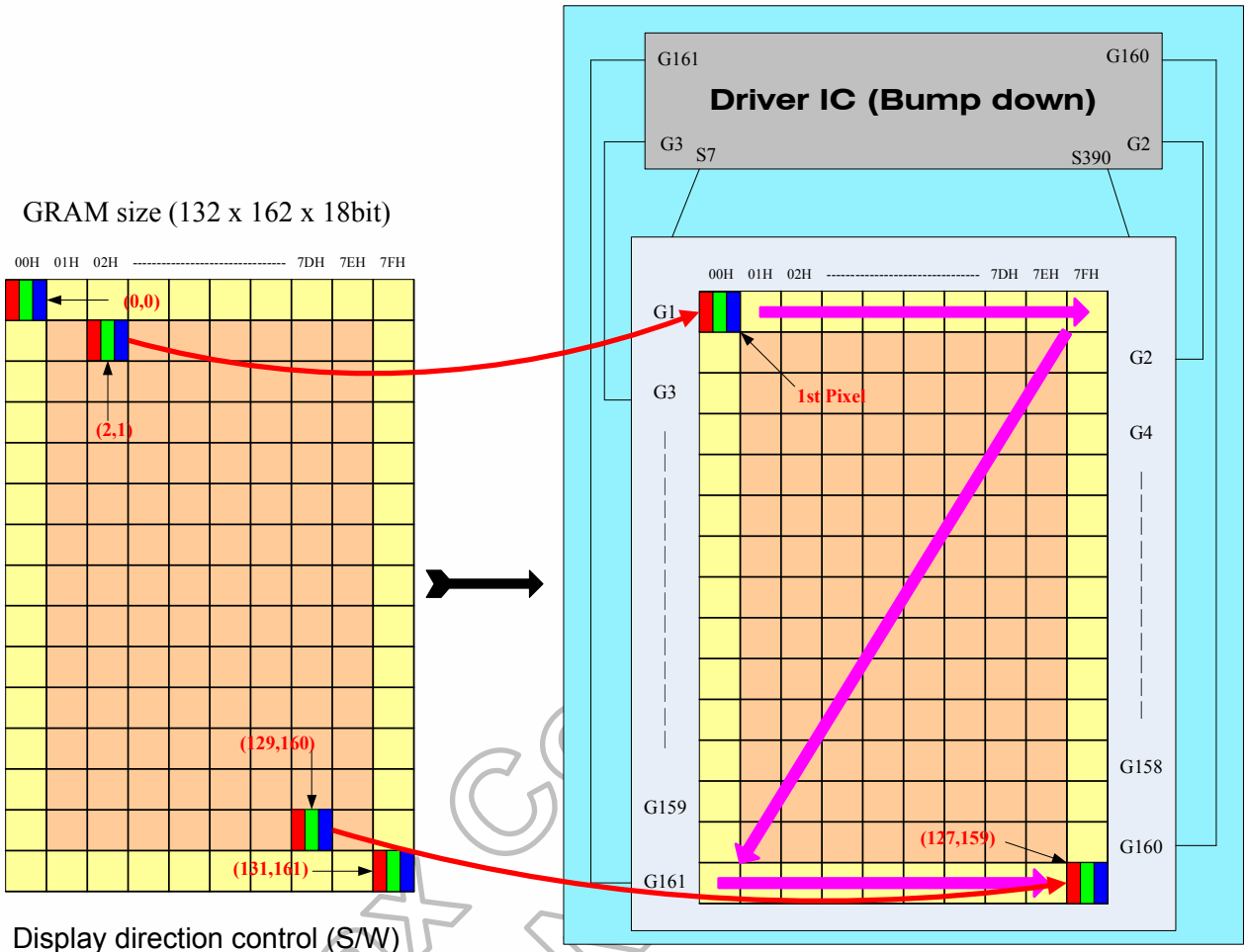


Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

Display size = 132RGB x 162 ~ Type 2
(P.S : STE_SEL = 0 ➔ Type1 ; STE_SEL = 1 ➔ Type 2)

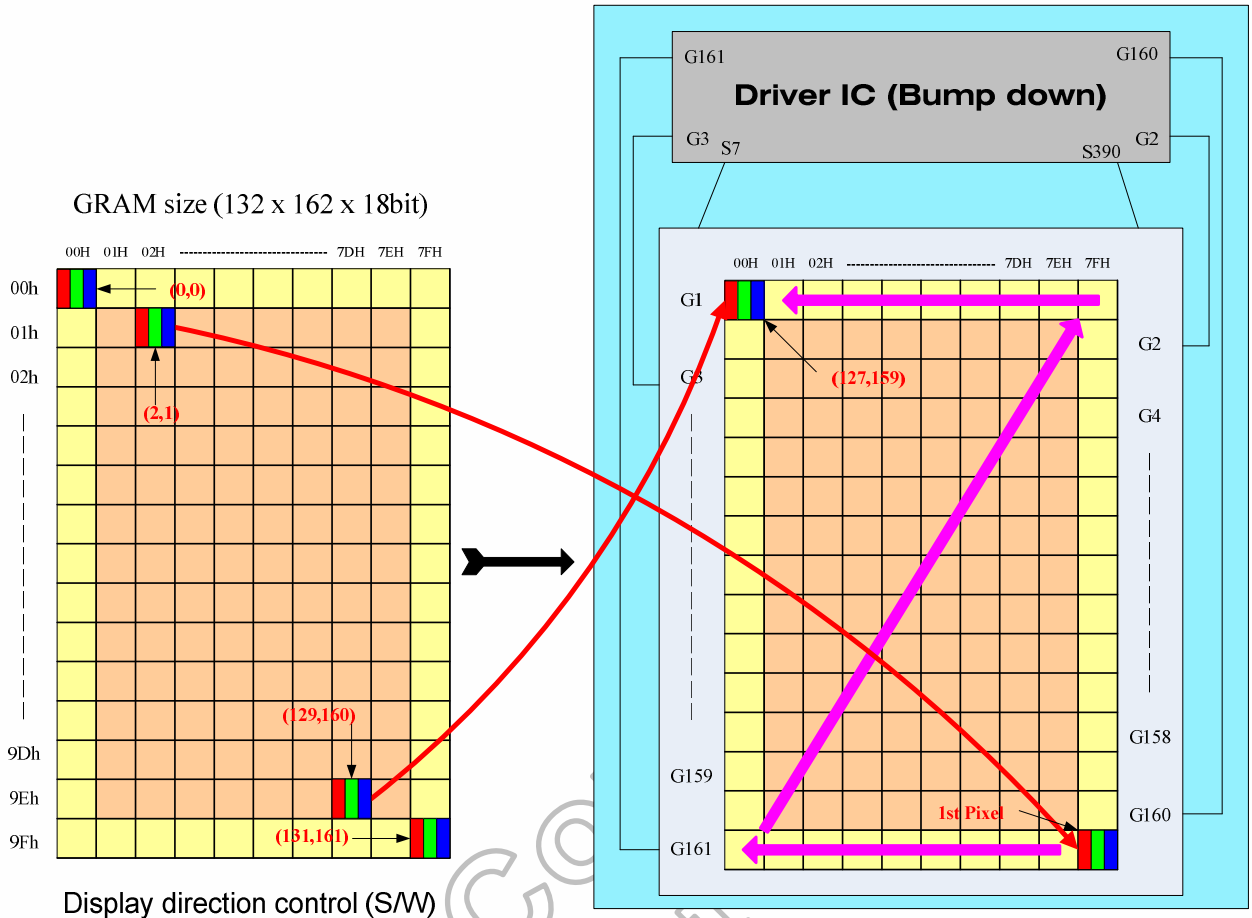
Example for SMX = SMY = 0



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Example for SMX = SMY = 0

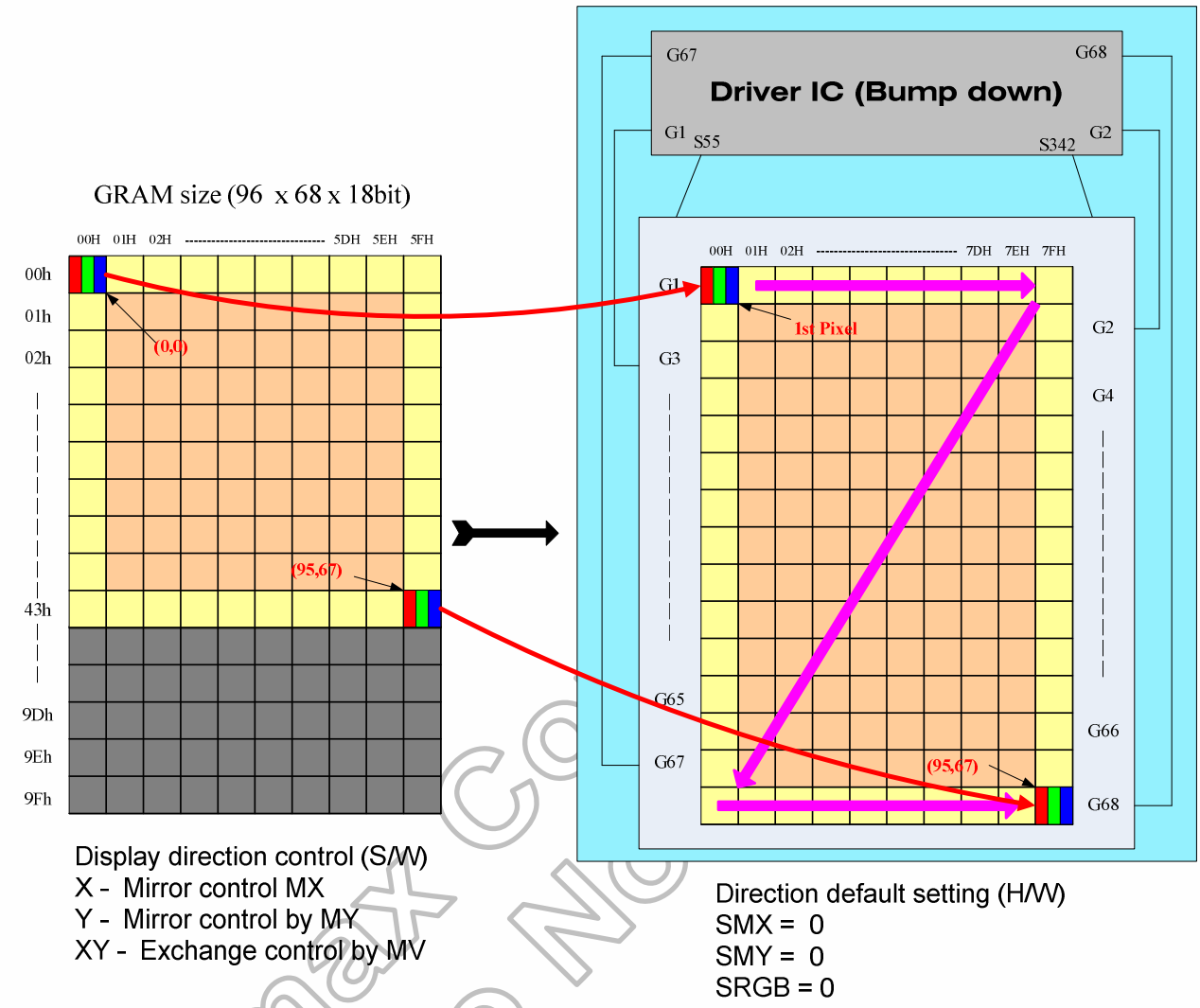


Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

Case 5 of resolution (96RGB x 68) (RSO[2:0] = 100) RAM size = 96 x 68 x 18-bits (Used)
Display size = 96RGB x 68

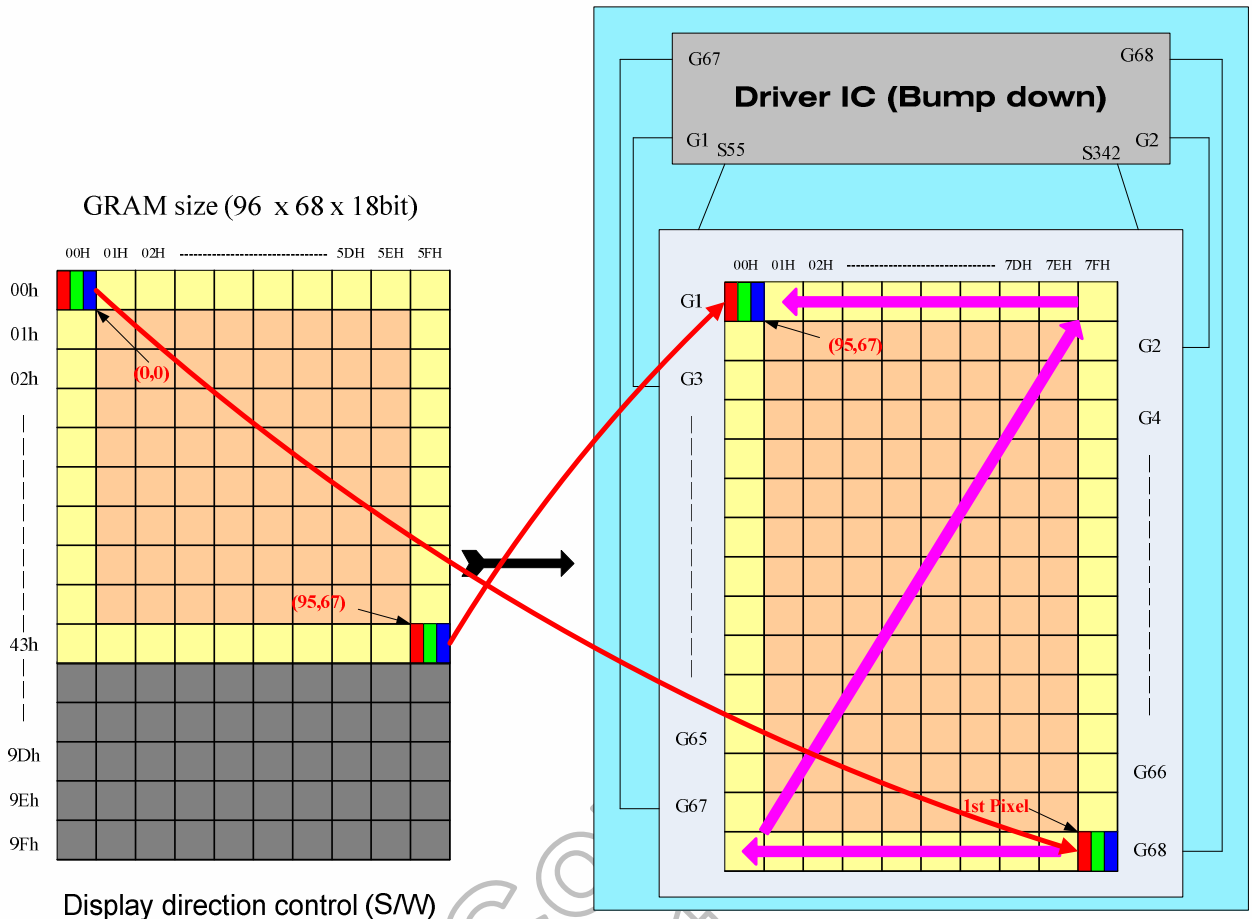
Example for SMX = SMY = 0



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Example for SMX = SMY = 1

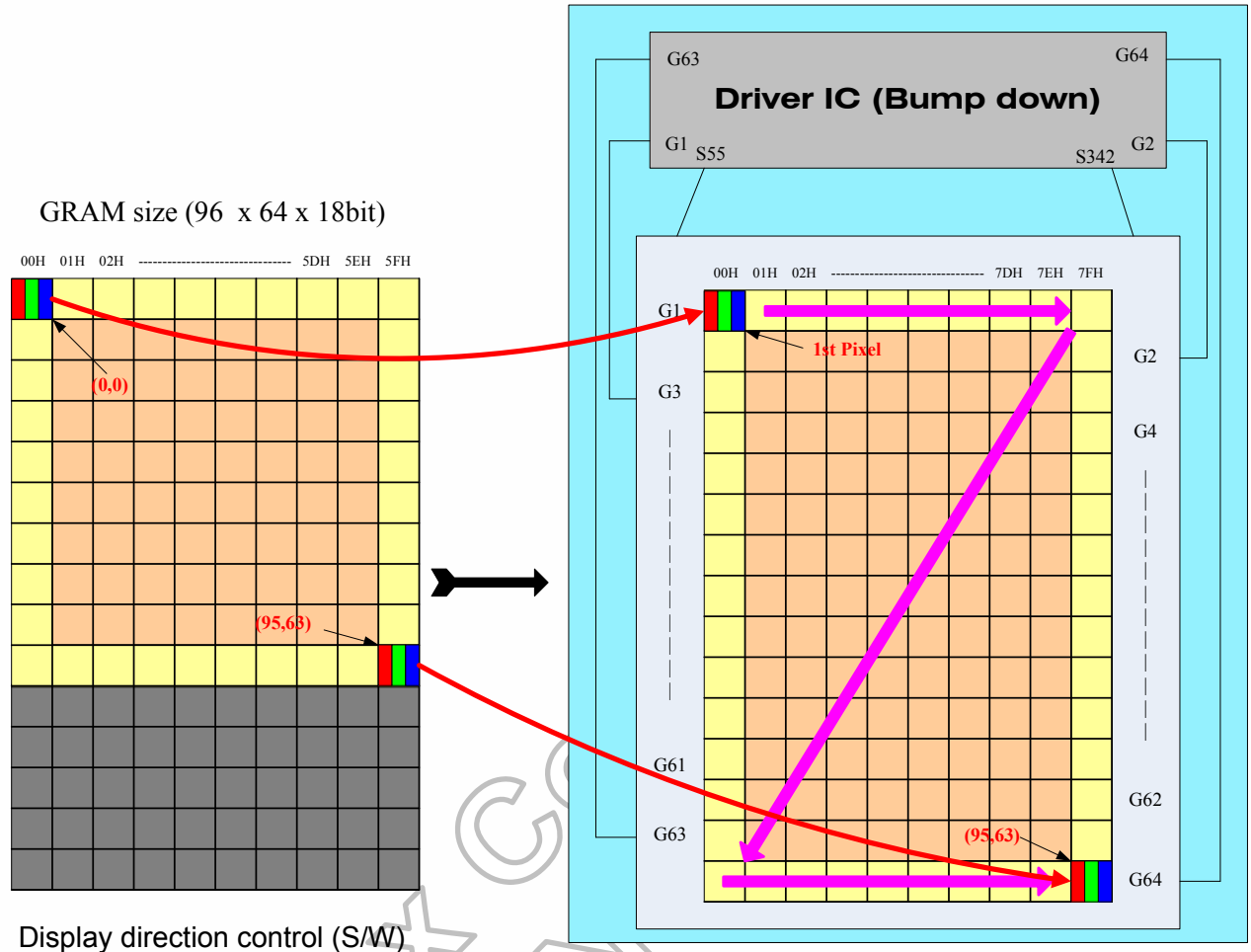


Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

Case 6 of resolution (96RGB x 64) (RSO[2:0] = 101) RAM size = 96 x 64 x 18-bits (Used)
Display size = 96RGB x 64

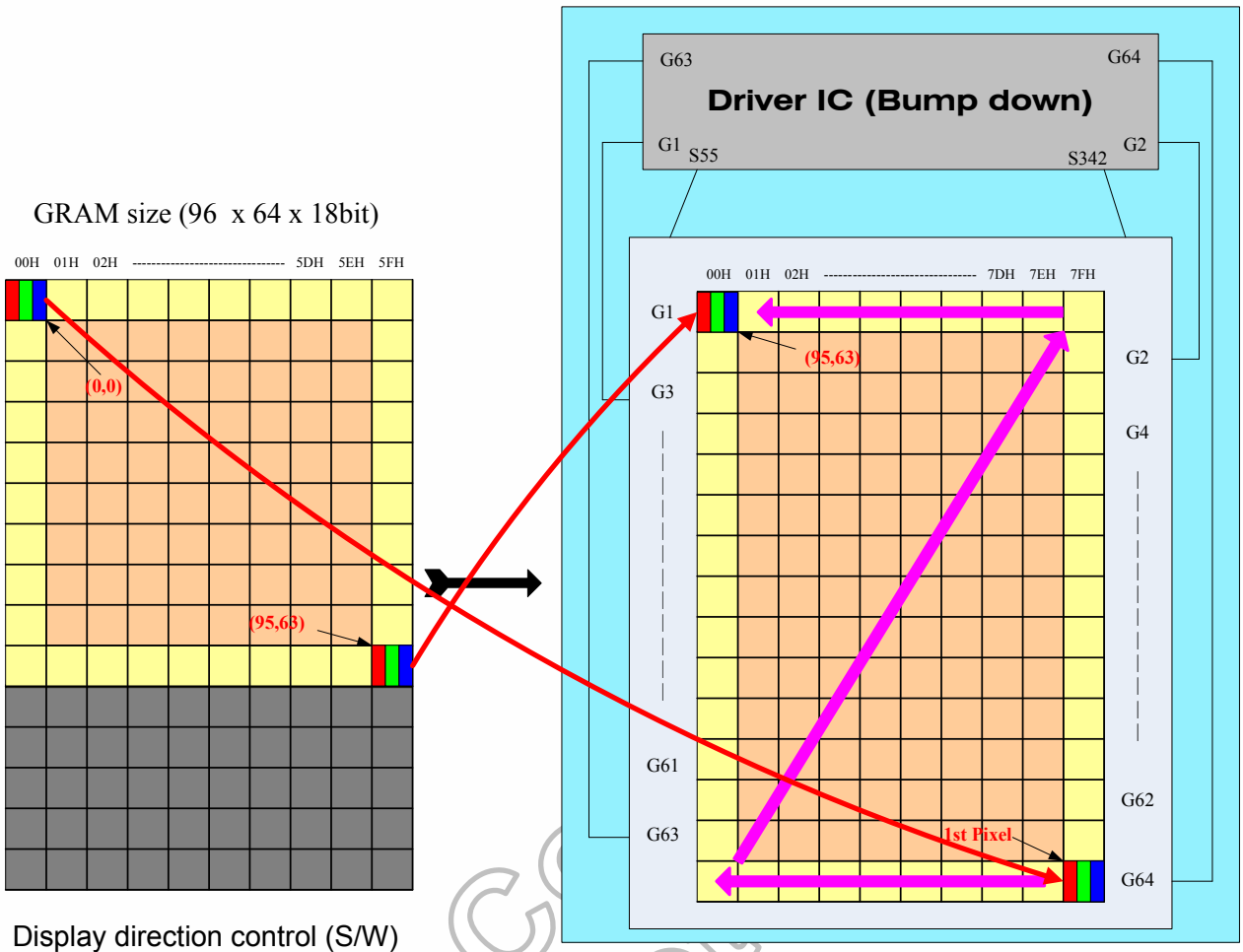
Example for SMX = SMY = 0



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 0
SMY = 0
SRGB = 0

Example for SMX = SMY = 1



Display direction control (S/W)
X - Mirror control MX
Y - Mirror control by MY
XY - Exchange control by MV

Direction default setting (H/W)
SMX = 1
SMY = 1
SRGB = 0

13. Ordering Information

Part No.	Package
HX8353-D000 PDxxx	PD : mean COG xxx : mean chip thickness (μm), (default: 250 μm)

14. Revision History

Version	Date	Description of Changes
01	2009/02/25	New setup
	2009/03/27	Remove VPNL_EN in P.166
	2009/04/20	Add In-House Register Command Setting
	2009/04/23	Modify RB5H => VR_TRIM(From [5:0] to [3:0])
	2009/05/25	Remove B1H Blank FS1[3:0] & FS0[3:0]
	2009/05/25	Modify B1H => PON is control VCL and VGL on/off
	2009/05/25	Modify BFH => PTBA[15] is control VGH on/off
	2009/06/17	Add application of connection with Different resolution
	2009/06/29	Modify VCI voltage form 2.3V to 2.5V Modify In-house register function. Modify OTP table. Modify Chip Size and pad coordinates. Modify CAP application (1uF at DDVDH, VGL, C11)
	2009/08/06	New Setup HX8353D ES1.0
	2009/08/12	Modify C1:16V ➔ 6.3V ; C2:16V ➔ 6.3V
	2009/09/02	Modify Au Bump Height 15um ➔ 12um
	2009/11/02	Modify ES1.3 IC default value
	2009/12/21	Modify OTP_index table and the N_RTN default value.
	2009/12/23	Modify chip thickness from 300um to 250um
	2010/01/22	Modify Pin assignment
	2010/02/02	update VGH & VGL voltage spec (P7,P11,P166)
	2010/02/09	Modify Fosc setting table
	2010/02/10	Define OTP current limit ≧20mA
	2010/04/12	Add VMF setting Note2(When Setting the VMF, be careful the VCOMH & VCOML voltage's range.)
	2010/04/23	Add RB0H、RC0H、RCBH、RE3H Register Command Set