DATA SHEET

(DOC No. HX8352-C01(T)-DS)

HX8352-C01(T)

240RGB x 432 dot, 262K color,
with internal GRAM,
TFT Mobile Single Chip Driver

Version 01 May, 2011

Himax Technologies, Inc.
http://www.himax.com.tw

List of Contents

May, 2011

List of Contents

List of Contents

List of Figures

List of Figures

List of Figures

List of Figures

List of Tables

1. General Description

This document describes Himax's HX8352-C01 supports 240x432 resolution driving controller. The HX8352-C01 is designed to provide a single-chip solution that combines a source driver, power supply circuit to drive a TFT dot matrix LCD with 240RGBx432 dots at maximum.

The HX8352-C01 can be operated in low-voltage condition for the interface and integrated internal boosters that produce the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8352-C01 also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8352-C01 supports several interface modes, including System interface mode and RGB interface mode. The interface mode is selected by the external hardware pins IM2~0.

The HX8352-C01 is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

This manual description focuses on Command-Parameter interface mode, about the Command-Parameter interface mode, please refer to the HX8352-C01(N) datasheet for detail.

2. Features

2.1 Display

- Single chip solution for a 240 x 432 type TFT LCD display
- Resolution: 240RGB x 432
- Display color modes
  - 262K colours (18-bit 6(R):6(G):6(B))
  - 65K colours (16-bit 5(R):6(G):5(B))
  - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

2.2 Display module

- Support 720 source channel outputs
- Supports 1-line / n-line/ frame inversion
- On module VCOM control (VCOMH= 3.0V to (DDVDH-0.5)V; VCOML=(VCL+0.5)V to 0V)
- Charge bump circuit for source, glass gate level shifter
  - DDVDH= 4.5V to 6.0V
  - Source output voltage level: VREG1= 4.0V to 5.5V
  - Positive gate driver output voltage level: VGH= 10V to 18V
  - Negative gate driver output voltage level: VGL= -5V to -12.5V
- Frame memory area 240 (H) x 432 (V) x 18-bit

2.3 Display / Control interface

- Display interface types supported
  - System Interface mode
    - 8080 MCU Type II interface (8-/ 9-/ 16-/ 18-bit bus)
    - 3 wrie Serial data transfer interface
    - 4 wrie Serial data transfer interface
  - RGB Interface mode
    - 16 bit/pixel R(5), G(6), B(5)
    - 18 bit/pixel R(6), G(6), B(6)

2.4 Input power

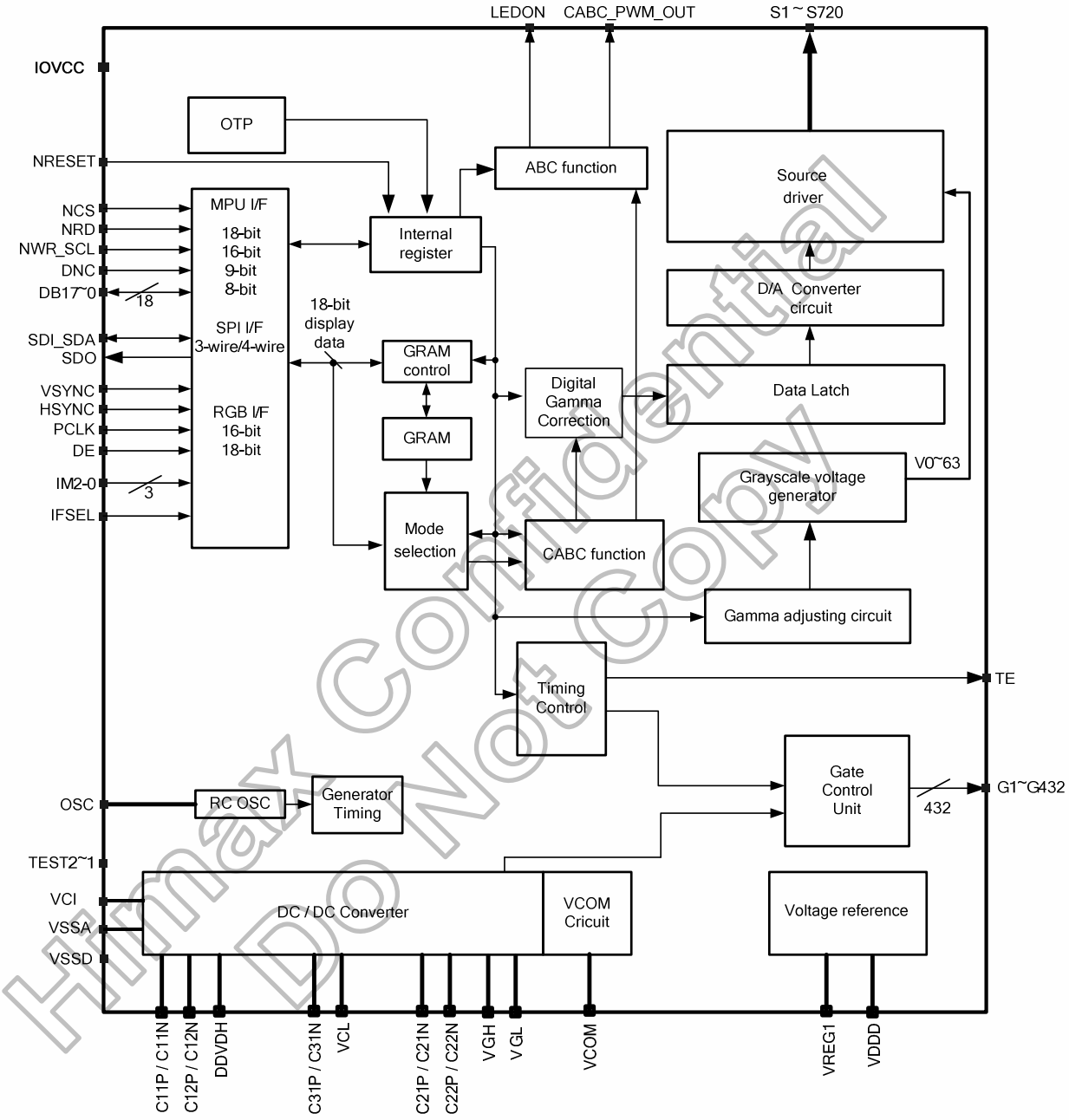
- I/O and Logic power power supply (IOVCC): 1.65V to 3.3V
- Analog power supply (VCI): 2.5V to 3.3V
- OTP programming voltage(internal generated or external supply on VGH): 7.5V ± 0.2V

2.5 Miscellaneous

- Partial display mode
- Vertical scrolling display
- Oscillator for display clock generation
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Optimized layout for COG assembly
- Temperature range: -40 to +85 ℃
- Support inversion mode
- DC/DC converter for source
- Support AC COM driving
- VCOM voltage generator
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 8 times MTP for VCOM setting and ID setting
- Support CABC (Content Adaptive Brightness Control) function
- Support 3 Gamma function(DGC, Digital Gamma Correction)

3. Device Overview

3.1 Block diagram

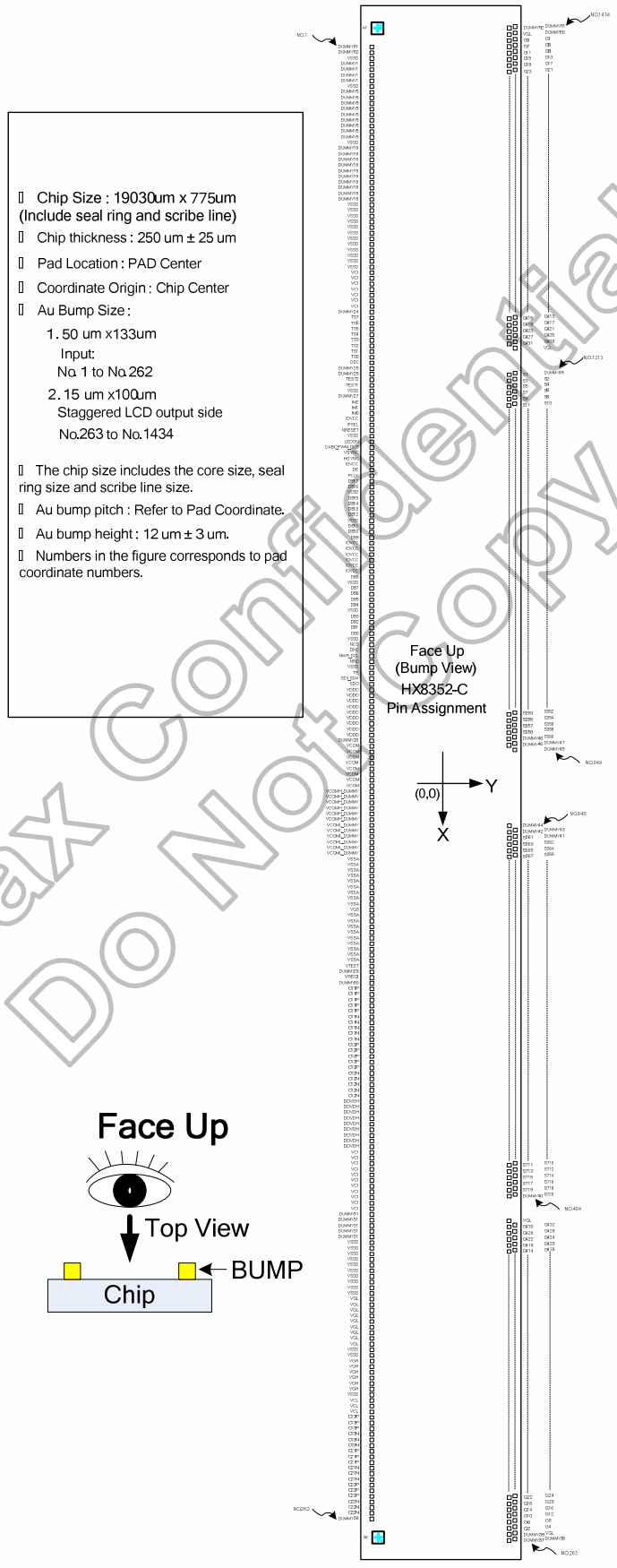


3.2 Pin description

<table>
<tr><th colspan="5">Host interface pins</th></tr>
<tr><th>Signals</th><th>I/O</th><th>Pin no.</th><th>Connected with</th><th>Description</th></tr>
<tr><td>IM2 ~ IM0</td><td>I</td><td>3</td><td>VSSD / IOVCC</td><td>Use with IFSEL=”H” Register-Content Interface mode
Select the interface mode as listed below:
<table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>Interface mode</th><th>DB pins</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>8080 MCU TYPE-II 18-bit</td><td>DB17-DB0: Data</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>8080 MCU TYPE-II 9-bit</td><td>DB8-DB0: Unused,
DB17-DB9: Data</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8080 MCU TYPE-II 16-bit</td><td>DB9, DB0:Unused,
DB17-DB10, DB8-DB1: Data</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8080 MCU TYPE-II 8-bit</td><td>DB9-DB0: Unused,
DB17-DB10: Data</td></tr>
<tr><td>1</td><td>0</td><td>ID</td><td>3-wire SPI</td><td>SDI_SDA, DB17-DB0</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>4-wire SPI</td><td>SDI_SDA, DB17-DB0</td></tr>
</table>
Pixel format (RGB565 / RGB666) is selected by command (0x17h)
Must be connected to VSSD or IOVCC.</td></tr>
<tr><td>IFSEL</td><td>I</td><td>1</td><td>VSSD / IOVCC</td><td>Interface format select pin
<table>
<tr><th>IFSEL</th><th>Interface Format Selection</th></tr>
<tr><td>1</td><td>Register-content interface mode</td></tr>
<tr><td>0</td><td>Command-Parameter interface mode</td></tr>
</table>
In this document, the IFSEL has to be connected to IOVCC and Register-content interface mode is selected.</td></tr>
<tr><td>NCS</td><td>I</td><td>1</td><td>MPU</td><td>Chip select signal.
Low: chip can be accessed.
High: chip cannot be accessed.
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>NRESET</td><td>I</td><td>1</td><td>MPU or reset circuit</td><td>Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or IOVCC).</td></tr>
<tr><td>NRD</td><td>I</td><td>1</td><td>MPU</td><td>Serves as a read signal and read data at the low level.
If this pin is not used, please connect it to VSSD or IVCC.</td></tr>
<tr><td>DNC</td><td>I</td><td>1</td><td>MPU</td><td>Data / Command Selection pin
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>NWR_SCL</td><td>I</td><td>1</td><td>MPU</td><td>DBI Type-B mode: Serves as a write signal and write data at the low level.
DBI Type-C mode: it servers as SCL (Serial Clock)
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>DB17~0</td><td>I/O</td><td>18</td><td>MPU</td><td>Data bus.
<table>
<tr><th>Interface mode</th><th>Command</th><th>Data</th></tr>
<tr><td>8080 MCU TYPE-II 8-bit</td><td>DB17~10</td><td>DB17~10</td></tr>
<tr><td>8080 MCU TYPE-II 9-bit</td><td>DB17~10</td><td>DB17~9</td></tr>
<tr><td>8080 MCU TYPE-II 16-bit</td><td>DB8~1</td><td>DB17~10, DB8~1</td></tr>
<tr><td>8080 MCU TYPE-II 18-bit</td><td>DB8~1</td><td>DB17~0</td></tr>
<tr><td>RGB 16-bit</td><td>SDI_SDA</td><td>DB15~0</td></tr>
<tr><td>RGB 18-bit</td><td>SDI_SDA</td><td>DB17~0</td></tr>
</table>
Please connect to VSSD or IOVCC for not used pin.</td></tr>
<tr><td>SDI_SDA</td><td>I/O</td><td>1</td><td>MPU</td><td>Serves as serial data input/output when SDA_EN=1. Serves as serial data input when SDA_EN=0.
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>SDO</td><td>O</td><td>1</td><td>MPU</td><td>Serial data output.
If this pin is not used, let it open.</td></tr>
<tr><th colspan="5">Clock input and DPI interface</th></tr>
<tr><td>HSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Line synchronizing signal.
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>DE</td><td>I</td><td>1</td><td>MPU</td><td>A data enable signal in DPI I/F mode.
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>1</td><td>MPU</td><td>Serves VS signal pin on DPI interface. (Input pad).
If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><td>PCLK</td><td>I</td><td>1</td><td>MPU</td><td>Dot clock signal. If this pin is not used, please connect it to VSSD or IOVCC.</td></tr>
<tr><th colspan="5">Source driver output pins</th></tr>
<tr><td>S1~S720</td><td>O</td><td>720</td><td>LCD</td><td>Output voltages applied to the liquid crystal.</td></tr>
<tr><td>TE</td><td>O</td><td>1</td><td>MPU</td><td>Serves TE (Tearing Effect) pin on MPU interface.
If not used, let it open.</td></tr>
<tr><th colspan="5">Gate driver output pins</th></tr>
<tr><td>G1~G432</td><td>O</td><td>432</td><td>LCD</td><td>Output voltages applied to the liquid crystal.</td></tr>
</table>

Power supply pins				
IOVCC	**P**	**8**	**Power supply**	A power supply for the I/O circuit and logic power. IOVCC=1.65 to 3.3V
VCI	**P**	**18**	**Power supply**	A power supply for the analog power, DC/DC converter VCI=2.5 to 3.3V.
VSSA	**P**	**18**	**Power supply**	Analoge ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSD	**P**	**36**	**Power supply**	Ground for the internal logic. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
Output Pins of Power and reference voltage				
DDVDH	**O**	**9**	**Stabilizing capacitor**	Output voltage from the step-up circuit, it is generated from VCI. Connect to a stabilizing capacitor between VSSA and DDVDH.
VREG1	**O**	**1**	**Open**	Internal generated stable power for source driver unit. Leave it open.
VCL	**O**	**3**	**Stabilizing capacitor**	Output voltage from the step-up circuit, it is generated from VCI. Connect to a stabilizing capacitor between VSSA and VCL.
VDDD	**O**	**9**	**Stabilizing capacitor**	Internal generated logic voltage(1.6V) output. Connect to a stabilizing capacitor between VSSD and VDDD.
VGH	**O**	**6**	**Stabilizing capacitor**	Output voltage from the step-up circuit, it is generated from DDVDH and VCI. Connect to a stabilizing capacitor between VSSA and VGH. If OTP program use external power mode, the VGH need connect to 7.5V.
VGL	**O**	**13**	**Stabilizing capacitor**	Output voltage from the step-up circuit, it is generated from VCL and VCI. Connect to a stabilizing capacitor between VSSA and VGL.
VCOM	**O**	**8**	**TFT common electrode**	The power supply of common voltage in TFT driving. The voltage amplitude between VCOMH and VCOML is output. Connect this pin to the common electrode on TFT panel.
VGS	**I**	**1**	**VSSD or external resistor**	Connect to a variable resistor to adjusting internal gamma reference voltage for matching the characteristic of different panel used.
DC/DC pumping				
C11P, C11N C12P, C12N	**I/O**	**5, 5 5, 5**	**Step-up Capacitor**	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the DDVDH voltage.
C21P, C21N C22P, C22N	**I/O**	**3, 3 3, 3**	**Step-up Capacitor**	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH/VGL voltage.
C31P, C31N	**I/O**	**3, 3**	**Step-up Capacitor**	Connect to the step-up capacitor according to the DC/DC pumping factor by pumping the VCL voltage.
CABC & ABC				
CABC_PWM_OUT	**O**	**1**	**LED Driver**	PWM output pin of Backlight control. If use CABC function, the pin can connect to external LED driver IC. The output voltage range= VSSD to IOVCC. If not used, let it open.
LEDON	**O**	**1**	**LED Driver**	Enable signal of Backlight LED driver(Active high). The output voltage range= VSSD to IOVCC. If not used, let it open.
Test Pins				
OSC	**I**	**1**	**Open**	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.
TEST1~2	**I**	**2**	**Open**	A test pin. This pin is by internal logic function test. If not used, let it open or connected to VSSD.(weak pull low)
TS0~7	**O**	**8**	**Open**	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open.
VTEST	**O**	**1**	**Open**	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMYR1 DUMMYR2	**-**	**2 2**	**Open**	Dummy pads. Available for measuring the COG contact resistance. They are short-circuited within the chip.
VCOMH_DUMMY	**-**	**6**	**Open**	Dummy pads.
VCOML_DUMMY	**-**	**6**	**Open**	Dummy pads.
DUMMY	**-**	**50**	**Open**	Dummy pads.

3.3 Pin assignment



3.4 PAD coordinates

No.	Name	X	Y	Bump size
1	DUMMYR1	-9135	-274	50*133
2	DUMMYR2	-9065	-274	50*133
3	VSSD	-8995	-274	50*133
4	DUMMY1	-8925	-274	50*133
5	DUMMY1	-8855	-274	50*133
6	DUMMY1	-8785	-274	50*133
7	DUMMY1	-8715	-274	50*133
8	VSSD	-8645	-274	50*133
9	DUMMY5	-8575	-274	50*133
10	DUMMY5	-8505	-274	50*133
11	DUMMY5	-8435	-274	50*133
12	DUMMY5	-8365	-274	50*133
13	DUMMY5	-8295	-274	50*133
14	DUMMY5	-8225	-274	50*133
15	DUMMY5	-8155	-274	50*133
16	DUMMY5	-8085	-274	50*133
17	DUMMY5	-8015	-274	50*133
18	VSSD	-7945	-274	50*133
19	DUMMY19	-7875	-274	50*133
20	DUMMY19	-7805	-274	50*133
21	DUMMY19	-7735	-274	50*133
22	DUMMY19	-7665	-274	50*133
23	DUMMY19	-7595	-274	50*133
24	DUMMY19	-7525	-274	50*133
25	DUMMY19	-7455	-274	50*133
26	DUMMY19	-7385	-274	50*133
27	DUMMY19	-7315	-274	50*133
28	DUMMY19	-7245	-274	50*133
29	VSSD	-7175	-274	50*133
30	VSSD	-7105	-274	50*133
31	VSSD	-7035	-274	50*133
32	VSSD	-6965	-274	50*133
33	VSSD	-6895	-274	50*133
34	VSSD	-6825	-274	50*133
35	VSSD	-6755	-274	50*133
36	VSSD	-6685	-274	50*133
37	VSSD	-6615	-274	50*133
38	VSSD	-6545	-274	50*133
39	VSSD	-6475	-274	50*133
40	VSSD	-6405	-274	50*133
41	VCI	-6335	-274	50*133
42	VCI	-6265	-274	50*133
43	VCI	-6195	-274	50*133
44	VCI	-6125	-274	50*133
45	VCI	-6055	-274	50*133
46	VCI	-5985	-274	50*133
47	VCI	-5915	-274	50*133
48	DUMMY24	-5845	-274	50*133
49	TS7	-5775	-274	50*133
50	TS6	-5705	-274	50*133
51	TS5	-5635	-274	50*133
52	TS4	-5565	-274	50*133
53	TS3	-5495	-274	50*133
54	TS2	-5425	-274	50*133
55	TS1	-5355	-274	50*133
56	TS0	-5285	-274	50*133
57	OSC	-5215	-274	50*133
58	DUMMY25	-5145	-274	50*133
59	DUMMY25	-5075	-274	50*133
60	TEST2	-5005	-274	50*133

No.	Name	X	Y	Bump size
61	TEST1	-4935	-274	50*133
62	VSSD	-4865	-274	50*133
63	DUMMY27	-4795	-274	50*133
64	IM2	-4725	-274	50*133
65	IM1	-4655	-274	50*133
66	IM0	-4585	-274	50*133
67	IOVCC	-4515	-274	50*133
68	IFSEL	-4445	-274	50*133
69	NRESET	-4375	-274	50*133
70	VSSD	-4305	-274	50*133
71	LEDON	-4235	-274	50*133
72	CABC_PWM_OUT	-4165	-274	50*133
73	VSYNC	-4095	-274	50*133
74	HSYNC	-4025	-274	50*133
75	IOVCC	-3955	-274	50*133
76	DE	-3885	-274	50*133
77	PCLK	-3815	-274	50*133
78	DB17	-3745	-274	50*133
79	DB16	-3675	-274	50*133
80	VSSD	-3605	-274	50*133
81	DB15	-3535	-274	50*133
82	DB14	-3465	-274	50*133
83	DB13	-3395	-274	50*133
84	DB12	-3325	-274	50*133
85	VSSD	-3255	-274	50*133
86	DB11	-3185	-274	50*133
87	DB10	-3115	-274	50*133
88	DB9	-3045	-274	50*133
89	IOVCC	-2975	-274	50*133
90	IOVCC	-2905	-274	50*133
91	IOVCC	-2835	-274	50*133
92	IOVCC	-2765	-274	50*133
93	IOVCC	-2695	-274	50*133
94	IOVCC	-2625	-274	50*133
95	DB8	-2555	-274	50*133
96	VSSD	-2485	-274	50*133
97	DB7	-2415	-274	50*133
98	DB6	-2345	-274	50*133
99	DB5	-2275	-274	50*133
100	DB4	-2205	-274	50*133
101	VSSD	-2135	-274	50*133
102	DB3	-2065	-274	50*133
103	DB2	-1995	-274	50*133
104	DB1	-1925	-274	50*133
105	DB0	-1855	-274	50*133
106	VSSD	-1785	-274	50*133
107	NCS	-1715	-274	50*133
108	DNC	-1645	-274	50*133
109	NWR_SCL	-1575	-274	50*133
110	NRD	-1505	-274	50*133
111	VSSD	-1435	-274	50*133
112	TE	-1365	-274	50*133
113	SDI_SDA	-1295	-274	50*133
114	SDO	-1225	-274	50*133
115	VDDD	-1155	-274	50*133
116	VDDD	-1085	-274	50*133
117	VDDD	-1015	-274	50*133
118	VDDD	-945	-274	50*133
119	VDDD	-875	-274	50*133
120	VDDD	-805	-274	50*133

No.	Name	X	Y	Bump size
121	VDDD	-735	-274	50*133
122	VDDD	-665	-274	50*133
123	VDDD	-595	-274	50*133
124	DUMMY28	-525	-274	50*133
125	VCOM	-455	-274	50*133
126	VCOM	-385	-274	50*133
127	VCOM	-315	-274	50*133
128	VCOM	-245	-274	50*133
129	VCOM	-175	-274	50*133
130	VCOM	-105	-274	50*133
131	VCOM	-35	-274	50*133
132	VCOM	35	-274	50*133
133	VCOMH_DUMMY	105	-274	50*133
134	VCOMH_DUMMY	175	-274	50*133
135	VCOMH_DUMMY	245	-274	50*133
136	VCOMH_DUMMY	315	-274	50*133
137	VCOMH_DUMMY	385	-274	50*133
138	VCOMH_DUMMY	455	-274	50*133
139	VCOML_DUMMY	525	-274	50*133
140	VCOML_DUMMY	595	-274	50*133
141	VCOML_DUMMY	665	-274	50*133
142	VCOML_DUMMY	735	-274	50*133
143	VCOML_DUMMY	805	-274	50*133
144	VCOML_DUMMY	875	-274	50*133
145	VSSA	945	-274	50*133
146	VSSA	1015	-274	50*133
147	VSSA	1085	-274	50*133
148	VSSA	1155	-274	50*133
149	VSSA	1225	-274	50*133
150	VSSA	1295	-274	50*133
151	VSSA	1365	-274	50*133
152	VSSA	1435	-274	50*133
153	VSSA	1505	-274	50*133
154	VGS	1575	-274	50*133
155	VSSA	1645	-274	50*133
156	VSSA	1715	-274	50*133
157	VSSA	1785	-274	50*133
158	VSSA	1855	-274	50*133
159	VSSA	1925	-274	50*133
160	VSSA	1995	-274	50*133
161	VSSA	2065	-274	50*133
162	VSSA	2135	-274	50*133
163	VSSA	2205	-274	50*133
164	VTEST	2275	-274	50*133
165	DUMMY29	2345	-274	50*133
166	VREG1	2415	-274	50*133
167	DUMMY30	2485	-274	50*133
168	C11P	2555	-274	50*133
169	C11P	2625	-274	50*133
170	C11P	2695	-274	50*133
171	C11P	2765	-274	50*133
172	C11P	2835	-274	50*133
173	C11N	2905	-274	50*133
174	C11N	2975	-274	50*133
175	C11N	3045	-274	50*133
176	C11N	3115	-274	50*133
177	C11N	3185	-274	50*133
178	C12P	3255	-274	50*133
179	C12P	3325	-274	50*133
180	C12P	3395	-274	50*133

No.	Name	X	Y	Bump size
181	C12P	3465	-274	50*133
182	C12P	3535	-274	50*133
183	C12N	3605	-274	50*133
184	C12N	3675	-274	50*133
185	C12N	3745	-274	50*133
186	C12N	3815	-274	50*133
187	C12N	3885	-274	50*133
188	DDVDH	3955	-274	50*133
189	DDVDH	4025	-274	50*133
190	DDVDH	4095	-274	50*133
191	DDVDH	4165	-274	50*133
192	DDVDH	4235	-274	50*133
193	DDVDH	4305	-274	50*133
194	DDVDH	4375	-274	50*133
195	DDVDH	4445	-274	50*133
196	DDVDH	4515	-274	50*133
197	VCI	4585	-274	50*133
198	VCI	4655	-274	50*133
199	VCI	4725	-274	50*133
200	VCI	4795	-274	50*133
201	VCI	4865	-274	50*133
202	VCI	4935	-274	50*133
203	VCI	5005	-274	50*133
204	VCI	5075	-274	50*133
205	VCI	5145	-274	50*133
206	VCI	5215	-274	50*133
207	VCI	5285	-274	50*133
208	DUMMY31	5355	-274	50*133
209	DUMMY31	5425	-274	50*133
210	DUMMY31	5495	-274	50*133
211	DUMMY31	5565	-274	50*133
212	DUMMY31	5635	-274	50*133
213	VSSD	5705	-274	50*133
214	VSSD	5775	-274	50*133
215	VSSD	5845	-274	50*133
216	VSSD	5915	-274	50*133
217	VSSD	5985	-274	50*133
218	VSSD	6055	-274	50*133
219	VSSD	6125	-274	50*133
220	VSSD	6195	-274	50*133
221	VSSD	6265	-274	50*133
222	VSSD	6335	-274	50*133
223	VGL	6405	-274	50*133
224	VGL	6475	-274	50*133
225	VGL	6545	-274	50*133
226	VGL	6615	-274	50*133
227	VGL	6685	-274	50*133
228	VGL	6755	-274	50*133
229	VGL	6825	-274	50*133
230	VGL	6895	-274	50*133
231	VGL	6965	-274	50*133
232	VSSD	7035	-274	50*133
233	VSSD	7105	-274	50*133
234	VGH	7175	-274	50*133
235	VGH	7245	-274	50*133
236	VGH	7315	-274	50*133
237	VGH	7385	-274	50*133
238	VGH	7455	-274	50*133
239	VGH	7525	-274	50*133
240	VSSD	7595	-274	50*133
241	VCL	7665	-274	50*133
242	VCL	7735	-274	50*133
243	VCL	7805	-274	50*133
244	C31P	7875	-274	50*133
245	C31P	7945	-274	50*133
246	C31P	8015	-274	50*133
247	C31N	8085	-274	50*133
248	C31N	8155	-274	50*133
249	C31N	8225	-274	50*133
250	C21P	8295	-274	50*133
251	C21P	8365	-274	50*133
252	C21P	8435	-274	50*133
253	C21N	8505	-274	50*133
254	C21N	8575	-274	50*133
255	C21N	8645	-274	50*133
256	C22P	8715	-274	50*133
257	C22P	8785	-274	50*133
258	C22P	8855	-274	50*133
259	C22N	8925	-274	50*133
260	C22N	8995	-274	50*133
261	C22N	9065	-274	50*133
262	DUMMY36	9135	-274	50*133
263	DUMMY37	9397.5	173.5	15*100
264	DUMMY38	9382.5	292.5	15*100
265	DUMMY39	9367.5	173.5	15*100
266	VGL	9352.5	292.5	15*100
267	G2	9337.5	173.5	15*100
268	G4	9322.5	292.5	15*100
269	G6	9307.5	173.5	15*100
270	G8	9292.5	292.5	15*100
271	G10	9277.5	173.5	15*100
272	G12	9262.5	292.5	15*100
273	G14	9247.5	173.5	15*100
274	G16	9232.5	292.5	15*100
275	G18	9217.5	173.5	15*100
276	G20	9202.5	292.5	15*100
277	G22	9187.5	173.5	15*100
278	G24	9172.5	292.5	15*100
279	G26	9157.5	173.5	15*100
280	G28	9142.5	292.5	15*100
281	G30	9127.5	173.5	15*100
282	G32	9112.5	292.5	15*100
283	G34	9097.5	173.5	15*100
284	G36	9082.5	292.5	15*100
285	G38	9067.5	173.5	15*100
286	G40	9052.5	292.5	15*100
287	G42	9037.5	173.5	15*100
288	G44	9022.5	292.5	15*100
289	G46	9007.5	173.5	15*100
290	G48	8992.5	292.5	15*100
291	G50	8977.5	173.5	15*100
292	G52	8962.5	292.5	15*100
293	G54	8947.5	173.5	15*100
294	G56	8932.5	292.5	15*100
295	G58	8917.5	173.5	15*100
296	G60	8902.5	292.5	15*100
297	G62	8887.5	173.5	15*100
298	G64	8872.5	292.5	15*100
299	G66	8857.5	173.5	15*100
300	G68	8842.5	292.5	15*100
301	G70	8827.5	173.5	15*100
302	G72	8812.5	292.5	15*100
303	G74	8797.5	173.5	15*100
304	G76	8782.5	292.5	15*100
305	G78	8767.5	173.5	15*100
306	G80	8752.5	292.5	15*100
307	G82	8737.5	173.5	15*100
308	G84	8722.5	292.5	15*100
309	G86	8707.5	173.5	15*100
310	G88	8692.5	292.5	15*100
311	G90	8677.5	173.5	15*100
312	G92	8662.5	292.5	15*100
313	G94	8647.5	173.5	15*100
314	G96	8632.5	292.5	15*100
315	G98	8617.5	173.5	15*100
316	G100	8602.5	292.5	15*100
317	G102	8587.5	173.5	15*100
318	G104	8572.5	292.5	15*100
319	G106	8557.5	173.5	15*100
320	G108	8542.5	292.5	15*100
321	G110	8527.5	173.5	15*100
322	G112	8512.5	292.5	15*100
323	G114	8497.5	173.5	15*100
324	G116	8482.5	292.5	15*100
325	G118	8467.5	173.5	15*100
326	G120	8452.5	292.5	15*100
327	G122	8437.5	173.5	15*100
328	G124	8422.5	292.5	15*100
329	G126	8407.5	173.5	15*100
330	G128	8392.5	292.5	15*100
331	G130	8377.5	173.5	15*100
332	G132	8362.5	292.5	15*100
333	G134	8347.5	173.5	15*100
334	G136	8332.5	292.5	15*100
335	G138	8317.5	173.5	15*100
336	G140	8302.5	292.5	15*100
337	G142	8287.5	173.5	15*100
338	G144	8272.5	292.5	15*100
339	G146	8257.5	173.5	15*100
340	G148	8242.5	292.5	15*100
341	G150	8227.5	173.5	15*100
342	G152	8212.5	292.5	15*100
343	G154	8197.5	173.5	15*100
344	G156	8182.5	292.5	15*100
345	G158	8167.5	173.5	15*100
346	G160	8152.5	292.5	15*100
347	G162	8137.5	173.5	15*100
348	G164	8122.5	292.5	15*100
349	G166	8107.5	173.5	15*100
350	G168	8092.5	292.5	15*100
351	G170	8077.5	173.5	15*100
352	G172	8062.5	292.5	15*100
353	G174	8047.5	173.5	15*100
354	G176	8032.5	292.5	15*100
355	G178	8017.5	173.5	15*100
356	G180	8002.5	292.5	15*100
357	G182	7987.5	173.5	15*100
358	G184	7972.5	292.5	15*100
359	G186	7957.5	173.5	15*100
360	G188	7942.5	292.5	15*100

No.	Name	X	Y	Bump size
361	G190	7927.5	173.5	15*100
362	G192	7912.5	292.5	15*100
363	G194	7897.5	173.5	15*100
364	G196	7882.5	292.5	15*100
365	G198	7867.5	173.5	15*100
366	G200	7852.5	292.5	15*100
367	G202	7837.5	173.5	15*100
368	G204	7822.5	292.5	15*100
369	G206	7807.5	173.5	15*100
370	G208	7792.5	292.5	15*100
371	G210	7777.5	173.5	15*100
372	G212	7762.5	292.5	15*100
373	G214	7747.5	173.5	15*100
374	G216	7732.5	292.5	15*100
375	G218	7717.5	173.5	15*100
376	G220	7702.5	292.5	15*100
377	G222	7687.5	173.5	15*100
378	G224	7672.5	292.5	15*100
379	G226	7657.5	173.5	15*100
380	G228	7642.5	292.5	15*100
381	G230	7627.5	173.5	15*100
382	G232	7612.5	292.5	15*100
383	G234	7597.5	173.5	15*100
384	G236	7582.5	292.5	15*100
385	G238	7567.5	173.5	15*100
386	G240	7552.5	292.5	15*100
387	G242	7537.5	173.5	15*100
388	G244	7522.5	292.5	15*100
389	G246	7507.5	173.5	15*100
390	G248	7492.5	292.5	15*100
391	G250	7477.5	173.5	15*100
392	G252	7462.5	292.5	15*100
393	G254	7447.5	173.5	15*100
394	G256	7432.5	292.5	15*100
395	G258	7417.5	173.5	15*100
396	G260	7402.5	292.5	15*100
397	G262	7387.5	173.5	15*100
398	G264	7372.5	292.5	15*100
399	G266	7357.5	173.5	15*100
400	G268	7342.5	292.5	15*100
401	G270	7327.5	173.5	15*100
402	G272	7312.5	292.5	15*100
403	G274	7297.5	173.5	15*100
404	G276	7282.5	292.5	15*100
405	G278	7267.5	173.5	15*100
406	G280	7252.5	292.5	15*100
407	G282	7237.5	173.5	15*100
408	G284	7222.5	292.5	15*100
409	G286	7207.5	173.5	15*100
410	G288	7192.5	292.5	15*100
411	G290	7177.5	173.5	15*100
412	G292	7162.5	292.5	15*100
413	G294	7147.5	173.5	15*100
414	G296	7132.5	292.5	15*100
415	G298	7117.5	173.5	15*100
416	G300	7102.5	292.5	15*100
417	G302	7087.5	173.5	15*100
418	G304	7072.5	292.5	15*100
419	G306	7057.5	173.5	15*100
420	G308	7042.5	292.5	15*100
421	G310	7027.5	173.5	15*100
422	G312	7012.5	292.5	15*100
423	G314	6997.5	173.5	15*100
424	G316	6982.5	292.5	15*100
425	G318	6967.5	173.5	15*100
426	G320	6952.5	292.5	15*100
427	G322	6937.5	173.5	15*100
428	G324	6922.5	292.5	15*100
429	G326	6907.5	173.5	15*100
430	G328	6892.5	292.5	15*100
431	G330	6877.5	173.5	15*100
432	G332	6862.5	292.5	15*100
433	G334	6847.5	173.5	15*100
434	G336	6832.5	292.5	15*100
435	G338	6817.5	173.5	15*100
436	G340	6802.5	292.5	15*100
437	G342	6787.5	173.5	15*100
438	G344	6772.5	292.5	15*100
439	G346	6757.5	173.5	15*100
440	G348	6742.5	292.5	15*100
441	G350	6727.5	173.5	15*100
442	G352	6712.5	292.5	15*100
443	G354	6697.5	173.5	15*100
444	G356	6682.5	292.5	15*100
445	G358	6667.5	173.5	15*100
446	G360	6652.5	292.5	15*100
447	G362	6637.5	173.5	15*100
448	G364	6622.5	292.5	15*100
449	G366	6607.5	173.5	15*100
450	G368	6592.5	292.5	15*100
451	G370	6577.5	173.5	15*100
452	G372	6562.5	292.5	15*100
453	G374	6547.5	173.5	15*100
454	G376	6532.5	292.5	15*100
455	G378	6517.5	173.5	15*100
456	G380	6502.5	292.5	15*100
457	G382	6487.5	173.5	15*100
458	G384	6472.5	292.5	15*100
459	G386	6457.5	173.5	15*100
460	G388	6442.5	292.5	15*100
461	G390	6427.5	173.5	15*100
462	G392	6412.5	292.5	15*100
463	G394	6397.5	173.5	15*100
464	G396	6382.5	292.5	15*100
465	G398	6367.5	173.5	15*100
466	G400	6352.5	292.5	15*100
467	G402	6337.5	173.5	15*100
468	G404	6322.5	292.5	15*100
469	G406	6307.5	173.5	15*100
470	G408	6292.5	292.5	15*100
471	G410	6277.5	173.5	15*100
472	G412	6262.5	292.5	15*100
473	G414	6247.5	173.5	15*100
474	G416	6232.5	292.5	15*100
475	G418	6217.5	173.5	15*100
476	G420	6202.5	292.5	15*100
477	G422	6187.5	173.5	15*100
478	G424	6172.5	292.5	15*100
479	G426	6157.5	173.5	15*100
480	G428	6142.5	292.5	15*100
481	G430	6127.5	173.5	15*100
482	G432	6112.5	292.5	15*100
483	VGL	6097.5	173.5	15*100
484	DUMMY40	5887.5	173.5	15*100
485	S720	5872.5	292.5	15*100
486	S719	5857.5	173.5	15*100
487	S718	5842.5	292.5	15*100
488	S717	5827.5	173.5	15*100
489	S716	5812.5	292.5	15*100
490	S715	5797.5	173.5	15*100
491	S714	5782.5	292.5	15*100
492	S713	5767.5	173.5	15*100
493	S712	5752.5	292.5	15*100
494	S711	5737.5	173.5	15*100
495	S710	5722.5	292.5	15*100
496	S709	5707.5	173.5	15*100
497	S708	5692.5	292.5	15*100
498	S707	5677.5	173.5	15*100
499	S706	5662.5	292.5	15*100
500	S705	5647.5	173.5	15*100
501	S704	5632.5	292.5	15*100
502	S703	5617.5	173.5	15*100
503	S702	5602.5	292.5	15*100
504	S701	5587.5	173.5	15*100
505	S700	5572.5	292.5	15*100
506	S699	5557.5	173.5	15*100
507	S698	5542.5	292.5	15*100
508	S697	5527.5	173.5	15*100
509	S696	5512.5	292.5	15*100
510	S695	5497.5	173.5	15*100
511	S694	5482.5	292.5	15*100
512	S693	5467.5	173.5	15*100
513	S692	5452.5	292.5	15*100
514	S691	5437.5	173.5	15*100
515	S690	5422.5	292.5	15*100
516	S689	5407.5	173.5	15*100
517	S688	5392.5	292.5	15*100
518	S687	5377.5	173.5	15*100
519	S686	5362.5	292.5	15*100
520	S685	5347.5	173.5	15*100
521	S684	5332.5	292.5	15*100
522	S683	5317.5	173.5	15*100
523	S682	5302.5	292.5	15*100
524	S681	5287.5	173.5	15*100
525	S680	5272.5	292.5	15*100
526	S679	5257.5	173.5	15*100
527	S678	5242.5	292.5	15*100
528	S677	5227.5	173.5	15*100
529	S676	5212.5	292.5	15*100
530	S675	5197.5	173.5	15*100
531	S674	5182.5	292.5	15*100
532	S673	5167.5	173.5	15*100
533	S672	5152.5	292.5	15*100
534	S671	5137.5	173.5	15*100
535	S670	5122.5	292.5	15*100
536	S669	5107.5	173.5	15*100
537	S668	5092.5	292.5	15*100
538	S667	5077.5	173.5	15*100
539	S666	5062.5	292.5	15*100
540	S665	5047.5	173.5	15*100

No.	Name	X	Y	Bump size
541	S664	5032.5	292.5	15*100
542	S663	5017.5	173.5	15*100
543	S662	5002.5	292.5	15*100
544	S661	4987.5	173.5	15*100
545	S660	4972.5	292.5	15*100
546	S659	4957.5	173.5	15*100
547	S658	4942.5	292.5	15*100
548	S657	4927.5	173.5	15*100
549	S656	4912.5	292.5	15*100
550	S655	4897.5	173.5	15*100
551	S654	4882.5	292.5	15*100
552	S653	4867.5	173.5	15*100
553	S652	4852.5	292.5	15*100
554	S651	4837.5	173.5	15*100
555	S650	4822.5	292.5	15*100
556	S649	4807.5	173.5	15*100
557	S648	4792.5	292.5	15*100
558	S647	4777.5	173.5	15*100
559	S646	4762.5	292.5	15*100
560	S645	4747.5	173.5	15*100
561	S644	4732.5	292.5	15*100
562	S643	4717.5	173.5	15*100
563	S642	4702.5	292.5	15*100
564	S641	4687.5	173.5	15*100
565	S640	4672.5	292.5	15*100
566	S639	4657.5	173.5	15*100
567	S638	4642.5	292.5	15*100
568	S637	4627.5	173.5	15*100
569	S636	4612.5	292.5	15*100
570	S635	4597.5	173.5	15*100
571	S634	4582.5	292.5	15*100
572	S633	4567.5	173.5	15*100
573	S632	4552.5	292.5	15*100
574	S631	4537.5	173.5	15*100
575	S630	4522.5	292.5	15*100
576	S629	4507.5	173.5	15*100
577	S628	4492.5	292.5	15*100
578	S627	4477.5	173.5	15*100
579	S626	4462.5	292.5	15*100
580	S625	4447.5	173.5	15*100
581	S624	4432.5	292.5	15*100
582	S623	4417.5	173.5	15*100
583	S622	4402.5	292.5	15*100
584	S621	4387.5	173.5	15*100
585	S620	4372.5	292.5	15*100
586	S619	4357.5	173.5	15*100
587	S618	4342.5	292.5	15*100
588	S617	4327.5	173.5	15*100
589	S616	4312.5	292.5	15*100
590	S615	4297.5	173.5	15*100
591	S614	4282.5	292.5	15*100
592	S613	4267.5	173.5	15*100
593	S612	4252.5	292.5	15*100
594	S611	4237.5	173.5	15*100
595	S610	4222.5	292.5	15*100
596	S609	4207.5	173.5	15*100
597	S608	4192.5	292.5	15*100
598	S607	4177.5	173.5	15*100
599	S606	4162.5	292.5	15*100
600	S605	4147.5	173.5	15*100
601	S604	4132.5	292.5	15*100
602	S603	4117.5	173.5	15*100
603	S602	4102.5	292.5	15*100
604	S601	4087.5	173.5	15*100
605	S600	4072.5	292.5	15*100
606	S599	4057.5	173.5	15*100
607	S598	4042.5	292.5	15*100
608	S597	4027.5	173.5	15*100
609	S596	4012.5	292.5	15*100
610	S595	3997.5	173.5	15*100
611	S594	3982.5	292.5	15*100
612	S593	3967.5	173.5	15*100
613	S592	3952.5	292.5	15*100
614	S591	3937.5	173.5	15*100
615	S590	3922.5	292.5	15*100
616	S589	3907.5	173.5	15*100
617	S588	3892.5	292.5	15*100
618	S587	3877.5	173.5	15*100
619	S586	3862.5	292.5	15*100
620	S585	3847.5	173.5	15*100
621	S584	3832.5	292.5	15*100
622	S583	3817.5	173.5	15*100
623	S582	3802.5	292.5	15*100
624	S581	3787.5	173.5	15*100
625	S580	3772.5	292.5	15*100
626	S579	3757.5	173.5	15*100
627	S578	3742.5	292.5	15*100
628	S577	3727.5	173.5	15*100
629	S576	3712.5	292.5	15*100
630	S575	3697.5	173.5	15*100
631	S574	3682.5	292.5	15*100
632	S573	3667.5	173.5	15*100
633	S572	3652.5	292.5	15*100
634	S571	3637.5	173.5	15*100
635	S570	3622.5	292.5	15*100
636	S569	3607.5	173.5	15*100
637	S568	3592.5	292.5	15*100
638	S567	3577.5	173.5	15*100
639	S566	3562.5	292.5	15*100
640	S565	3547.5	173.5	15*100
641	S564	3532.5	292.5	15*100
642	S563	3517.5	173.5	15*100
643	S562	3502.5	292.5	15*100
644	S561	3487.5	173.5	15*100
645	S560	3472.5	292.5	15*100
646	S559	3457.5	173.5	15*100
647	S558	3442.5	292.5	15*100
648	S557	3427.5	173.5	15*100
649	S556	3412.5	292.5	15*100
650	S555	3397.5	173.5	15*100
651	S554	3382.5	292.5	15*100
652	S553	3367.5	173.5	15*100
653	S552	3352.5	292.5	15*100
654	S551	3337.5	173.5	15*100
655	S550	3322.5	292.5	15*100
656	S549	3307.5	173.5	15*100
657	S548	3292.5	292.5	15*100
658	S547	3277.5	173.5	15*100
659	S546	3262.5	292.5	15*100
660	S545	3247.5	173.5	15*100
661	S544	3232.5	292.5	15*100
662	S543	3217.5	173.5	15*100
663	S542	3202.5	292.5	15*100
664	S541	3187.5	173.5	15*100
665	S540	3172.5	292.5	15*100
666	S539	3157.5	173.5	15*100
667	S538	3142.5	292.5	15*100
668	S537	3127.5	173.5	15*100
669	S536	3112.5	292.5	15*100
670	S535	3097.5	173.5	15*100
671	S534	3082.5	292.5	15*100
672	S533	3067.5	173.5	15*100
673	S532	3052.5	292.5	15*100
674	S531	3037.5	173.5	15*100
675	S530	3022.5	292.5	15*100
676	S529	3007.5	173.5	15*100
677	S528	2992.5	292.5	15*100
678	S527	2977.5	173.5	15*100
679	S526	2962.5	292.5	15*100
680	S525	2947.5	173.5	15*100
681	S524	2932.5	292.5	15*100
682	S523	2917.5	173.5	15*100
683	S522	2902.5	292.5	15*100
684	S521	2887.5	173.5	15*100
685	S520	2872.5	292.5	15*100
686	S519	2857.5	173.5	15*100
687	S518	2842.5	292.5	15*100
688	S517	2827.5	173.5	15*100
689	S516	2812.5	292.5	15*100
690	S515	2797.5	173.5	15*100
691	S514	2782.5	292.5	15*100
692	S513	2767.5	173.5	15*100
693	S512	2752.5	292.5	15*100
694	S511	2737.5	173.5	15*100
695	S510	2722.5	292.5	15*100
696	S509	2707.5	173.5	15*100
697	S508	2692.5	292.5	15*100
698	S507	2677.5	173.5	15*100
699	S506	2662.5	292.5	15*100
700	S505	2647.5	173.5	15*100
701	S504	2632.5	292.5	15*100
702	S503	2617.5	173.5	15*100
703	S502	2602.5	292.5	15*100
704	S501	2587.5	173.5	15*100
705	S500	2572.5	292.5	15*100
706	S499	2557.5	173.5	15*100
707	S498	2542.5	292.5	15*100
708	S497	2527.5	173.5	15*100
709	S496	2512.5	292.5	15*100
710	S495	2497.5	173.5	15*100
711	S494	2482.5	292.5	15*100
712	S493	2467.5	173.5	15*100
713	S492	2452.5	292.5	15*100
714	S491	2437.5	173.5	15*100
715	S490	2422.5	292.5	15*100
716	S489	2407.5	173.5	15*100
717	S488	2392.5	292.5	15*100
718	S487	2377.5	173.5	15*100
719	S486	2362.5	292.5	15*100
720	S485	2347.5	173.5	15*100

No.	Name	X	Y	Bump size
721	S484	2332.5	292.5	15*100
722	S483	2317.5	173.5	15*100
723	S482	2302.5	292.5	15*100
724	S481	2287.5	173.5	15*100
725	S480	2272.5	292.5	15*100
726	S479	2257.5	173.5	15*100
727	S478	2242.5	292.5	15*100
728	S477	2227.5	173.5	15*100
729	S476	2212.5	292.5	15*100
730	S475	2197.5	173.5	15*100
731	S474	2182.5	292.5	15*100
732	S473	2167.5	173.5	15*100
733	S472	2152.5	292.5	15*100
734	S471	2137.5	173.5	15*100
735	S470	2122.5	292.5	15*100
736	S469	2107.5	173.5	15*100
737	S468	2092.5	292.5	15*100
738	S467	2077.5	173.5	15*100
739	S466	2062.5	292.5	15*100
740	S465	2047.5	173.5	15*100
741	S464	2032.5	292.5	15*100
742	S463	2017.5	173.5	15*100
743	S462	2002.5	292.5	15*100
744	S461	1987.5	173.5	15*100
745	S460	1972.5	292.5	15*100
746	S459	1957.5	173.5	15*100
747	S458	1942.5	292.5	15*100
748	S457	1927.5	173.5	15*100
749	S456	1912.5	292.5	15*100
750	S455	1897.5	173.5	15*100
751	S454	1882.5	292.5	15*100
752	S453	1867.5	173.5	15*100
753	S452	1852.5	292.5	15*100
754	S451	1837.5	173.5	15*100
755	S450	1822.5	292.5	15*100
756	S449	1807.5	173.5	15*100
757	S448	1792.5	292.5	15*100
758	S447	1777.5	173.5	15*100
759	S446	1762.5	292.5	15*100
760	S445	1747.5	173.5	15*100
761	S444	1732.5	292.5	15*100
762	S443	1717.5	173.5	15*100
763	S442	1702.5	292.5	15*100
764	S441	1687.5	173.5	15*100
765	S440	1672.5	292.5	15*100
766	S439	1657.5	173.5	15*100
767	S438	1642.5	292.5	15*100
768	S437	1627.5	173.5	15*100
769	S436	1612.5	292.5	15*100
770	S435	1597.5	173.5	15*100
771	S434	1582.5	292.5	15*100
772	S433	1567.5	173.5	15*100
773	S432	1552.5	292.5	15*100
774	S431	1537.5	173.5	15*100
775	S430	1522.5	292.5	15*100
776	S429	1507.5	173.5	15*100
777	S428	1492.5	292.5	15*100
778	S427	1477.5	173.5	15*100
779	S426	1462.5	292.5	15*100
780	S425	1447.5	173.5	15*100

No.	Name	X	Y	Bump size
781	S424	1432.5	292.5	15*100
782	S423	1417.5	173.5	15*100
783	S422	1402.5	292.5	15*100
784	S421	1387.5	173.5	15*100
785	S420	1372.5	292.5	15*100
786	S419	1357.5	173.5	15*100
787	S418	1342.5	292.5	15*100
788	S417	1327.5	173.5	15*100
789	S416	1312.5	292.5	15*100
790	S415	1297.5	173.5	15*100
791	S414	1282.5	292.5	15*100
792	S413	1267.5	173.5	15*100
793	S412	1252.5	292.5	15*100
794	S411	1237.5	173.5	15*100
795	S410	1222.5	292.5	15*100
796	S409	1207.5	173.5	15*100
797	S408	1192.5	292.5	15*100
798	S407	1177.5	173.5	15*100
799	S406	1162.5	292.5	15*100
800	S405	1147.5	173.5	15*100
801	S404	1132.5	292.5	15*100
802	S403	1117.5	173.5	15*100
803	S402	1102.5	292.5	15*100
804	S401	1087.5	173.5	15*100
805	S400	1072.5	292.5	15*100
806	S399	1057.5	173.5	15*100
807	S398	1042.5	292.5	15*100
808	S397	1027.5	173.5	15*100
809	S396	1012.5	292.5	15*100
810	S395	997.5	173.5	15*100
811	S394	982.5	292.5	15*100
812	S393	967.5	173.5	15*100
813	S392	952.5	292.5	15*100
814	S391	937.5	173.5	15*100
815	S390	922.5	292.5	15*100
816	S389	907.5	173.5	15*100
817	S388	892.5	292.5	15*100
818	S387	877.5	173.5	15*100
819	S386	862.5	292.5	15*100
820	S385	847.5	173.5	15*100
821	S384	832.5	292.5	15*100
822	S383	817.5	173.5	15*100
823	S382	802.5	292.5	15*100
824	S381	787.5	173.5	15*100
825	S380	772.5	292.5	15*100
826	S379	757.5	173.5	15*100
827	S378	742.5	292.5	15*100
828	S377	727.5	173.5	15*100
829	S376	712.5	292.5	15*100
830	S375	697.5	173.5	15*100
831	S374	682.5	292.5	15*100
832	S373	667.5	173.5	15*100
833	S372	652.5	292.5	15*100
834	S371	637.5	173.5	15*100
835	S370	622.5	292.5	15*100
836	S369	607.5	173.5	15*100
837	S368	592.5	292.5	15*100
838	S367	577.5	173.5	15*100
839	S366	562.5	292.5	15*100
840	S365	547.5	173.5	15*100

No.	Name	X	Y	Bump size
841	S364	532.5	292.5	15*100
842	S363	517.5	173.5	15*100
843	S362	502.5	292.5	15*100
844	S361	487.5	173.5	15*100
845	DUMMY41	472.5	292.5	15*100
846	DUMMY42	457.5	173.5	15*100
847	DUMMY43	442.5	292.5	15*100
848	DUMMY44	427.5	173.5	15*100
849	DUMMY45	-427.5	292.5	15*100
850	DUMMY46	-442.5	173.5	15*100
851	DUMMY47	-457.5	292.5	15*100
852	DUMMY48	-472.5	173.5	15*100
853	S360	-487.5	292.5	15*100
854	S359	-502.5	173.5	15*100
855	S358	-517.5	292.5	15*100
856	S357	-532.5	173.5	15*100
857	S356	-547.5	292.5	15*100
858	S355	-562.5	173.5	15*100
859	S354	-577.5	292.5	15*100
860	S353	-592.5	173.5	15*100
861	S352	-607.5	292.5	15*100
862	S351	-622.5	173.5	15*100
863	S350	-637.5	292.5	15*100
864	S349	-652.5	173.5	15*100
865	S348	-667.5	292.5	15*100
866	S347	-682.5	173.5	15*100
867	S346	-697.5	292.5	15*100
868	S345	-712.5	173.5	15*100
869	S344	-727.5	292.5	15*100
870	S343	-742.5	173.5	15*100
871	S342	-757.5	292.5	15*100
872	S341	-772.5	173.5	15*100
873	S340	-787.5	292.5	15*100
874	S339	-802.5	173.5	15*100
875	S338	-817.5	292.5	15*100
876	S337	-832.5	173.5	15*100
877	S336	-847.5	292.5	15*100
878	S335	-862.5	173.5	15*100
879	S334	-877.5	292.5	15*100
880	S333	-892.5	173.5	15*100
881	S332	-907.5	292.5	15*100
882	S331	-922.5	173.5	15*100
883	S330	-937.5	292.5	15*100
884	S329	-952.5	173.5	15*100
885	S328	-967.5	292.5	15*100
886	S327	-982.5	173.5	15*100
887	S326	-997.5	292.5	15*100
888	S325	-1012.5	173.5	15*100
889	S324	-1027.5	292.5	15*100
890	S323	-1042.5	173.5	15*100
891	S322	-1057.5	292.5	15*100
892	S321	-1072.5	173.5	15*100
893	S320	-1087.5	292.5	15*100
894	S319	-1102.5	173.5	15*100
895	S318	-1117.5	292.5	15*100
896	S317	-1132.5	173.5	15*100
897	S316	-1147.5	292.5	15*100
898	S315	-1162.5	173.5	15*100
899	S314	-1177.5	292.5	15*100
900	S313	-1192.5	173.5	15*100

No.	Name	X	Y	Bump size
901	S312	-1207.5	292.5	15*100
902	S311	-1222.5	173.5	15*100
903	S310	-1237.5	292.5	15*100
904	S309	-1252.5	173.5	15*100
905	S308	-1267.5	292.5	15*100
906	S307	-1282.5	173.5	15*100
907	S306	-1297.5	292.5	15*100
908	S305	-1312.5	173.5	15*100
909	S304	-1327.5	292.5	15*100
910	S303	-1342.5	173.5	15*100
911	S302	-1357.5	292.5	15*100
912	S301	-1372.5	173.5	15*100
913	S300	-1387.5	292.5	15*100
914	S299	-1402.5	173.5	15*100
915	S298	-1417.5	292.5	15*100
916	S297	-1432.5	173.5	15*100
917	S296	-1447.5	292.5	15*100
918	S295	-1462.5	173.5	15*100
919	S294	-1477.5	292.5	15*100
920	S293	-1492.5	173.5	15*100
921	S292	-1507.5	292.5	15*100
922	S291	-1522.5	173.5	15*100
923	S290	-1537.5	292.5	15*100
924	S289	-1552.5	173.5	15*100
925	S288	-1567.5	292.5	15*100
926	S287	-1582.5	173.5	15*100
927	S286	-1597.5	292.5	15*100
928	S285	-1612.5	173.5	15*100
929	S284	-1627.5	292.5	15*100
930	S283	-1642.5	173.5	15*100
931	S282	-1657.5	292.5	15*100
932	S281	-1672.5	173.5	15*100
933	S280	-1687.5	292.5	15*100
934	S279	-1702.5	173.5	15*100
935	S278	-1717.5	292.5	15*100
936	S277	-1732.5	173.5	15*100
937	S276	-1747.5	292.5	15*100
938	S275	-1762.5	173.5	15*100
939	S274	-1777.5	292.5	15*100
940	S273	-1792.5	173.5	15*100
941	S272	-1807.5	292.5	15*100
942	S271	-1822.5	173.5	15*100
943	S270	-1837.5	292.5	15*100
944	S269	-1852.5	173.5	15*100
945	S268	-1867.5	292.5	15*100
946	S267	-1882.5	173.5	15*100
947	S266	-1897.5	292.5	15*100
948	S265	-1912.5	173.5	15*100
949	S264	-1927.5	292.5	15*100
950	S263	-1942.5	173.5	15*100
951	S262	-1957.5	292.5	15*100
952	S261	-1972.5	173.5	15*100
953	S260	-1987.5	292.5	15*100
954	S259	-2002.5	173.5	15*100
955	S258	-2017.5	292.5	15*100
956	S257	-2032.5	173.5	15*100
957	S256	-2047.5	292.5	15*100
958	S255	-2062.5	173.5	15*100
959	S254	-2077.5	292.5	15*100
960	S253	-2092.5	173.5	15*100

No.	Name	X	Y	Bump size
961	S252	-2107.5	292.5	15*100
962	S251	-2122.5	173.5	15*100
963	S250	-2137.5	292.5	15*100
964	S249	-2152.5	173.5	15*100
965	S248	-2167.5	292.5	15*100
966	S247	-2182.5	173.5	15*100
967	S246	-2197.5	292.5	15*100
968	S245	-2212.5	173.5	15*100
969	S244	-2227.5	292.5	15*100
970	S243	-2242.5	173.5	15*100
971	S242	-2257.5	292.5	15*100
972	S241	-2272.5	173.5	15*100
973	S240	-2287.5	292.5	15*100
974	S239	-2302.5	173.5	15*100
975	S238	-2317.5	292.5	15*100
976	S237	-2332.5	173.5	15*100
977	S236	-2347.5	292.5	15*100
978	S235	-2362.5	173.5	15*100
979	S234	-2377.5	292.5	15*100
980	S233	-2392.5	173.5	15*100
981	S232	-2407.5	292.5	15*100
982	S231	-2422.5	173.5	15*100
983	S230	-2437.5	292.5	15*100
984	S229	-2452.5	173.5	15*100
985	S228	-2467.5	292.5	15*100
986	S227	-2482.5	173.5	15*100
987	S226	-2497.5	292.5	15*100
988	S225	-2512.5	173.5	15*100
989	S224	-2527.5	292.5	15*100
990	S223	-2542.5	173.5	15*100
991	S222	-2557.5	292.5	15*100
992	S221	-2572.5	173.5	15*100
993	S220	-2587.5	292.5	15*100
994	S219	-2602.5	173.5	15*100
995	S218	-2617.5	292.5	15*100
996	S217	-2632.5	173.5	15*100
997	S216	-2647.5	292.5	15*100
998	S215	-2662.5	173.5	15*100
999	S214	-2677.5	292.5	15*100
1000	S213	-2692.5	173.5	15*100
1001	S212	-2707.5	292.5	15*100
1002	S211	-2722.5	173.5	15*100
1003	S210	-2737.5	292.5	15*100
1004	S209	-2752.5	173.5	15*100
1005	S208	-2767.5	292.5	15*100
1006	S207	-2782.5	173.5	15*100
1007	S206	-2797.5	292.5	15*100
1008	S205	-2812.5	173.5	15*100
1009	S204	-2827.5	292.5	15*100
1010	S203	-2842.5	173.5	15*100
1011	S202	-2857.5	292.5	15*100
1012	S201	-2872.5	173.5	15*100
1013	S200	-2887.5	292.5	15*100
1014	S199	-2902.5	173.5	15*100
1015	S198	-2917.5	292.5	15*100
1016	S197	-2932.5	173.5	15*100
1017	S196	-2947.5	292.5	15*100
1018	S195	-2962.5	173.5	15*100
1019	S194	-2977.5	292.5	15*100
1020	S193	-2992.5	173.5	15*100

No.	Name	X	Y	Bump size
1021	S192	-3007.5	292.5	15*100
1022	S191	-3022.5	173.5	15*100
1023	S190	-3037.5	292.5	15*100
1024	S189	-3052.5	173.5	15*100
1025	S188	-3067.5	292.5	15*100
1026	S187	-3082.5	173.5	15*100
1027	S186	-3097.5	292.5	15*100
1028	S185	-3112.5	173.5	15*100
1029	S184	-3127.5	292.5	15*100
1030	S183	-3142.5	173.5	15*100
1031	S182	-3157.5	292.5	15*100
1032	S181	-3172.5	173.5	15*100
1033	S180	-3187.5	292.5	15*100
1034	S179	-3202.5	173.5	15*100
1035	S178	-3217.5	292.5	15*100
1036	S177	-3232.5	173.5	15*100
1037	S176	-3247.5	292.5	15*100
1038	S175	-3262.5	173.5	15*100
1039	S174	-3277.5	292.5	15*100
1040	S173	-3292.5	173.5	15*100
1041	S172	-3307.5	292.5	15*100
1042	S171	-3322.5	173.5	15*100
1043	S170	-3337.5	292.5	15*100
1044	S169	-3352.5	173.5	15*100
1045	S168	-3367.5	292.5	15*100
1046	S167	-3382.5	173.5	15*100
1047	S166	-3397.5	292.5	15*100
1048	S165	-3412.5	173.5	15*100
1049	S164	-3427.5	292.5	15*100
1050	S163	-3442.5	173.5	15*100
1051	S162	-3457.5	292.5	15*100
1052	S161	-3472.5	173.5	15*100
1053	S160	-3487.5	292.5	15*100
1054	S159	-3502.5	173.5	15*100
1055	S158	-3517.5	292.5	15*100
1056	S157	-3532.5	173.5	15*100
1057	S156	-3547.5	292.5	15*100
1058	S155	-3562.5	173.5	15*100
1059	S154	-3577.5	292.5	15*100
1060	S153	-3592.5	173.5	15*100
1061	S152	-3607.5	292.5	15*100
1062	S151	-3622.5	173.5	15*100
1063	S150	-3637.5	292.5	15*100
1064	S149	-3652.5	173.5	15*100
1065	S148	-3667.5	292.5	15*100
1066	S147	-3682.5	173.5	15*100
1067	S146	-3697.5	292.5	15*100
1068	S145	-3712.5	173.5	15*100
1069	S144	-3727.5	292.5	15*100
1070	S143	-3742.5	173.5	15*100
1071	S142	-3757.5	292.5	15*100
1072	S141	-3772.5	173.5	15*100
1073	S140	-3787.5	292.5	15*100
1074	S139	-3802.5	173.5	15*100
1075	S138	-3817.5	292.5	15*100
1076	S137	-3832.5	173.5	15*100
1077	S136	-3847.5	292.5	15*100
1078	S135	-3862.5	173.5	15*100
1079	S134	-3877.5	292.5	15*100
1080	S133	-3892.5	173.5	15*100

No.	Name	X	Y	Bump size
1081	S132	-3907.5	292.5	15*100
1082	S131	-3922.5	173.5	15*100
1083	S130	-3937.5	292.5	15*100
1084	S129	-3952.5	173.5	15*100
1085	S128	-3967.5	292.5	15*100
1086	S127	-3982.5	173.5	15*100
1087	S126	-3997.5	292.5	15*100
1088	S125	-4012.5	173.5	15*100
1089	S124	-4027.5	292.5	15*100
1090	S123	-4042.5	173.5	15*100
1091	S122	-4057.5	292.5	15*100
1092	S121	-4072.5	173.5	15*100
1093	S120	-4087.5	292.5	15*100
1094	S119	-4102.5	173.5	15*100
1095	S118	-4117.5	292.5	15*100
1096	S117	-4132.5	173.5	15*100
1097	S116	-4147.5	292.5	15*100
1098	S115	-4162.5	173.5	15*100
1099	S114	-4177.5	292.5	15*100
1100	S113	-4192.5	173.5	15*100
1101	S112	-4207.5	292.5	15*100
1102	S111	-4222.5	173.5	15*100
1103	S110	-4237.5	292.5	15*100
1104	S109	-4252.5	173.5	15*100
1105	S108	-4267.5	292.5	15*100
1106	S107	-4282.5	173.5	15*100
1107	S106	-4297.5	292.5	15*100
1108	S105	-4312.5	173.5	15*100
1109	S104	-4327.5	292.5	15*100
1110	S103	-4342.5	173.5	15*100
1111	S102	-4357.5	292.5	15*100
1112	S101	-4372.5	173.5	15*100
1113	S100	-4387.5	292.5	15*100
1114	S99	-4402.5	173.5	15*100
1115	S98	-4417.5	292.5	15*100
1116	S97	-4432.5	173.5	15*100
1117	S96	-4447.5	292.5	15*100
1118	S95	-4462.5	173.5	15*100
1119	S94	-4477.5	292.5	15*100
1120	S93	-4492.5	173.5	15*100
1121	S92	-4507.5	292.5	15*100
1122	S91	-4522.5	173.5	15*100
1123	S90	-4537.5	292.5	15*100
1124	S89	-4552.5	173.5	15*100
1125	S88	-4567.5	292.5	15*100
1126	S87	-4582.5	173.5	15*100
1127	S86	-4597.5	292.5	15*100
1128	S85	-4612.5	173.5	15*100
1129	S84	-4627.5	292.5	15*100
1130	S83	-4642.5	173.5	15*100
1131	S82	-4657.5	292.5	15*100
1132	S81	-4672.5	173.5	15*100
1133	S80	-4687.5	292.5	15*100
1134	S79	-4702.5	173.5	15*100
1135	S78	-4717.5	292.5	15*100
1136	S77	-4732.5	173.5	15*100
1137	S76	-4747.5	292.5	15*100
1138	S75	-4762.5	173.5	15*100
1139	S74	-4777.5	292.5	15*100
1140	S73	-4792.5	173.5	15*100
1141	S72	-4807.5	292.5	15*100
1142	S71	-4822.5	173.5	15*100
1143	S70	-4837.5	292.5	15*100
1144	S69	-4852.5	173.5	15*100
1145	S68	-4867.5	292.5	15*100
1146	S67	-4882.5	173.5	15*100
1147	S66	-4897.5	292.5	15*100
1148	S65	-4912.5	173.5	15*100
1149	S64	-4927.5	292.5	15*100
1150	S63	-4942.5	173.5	15*100
1151	S62	-4957.5	292.5	15*100
1152	S61	-4972.5	173.5	15*100
1153	S60	-4987.5	292.5	15*100
1154	S59	-5002.5	173.5	15*100
1155	S58	-5017.5	292.5	15*100
1156	S57	-5032.5	173.5	15*100
1157	S56	-5047.5	292.5	15*100
1158	S55	-5062.5	173.5	15*100
1159	S54	-5077.5	292.5	15*100
1160	S53	-5092.5	173.5	15*100
1161	S52	-5107.5	292.5	15*100
1162	S51	-5122.5	173.5	15*100
1163	S50	-5137.5	292.5	15*100
1164	S49	-5152.5	173.5	15*100
1165	S48	-5167.5	292.5	15*100
1166	S47	-5182.5	173.5	15*100
1167	S46	-5197.5	292.5	15*100
1168	S45	-5212.5	173.5	15*100
1169	S44	-5227.5	292.5	15*100
1170	S43	-5242.5	173.5	15*100
1171	S42	-5257.5	292.5	15*100
1172	S41	-5272.5	173.5	15*100
1173	S40	-5287.5	292.5	15*100
1174	S39	-5302.5	173.5	15*100
1175	S38	-5317.5	292.5	15*100
1176	S37	-5332.5	173.5	15*100
1177	S36	-5347.5	292.5	15*100
1178	S35	-5362.5	173.5	15*100
1179	S34	-5377.5	292.5	15*100
1180	S33	-5392.5	173.5	15*100
1181	S32	-5407.5	292.5	15*100
1182	S31	-5422.5	173.5	15*100
1183	S30	-5437.5	292.5	15*100
1184	S29	-5452.5	173.5	15*100
1185	S28	-5467.5	292.5	15*100
1186	S27	-5482.5	173.5	15*100
1187	S26	-5497.5	292.5	15*100
1188	S25	-5512.5	173.5	15*100
1189	S24	-5527.5	292.5	15*100
1190	S23	-5542.5	173.5	15*100
1191	S22	-5557.5	292.5	15*100
1192	S21	-5572.5	173.5	15*100
1193	S20	-5587.5	292.5	15*100
1194	S19	-5602.5	173.5	15*100
1195	S18	-5617.5	292.5	15*100
1196	S17	-5632.5	173.5	15*100
1197	S16	-5647.5	292.5	15*100
1198	S15	-5662.5	173.5	15*100
1199	S14	-5677.5	292.5	15*100
1200	S13	-5692.5	173.5	15*100
1201	S12	-5707.5	292.5	15*100
1202	S11	-5722.5	173.5	15*100
1203	S10	-5737.5	292.5	15*100
1204	S9	-5752.5	173.5	15*100
1205	S8	-5767.5	292.5	15*100
1206	S7	-5782.5	173.5	15*100
1207	S6	-5797.5	292.5	15*100
1208	S5	-5812.5	173.5	15*100
1209	S4	-5827.5	292.5	15*100
1210	S3	-5842.5	173.5	15*100
1211	S2	-5857.5	292.5	15*100
1212	S1	-5872.5	173.5	15*100
1213	DUMMY49	-5887.5	292.5	15*100
1214	VGL	-6097.5	292.5	15*100
1215	G431	-6112.5	173.5	15*100
1216	G429	-6127.5	292.5	15*100
1217	G427	-6142.5	173.5	15*100
1218	G425	-6157.5	292.5	15*100
1219	G423	-6172.5	173.5	15*100
1220	G421	-6187.5	292.5	15*100
1221	G419	-6202.5	173.5	15*100
1222	G417	-6217.5	292.5	15*100
1223	G415	-6232.5	173.5	15*100
1224	G413	-6247.5	292.5	15*100
1225	G411	-6262.5	173.5	15*100
1226	G409	-6277.5	292.5	15*100
1227	G407	-6292.5	173.5	15*100
1228	G405	-6307.5	292.5	15*100
1229	G403	-6322.5	173.5	15*100
1230	G401	-6337.5	292.5	15*100
1231	G399	-6352.5	173.5	15*100
1232	G397	-6367.5	292.5	15*100
1233	G395	-6382.5	173.5	15*100
1234	G393	-6397.5	292.5	15*100
1235	G391	-6412.5	173.5	15*100
1236	G389	-6427.5	292.5	15*100
1237	G387	-6442.5	173.5	15*100
1238	G385	-6457.5	292.5	15*100
1239	G383	-6472.5	173.5	15*100
1240	G381	-6487.5	292.5	15*100
1241	G379	-6502.5	173.5	15*100
1242	G377	-6517.5	292.5	15*100
1243	G375	-6532.5	173.5	15*100
1244	G373	-6547.5	292.5	15*100
1245	G371	-6562.5	173.5	15*100
1246	G369	-6577.5	292.5	15*100
1247	G367	-6592.5	173.5	15*100
1248	G365	-6607.5	292.5	15*100
1249	G363	-6622.5	173.5	15*100
1250	G361	-6637.5	292.5	15*100
1251	G359	-6652.5	173.5	15*100
1252	G357	-6667.5	292.5	15*100
1253	G355	-6682.5	173.5	15*100
1254	G353	-6697.5	292.5	15*100
1255	G351	-6712.5	173.5	15*100
1256	G349	-6727.5	292.5	15*100
1257	G347	-6742.5	173.5	15*100
1258	G345	-6757.5	292.5	15*100
1259	G343	-6772.5	173.5	15*100
1260	G341	-6787.5	292.5	15*100

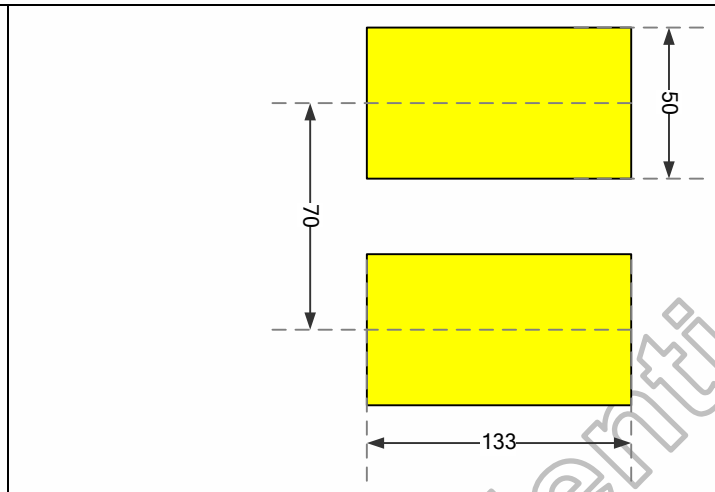
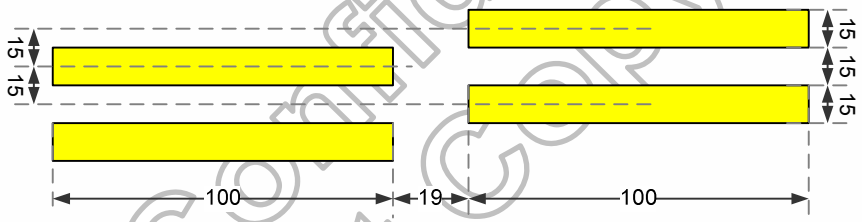
No.	Name	X	Y	Bump size
1261	G339	-6802.5	173.5	15*100
1262	G337	-6817.5	292.5	15*100
1263	G335	-6832.5	173.5	15*100
1264	G333	-6847.5	292.5	15*100
1265	G331	-6862.5	173.5	15*100
1266	G329	-6877.5	292.5	15*100
1267	G327	-6892.5	173.5	15*100
1268	G325	-6907.5	292.5	15*100
1269	G323	-6922.5	173.5	15*100
1270	G321	-6937.5	292.5	15*100
1271	G319	-6952.5	173.5	15*100
1272	G317	-6967.5	292.5	15*100
1273	G315	-6982.5	173.5	15*100
1274	G313	-6997.5	292.5	15*100
1275	G311	-7012.5	173.5	15*100
1276	G309	-7027.5	292.5	15*100
1277	G307	-7042.5	173.5	15*100
1278	G305	-7057.5	292.5	15*100
1279	G303	-7072.5	173.5	15*100
1280	G301	-7087.5	292.5	15*100
1281	G299	-7102.5	173.5	15*100
1282	G297	-7117.5	292.5	15*100
1283	G295	-7132.5	173.5	15*100
1284	G293	-7147.5	292.5	15*100
1285	G291	-7162.5	173.5	15*100
1286	G289	-7177.5	292.5	15*100
1287	G287	-7192.5	173.5	15*100
1288	G285	-7207.5	292.5	15*100
1289	G283	-7222.5	173.5	15*100
1290	G281	-7237.5	292.5	15*100
1291	G279	-7252.5	173.5	15*100
1292	G277	-7267.5	292.5	15*100
1293	G275	-7282.5	173.5	15*100
1294	G273	-7297.5	292.5	15*100
1295	G271	-7312.5	173.5	15*100
1296	G269	-7327.5	292.5	15*100
1297	G267	-7342.5	173.5	15*100
1298	G265	-7357.5	292.5	15*100
1299	G263	-7372.5	173.5	15*100
1300	G261	-7387.5	292.5	15*100
1301	G259	-7402.5	173.5	15*100
1302	G257	-7417.5	292.5	15*100
1303	G255	-7432.5	173.5	15*100
1304	G253	-7447.5	292.5	15*100
1305	G251	-7462.5	173.5	15*100
1306	G249	-7477.5	292.5	15*100
1307	G247	-7492.5	173.5	15*100
1308	G245	-7507.5	292.5	15*100
1309	G243	-7522.5	173.5	15*100
1310	G241	-7537.5	292.5	15*100
1311	G239	-7552.5	173.5	15*100
1312	G237	-7567.5	292.5	15*100
1313	G235	-7582.5	173.5	15*100
1314	G233	-7597.5	292.5	15*100
1315	G231	-7612.5	173.5	15*100
1316	G229	-7627.5	292.5	15*100
1317	G227	-7642.5	173.5	15*100
1318	G225	-7657.5	292.5	15*100
1319	G223	-7672.5	173.5	15*100
1320	G221	-7687.5	292.5	15*100

No.	Name	X	Y	Bump size
1321	G219	-7702.5	173.5	15*100
1322	G217	-7717.5	292.5	15*100
1323	G215	-7732.5	173.5	15*100
1324	G213	-7747.5	292.5	15*100
1325	G211	-7762.5	173.5	15*100
1326	G209	-7777.5	292.5	15*100
1327	G207	-7792.5	173.5	15*100
1328	G205	-7807.5	292.5	15*100
1329	G203	-7822.5	173.5	15*100
1330	G201	-7837.5	292.5	15*100
1331	G199	-7852.5	173.5	15*100
1332	G197	-7867.5	292.5	15*100
1333	G195	-7882.5	173.5	15*100
1334	G193	-7897.5	292.5	15*100
1335	G191	-7912.5	173.5	15*100
1336	G189	-7927.5	292.5	15*100
1337	G187	-7942.5	173.5	15*100
1338	G185	-7957.5	292.5	15*100
1339	G183	-7972.5	173.5	15*100
1340	G181	-7987.5	292.5	15*100
1341	G179	-8002.5	173.5	15*100
1342	G177	-8017.5	292.5	15*100
1343	G175	-8032.5	173.5	15*100
1344	G173	-8047.5	292.5	15*100
1345	G171	-8062.5	173.5	15*100
1346	G169	-8077.5	292.5	15*100
1347	G167	-8092.5	173.5	15*100
1348	G165	-8107.5	292.5	15*100
1349	G163	-8122.5	173.5	15*100
1350	G161	-8137.5	292.5	15*100
1351	G159	-8152.5	173.5	15*100
1352	G157	-8167.5	292.5	15*100
1353	G155	-8182.5	173.5	15*100
1354	G153	-8197.5	292.5	15*100
1355	G151	-8212.5	173.5	15*100
1356	G149	-8227.5	292.5	15*100
1357	G147	-8242.5	173.5	15*100
1358	G145	-8257.5	292.5	15*100
1359	G143	-8272.5	173.5	15*100
1360	G141	-8287.5	292.5	15*100
1361	G139	-8302.5	173.5	15*100
1362	G137	-8317.5	292.5	15*100
1363	G135	-8332.5	173.5	15*100
1364	G133	-8347.5	292.5	15*100
1365	G131	-8362.5	173.5	15*100
1366	G129	-8377.5	292.5	15*100
1367	G127	-8392.5	173.5	15*100
1368	G125	-8407.5	292.5	15*100
1369	G123	-8422.5	173.5	15*100
1370	G121	-8437.5	292.5	15*100
1371	G119	-8452.5	173.5	15*100
1372	G117	-8467.5	292.5	15*100
1373	G115	-8482.5	173.5	15*100
1374	G113	-8497.5	292.5	15*100
1375	G111	-8512.5	173.5	15*100
1376	G109	-8527.5	292.5	15*100
1377	G107	-8542.5	173.5	15*100
1378	G105	-8557.5	292.5	15*100
1379	G103	-8572.5	173.5	15*100
1380	G101	-8587.5	292.5	15*100

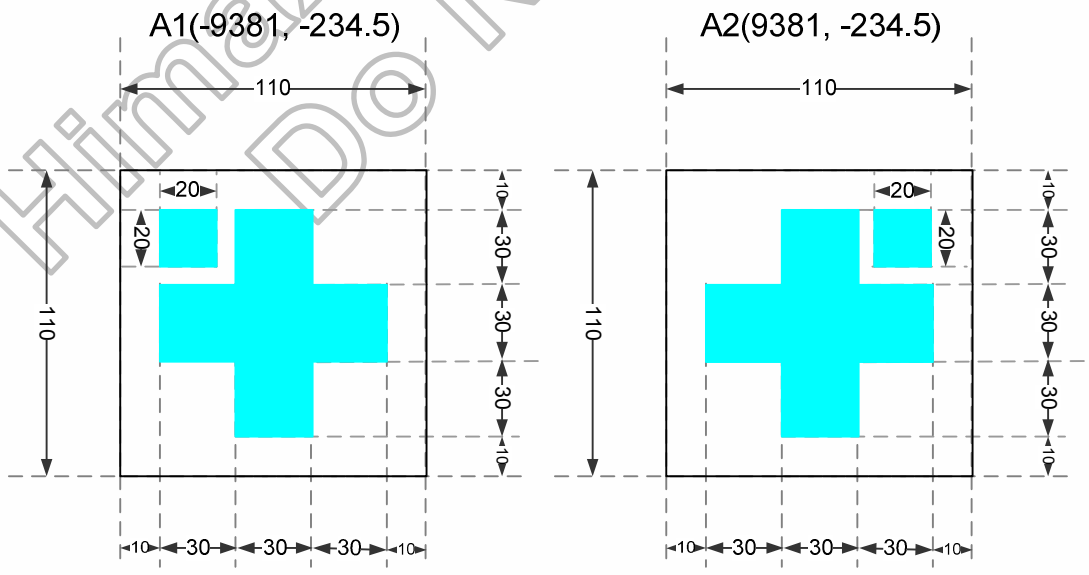
No.	Name	X	Y	Bump size
1381	G99	-8602.5	173.5	15*100
1382	G97	-8617.5	292.5	15*100
1383	G95	-8632.5	173.5	15*100
1384	G93	-8647.5	292.5	15*100
1385	G91	-8662.5	173.5	15*100
1386	G89	-8677.5	292.5	15*100
1387	G87	-8692.5	173.5	15*100
1388	G85	-8707.5	292.5	15*100
1389	G83	-8722.5	173.5	15*100
1390	G81	-8737.5	292.5	15*100
1391	G79	-8752.5	173.5	15*100
1392	G77	-8767.5	292.5	15*100
1393	G75	-8782.5	173.5	15*100
1394	G73	-8797.5	292.5	15*100
1395	G71	-8812.5	173.5	15*100
1396	G69	-8827.5	292.5	15*100
1397	G67	-8842.5	173.5	15*100
1398	G65	-8857.5	292.5	15*100
1399	G63	-8872.5	173.5	15*100
1400	G61	-8887.5	292.5	15*100
1401	G59	-8902.5	173.5	15*100
1402	G57	-8917.5	292.5	15*100
1403	G55	-8932.5	173.5	15*100
1404	G53	-8947.5	292.5	15*100
1405	G51	-8962.5	173.5	15*100
1406	G49	-8977.5	292.5	15*100
1407	G47	-8992.5	173.5	15*100
1408	G45	-9007.5	292.5	15*100
1409	G43	-9022.5	173.5	15*100
1410	G41	-9037.5	292.5	15*100
1411	G39	-9052.5	173.5	15*100
1412	G37	-9067.5	292.5	15*100
1413	G35	-9082.5	173.5	15*100
1414	G33	-9097.5	292.5	15*100
1415	G31	-9112.5	173.5	15*100
1416	G29	-9127.5	292.5	15*100
1417	G27	-9142.5	173.5	15*100
1418	G25	-9157.5	292.5	15*100
1419	G23	-9172.5	173.5	15*100
1420	G21	-9187.5	292.5	15*100
1421	G19	-9202.5	173.5	15*100
1422	G17	-9217.5	292.5	15*100
1423	G15	-9232.5	173.5	15*100
1424	G13	-9247.5	292.5	15*100
1425	G11	-9262.5	173.5	15*100
1426	G9	-9277.5	292.5	15*100
1427	G7	-9292.5	173.5	15*100
1428	G5	-9307.5	292.5	15*100
1429	G3	-9322.5	173.5	15*100
1430	G1	-9337.5	292.5	15*100
1431	VGL	-9352.5	173.5	15*100
1432	DUMMY50	-9367.5	292.5	15*100
1433	DUMMYR2	-9382.5	173.5	15*100
1434	DUMMYR1	-9397.5	292.5	15*100

Alignment Mark	X	Y	
A1	-9381	-234.5	
A2	9381	-234.5	

3.5 Bump arrangement

Input Pad (No.1~262)	 unit: um
Output Pad (No.263~1434)	 unit: um

Alignment Mark



unit: um

4. Interface

4.1 System interface

The HX8352-C01 supports System Interface and RGB Interface. Where System Interface supports 8080 MCU (18-/16-/9-/8-bit) Parallel Interface (Type II) and Serial interface (3-wire/ 4-wire). The interface mode can be selected by IM2-0 pins setting as show in Table 4.1.

IM2	IM1	IM0	Interface	Display data
0	0	0	8080 System TYPE-II 18-bit	GRAM
0	0	1	8080 System TYPE-II 9-bit	GRAM
0	1	0	8080 System TYPE-II 16-bit	GRAM
0	1	1	8080 System TYPE-II 8-bit	GRAM
1	0	ID	3-wire SPI	RGB / GRAM
1	1	X	4-wire SPI	RGB / GRAM

Table 4.1: Interface selection

The HX8352-C01 includes an index register (IR), which is stored the index data of internal control register and GRAM. When DNC="L", the command via 8080 system interface write into register. When DNC="H", GRAM data via R22h register can be written through data bus. When the data is written into the GRAM from the MPU, it is first written into the write-data latch and then automatically written into the GRAM by internal operation. Data is read through the read-data latch when reading from the GRAM.

When data is read from the GRAM to the MPU, it is first read from GRAM to the read-data latch and then data is read to MPU through the read-data latch in next read operation. Therefore, the first read operation data in data bus is invalid, and the second and the following read operation data in data bus is valid.

Interface	NRD	NWR_SCL	DNC	D17–D0 or other input pin
3-wire serial interface	Unused	SCL	Unused	DB17–DB0: 18-bit data bus SDI_SDA, SDO
4-wire serial interface	Unused	SCL	DNC	DB17–DB0: 18-bit data bus SDI_SDA, SDO
8080 System Type II 8-bit	NRD	NWR	DNC	DB9–DB0: Unused, D17–D10: 8-bit data bus
8080 System Type II 9-bit	NRD	NWR	DNC	DB8–DB0: Unused, DB17–DB9: 9-bit data bus
8080 System Type II 16-bit	NRD	NWR	DNC	DB9,DB0: Unused, DB17–DB10,DB8–DB1: 16-bit data bus
8080 System Type II 18-bit	NRD	NWR	DNC	DB17–DB0: 18-bit data bus

Table 4.2: Pin connection based on different interface

4.1.1 8080 System interface

The selection of 8080 System interface is by IM2~IM0 pins. The parallel interface timing diagram is described in Figure 4.1~4.2.

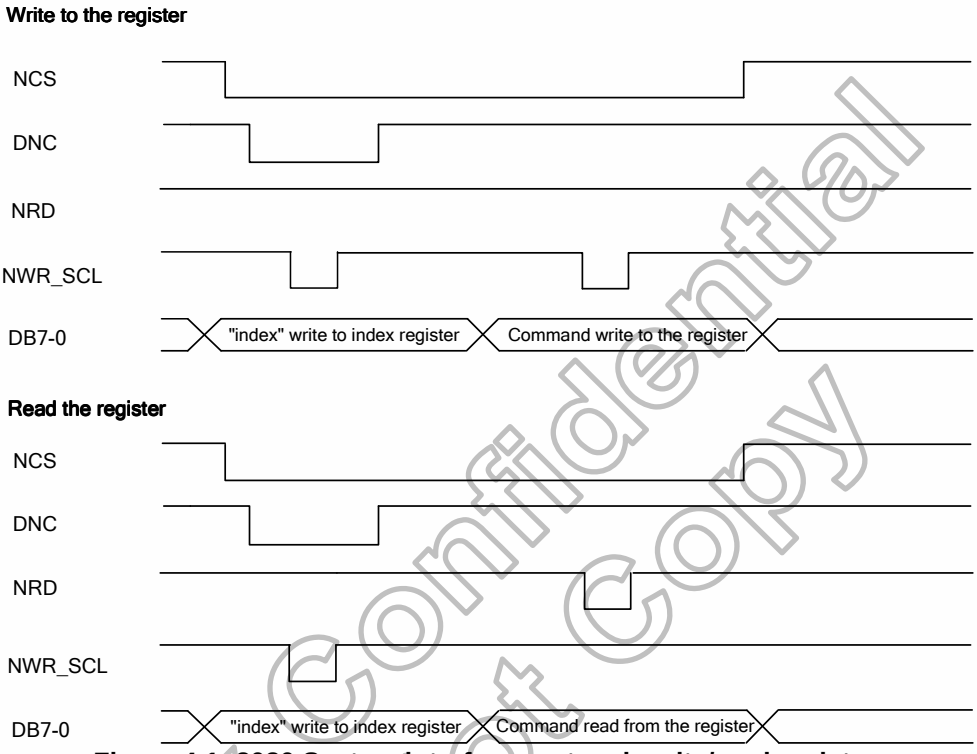


Figure 4.1: 8080 System interface protocol, write/read register

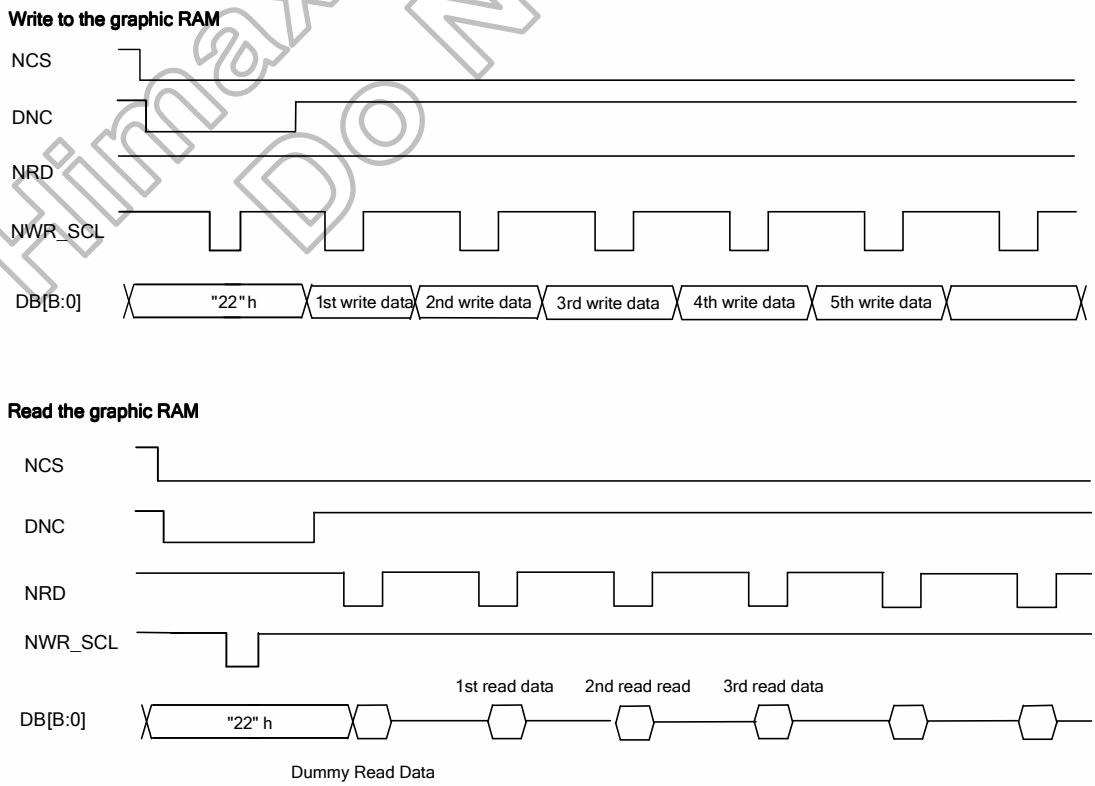


Figure 4.2: 8080 System interface protocol, write/read GRAM

4.1.2 I80 8-bit Parallel Bus System Interface

The I80 8-bit parallel bus interface mode can be used by setting external pins “IM2-0” pins to “011”. Figure 4.3 is the example of I80 8-bit interface

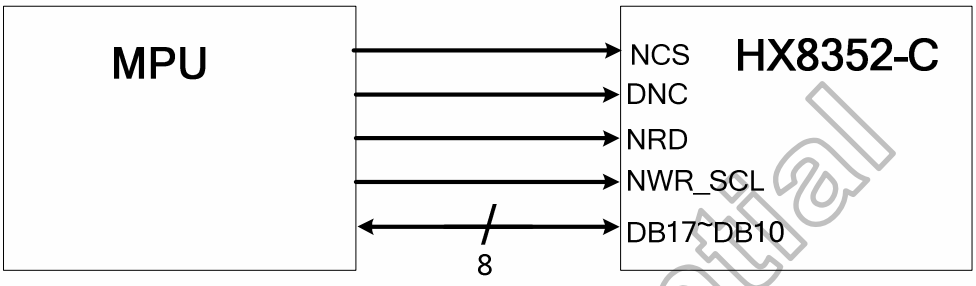


Figure 4.3: Example of I80 8-bit bus interface

8-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 17H=”05h”. There is 1-pixel (3 sub-pixels) per 2-bytes.

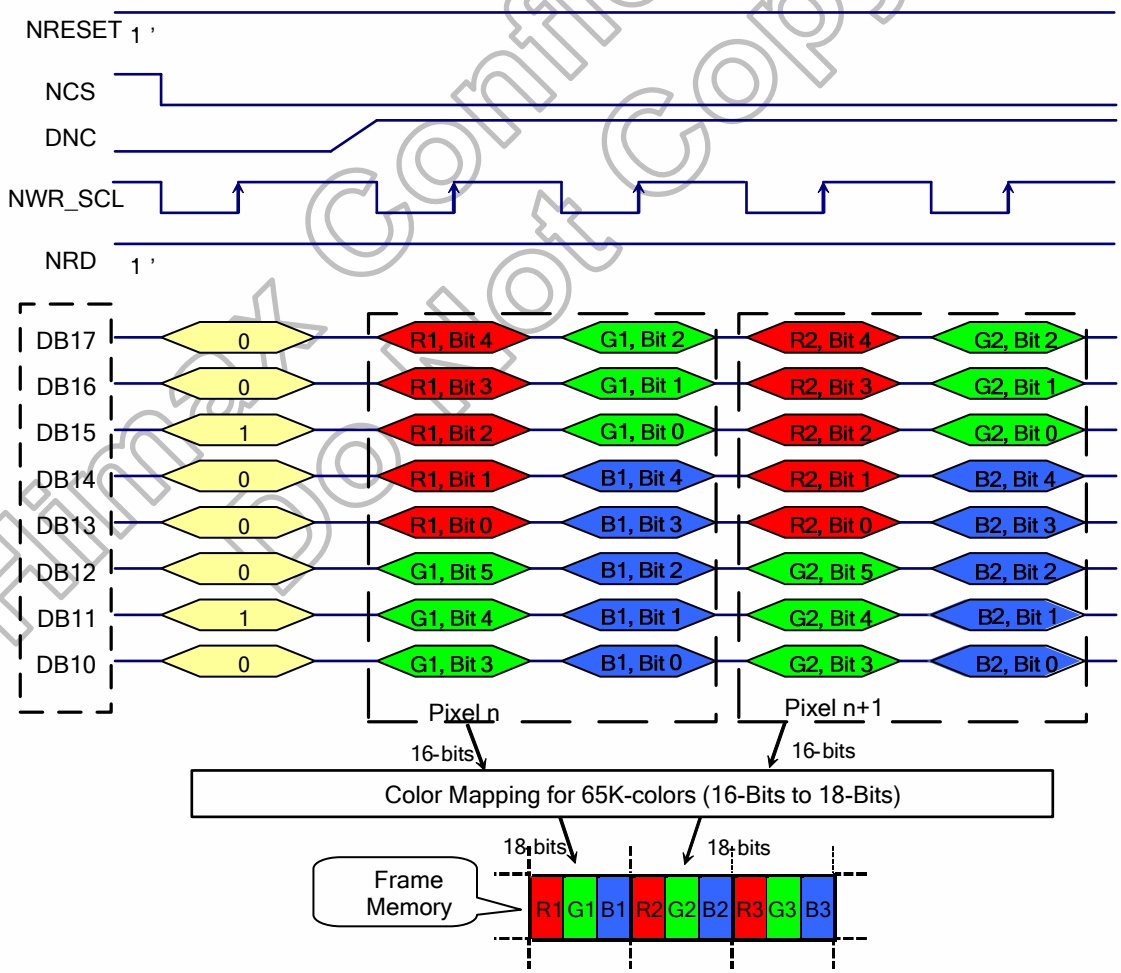


Figure 4.4: Write data for RGB 5-6-5 bits input in I80 8-bit parallel bus interface

8-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h". There is 1-pixel (3 sub-pixels) per 3-bytes.

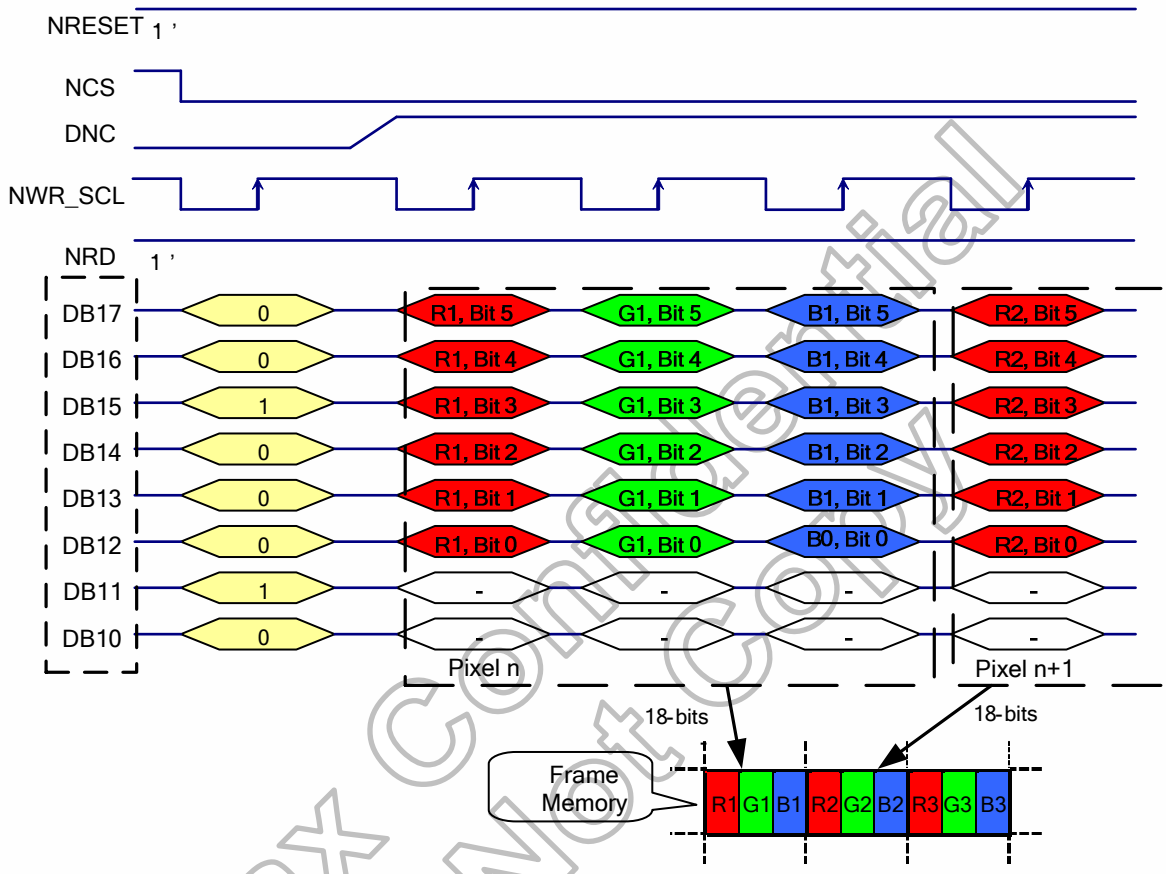


Figure 4.5: Write data for RGB 6-6-6 bits input in I80 8-bit parallel bus interface

4.1.3 I80 9-bit Parallel Bus System Interface

The I80 9-bit parallel bus interface mode can be used by setting external pins “IM2-0” pins to “001”. Figure 4.6 is the example of I80 9-bit interface.

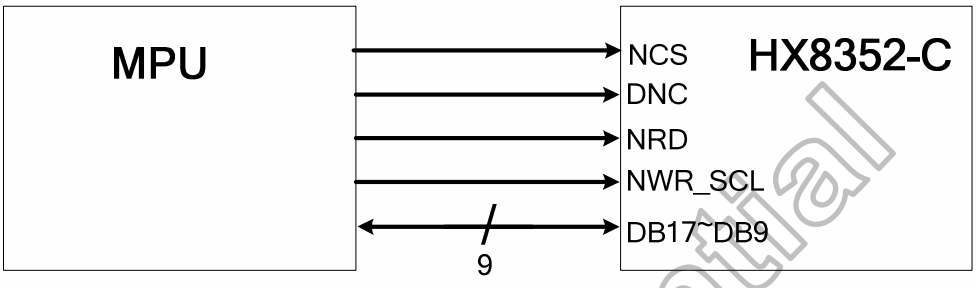


Figure 4.6: Example of I80 9-bit bus interface

9-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H=”06h”. There is 1-pixel (3 sub-pixels) per 2-bytes.

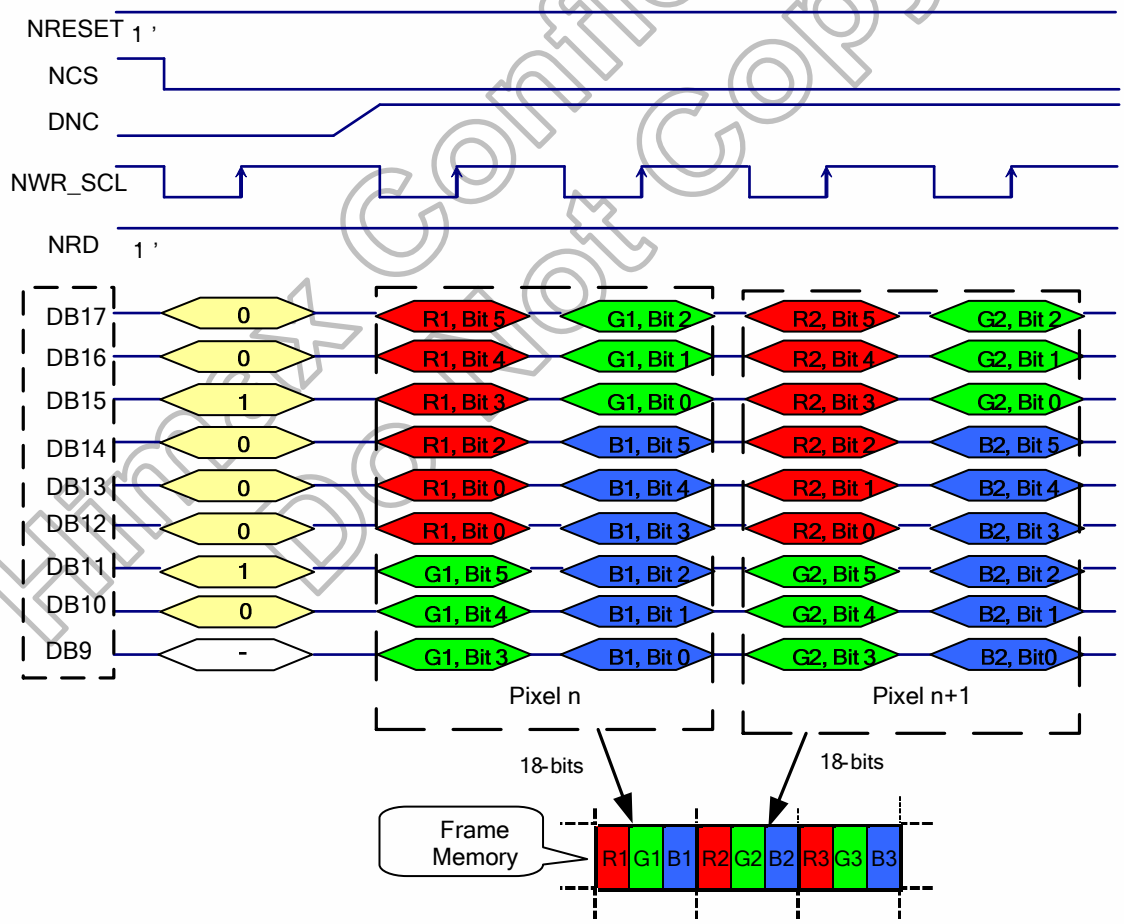


Figure 4.7: Write data for RGB 6-6-6 bits input in I80 9-bit parallel bus interface

4.1.4 I80 16-bit Parallel Bus System Interface

The I80 16-bit parallel bus interface mode can be used by setting external pins “IM2-0”pins to “010”. Figure 4.8 is the example of I80 16-bit interface.

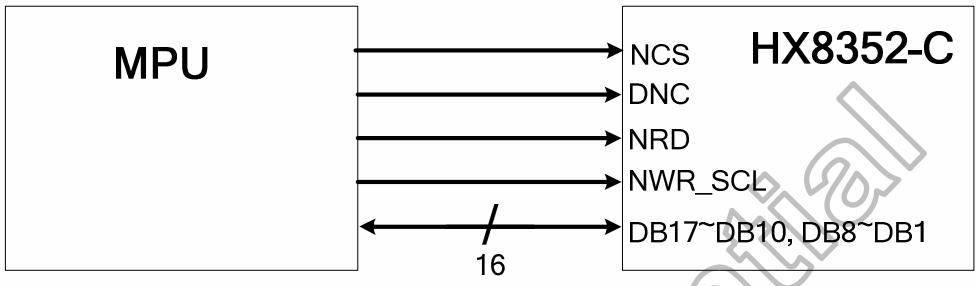


Figure 4.8: Example of I80 16-Bit parallel bus interface

16-bits data bus for 16-bits/pixel (RGB 5-6-5-bits input), 65K-colors, 17H="05h". There is 1-pixel (3 sub-pixels) per 1-byte

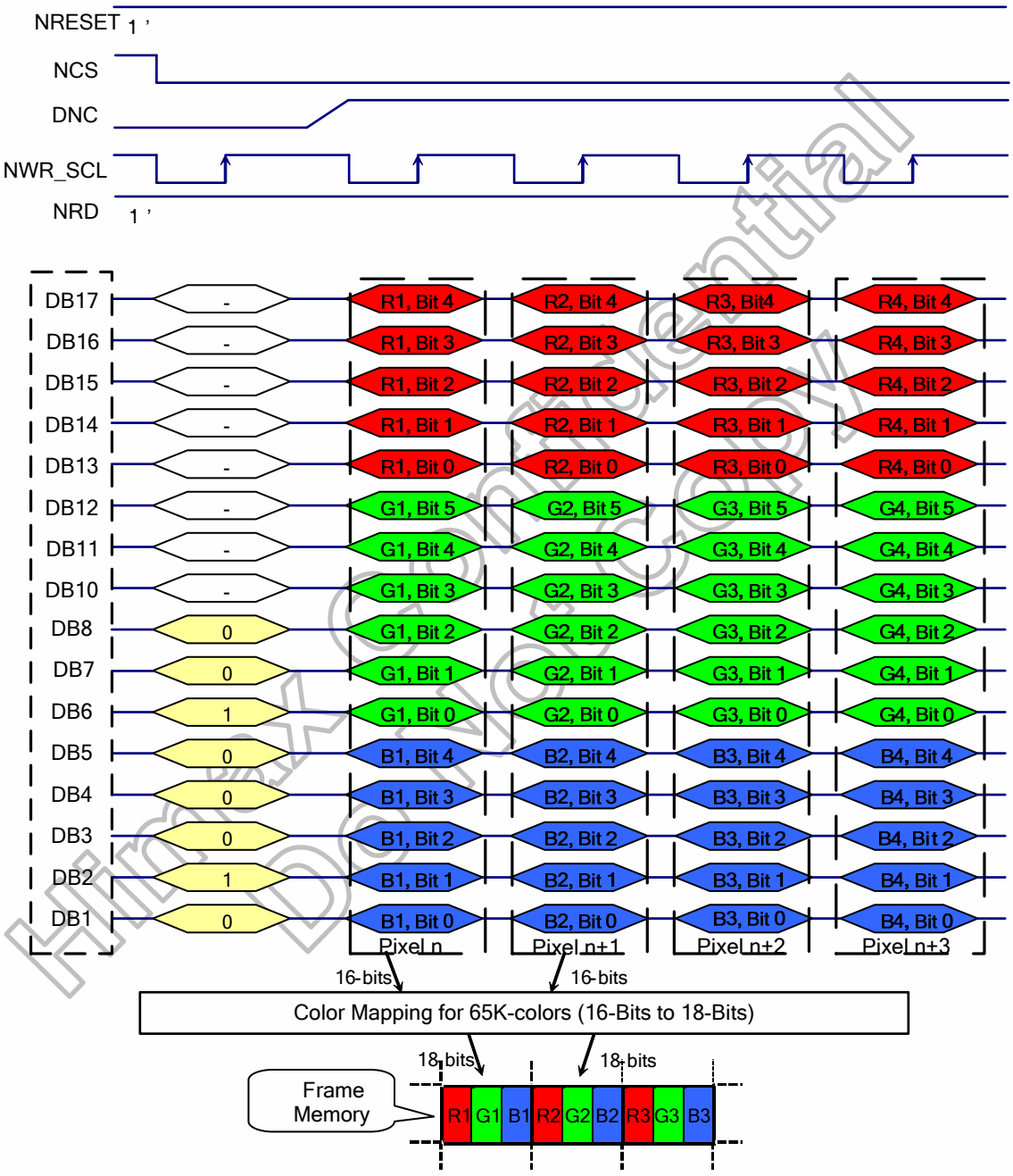


Figure 4.9: Write data for RGB 5-6-5 bits input in I80 16-bit parallel bus interface

16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h". There are 2-pixels (6 sub-pixels) per 3-bytes

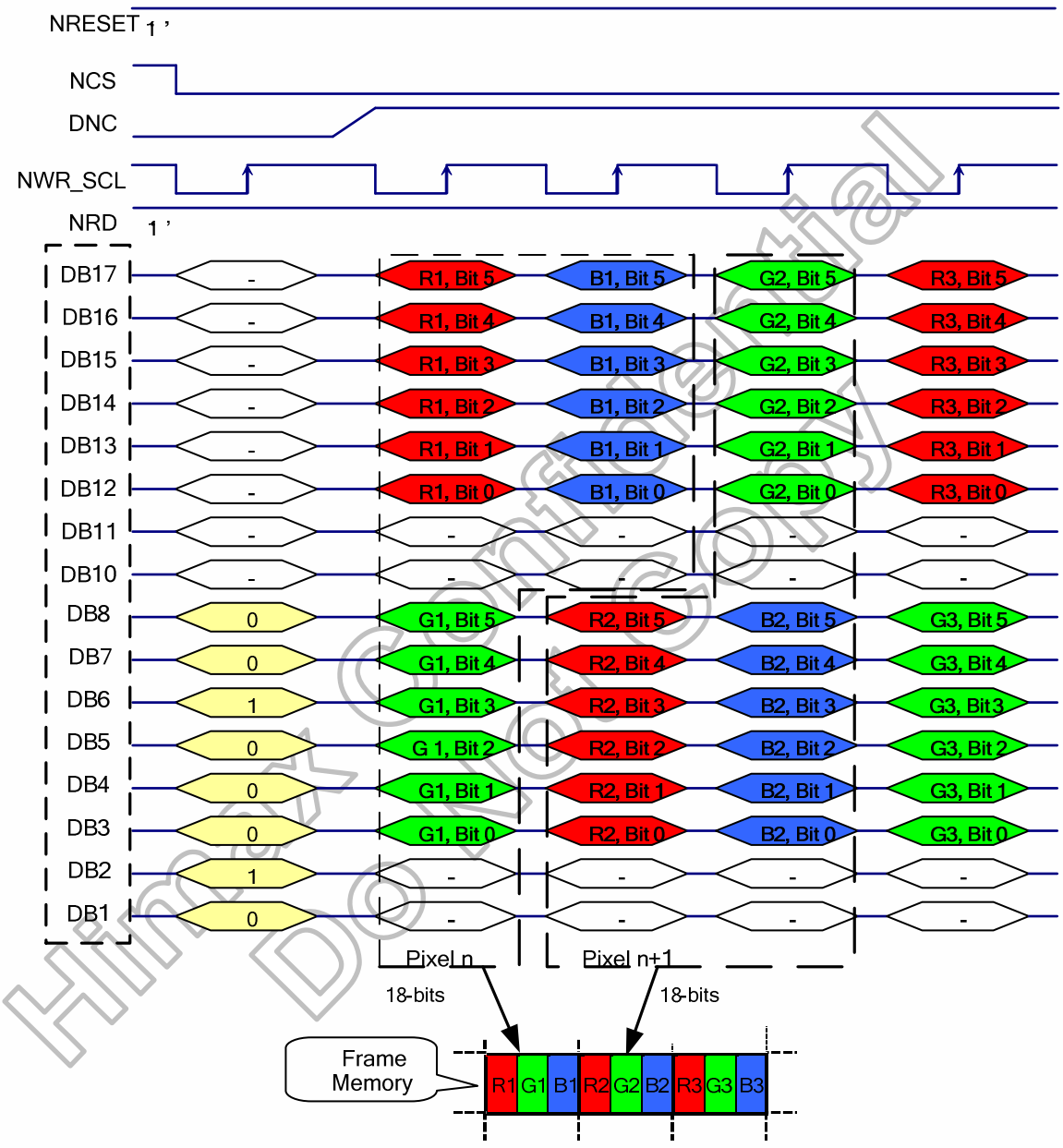


Figure 4.10: Write data for RGB 6-6-6 bits input in I80 16-bit parallel bus interface (DFM=0)

16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="07h". There are 1-pixels (3 sub-pixels) per 2-bytes

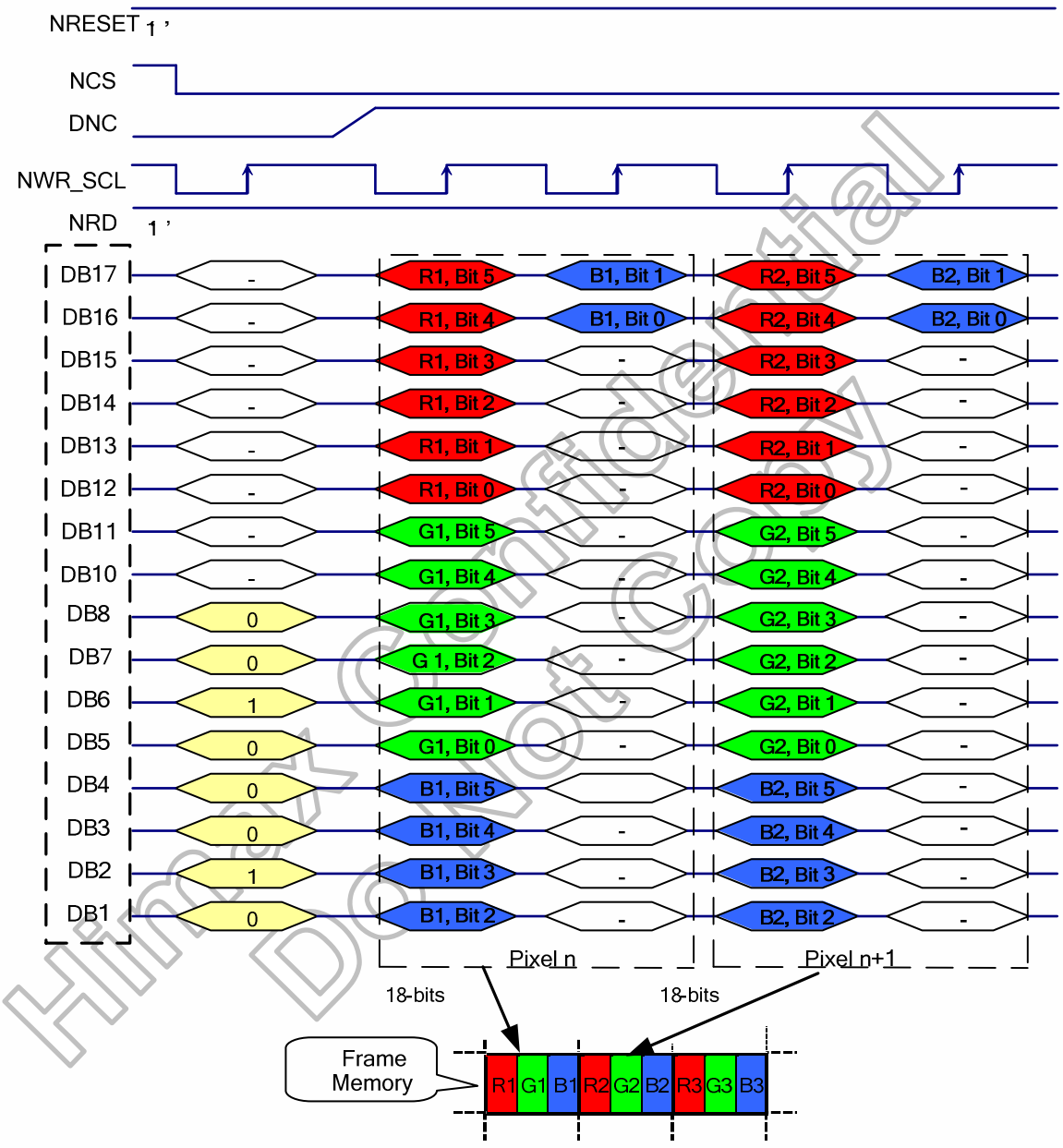


Figure 4.11: Write data for RGB 6-6-6 bits input in I80 16-bit parallel bus interface (R17h=07h)

16-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="04h". There are 1-pixels (3 sub-pixels) per 2-bytes

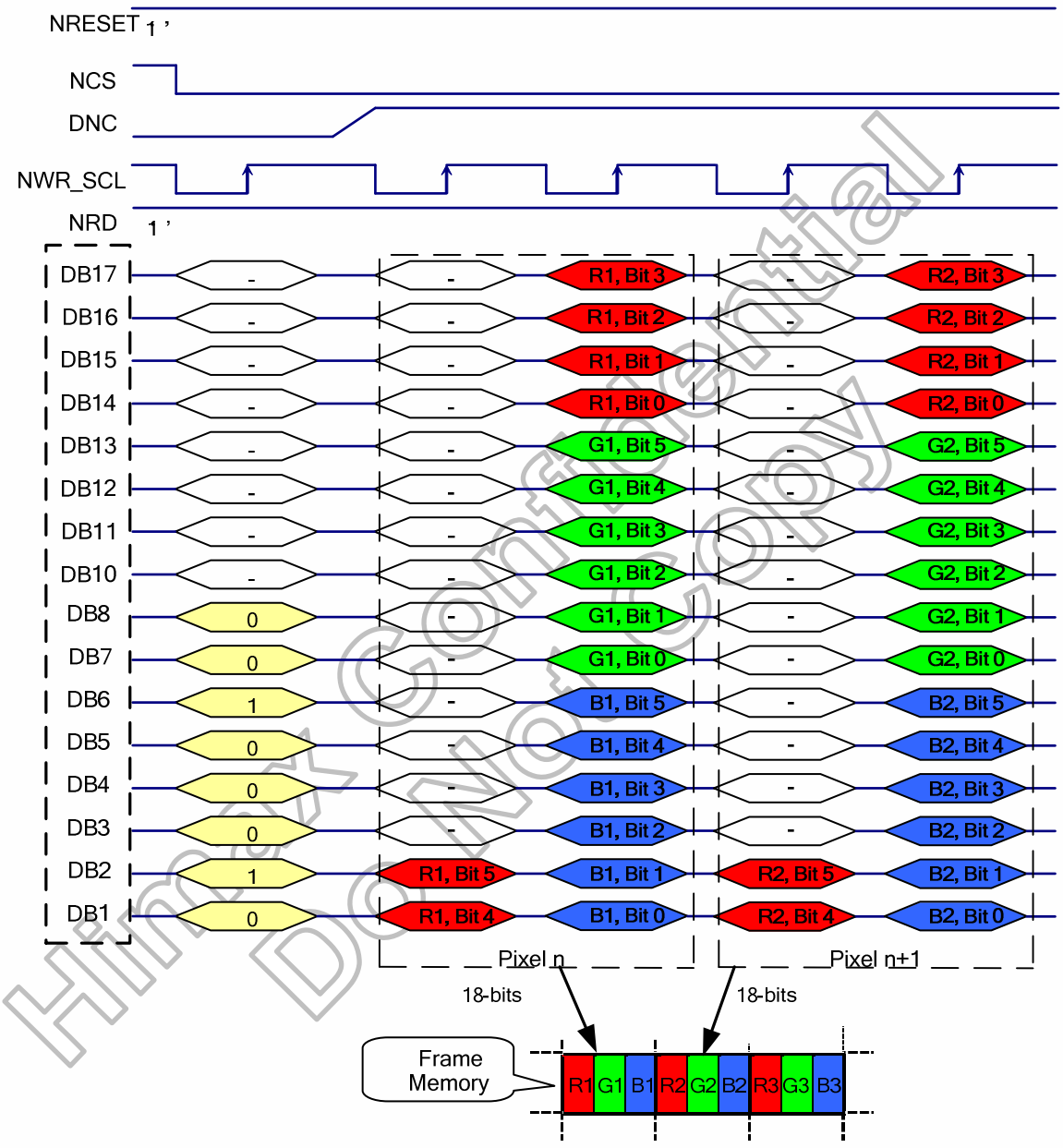


Figure 4.12: Write data for RGB 6-6-6 bits input in I80 16-bit parallel bus interface (R17h=04h)

4.1.5 I80 18-bit Parallel Bus System Interface

The I80 18-bit parallel bus interface mode can be used by setting external pins“IM2-0” pins to “000”. Figure 4.13 is the example of interface with I8018-bit interface.

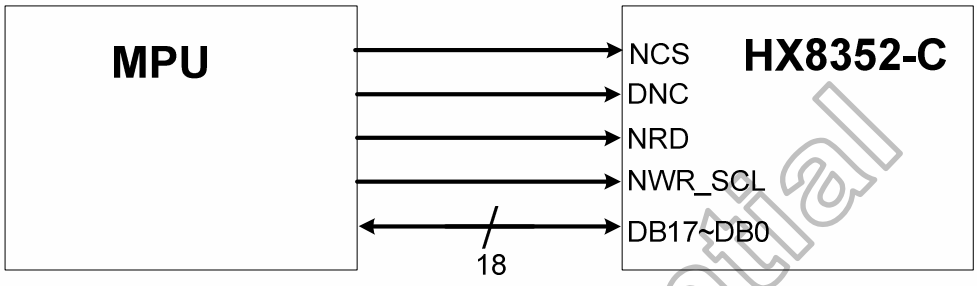


Figure 4.13: Example of I80 18-Bit parallel bus interface

18-bits data bus for 18-bits/pixel (RGB 6-6-6-bits input), 262K-colors, 17H="06h", There is 1-pixel (3 sub-pixels) per 1-byte

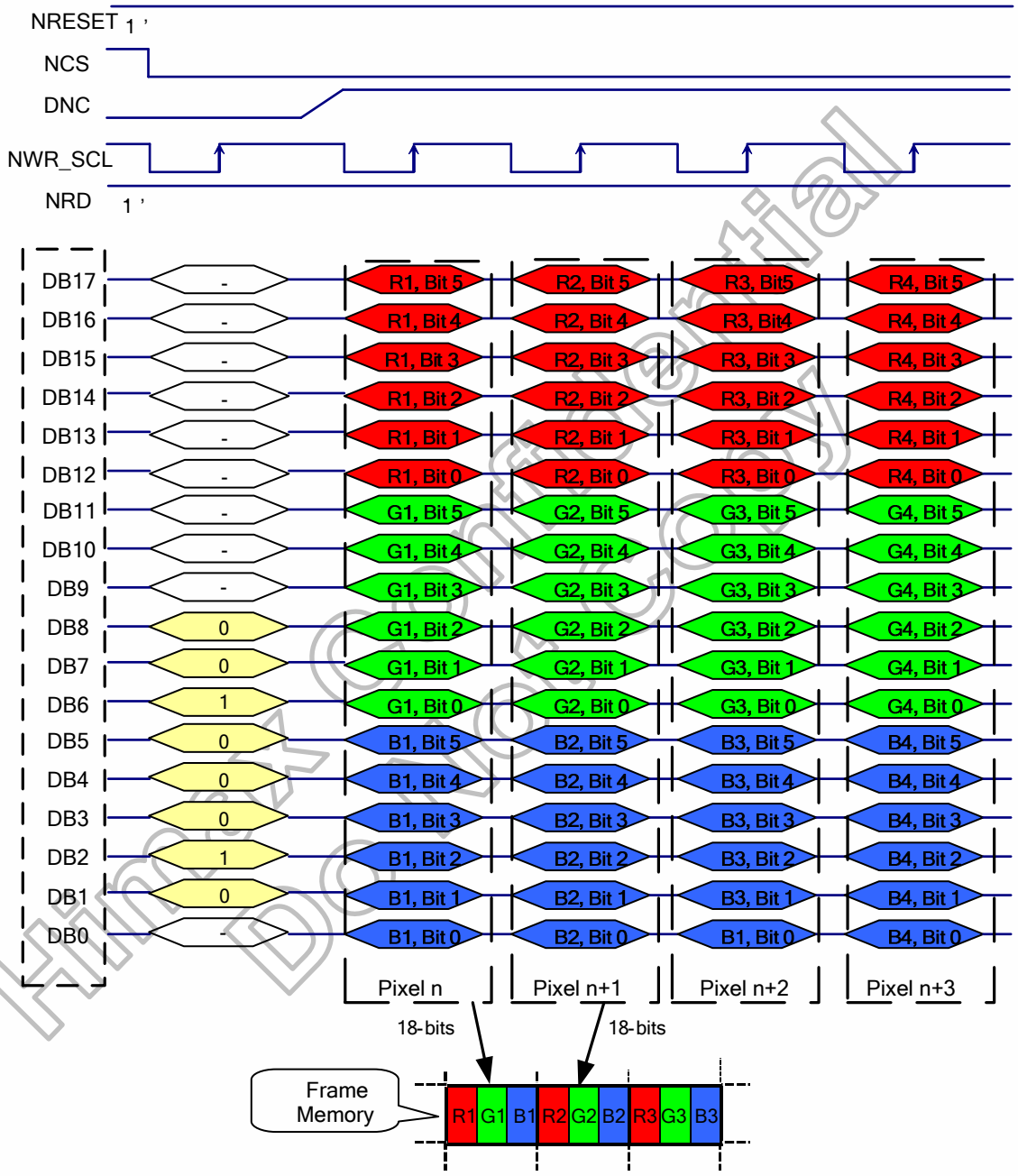


Figure 4.14: Write data for RGB 6-6-6 bits input in I80 18-bit parallel bus interface

I80 Interface Data Color Coding

I80 Interface Data Color Coding for GRAM data ***Write***

- I80 8-Bits Bus Interface (IM2-0="011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22h**
17h	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	x	65K-Color (1-pixels/ 2-bytes)
	G2	G1	G0	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	
06h	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 3bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 4.3: I80 8-Bits Interface GRAM Write Table

- I80 9-Bits Bus Interface (IM2-0="001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22h**
17h	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 4.4: I80 9-Bits Interface GRAM Write Table

- I80 16-Bits Bus Interface (IM2-0="010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22h**
17h	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
05h	R4	R3	R2	R1	R0	G5	G4	G3	x	G2	G1	G0	B4	B3	B2	B1	B0	x	65K-Color
06h	R15	R14	R13	R12	R11	R10	x	x	x	G15	G14	G13	G12	G11	G10	x	x	x	262K-Color (2-pixels/ 3bytes)
	B15	B14	B13	B12	B11	B10	x	x	x	R25	R24	R23	R22	R21	R20	x	x	x	
	G25	G24	G23	G22	G21	G20	x	x	x	B25	B24	B23	B22	B21	B20	x	x	x	
07h	R5	R4	R3	R2	R1	R0	G5	G4	x	G3	G2	G1	G0	B5	B4	B3	B2	x	262K-Color (1-pixels/ 2bytes)
	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
04h	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	R5	R4	x	262K-Color (1-pixels/ 2bytes)
	R3	R2	R1	R0	G5	G4	G3	G2	x	G1	G0	B5	B4	B3	B2	B1	B0	x	

Table 4.5: I80 16-Bits Interface GRAM Write Table

- I80 18-Bits Bus Interface (IM2-0="000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22h**
17h	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
06h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4.6: I80 18-Bits Interface GRAM Write Table

I80 Interface Data Color Coding for GRAM data ***Read***

- I80 8-Bits Bus Interface (IM2-0="011")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22h**
Read Data foramt	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	x	x	x	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 3-bytes)
	G5	G4	G3	G2	G1	G0	x	x	x	x	x	x	x	x	x	x	x	x	
	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	x	x	x	

Table 4.7: I80 8-Bits Interface GRAM Read Table

- I80 9-Bits Bus Interface (IM2-0="001")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	0	0	1	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	**22h**
Read Data foramt	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	x	x	x	x	x	x	x	x	x	262K-Color (1-pixels/ 2bytes)
	G2	G1	G0	B5	B4	B3	B2	B1	B0	x	x	x	x	x	x	x	x	x	

Table 4.8: I80 9-Bits Interface GRAM Read Table

- I80 16-Bits Bus Interface (IM2-0="010")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22h**
Read Data foramt	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R15	R14	R13	R12	R11	R10	x	x	x	G15	G14	G13	G12	G11	G10	x	x	x	262K-Color (2-pixels/ 3bytes)
	B15	B14	B13	B12	B11	B10	x	x	x	R25	R24	R23	R22	R21	R20	x	x	x	
	G25	G24	G23	G22	G21	G20	x	x	x	B25	B24	B23	B22	B21	B20	x	x	x	

Table 4.9: I80 16-Bits Interface GRAM Read Table

- I80 18-Bits Bus Interface (IM2-0="000")

Register Command	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Register
	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0	1	0	x	**22h**
Read Data foramt	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Color
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Dummy Read
	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	262K-Color

Table 4.10: I80 18-Bits Interface GRAM Read Table

- Data Mapping Extend to 18-bit Data

		GRAM Data																	
Input Data	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18-bit	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16-bit	00	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	01	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	10	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4
	11	Reference EPF[1:0] setting in R6Bh																	

Table 4.11: Data Mapping Extend to 18-bit Data

4.2 Serial Data Transfer Interface

The HX8352-C01 supports 3-wire and 4-wire serial data transfer interface, the interface selection by setting IM2-0 pins, The IM2-0 set “10x” is select option1 3 wire serial bus. The IM2-0 set “11x” is select option3 4 wire serial bus.

The 3 wire serial bus is use: chip select line (NCS), the serial transfer clock line (NWR_SCL). When SDA_EN=0, SDI_SDA pin is for serial interface input data and SDO pin is for serial interface output data. When SDA_EN=1, SDI_SDA pin is for serial interface input/output data and SDO pin is unused.

The 4 wire serial bus is use: chip select line (NCS), data/command select (DNC), the serial transfer clock line (NWR_SCL). When SDA_EN=0, SDI_SDA pin is for serial interface input data and SDO pin is for serial interface output data. When SDA_EN=1, SDI_SDA pin is for serial interface input/output data and SDO pin is unused.

4.2.1 3-wire serial interface

As the chip select signal (NCS) goes low, the start byte needs to be transferred first. The start byte is made up of 6-bit bus device identification code; register select (RS) bit and read/write operation (RW) bit. The five upper bits of 6-bit bus device identification code must be set to “01110”, and the least significant bit of the identification code must be set as the external pin IM0 input as “ID”.

The seventh bit (RS) of the start byte determines internal index register or register, GRAM accessing. RS must be set to “0” when writing data to the index register or reading the status and it must be set to “1” when writing or reading a command or GRAM data. The read or write operation is selected by the eighth bit (RW) of the start byte. The data is written to the chip when R/W = 0, and read from chip when RW = 1.

RS	R/W	Function
0	0	Set index register
1	0	Writes Instruction or GRAM data
1	1	Reads command (Not support GRAM read)

Table 4.12: Function of RS and R/W bit bus

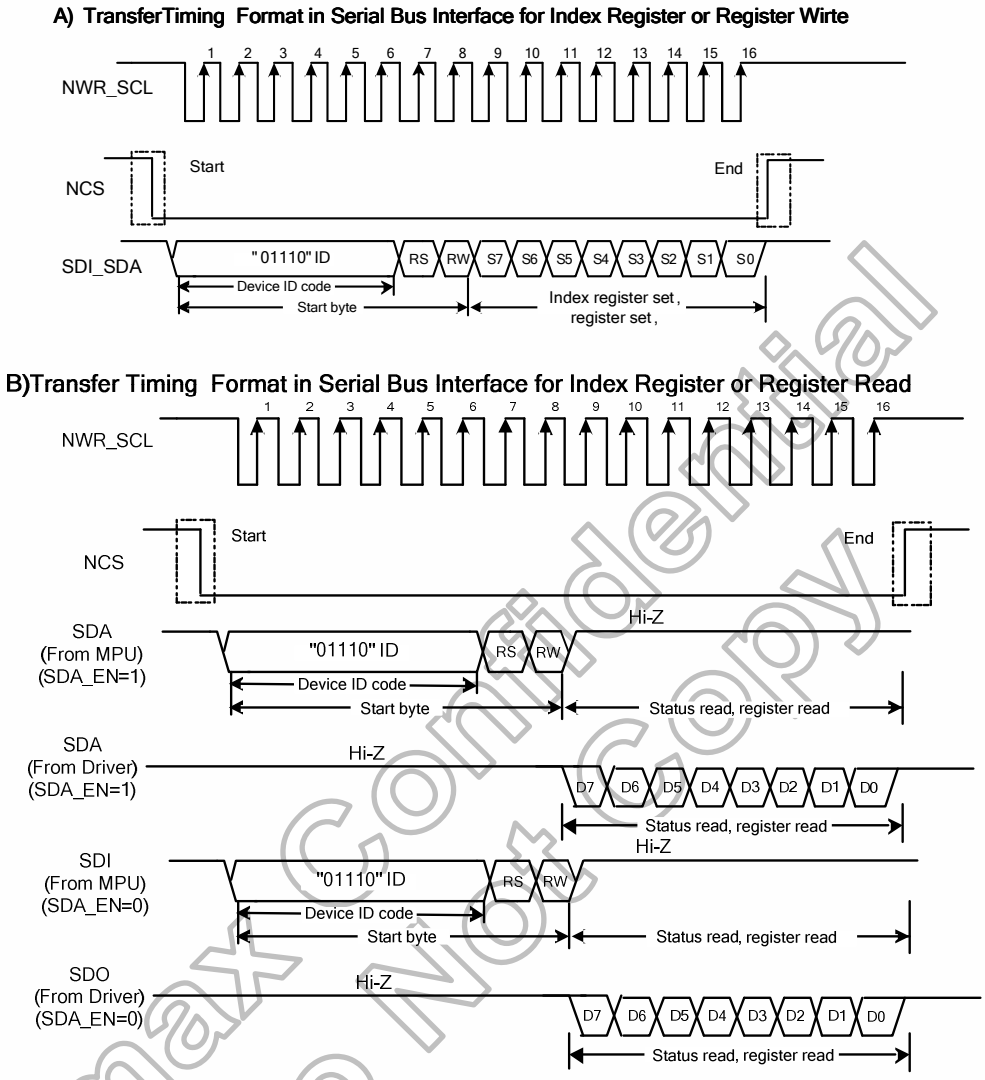


Figure 4.15: Index register read/write timing in 3-wire serial bus system interface

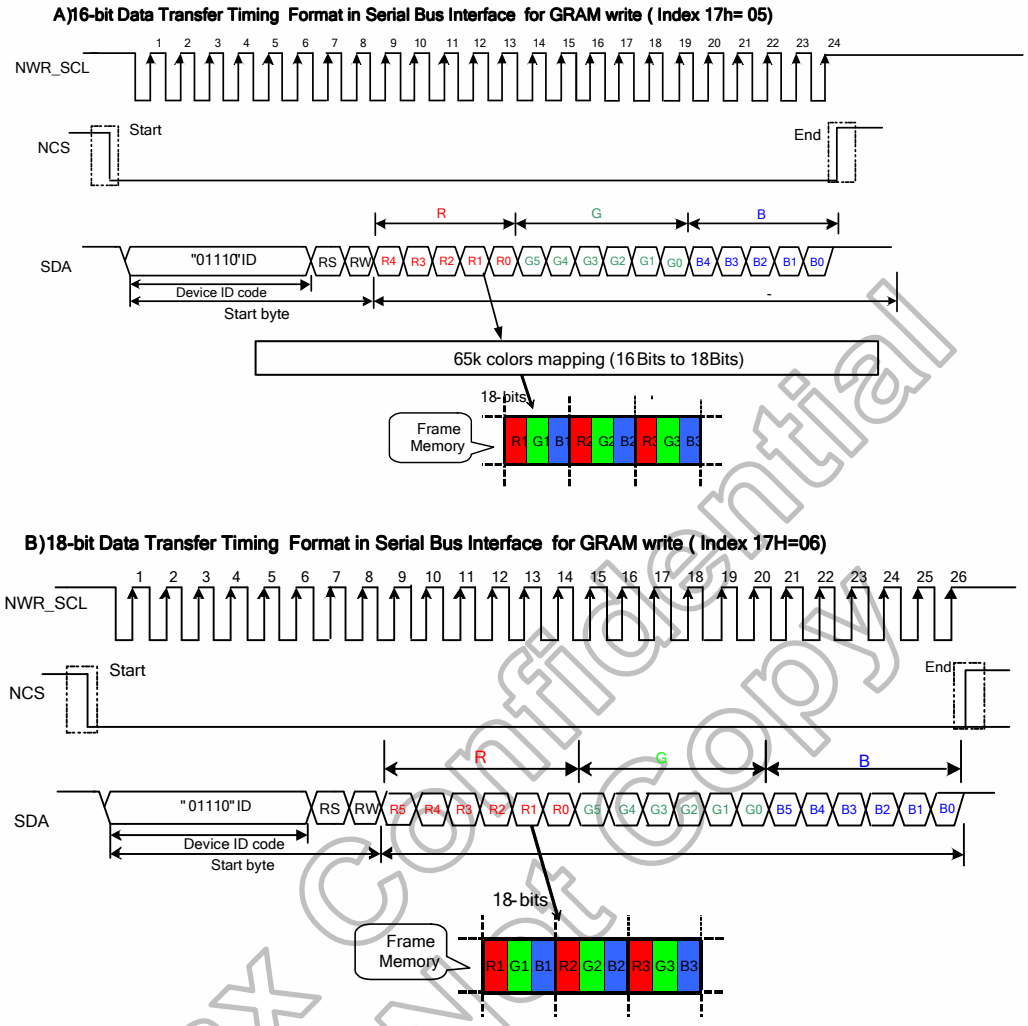


Figure 4.16: Data write timing in 3-wire serial bus system interface

4.2.2 4-wire serial interface

4-pin serial case, data packet contains just transmission byte and control bit DNC is transferred by DNC pin. If DNC is low, the transmission byte is command byte. If DNC is high, the transmission byte is stored to index register or GRAM. The MSB is transmitted first. The serial interface is initialized when NCS is high. In this state, NWR_SCL clock pulse or SDA data have no effect. A falling edge on NCS enables the serial interface and indicates the start of data transmission.

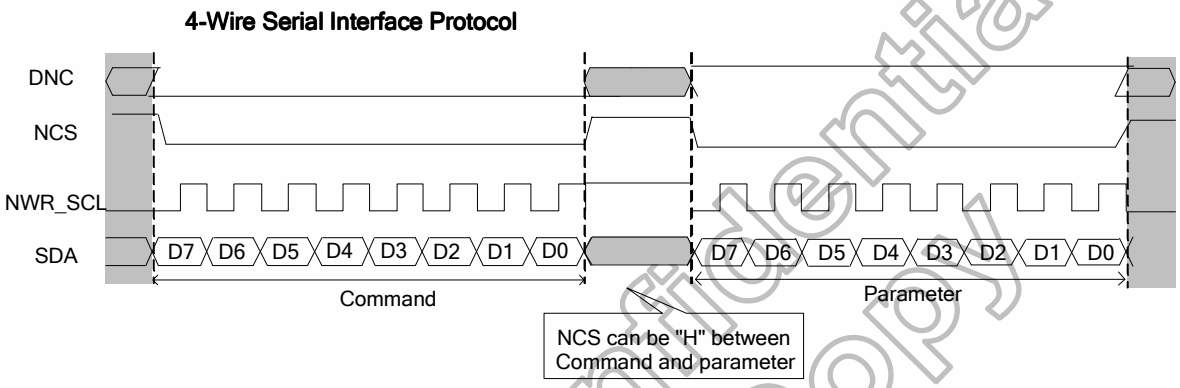


Figure 4.17: Index register write timing in 4-wire serial bus system interface

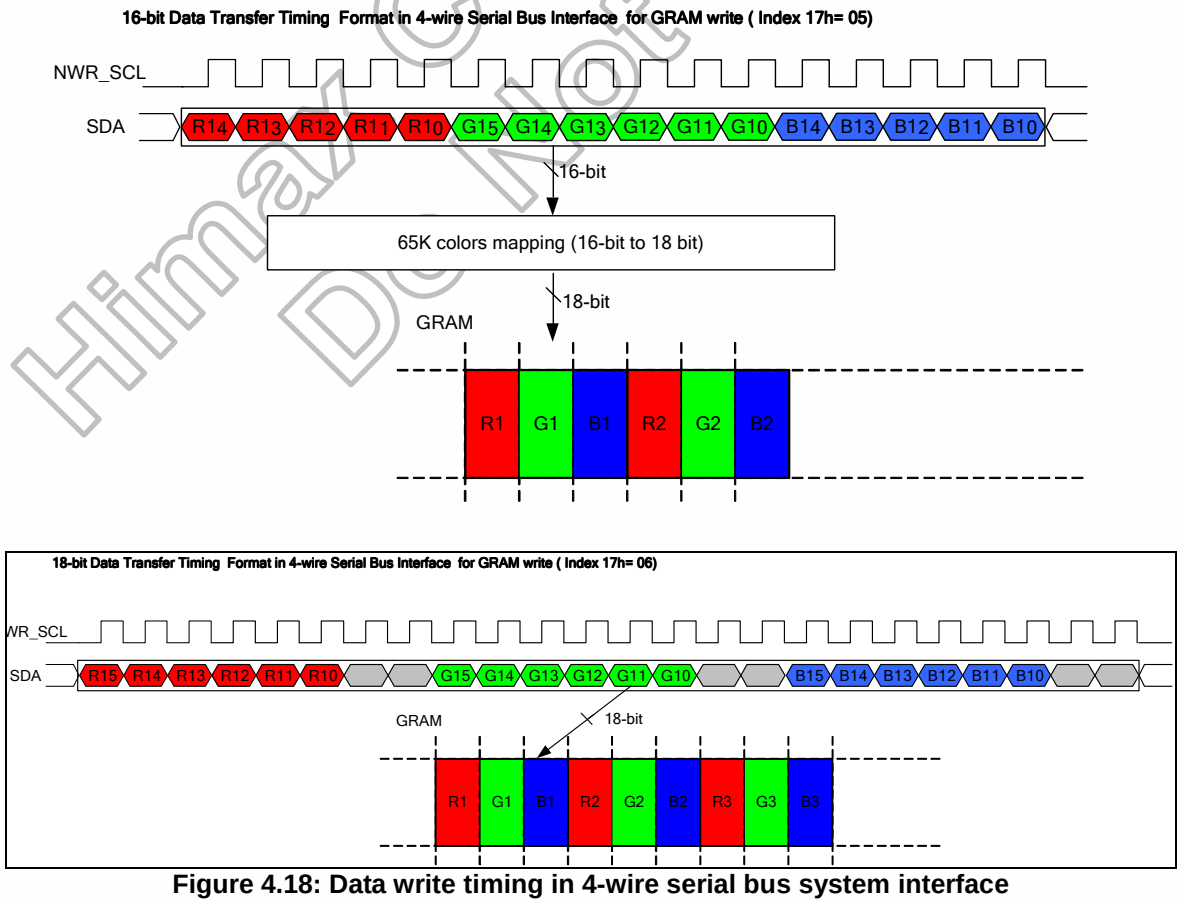


Figure 4.18: Data write timing in 4-wire serial bus system interface

4.3 RGB interface

The HX8352-C01 uses 16, 18-bit parallel RGB interface which includes: HSYNC, VSYNC, DE, PCLK, DB17~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB17~DB0 –lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Standby mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (‘-‘, ‘0’, low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (‘-‘, ‘0’, low) active and its state is read to the display module by a rising edge of the PCLK-line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is positive (‘+’, ‘1’, high) active and its state is read to the display module by a rising edge of the PCLK-line. 18 bit: DB17-DB12(R5-R0), DB11-DB6(G5-G0) and DB5-DB0(B5-B0); 16 bit: DB15-DB11(R4- R0), DB10-DB5(G5-G0) and DB4-DB0(B4-B0) are used to tell what is the information of the image that is transferred on the display (when DE =1 and there is a rising edge of PCLK). DB17~DB0 – lines can be set to “0” (low) or “1” (high). These lines are read by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.

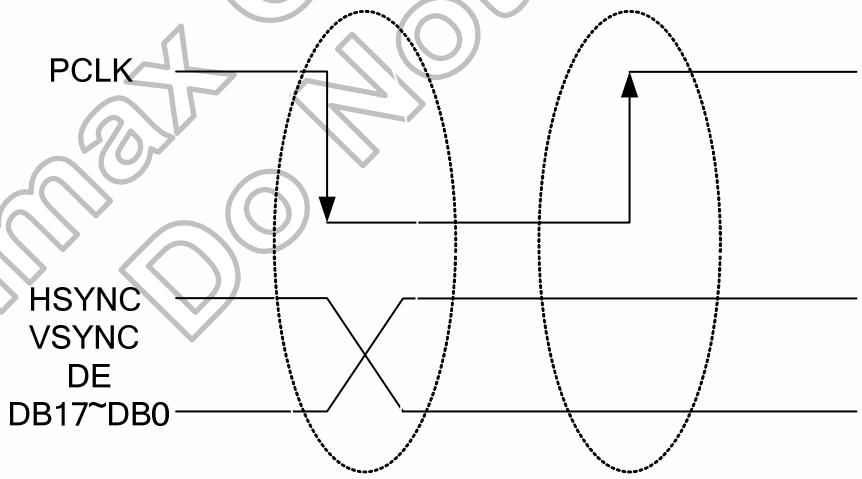


Figure 4.19: PCLK cycle
Note: PCLK is an unsynchronized signal (It can be stopped).

General Timing Diagram

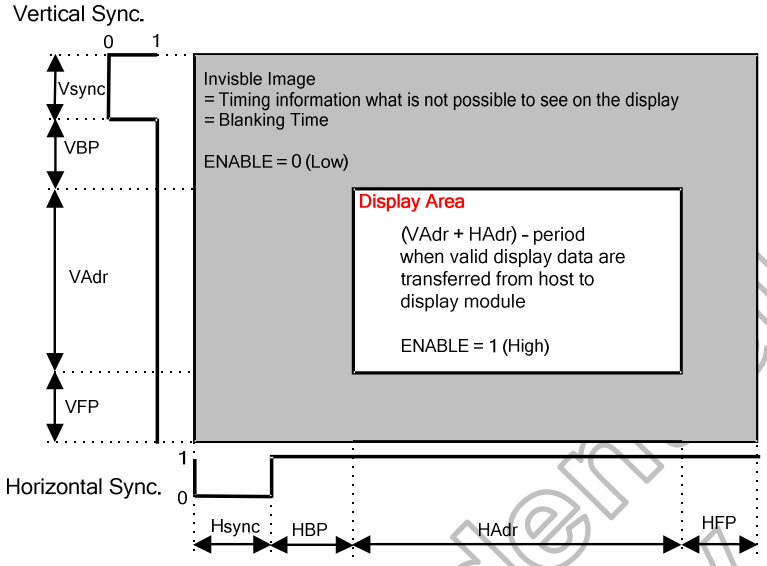


Figure 4.20: General Timing Diagram

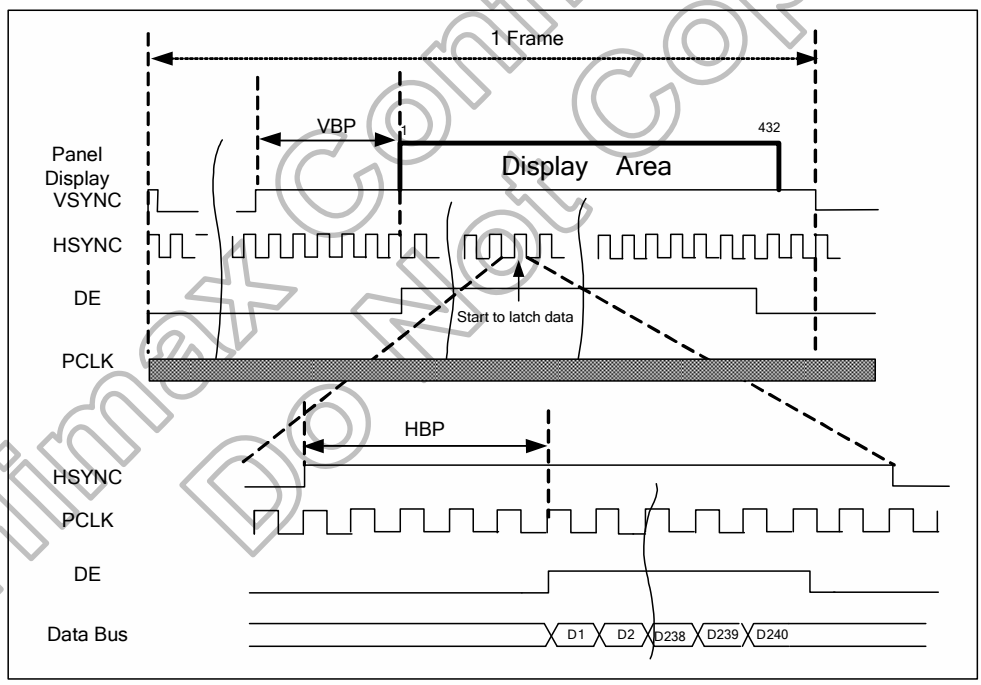


Figure 4.21: DPI timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

4.3.1 RGB Interface Data Color Coding

The RGB interface includes two types which are 16-/ 18-bit data format by register R17h to select.

R17h	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPI Interface mode
50h	R4	R3	R2	R1	R0	X	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	X	16-bit 65K-Color
60h	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit 262K-Color

Table 4.13: DPI Input Data Format

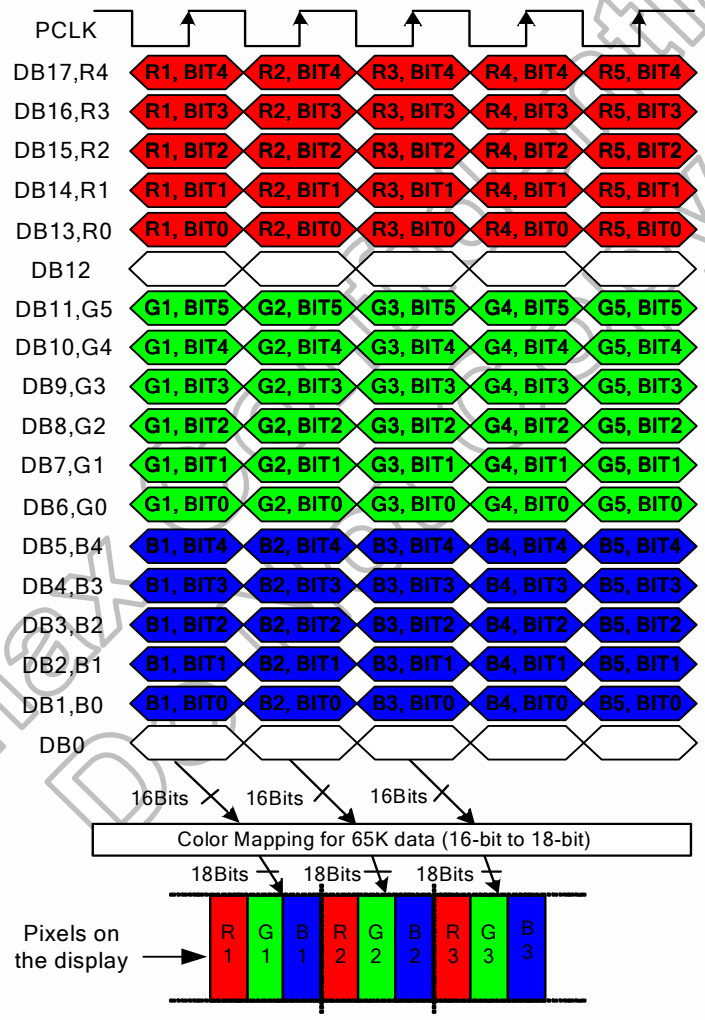


Figure 4.22: 16 bit data bus color order on DPI interface

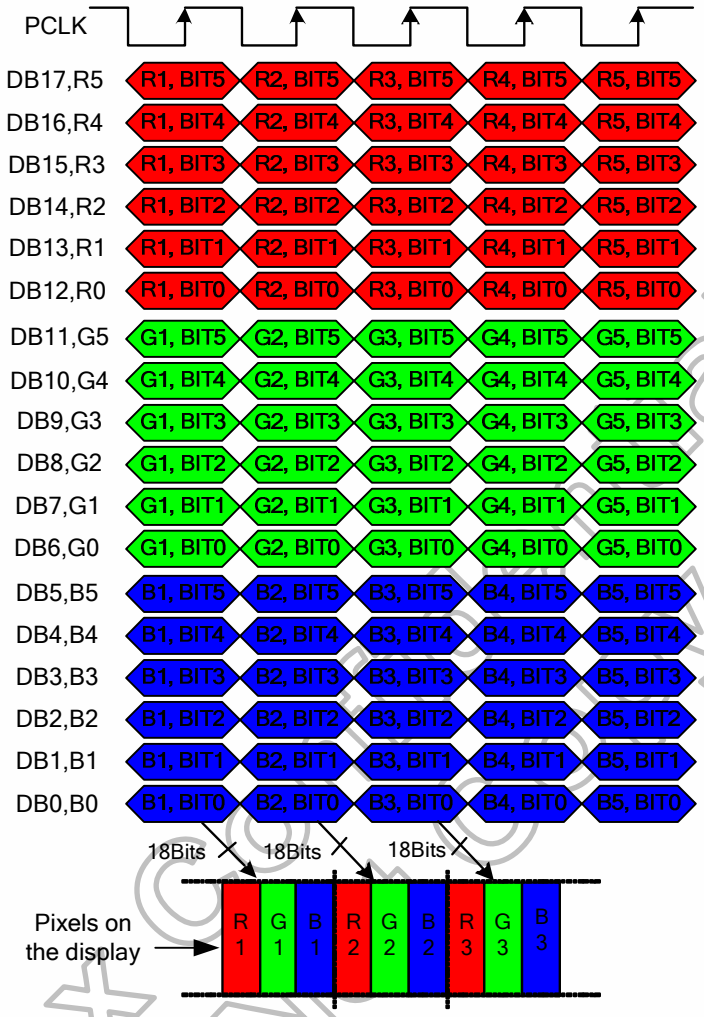


Figure 4.23: 18 bit data bus color order on DPI interface

- Data Mapping Extend to 18-bit Data

		GRAM Data																	
Input Data	EPF[1:0]	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
18-bit	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16-bit	00	R4	R3	R2	R1	R0	0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	0
	01	R4	R3	R2	R1	R0	1	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	1
	10	R4	R3	R2	R1	R0	R4	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	B4
	11	Reference EPF[1:0] setting in R6Bh																	

Table 4.14: DPI Data Mapping Extend to 18-bit Data

DPI interface displaying moving pictures can be selected to rewrite into the GRAM or not through GRAM. The selection is set by register DM[1:0] and RM.

RM The bit is used to select an interface for the Frame Memory access operation. The Frame Memory is accessed only via the interface defined by RM bit. Because the interface can be selected separately from display operation mode, writing data to the Frame Memory is possible via system interface when RM = 0, even in the DPI display operation.

RM setting is enabled from the next frame. Wait 1 frame to transfer data after setting.

RM	Interface for RAM access
0	DBI Interface (CPU)
1	DPI Interface (RGB)

DM[1:0] The bit is used to select display operation mode. The setting allows switching between display operation in synchronization with internal oscillation clock, VSYNC, or DPI signal.

Note that switching between DPI operation is prohibited.

DM 1	DM 0	Display Mode
0	0	Internal oscillation clock
0	1	DPI interface(GRAM)
1	0	RGB data bypass GRAM mode 1
1	1	RGB data bypass GRAM mode 2

Operation Mode	Frame Memory Access Setting (RM)	Display Operation Mode (DM[1:0])
Internal clock operation (displaying still pictures)	MPU interface (RM=0)	Internal clock operation (DM[1:0]=00)
DPI interface : capture mode (1) (displaying moving pictures)	DPI interface (RM=1)	DPI interface : VS & HS (DM[1:0]=01)
DPI interface : capture mode (2) (rewriting still pictures while displaying moving pictures)	MPU interface (RM=0)	DPI interface : VS (DM[1:0]=01)
DPI interface : through mode (1) (displaying moving pictures)	Bypass frame memory	DPI interface : VS & HS & DE (DM[1:0]=10)
DPI interface : through mode (2) (displaying moving pictures)	Bypass frame memory	DPI interface : VS & HS (DM[1:0]=11)
Internal clock operation DPI data format	DPI interface (RM=1)	Internal clock operation (DM[1:0]=00)

5. Function Description

5.1 Display data GRAM

HX8352-C01 support the display data RAM that stores display dots and consists of 1,866,240 bits (240x432x18 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

5.1.1 Address counter (AC)

The HX8352-C01 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM whose addresses range:

MV	X range	Y range	Panel resolution
0	0~239d.	0~431d.	240 RGBX432 dot
1	0~431d.	0~239d.	

Table 5.1: Addresses counter range

Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (MV, MX and MY bit) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data is written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the Column address register (start: SC, end: EC) or the Row address register (start: SP, end: EP). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

5.1.2 Source, gate and memory map

R16h: B5=0

Source Out		S1	S2	S3	S4	S5	S6	---	S715	S716	S717	S718	S719	S720		
		BGR=0	BGR=1		BGR=0	BGR=1			BGR=0	BGR=1		BGR=0	BGR=1			
RA															SA	
MY=0	MY=1														ML=0	ML=1
0	431	R0 5-0	G0 5-0	B0 5-0	R1 5-0	G1 5-0	B1 5-0	---	R238 5-0	G238 5-0	B238 5-0	R239 5-0	G239 5-0	B239 5-0	0	431
1	430							---							1	430
2	429							---							2	429
3	428							---							3	428
4	427							---							4	427
5	426							---							5	426
6	425							---							6	425
7	424							---							7	424
8	423							---							8	423
9	422							---							9	422
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
424	7							---							424	7
425	6							---							425	6
426	5							---							426	5
427	4							---							427	4
428	3							---							428	3
429	2							---							429	2
430	1							---							430	1
431	0							---							431	0
CA	MX=0	0			1			---	238			239				
	MX=1	239			238			---	1			0				

Note:RA=Row Address
CA=Colum Address
SA=Scan Address
MX=Colum address direction parameter
MY=Row address direction parameter
ML=Scan direction parameter
RGB=Red,Green and Blue pixel position change

Table 5.2: Memory map of 240RGB x432 resolution

5.1.3 MCU to memory write / read direction

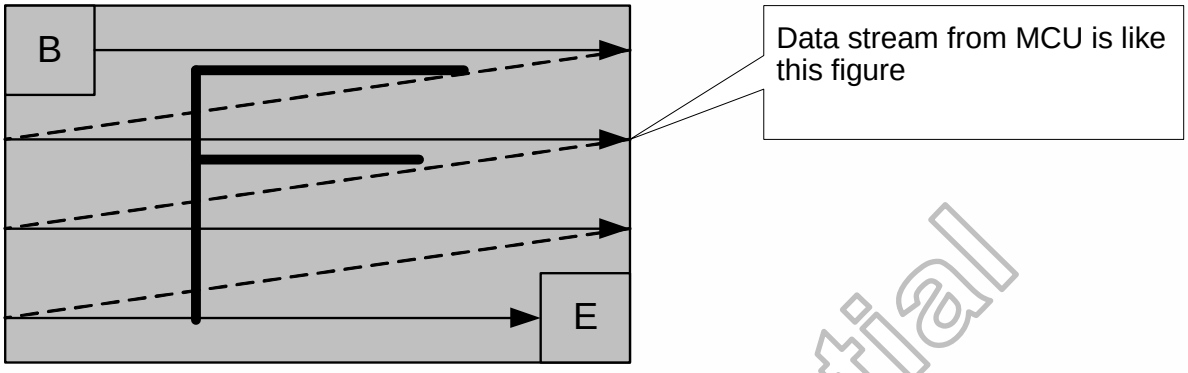


Figure 5.1: MCU to Memory write / read direction

The data is written in the order as illustrated above. The counter that dictates which physical memory the data is to be written is controlled by “Memory Access Control” Command, Bits MY, MX, MV as described below.

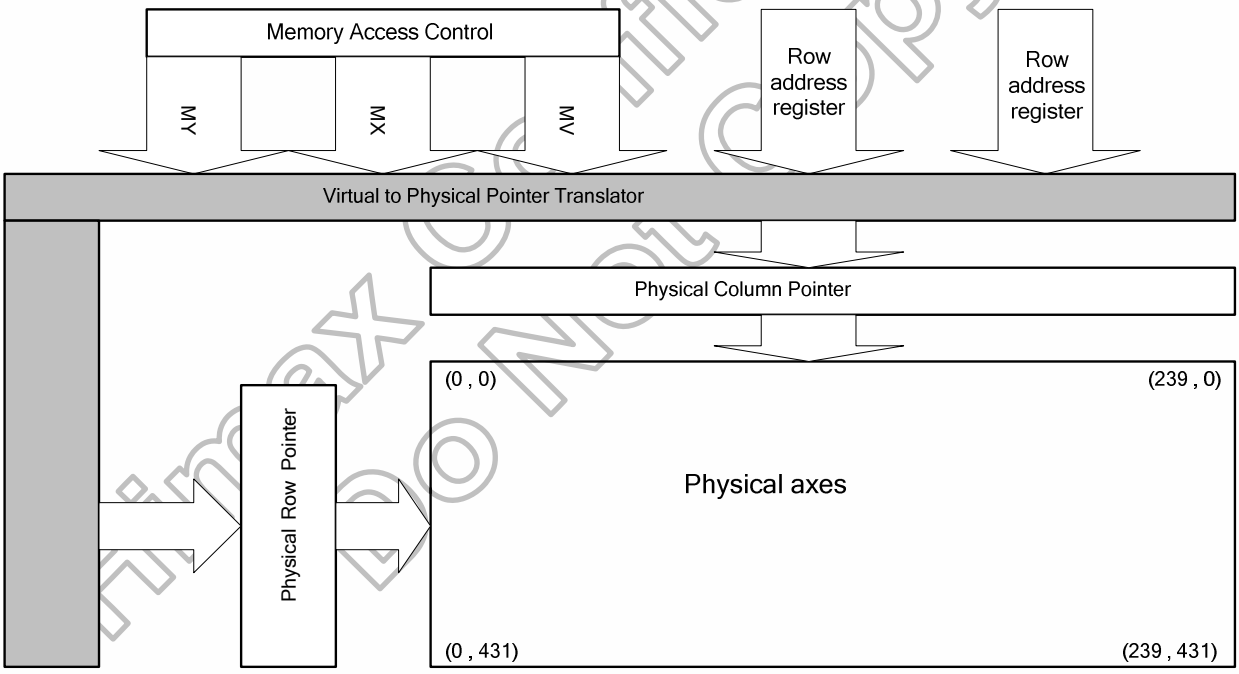


Figure 5.2: MY, MX, MV setting

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (431-Physical Row Pointer) with SC
0	1	0	Direct to (239-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (239-Physical Column Pointer)	Direct to (431-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (431-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (239-Physical Column Pointer)
1	1	1	Direct to (431-Physical Row Pointer)	Direct to (239-Physical Column Pointer)

Table 5.3: MY, MX, MV setting

The following figure depicts the update method set by MV, MX and MY bit.

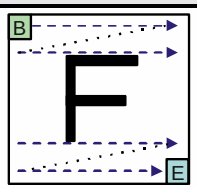
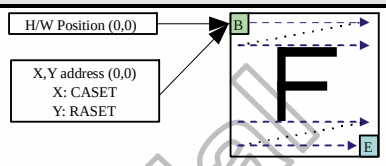
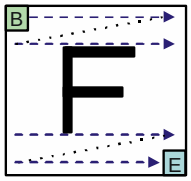
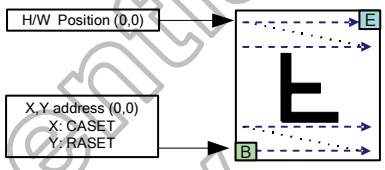
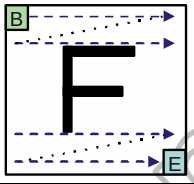
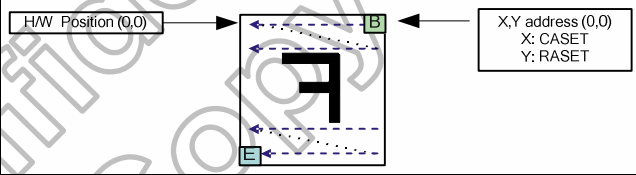
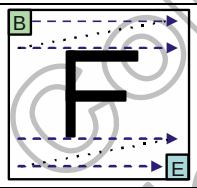
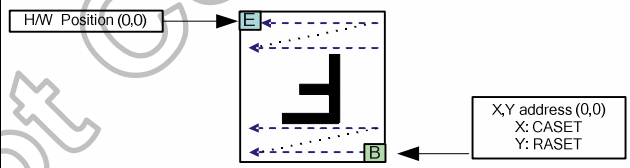
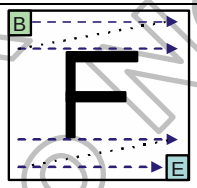
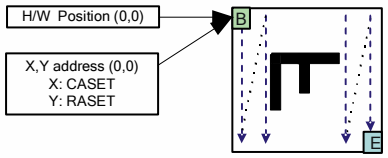
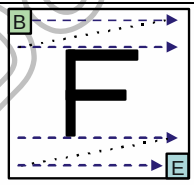
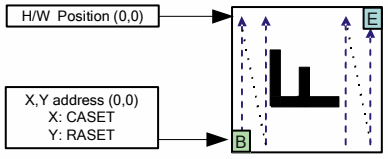
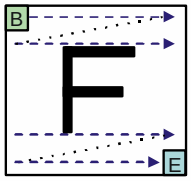
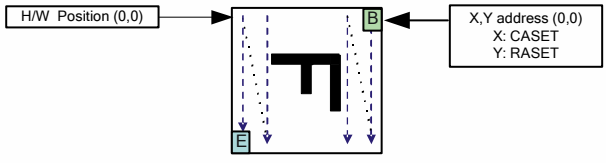
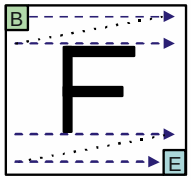
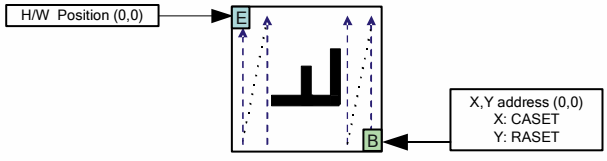
Display Data Direction	Memory Access Control			Image in the Host	Image in the Driver (GRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

Figure 5.3: Address direction settings

5.1.4 Fully display, partial display, vertical scrolling display

5.1.4.1 Fully display

Example: (1) 240RGBx432 dot display mode.
(2) Normal Display Mode.
(3) SC=0x000h, EC=0x0EFh and SP=0x000h, EP=0x1AFh, ML=0.

GRAM	000h DB---DB 17 ---0	001h DB---DB 17 ---0	---------	0EEh DB---DB 17 ---0	0EFh DB---DB 17 ---0
000h	000000H	000001H	---------	0000EEH	0000EFH
001h	001000H	001001H	---------	0010EEH	0010EFH
002h	002000H	002001H	---------	0020EEH	0020EFH
003h	003000H	003001H	---------	0030EEH	0030EFH
004h	004000H	004001H	---------	0040EEH	0040EFH
005h	005000H	005001H	---------	0050EEH	0050EFH
⋮	⋮	⋮	---------	⋮	⋮
1AAh	1AA000H	1AA001H	---------	1AA0EEH	1AA0EFH
1ABh	1AB000H	1AB001H	---------	1AB0EEH	1AB0EFH
1ACh	1AC000H	1AC001H	---------	1AC0EEH	1AC0EFH
1ADh	1AD000H	1AD001H	---------	1AD0EEH	1AD0EFH
1AEh	1AE000H	1AE001H	---------	1AE0EEH	1AE0EFH
1AFh	1AF000H	1AF001H	---------	1AF0EEH	1AF0EFH

Table 5.4: 240RGB x 432 resolution (SRAM assignment)

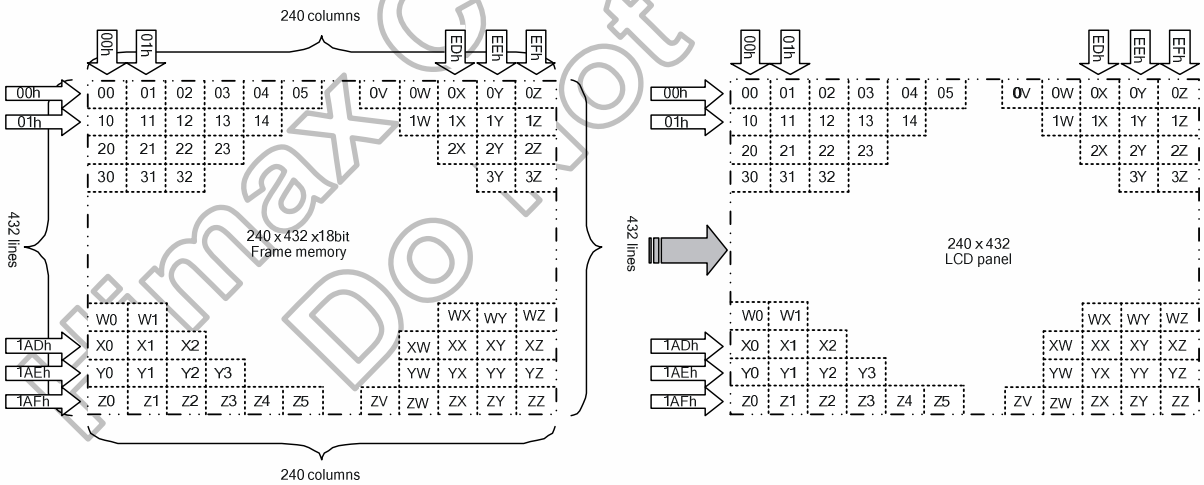


Figure 5.4: 240RGB x 432 resolution

5.1.4.2 Partial Display

Example: (1) 240RGBx432 dot display mode.
(2) PLTON=1.
(3) SR[15:0]=0002h, ER[15:0]=01ABh, ML=0.

GRAM	00h DB---DB 17 --- 0	01h DB---DB 17 --- 0	---------	EEh DB---DB 17 --- 0	EFh DB---DB 17 --- 0
000h	000000H	000001H	---------	0000EEH	0000EFH
001h	001000H	001001H	---------	0010EEH	0010EFH
002h	002000H	002001H	---------	0020EEH	0020EFH
003h	003000H	003001H	---------	0030EEH	0030EFH
004h	004000H	004001H	---------	0040EEH	0040EFH
005h	005000H	005001H	---------	0050EEH	0050EFH
⋮	⋮	⋮	---------	⋮	⋮
1AAh	1AA000H	1AA001H	---------	1AA0EEH	1AA0EFH
1ABh	1AB000H	1AB001H	---------	1AB0EEH	1AB0EFH
1ACh	1AC000H	1AC001H	---------	1AC0EEH	1AC0EFH
1ADh	1AD000H	1AD001H	---------	1AD0EEH	1AD0EFH
1AEh	1AE000H	1AE001H	---------	1AE0EEH	1AE0EFH
1AFh	1AF000H	1AF001H	---------	1AF0EEH	1AF0EFH

	LCD panel S/G pins	Pixel 1	Pixel 2	---------	Pixel239	Pixel240
Non-display area -> 2 lines	G1	000000H	000001H	---------	0000EEH	0000EFH
	G2	001000H	001001H	---------	0010EEH	0010EFH
Display area -> 426 lines	G3	002000H	002001H	---------	0020EEH	0020EFH
	G4	003000H	003001H	---------	0030EEH	0030EFH
	G5	004000H	004001H	---------	0040EEH	0040EFH
	G6	005000H	005001H	---------	0050EEH	0050EFH
	⋮	⋮	⋮	---------	⋮	⋮
	G427	1AA000H	1AA001H	---------	1AA0EEH	1AA0EFH
	G428	1AB000H	1AB001H	---------	1AB0EEH	1AB0EFH
Non-display area -> 4 lines	G429	1AC000H	1AC001H	---------	1AC0EEH	1AC0EFH
	G430	1AD000H	1AD001H	---------	1AD0EEH	1AD0EFH
	G431	1AE000H	1AE001H	---------	1AE0EEH	1AE0EFH
	G432	1AF000H	1AF001H	---------	1AF0EEH	1AF0EFH

Table 5.5: Memory map of partial display

5.1.4.3 Vertical scrolling display

When **SCROL** bit is set to '1', the scrolling display mode is active and the vertical scrolling display is specified by **TFA, VSA, BFA** bits (R0Eh~R13h) and **VSP** bits (R14h~R15h).

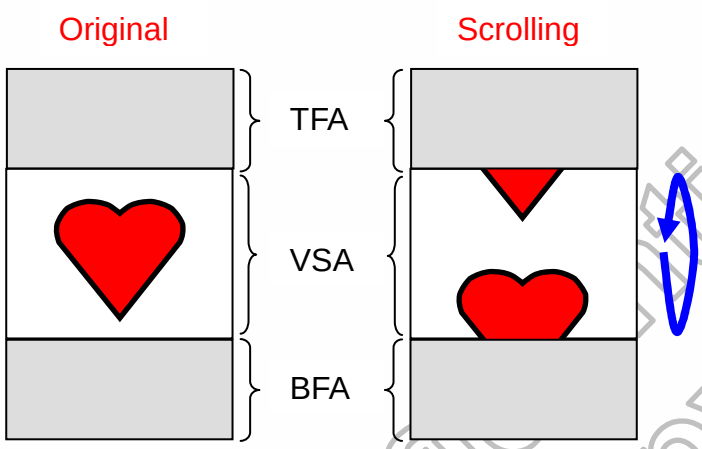


Figure 5.5: Vertical scrolling

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=Panel total scan lines. In this case, scrolling is applied as shown below.

Example:

When Vertical Scrolling Definition Parameters (TFA+VSA+BFA)=432. In this case, scrolling is applied as shown below.

Example (1) TFA=2, VSA=430, BFA=0 when ML=0

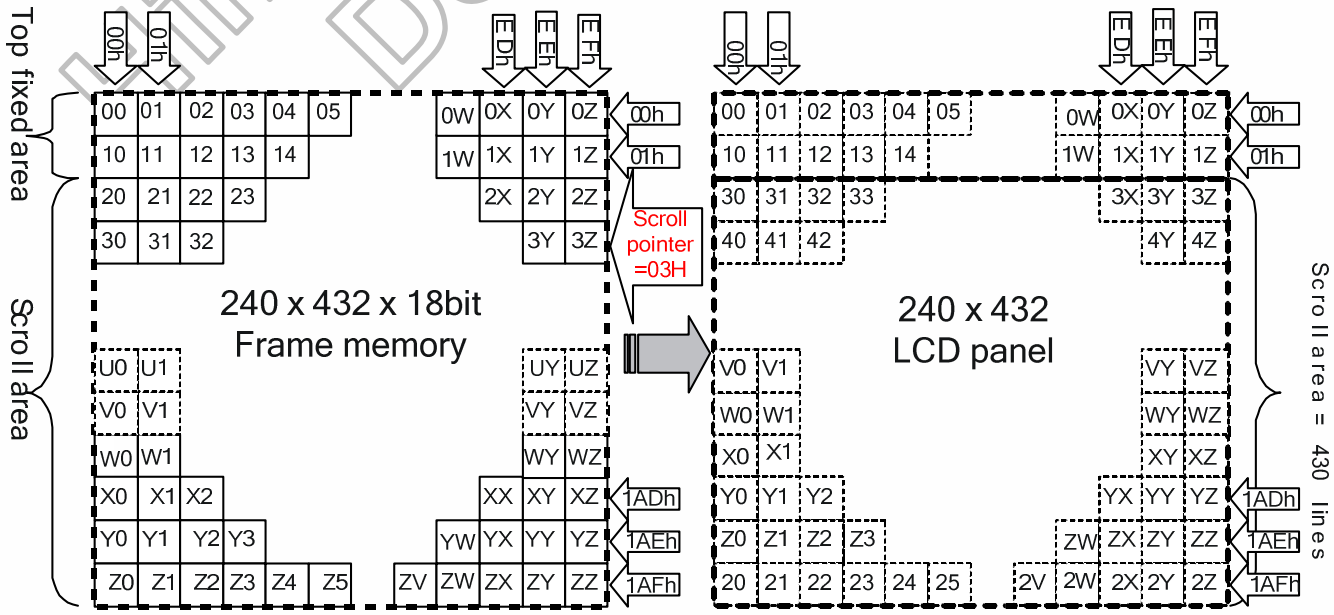


Figure 5.6: Memory map of vertical scrolling 1

Example (2) TFA=2, VSA=428, BFA=2 when ML=0

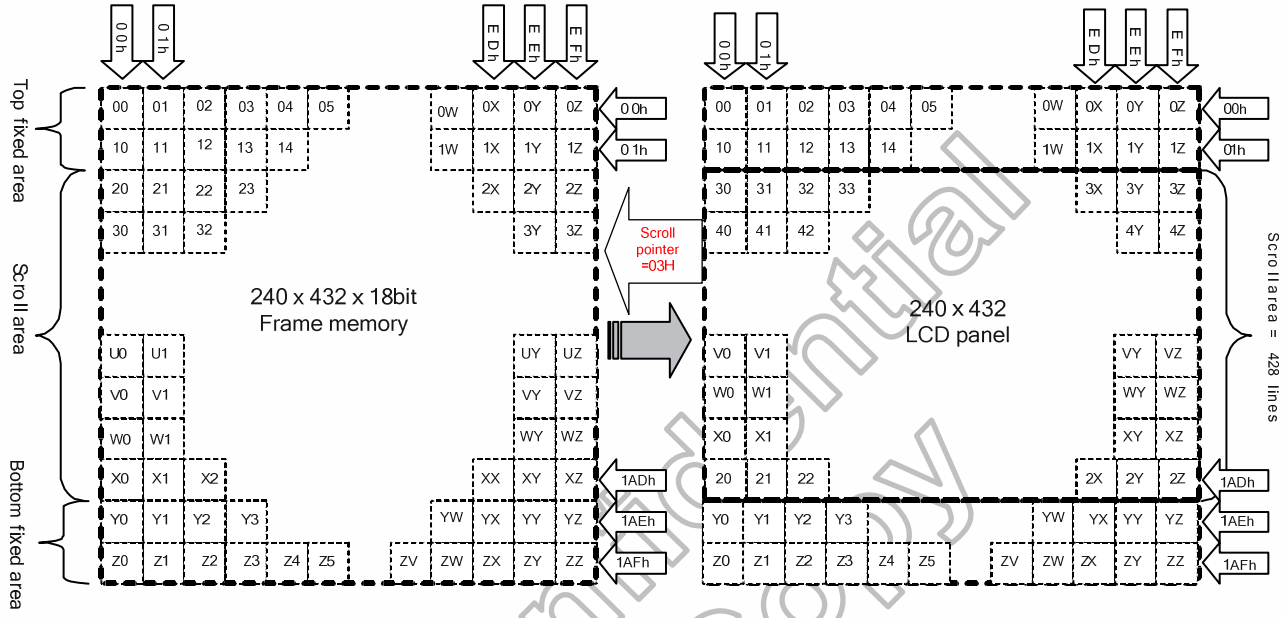


Figure 5.7: Memory map of vertical scrolling 2

Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits (R0Eh~R13h) and **VSP** bits (R14h~R15h).

Case 1: TFA + VSA + BFA≠432

Do not set TFA + VSA + BFA≠432. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA=432 (Scrolling)

Example (1) When TFA=0, VSA=432, BFA=0 and VSP=40. ML="0"

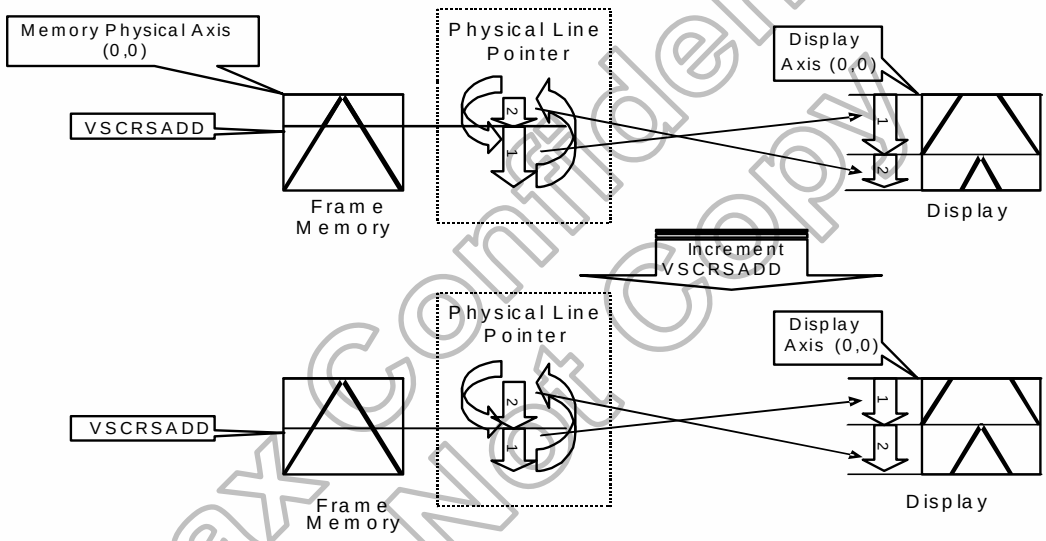


Figure 5.8: Vertical scroll example 1

Example (2) TFA=30, VSA=402, BFA=0 and VSP =80. ML="1"

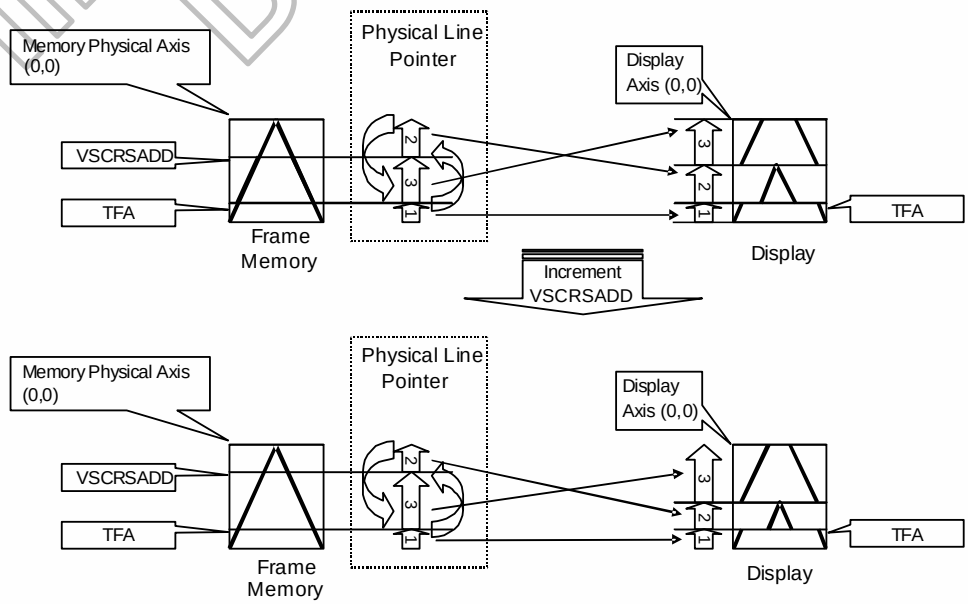


Figure 5.9: Vertical scroll example 2

5.2 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.2.1 Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

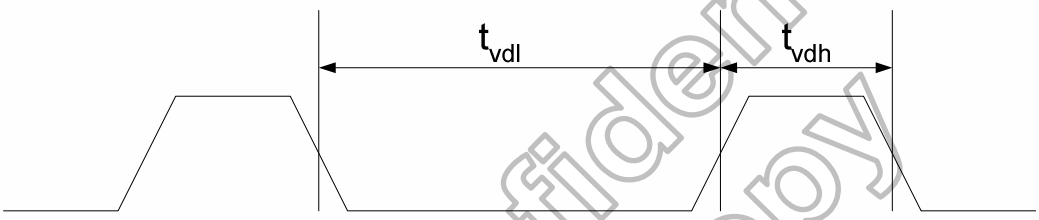


Figure 5.10: Tearing Effect Output signal mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TSEL[15:0] setting.

Ex: 1. TSEL[15:0]=0, then TE signal will output after last Line finished.

TSEL[15:0]=2, then TE signal will output at second Line start.

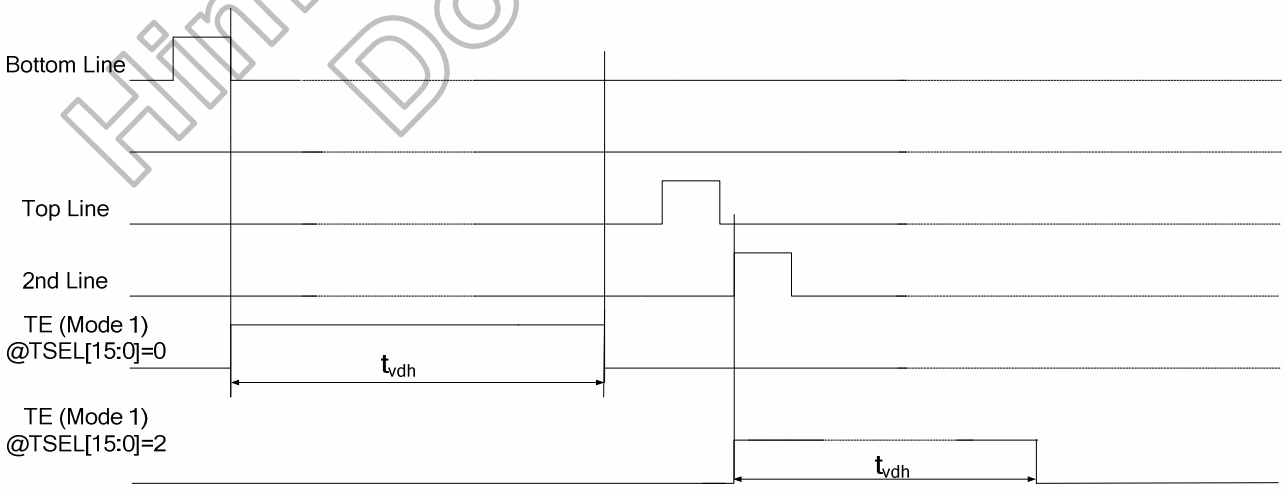


Figure 5.11: TE Delay Output

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 432 H-sync pulses per field.

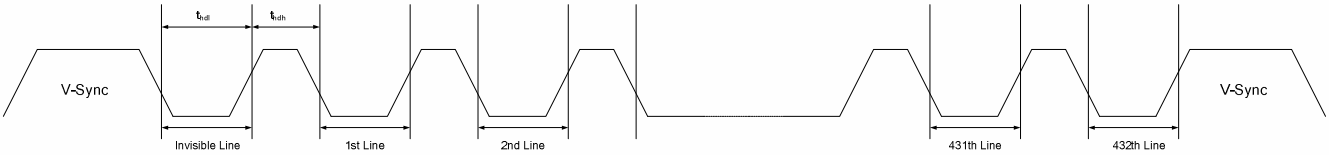


Figure 5.12: Tearing Effect Output signal mode 2

thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Under Mode2, the H-sync pulese output amount will be defined by TSEL[15:0] setting.

Ex: 1. TSEL[15:0]=0, then TE signal will output 432 H-sync.

TSEL[15:0]=1, then TE signal will output 431 H-sync.

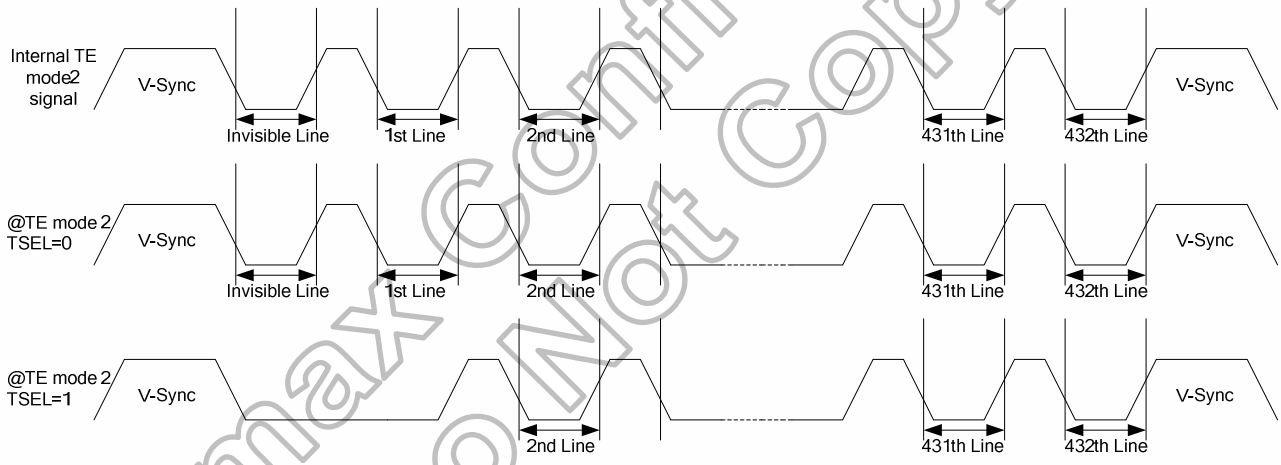


Figure 5.13: TE Output for TELINE setting

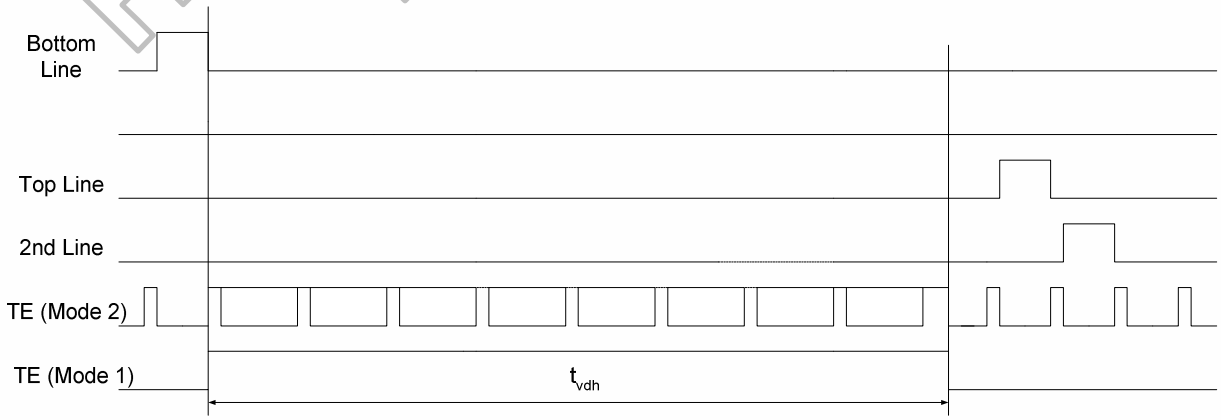


Figure 5.14: Tearing Effect Output signal

Note: During Sleep In Mode, the Tearing Output Pin is active Low

5.2.2 Tearing Effect Line Timing

The Tearing Effect signal is described below:

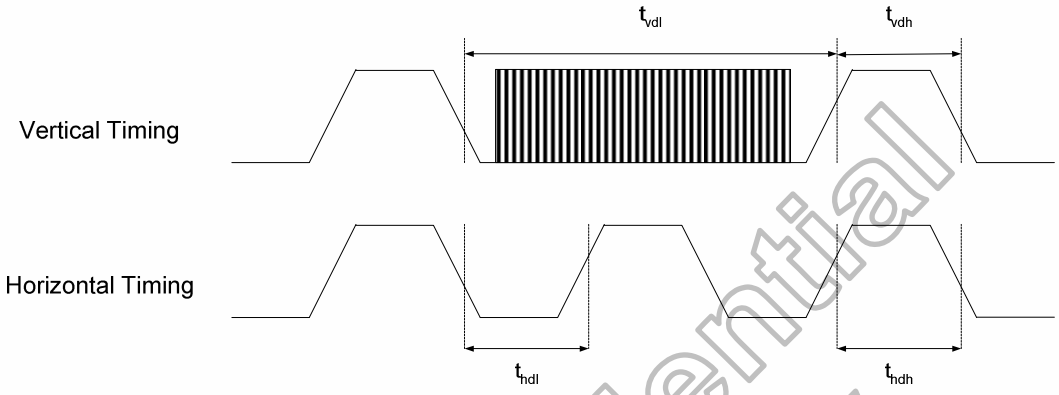


Figure 5.15: Tearing Effect Line Timing

Idle Mode Off (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Max.	Unit	description
tvdl	Vertical Timing Low Duration	-	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	-	-	us	-
thdh	Horizontal Timing High Duration	-	500	us	-

NOTE: The timings in Table 5.6 apply when MADCTL ML=0 and ML=1

Table 5.6: AC characteristics of Tearing Effect Signal

The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

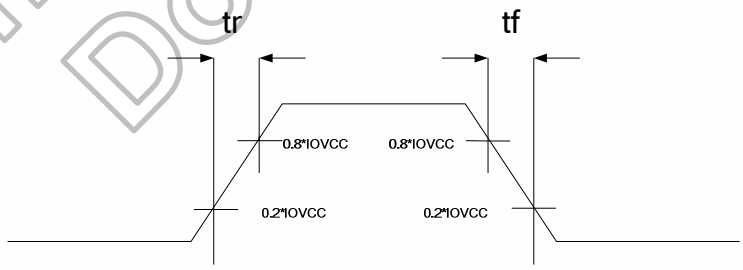


Figure 5.16: Rise and Fall times of TE signal

The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

Example 1: MPU's Write is Faster than Panel's Read.

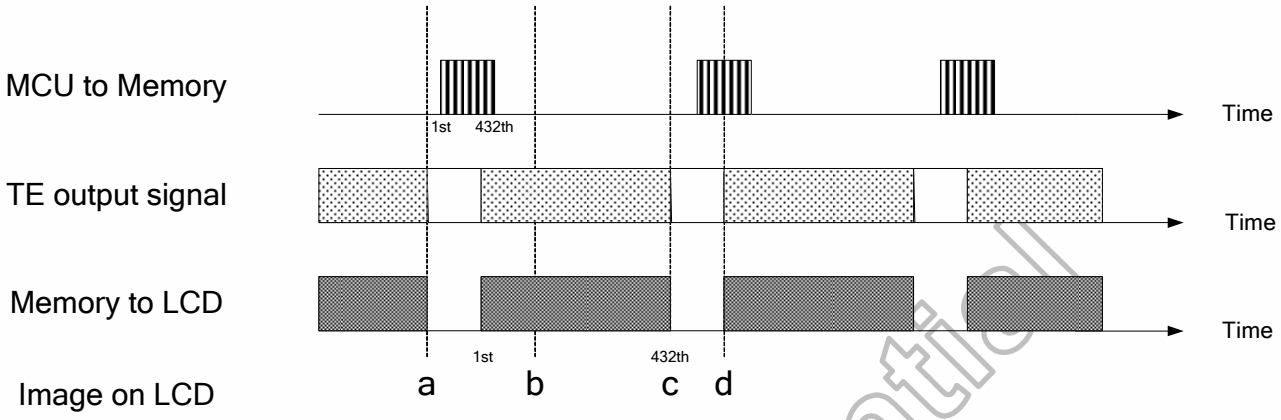


Figure 5.17: Tearing Effect - Example 1-1

Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

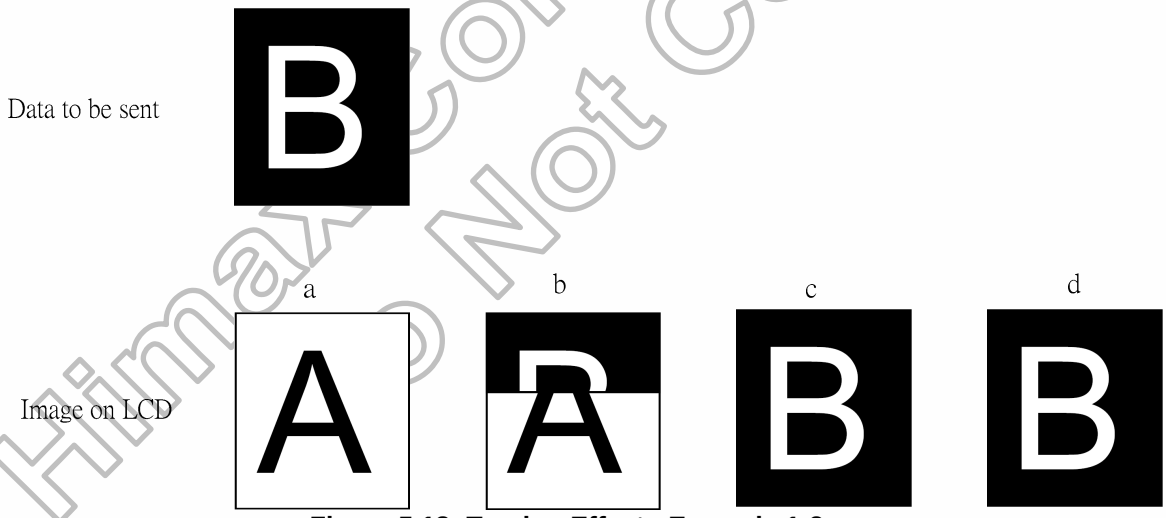


Figure 5.18: Tearing Effect - Example 1-2

Example 2: MPU's Write is Slower than Panel's Read.

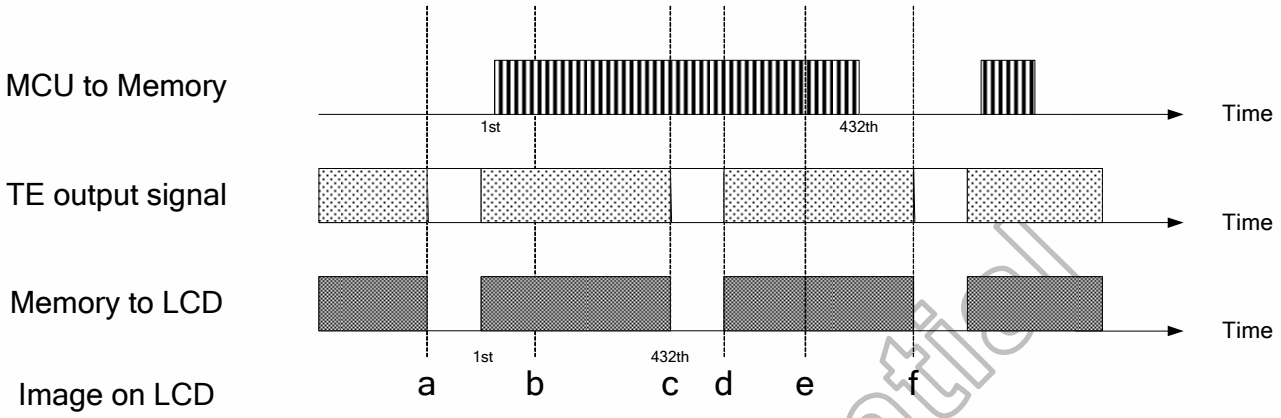


Figure 5.19: Tearing Effect - Example 2-1

The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.

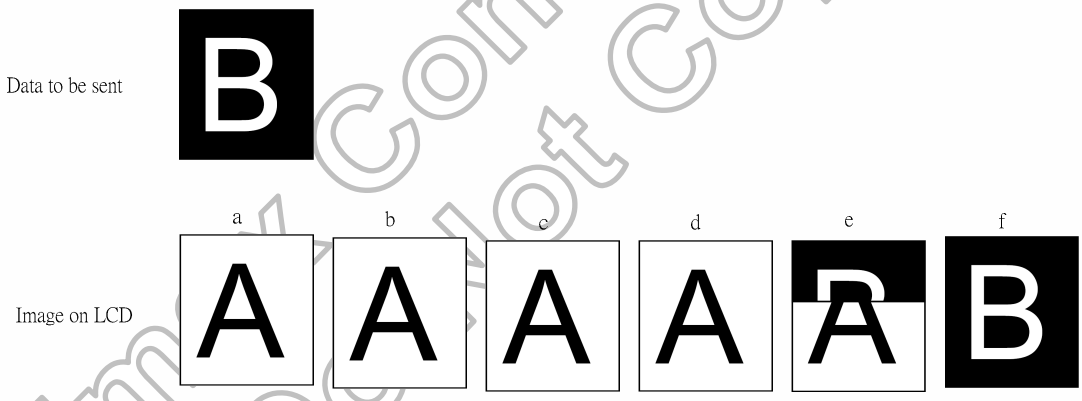


Figure 5.20: Tearing Effect - Example 2-2

5.3 Oscillator

The HX8352-C01 can oscillate an internal R-C oscillator with an internal oscillation resistor (Rf). The oscillation frequency is changed according to the RADJ[3:0] internal register. The default frequency is 3.69MHz.

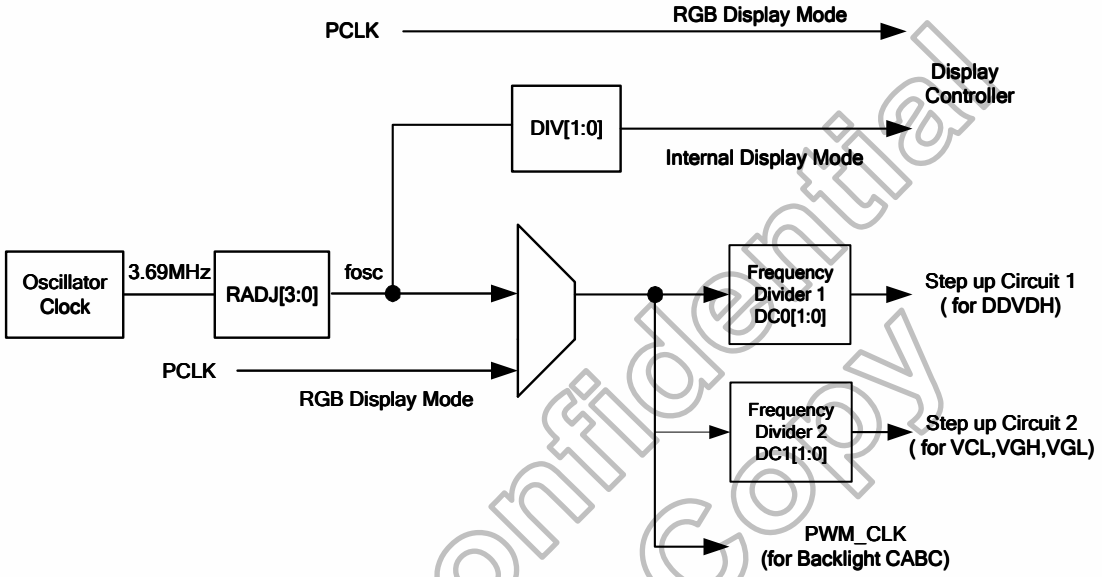


Figure 5.21: OSC aritecture

5.4 Source driver

The HX8352-C01 contains a 720 channels of source driver which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

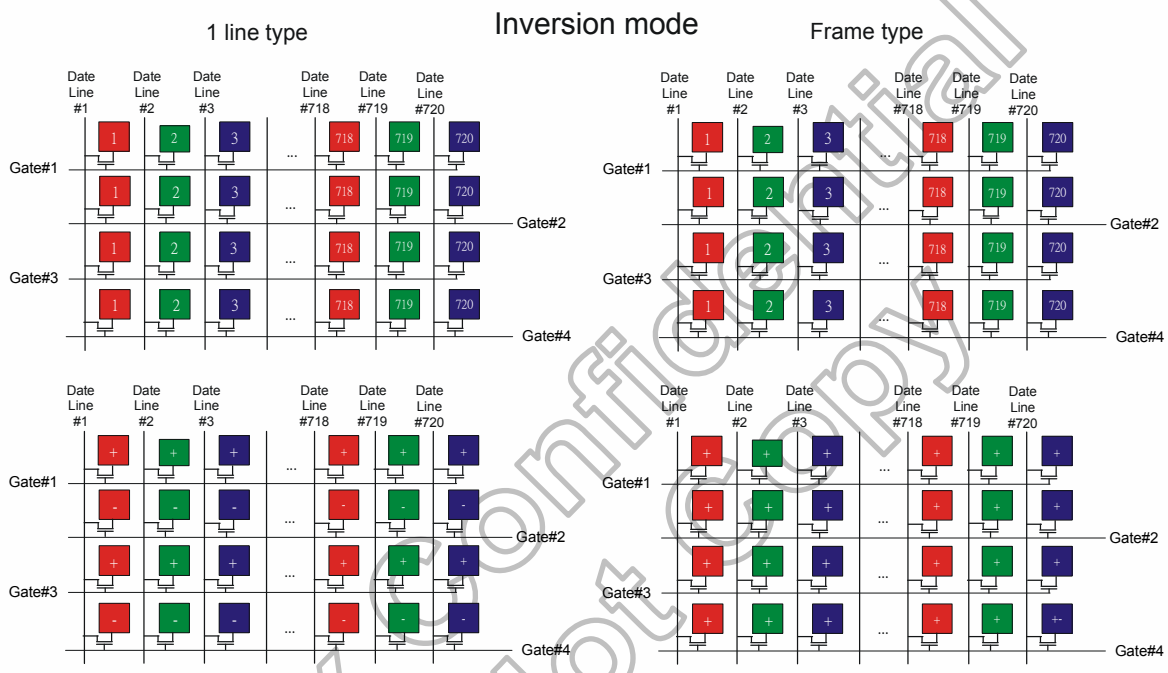


Figure 5.22: Source channels of different inversion mode

5.5 Gate Driver

The HX8352-C01 contains a 432 gate channels of gate driver (G1~G432) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

HX8352-C01 can set internal register SM and GS bit to determine the pin assignment of gate. The SM and GS setting allows changing the shift direction of gate outputs by connecting LCD panel with the HX8352-C01.

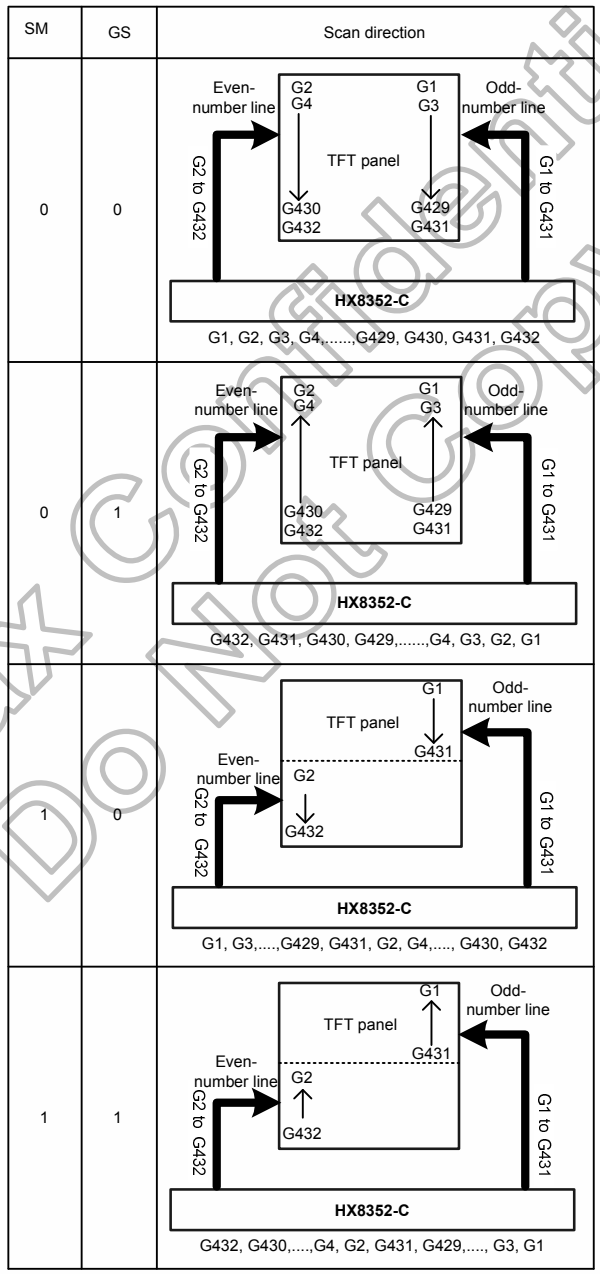


Figure 5.23: Scan direction of Gate Driver

5.6 Power generation

5.6.1 LCD power generation scheme

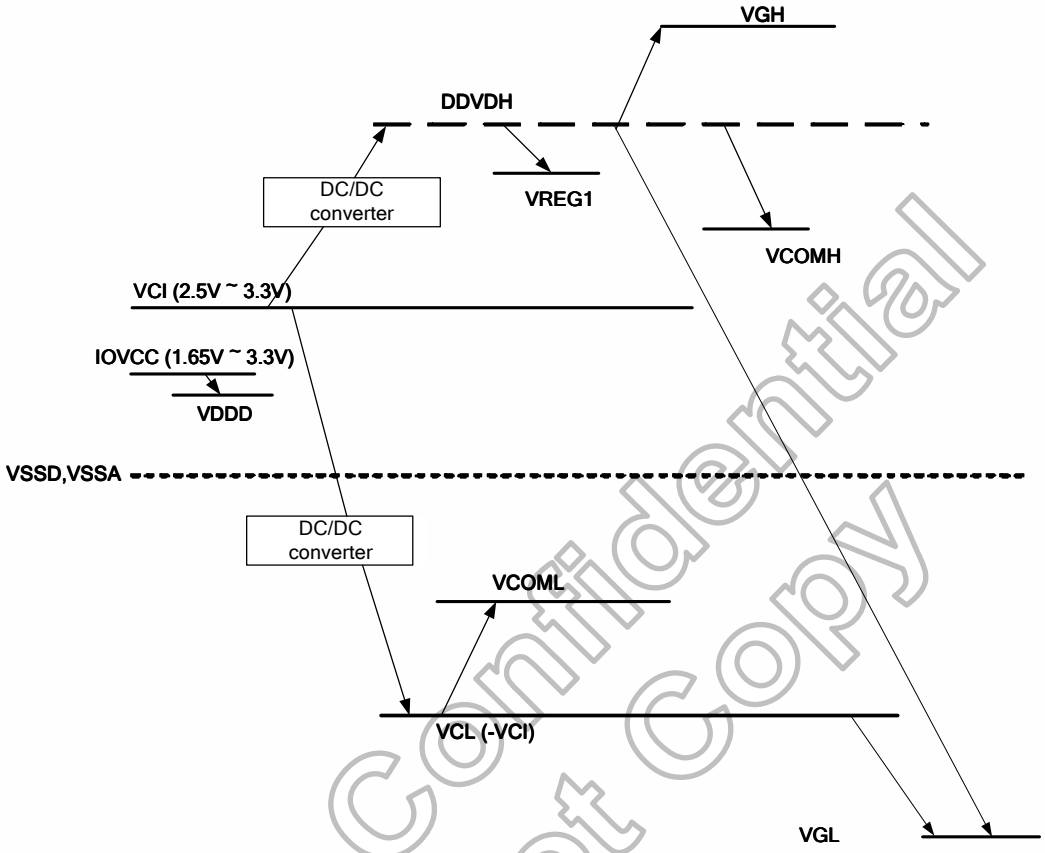


Figure 5.24: LCD power generation scheme

Voltage configuration

HX8352-C01 has an internal power supply circuit to drive a-Si LCD panel. Please set up each voltage output according to the LCD panel.

Name	Function	Set up Value	Note
DDVDH	DC/DC converter circuit output	4.5 V or 6.0V	-
VCL	DC/DC converter circuit output	-VCI	-
VREG1	Reference voltage for gamma circuit	4.0 ~ 5.5V	Reference register
VGH	TFT gate on voltage output	10 ~ 18V	Reference register
VGL	TFT gate off voltage output	-5 ~ -12.5V	Reference register
VCOMH	TFT common electrode voltage	3 ~ (DDVDH-0.5)V	Reference register
VCOML	TFT common electrode voltage	(VCL+0.5) ~ 0V	Reference register

Table 5.7: Power supply voltage configuration

5.6.2 Power supply circuit

The power circuit of HX8352-C01 is used to generate supply voltages for LCD panel driving and backlight control.

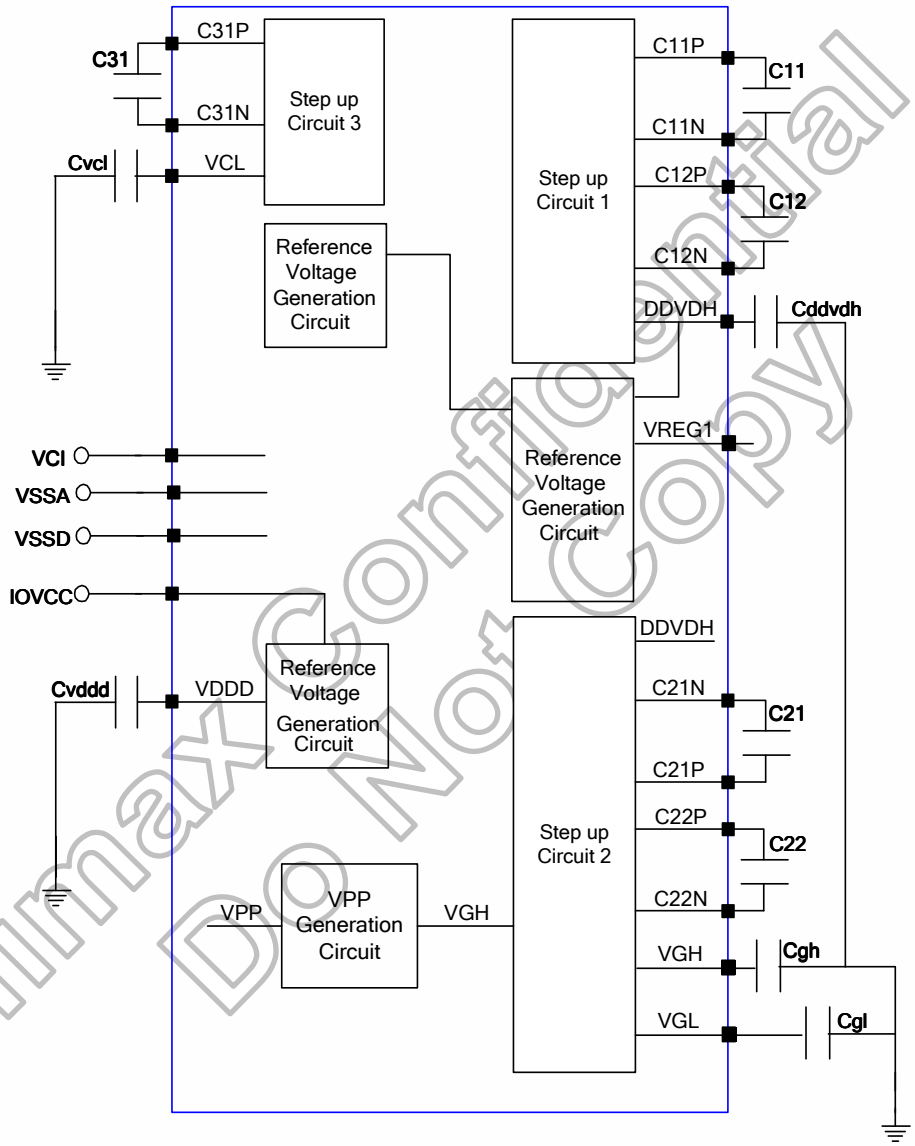


Figure 5.25: Block diagram of HX8352-C01 power circuit with internal charge pump

Specification of connected passive component

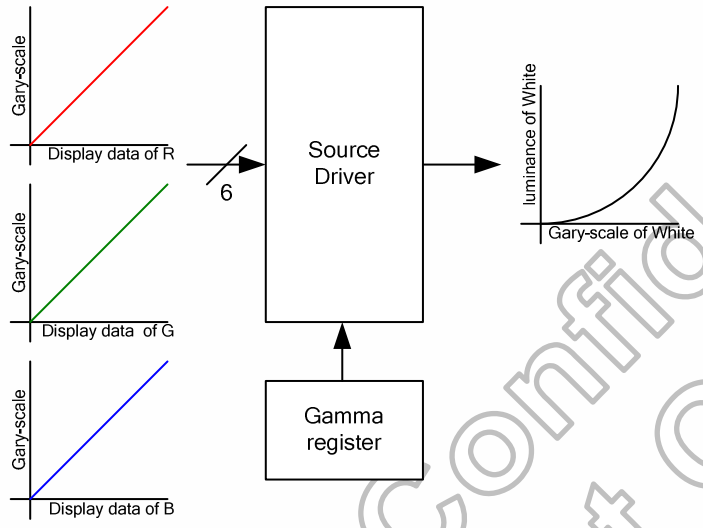
Capacitor	Recommended voltage	Capacity
Cvddd (VDDD)	6V	1 µF (B characteristics)
Cddvdh (DDVDH)	10V	1 µF (B characteristics)
Cvcl (VCL)	6V	1 µF (B characteristics)
C11 (C11P/N)	6V	1 µF (B characteristics)
C12 (C12P/N)	6V	1 µF (B characteristics)
C31 (C31P/N)	6V	1 µF (B characteristics)
C21 (C21P/N)	10V	1 µF (B characteristics)
C22 (C22P/N)	10V	1 µF (B characteristics)
Cgh (VGH)	25V	1 µF (B characteristics)
Cgl (VGL)	16V	1 µF (B characteristics)

Table 5.8: Adoptability of capacitor

5.7 Gamma characteristic correction function

The HX8352-C01 offers two kinds of Gamma adjustment ways to come to accord with LC characteristic, one kind is through Source Driver directly, another one is adjusted by the digital gamma correction. The Gamma adjustment way is select by internal register DGC_EN bit.

A) Gamma adjustment of Source Driver



B) Gamma adjustment of Digital Gamma Correction

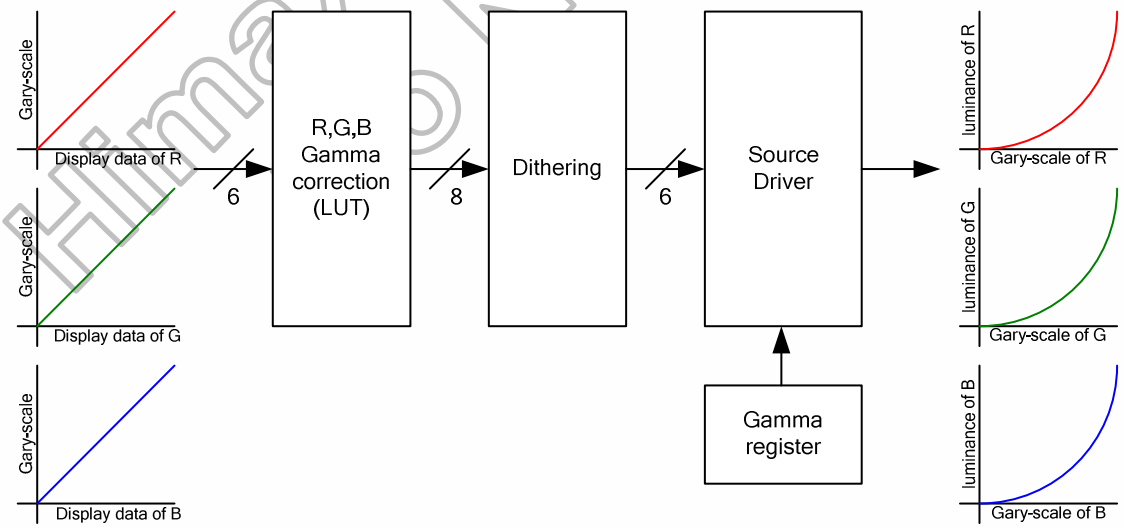


Figure 5.26: Gamma adjustments different of source driver with digital gamma correction

5.7.1 Gray Voltage Generator for Source Driver

The HX8352-C01 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment operation is implemented by deciding the 8 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 128 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

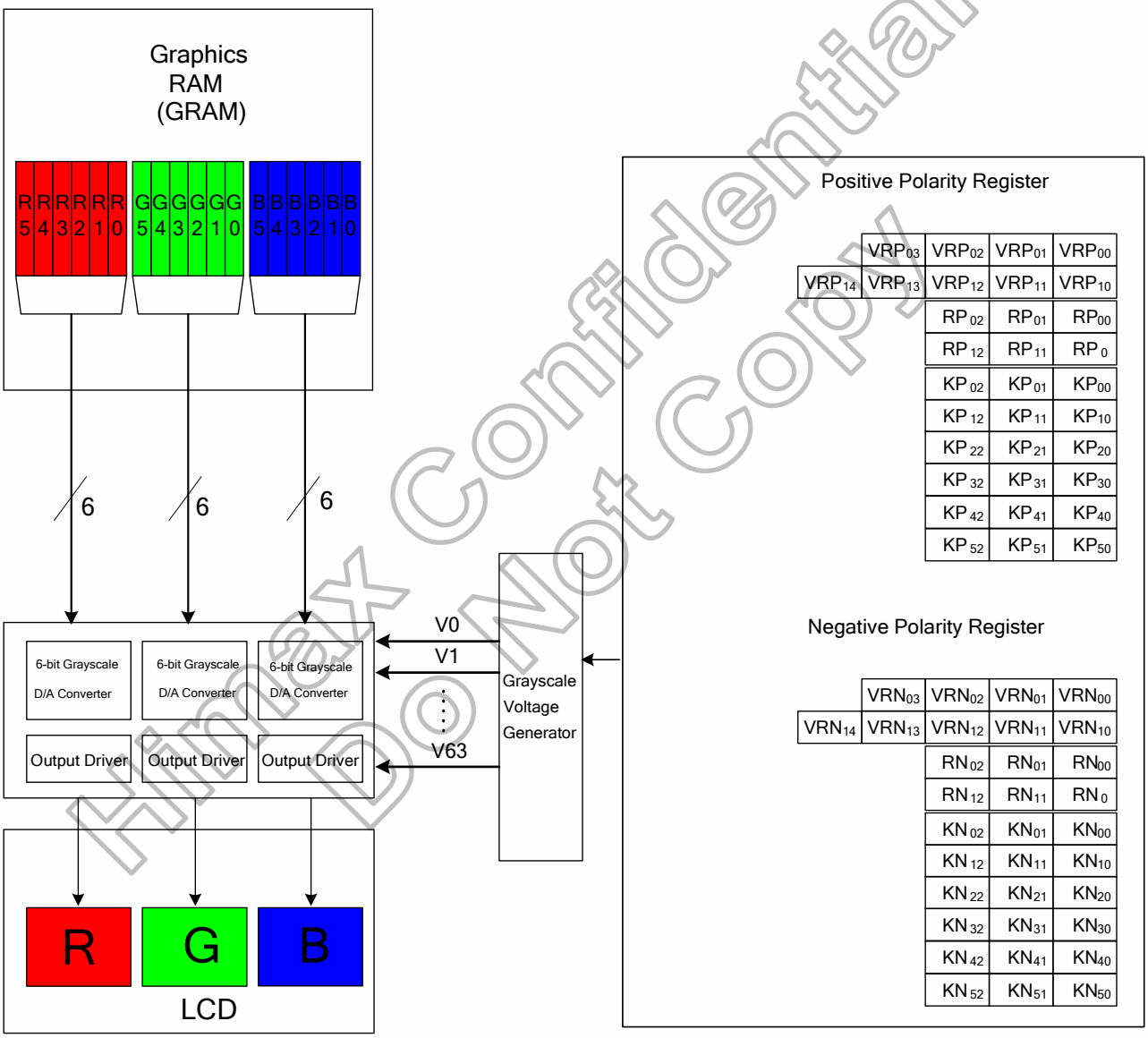


Figure 5.27: Grayscale Control

5.7.1.1 Structure of Grayscale Voltage Generator

Eight reference gamma voltages VgP/N(4, 9, 16, 28, 51, 63, 70, 75) for positive and negative polarity are specified by the center adjustment, the micro adjustment and the offset adjustment registers firstly. With those eight voltages injected into specified node of grayscale voltage generator, total 64 grayscale voltages (V0-V63) can be generated from grayscale amplifier for LCD panel used.

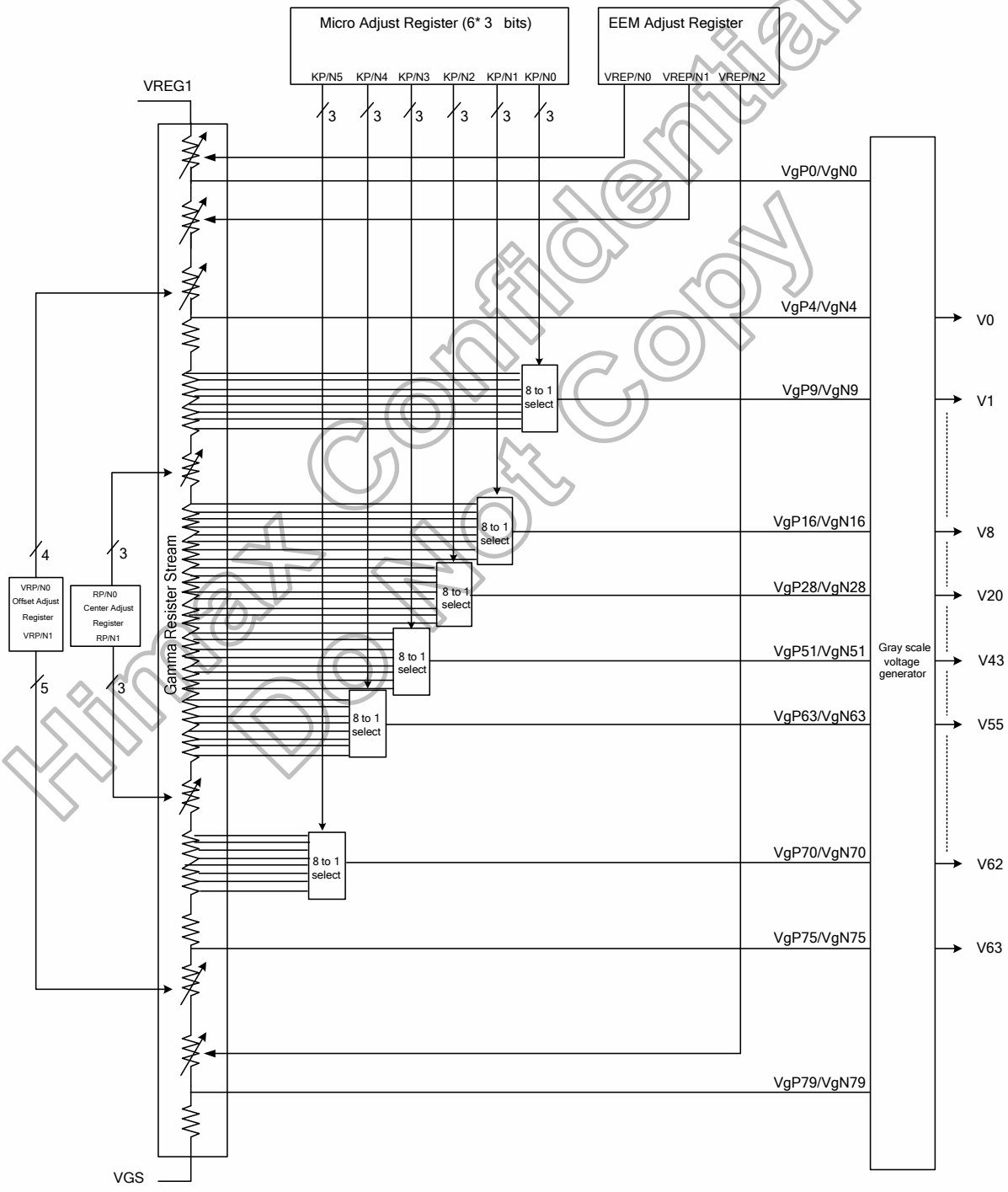


Figure 5.28: Structure of Grayscale Voltage Generator

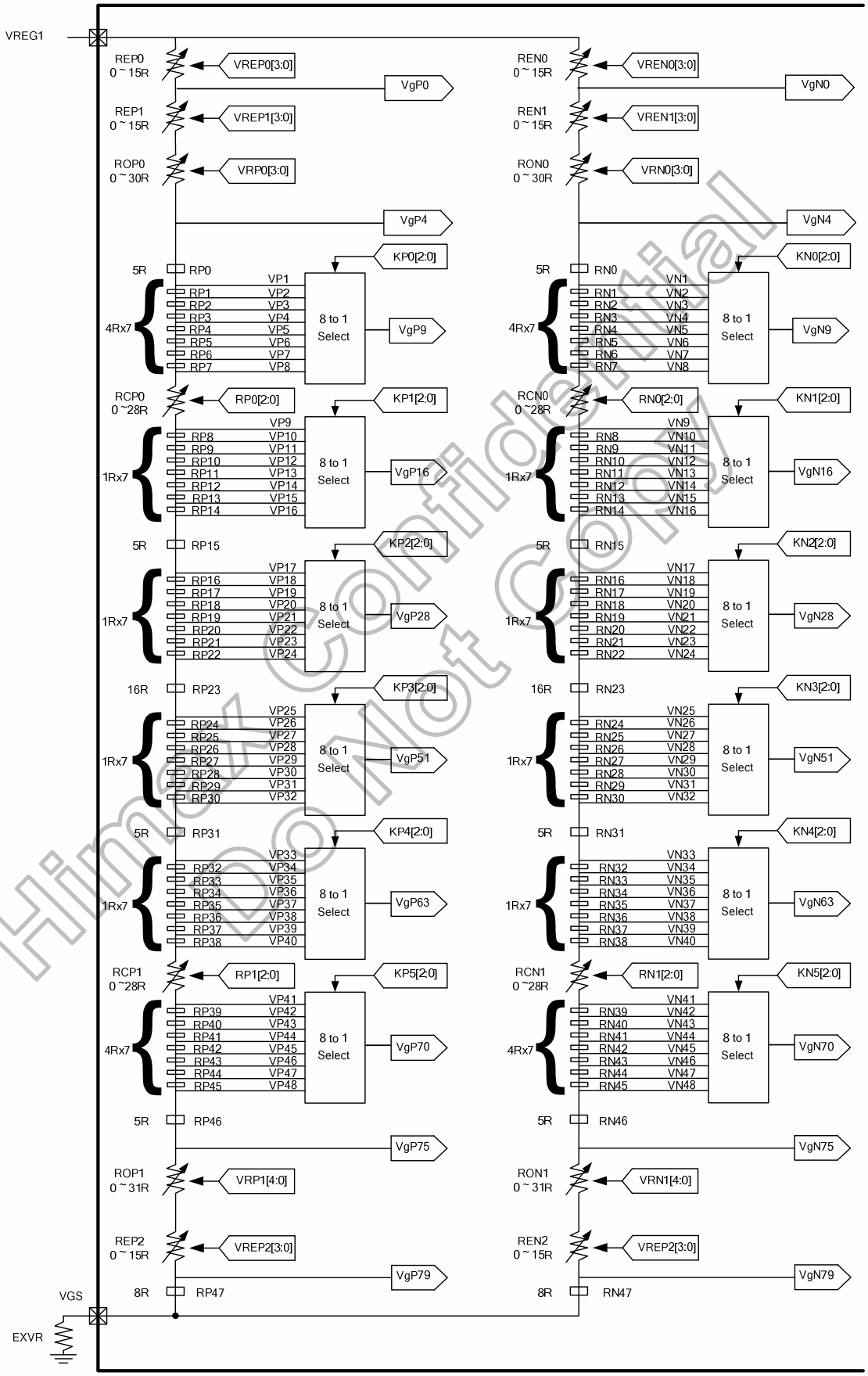


Figure 5.29: Gamma Resister Steam and Reference Voltage

5.7.1.2 Gamma Characteristics Adjustment Register

This HX8352-C01 has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

(1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resisters in the top and bottom of the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(2) Gamma center adjustment registers

The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 8 to 1 selector in the gamma resister stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 8-to-1 selectors (KP/N0~5), each of which has 8 inputs and generate one reference voltage output (VgP/N) 9, 16, 28, 51, 63, 70). These registers are available for both positive and negative polarities.

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	RP0 2-0	RN0 2-0	Variable resistor (RCP/N0) for center adjustment
	RP1 2-0	RN1 2-0	Variable resistor (RCP/N1) for center adjustment
Macro Adjustment	KP0 2-0	KN0 2-0	8-to-1 selector (voltage level of grayscale 70)
	KP1 2-0	KN1 2-0	8-to-1 selector (voltage level of grayscale 63)
	KP2 2-0	KN2 2-0	8-to-1 selector (voltage level of grayscale 51)
	KP3 2-0	KN3 2-0	8-to-1 selector (voltage level of grayscale 28)
	KP4 2-0	KN4 2-0	8-to-1 selector (voltage level of grayscale 16)
	KP5 2-0	KN5 2-0	8-to-1 selector (voltage level of grayscale 9)
Offset Adjustment	VRP0 3-0	VRN0 3-0	Variable resistor (ROP/N0) for offset adjustment
	VRP1 4-0	VRN1 4-0	Variable resistor (ROP/N1) for offset adjustment

Table 5.9: Gamma-Adjustment Registers

Variable Resister

There are three types of variable resistors, one is for center adjustment, one is for offset adjustment and the other one is for EEM adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment and EEM adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 3-0	Resistance RO(P/N)0	Value in Register VR(P/N)1 4-0	Resistance RO(P/N)1
0000	0R	00000	0R
0001	2R	00001	1R
0010	4R	00010	2R
• •	• •	• •	• •
1101	26R	11101	29R
1110	28R	11110	30R
1111	30R	11111	31R

Table 5.10: Offset Adjustment

Value in Register VRE(P/N)0 3-0	Resistance RE(P/N)0	Value in Register VRE(P/N)1 3-0	Resistance RE(P/N)1	Value in Register VRE(P/N)2 3-0	Resistance RE(P/N)2
0000	0R	0000	0R	0000	0R
0001	1R	0001	1R	0001	1R
0010	2R	0010	2R	0010	2R
• •	• •	• •	• •	• •	• •
1101	13R	1101	13R	1101	13R
1110	14R	1110	14R	1110	14R
1111	15R	1111	15R	1111	15R

Table 5.11: EEM Adjustment

Value in Register R(P/N)0 2-0	Resistance RC(P/N)0	Value in Register R(P/N)1 2-0	Resistance RC(P/N)1
000	0R	000	0R
001	4R	001	4R
010	8R	010	8R
• •	• •	• •	• •
101	20R	101	20R
110	24R	110	24R
111	28R	111	28R

Table 5.12: Center Adjustment

8 to 1 Selector

The 8 to 1 selector has eight input voltages generated by gamma resister stream. It outputs one reference voltages selected from inputs for gamma reference voltage generation by setting value in macro adjustment register. These six 8 to 1 selectors and the relationship are shown below.

Value in Register	Voltage level					
K(P/N) 2-0	Vg(P/N) 9	Vg(P/N) 16	Vg(P/N) 28	Vg(P/N) 51	V(P/N) 63	V(P/N) 70
000	VP(N)1	VP(N)9	VP(N)17	VP(N)25	VP(N)33	VP(N)41
001	VP(N)2	VP(N)10	VP(N)18	VP(N)26	VP(N)34	VP(N)42
010	VP(N)3	VP(N)11	VP(N)19	VP(N)27	VP(N)35	VP(N)43
011	VP(N)4	VP(N)12	VP(N)20	VP(N)28	VP(N)36	VP(N)44
100	VP(N)5	VP(N)13	VP(N)21	VP(N)29	VP(N)37	VP(N)45
101	VP(N)6	VP(N)14	VP(N)22	VP(N)30	VP(N)38	VP(N)46
110	VP(N)7	VP(N)15	VP(N)23	VP(N)31	VP(N)39	VP(N)47
111	VP(N)8	VP(N)16	VP(N)24	VP(N)32	VP(N)40	VP(N)48

Table 5.13: Output Voltage of 8 to 1 Selector

The grayscale levels are determined by the following formulas

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgP79	-	VD*(8R /sumRP) + VGS	-
VgP75	-	VD*(8R+REP2+ROP1)/sumRP + VGS	-
VgP70	KP5 2-0=111	VD*(13R+REP2+ROP1)/sumRP + VGS	VP48
	KP5 2-0=110	VD*(17R+REP2+ROP1)/sumRP + VGS	VP47
	KP5 2-0=101	VD*(21R+REP2+ROP1)/sumRP + VGS	VP46
	KP5 2-0=100	VD*(25R+REP2+ROP1)/sumRP + VGS	VP45
	KP5 2-0=011	VD*(29R+REP2+ROP1)/sumRP + VGS	VP44
	KP5 2-0=010	VD*(33R+REP2+ROP1)/sumRP + VGS	VP43
	KP5 2-0=001	VD*(37R+REP2+ROP1)/sumRP + VGS	VP42
	KP5 2-0=000	VD*(41R+REP2+ROP1)/sumRP + VGS	VP41
VgP63	KP4 2-0=111	VD*(41R+REP2+ROP1+RCP1)/sumRP + VGS	VP40
	KP4 2-0=110	VD*(42R+REP2+ROP1+RCP1)/sumRP + VGS	VP39
	KP4 2-0=101	VD*(43R+REP2+ROP1+RCP1)/sumRP + VGS	VP38
	KP4 2-0=100	VD*(44R+REP2+ROP1+RCP1)/sumRP + VGS	VP37
	KP4 2-0=011	VD*(45R+REP2+ROP1+RCP1)/sumRP + VGS	VP36
	KP4 2-0=010	VD*(46R+REP2+ROP1+RCP1)/sumRP + VGS	VP35
	KP4 2-0=001	VD*(47R+REP2+ROP1+RCP1)/sumRP + VGS	VP34
	KP4 2-0=000	VD*(48R+REP2+ROP1+RCP1)/sumRP + VGS	VP33
VgP51	KP3 2-0=111	VD*(53R+REP2+ROP1+RCP1)/sumRP + VGS	VP32
	KP3 2-0=110	VD*(54R+REP2+ROP1+RCP1)/sumRP + VGS	VP31
	KP3 2-0=101	VD*(55R+REP2+ROP1+RCP1)/sumRP + VGS	VP30
	KP3 2-0=100	VD*(56R+REP2+ROP1+RCP1)/sumRP + VGS	VP29
	KP3 2-0=011	VD*(57R+REP2+ROP1+RCP1)/sumRP + VGS	VP28
	KP3 2-0=010	VD*(58R+REP2+ROP1+RCP1)/sumRP + VGS	VP27
	KP3 2-0=001	VD*(59R+REP2+ROP1+RCP1)/sumRP + VGS	VP26
	KP3 2-0=000	VD*(60R+REP2+ROP1+RCP1)/sumRP + VGS	VP25
VgP28	KP2 2-0=111	VD*(76R+REP2+ROP1+RCP1)/sumRP + VGS	VP24
	KP2 2-0=110	VD*(77R+REP2+ROP1+RCP1)/sumRP + VGS	VP23
	KP2 2-0=101	VD*(78R+REP2+ROP1+RCP1)/sumRP + VGS	VP22
	KP2 2-0=100	VD*(79R+REP2+ROP1+RCP1)/sumRP + VGS	VP21
	KP2 2-0=011	VD*(80R+REP2+ROP1+RCP1)/sumRP + VGS	VP20
	KP2 2-0=010	VD*(81R+REP2+ROP1+RCP1)/sumRP + VGS	VP19
	KP2 2-0=001	VD*(82R+REP2+ROP1+RCP1)/sumRP + VGS	VP18
	KP2 2-0=000	VD*(83R+REP2+ROP1+RCP1)/sumRP + VGS	VP17
VgP16	KP1 2-0=111	VD*(88R+REP2+ROP1+RCP1)/sumRP + VGS	VP16
	KP1 2-0=110	VD*(89R+REP2+ROP1+RCP1)/sumRP + VGS	VP15
	KP1 2-0=101	VD*(90R+REP2+ROP1+RCP1)/sumRP + VGS	VP14
	KP1 2-0=100	VD*(91R+REP2+ROP1+RCP1)/sumRP + VGS	VP13
	KP1 2-0=011	VD*(92R+REP2+ROP1+RCP1)/sumRP + VGS	VP12
	KP1 2-0=010	VD*(93R+REP2+ROP1+RCP1)/sumRP + VGS	VP11
	KP1 2-0=001	VD*(94R+REP2+ROP1+RCP1)/sumRP + VGS	VP10
	KP1 2-0=000	VD*(95R+REP2+ROP1+RCP1)/sumRP + VGS	VP9
VgP9	KP0 2-0=111	VD*(95R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP8
	KP0 2-0=110	VD*(99R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP7
	KP0 2-0=101	VD*(103R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP6
	KP0 2-0=100	VD*(107R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP5
	KP0 2-0=011	VD*(111R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP4
	KP0 2-0=010	VD*(115R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP3
	KP0 2-0=001	VD*(119R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP2
	KP0 2-0=000	VD*(123R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	VP1
VgP4	-	VD*(128R+REP2+ROP1+RCP1+RCP0)/sumRP + VGS	-
VgP0	-	VD*(128R+ REP2+ROP1+RCP1+RCP0+ROP0+REP1)/sumRP + VGS	-

sumRP = 128R + REP0 + REP1 + ROP0 + RCP0 + RCP1 + ROP1 + REP2
sumRN = 128R + REN0 + REN1 + RON0 + RCN0 + RCN1 + RON1 + REN2
VD=(VREG1 -VGS)

Table 5.14: Voltage Calculation Formula (Positive Polarity)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgP4	V32	(11/23)*(VgP28-VgP51) + VgP51
V1	VgP9	V33	(10/23)*(VgP28-VgP51) + VgP51
V2	(30/48)*(VgP9-VgP16) + VgP16	V34	(9/23)*(VgP28-VgP51) + VgP51
V3	(23/48)*(VgP9-VgP16) + VgP16	V35	(8/23)*(VgP28-VgP51) + VgP51
V4	(16/48)*(VgP9-VgP16) + VgP16	V36	(7/23)*(VgP28-VgP51) + VgP51
V5	(12/48)*(VgP9-VgP16) + VgP16	V37	(6/23)*(VgP28-VgP51) + VgP51
V6	(8/48)*(VgP9-VgP16) + VgP16	V38	(5/23)*(VgP28-VgP51) + VgP51
V7	(4/48)*(VgP9-VgP16) + VgP16	V39	(4/23)*(VgP28-VgP51) + VgP51
V8	VgP16	V40	(3/23)*(VgP28-VgP51) + VgP51
V9	(22/24)*(VgP16-VgP28) + VgP28	V41	(2/23)*(VgP28-VgP51) + VgP51
V10	(20/24)*(VgP16-VgP28) + VgP28	V42	(1/23)*(VgP28-VgP51) + VgP51
V11	(18/24)*(VgP16-VgP28) + VgP28	V43	VgP51
V12	(16/24)*(VgP16-VgP28) + VgP28	V44	(22/24)*(VgP51-VgP63) + VgP63
V13	(14/24)*(VgP16-VgP28) + VgP28	V45	(20/24)*(VgP51-VgP63) + VgP63
V14	(12/24)*(VgP16-VgP28) + VgP28	V46	(18/24)*(VgP51-VgP63) + VgP63
V15	(10/24)*(VgP16-VgP28) + VgP28	V47	(16/24)*(VgP51-VgP63) + VgP63
V16	(8/24)*(VgP16-VgP28) + VgP28	V48	(14/24)*(VgP51-VgP63) + VgP63
V17	(6/24)*(VgP16-VgP28) + VgP28	V49	(12/24)*(VgP51-VgP63) + VgP63
V18	(4/24)*(VgP16-VgP28) + VgP28	V50	(10/24)*(VgP51-VgP63) + VgP63
V19	(2/24)*(VgP16-VgP28) + VgP28	V51	(8/24)*(VgP51-VgP63) + VgP63
V20	VgP28	V52	(6/24)*(VgP51-VgP63) + VgP63
V21	(22/23)*(VgP28-VgP51) + VgP51	V53	(4/24)*(VgP51-VgP63) + VgP63
V22	(21/23)*(VgP28-VgP51) + VgP51	V54	(2/24)*(VgP51-VgP63) + VgP63
V23	(20/23)*(VgP28-VgP51) + VgP51	V55	VgP63
V24	(19/23)*(VgP28-VgP51) + VgP51	V56	(44/48)*(VgP63-VgP70) + VgP70
V25	(18/23)*(VgP28-VgP51) + VgP51	V57	(40/48)*(VgP63-VgP70) + VgP70
V26	(17/23)*(VgP28-VgP51) + VgP51	V58	(36/48)*(VgP63-VgP70) + VgP70
V27	(16/23)*(VgP28-VgP51) + VgP51	V59	(32/48)*(VgP63-VgP70) + VgP70
V28	(15/23)*(VgP28-VgP51) + VgP51	V60	(25/48)*(VgP63-VgP70) + VgP70
V29	(14/23)*(VgP28-VgP51) + VgP51	V61	(18/48)*(VgP63-VgP70) + VgP70
V30	(13/23)*(VgP28-VgP51) + VgP51	V62	VgP70
V31	(12/23)*(VgP28-VgP51) + VgP51	V63	VgP75

Table 5.15: Voltage Calculation Formula of Grayscale Voltage (Positive Polarity)

Reference Voltage	Macro Adjustment Value	Formula	Pin
VgN79	-	VD*(8R /sumRN) + VGS	-
VgN75	-	VD*(8R+REN2+RON1)/sumRN + VGS	-
VgN70	KN5 2-0=111	VD*(13R+REN2+RON1)/sumRN + VGS	VN48
	KN5 2-0=110	VD*(17R+REN2+RON1)/sumRN + VGS	VN47
	KN5 2-0=101	VD*(21R+REN2+RON1)/sumRN + VGS	VN46
	KN5 2-0=100	VD*(25R+REN2+RON1)/sumRN + VGS	VN45
	KN5 2-0=011	VD*(29R+REN2+RON1)/sumRN + VGS	VN44
	KN5 2-0=010	VD*(33R+REN2+RON1)/sumRN + VGS	VN43
	KN5 2-0=001	VD*(37R+REN2+RON1)/sumRN + VGS	VN42
	KN5 2-0=000	VD*(41R+REN2+RON1)/sumRN + VGS	VN41
VgN63	KN4 2-0=111	VD*(41R+REN2+RON1+RCN1)/sumRN + VGS	VN40
	KN4 2-0=110	VD*(42R+REN2+RON1+RCN1)/sumRN + VGS	VN39
	KN4 2-0=101	VD*(43R+REN2+RON1+RCN1)/sumRN + VGS	VN38
	KN4 2-0=100	VD*(44R+REN2+RON1+RCN1)/sumRN + VGS	VN37
	KN4 2-0=011	VD*(45R+REN2+RON1+RCN1)/sumRN + VGS	VN36
	KN4 2-0=010	VD*(46R+REN2+RON1+RCN1)/sumRN + VGS	VN35
	KN4 2-0=001	VD*(47R+REN2+RON1+RCN1)/sumRN + VGS	VN34
	KN4 2-0=000	VD*(48R+REN2+RON1+RCN1)/sumRN + VGS	VN33
VgN51	KN3 2-0=111	VD*(53R+REN2+RON1+RCN1)/sumRN + VGS	VN32
	KN3 2-0=110	VD*(54R+REN2+RON1+RCN1)/sumRN + VGS	VN31
	KN3 2-0=101	VD*(55R+REN2+RON1+RCN1)/sumRN + VGS	VN30
	KN3 2-0=100	VD*(56R+REN2+RON1+RCN1)/sumRN + VGS	VN29
	KN3 2-0=011	VD*(57R+REN2+RON1+RCN1)/sumRN + VGS	VN28
	KN3 2-0=010	VD*(58R+REN2+RON1+RCN1)/sumRN + VGS	VN27
	KN3 2-0=001	VD*(59R+REN2+RON1+RCN1)/sumRN + VGS	VN26
	KN3 2-0=000	VD*(60R+REN2+RON1+RCN1)/sumRN + VGS	VN25
VgN28	KN2 2-0=111	VD*(76R+REN2+RON1+RCN1)/sumRN + VGS	VN24
	KN2 2-0=110	VD*(77R+REN2+RON1+RCN1)/sumRN + VGS	VN23
	KN2 2-0=101	VD*(78R+REN2+RON1+RCN1)/sumRN + VGS	VN22
	KN2 2-0=100	VD*(79R+REN2+RON1+RCN1)/sumRN + VGS	VN21
	KN2 2-0=011	VD*(80R+REN2+RON1+RCN1)/sumRN + VGS	VN20
	KN2 2-0=010	VD*(81R+REN2+RON1+RCN1)/sumRN + VGS	VN19
	KN2 2-0=001	VD*(82R+REN2+RON1+RCN1)/sumRN + VGS	VN18
	KN2 2-0=000	VD*(83R+REN2+RON1+RCN1)/sumRN + VGS	VN17
VgN16	KN1 2-0=111	VD*(88R+REN2+RON1+RCN1)/sumRN + VGS	VN16
	KN1 2-0=110	VD*(89R+REN2+RON1+RCN1)/sumRN + VGS	VN15
	KN1 2-0=101	VD*(90R+REN2+RON1+RCN1)/sumRN + VGS	VN14
	KN1 2-0=100	VD*(91R+REN2+RON1+RCN1)/sumRN + VGS	VN13
	KN1 2-0=011	VD*(92R+REN2+RON1+RCN1)/sumRN + VGS	VN12
	KN1 2-0=010	VD*(93R+REN2+RON1+RCN1)/sumRN + VGS	VN11
	KN1 2-0=001	VD*(94R+REN2+RON1+RCN1)/sumRN + VGS	VN10
	KN1 2-0=000	VD*(95R+REN2+RON1+RCN1)/sumRN + VGS	VN9
VgN9	KN0 2-0=111	VD*(95R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN8
	KN0 2-0=110	VD*(99R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN7
	KN0 2-0=101	VD*(103R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN6
	KN0 2-0=100	VD*(107R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN5
	KN0 2-0=011	VD*(111R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN4
	KN0 2-0=010	VD*(115R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN3
	KN0 2-0=001	VD*(119R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN2
	KN0 2-0=000	VD*(123R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	VN1
VgN4	-	VD*(128R+REN2+RON1+RCN1+RCN0)/sumRN + VGS	-
VgN0	-	VD*(128R+ REN2+RON1+RCN1+RCN0+RON0+REN1)/sumRN + VGS	-

sumRP = 128R + REP0 + REP1 + ROP0 + RCP0 + RCP1 + ROP1 + REP2
sumRN = 128R + REN0 + REN1 + RON0 + RCN0 + RCN1 + RON1 + REN2
VD=(VREG1 -VGS)

Table 5.16: Voltage Calculation Formula (Negative Polarity)

Grayscale Voltage	Formula	Grayscale Voltage	Formula
V0	VgN4	V32	(11/23)*(VgN28-VgN51) + VgN51
V1	VgN9	V33	(10/23)*(VgN28-VgN51) + VgN51
V2	(30/48)*(VgN9-VgN16) + VgN16	V34	(9/23)*(VgN28-VgN51) + VgN51
V3	(23/48)*(VgN9-VgN16) + VgN16	V35	(8/23)*(VgN28-VgN51) + VgN51
V4	(16/48)*(VgN9-VgN16) + VgN16	V36	(7/23)*(VgN28-VgN51) + VgN51
V5	(12/48)*(VgN9-VgN16) + VgN16	V37	(6/23)*(VgN28-VgN51) + VgN51
V6	(8/48)*(VgN9-VgN16) + VgN16	V38	(5/23)*(VgN28-VgN51) + VgN51
V7	(4/48)*(VgN9-VgN16) + VgN16	V39	(4/23)*(VgN28-VgN51) + VgN51
V8	VgN16	V40	(3/23)*(VgN28-VgN51) + VgN51
V9	(22/24)*(VgN16-VgN28) + VgN28	V41	(2/23)*(VgN28-VgN51) + VgN51
V10	(20/24)*(VgN16-VgN28) + VgN28	V42	(1/23)*(VgN28-VgN51) + VgN51
V11	(18/24)*(VgN16-VgN28) + VgN28	V43	VgN51
V12	(16/24)*(VgN16-VgN28) + VgN28	V44	(22/24)*(VgN51-VgN63) + VgN63
V13	(14/24)*(VgN16-VgN28) + VgN28	V45	(20/24)*(VgN51-VgN63) + VgN63
V14	(12/24)*(VgN16-VgN28) + VgN28	V46	(18/24)*(VgN51-VgN63) + VgN63
V15	(10/24)*(VgN16-VgN28) + VgN28	V47	(16/24)*(VgN51-VgN63) + VgN63
V16	(8/24)*(VgN16-VgN28) + VgN28	V48	(14/24)*(VgN51-VgN63) + VgN63
V17	(6/24)*(VgN16-VgN28) + VgN28	V49	(12/24)*(VgN51-VgN63) + VgN63
V18	(4/24)*(VgN16-VgN28) + VgN28	V50	(10/24)*(VgN51-VgN63) + VgN63
V19	(2/24)*(VgN16-VgN28) + VgN28	V51	(8/24)*(VgN51-VgN63) + VgN63
V20	VgN28	V52	(6/24)*(VgN51-VgN63) + VgN63
V21	(22/23)*(VgN28-VgN51) + VgN51	V53	(4/24)*(VgN51-VgN63) + VgN63
V22	(21/23)*(VgN28-VgN51) + VgN51	V54	(2/24)*(VgN51-VgN63) + VgN63
V23	(20/23)*(VgN28-VgN51) + VgN51	V55	VgN63
V24	(19/23)*(VgN28-VgN51) + VgN51	V56	(44/48)*(VgN63-VgN70) + VgN70
V25	(18/23)*(VgN28-VgN51) + VgN51	V57	(40/48)* (VgN63-VgN70) + VgN70
V26	(17/23)*(VgN28-VgN51) + VgN51	V58	(36/48)* (VgN63-VgN70) + VgN70
V27	(16/23)*(VgN28-VgN51) + VgN51	V59	(32/48)* (VgN63-VgN70) + VgN70
V28	(15/23)*(VgN28-VgN51) + VgN51	V60	(25/48)* (VgN63-VgN70) + VgN70
V29	(14/23)*(VgN28-VgN51) + VgN51	V61	(18/48)* (VgN63-VgN70) + VgN70
V30	(13/23)*(VgN28-VgN51) + VgN51	V62	VgN70
V31	(12/23)*(VgN28-VgN51) + VgN51	V63	VgN75

Table 5.17: Voltage Calculation Formula of Grayscale Voltage (Negative Polarity)

5.7.1.3 Relationship between data and output voltages

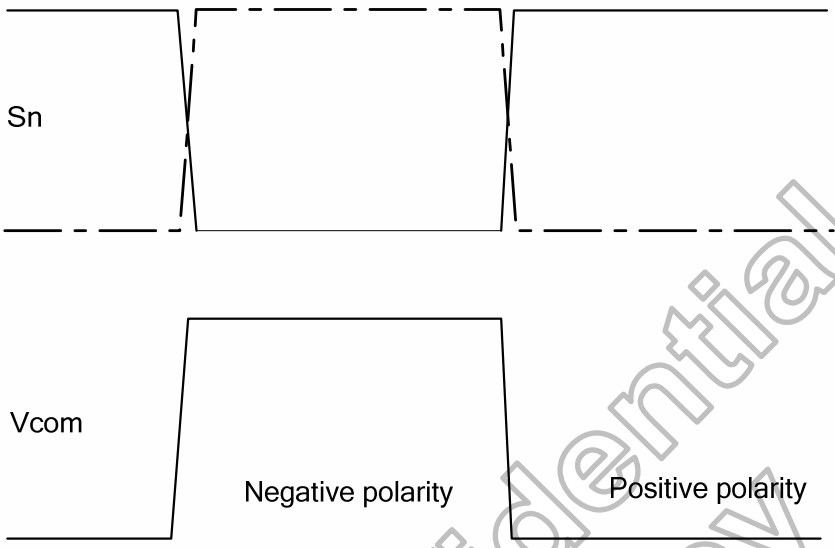


Figure 5.30: Relationship between source output and Vcom

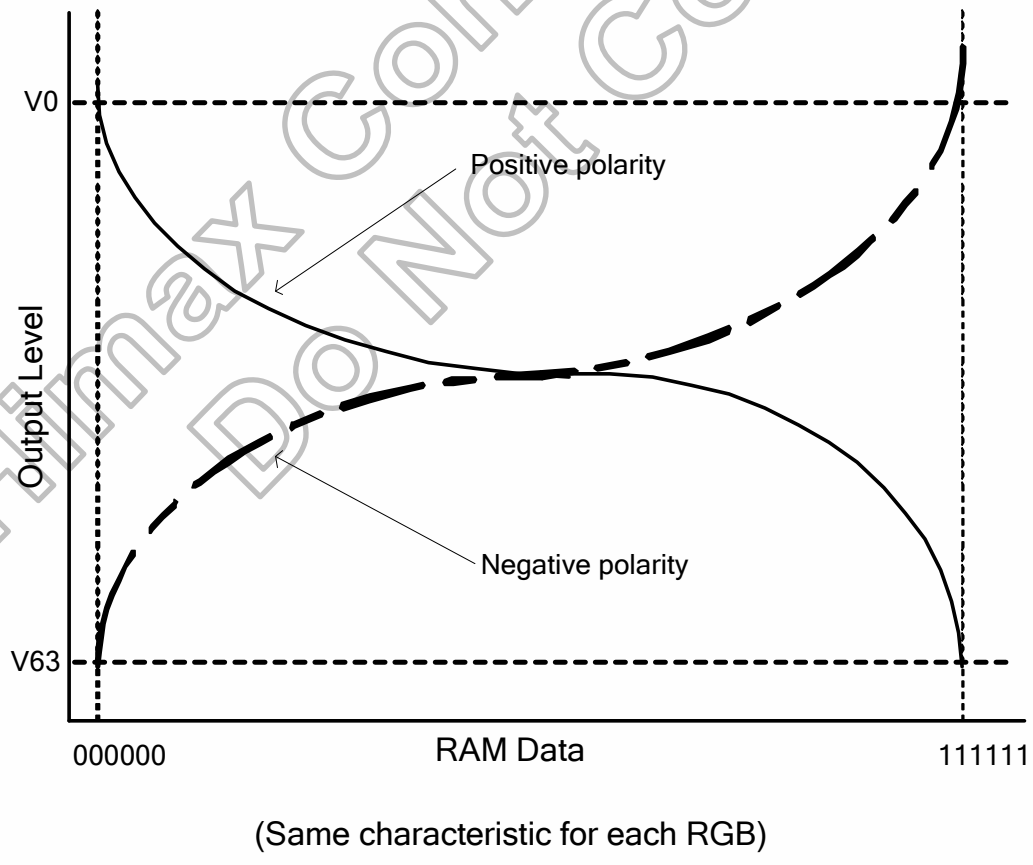


Figure 5.31: Relationship between data and output level, REV =0, normal white

5.7.2 Gray Voltage Generator for Digital Gamma Correction

The HX8352-C01 digital gamma correction can reach the independent GAMMA curve of RGB. HX8352-C01 utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 6-bit into 8-bit and sends 8-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

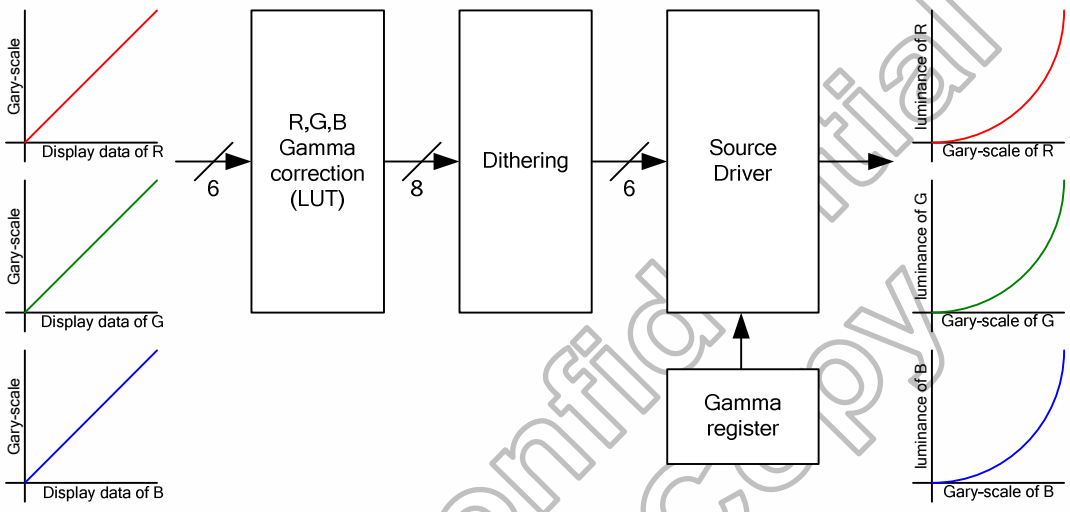


Figure 5.32: Block Diagram of Digital Gamma Correction

The HX8352-C01 builds one 99-bytes DGC_LUT (Digital Gamma Correction Look Up Table) to transfer every display data of Dithering circuit input and setting by DGC_LUT register.

LUT	D7	D6	D5	D4	D3	D2	D1	D0	Default	Gray Mapping
1st	R007	R006	R005	R004	R003	R002	R001	R000	00h	R_V0
2nd	R017	R016	R015	R014	R013	R012	R011	R010	08h	R_V2
3rd	R027	R026	R025	R024	R023	R022	R021	R020	10h	R_V4
:	:	:	:	:	:	:	:	:	:	:
32nd	R317	R316	R315	R314	R313	R312	R311	R310	F8h	R_V62
33rd	R327	R326	R325	R324	R323	R322	R321	R320	FCh	R_V63
34th	G007	G006	G005	G004	G003	G002	G001	G000	00h	G_V0
35th	G017	G016	G015	G014	G013	G012	G011	G010	08h	G_V2
36th	G027	G026	G025	G024	G023	G022	G021	G020	10h	G_V4
:	:	:	:	:	:	:	:	:	:	:
65th	G317	G316	G315	G314	G313	G312	G311	G310	F8h	G_V62
66th	G327	G326	G325	G324	G323	G322	G321	G320	FCh	G_V63
67th	B007	B006	B005	B004	B003	B002	B001	B000	00h	B_V0
68th	B017	B016	B015	B014	B013	B012	B011	B010	08h	B_V2
69th	B027	B026	B025	B024	B023	B022	B021	B020	10h	B_V4
:	:	:	:	:	:	:	:	:	:	:
98th	B317	B316	B315	B314	B313	B312	B311	B310	F8h	B_V62
99th	B327	B326	B325	B324	B323	B322	B321	B320	FCh	B_V63

Table 5.18: DGC LUT

5.8 Characteristics of I/O

5.8.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE	Low	Low	Low
CABC_PWM_OUT	Low	Low	Low
LEDON	Low	Low	Low
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDI_SDA	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Table 5.19: Characteristics of output or bi-directional (I/O) pins

5.8.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
NRESET	Setion.5.10	Input valid	Input valid	Input valid	Setion.5.10
NCS	Input valid	Input valid	Input valid	Input valid	Input valid
DNC	Input valid	Input valid	Input valid	Input valid	Input valid
NWR_SCL	Input valid	Input valid	Input valid	Input valid	Input valid
NRD	Input valid	Input valid	Input valid	Input valid	Input valid
DB17 to DB0 SDI_SDA	Input valid	Input valid	Input valid	Input valid	Input valid
HSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
VSYNC	Input valid	Input valid	Input valid	Input valid	Input valid
PCLK	Input valid	Input valid	Input valid	Input valid	Input valid
DE	Input valid	Input valid	Input valid	Input valid	Input valid
OSC, IFSEL, IM2, IM1, IM0,	Input valid	Input valid	Input valid	Input valid	Input valid
TEST2-1	Low	Low	Low	Low	Low

Table 5.20: Characteristics of input pins

5.9 Power on/off sequence

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order. During power off, if LCD is in the Sleep Out mode, IOVCC must be powered down minimum 120msec after NRESET has been released. During power off, if LCD is in the Standby mode, IOVCC and VCI can be powered down minimum 0msec after NRESET has been released. NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving STB Out command. Also between receiving STB In command and Power Off Sequence. If NRESET line is not held stable by host during Power On Sequence as defined in Sections 5.9.1 and 5.9.2, then it will be necessary to apply a Hardware Reset (NRESET) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

5.9.1 Case 1: NRESET line is held high or unstable by host at power on

If NRESET line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both IOVCC and VCI have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

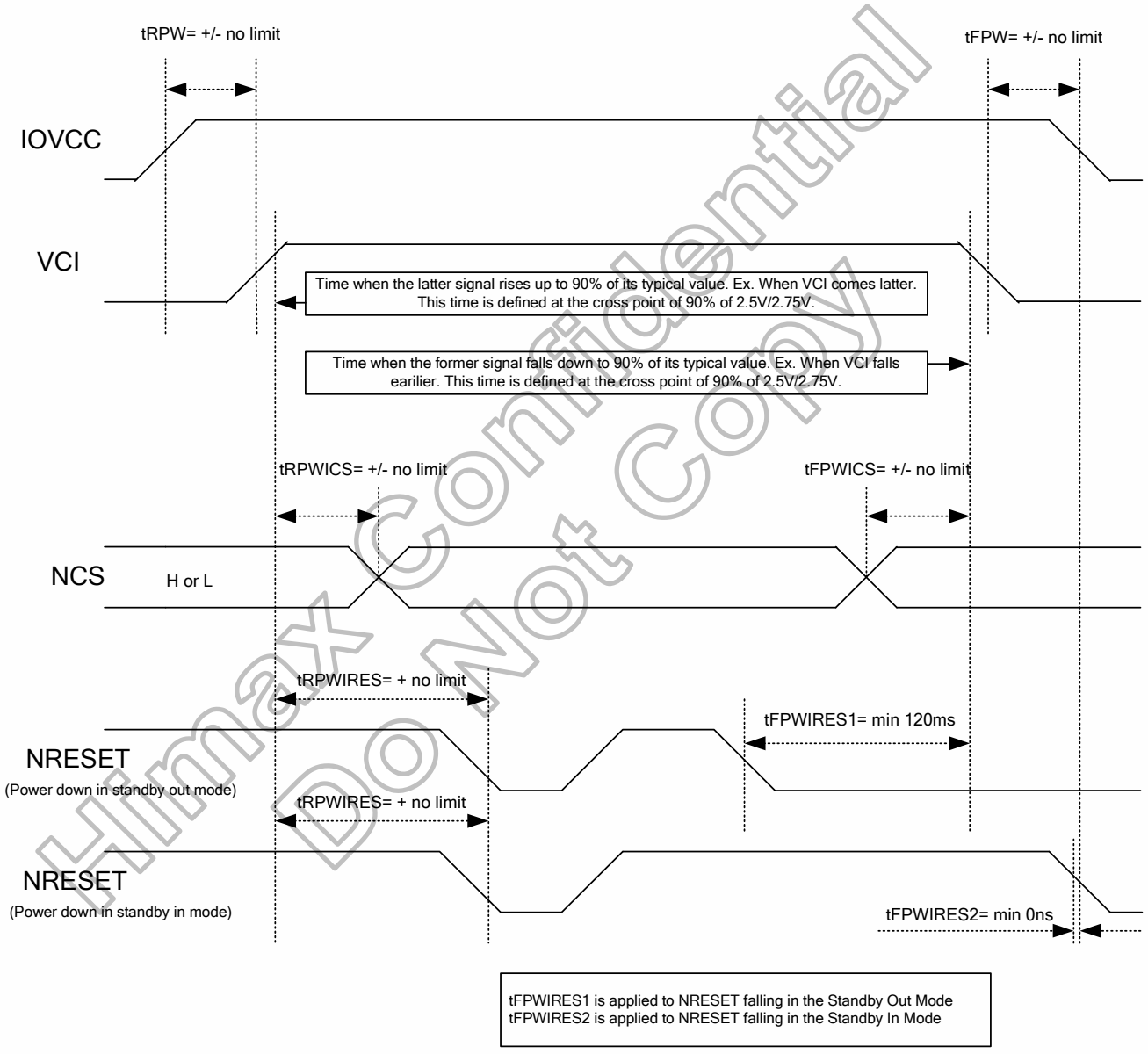


Figure 5.33: Case 1: NRESET line is held high or unstable by host at power on

5.9.2 Case 2: NRESET line is held low by host at power on

If NRESET line is held low (and stable) by the host during power on, then the NRESET must be held low for minimum 10µsec after both IOVCC and VCI have been applied.

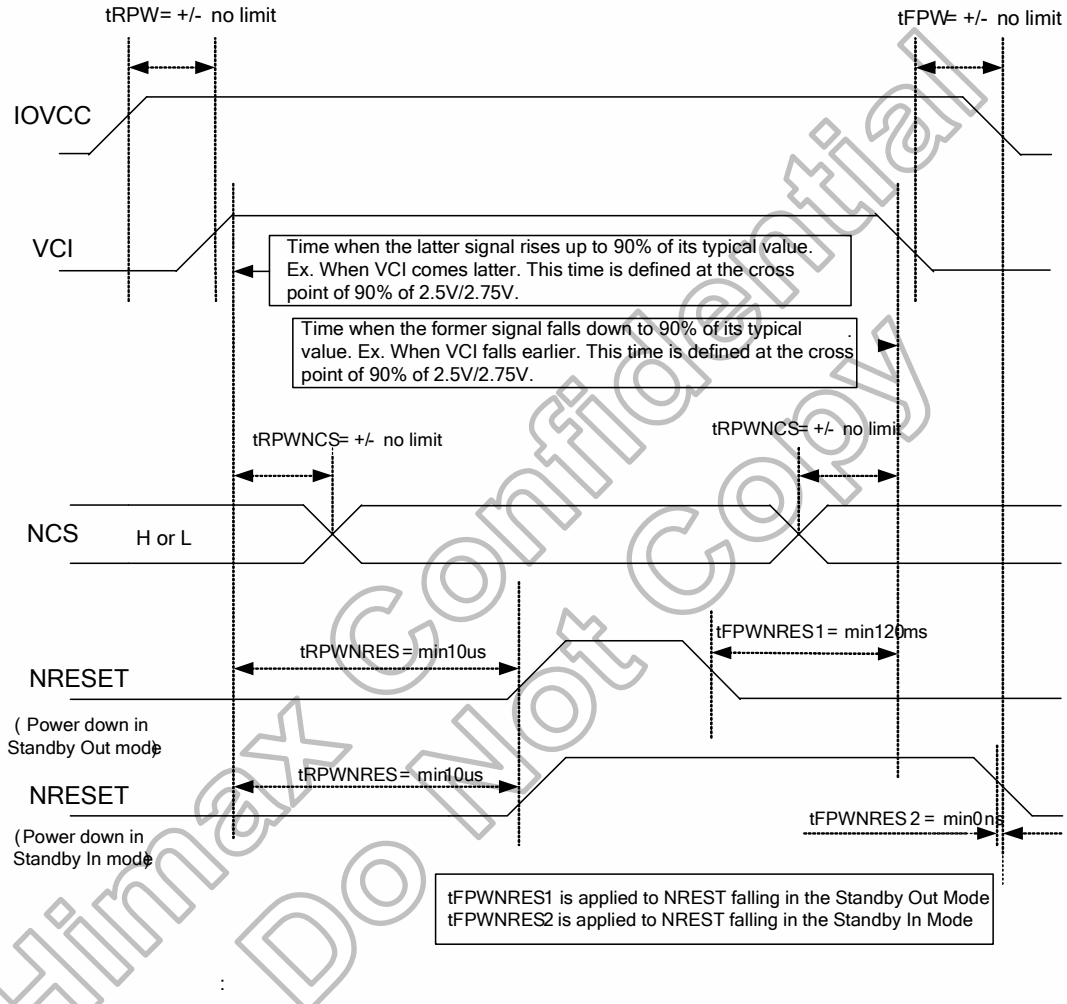


Figure 5.34: Case 2: NRESET line is held low by host at power on

5.10 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

5.11 Power On/Off Sequence

The following are the sequences of register setting flow that applied to this driver driving the TFT display, when operate in Register-Content interface mode.

Display On/Off Set flow

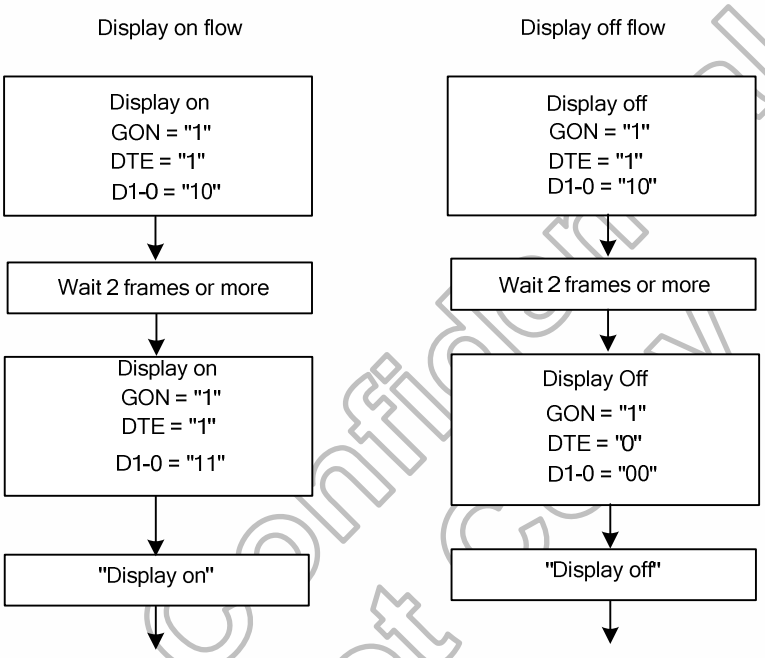


Figure 5.35: Display On/Off Set flow

Standby Mode Set up Flow

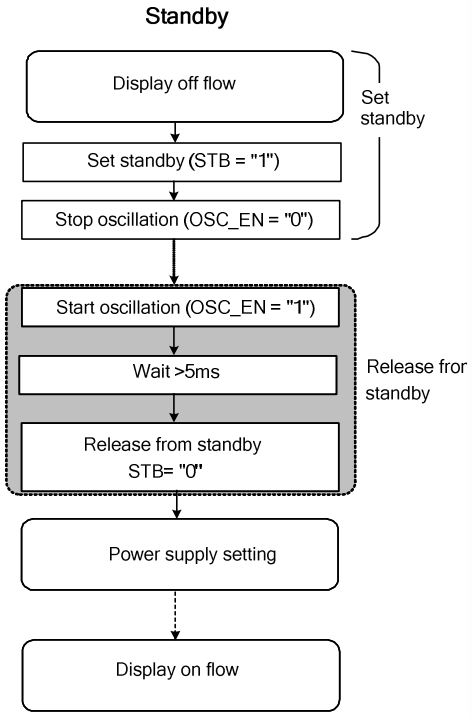


Figure 5.36: Standby Mode Setting flow

Deep Standby Mode Set up Flow

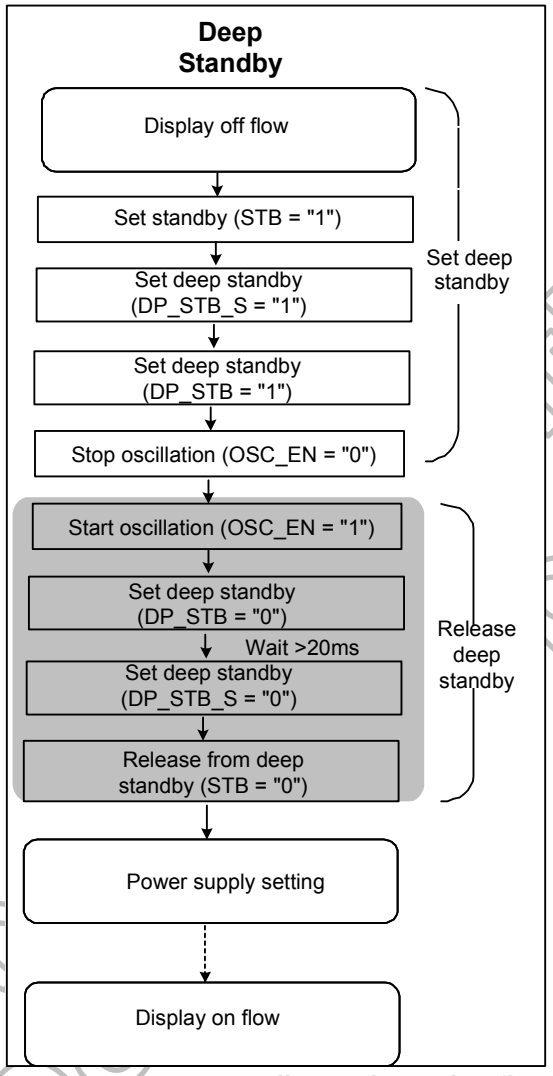


Figure 5.37: Deep Standby Mode Setting flow

Power On/Off Setting up Flow

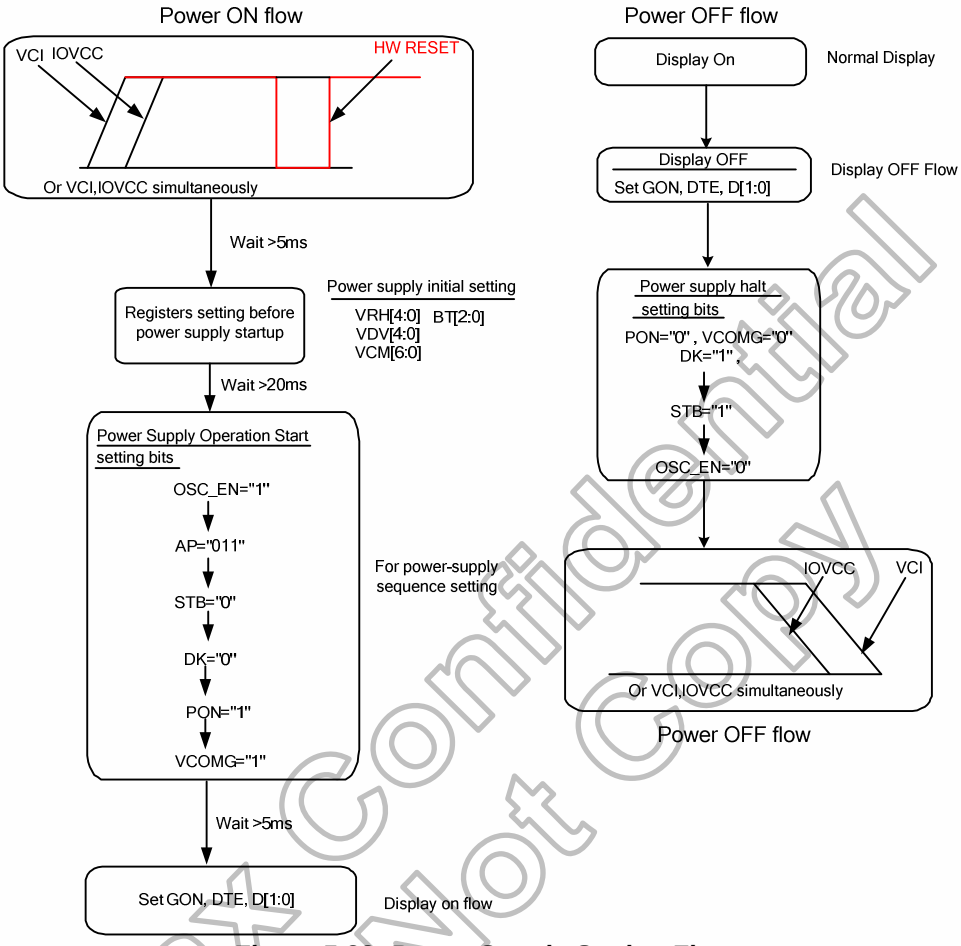


Figure 5.38: Power Supply Setting Flow

5.12 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

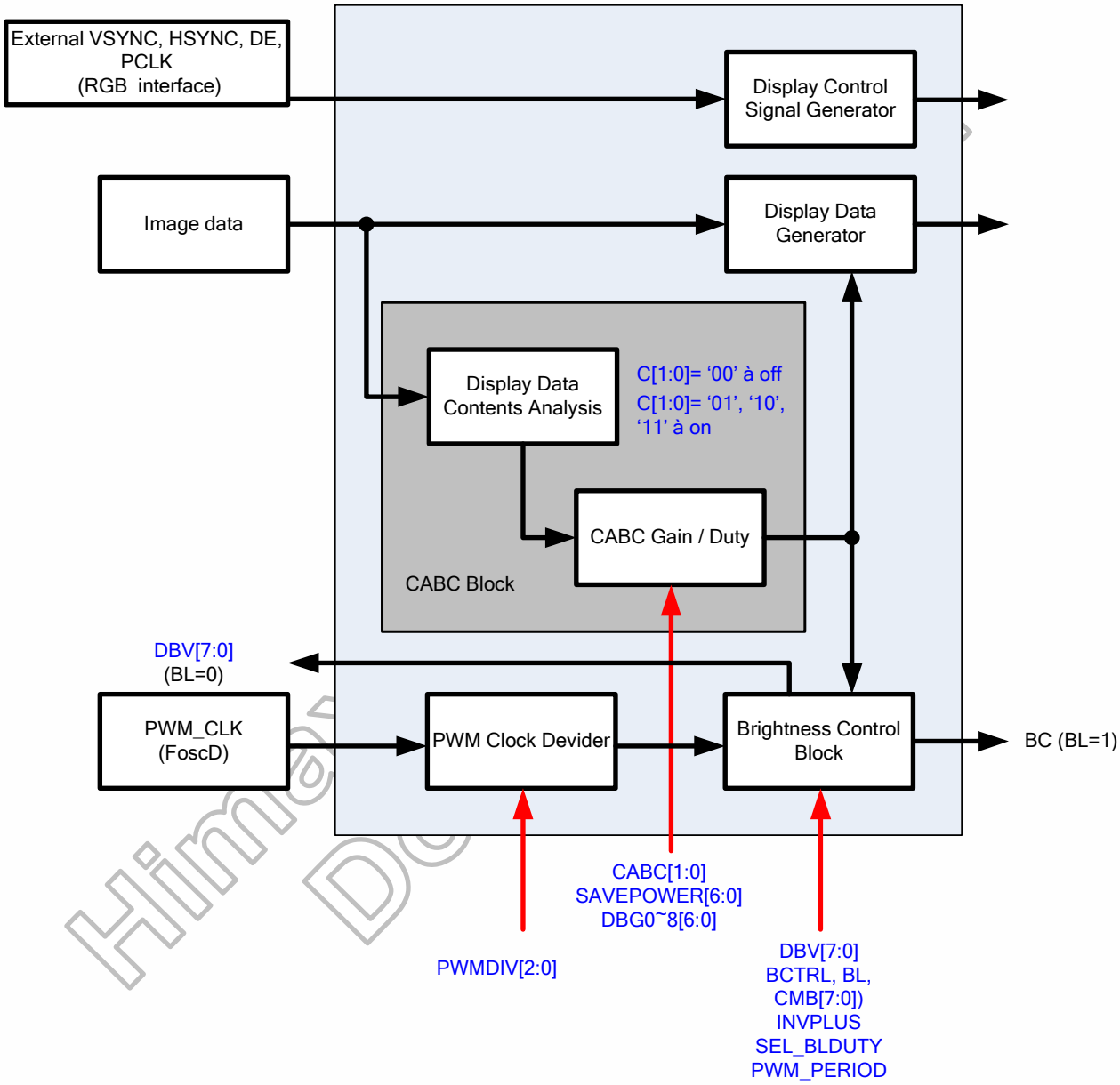
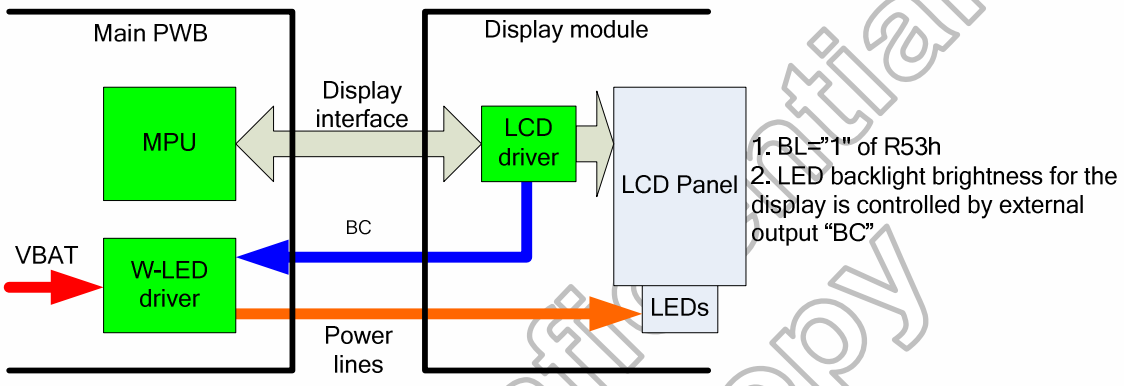


Figure 5.39: CABC block diagram

5.12.1 Module architectures

HX8352-C01 can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- Architecture I



- Architecture II

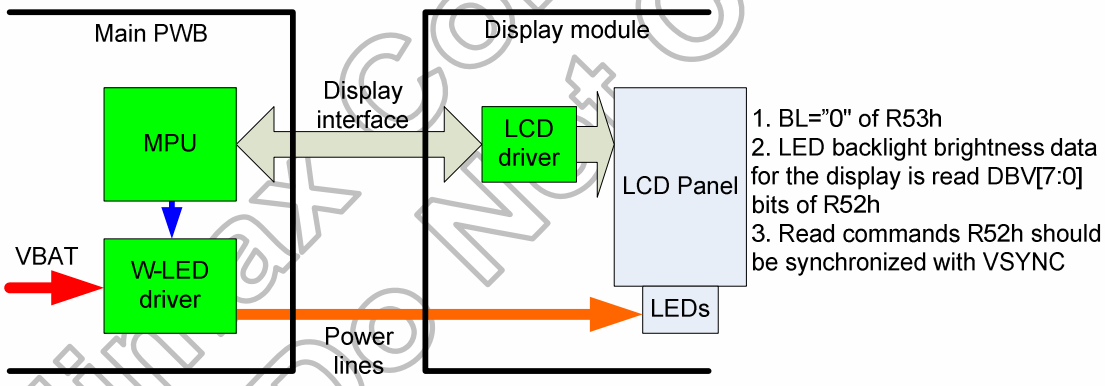


Figure 5.40: Module architecture

5.12.2 CABC block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that : Duty (valid level period (LED on) / one complete period)=1/ gain.

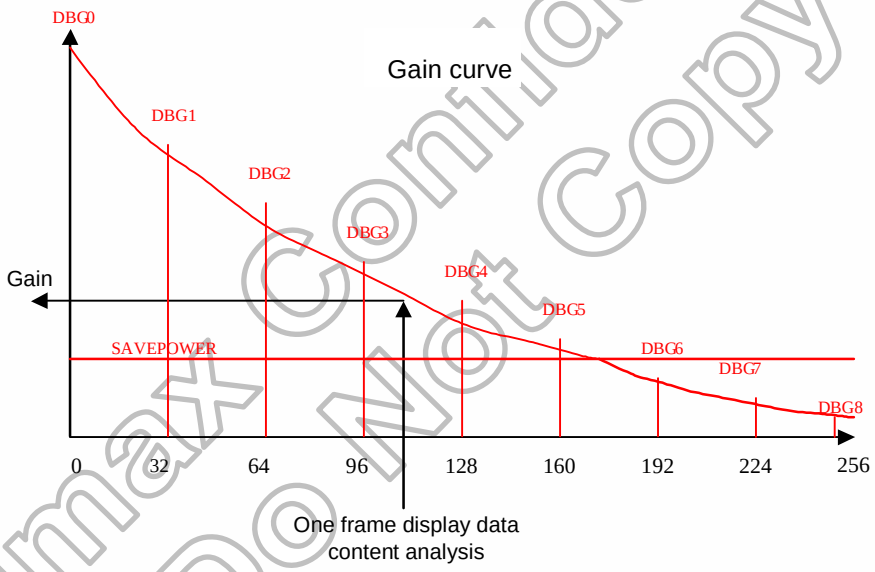


Figure 5.41: CABC gain / CABC duty generation

For power saving of backlight module, there are SAVEPOWER[6:0] bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain / duty after one-frame display data contents analysis is smaller(gain) / larger(duty) than SAVEPOWER[6:0] bits setting, the CABC block will output CABC gain / duty equal to SAVEPOWER[6:0] and ignore the result of display data contents analysis.

5.12.3 Brightness control block

There is an external output signal(CABC_PWM_OUT) from brightness block to control the LED driver IC in order to control display brightness.

There are resister bits DBV[7:0] for display brightness of manual brightness setting. The CABC_PWM_OUT output duty is calculated as (DBV[7:0])/255 x CABC duty (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT output period=2.95 ms, and DBV[7:0](R51h)='228DEC' and CABC duty is 74.42%. Then CABC_PWM_OUT output duty=(228) / 255 x 74.42%≡66.54%. Correspond to the CABC_PWM_OUT output period=2.95 ms, the high-level of CABC_PWM_OUT output (high effective) = 1.96ms, and the low-level of BC output =0.99ms.

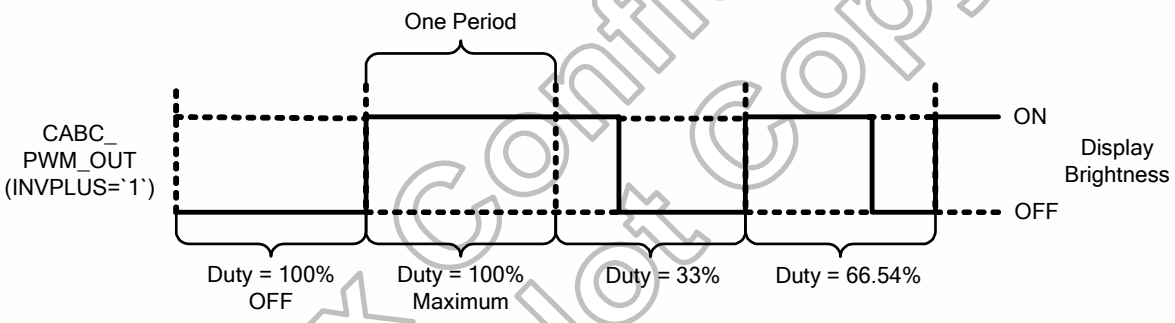


Figure 5.42: CABC_PWM_OUT output duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Table 5.21: CABC timing table

Note1: The signal rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.
Note2: The pulse width range by setting CABC related registers is locate between 0.0333ms to 8.33ms.

When Architecture II module is used (BL='0') with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0] will be read a value as 169DEC ((169)/255≡ 66.27%).

5.12.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (CMB[7:0] bits) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=’0’), CABC minimum brightness setting is ignored. “CMB[7:0], Read CABC minimum brightness“ always read the setting value of “CMB[7:0], Write CABC minimum brightness”

5.13 OTP programing

5.13.1 OTP table

PA	D7	D6	D5	D4	D3	D2	D1	D0	Command Set
00	ID1[7:0]								-
01	ID2[7:0]								-
02	ID3[7:0]								-
03	ID1[7:0]								-
04	ID2[7:0]								-
05	ID3[7:0]								-
06	ID1[7:0]								-
07	ID2[7:0]								-
08	ID3[7:0]								-
09	ID1[7:0]								-
0A	ID2[7:0]								-
0B	ID3[7:0]								-
0C	ID1[7:0]								-
0D	ID2[7:0]								-
0E	ID3[7:0]								-
0F	ID1[7:0]								-
10	ID2[7:0]								-
11	ID3[7:0]								-
12	ID1[7:0]								-
13	ID2[7:0]								-
14	ID3[7:0]								-
15	ID1[7:0]								-
16	ID2[7:0]								-
17	ID3[7:0]								-
18	nValid_ID8	nValid_ID7	nValid_ID6	nValid_ID5	nValid_ID4	nValid_ID3	nValid_ID2	nValid_ID1	-
19	nValid_VCM1	VCM[6:0]							-
1A	No used			VDV[4:0]					-
1B	nValid_VCM2	VCM[6:0]							-
1C	No used			VDV[4:0]					-
1D	nValid_VCM3	VCM[6:0]							-
1E	No used			VDV[4:0]					-
1F	nValid_VCM4	VCM[6:0]							-
20	No used			VDV[4:0]					-
21	nValid_VCM5	VCM[6:0]							-
22	No used			VDV[4:0]					-
23	nValid_VCM6	VCM[6:0]							-
24	No used			VDV[4:0]					-
25	nValid_VCM7	VCM[6:0]							-
26	No used			VDV[4:0]					-
27	nValid_VCM8	VCM[6:0]							-
28	No used			VDV[4:0]					-
29	nValid_PANEL	No used		REV	SM	GS	BGR	SS	-
2A	nValid_GAM	KP1[2:0]			No used	KP0[2:0]			-
2B	No used	KP3[2:0]			No used	KP2[2:0]			-
2C	No used	KP5[2:0]			No used	KP4[2:0]			-
2D	No used	RP1[2:0]			No used	RP0[2:0]			-
2E	No used				VRP0[3:0]				-
2F	No used			VRP1[4:0]					-
30	No used	KN1[2:0]			No used	KN0[2:0]			-
31	No used	KN3[2:0]			No used	KN2[2:0]			-
32	No used	KN5[2:0]			No used	KN4[2:0]			-
33	No used	RN1[2:0]			No used	RN0[2:0]			-
34	No used				VRN0[3:0]				-
35	No used			VRN1[4:0]					-
36	VREP1[3:0]				VREP0[3:0]				-
37	VREN0[3:0]				VREP2[3:0]				-
38	VREN2[3:0]				VREN1[3:0]				-

Note: (1) The same color means the same nVALID bit controlled. When OTP Index programmed, the related nVALID bit will be programmed to “0” automatically. If the nVALID bit programmed to “0”, the OTP value will be reload to related register after HW reset or SLPOUT command.

(2) If want to program ID1~ID3, it just need to program Index 00h (ID2 and ID3 will be programmed automatically). If ID had be programmed, it also need to program Index 00h when second to eighth times programming(it will

be programmed to corresponding Index automatically).

(3) If want to program VCOM, it just need to program Index 19h (VDV will be programmed automatically). If VCOM had be programmed, it also need to program Index 19h when second to eighth times programming(it will be programmed to corresponding Index automatically).

5.13.2 OTP programming flow

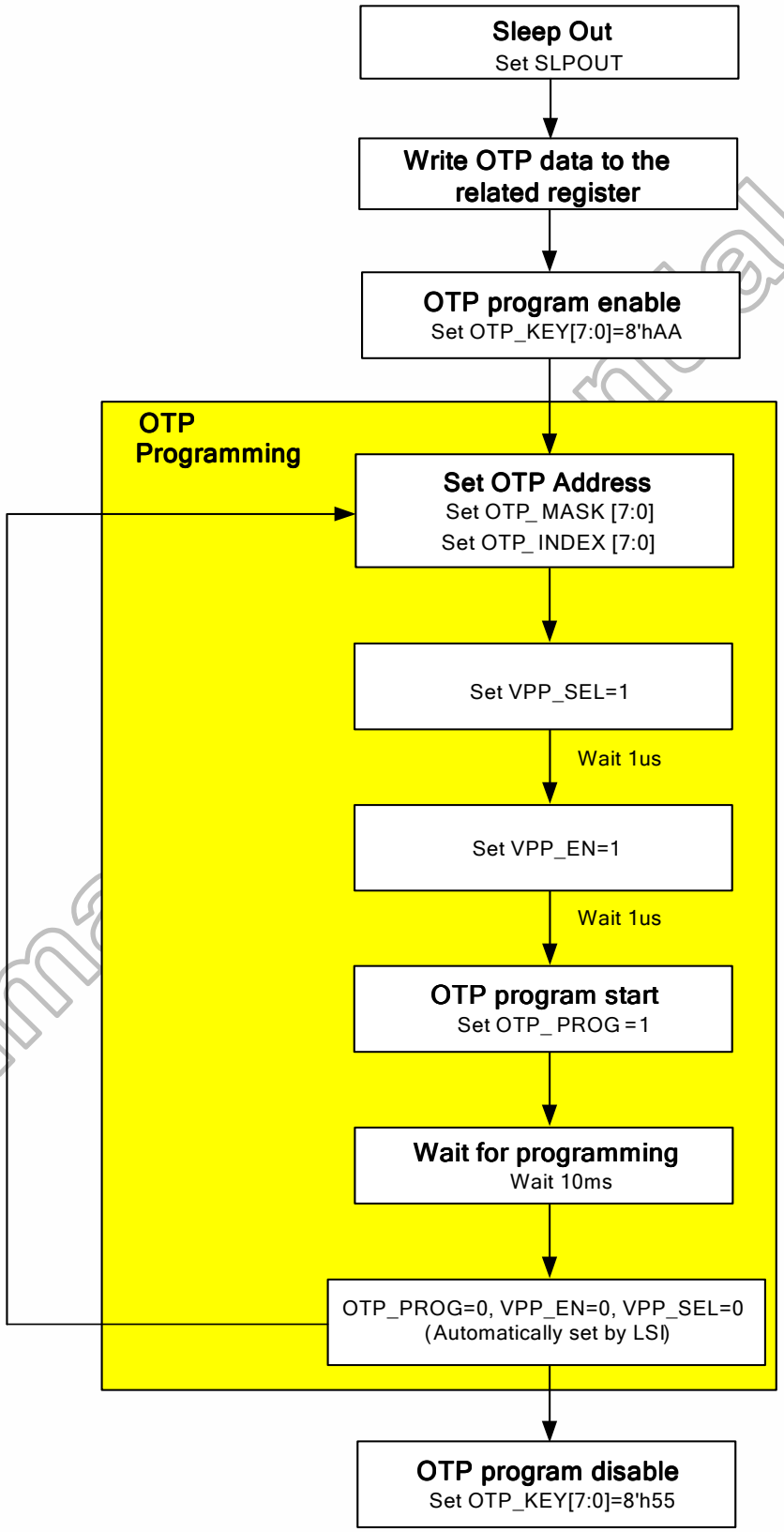


Figure 5.43: OTP programming sequence

5.13.3 Programming sequence

Step	Operation
1	Power on and reset the module.
2	SLPOUT
3	Set VPP power to 7.5V for OTP programming state.
4	Write optimized values to related registers.
5	Set OTP_KEY[7:0] (REBh)=0xAAh to enter OTP program mode.
6	Specify OTP_INDEX, please refer to the OTP table.
7	Set OTP_MASK[7:0]=0x00h, programming the entire bit of one parameter.
8	Set VPP_SEL=1
9	Wait 1 us
10	Set VPP_EN=1
11	Wait 1 us
12	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_INDEX.
13	Wait 10 ms
14	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (6). Otherwise, set OTP_KEY[7:0] (RBBh)=0x55h to leave OTP program mode and power off the module.

Table 5.22: OTP Programming sequence

6. Command

6.1 Command list

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	Himax ID	R	-	0	1	1	1	0	0	1	0	0x72
R01h	Display Mode control	W/R	-	DSTB(0)	-	-	-	SCROLL(0)	IDMON(0)	INVON(0)	PTLON(0)	0x00
R02h	Column address start 2	W/R	-	SC[15:8] (8'b0000_0000)								0x00
R03h	Column address start 1	W/R	-	SC[7:0] (8'b0000_0000)								0x00
R04h	Column address end 2	W/R	-	EC[15:8] (8'b0000_0000)								0x00
R05h	Column address end 1	W/R	-	EC[7:0] (8'b1110_1111)								0xEF
R06h	Row address start 2	W/R	-	SP[15:8] (8'b0000_0000)								0x00
R07h	Row address start 1	W/R	-	SP[7:0] (8'b0000_00000)								0x00
R08h	Row address end 2	W/R	-	EP[15:8] (8'b0000_0001)								0x01
R09h	Row address end 1	W/R	-	EP[7:0] (8'b1010_1111)								0xAF
R0Ah	Partial area start row 2	W/R	-	PSL[15:8] (8'b0000_0000)								0x00
R0Bh	Partial area start row 1	W/R	-	PSL[7:0] (8'b0000_00000)								0x00
R0Ch	Partial area end row 2	W/R	-	PEL[15:8] (8'b0000_0001)								0x01
R0Dh	Partial area end row 1	W/R	-	PEL[7:0] (8'b1010_1111)								0xAF
R0Eh	Vertical Scroll Top fixed area 2	W/R	-	TFA[15:8] (8'b0000_0000)								0x00
R0Fh	Vertical Scroll Top fixed area 1	W/R	-	TFA[7:0] (8'b0000_0000)								0x00
R10h	Vertical Scroll height area 2	W/R	-	VSA[15:8] (8'b0000_0001)								0x01
R11h	Vertical Scroll height area 1	W/R	-	VSA[7:0] (8'b1011_0000)								0xB0
R12h	Vertical Scroll Button area 2	W/R	-	BFA[15:8] (8'b0000_0000)								0x00
R13h	Vertical Scroll Button area 1	W/R	-	BFA [7:0] (8'b0000_0000)								0x00
R14h	Vertical Scroll Start address 2	W/R	-	VSP [15:8] (8'b0000_0000)								0x00
R15h	Vertical Scroll Start address 1	W/R	-	VSP [7:0] (8'b0000_0000)								0X00
R16h	Memory Access control	W/R	-	MY(0)	MX(0)	MV(0)	ML(0)	BGR(0)	-	-	-	0x00
R17h	COLMOD	W/R	-	-	CSEL[2:0] (3b'110)			-	IFPF[2:0] (3b'110)			0x66
R18h	OSC Control 2	W/R	-	-	-	-	-	RADJ[2:0](4b'0100)				0x04
R19h	OSC Control 1	W/R	-	-	-	-	-	-	-	-	OSC_EN(0)	0x00
R1Ah	Power Control 1	W/R	-	-	-	-	-	-	BT[2:0] (100)			0x04
R1Bh	Power Control 2	W/R	-	VCIRE(1)	-	-	VRH[4:0] (0_1100)					0x8C
R1Ch	Power Control 3	W/R	-	-	-	-	-	-	AP[2:0] (011)			0x03
R1Fh	Power Control 5	W/R	-	GASEN(1)	VCOMG(0)	-	PON(0)	DK(1)	XDK(0)	DDVDH_TRI(0)	STB(1)	0x89
R22h	SRAM Write Control	W/R	SRAM Write									-
R23h	VCOM Control 1	W/R	-	-	-	-	-	-	-	-	SELVCM(0)	0x00
R24h	VCOM Control 2	W/R	-	-	VCM[6:0](100_0000)							0x40
R25h	VCOM Control 3	W/R	-	-	-	-	VDV[4:0](0_1111)					0x0F
R26h	Display Control 1	W/R	-	-	-	-	PTG(0)	ISC[3:0](0001)				0x01

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R27h	Display Control 2	W/R	-	-	-	-	-	-	-	-	REF(1)	0x01
R28h	Display Control 3	W/R	-	-	-	GON(1)	DTE(0)	D[1:0] (00)		-	-	0x20
R29h	Display Control 4	W/R	-	-	-	NL[5:0](6'b11_0001)						0x31
R2Ah	Display Control 5	W/R	-	-	SCN[6:0](000_0000)							0x00
R2Bh	Display Control 6	W/R	-	-	-	-	-	-	-	PTS[1:0](00)		0x00
R2Ch	Display Control 7	W/R	-	-	-	-	-	-	-	DIVE[1:0](10)		0x02
R2Dh	Cycle Control 1	W/R	-	-	SDT[2:0](000)			-	NOW[2:0](110)			0x06
R2Eh	Cycle Control 2	W/R	-			NW[5:0](00_0000)						0x00
R31h	RGB interface control 1	W/R	-	-	-	-	RM(0)	-	-	DM[1:0](00)		0x00
R32h	RGB interface control 2	W/R	-	SDA_EN(0)	-	-	VSPL (0)	HSPL (0)	-	EPL(1)	DPL(0)	0x02
R33h	RGB interface control 3	W/R	-	HBP[7:0](8'b0000_1000)								0x08
R34h	RGB interface control 4	W/R	-	HBP[9:8](2'b00)		VBP[5:0](6'b00_0100)						0x04
R36h	Panel Characteristic	W/R	-	-	-	-	REV_PANEL (0)	SM_PANEL (0)	GS_PANEL(0)l	BGR_PANEL(0)	SS_PANEL (0)	0x00
R38h	OTP Control 1	W/R	-	OTP_MASK[7:0] (8'h00)								0x00
R39h	OTP Control 2	W/R	-	OTP_INDEX[7:0] (8'h00)								0x00
R3Ah	OTP Control 3	W/R	-	-	VPP_EN (0)	OTP_POR(0)	OTP_PWE(0)	OTP_PTM[1:0] (00)		VPP_SEL (0)	OTP_PROG(0)	0x00
R3Bh	OTP Control 4	R	-	OTP_DATA[7:0]								0xFF
R3Ch	CABC Control 1	W/R	-	DBV[7:0] (8'h00)								0x00
R3Dh	CABC Control 2	W/R	-	-	-	BCTRL (0)	-	DD(0)	BL(0)	-	-	0x00
R3Eh	CABC Control 3	W/R	-	-	-	-	-	-	-	CACB[1:0] (00)		0x00
R3Fh	CABC Control 4	W/R	-	CMB[7:0] (8'h00)								0x00
R40h	Gamma Control 1	W/R	-	-	KP1[2:0](100)			-	KP0[2:0](100)			0x44
R41h	Gamma Control 2	W/R	-	-	KP3[2:0](100)			-	KP2[2:0](100)			0x44
R42h	Gamma Control 3	W/R	-	-	KP5[2:0](100)			-	KP4[2:0](100)			0x44
R43h	Gamma Control 4	W/R	-	-	RP1[2:0](100)			-	RP0[2:0](100)			0x44
R44h	Gamma Control 5	W/R	-	-	-	-	-	VRP0[3:0]				0x08
R45h	Gamma Control 6	W/R	-	-	-	-	VRP1[4:0]					0x10
R46h	Gamma Control 7	W/R	-	-	KN1[2:0](100)			-	KN0[2:0](100)			0x44
R47h	Gamma Control 8	W/R	-	-	KN3[2:0](100)			-	KN2[2:0](100)			0x44
R48h	Gamma Control 9	W/R	-	-	KN5[2:0](100)			-	KN4[2:0](100)			0x44
R49h	Gamma Control 10	W/R	-	-	RN1[2:0](100)			-	RN0[2:0](100)			0x44
R4Ah	Gamma Control 11	W/R	-	-	-	-	-	0x08				0x08
R4Bh	Gamma Control 12	W/R	-	-	-	-	VRN1[3:0]					0x10
R4Ch	Gamma Control 13	W/R	-	VREP1[3:0]				VREP0[3:0]				0x88
R4Dh	Gamma Control 14	W/R	-	VREN0[3:0]				VREP2[3:0]				0x88
R4Eh	Gamma Control 15	W/R	-	VREN2[3:0]				VREN1[3:0]				0x88
R60h	TE Control	W/R	-	-	-		TE_MODE(0)	TEON (0)		-	-	0x00
R61h	ID1	W/R	-	ID1[7:0](8'h00)								0x00
R62h	ID2	W/R	-	ID2[7:0](8'h00)								0x00
R63h	ID3	W/R	-	ID3[7:0](8'h00)								0x00
R68h	Memory Write Control	W/R	-	-	-	-	-	-	-	WEMODE (1)	-	0x02
R69h	TE Interval Control	W/R	-	-	-	-	-	-	TEI[2:0](000)			0x00
R6Ah	RGB SRAM Cycle	W/R	-	-	-	-	-	-	DENC[2:0](000)			0x00
R6Bh	Data Format Control	W/R	-	-	-	EPF[1:0](10)		-	-	-	DFM(0)	0x20
R70h	Frame Rate Control 1	W/R	-	-	-	-	BC0(1)	-	-	DIV0[1:0](00)		0x10
R71h	Frame Rate Control 2	W/R	-	-	-	-	RTN0[4:0](1_0000)					0x1A
R72h	Frame Rate Control 3	W/R	-	BP0[7:0](8'h02)								0x02
R73h	Frame Rate Control 4	W/R	-	FP0[7:0](8'h02)								0x02
R74h	Frame Rate Control 5	W/R	-	-	-	-	BC2(0)	-	-	DIV2[1:0](00)		0x00
R75h	Frame Rate Control 6	W/R	-	-	-	-	RTN2[4:0](1_0000)					0x1A

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R76h	Frame Rate Control 7	W/R	-	BP2[7:0](8'h02)								0x02
R77h	Frame Rate Control 8	W/R	-	FP2[7:0](8'h02)								0x02
R7Ah	Power Control 6	W/R	-	-	-	-	-	-	SAP0[2:0](001)			0x01
R7Bh	Power Control 7	W/R	-	-	DC10[2:0](100)			-	DC00[2:0](100)			0x44
R7Ch	Power Control 8	W/R	-	-	-	-	-	-	SAP1[2:0](001)			0x01
R7Dh	Power Control 9	W/R	-	-	DC11[2:0](100)			-	DC01[2:0](100)			0x44
R7Eh	Power Control 10	W/R	-	-	-	-	-	-	SAP2[2:0](001)			0x01
R7Fh	Power Control 11	W/R	-	-	DC12[2:0](100)			-	DC02[2:0](100)			0x44
R84h	TE Output Line 2	W/R	-	TSEL[15:8](8'h00)								0x00
R85h	TE Output Line 1	W/R	-	TSEL[7:0](8'h00)								0x00
R86h	VPP Control	W/R	-	-	-	-	-	-	VPP[2:0](011)			0x03
R87h	OTP Control 5	W/R	-	OTP_KEY[7:0](8'h55)								0x55
R88h	Get Scan Line 2	R	-	SL[15:8](8'hFF)								0xFF
R89h	Get Scan Line 1	R	-	SL[7:0](8'hFF)								0xFF
R8Ah	Read VCOM OTP Times	R	-	-	-	-	-	VCOM_OTP_TIMES[3:0]				0x00
R8Bh	Read ID OTP Times	R	-	-	-	-	-	ID_OTP_TIMES[3:0]				0x00
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0] (00)		0x00

Table 6.1: List table of command set page 0

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R00h	DGC Control	W/R	-	-	-	-	-	-	-	-	DGC_EN(0)	0x00
R01h	DGC LUT1	W	-	DGC_LUT_R00(8'h00)								0x00
R02h	DGC LUT2	W	-	DGC_LUT_R01(8'h08)								0x08
R03h	DGC LUT3	W	-	DGC_LUT_R02(8'h10)								0x10
R04h	DGC LUT4	W	-	DGC_LUT_R03(8'h18)								0x18
R05h	DGC LUT5	W	-	DGC_LUT_R04(8'h20)								0x20
R06h	DGC LUT6	W	-	DGC_LUT_R05(8'h28)								0x28
R07h	DGC LUT7	W	-	DGC_LUT_R06(8'h30)								0x30
R08h	DGC LUT8	W	-	DGC_LUT_R07(8'h38)								0x38
R09h	DGC LUT9	W	-	DGC_LUT_R08(8'h40)								0x40
R0Ah	DGC LUT10	W	-	DGC_LUT_R09(8'h48)								0x48
R0Bh	DGC LUT11	W	-	DGC_LUT_R10(8'h50)								0x50
R0Ch	DGC LUT12	W	-	DGC_LUT_R11(8'h58)								0x58
R0Dh	DGC LUT13	W	-	DGC_LUT_R12(8'h60)								0x60
R0Eh	DGC LUT14	W	-	DGC_LUT_R13(8'h68)								0x68
R0Fh	DGC LUT15	W	-	DGC_LUT_R14(8'h70)								0x70
R10h	DGC LUT16	W	-	DGC_LUT_R15(8'h78)								0x78
R11h	DGC LUT17	W	-	DGC_LUT_R16(8'h80)								0x80
R12h	DGC LUT18	W	-	DGC_LUT_R17(8'h88)								0x88
R13h	DGC LUT19	W	-	DGC_LUT_R18(8'h90)								0x90
R14h	DGC LUT20	W	-	DGC_LUT_R19(8'h98)								0x98
R15h	DGC LUT21	W	-	DGC_LUT_R20(8'hA0)								0xA0
R16h	DGC LUT22	W	-	DGC_LUT_R21(8'hA8)								0xA8
R17h	DGC LUT23	W	-	DGC_LUT_R22(8'hB0)								0xB0
R18h	DGC LUT24	W	-	DGC_LUT_R23(8'hB8)								0xB8
R19h	DGC LUT25	W	-	DGC_LUT_R24(8'hC0)								0xC0
R1Ah	DGC LUT26	W	-	DGC_LUT_R25(8'hC8)								0xC8
R1Bh	DGC LUT27	W	-	DGC_LUT_R26(8'hD0)								0xD0
R1Ch	DGC LUT28	W	-	DGC_LUT_R27(8'hD8)								0xD8
R1Dh	DGC LUT29	W	-	DGC_LUT_R28(8'hE0)								0xE0
R1Eh	DGC LUT30	W	-	DGC_LUT_R29(8'hE8)								0xE8
R1Fh	DGC LUT31	W	-	DGC_LUT_R30(8'hF0)								0xF0
R20h	DGC LUT32	W	-	DGC_LUT_R31(8'hF8)								0xF8
R21h	DGC LUT33	W	-	DGC_LUT_R32(8'hFC)								0xFC
R22h	DGC LUT34	W	-	DGC_LUT_G00(8'h00)								0x00
R23h	DGC LUT35	W	-	DGC_LUT_G01(8'h08)								0x08
R24h	DGC LUT36	W	-	DGC_LUT_G02(8'h10)								0x10
R25h	DGC LUT37	W	-	DGC_LUT_G03(8'h18)								0x18
R26h	DGC LUT38	W	-	DGC_LUT_G04(8'h20)								0x20
R27h	DGC LUT39	W	-	DGC_LUT_G05(8'h28)								0x28
R28h	DGC LUT40	W	-	DGC_LUT_G06(8'h30)								0x30
R29h	DGC LUT41	W	-	DGC_LUT_G07(8'h38)								0x38
R2Ah	DGC LUT42	W	-	DGC_LUT_G08(8'h40)								0x40
R2Bh	DGC LUT43	W	-	DGC_LUT_G09(8'h48)								0x48
R2Ch	DGC LUT44	W	-	DGC_LUT_G10(8'h50)								0x50
R2Dh	DGC LUT45	W	-	DGC_LUT_G11(8'h58)								0x58
R2Eh	DGC LUT46	W	-	DGC_LUT_G12(8'h60)								0x60
R2Fh	DGC LUT47	W	-	DGC_LUT_G13(8'h68)								0x68
R30h	DGC LUT48	W	-	DGC_LUT_G14(8'h70)								0x70
R31h	DGC LUT49	W	-	DGC_LUT_G15(8'h78)								0x78
R32h	DGC LUT50	W	-	DGC_LUT_G16(8'h80)								0x80
R33h	DGC LUT51	W	-	DGC_LUT_G17(8'h88)								0x88
R34h	DGC LUT52	W	-	DGC_LUT_G18(8'h90)								0x90
R35h	DGC LUT53	W	-	DGC_LUT_G19(8'h98)								0x98
R36h	DGC LUT54	W	-	DGC_LUT_G20(8'hA0)								0xA0
R37h	DGC LUT55	W	-	DGC_LUT_G21(8'hA8)								0xA8
R38h	DGC LUT56	W	-	DGC_LUT_G22(8'hB0)								0xB0
R39h	DGC LUT57	W	-	DGC_LUT_G23(8'hB8)								0xB8
R3Ah	DGC LUT58	W	-	DGC_LUT_G24(8'hC0)								0xC0
R3Bh	DGC LUT59	W	-	DGC_LUT_G25(8'hC8)								0xC8
R3Ch	DGC LUT60	W	-	DGC_LUT_G26(8'hD0)								0xD0
R3Dh	DGC LUT61	W	-	DGC_LUT_G27(8'hD8)								0xD8
R3Eh	DGC LUT62	W	-	DGC_LUT_G28(8'hE0)								0xE0
R3Fh	DGC LUT63	W	-	DGC_LUT_G29(8'hE8)								0xE8
R40h	DGC LUT64	W	-	DGC_LUT_G30(8'hF0)								0xF0
R41h	DGC LUT65	W	-	DGC_LUT_G31(8'hF8)								0xF8
R42h	DGC LUT66	W	-	DGC_LUT_G32(8'hFC)								0xFC

Register No.	Register	W/R	Upper Code	Lower Code								Default Value
			D[17:8]	D7	D6	D5	D4	D3	D2	D1	D0	
R43h	DGC LUT67	W	-	DGC_LUT_B00(8'h00)								0x00
R44h	DGC LUT68	W	-	DGC_LUT_B01(8'h08)								0x08
R45h	DGC LUT69	W	-	DGC_LUT_B02(8'h10)								0x10
R46h	DGC LUT70	W	-	DGC_LUT_B03(8'h18)								0x18
R47h	DGC LUT71	W	-	DGC_LUT_B04(8'h20)								0x20
R48h	DGC LUT72	W	-	DGC_LUT_B05(8'h28)								0x28
R49h	DGC LUT73	W	-	DGC_LUT_B06(8'h30)								0x30
R4Ah	DGC LUT74	W	-	DGC_LUT_B07(8'h38)								0x38
R4Bh	DGC LUT75	W	-	DGC_LUT_B08(8'h40)								0x40
R4Ch	DGC LUT76	W	-	DGC_LUT_B09(8'h48)								0x48
R4Dh	DGC LUT77	W	-	DGC_LUT_B10(8'h50)								0x50
R4Eh	DGC LUT78	W	-	DGC_LUT_B11(8'h58)								0x58
R4Fh	DGC LUT79	W	-	DGC_LUT_B12(8'h60)								0x60
R50h	DGC LUT80	W	-	DGC_LUT_B13(8'h68)								0x68
R51h	DGC LUT81	W	-	DGC_LUT_B14(8'h70)								0x70
R52h	DGC LUT82	W	-	DGC_LUT_B15(8'h78)								0x78
R53h	DGC LUT83	W	-	DGC_LUT_B16(8'h80)								0x80
R54h	DGC LUT84	W	-	DGC_LUT_B17(8'h88)								0x88
R55h	DGC LUT85	W	-	DGC_LUT_B18(8'h90)								0x90
R56h	DGC LUT86	W	-	DGC_LUT_B19(8'h98)								0x98
R57h	DGC LUT87	W	-	DGC_LUT_B20(8'hA0)								0xA0
R58h	DGC LUT88	W	-	DGC_LUT_B21(8'hA8)								0xA8
R59h	DGC LUT89	W	-	DGC_LUT_B22(8'hB0)								0xB0
R5Ah	DGC LUT90	W	-	DGC_LUT_B23(8'hB8)								0xB8
R5Bh	DGC LUT91	W	-	DGC_LUT_B24(8'hC0)								0xC0
R5Ch	DGC LUT92	W	-	DGC_LUT_B25(8'hC8)								0xC8
R5Dh	DGC LUT93	W	-	DGC_LUT_B26(8'hD0)								0xD0
R5Eh	DGC LUT94	W	-	DGC_LUT_B27(8'hD8)								0xD8
R5Fh	DGC LUT95	W	-	DGC_LUT_B28(8'hE0)								0xE0
R60h	DGC LUT96	W	-	DGC_LUT_B29(8'hE8)								0xE8
R61h	DGC LUT97	W	-	DGC_LUT_B30(8'hF0)								0xF0
R62h	DGC LUT98	W	-	DGC_LUT_B31(8'hF8)								0xF8
R63h	DGC LUT99	W	-	DGC_LUT_B32(8'hFC)								0xFC
RC3h	CABC Control 5	W/R	-	LEDONPOL (0)	PWMDIV[2:0](000)			SEL_GAIN[1:0] (11)		INVPLUS(1)	SEL_BLDUTY (1)	0x0F
RC5h	CABC Control 7	W/R	-	PWM_PERIOD[7:0](8'h23)								0x23
RFFh	Page select	W/R	-	-	-	-	-	-	-	PAGE_SEL[1:0](00)		0x00

Table 6.2: List table of command set page 1

6.2 Index register

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 6.1 Index register

Index register (IR) specifies the Index of register from R00h to RFFh. It sets the register number (ID7-0) in the range from 00000000b to 11111111b in binary form.

6.3 Himax ID register (PAGE0 -R00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	1	1	1	0	0	1	0

Figure 6.2 Himax ID register (PAGE0 -00h)

This command is used to read this IC's ID code. The ID code of this IC is 72h.

6.4 Display mode control register (PAGE0 -01h)

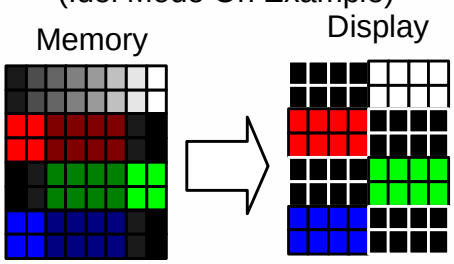
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	DSTB	*	*	*	SCROLL	IDMON	INVON	PLTON
R	1	DSTB	*	*	*	SCROLL	IDMON	INVON	PLTON

Figure 6.3 Display mode control register (PAGE0 -01h)

DSTB: This bits can let the driver into the deep standby mode. And when into deep standby(**DSTB**='1), all display operation stops, including the internal R-C oscillator. In the deep standby mode, the GRAM data and register content are not retained.

IDMON: This bit is Idle mode (8-color display mode) enable bit. **IDMON** = '1', chip will be into idle mode, and color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.

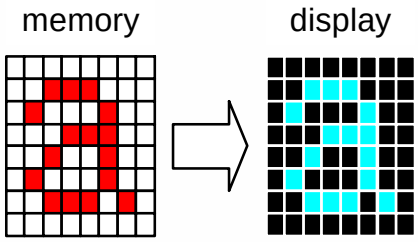
(Idel Mode On Example)



SCROLL : This bit turns on scroll mode by setting SCROLL = '1'. The scroll mode window is described by the Vertical Scroll Area command **TFA[15:0], VSA[15:0], BFA[15:0]** and the Vertical start address **VSP[15:0]** (R0Eh~R15h). To leave scroll mode to normal mode, the **SCROLL** bit should be set to '0'.

INVON: This bit is display inversion mode enable bit. **INVON** = '1', chip will be into display inversion mode, and makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.

(Example)



PTLON: This command is used for turning on/off Partial mode by setting PTLON=1/0. The partial mode window is described by the Partial Area command **PSL[15:0], PEL[15:0]** bits(R0Ah~R0Dh). To leave Partial mode to normal mode, the **PLTON** bit should be set to '0'.

6.5 Column address start register (PAGE0 -02~03h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8
R	1	SC 15	SC 14	SC 13	SC 12	SC 11	SC 10	SC9	SC8

Figure 6.4 Column address start register upper byte (PAGE0 -02h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
R	1	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Figure 6.5 Column address start register low byte (PAGE0 -03h)

6.6 Column address end register (PAGE0 -04~05h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8
R	1	EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC9	EC8

Figure 6.6 Column address end register upper byte (PAGE0 -04h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
R	1	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

Figure 6.7 Column address end register low byte (PAGE0 -05h)

6.7 Row address start register (PAGE0 -06~07h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8
R	1	SP 15	SP 14	SP 13	SP 12	SP 11	SP 10	SP9	SP8

Figure 6.8 Row address start register upper byte (PAGE0 -06h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
R	1	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Figure 6.9 Row address start register low byte (PAGE0 -07h)

6.8 Row address end register (PAGE0 -08~09h)

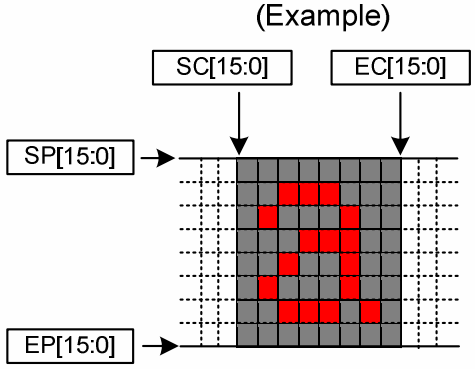
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8
R	1	EP 15	EP 14	EP 13	EP 12	EP 11	EP 10	EP9	EP8

Figure 6.10 Row address end register upper byte (PAGE0 -08h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0
R	1	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0

Figure 6.11 Row address end register low byte (PAGE0 -09h)

These commands (R02h~R09h) are used to define area of frame memory where MCU can access. The values of SC[15:0], EC[15:0], SP[15:0] and EP[15:0] are referred when RAMWR command comes. Each value of SC[15:0], EC[15:0] represents one column line in the Frame Memory. Each value of SP[15:0], EP[15:0] represents one page line in the Frame Memory.



6.9 Partial Area Start Row Register (PAGE0 -0A~0Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8
R	1	PSL 15	PSL 14	PSL 13	PSL 12	PSL 11	PSL 10	PSL 9	PSL 8

Figure 6.12 Partial area start row register upper byte (PAGE0 -0Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0
R	1	PSL 7	PSL 6	PSL 5	PSL 4	PSL 3	PSL 2	PSL 1	PSL 0

Figure 6.13 Partial area start row register low byte (PAGE0 -0Bh)

6.10 Partial Area End Row Register (PAGE0 -0C~0Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8
R	1	PEL 15	PEL 14	PEL 13	PEL 12	PEL 11	PEL 10	PEL 9	PEL 8

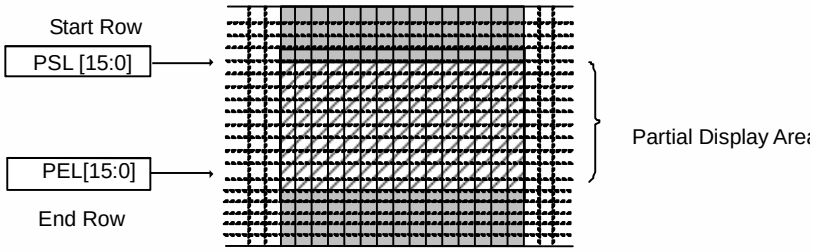
Figure 6.14 Partial area end row register upper byte (PAGE0 -0Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0
R	1	PEL 7	PEL 6	PEL 5	PEL 4	PEL 3	PEL 2	PEL 1	PEL 0

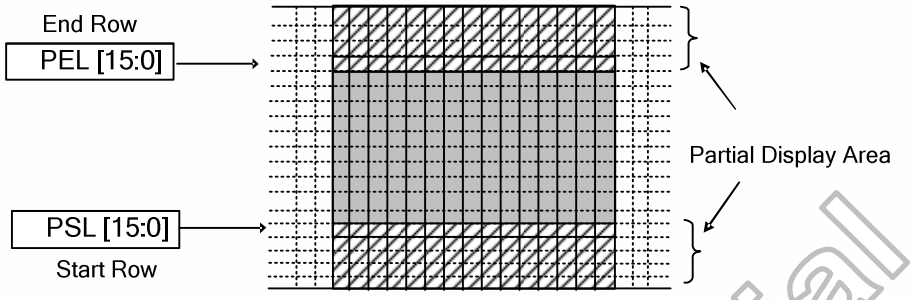
Figure 6.15 Partial area end row register low byte (PAGE0 -0Dh)

These commands (PAGE0 -0Ah~~0Dh) define the partial mode's display area. The Start Row (PSL) and the second the End Row (PEL) are illustrated in the figures below. PSL and PEL refer to the Frame Memory Line Pointer.

If End Row > Start Row



If End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

6.11 Vertical scroll top fixed area register (PAGE0 -0E~0Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8
R	1	TFA 15	TFA 14	TFA 13	TFA 12	TFA 11	TFA 10	TFA 9	TFA 8

Figure 6.16 Vertical scroll top fixed area register upper byte (PAGE0 -0Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0
R	1	TFA 7	TFA 6	TFA 5	TFA 4	TFA 3	TFA 2	TFA 1	TFA 0

Figure 6.17 Vertical scroll top fixed area register low byte (PAGE0 -0Fh)

6.12 Vertical scroll height area register (PAGE0 -10~11h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8
R	1	VSA 15	VSA 14	VSA 13	VSA 12	VSA 11	VSA 10	VSA 9	VSA 8

Figure 6.18 Vertical scroll height area register upper byte (PAGE0 -10h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
R	1	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

Figure 6.19 Vertical scroll height area register low byte (PAGE0 -11h)

6.13 Vertical scroll button fixed area register (PAGE0 -12~13h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8
R	1	BFA 15	BFA 14	BFA 13	BFA 12	BFA 11	BFA 10	BFA 9	BFA 8

Figure 6.20 Vertical scroll button fixed area register upper byte (PAGE0 -12h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0
R	1	BFA 7	BFA 6	BFA 5	BFA 4	BFA 3	BFA 2	BFA 1	BFA 0

Figure 6.21 Vertical scroll button fixed area register low byte (PAGE0 -13h)

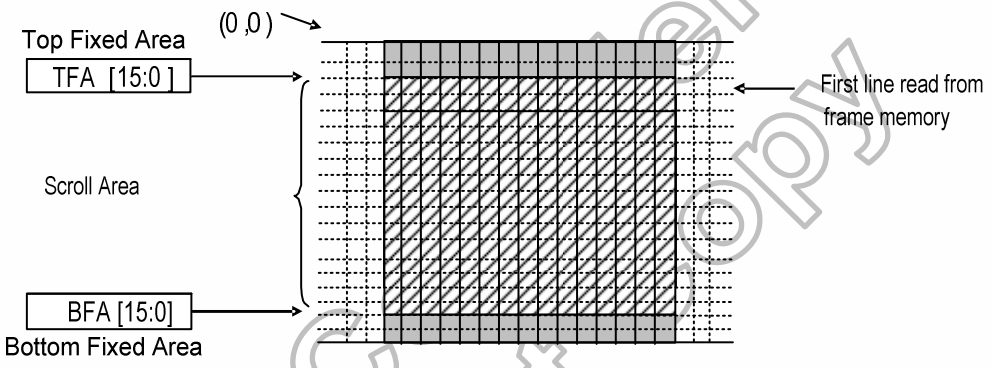
These commands (PAGE0 -0E~0Fh, R10~11h, R12~13h) define the Vertical Scrolling Area of the display.

TFA[15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

VSA[15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

BFA[15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Please note that (TFA+VSA+BFA) must be set to '432d', otherwise Scrolling mode is undefined. In Vertical Scroll Mode, **MV** bit should be set to '0' – this only affects the Frame Memory Write.

6.14 Vertical scroll start address register (PAGE0 -14~15h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8
R	1	VSP 15	VSP 14	VSP 13	VSP 12	VSP 11	VSP 10	VSP 9	VSP 8

Figure 6.22 Vertical Scroll Start Address Register Upper Byte (PAGE0 -14h)

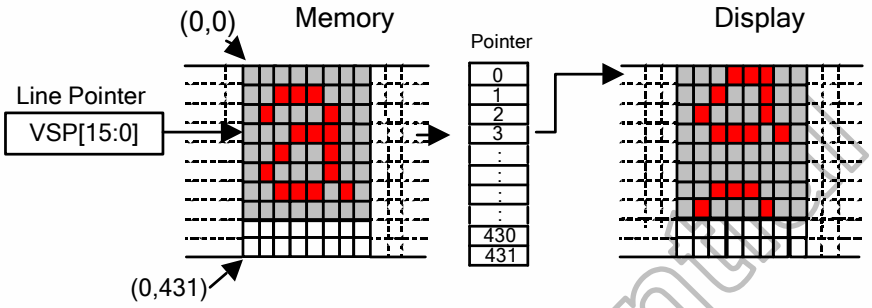
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0
R	1	VSP 7	VSP 6	VSP 5	VSP 4	VSP 3	VSP 2	VSP 1	VSP 0

Figure 6.23 Vertical Scroll Start Address Register Low Byte (PAGE0 -15h)

VSP[15:0] is used together with Vertical Scrolling Definition register (PAGE0 -0Eh~R13h), which describe the scrolling area and the scrolling mode.
VSP[15:0] refers to the Frame Memory line Pointer, and describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:

Example:
When Top Fixed Area TFA = ‘00d’, Bottom Fixed Area BFA = ‘02’d, Vertical Scrolling Area VSA = ‘430'd’ and VSP = ‘3d’ (**SS**=’0’, **GS**=’0’)

(Example)



When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect.

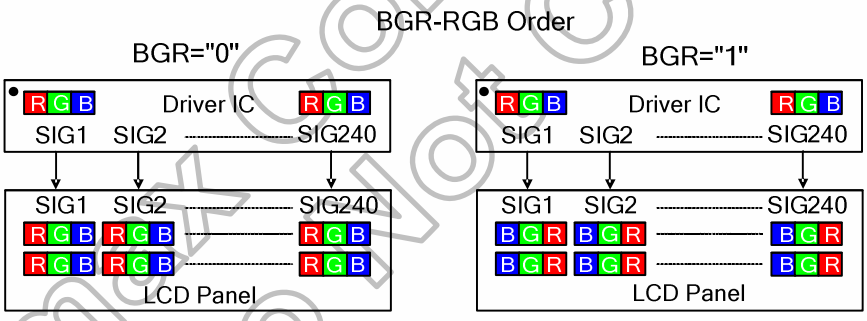
6.15 Memory access control register (PAGE0 -16h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	MY	MX	MV	ML	BGR	*	*	*
R	1	MY	MX	MV	ML	BGR	0	0	0

Figure 6.24 Memory access control register (PAGE0 -16h)

This command defines read/write scanning direction of frame memory. **MX, MY** bits also define the display direction in the RGB interface. This command makes no change on the other driver status.

Bit	Name	Description
MY	PAGE ADDRESS ORDER	These 3 bits controls MCU to memory write direction.
MX	COLUMN ADDRESS ORDER	
MV	PAGE/COLUMN SELECTION	
ML	Vertical ORDER	LCD vertical refresh direction control
BGR	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)



6.16 COLMOD control register (PAGE0 -17h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	CSEL2	CSEL1	CSEL0	*	IFPF2	IFPF1	IFPF0
R	1	*	CSEL2	CSEL1	CSEL0	*	IFPF2	IFPF1	IFPF0

Figure 6.25 COLMOD control register (PAGE0 -17h)

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

System interface

Interface Format	IFPF2	IFPF1	IFPF0
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	1	1	1

RGB interface

Interface Format	CSEL2	CSEL1	CSEL0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
Not Defined	The Other Setting		

6.17 OSC control register (PAGE0 -18h & R19h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	RADJ 3	RADJ 2	RADJ 1	RADJ 0
R	1	*	*	*	*	RADJ 3	RADJ 2	RADJ 1	RADJ 0

Figure 6.26 OSC control 1 register (PAGE0 -18h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	OSC_ EN
R	1	0	0	0	0	0	0	0	OSC_ EN

Figure 6.27 OSC control 2 register (PAGE0 -19h)

These commands are used to set internal oscillator related setting

OSC_EN: Enable internal oscillator, OSC_EN = '1', internal oscillator start to oscillate. OSC_EN = '0', internal oscillator stop. In RGB interface mode (DM[1:0] = '01' or '1x'), internal oscillator will be stop to oscillate and OSC_EN bit control is invalid.

RADJ[3:0]: Internal oscillator frequency adjusts.

RADJ3	RADJ2	RADJ1	RADJ0	Internal Oscillator Frequency	Display Frame rate
0	0	0	0	160% x 3.69MHz	96Hz
0	0	0	1	147% x 3.69MHz	88Hz
0	0	1	0	137% x 3.69MHz	82Hz
0	0	1	1	127% x 3.69MHz	76Hz
0	1	0	0	120% x 3.69MHz	72Hz
0	1	0	1	113% x 3.69MHz	68Hz
0	1	1	0	107% x 3.69MHz	64Hz
0	1	1	1	100% x 3.69MHz	60Hz
1	0	0	0	167% x 3.69MHz	100Hz
1	0	0	1	175% x 3.69MHz	105Hz
1	0	1	0	183% x 3.69MHz	110Hz
1	0	1	1	192% x 3.69MHz	115Hz
1	1	0	0	200% x 3.69MHz	120Hz
Other setting				Setting Inhibited	

6.18 Power control 1 register (PAGE0 -1Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	BT2	BT1	BT0
R	1	*	*	*	*	*	BT2	BT0	BT0

Figure 6.28 Power control 1 register (PAGE0 -1Ah)

BT[2:0]: Switch the output factor of step-up circuit 2 for VGH and VGL voltage generation. The LCD drive voltage level can be selected according to the characteristic of liquid crystal which panel used. Lower amplification of the step-up circuit consumes less current and then the power consumption can be reduced.

BT2	BT1	BT0	DDVDH	VCL	VGH	VGL
0	0	0	5.0V	-VCI	3DDVDH	-VCI-2DDVDH
0	0	1	5.0V	-VCI	3DDVDH	-2DDVDH
0	1	0	5.0V	-VCI	3DDVDH	VCI-2DDVDH
0	1	1	5.0V	-VCI	VCI + 2DDVDH	-VCI-2DDVDH
1	0	0	5.0V	-VCI	VCI + 2DDVDH	-2DDVDH
1	0	1	5.0V	-VCI	VCI + 2DDVDH	VCI-2DDVDH
1	1	0	5.0V	-VCI	2DDVDH	-2DDVDH
1	1	1	5.0V	-VCI	2DDVDH	-VCI-DDVDH

6.19 Power control 2 register (PAGE0 -1Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VCIRE	*	*	VRH4	VRH3	VRH2	VRH1	VRH0
R	1	VCIRE	*	*	VRH4	VRH3	VRH2	VRH1	VRH0

Figure 6.29 Power control 2 register (PAGE0 -1Bh)

VCIRE: Select VREG1 reference voltage come from external voltage or internal generated voltage.
'0': External reference voltage VCI.
'1': Internal reference voltage 2.5V

VRH[4:0]: Specify the VREG1 voltage adjusting. (VREG1 must lower than DDVDH - 0.3V).

VRH[4:0]	VREG1 Voltage (VCIRE=0)	VRH[4:0]	VREG1 Voltage (VCIRE=1)
5'h00	VCI x 1.600	5'h00	2.5 x 1.600
5'h01	VCI x 1.625	5'h01	2.5 x 1.625
5'h02	VCI x 1.650	5'h02	2.5 x 1.650
5'h03	VCI x 1.675	5'h03	2.5 x 1.675
:	:	:	:
5'h0E	VCI x 1.950	5'h0E	2.5 x 1.950
5'h0F	VCI x 1.975	5'h0F	2.5 x 1.975
5'h10	Setting inhabited	5'h10	2.5 x 2.000
5'h11	Setting inhabited	5'h11	2.5 x 2.025
5'h12	Setting inhabited	5'h12	2.5 x 2.050
5'h13	Setting inhabited	5'h13	2.5 x 2.075
5'h14	Setting inhabited	5'h14	2.5 x 2.100
5'h15	Setting inhabited	5'h15	2.5 x 2.125
5'h16	Setting inhabited	5'h16	2.5 x 2.150
5'h17	Setting inhabited	5'h17	2.5 x 2.175
5'h18	Setting inhabited	5'h18	2.5 x 2.200
Others	Setting inhabited	Others	Setting inhabited

6.20 Power control 3 register (PAGE0 -1Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	AP2	AP1	AP0
R	1	*	*	*	*	*	AP2	AP1	AP0

Figure 6.30 Power control 3 register (PAGE0 -1Ch)

AP[2:0]: Adjust the amount of current driving for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Operation of the operational amplifier stops
0	0	1	Small
0	1	0	Small
0	1	1	Small
1	0	0	Medium
1	0	1	Medium High
1	1	0	Large
1	1	1	Small

6.21 Power control 5 register (PAGE0 -1Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB
R	1	GASEN	VCOMG	*	PON	DK	XDK	DDVDH_TRI	STB

Figure 6.31 Power control 5 register (PAGE0 -1Fh)

PON: Specify on/off control of step-up circuit 2 for VGH, VGL voltage generation. For detail, see the Power On/Off Setting Flow.

PON	Operation of step-up circuit 2
0	OFF
1	ON

DK: Specify on/off control of step-up circuit 1 for DDVDH voltage generation. For detail, see the Power Supply Setting Sequence.

DK	Operation of step-up circuit 1
0	ON
1	OFF

STB: When **STB** = '1', the HX8352-C01 into the standby mode, where all display operation stops, suspend all the internal operations including the internal R-C oscillator. During the standby mode, only the following process can be executed. For details, please refer to STB mode flow.

a. Start the oscillation
b. Exit the Standby mode (STB = "0") ,

In the standby mode, the GRAM data and register content are retained.

XDK, DDVDH_TRI: Specify the ratio of step-up circuit for DDVDH voltage generation.

DDVDH_TRI	XDK	Step up circuit 1	Capacitor connection pins used
0	0	2 x VCI	C11P, C11N
0	1	2 x VCI	C11P, C11N, C12P, C12N
1	0	3 x VCI	C11P, C11N, C12P, C12N
1	1	Setting inhabited	Setting inhabited

VCOMG: Specify on/off control of step-up circuit 3 for VCL voltage generation. For detail, see the Power Supply Setting Sequence. When VCOMG = '0', VCOML = GND.

VCOMG	Operation of step-up circuit 3
0	OFF
1	ON

GASEN: This stands for abnormal power-off monitor function when the power is off.

6.22 Read data register (PAGE0 -22h)

R/W	RS	RB17	RB16	RB15	RB14	RB13	RB12	RB11	RB10	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
R	1	RD 17	RD 16	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 6.32 Read data register (PAGE0 -22h)

WD[17:0] : Transforms the data into 18-bit bus before written to GRAM through the write data register (WDR). After a write operation is issued, the address is automatically updated according to the AM and I/D bits.

RD[17:0]: Read 18-bit data from GRAM through the read data register (RDR). When the data is read by microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (D17–0) becomes invalid and the second-word read is normal.

6.23 VCOM control 1~3 register (PAGE0 -23~25h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	SEL VCM
R	1	*	*	*	*	*	*	*	SEL VCM

Figure 6.33 VCOM control 1 register (PAGE0 -23h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	VCM 6	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0
R	1	*	VCM 6	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0

Figure 6.34 VCOM control 2 register (PAGE0 -24h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0
R	1	*	*	*	VDV 4	VDV 3	VDV 2	VDV 1	VDV 0

Figure 6.35 VCOM control 3 register (PAGE0 -25h)

This command is used to set VCOM Voltage include VCOM Low and VCOM High Voltage

SELVCM: Select the VCM setting. When OTP is programmed, the SELVCM will be set as “1” automatically.

‘0’: Register R24h&R25h setting selected for VCOM voltage.
‘1’: OTP value selected for VCOM voltage.

VCM[6:0]: Set VCOMH voltage.

VCM[6:0]	VCOMH Voltage
7’h00	VREG1 x 0.492
7’h01	VREG1 x 0.496
7’h02	VREG1 x 0.500
7’h02	VREG1 x 0.504
:	:
7’h7C	VREG1 x 0.988
7’h7D	VREG1 x 0.992
7’h7E	VREG1 x 0.996
7’h7F	VREG1 x 1.00

VDV[4:0]: Set VCOM amplitude.

VDV[4:0]	VCOM Amplitude
5’h00	VREG1 x 070
5’h01	VREG1 x 0.72
5’h02	VREG1 x 0.74
5’h02	VREG1 x 0.76
:	:

5'h1C	VREG1 x 1.26
5'h1D	VREG1 x 1.28
5'h1E	VREG1 x 1.30
5'h1F	VREG1 x 1.32

6.24 Display control 1~7 register (PAGE0 -26h~2Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	PTG	ISC3	ISC2	ISC1	ISC0
R	1	*	*	*	PTG	ISC3	ISC2	ISC1	ISC0

Figure 6.36 Display control 1 register (PAGE0 -26h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	PTV 1	PTV 0	*	*	*	REF
R	1	*	*	PTV 1	PTV 0	*	*	*	REF

Figure 6.37 Display control 2 register (PAGE0 -27h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	GON	DTE	D1	D0	*	*
R	1	*	*	GON	DTE	D1	D0	*	*

Figure 6.38 Display control 3 register (PAGE0 -28h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	NL5	NL4	NL3	NL2	NL1	NL0
R	1	*	*	NL5	NL4	NL3	NL2	NL1	NL0

Figure 6.39 Display control 4 register (PAGE0 -29h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	SCN 6	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0
R	1	*	SCN 6	SCN 5	SCN 4	SCN 3	SCN 2	SCN 1	SCN 0

Figure 6.40 Display control 5 register (PAGE0 -2Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	PTS 1	PTS 0
R	1	*	*	*	*	*	*	PTS 1	PTS 0

Figure 6.41 Display control 6 register (PAGE0 -2Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	DIVE 1	DIVE 0
R	1	*	*	*	*	*	*	DIVE 1	DIVE 0

Figure 6.42 Display control 7 register (PAGE0 -2Ch)

PTG: Set the scan mode in non-display area. Select frame inversion when interval scan selected.

PTG	Scan Mode in Non-display Area
0	Normal Scan
1	Interval Scan

ISC[3:0]: Specify the scan cycle of gate driver when REF = '1' in non-display area. Then scan cycle is odd number from 3 to 31 frame.The polarity is inverted every scan cycle.

ISC3	ISC2	ISC1	ISC0	Scan Cycle	f_{FLM} = 60Hz
0	0	0	0	Setting inhibited	
0	0	0	1	3 frames	50ms
0	0	1	0	5 frames	83ms
0	0	1	1	7 frames	117ms
0	1	0	0	9 frames	150ms
0	1	0	1	11 frames	183ms
0	1	1	0	13 frames	217ms
0	1	1	1	15 frames	250ms
1	0	0	0	17 frames	283ms
1	0	0	1	19 frames	317ms
1	0	1	0	21 frames	350ms
1	0	1	1	23 frames	383ms
1	1	0	0	25 frames	417ms
1	1	0	1	27 frames	450ms
1	1	1	0	29 frames	483ms
1	1	1	1	31 frames	517ms

REF: Refresh display in non-display area in Partial mode enable bit.
REF = '0': Refresh display operation is disabling.
REF = '1': Refresh display operation is enable.

GON, DTE: Control gate output level.

GON	DTE	Gate Output
0	0	Fixed to VGH
0	1	Fixed to VGH
1	0	Fixed to VGL
1	1	Normal Operation (VGH/VGL)

D[1:0]: When D1 = '1', display is on; when D1 = '0', display is off. When display is off, the display data is retained in the GRAM and the entire source outputs are set to the VSSD level. When D[1:0]= '01', the internal display of the HX8352-C01 is performed although the actual display is off. When D[1:0]= '00', the internal display operation halts and the display is off.

D1	D0	Source Output	Internal Display Operations	Gate-Driver Control Signals
0	0	VSSD	Halt	Halt
0	1	VSSD	Operate	Operate
1	0	=PTS(0,0)	Operate	Operate
1	1	Display	Operate	Operate

NL[5:0]: Set the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal

panel.

NL5	NL4	NL3	NL2	NL1	NL0	LCD Drive Lines
0	0	0	0	0	0	8 lines
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
:	:	:	:	:	:	:
1	1	0	1	0	0	424 lines
1	1	0	1	0	1	432 lines
Other Setting						432 lines

SCN[6:0]: Specifies the gate line where the gate driver starts scan.

SCN[6:0]	Scanning Start Position			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
00h~35h	G(1+SCN[6:0]*4)	G((NL[5:0]+1)*8)	G(1+SCN[6:0]*8)	G((NL[5:0]+1)*8)
36h~6Bh	G(1+SCN[6:0]*4)	G((NL[5:0]+1)*8)	G(2+(SCN[6:0]-36h) *8)	G((NL[5:0]+1)*8)
Others	Setting inhibited	Setting inhibited	Setting inhibited	Setting inhibited

Note: When GS=1, SCN must be setted to 00h.

PTS[1:0]: Specify the Non-display area source output in partial display mode.

PTS[1:0]		Source/VCOM Outputs in Non-display Area	
		(REV=0)	(REV=1)
00	Refresh cycle	White	Black
	Non-refresh cycle	Source=GND VCOM=GND	Source=GND VCOM=GND
01	Refresh cycle	Black	White
	Non-refresh cycle	Source=V0 VCOM=VCOML	Source=V0 VCOM=VCOML
10	Refresh cycle	White	Black
	Non-refresh cycle	Source=V63 VCOM=VCOML	Source=V63 VCOM=VCOML
11	Refresh cycle	White	Black
	Non-refresh cycle	Source=Hi-Z VCOM=Hi-Z	Source=Hi-Z VCOM=Hi-Z

DIVE[1:0]: Used to set division ratio of PCLK clock frequency when the DPI interface selected. The divided PCLK will be used as internal clock for the source pre-charge, VCOM equalizing, etc.

DIVE[1:0]	Division Ratio
2'b00	1/8
2'b01	1/1
2'b10	1/2
2'b11	1/4

6.25 Cycle control 1~2 register (PAGE0 -2Dh~2Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	SDT 2	SDT 1	SDT 0	*	NO W2	NO W1	NO W0
R	1	*	SDT 2	SDT 1	SDT 0	*	NO W2	NO W1	NO W0

Figure 6.43 Cycle control 1 register (PAGE0 -2Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	NW5	NW4	NW3	NW2	NW1	NW0
R	1	*	*	NW5	NW4	NW3	NW2	NW1	NW0

Figure 6.44 Cycle control 2 register (PAGE0 -2Eh)

SDT[2:0]: No function.

NOW[2:0]: Used to set the gate output non-overlap.

1 clock cycle=2 oscillator clock cycle.

NOW[2:0]	Gate Output Non-overlap Period
3'b000	Setting Inhibited
3'b001	1 clock
3'b010	2 clocks
3'b011	3 clocks
3'b100	4 clocks
3'b101	5 clocks
3'b110	6 clocks
3'b111	7 clocks

NW[5:0]: Set number of lines for VCOM inverting.

NW[5:0]	Inversion Lines
6'h00	1 line
6'h01	2 lines
6'h02	3 lines
:	:
6'h3E	63 lines
6'h3F	64 lines

6.26 RGB interface control 1~4 register (PAGE0 -31h~34h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	RM	*	*	DM1	DM0
R	1	*	*	*	RM	*	*	DM1	DM0

Figure 6.45 RGB interface control 1 register (PAGE0 -31h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	SDA_EN	*	*	VSPL	HSPL	*	EPL	DPL
R	1	SDA_EN	0	0	VSPL	HSPL	*	EPL	DPL

Figure 6.46 RGB interface control 2 register (PAGE0 -32h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
R	1	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

Figure 6.47 RGB interface control 3 register (PAGE0 -33h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	HBP9	HBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R	1	HBP9	HBP8	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

Figure 6.48 RGB interface control 4 register (PAGE0 -34h)

This command is used to set RGB interface related register.

RM: Interface slecetion for GRAM access.

RM	Interface for RAM access
0	DBI Interface (CPU)
1	DPI Interface (RGB)

DM[1:0]: Display mode selection for DPI interface.

DM 1	DM 0	Display Mode
0	0	Internal oscillation clock
0	1	DPI interface(GRAM)
1	1	RGB data bypass GRAM mode 1
1	1	RGB data bypass GRAM mode 2

EPL: Specify the polarity of Enable pin in RGB interface mode.

EPL	DE pin	GRAM address	Write to GRAM	Operation
0	Low	Update	Enable	Write data to DB17-0
0	High	Keep	Disable	Disable
1	Low	Keep	Disable	Disable
1	High	Update	Enable	Write data to DB17-0

VSPL: The polarity of VSYNC pin. When VSPL='0', the VSYNC signal is Low active. When VSPL=1, the VSYNC signal is High active.

HSPL: The polarity of HSYNC pin. When HSPL='0', the HSYNC signal is Low active. When HSPL=1, the HSYNC signal is High active.

DPL: The polarity of DOTCLK pin. When DPL='0', the data is latched by the chip on the rising edge of DOTCLK signal. When DPL='1', the data is latched by the chip on the falling edge of DOTCLK signal.

HBP and **VBP** are used to set vertical and horizontal back porch control in RGB I/F bypass GRAM mode 2 (DM[1:0]= '11')

HBP[9:0]: Set the delay period from falling edge of HSYNC signal to first valid data in RGB I/F bypass GRAM mode 2.

HBP[9:0]	No. of Clock Cycle of DOTCLK
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
1021d	1021
1022d	1022
1023d	Setting Inhibited

VBP[5:0]: Set the delay period from falling edge of VSYNC signal to first valid line in RGB I/F bypass GRAM mode 2.

VBP[5:0]	No. of Clock Cycle of HSYNC
00d	Setting Inhibited
01d	Setting Inhibited
02d	2
03d	3
04d	4
:	:
61d	61
62d	62
63d	63

6.27 Panel characteristic control register (PAGE0 -36h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	REV_PANEL	SM_PANEL	GS_PANEL	BGR_PANEL	SS_PANEL
R	1	*	*	*	REV_PANEL	SM_PANEL	GS_PANEL	BGR_PANEL	SS_PANEL

Figure 6.49 Panel characteristic control register (PAGE0 -36h)

This command is internal use for display panel setting.

REV_PANEL: The source output data polarity selected. When REV_PANEL=0, normally white panel is selected. When REV_PANEL = 1, normally black panel is selected.

SM_PANEL: Set the gate driver pin arrangement in combination with the GS bit to slecet the optimal scan mode for the module. Please reference Scan direction of Gate Driver.

GS_PANEL: The gate driver output shift direction selected. When GS_PANEL=0, the shift direction don't reverse. When GS_PANEL = 1, the shift direction will be reversed.

BGR_PANEL: The color filter order direction selected. When BGR_PANEL=0, RGB-BGR order don't reverse. When BGR_PANEL = 1, the color filter order will be reversed.

SS_PANEL: The source driver output shift direction selected. When SS_PANEL=0, the shift direction don't reverse. When SS_PANEL = 1, the shift direction will be reversed.

6.28 OTP control 1~5 register (PAGE0 -38h ~ 3Bh, 87h)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0
R	1	OTP_MASK7	OTP_MASK6	OTP_MASK5	OTP_MASK4	OTP_MASK3	OTP_MASK2	OTP_MASK1	OTP_MASK0

Figure 6.50 OTP control 1 (PAGE0 -38h)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_INDEX7	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0
R	1	OTP_INDEX7	OTP_INDEX6	OTP_INDEX5	OTP_INDEX4	OTP_INDEX3	OTP_INDEX2	OTP_INDEX1	OTP_INDEX0

Figure 6.51 OTP control 2 (PAGE0 -39h)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	*	VPP_EN	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG
R	1	*	VPP_EN	OTP_POR	OTP_PWE	OTP_PTM1	OTP_PTM0	VPP_SEL	OTP_PROG

Figure 6.52 OTP control 3 (PAGE0 -3Ah)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
R	1	OTP_DOUT7	OTP_DOUT6	OTP_DOUT5	OTP_DOUT4	OTP_DOUT3	OTP_DOUT2	OTP_DOUT1	OTP_DOUT0

Figure 6.53 OTP control 4 (PAGE0 -3Bh)

R/W	DNC	D7	D6	D5	D4	D3	D2	D1	D0
W	1	OTP_KEY7	OTP_KEY6	OTP_KEY5	OTP_KEY4	OTP_KEY3	OTP_KEY2	OTP_KEY1	OTP_KEY0
R	1	OTP_KEY7	OTP_KEY6	OTP_KEY5	OTP_KEY4	OTP_KEY3	OTP_KEY2	OTP_KEY1	OTP_KEY0

Figure 6.54 OTP control 5 (PAGE0 -87h)

This command is used to set the OTP related setting. Please see OTP flow for detail use.
OTP_MASK[7:0]: OTP bit programming mask, if set to '1', it means the related bit in OTP can not be programmed.
OTP_INDEX[7:0]: Set index location in OTP to be programmed.
OTP_PROG: When this bit set to "1", it will programmed to the setting OTP index from related register value..
VPP_SEL: When set to '1', VPP input voltage is fed to OTP.
VPP_EN: When written to "1", OTP power OP is enable.
OTP_PTM[1:0]: Internal use, not open.
OTP_PWE: Internal use, not open.
OTP_POR: When set to '1', OTP data can be read the related OTP Index data at OTP_DOUT[7:0]
OTP_DOUT[7:0]: Read OTP data.
OTP_KEY[7:0]: Set to "AAh" to enable OTP control register access.

6.29 CABC control 1~4 register (PAGE0 -3Ch~3Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
R	1	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

Figure 6.55 CABC control 1 register (PAGE0 -3Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	BCTRL	*	DD	BL	*	*
R	1	*	*	BCTRL	*	DD	BL	*	*

Figure 6.56 CABC control 2 register (PAGE0 -3Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	CABC1	CABC0
R	1	*	*	*	*	*	*	CABC1	CABC0

Figure 6.57 CABC control 3 register (PAGE0 -3Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0
R	1	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0

Figure 6.58 CABC control 4 register (PAGE0 -3Fh)

These commands are used to set CABC parameter

DBV[7:0]: The backlight PWM pulse output duty is equal to DBV[7:0]/255 x CABC_duty.

BCTRL: Backlight Control Block On/Off, This bit is always used to switch brightness for display.

'0' = Off (Equal to DBV[7:0] = '00h')

'1' = On (Brightness registers are active.)

DD: Display Dimming (Only for manual brightness setting)

'0': Display Dimming is off.

'1': Display Dimming is on.

BL: Backlight Control On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)

'1' = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (**DD=1**) are selected.

C[1:0]: This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C1	C0	Function	Note
0	0	Off	-
0	1	User Interface Image	-
1	0	Still Picture	-
1	1	Moving Image	-

CMB[7:0]: This command is used to set the minimum brightness value of the display for CABC function.
In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

6.30 Gamma control 1~15 register (PAGE0 -40h~4Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	KP12	KP11	KP10	*	KP02	KP01	KP00
R	1	*	KP12	KP11	KP10	*	KP02	KP01	KP00

Figure 6.59 Gamma control 1 register (PAGE0 -40h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	KP32	KP31	KP30	*	KP22	KP21	KP20
R	1	*	KP32	KP31	KP30	*	KP22	KP21	KP20

Figure 6.60 Gamma control 2 register (PAGE0 -41h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	KP52	KP51	KP50	*	KP42	KP41	KP40
R	1	*	KP52	KP51	KP50	*	KP42	KP41	KP40

Figure 6.61 Gamma control 3 register (PAGE0 -42h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	RP12	RP11	RP10	*	RP02	RP01	RP00
R	1	*	RP12	RP11	RP10	*	RP02	RP01	RP00

Figure 6.62 Gamma control 4 register (PAGE0 -43h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	VRP03	VRP02	VRP01	VRP00
R	1	*	*	*	*	VRP03	VRP02	VRP01	VRP00

Figure 6.63 Gamma control 5 register (PAGE0 -44h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	VRP14	VRP13	VRP12	VRP11	VRP10
R	1	*	*	*	VRP14	VRP13	VRP12	VRP11	VRP10

Figure 6.64 Gamma control 6 register (PAGE0 -45h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	KN12	KN11	KN10	*	KN02	KN01	KN00
R	1	*	KN12	KN11	KN10	*	KN02	KN01	KN00

Figure 6.65 Gamma control 7 register (PAGE0 -46h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	KN32	KN31	KN30	*	KN22	KN21	KN20
R	1	*	KN32	KN31	KN30	*	KN22	KN21	KN20

Figure 6.66 Gamma control 8 register (PAGE0 -47h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	KN52	KN51	KN50	*	KN42	KN41	KN40
R	1	*	KN52	KN51	KN50	*	KN42	KN41	KN40

Figure 6.67 Gamma control 9 register (PAGE0 -48h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	RN12	RN11	RN10	*	RN02	RN01	RN00
R	1	*	RN12	RN11	RN10	*	RN02	RN01	RN00

Figure 6.68 Gamma control 10 register (PAGE0 -49h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	VRN03	VRN02	VRN01	VRN00
R	1	*	*	*	*	VRN03	VRN02	VRN01	VRN00

Figure 6.69 Gamma control 11 register (PAGE0 -4Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	VRN14	VRN13	VRN12	VRN11	VRN10
R	1	*	*	*	VRN14	VRN13	VRN12	VRN11	VRN10

Figure 6.70 Gamma control 12 register (PAGE0 -4Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VREP13	VREP12	VREP11	VREP10	VREP03	VREP02	VREP01	VREP00
R	1	VREP13	VREP12	VREP11	VREP10	VREP03	VREP02	VREP01	VREP00

Figure 6.71 Gamma control 13 register (PAGE0 -4Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VREN03	VREN02	VREN01	VREN00	VREP23	VREP22	VREP21	VREP20
R	1	VREN03	VREN02	VREN01	VREN00	VREP23	VREP22	VREP21	VREP20

Figure 6.72 Gamma control 14 register (PAGE0 -4Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	VREN23	VREN22	VREN21	VREN20	VREN13	VREN12	VREN11	VREN10
R	1	VREN23	VREN22	VREN21	VREN20	VREN13	VREN12	VREN11	VREN10

Figure 6.73 Gamma control 15 register (PAGE0 -4Eh)

VRP0[3:0], VRP1[4:0]: Gamma Offset adjustment registers for positive polarity output
VRN0[3:0], VRN1[4:0]: Gamma Offset adjustment registers for negative polarity output
RP1-0[2:0]: Gamma Center adjustment registers for positive polarity output
RN1-0[2:0]: Gamma Center adjustment registers for negative polarity output
KP5-0[2:0]: Gamma Macro adjustment registers for positive polarity output
KN5-0[2:0]: Gamma Macro adjustment registers for negative polarity output
VREP2-0[3:0]: Gamma EEM adjustment registers for positive polarity output
VREN2-0[3:0]: Gamma EEM adjustment registers for negative polarity output
For details, please refer to 5.7.1.2 Gamma Characteristics Adjustment Register.

6.31 TE control register (PAGE0 -60h, 84h~85h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	TEMODE	TEON	*	*	*
R	1	*	*	*	TEMODE	TEON	*	*	*

Figure 6.74 TE control register (PAGE0 -60h)

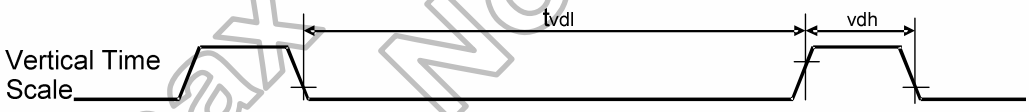
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TSEL15	TSEL14	TSEL13	TSEL12	TSEL11	TSEL10	TSEL9	TSEL8
R	1	TSEL15	TSEL14	TSEL13	TSEL12	TSEL11	TSEL10	TSEL9	TSEL8

Figure 6.75 TE output line2 register (PAGE0 -84h)

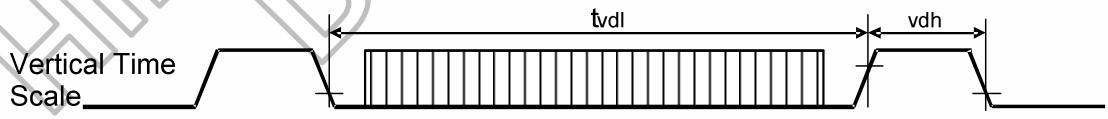
R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	TSEL7	TSEL6	TSEL5	TSEL4	TSEL3	TSEL2	TSEL1	TSEL0
R	1	TSEL7	TSEL6	TSEL5	TSEL4	TSEL3	TSEL2	TSEL1	TSEL0

Figure 6.76 TE output line1 register (PAGE0 -85h)

TEMODE: Specify the Tearing-Effect mode.
When **TEMODE** = '0': The Tearing Effect Output line (TE) consists of V-Blanking information only.



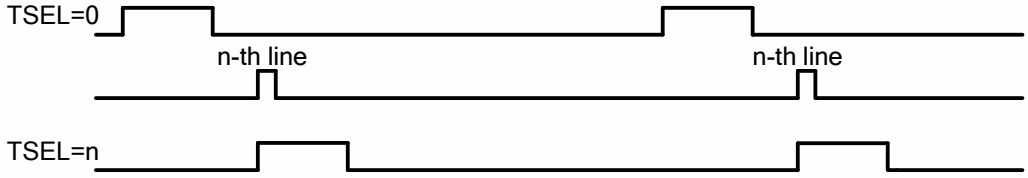
When **TEMODE** ='1': The Tearing Effect Output Line (TE) consists of both V-Blanking and H-Blanking information



Note: During Standby Mode with Tearing Effect Line On, Tearing Effect Output pin active low

TEON: This command is used to turn ON the Tearing Effect output signal from the TE signal line.

TSEL[15:0]: This command is used to setting TE delay line at TEMODE="0". When TSEL[15:0]=16'h0000, TE output is the same as TEMODE="0". When Decimal(TSEL[15:0])=n, TE output at n-th line starting.



6.32 ID register (PAGE0 -61h~63h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10
R	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10

Figure 6.77 ID1 register (PAGE0 -61h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20
R	1	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20

Figure 6.78 ID2 register (PAGE0 -62h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30
R	1	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30

Figure 6.79 ID3 register (PAGE0 -63h)

ID1~ID3: ID setting related register.

6.33 Memory write control register (PAGE0 -68h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	WEMODE	*
R	1	*	*	*	*	*	*	WEMODE	*

Figure 6.80 Memory write control register (PAGE0 -68h)

WEMODE: Memory write control register.
WEMODE = '0': When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.
WEMODE = '1': When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

6.34 TE interval control register (PAGE0 -69h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	TEI2	TEI1	TEI0
R	1	*	*	*	*	*	TEI2	TEI1	TEI0

Figure 6.81 TE interval control register (PAGE0 -69h)

TEI[2:0]: TE output interval control.

TEI[2:0]	TE Output Interval
3'b000	1 frame
3'b001	2 frame
3'b010	3 frame
3'b011	4 frame
3'b100	5 frame
3'b101	6 frame
3'b110	7 frame
3'b111	8 frame

6.35 RGB SRAM cycle control register (PAGE0 -6Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	DENC2	DENC1	DENC0
R	1	*	*	*	*	*	DENC2	DENC1	DENC0

Figure 6.82 RGB SRAM cycle control register (PAGE0 -6Ah)

DENC[2:0]: Set the GRAM write cycle through the RGB interface.

DENC[2:0]	GRAM Write Cycle
3'b000	1 frame
3'b001	2 frame
3'b010	3 frame
3'b011	4 frame
3'b100	5 frame
3'b101	6 frame
3'b110	7 frame
3'b111	8 frame

6.36 Data format control register (PAGE0 -6Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	EPF1	EFP0	*	*	*	DFM
R	1	*	*	EPF1	EPF0	*	*	*	DFM

Figure 6.83 Data format control register (PAGE0 -6Bh)

EPF[1:0]: Set the data mapping 16-bit/pixel data to 18-bit internal GRAM.

EPF[1:0]	Gate Outputs in Non-display Area
2'b00	r[5:0] = {R[4:0],0} g[5:0] = G[5:0] b[5:0] = {B[4:0],0} Exception: R[4:0], B[4:0]=5'h1F => r[5:0], b[5:0]=6'h3E
2'b01	r[5:0] = {R[4:0],1} g[5:0] = G[5:0] b[5:0] = {B[4:0],1} Exception: R[4:0], B[4:0]=5'h00 => r[5:0], b[5:0]=6'h01
2'b10	r[5:0] = {R[4:0],R[4]} g[5:0] = G[5:0] b[5:0] = {B[4:0],B[4]}
2'b11	Compare R[4:0], G[5:1] and B[4:0] : Case 1: R=G=B => r[5:0] = {R[4:0], G[0]}, g[5:0] = G[5:0], b[5:0] = {B[4:0], G[0]} Case 2: R=B≠G => r[5:0] = {R[4:0], R[4]}, g[5:0] = G[5:0], b[5:0] = {B[4:0], B[4]} Case 3: R=G≠B => r[5:0] = {R[4:0], G[0]}, g[5:0] = G[5:0], b[5:0] = {B[4:0], B[4]} Case 4: B=G≠R => r[5:0] = {R[4:0], R[4]}, g[5:0] = G[5:0], b[5:0] = {B[4:0], G[0]}

DFM: No function.

6.37 Frame rate control 1~8 register (PAGE0 -70h~77h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	BC0	*	*	DIV01	DIV00
R	1	*	*	*	BC0	*	*	DIV01	DIV00

Figure 6.84 Frame rate control 1 register (PAGE0 -70h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	RTN04	RTN03	RTN02	RTN01	RTN00
R	1	*	*	*	RTN04	RTN03	RTN02	RTN01	RTN00

Figure 6.85 Frame rate control 2 register (PAGE0 -71h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BP07	BP06	BP05	BP04	BP03	BP02	BP01	BP00
R	1	BP07	BP06	BP05	BP04	BP03	BP02	BP01	BP00

Figure 6.86 Frame rate control 3 register (PAGE0 -72h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	FP07	FP06	FP05	FP04	FP03	FP02	FP01	FP00
R	1	FP07	FP06	FP05	FP04	FP03	FP02	FP01	FP00

Figure 6.87 Frame rate control 4 register (PAGE0 -73h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	BC2	*	*	DIV21	DIV20
R	1	*	*	*	BC2	*	*	DIV21	DIV20

Figure 6.88 Frame rate control 5 register (PAGE0 -74h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	RTN24	RTN23	RTN22	RTN21	RTN20
R	1	*	*	*	RTN24	RTN23	RTN22	RTN21	RTN20

Figure 6.89 Frame rate control 6 register (PAGE0 -75h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	BP27	BP26	BP25	BP24	BP23	BP22	BP21	BP20
R	1	BP27	BP26	BP25	BP24	BP23	BP22	BP21	BP20

Figure 6.90 Frame rate control 7 register (PAGE0 -76h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	FP27	FP26	FP25	FP24	FP23	FP22	FP21	FP20
R	1	FP27	FP26	FP25	FP24	FP23	FP22	FP21	FP20

Figure 6.91 Frame rate control 8 register (PAGE0 -77h)

BC0: Used to select Normal/Partial mode VCOM drive waveform.
BC2: Used to select Idle mode VCOM drive waveform.
'0': Frame inversion waveform is selected
'1': Line inversion waveform is selected.

DIV0[1:0]: Used to set Normal/Partial mode division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV0 setting is changed, the width od the reference clock for LC control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits)

DIV2[1:0]: Used to set Idle mode division ratio of internal clock frequency. The internal operation is synchronized with the frequency divided internal clock. When DIV2 setting is changed, the width od the reference clock for LC control signals is changed. The frame frequency can be adjusted by register setting (RTN and DIV bits)

DIV0/2[1:0]	Division Ratio
2'b00	fosc/1
2'b01	fosc/2
2'b10	fosc/4
2'b11	fosc/8

RTN0[4:0]: Specify Normal/Partial mode clock number of one line period for internal operation.

RTN2[4:0]: Specify Idle mode clock number of one line period for internal operation.

Clock cycles=1/internal operation clock frequency(fosc)

RTN0/2[4:0]	Clock number per Line	RTN0/2[4:0]	Clock number per Line
5'b00000	Setting Inhibited	5'b10000	132
5'b00001	Setting Inhibited	5'b10001	133
5'b00010	Setting Inhibited	5'b10010	134
5'b00011	Setting Inhibited	5'b10011	135
5'b00100	Setting Inhibited	5'b10100	136
5'b00101	Setting Inhibited	5'b10101	137
5'b00110	Setting Inhibited	5'b10110	138
5'b00111	Setting Inhibited	5'b10111	139
5'b01000	Setting Inhibited	5'b11000	140
5'b01001	Setting Inhibited	5'b11001	141
5'b01010	Setting Inhibited	5'b11010	142
5'b01011	127	5'b11011	143

5'b01100	128	5'b11100	144
5'b01101	129	5'b11101	145
5'b01110	130	5'b11110	146
5'b01111	131	5'b11111	147

BP0[7:0]: Specify Normal/Partial mode back porch lines.

BP2[7:0]: Specify Idle mode back porch lines.

FP0[7:0]: Specify Normal/Partial mode front porch lines.

FP2[7:0]: Specify Idle mode front porch lines.

BP0/2[7:0], FP0/2[7:0]	Line number of back/front porch
000d	15
001d	16
002d	17
003d	18
004d	19
:	:
127d	142
128d	Setting Inhibited
129d	Setting Inhibited
130d	2
131d	3
132d	4
:	:
142d	14
others	Setting Inhibited

6.38 Power control 6~11 register (PAGE0 -7Ah~7Fh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	SAP02	SAP01	SAP00
R	1	*	*	*	*	*	SAP02	SAP01	SAP00

Figure 6.92 Power control 6 register (PAGE0 -7Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DC102	DC101	DC100	*	DC002	DC001	DC000
R	1	*	DC102	DC101	DC100	*	DC002	DC001	DC000

Figure 6.93 Power control 7 register (PAGE0 -7Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	SAP12	SAP11	SAP10
R	1	*	*	*	*	*	SAP12	SAP11	SAP10

Figure 6.94 Power control 8 register (PAGE0 -7Ch)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DC112	DC111	DC110	*	DC012	DC011	DC010
R	1	*	DC112	DC111	DC110	*	DC012	DC011	DC010

Figure 6.95 Power control 9 register (PAGE0 -7Dh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	SAP22	SAP21	SAP20
R	1	*	*	*	*	*	SAP22	SAP21	SAP20

Figure 6.96 Power control 10 register (PAGE0 -7Eh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	DC122	DC121	DC120	*	DC022	DC021	DC020
R	1	*	DC122	DC121	DC120	*	DC022	DC021	DC020

Figure 6.97 Power control 11 register (PAGE0 -7Fh)

SAP0[2:0]: Used to adjust the Normal mode constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the driving ability of the LCD, but it also increases the current consumption. In no-display period, set SAP0[2:0]=3'b000 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

SAP1[2:0]: Used to adjust the Partial mode constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the driving ability of the LCD, but it also increases the current consumption. In no-display period, set SAP1[2:0]=3'b000 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

SAP2[2:0]: Used to adjust the Idle mode constant current in the operational amplifier circuit in the LCD power supply circuit. Larger constant current enhances the driving ability of the LCD, but it also increases the current consumption. In no-display period, set SAP2[2:0]=3'b000 to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

SAP0/1/2[2:0]	Gamma Driver Amplifier	Source Driver Amplifier
3'b000	Halt operation	Halt operation
3'b001	1.00	1.00
3'b010	1.00	0.75
3'b011	1.00	0.50
3'b100	0.75	1.00
3'b101	0.75	0.75
3'b110	0.75	0.50
3'b111	0.50	0.50

DC00[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Normal mode.

DC01[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Partial mode.

DC02[2:0]: Set the operating frequency of the step-up circuit 1 and extra step-up circuit 1 for DDVDH voltage generation in Idle mode.

DC00/1/2[2:0]	Operation Frequency of Step-up Circuit 1 and Extra Step-up circuit 1
3'b000	¼ x H Line Frequency
3'b001	½ x H Line Frequency
3'b010	1 x H Line Frequency
3'b011	1.5 x H Line Frequency
3'b100	2 x H Line Frequency
3'b101	3 x H Line Frequency
3'b110	4 x H Line Frequency
3'b111	8 x H Line Frequency

DC10[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Normal mode.

DC11[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Partial mode.

DC12[2:0]: Set the operating frequency of the step-up circuit 2 and 3 for VGH, VGL and VCL voltage generation in Idle mode.

DC10/1/2[2:0]	Operation Frequency of Step-up Circuit 2, Step-up Circuit 3
3'b000	¼ x H Line Frequency
3'b001	½ x H Line Frequency
3'b010	1 x H Line Frequency
3'b011	1.5 x H Line Frequency
3'b100	2 x H Line Frequency
3'b101	3 x H Line Frequency
3'b110	4 x H Line Frequency
3'b111	8 x H Line Frequency

6.39 VPP voltage control register (PAGE0 -86h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	VPP2	VPP1	VPP0
R	1	*	*	*	*	*	VPP2	VPP1	VPP0

Figure 6.98 VPP voltage control register (PAGE0 -86h)

VPP[2:0]: Internal generated OTP VPP voltage setting.

VPP2	VPP1	VPP0	VPP Voltage
0	0	0	7.2V
0	0	1	7.3V
0	1	0	7.4V
0	1	1	7.5V
1	0	0	7.6V
1	0	1	7.7V
1	1	0	7.8V
1	1	1	Exrenal VPP Supplied

6.40 Get scan line 1~2 register (PAGE0 -88h~89h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8

Figure 6.99 Get scan line 2 register (PAGE0 -88h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

Figure 6.100 Get scan line 1 register (PAGE0 -89h)

SL[15:0]: The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.

6.41 Read VCOM OTP times register (PAGE0 -R8Ah)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	VCOM_OTP_TIMES3	VCOM_OTP_TIMES2	VCOM_OTP_TIMES1	VCOM_OTP_TIMES0

Figure 6.101 Read VCOM OTP times register (PAGE0 -R8Ah)

VCOM_OTP_TIMES[3:0]: Read VCOM OTP programmed times.

VCOM_OTP_TIMES[3:0]	VCOM OTP programmed times
4'b0000	Not programmed
4'b0001	1 time
4'b0010	2 times
4'b0011	3 times
4'b0100	4 times
4'b0101	5 times
4'b0110	6 times
4'b0111	7 times
4'b1000	8 times

6.42 Read ID OTP times register (PAGE0 -R8Bh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
R	1	0	0	0	0	ID_OTP_TIMES3	ID_OTP_TIMES2	ID_OTP_TIMES1	ID_OTP_TIMES0

Figure 6.102 Read ID OTP times register (PAGE0 -R8Bh)

ID_OTP_TIMES[3:0]: Read ID OTP programmed times.

ID_OTP_TIMES[3:0]	ID OTP programmed times
4'b0000	Not programmed
4'b0001	1 time
4'b0010	2 times
4'b0011	3 times
4'b0100	4 times
4'b0101	5 times
4'b0110	6 times
4'b0111	7 times
4'b1000	8 times

6.43 Command page select register (RFFh)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	PAGE_SEL1	PAGE_SEL0
R	1	0	0	0	0	0	0	PAGE_SEL1	PAGE_SEL0

Figure 6.103 Command page select register (RFFh)

PAGE_SEL[1:0]: Command set page select.

PAGE_SEL1	PAGE_SEL0	Command Page
0	0	Page 0
0	1	Page 1

6.44 DGC control register (PAGE1 -00h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	*	*	*	*	*	*	*	DGC_EN
R	1	0	0	0	0	0	0	0	DGC_EN

Figure 6.104 DGC control register (PAGE1 -00h)

DGC_EN: Digital gamma correction enable.
0: Disable
1: Enable

6.45 DGC LUT register (PAGE1 -01h~63h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	D7	D6	D5	D4	D3	D2	D1	D0
R	1	D7	D6	D5	D4	D3	D2	D1	D0

Figure 6.105 DGC LUT register (PAGE1 -01h~63h)

There are 99 bytes DGC LUT to set R, G, B gamma independently. When DGC_EN=1, R, G, B gamma will mapping V0, V2, V4, ..., V60, V62, V63 voltage to the LUT register setting gray level voltage of real gamma. V(2N+1) = (V(2N) + V(2N+2))/2 (N=0~30).

LUT	D7	D6	D5	D4	D3	D2	D1	D0	Default	Gray Mapping
R01h	R007	R006	R005	R004	R003	R002	R001	R000	00h	R_V0
R02h	R017	R016	R015	R014	R013	R012	R011	R010	08h	R_V2
R03h	R027	R026	R025	R024	R023	R022	R021	R020	10h	R_V4
:	:	:	:	:	:	:	:	:	:	:
R20h	R317	R316	R315	R314	R313	R312	R311	R310	F8h	R_V62
R21h	R327	R326	R325	R324	R323	R322	R321	R320	FCh	R_V63
R22h	G007	G006	G005	G004	G003	G002	G001	G000	00h	G_V0
R23h	G017	G016	G015	G014	G013	G012	G011	G010	08h	G_V2
R24h	G027	G026	G025	G024	G023	G022	G021	G020	10h	G_V4
:	:	:	:	:	:	:	:	:	:	:
R41h	G317	G316	G315	G314	G313	G312	G311	G310	F8h	G_V62
R42h	G327	R326	G325	G324	G323	G322	G321	G320	FCh	G_V63
R43h	B007	B006	B005	B004	B003	B002	B001	B000	00h	B_V0
R44h	B017	B016	B015	B014	B013	B012	B011	B010	08h	B_V2
R45h	B027	B026	B025	B024	B023	B022	B021	B020	10h	B_V4
:	:	:	:	:	:	:	:	:	:	:
R62h	B317	B316	B315	B314	B313	B312	B311	B310	F8h	B_V62
R63h	B327	B326	B325	B324	B323	B322	B321	B320	FCh	B_V63

6.46 CABC control 5 & 7 register (PAGE1 –C3h, C5h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	LEDONPOL	PWMDIV2	PWMDIV1	PWMDIV0	SEL_GAIN1	SEL_GAIN0	INVPLUS	SEL_BLDUTY
R	1	LEDONPOL	PWMDIV2	PWMDIV1	PWMDIV0	SEL_GAIN1	SEL_GAIN0	INVPLUS	SEL_BLDUTY

Figure 6.106 CABC control 5 register (PAGE1 –C3h)

R/W	DNC	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
W	1	PWM_PERIOD7	PWM_PERIOD6	PWM_PERIOD5	PWM_PERIOD4	PWM_PERIOD3	PWM_PERIOD2	PWM_PERIOD1	PWM_PERIOD0
R	1	PWM_PERIOD7	PWM_PERIOD6	PWM_PERIOD5	PWM_PERIOD4	PWM_PERIOD3	PWM_PERIOD2	PWM_PERIOD1	PWM_PERIOD0

Figure 6.107 CABC control 7 register (PAGE1 –C5h)

LEDONPOL: The control reigister for LED driver when IC needs enable signal.
'0': LEDONPOL pin='L'.
'1': LEDONPOL pin='H'.

PWMDIV[2:0]: Internal PWM_CLK divider for CABC clock.

PWMDIV[2:0]	Divider
0	PWM_CLK/1
1	PWM_CLK/2
2	PWM_CLK/4
3	PWM_CLK/8
4	PWM_CLK/16
5	PWM_CLK/32
6	PWM_CLK/64
7	PWM_CLK/128

SEL_GAIN[1:0]: CABC gain select. **(Not Open)**

SEL_BLDUTY: The backlight PWM output duty on/off control when CABC operated.
'0': The backlight PWM output duty is 100%.
'1': The backlight PWM output duty is calculated from CABC operation.

INVPULS: The backlight PWM output polarity select.
'0', The backlight PWM output is low level active.
'1', The backlight PWM output is high level active.

PWM_PERIOD[7:0] : The backlight PWM output period setting.
Backlight PWM output period = 1 / (PWM_CLK / clock divider (PWMDIV)) x (255x(PWM_PERIOD[7:0]+1))

7. Layout Recommendation

7.1 Layout Recommendation

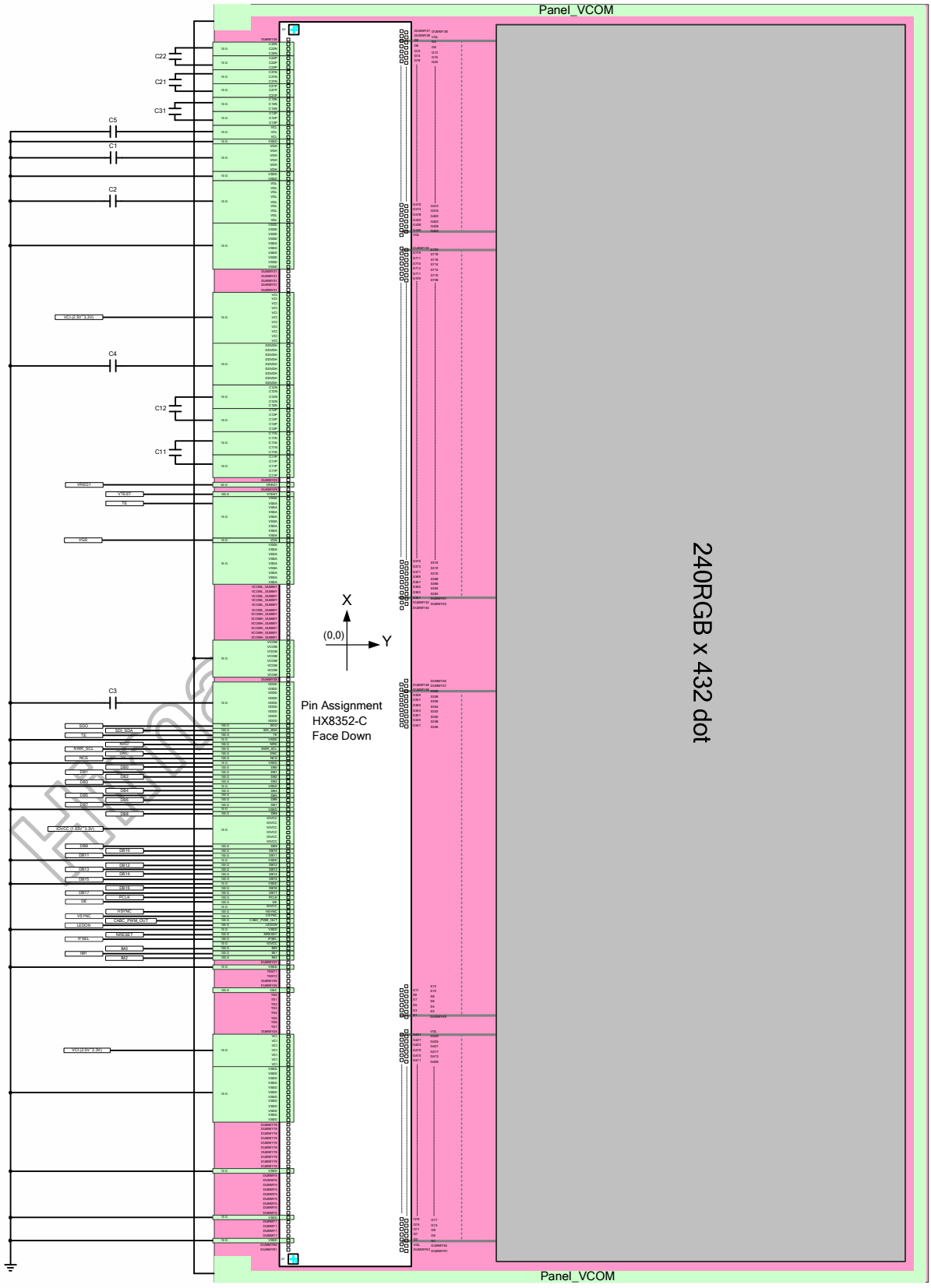


Figure 7.1: Layout Recommendation

7.2 Maximum layout resistance

Name	Type	Maximum series resistance	Unit
IOVCC	Power supply	10	Ω
VCI	Power supply	10	Ω
VSSD	Power supply	10	Ω
VSSA	Power supply	10	Ω
IFSEL, IM[2:0]	Input	100	Ω
NRD, NWR_SCL, DNC, NCS, NRESET	Input	100	Ω
HSYNC, VSYNC, DE, PCLK	Input	100	Ω
SDI_SDA	Input + Output	100	Ω
DB[17:0]	Output	100	Ω
SDO, CABC_PWM_OUT, LEDON, TE	Output	100	Ω
VCOM	Output	10	Ω
VDDD	Capacitor Connection	10	Ω
DDVDH	Capacitor Connection	10	Ω
VREG1	Output	50	Ω
VGS	Power supply	10	Ω
VCL	Capacitor Connection	10	Ω
VGL	Capacitor Connection	10	Ω
VGH	Capacitor Connection	10	Ω
OSC	Input	100	Ω
C11P,C11N,C12P,C12N,, C21P,C21N,C22P,C22N, C31P,C31N	Capacitor Connection	10	Ω
TEST[2:1]	Input	100	Ω
VTEST, TS[7:0]	Output	100	Ω

Table 7.1: Maximum Layout Resistance

7.3 External Components Connection

Internal charge pumping mode:

Symbol	Pad Name	Connection	Typical Component Value
C1	VGH	Connect to Capacitor (Min. 25V): VGH ---(+)----| |--- (-)----- VSSA	1 µF
C2	VGL	Connect to Capacitor (Min. 16V): VGL ---(+)----| |--- (-)----- VSSA	1 µF
C11	C11P – C11N	Connect to Capacitor (Min. 6V): C11P ---(+)----| |--- (-)-----C11N	1 µF
C12	C12P – C12N	Connect to Capacitor (Min. 6V): C12P ---(+)----| |--- (-)-----C12N	1 µF
C21	C21P – C21N	Connect to Capacitor (Min. 10V): C21P ---(+)----| |--- (-)-----C21N	1 µF
C22	C22P – C22N	Connect to Capacitor (Min. 10V): C22P ---(+)----| |--- (-)-----C22N	1 µF
C31	C31P – C31N	Connect to Capacitor (Min. 6V): C31P ---(+)----| |--- (-)-----C31N	1 µF
C3	VDDD	Connect to Capacitor (Min. 6V): VDDD ---(+)----| |--- (-)-----VSSD	1 µF
C4	DDVDH	Connect to Capacitor (Min. 10V):DDVDH ---(+)----| |--- (-)-----VSSA	1 µF
C5	VCL	Connect to Capacitor (Min. 6V):VCL ---(+)----| |--- (-)-----VSSA	1 µF

Table 7.2: Adoptability of component

8. Electrical Characteristics

8.1 Absolute maximum ratings

The absolute maximum ratings are list on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	IOVCC~ VSSD	V	-0.3 to +4.6	Note(1),(2)
Power Supply Voltage 2	VCI ~ VSSA	V	-0.3 to +4.6	Note(1),(3)
Power Supply Voltage 3	DDVDH ~ VSSA	V	-0.3 to +6.6	Note(4)
Power Supply Voltage 4	VSSA ~ VCL	V	-0.3 to +4.6	Note(5)
Power Supply Voltage 5	DDVDH ~ VCL	V	-0.3 to +9	Note(6)
Power Supply Voltage 6	VGH ~ VSSA	V	-0.3 to 18.5	Note(7)
Power Supply Voltage 6	VSSA ~ VGL	V	-16.5 to 0	Note(8)
Operating Temperature	Topr	°C	-40 to +85	Note(9)
Storage Temperature	Tstg	°C	-55 to +110	Note(10)

Note: (1) IOVCC, VCI, VSSD, VSSSA must be maintained.
(2) To make sure IOVCC ≥ VSSD.
(3) To make sure VCI ≥ VSSA.
(4) To make sure DDVDH ≥ VSSA.
(5) To make sure VSSA ≥ VCL.
(6) To make sure DDVDH ≥ VCL
(7) To make sure VGH ≥ VSSA.
(8) To make sure VSSA ≥ VGL
VGH +|VGL| < 32V
(9) For die and wafer products, specified up to +85℃.
(10) This temperature specifications apply to the TCP package.

Table 8.1: Absolute maximum rating

8.2 DC characteristics

(VCI=2.5 ~ 3.3V, IOVCC=1.65~3.3V, T_A=-40 ~ 85 ºC)

Item	Symbol	Unit	Test condition	Min.	Typ.	Max.
Input high voltage	V_{IH}	V	IOVCC=1.65 ~ 3.3V	0.7xIOVCC	-	IOVCC
Input low voltage	V_{IL}	V	IOVCC=1.65 ~ 3.3V	-0.3V	-	0.3xIOVCC
Output high voltage (DB0-17 Pins, SDA/SDO)	V_{OH1}	V	I_{OH}= -1mA	0.8xIOVCC	-	-
Output low voltage (DB0-17 Pins, SDA/SDO)	V_{OL1}	V	IOVCC=1.65 ~ 2.4V I_{OL}=1mA	-	-	0.2xIOVCC
I/O leakage current	I_{Li}	µA	Vin=0 ~ IOVCC	-1	-	1
Current consumption during normal operation (IOVCC-VSSD)	$I_{OP(IOVCC)}$	µA	IOVCC=VCI=2.8V , Ta=25℃ , GRAM data=0000h, Frame rate=60Hz, REV=0, AP=011, DC0=100, DC1=100, BT=010, VCIRE=1, VRH=01000, VCOMG=1	-	850	-
Current consumption during normal operation (VCI – VSSA)	$I_{OP(VCI)}$	mA		-	6.5	-
Current consumption during standby mode (IOVCC-VSSD)	$I_{ST(IOVCC)}$	µA	IOVCC=2.8V, VCI=2.8V , Ta=25°C	-	-	60
Current consumption during standby mode (VCI-VSSA)	$I_{ST(VCI)}$	µA		-	-	10
Output voltage deviation	DOS	mV	VSSD+1.0V ~ VREG1-1.0V	-	±10	±20
			VSSD+0.1V ~ VSSD+1.0V VREG1-1.0V ~ VERG1-.01V	-	±30	±50
Dispersion of the Average Output Voltage	V	mV	-	-	-	35

Table 8.2: DC characteristic

8.3 AC characteristics

8.3.1 8080 system interface characteristics

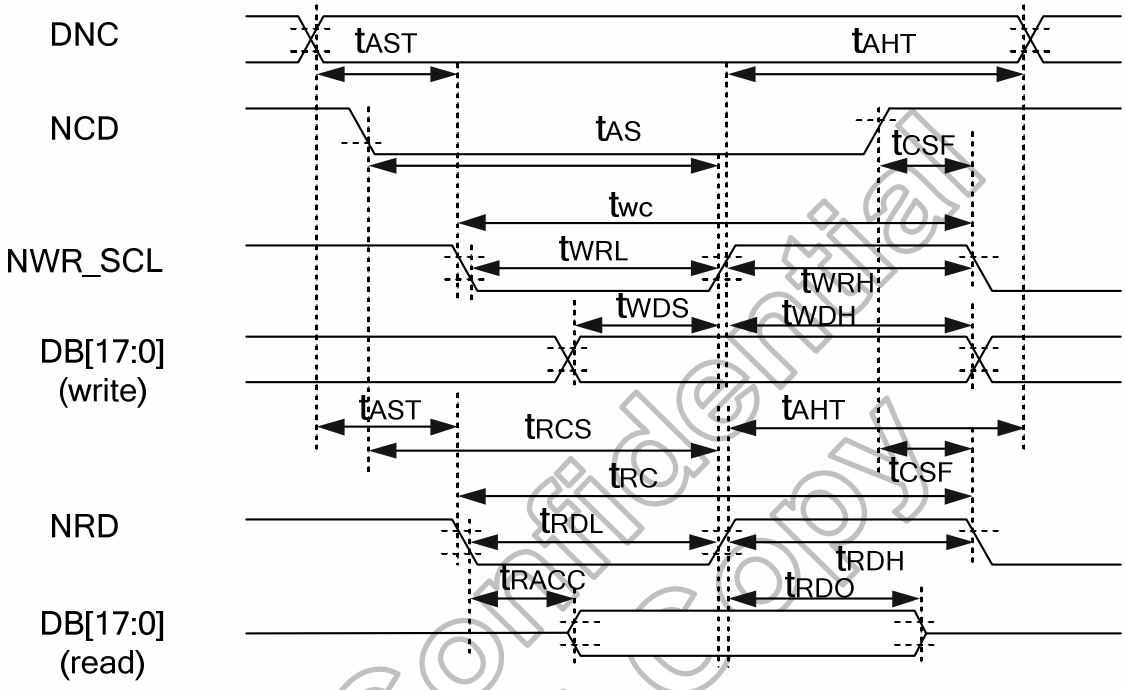


Figure 8.1: I80 interface characteristics

(VSSA=0V, IOVCC=1.8V, VCI=2.8V, T_A=25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NCS	t_{CS}	Chip select setup time (Write)	15	-	ns	-
	t_{RCS}	Chip select setup time (Read register)	45	-		
	t_{RCS}	Chip select setup time (GRAM)	355	-		
	t_{CSF}	Chip select wait time (Write/Read)	10	-		
NWR_SCL	t_{WC}	Write cycle (1 pixel/1 time)	100	-	ns	-
	t_{WC}	Write cycle (1 pixel/2 or 3 times)	50	-		
	t_{WRH}	Control pulse “H” duration	15	-		
	t_{WRL}	Control pulse “L” duration	15			
NRD	t_{RC}	Read cycle (read register)	160	-	ns	-
	t_{RC}	Read cycle (GRAM)	450	-		
	t_{RDH}	Control pulse “H” duration	90	-		
	t_{RDL}	Control pulse “L” duration(read register)	45	-		
	t_{RDL}	Control pulse “L” duration(GRAM)	355	-		
DB[17:0]	t_{WDT}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{WHT}	Data hold time	10	-		
	t_{RACC}	Read access time(read register)	-	40		
	t_{RACC}	Read access time(GRAM)	-	340		
	t_{ROH}	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.3: I80 interface characteristics

8.3.2 Serial interface characteristics

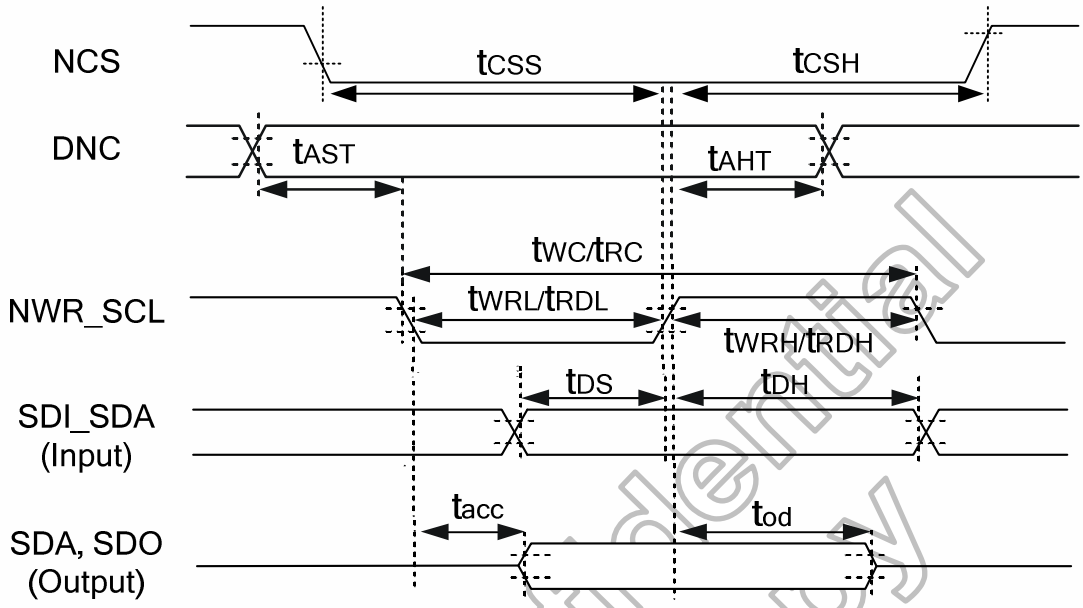


Figure 8.2: Serial interface characteristics

(VSSA=0V, IOVCC=1.8V, VCI=2.8V, T_A = 25℃)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
NCS	t_{CSS}	Chip select setup time (Write)	15	-	ns	-
	t_{CSS}	Chip select setup time (Read)	60	-		
	t_{CSH}	Chip select hold time (Write)	15	-		
	t_{CSH}	Chip select hold time (Read)	65	-		
DNC	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
NWR_SCL (Write)	t_{WC}	Write cycle	20	-	ns	-
	t_{WRH}	Control pulse “H” duration	10	-		
	t_{WRL}	Control pulse “L” duration	10	-		
NWR_SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse “H” duration	60	-		
	t_{RDL}	Control pulse “L” duration	60	-		
SDI_SDA (Input)	t_{DS}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DT}	Data hold time	10	-		
SDA, SDO (Output)	t_{RACC}	Read access time	10	50	ns	
	t_{OD}	Output disable time	15	50		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 8.4: Serial interface characteristics

8.3.3 RGB interface characteristics

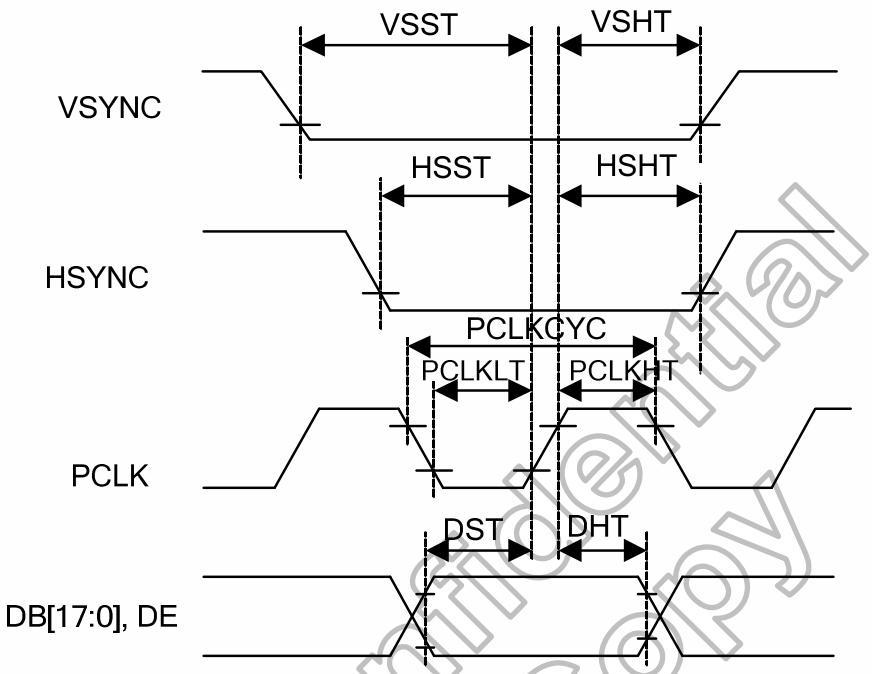


Figure 8.3: General timings for RGB I/F-1

(T_A=25°C, IOVCC=1.65~3.3V, VCI=2.5~3.3V, VSSA=0V)

Item	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical sync. Setup Time	VSST	-	10	-	-	ns
Vertical sync. Hold Time	VSHT	-	10	-	-	ns
Horizontal sync. Setup Time	HSST	-	10	-	-	ns
Horizontal sync. Hold Time	HSHT	-	10	-	-	ns
Pixel Clock Cycle	PCLKCYC	18-/ 16-bit	100	-	-	ns
Pixel Clock Setup Time	PLCKLT	-	10	-	-	ns
Pixel Clock High Time	PCLKHT	-	10	-	-	ns
Data Setup Time DB[17:0], Enable	DST	-	10	-	-	ns
Data Hold Time DB[17:0], Enable	DHT	-	10	-	-	ns

Note: (1) Signal rise and fall times are equal or less than 20ns.
(2) Measure of input signals are using 0.3xIOVCC for low state and 0.7xIOVCC for high state.

Table 8.5: RGB interface characteristics-1

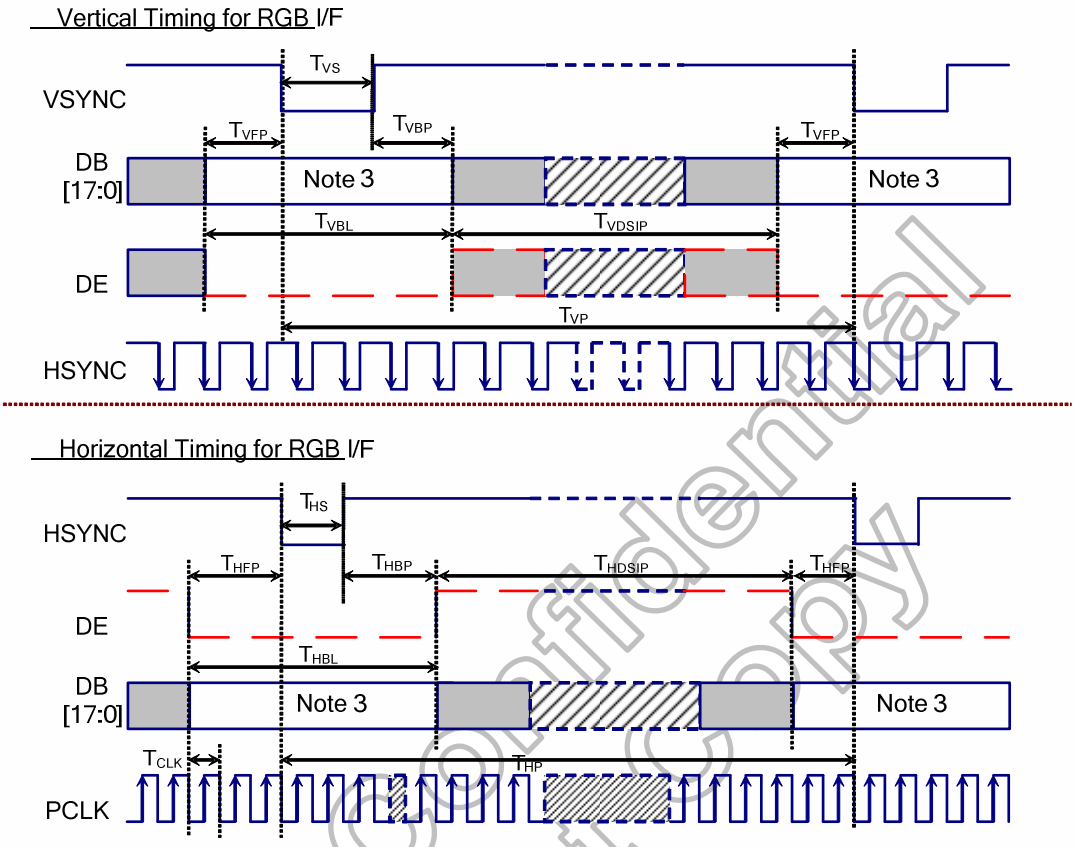


Figure 8.4: General timings for RGB I/F-2

Item	Symbol	Condition	Specification			Unit
			Min	Type.	Max	
Vertical Timing						
Vertical cycle period	T_{VP}	-	438	-	503	HS
Vertical low pulse width	T_{VS}	-	2	2	-	HS
Vertical front porch	T_{VFP}	-	2	2	6	HS
Vertical back porch	T_{VBP}	-	2	6	63	HS
Vertical blanking period	T_{VBL}	$T_{VS} + T_{VBP} + T_{VFP}$	6	10	71	HS
Vertical active area	T_{VDISP}	-	-	432	-	HS
			-		-	HS
					-	HS
Vertical refresh rate	T_{VRR}	Frame rate	50	60	80	Hz
Horizontal Timing						
Horizontal cycle period	T_{HP}	-	246	-	1008	PCLK
Horizontal low pulse width	T_{HS}	-	2	2	256	PCLK
Horizontal front porch	T_{HFP}	-	2	2	256	PCLK
Horizontal back porch	T_{HBP}	-	2	6	256	PCLK
Horizontal blanking period (through mode)	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	6	10	768	PCLK
Horizontal blanking period (capture mode)	T_{HBL}	$T_{HS} + T_{HBP} + T_{HFP}$	47	51	768	PCLK
Horizontal active area	T_{HDISP}	-	-	240	-	PCLK
Pixel clock cycle	f_{CLKCYC}	-	5.39	-	10	MHz

Note: (1) IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, VSSA=VSSD=0V, Ta=-30 to 70℃ (to +85℃ no damage)
(2) Data lines can be set to "High" or "Low" during blanking time – Don't care.
(3) HP is multiples of PCLK.

Table 8.6: RGB interface characteristics-2

8.3.4 Reset input timing

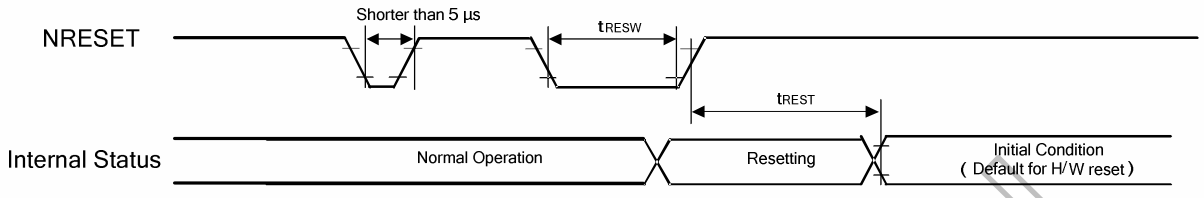


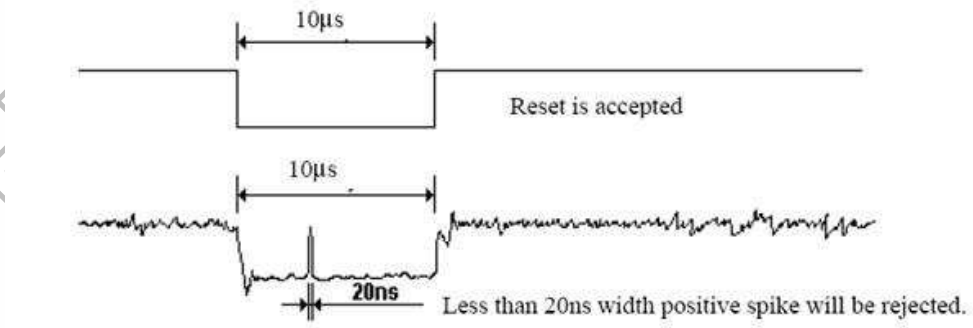
Figure 8.5: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width(1)	NRESET	10	-	-	-	µs
t_{REST}	Reset operating time(2)	-	5	-	-	When reset is applied during Standby mode	ms
		-	120	-	-	When reset is applied during STB Out mode	ms

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Standby Out –mode. The display remains the blank state in Standby –mode) and then returns to Default condition for H/W reset.
(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Standby Mode.
(6) When Reset is applied during Standby Out Mode.
(7) It is necessary to wait 5msec after releasing NRESET before sending commands. Also Standby Out command cannot be sent for 120msec.

Table 8.7: Reset timing

9. Ordering Information

Part No.	Package
HX8352-C010 PDxxx	PD: mean COG xxx: mean chip thickness (μm), (default: 250 μm)

10. Revision History

Version	Date	Description of Changes
01	2010/09/29	New setup
	2010/10/18	Modify SPI AC timing in P.157.
	2011/01/28	Modify IFSEL description in P.14.
	2011/05/18	Modify input pad size in P.16.