FSA506

(FSA0AC197A)

FSA506

Preliminary Specification

Version 0.3

Date: 2007/06/02

Prepared by: Y.C. Lee

0 Revise History

Date	Version	Description	Owner
2007/03/08	V 0.1	Initialized Release	Y.C.
2007/04/27	V 0.2	Register setting	Y.C.
2007/06/02	V 0.3	General function added	Y.C.

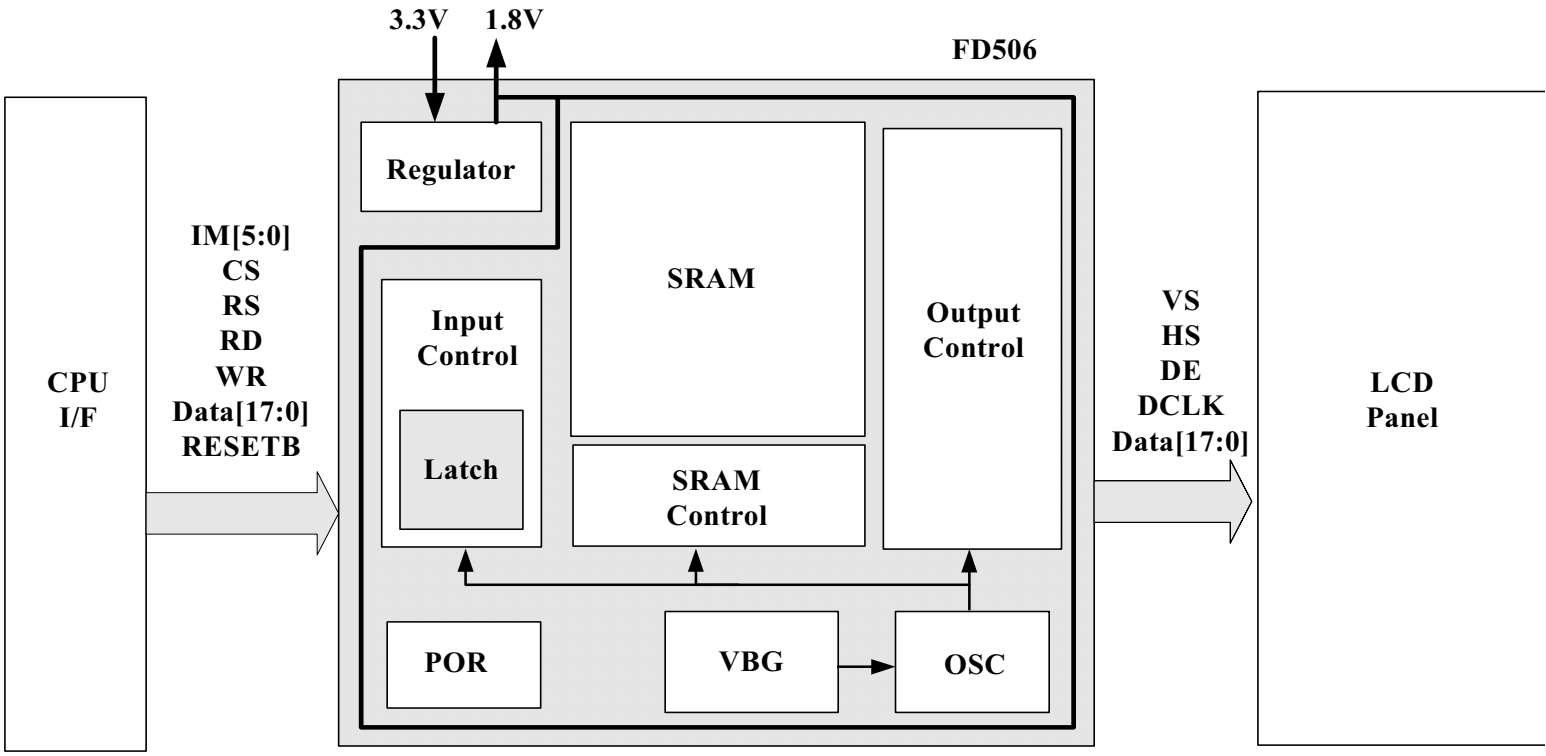
1 Introduction

FSA506 is a CPU interface based TFT LCD controller. It can support panel resolution up to 640x240 pixels with 262144 colors depth. User can send either a full screen picture or a partial image by controlling the MPU with popular microprocessor interface, 18/16/9/8 bits 68-series or 80-series. Output data and synchronization signals will be delivered to TCON simultaneously.

The integrated on-chip functions include:

- Supported panel resolution
  - Max. 153600 pixels (H x V) resolution
- Built-in separated RGB SRAM with 18-bits addressing space
- MPU data transfer interface
  - 18/16/9/8-bis 68-series system
  - 18/16/9/8-bis 80-series system
- Both delta and stripe type panel supported
- Build in Images rotate and shift function
- Arbitrary display memory address access
- Supply voltage: 3.3v
- 100 pin LQFP package

2 Block Diagram



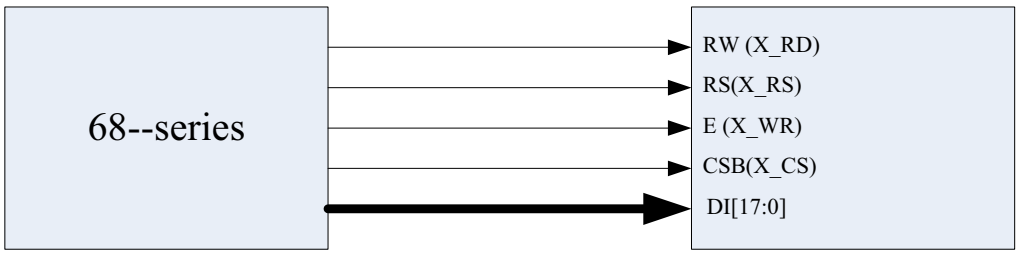
3 System Organization

3.1 MPU interface connection

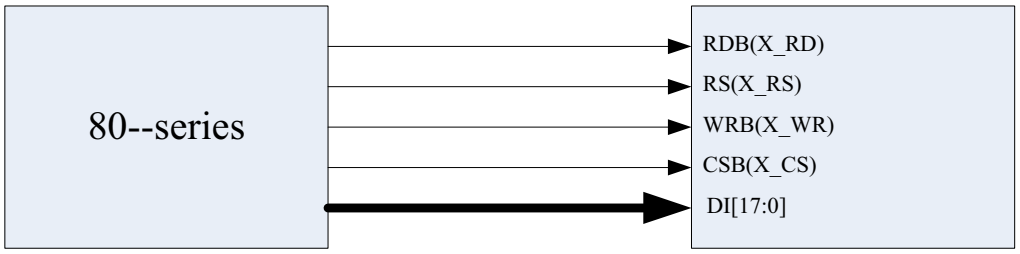
FD506 can support both MPU interfaces with variable data bus width. User can change to different mode by configuring the input ports and related registers. These two interfaces are 68-series and 80-series

- 68-series: Without address bus, data bus may be configured to 18/9/16/8 bits.
- 80-series: same as 68 series but the way of controlling signals.

3.1.1 68-series interface

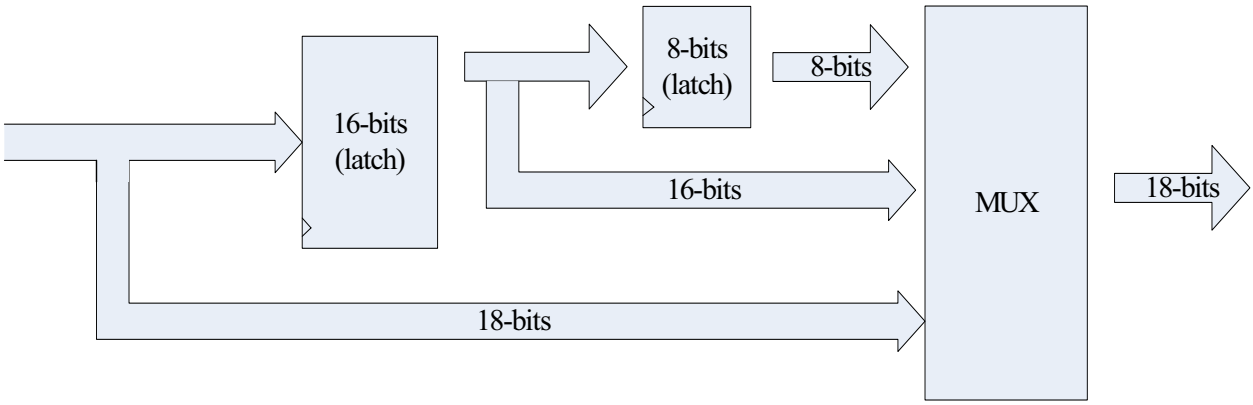


3.1.2 80-series interface



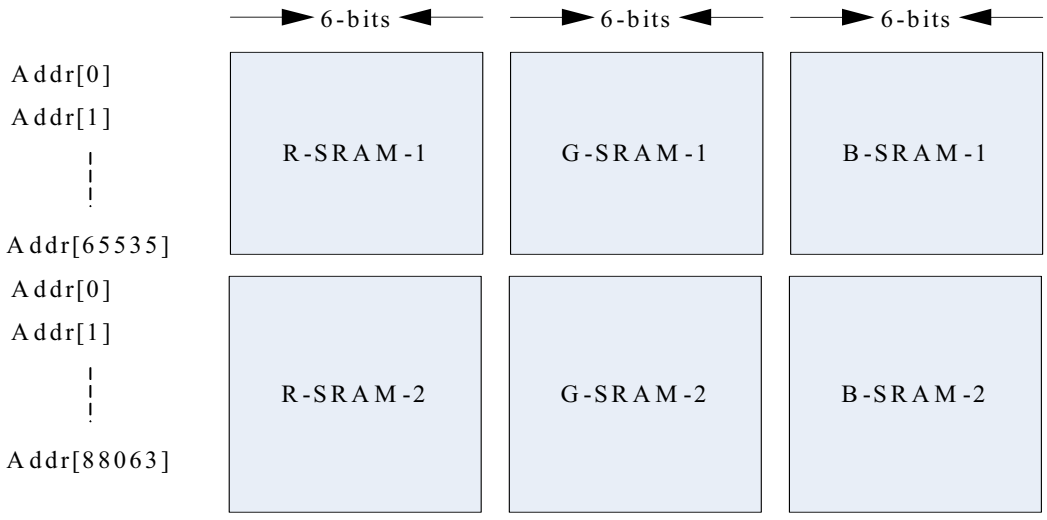
3.2 Input Interface

FD506 has variable interface data input including 8/9/16/18 bits and data depth (666 or 565), therefore before writing into memory it needs to be latched and normalized. The aim of this block is to normalize the input data from variable MPU interface and save them to memory in regular way. Following diagram shows the data flow in this block.



3.3 Memory Configuration

The size of SRAM of FD506 is 640x240x3x6 bits. It can be configured into 6 parts and each part has 6 bits width.

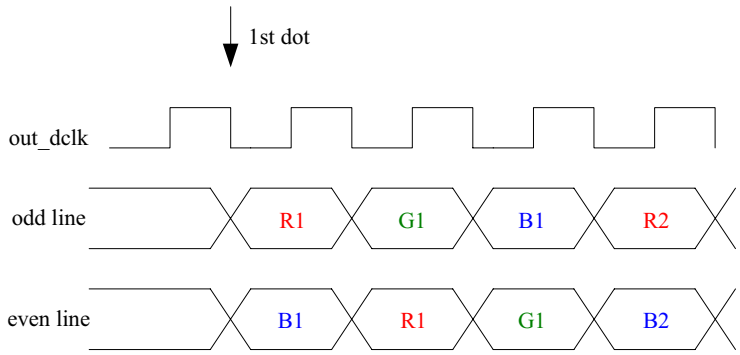


3.4 Output unit

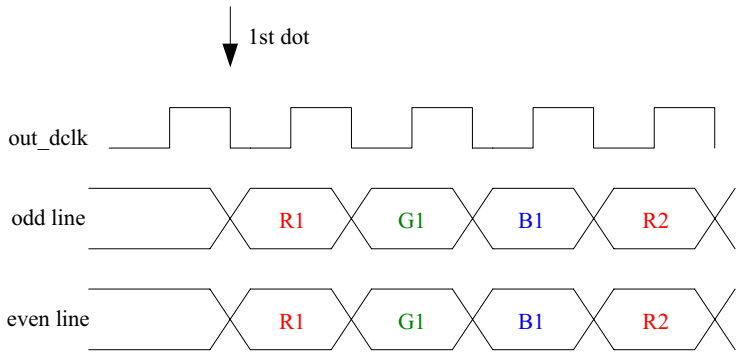
Output controller is a unit translating the parallel data to serial one and ordering the sequence of data read from memory. It has several functions including:

- Control data direction of accessing memory
- Translate the parallel data to serial
- Generate output sync. timing
- Switch data sequence to meet delta and stripe type TFT LCD panel

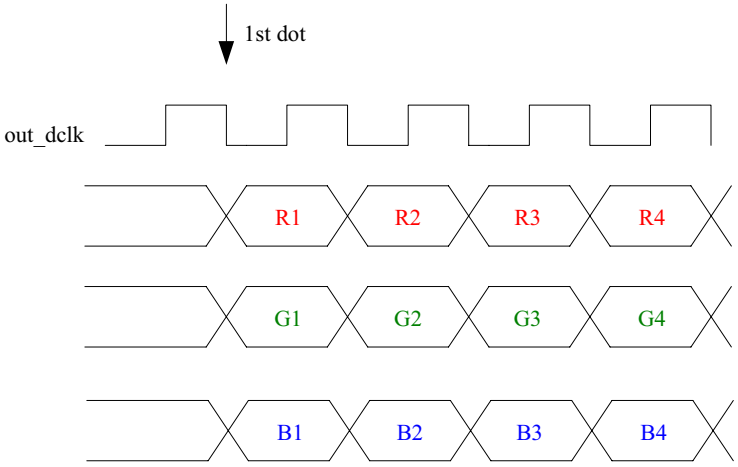
3.4.3 Output data for serial delta panel



3.4.4 Output data for serial stripe panel

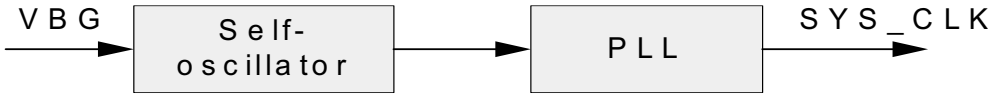


3.4.5 Output data for parallel panel

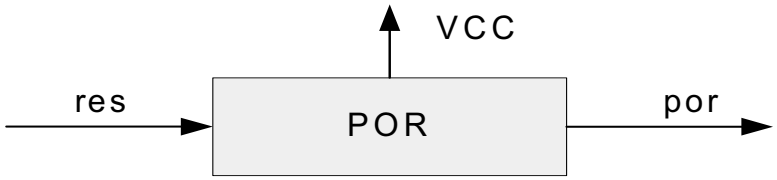


3.5 Internal oscillator & PLL

Generate 80MHz clock (SYS_CLK) to all system.

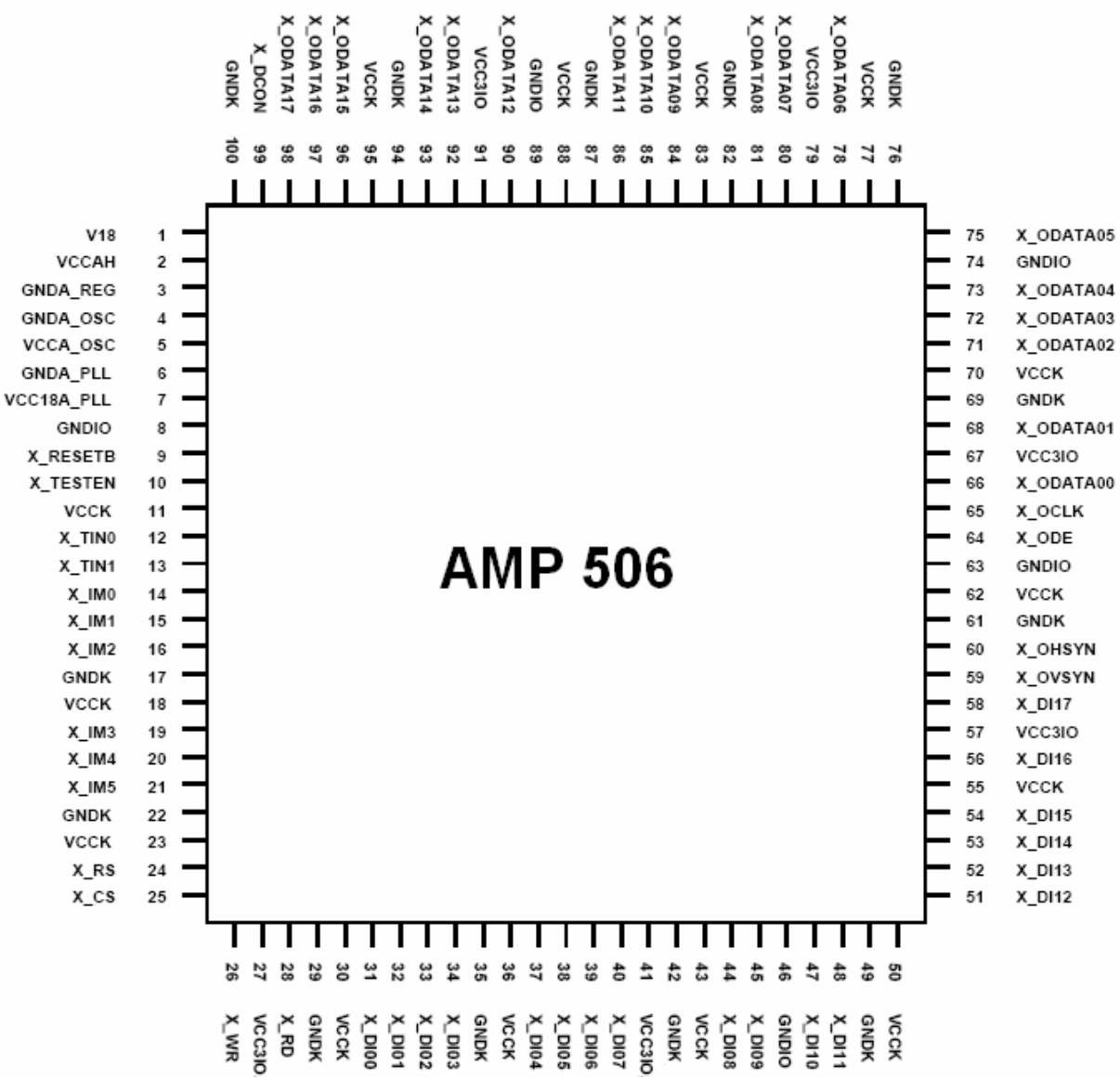


3.6 POR



3.7 Pin description

3.7.1 Pin assignment



3.7.2 Power supply

Pin-no	Symbol	I/O	Description	Remark
1	R_V18	P	Regulator 1.8V power out	
2	VCCAH	P	Regulator 3.3V power in	
3	GNDA_REG	P	Regulator ground	
4	GNDA_OSC	P	Oscillator ground	
5	GNDA_PLL	P	PLL ground	
6	VCC18V_PLL	P	PLL power in	
11, 18, 23, 30, 36, 43, 50, 55, 62, 70, 77, 83, 88, 95	VCCK	P	Core power	
17, 22, 29, 35, 42, 49, 61, 69, 76, 82, 87, 94, 100	GNDK	P	Core ground	
27, 41, 57, 67, 79, 91	VCCIO	P	Pad power	
8, 46, 63, 74, 89	GNDIO	P	Pad ground	

3.7.3 Output pin

Pin-no	Symbol	I/O	Description	Remark
59	X_VSYNC	O	V sync. output pin	
60	X_HSYNC	O	H sync. output pin	
64	X_ODE	O	Data enable output pin	
65	X_OCLK	O	Clock output pin	
66	DO00	O	Data output pin	
68	DO01	O		
71	DO02	O		
72	DO03	O		
73	DO04	O		
75	DO05	O		
78	DO06	O		
80	DO07	O		
81	DO08	O		
84	DO09	O		
85	DO10	O		
86	DO11	O		
90	DO12	O		
92	DO13	O		
93	DO14	O		
96	DO15	O		
97	DO16	O		
98	DO17	O		
99	DCON	O	DC/DC on/off pin	

3.7.4 Input pin

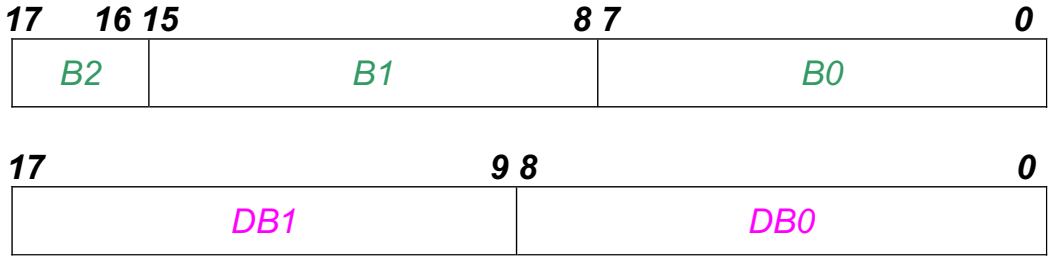
<table>
<tr><th>Pin-no</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>10</td><td>X_TESTEN</td><td>I</td><td>Test mode enable pin</td><td></td></tr>
<tr><td>12</td><td>X_TIN0</td><td>I</td><td>Test mode reserved</td><td></td></tr>
<tr><td>13</td><td>X_TIN1</td><td>I</td><td>Test mode reserved</td><td></td></tr>
<tr><td>14</td><td>X_IM0</td><td>I</td><td rowspan="8">Transport Interface selection
X_IM5: Data type
0: 16-bits data (565); 1: 18-bits data (666)
X_IM4: Data byte transfer order
0: LSB first; 1: MSB first
<table><tr><th colspan="4">X_IM[3:0]</th><th>MPU interface mode</th></tr><tr><td rowspan="8">0</td><td rowspan="4">0</td><td rowspan="2">0</td><td>0</td><td>80 mode 18-bit bus interface</td></tr><tr><td>1</td><td>80 mode 16-bit bus interface</td></tr><tr><td rowspan="2">1</td><td>0</td><td>80 mode 9-bit bus interface</td></tr><tr><td>1</td><td>80 mode 8-bit bus interface</td></tr><tr><td rowspan="4">1</td><td rowspan="2">0</td><td>0</td><td>68 mode 18-bit bus interface</td></tr><tr><td>1</td><td>68 mode 16-bit bus interface</td></tr><tr><td rowspan="2">1</td><td>0</td><td>68 mode 9-bit bus interface</td></tr><tr><td>1</td><td>68 mode 8-bit bus interface</td></tr></table></td><td></td></tr>
<tr><td>15</td><td>X_IM1</td><td>I</td><td></td></tr>
<tr><td>16</td><td>X_IM2</td><td>I</td><td></td></tr>
<tr><td>19</td><td>X_IM3</td><td>I</td><td></td></tr>
<tr><td>20</td><td>X_IM4</td><td>I</td><td></td></tr>
<tr><td>21</td><td>X_IM5</td><td>I</td><td></td></tr>
<tr><td>24</td><td>X_RS</td><td>I</td><td>Control signal</td><td></td></tr>
<tr><td>25</td><td>X_CS</td><td>I</td><td>Control signal</td><td></td></tr>
<tr><td>26</td><td>X_WR</td><td>I</td><td>Control signal</td><td></td></tr>
<tr><td>28</td><td>X_RD</td><td>I</td><td>Control signal</td><td></td></tr>
<tr><td>31</td><td>X_DI00</td><td>I/O</td><td rowspan="9">Data Input/output pin
<table><tr><th>X_IM[1:0]</th><th>Bus-type</th><th>Valid data bus</th></tr><tr><td>00</td><td>18 bits</td><td>X_DI17 - X_DI00</td></tr><tr><td>01</td><td>16 bits</td><td>X_DI15 - X_DI00</td></tr><tr><td>10</td><td>9 bits</td><td>X_DI08 - X_DI00</td></tr><tr><td>11</td><td>8 bits</td><td>X_DI07 - X_DI00</td></tr></table></td><td></td></tr>
<tr><td>32</td><td>X_DI01</td><td>I/O</td><td></td></tr>
<tr><td>33</td><td>X_DI02</td><td>I/O</td><td></td></tr>
<tr><td>34</td><td>X_DI03</td><td>I/O</td><td></td></tr>
<tr><td>37</td><td>X_DI04</td><td>I/O</td><td></td></tr>
<tr><td>38</td><td>X_DI05</td><td>I/O</td><td></td></tr>
<tr><td>39</td><td>X_DI06</td><td>I/O</td><td></td></tr>
<tr><td>40</td><td>X_DI07</td><td>I/O</td><td></td></tr>
</table>

Pin-no	Symbol	I/O	Description	Remark
44	X_DI08	I/O		
45	X_DI09	I/O		
47	X_DI10	I/O		
48	X_DI11	I/O		
51	X_DI12	I/O		
52	X_DI13	I/O		
53	X_DI14	I/O		
54	X_DI15	I/O		
56	X_DI16	I/O		
58	X_DI17	I/O		

4 General Description

4.1 Input data transfer order

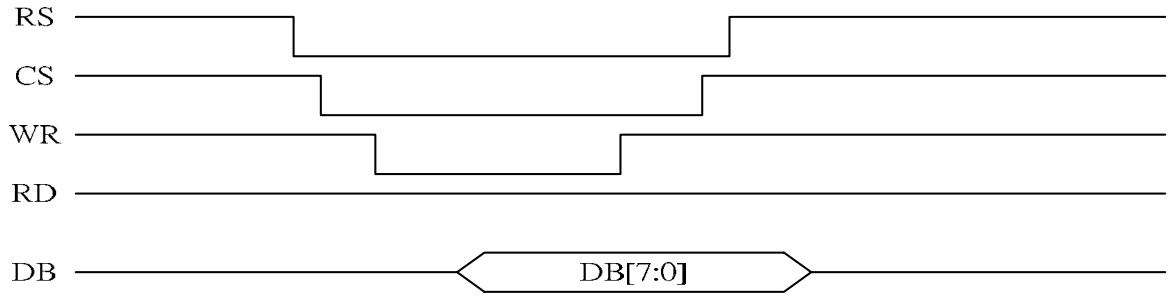
This chip supports four bus widths, 8/9/16/18, for transporting 16 (565) or 18 (666) bits data. In some setting mode of X_IM [5:0], data has to be segmented in several parts. Once transferring start, the following rule of order must be kept:



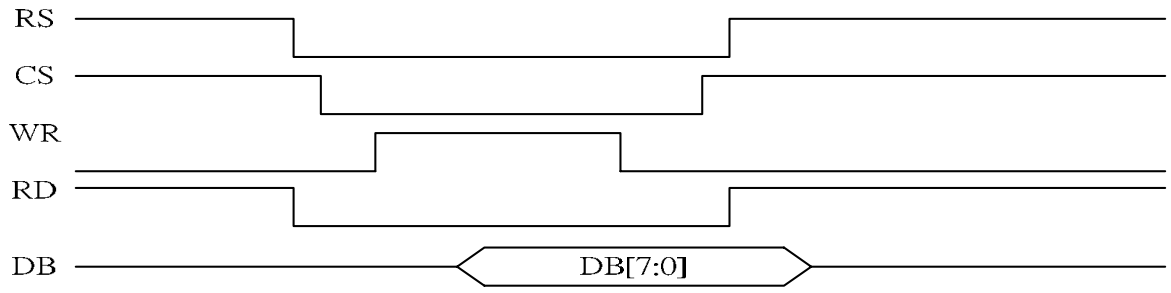
Bus type	X_IM [5] = 0 (16 bits)		X_IM [5] = 1 (18 bits)	
	X_IM [4] = 0	X_IM [4] = 1	X_IM [4] = 0	X_IM [4] = 1
8-bits	*B0 -> B1*	*B1 -> B0*	*B0 -> B1 -> B2*	*B2 -> B1 -> B0*
9-bits	Not allowed		*DB0 -> DB1*	*DB1 -> DB0*
16-bits	*(B1, B0)*		*(B1, B0) -> B2*	*B2 -> (B1, B0)*
18-bits	Not allowed		*(B2, B1, B0)*	

4.2 WRITE command format

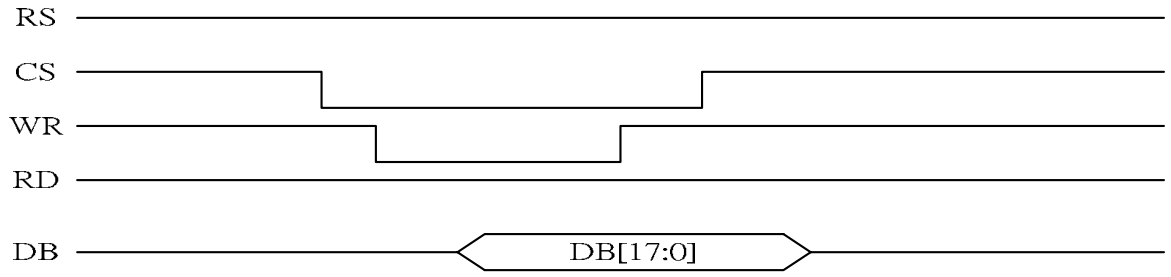
All commands have 8 bits width with each bit has its own definition. Through command issues, the coming data can be direct to register for system setting or memory for access. Following shows how to issues a command in both 80-series and 68-series mode



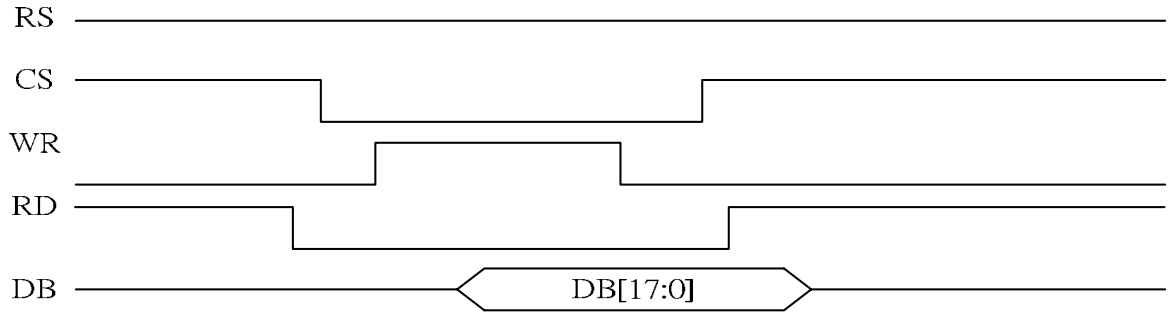
80-series mode issues a command



68-series mode issues a command



80-series mode writes a data



68-series mode writes a data

4.2.1 Register setting command format

7	6	0
0	Register Address	

EX: Write burst value 0 to 3 to register address from 7'h23 to 7'h26

command order	1st	2nd	3rd	4th	5th
command	*WC*	*WD*	*WD*	*WD*	*WD*
counting address		23	24	25	26
value	8'h23	8'h0	8'h1	8'h2	8'h3

where *WC* represents writes a command and *WD* represents writes a data

4.2.2 Memory write command format

7	6		0
1	Start	Reserved	MEM

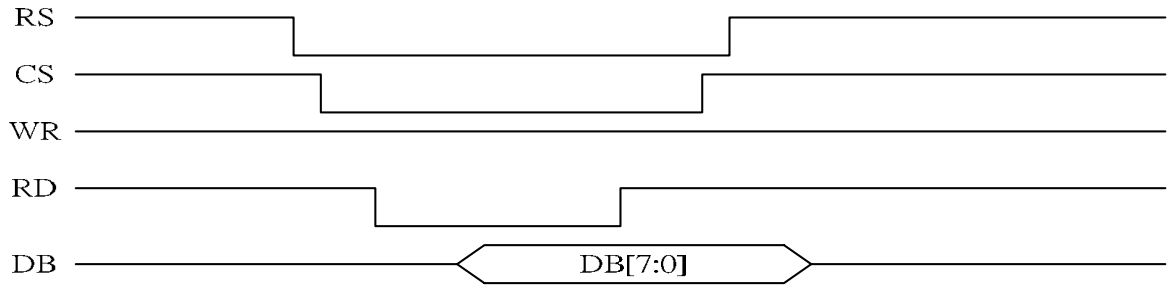
Start : memory access start bit
MEM: display memory selection

EX: Write burst value 0 to 3 to display area which has been defined in register

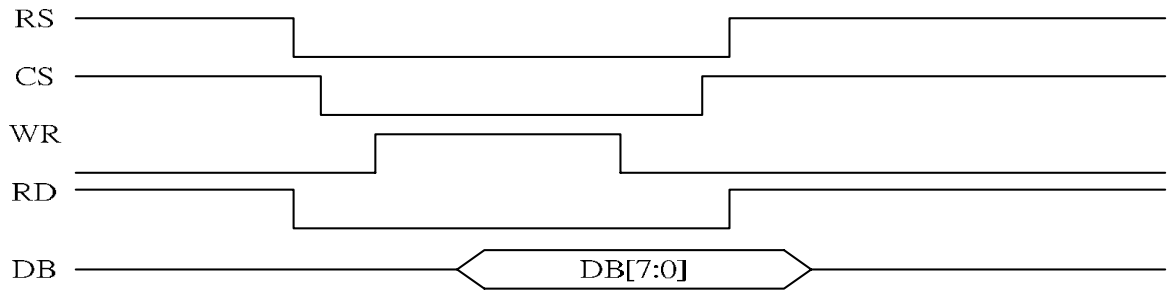
command order	1st	2nd	3rd	4th	5th
command	*WC*	*WD*	*WD*	*WD*	*WD*
counting address		addr1	addr2	addr3	addr4
value	8'hc1	8'h0	8'h1	8'h2	8'h3

4.3 READ command format

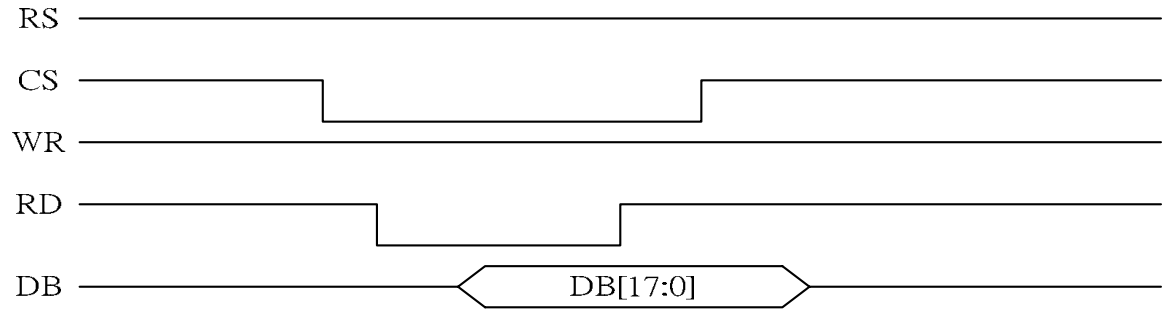
Register value and Memory data can be read out from the chip by issue read command show below:



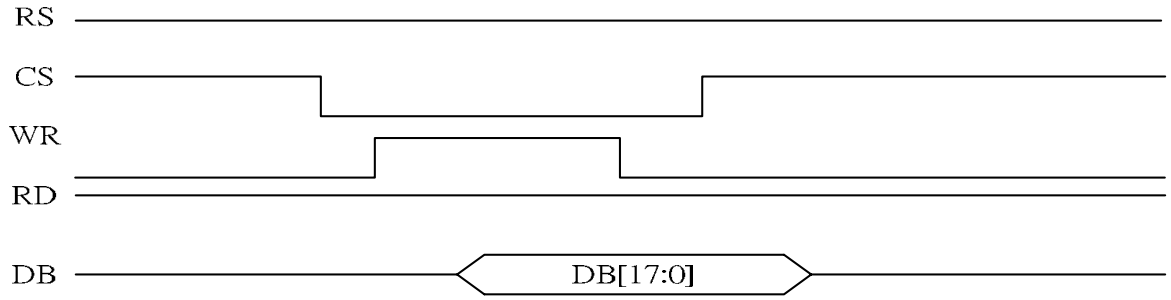
80-series mode reads a command



68-series mode reads a command



80-series mode reads a data



68-series mode reads a data

4.3.1 Read from register

Following example shows how to read value in burst from register

EX: read burst value from register address 7'h23 to 7'h26

command order	1st	2nd	3rd	4th	5th
command	*WC*	*RD*	*RD*	*RD*	*RD*
counting address		23	24	25	26
value	8'h23	8'h0	8'h1	8'h2	8'h3

where *RD* represents reads a data

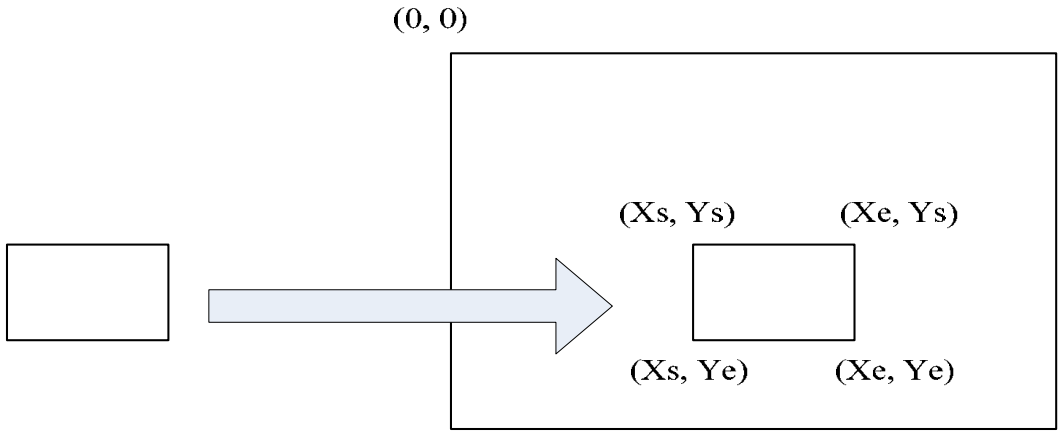
4.3.2 Read from internal memory

EX**:** read burst value from display area which has been defined in register

command order	1st	2nd	3rd	4th	5th
command	*WC*	*RD*	*RD*	*RD*	*RD*
counting address		addr1	addr2	addr3	addr4
value	8'hc1	8'h0	8'h1	8'h2	8'h3

4.4 Display control

All display areas such as panel visual period is treated as a coordinate image. Any image that smaller than or equal to this period can be transported and displayed in any place of this period which four vertexes coordinates defined.



5 Register Description

5.1 Register Setting

Address #00 Default: 00

Bit	Description
[7:0]	MSB of horizontal start coordinate value

Address #01 Default: 00

Bit	Description
[7:0]	LSB of horizontal start coordinate value

Address #02 Defaults: 01

Bit	Description
[7:0]	MSB of horizontal end coordinate value

Address #03 Defaults: 3F

Bit	Description
[7:0]	LSB of horizontal end coordinate value

Address #04 Defaults: 00

Bit	Description
[7:0]	MSB of vertical start coordinate value

Address #05 Defaults: 00

Bit	Description
[7:0]	LSB of vertical start coordinate value

Address #06 Defaults: 00

Bit	Description
[7:0]	MSB of vertical end coordinate value

Address #07 Defaults: EF

Bit	Description
[7:0]	LSB of vertical end coordinate value

Address #08 Defaults: 01

Bit	Description
[7:2]	Reserved
[1:0]	MSB of input image horizontal resolution

Address #09 Defaults: 40

Bit	Description
[7:0]	LSB of input image horizontal resolution

Address #0A Defaults: 00

Bit	Description
[7:2]	Reserved
[1:0]	[17:16] bits of memory write start address

Address #0B Defaults: 00

Bit	Description
[7:0]	[15:8] bits of memory write start address

Address #0C Defaults: 00

Bit	Description
[7:0]	[7:0] bits of memory write start address

Address #10 Defaults: 0D

Bit	Description
[7]	Output data bits swap 0: Normal 1:Swap
[6]	Output test mode enable 0: disable 1: enable
[5:4]	Serial mode data out bus selection 00: X_ODATA17 ~ X_ODATA12 active , others are set to zero 01: X_ODATA11 ~ X_ODATA06 active , others are set to zero 10: X_ODATA05 ~ X_ODATA00 active , others are set to zero 11: reserved
[3]	Output data blanking 0: set output data to 0 1: Normal display
[2]	Parallel or serial mode selection 0: serial data out 1: parallel data output

[1:0]	Output clock selection 00: system clock divided by 2 01: system clock divided by 4 10: system clock divided by 8 11: reserved

Address #11 Defaults: 00

Bit	Description
[7]	Reserved
[6:4]	Even line of serial panel data out sequence or data bus order of parallel panel 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved
[3]	Reversed
[2:0]	Odd line of serial panel data out sequence 000: RGB 001: RBG 010: GRB 011: GBR 100: BRG 101: BGR Others: reserved

Address #12 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output H sync. pulse start position

Address #13 Defaults: 00

Bit	Description
[7:0]	LSB of output H sync. pulse start position

Address #14 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output H sync. pulse width

Address #15 Defaults: 10

Bit	Description
[7:0]	LSB of output H sync. pulse width

Address #16 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output DE horizontal start position

Address #17 Defaults: 38

Bit	Description
[7:0]	LSB of output DE horizontal start position

Address #18 Defaults: 01

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output DE horizontal active region in pixel

Address #19 Defaults: 40

Bit	Description
[7:0]	LSB of output DE horizontal active region in pixel

Address #1a Defaults: 01

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output H total in pixel

Address #1b Defaults: B8

Bit	Description
[7:0]	LSB of output H total in pixel

Address #1C Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output V sync. pulse start position

Address #1D Default: 00

Bit	Description
[7:0]	LSB of output V sync. pulse start position

Address #1E Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output V sync. pulse width

Address #1F Defaults: 08

Bit	Description
[7:0]	LSB of output V sync. pulse width

Address #20 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output DE vertical start position

Address #21 Defaults: 12

Bit	Description
[7:0]	LSB of output DE vertical start position

Address #22 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of output DE vertical active region in line

Address #23 Defaults: F0

Bit	Description
[7:0]	LSB of output DE vertical active region in line

Address #24 Defaults: 01

Bit	Description
[7:4]	Reversed
[3:0]	MSB of output V total in line

Address #25 Defaults: 09

Bit	Description
[7:0]	LSB of output V total in line

Address #26 Defaults: 00

Bit	Description
[7:2]	Reserved
[1:0]	[17:16] bits of memory read start address

Address #27 Defaults: 00

Bit	Description
[7:0]	[15:8] bits of memory read start address

Address #28 Defaults: 00

Bit	Description
[7:0]	[7:0] bits of memory read start address

Address #29 Defaults: 00

Bit	Description
[7:1]	Reversed
[0]	Load output timing related setting (H sync., V sync. and DE) to take effect

Address #2a Defaults: 00

Bit	Description
[7:6]	Reserved
[5:0]	Output value setting R when output test mode enable (ref. register #10)

Address #2b Defaults: 00

Bit	Description
[7:6]	Reserved
[5:0]	Output value setting G when output test mode enable (ref. register #10)

Address #2c Defaults: 00

Bit	Description
[7:6]	Reserved
[5:0]	Output value setting B when output test mode enable (ref. register #10)

Address #2d Defaults: 00

Bit	Description
[7:4]	Reserved
[3]	Output pin X_DCON level control
[2]	Output clock inversion 0: Normal 1: Inverse
[1:0]	Image rotate 00: 0° 01: 90° 10: 270° 11: 180°

Address #30 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of image horizontal shift value

Address #31 Defaults: 00

Bit	Description
[7:0]	LSB of image horizontal shift value

Address #32 Defaults: 00

Bit	Description
[7:4]	Reserved
[3:0]	MSB of image vertical shift value

Address #33 Defaults: 00

Bit	Description
[7:0]	LSB of image vertical shift value

Address #34 Defaults: 01

Bit	Description
[7:4]	Reserved
[3:0]	MSB of image horizontal physical resolution in memory

Address #35 Defaults: 40

Bit	Description
[7:0]	LSB of image horizontal physical resolution in memory

Address #36 Defaults: 01

Bit	Description
[7:4]	Reserved
[3:0]	MSB of image vertical physical resolution in memory

Address #37 Defaults: E0

Bit	Description
[7:0]	LSB of image vertical physical resolution in memory

Address #40 Defaults: 12

Bit	Description
[7:6]	Reserved
[5]	PLL control pins to select out frequency range 0: 20MHz ~ 100MHz 1: 100MHz ~ 300MHz
[4]	Reserved
[3]	Reserved
[2:1]	Output Driving Capability 00: 4mA 01: 8mA 10: 12mA 11: 16mA
[0]	Output slew rate 0: Fast 1: Slow

Address #41 Defaults: 01

Bit	Description
[7:6]	Reserved
[5:0]	PLL Programmable pre-divider, 6bit(1~63)

Address #42 Defaults: 02

Bit	Description
[7:6]	Reserved
[5:0]	PLL Programmable loop divider, 6bit(1~63)

6 Electrical Specification

6.1 DC characteristics

DC Characteristics of 3.3V with 5V Tolerance I/O Cells

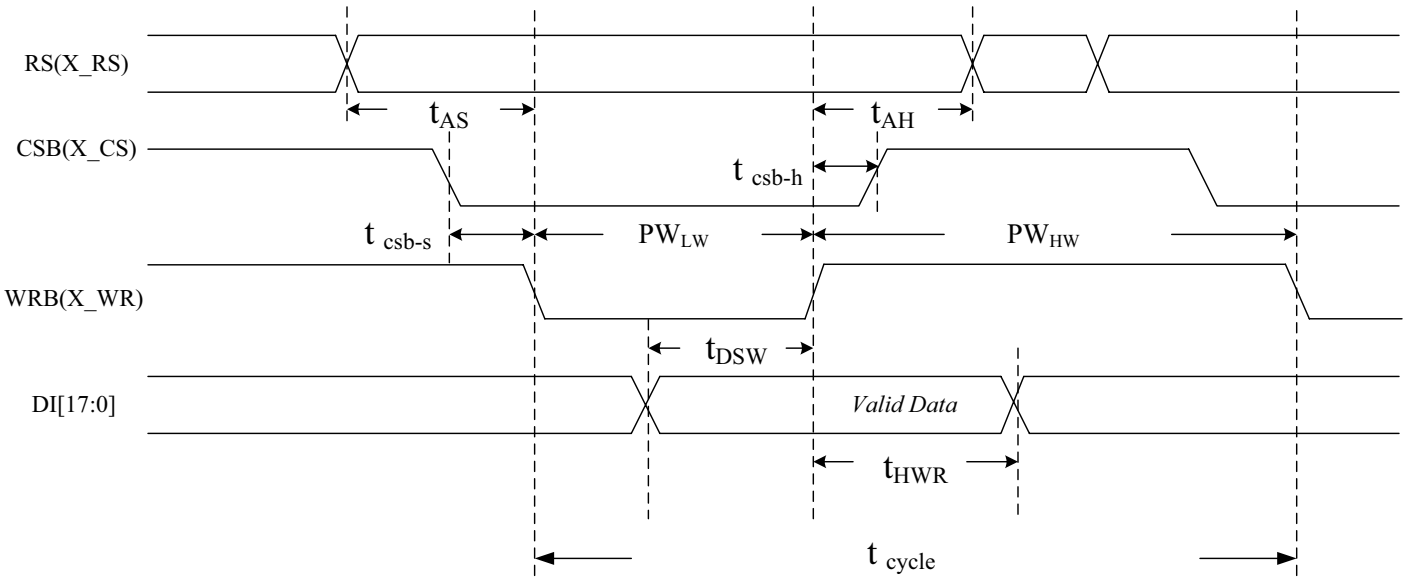
Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCCK	Core power supply	Core area	1.62	1.8	1.98	V
VCC3I	Power supply	3.3V I/O	2.97	3.3	3.63	V
VCC3O	Power supply		2.97	3.3	3.63	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	LVTTL			0.8	V
Vih	Input high voltage		2.0			V
Vt	Switching threshold	LVTTL	1.5	V		
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1		V
Vt+	Schmitt trigger positive going threshold voltage			1.6	2.0	V
Vol	Output low voltage	Iol = 2 ~ 16 mA			0.4	V
Voh	Output high voltage	Ioh = -2 ~ -16 mA	2.4			V
Rpu	Input pull-up resistance	Vin = 0	40	75	190	KΩ
Rpd	Input pull-down resistance	Vin = VCC3I	40	75	190	KΩ
Iin	Input leakage current	Vin = 5.5V or 0		±5		uA
	Input leakage current with pull-up resistance	Vin = 0	-15	-45	-85	uA
	Input leakage current with pull-down resistance	Vin = VCC3I	15	45	85	uA
Ioz	Tri-state output leakage current	Vin = 5.5V or 0		±10		uA

6.2 AC characteristics

6.2.1 80-series AC timing table

Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{HW}	Enable high-level pulse width	66	70		ns	
PW_{LW}	Enable low-level pulse width	33	130		ns	
t_{AS}	RS setup time	16	25		ns	
t_{AH}	RS hold time	16	45		ns	
t_{DSW}	Write data setup time	50	50		ns	
t_{HWR}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

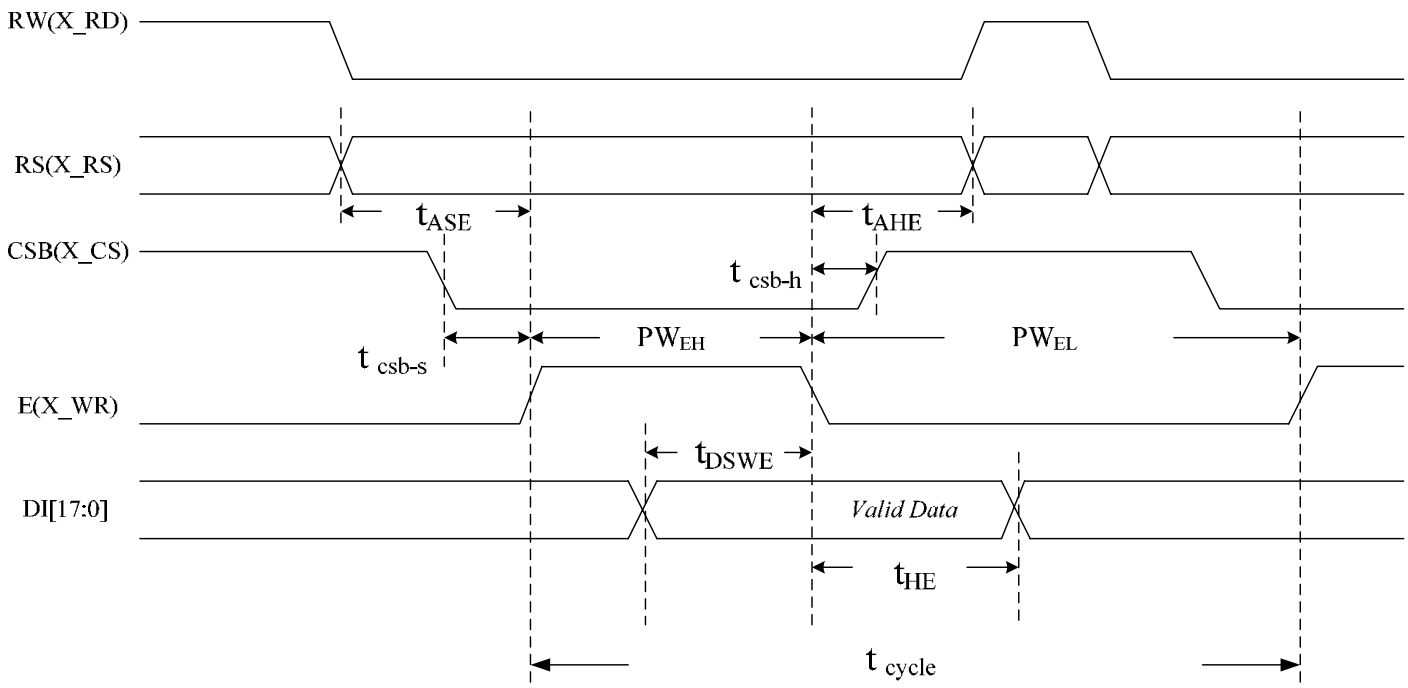
6.2.2 80-series AC timing chart



6.2.3 68-series AC timing table

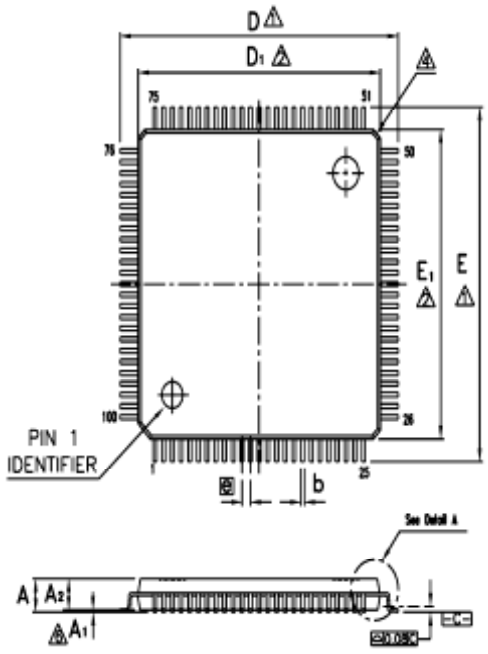
Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{cycle}	Enable cycle time	100	200		ns	
PW_{EH}	Enable high-level pulse width	33	70		ns	
PW_{EL}	Enable low-level pulse width	66	130		ns	
t_{ASE}	RS setup time	16	25		ns	
t_{AHE}	RS hold time	16	45		ns	
t_{DSWE}	Write data setup time	50	50		ns	
t_{HE}	Write data hold time	50	40		ns	
t_{csb-s}	CSB setup time	16	20		ns	
t_{csb-h}	CSB hold time	16	30		ns	

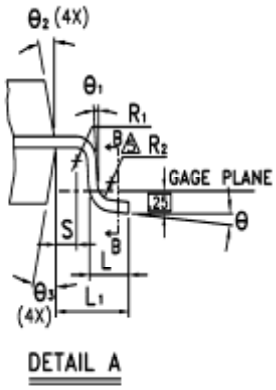
6.2.4 68-series AC timing chart



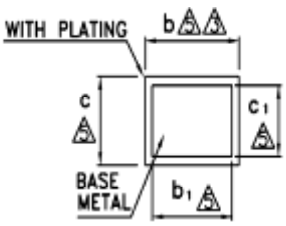
7 Package Outline

LQFP 100





DETAIL A



SECTION B-B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BED.

TITLE: 100LD LQFP(14x14x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm

L/F MATERIAL: C7025 1/2H

APPR.			D100-SW2
R&D		REV NO.	D
Q.M		SCALE	
CHK.		DATE	JAN 18,'97
DEN.	J.F.C	SHT NO.	1/1

REV NO	DESCRIPTION	DATE
D	Follow JEDEC SPEC dimension.	Jan,18'97
C	1. Update form. 2. A1 ,b,D,E,L Modify.	Jul,01'94
B	Leadframe material modify	Jan,18'94

COPY CONTROLLED