RAM Mapping 32×4 LCD Controller for I/O μC

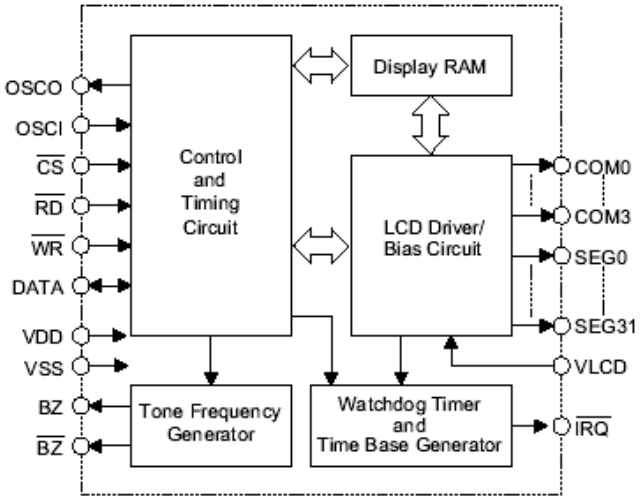
General Description

The AIP31621 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the AIP31621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only three or four lines are required for the interface between the host controller and the AIP31621. The AIP31621 contains a power down command to reduce power consumption.

Features

- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage

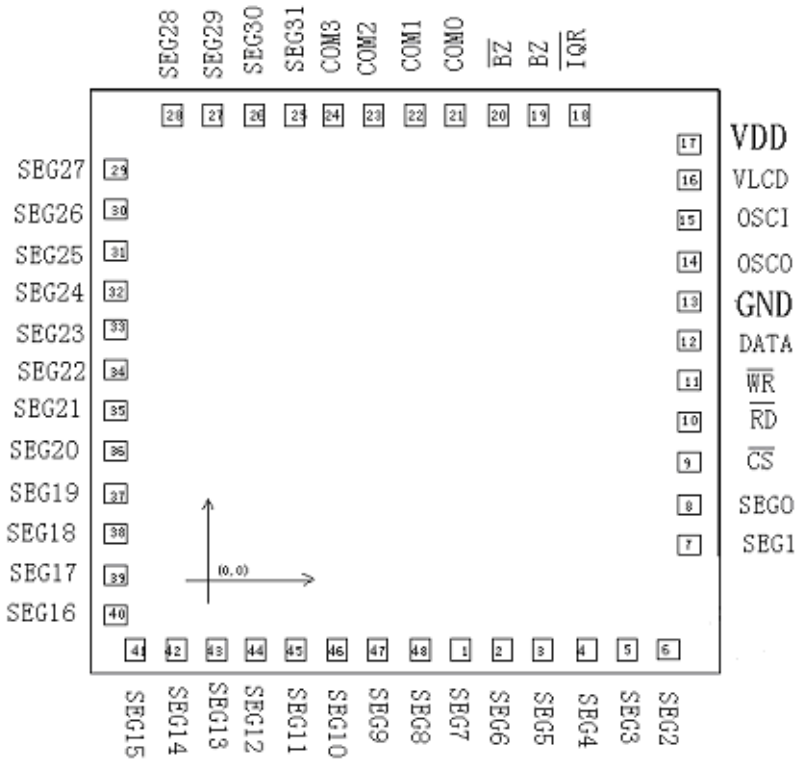
Block Diagram



Note: CS: Chip selection
BZ, BZ: Tone outputs
WR, RD, DATA: Serial interface
COM0~COM3, SEG0~SEG31: LCD outputs
IRQ: Time base or WDT overflow output

Pin Assignment

Pad Coordinates



chip size: （2.095mm*1.980mm）

The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

NO.	Name	Coordinate	NO.	Name	Coordinate
1	SEG<7>	(1126.10，64.00)	25	SEG<31>	(497.35，1803.10)
2	SEG<6>	(1246.10，64.00)	26	SEG<30>	(377.35，1803.10)
3	SEG<5>	(1366.10，64.00)	27	SEG<29>	(257.35，1803.10)
4	SEG<4>	(1486.10，64.00)	28	SEG<28>	(137.35，1803.10)
5	SEG<3>	(1606.10，64.00)	29	SEG<27>	(64.00，1580.00)
6	SEG<2>	(1726.10，64.00)	30	SEG<26>	(64.00，1460.00)
7	SEG<1>	(1916.20，166.35)	31	SEG<25>	(64.00，1340.00)
8	SEG<0>	(1916.20，286.40)	32	SEG<24>	(64.00，1220.00)
9	NCS	(1916.20，406.40)	33	SEG<23>	(64.00，1100.00)
10	NRD	(1916.20，526.40)	34	SEG<22>	(64.00，980.00)
11	NWR	(1916.20，780.55)	35	SEG<21>	(64.00，860.00)
12	DATA	(1916.20，952.10)	36	SEG<20>	(64.00，740.00)
13	GND	(1916.20，1113.65)	37	SEG<19>	(64.00，620.00)
14	OSCO	(1916.20，1233.65)	38	SEG<18>	(64.00，500.00)
15	OSCI	(1916.20，1487.75)	39	SEG<17>	(64.00，380.00)
16	VLCD	(1916.20，1608.30)	40	SEG<16>	(64.00，260.00)
17	VDD	(1916.20，1800.10)	41	SEG<15>	(166.10，64.00)
18	NIRQ	(1446.55，1803.10)	42	SEG<14>	(286.10，64.00)
19	BZ	(1271.65，1803.10)	43	SEG<13>	(406.10，64.00)
20	BZN	(1151.65，1803.10)	44	SEG<12>	(526.10，64.00)
21	COM<0>	(617.35，1803.10)	45	SEG<11>	(646.10，64.00)
22	COM<1>	(737.35，1803.10)	46	SEG<10>	(766.10，64.00)
23	COM<2>	(857.35，1803.10)	47	SEG<9>	(886.10，64.00)
24	COM<3>	(977.35，1803.10)	48	SEG<8>	(1006.10，64.00)

Pad Description

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the AIP31621 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the AIP31621 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the AIP31621 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the AIP31621 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	VSS	-	Negative power supply, ground
6	OSCO	O	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
7	OSCI	I	
8	VLCD	I	LCD power input
9	VDD	-	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11,12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
13～16	COM0~COM3	O	LCD common outputs
48～17	SEG0~SEG31	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage .....……VSS-0.3V to VSS+5.5V
Storage Temperature.....…-50℃ to 125℃
Input Voltage.....……VSS-0.3V to VDD+0.3V
Operating Temperature.....-25℃ to 75℃
Note: These are stress ratings only. Stresses exceeding the range specified under Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	—	5.2	V
I_{DD1}	Operating Current	3V	No load/LCD ON On-chip RC oscillator	—	150	300	μA
		5V		—	300	600	μA
I_{DD2}	Operating Current	3V	No load/LCD ON Crystal oscillator	—	60	120	μA
		5V		—	120	240	μA
I_{DD3}	Operating Current	3V	No load/LCD ON External clock source	—	100	200	μA
		5V		—	200	400	μA
I_{STB}	Standby Current	3V	No load Power down mode	—	0.1	5	μA
		5V		—	0.3	10	μA
V_{IL}	Input Low Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V_{IH}	Input High Voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I_{OL1}	DATA, BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.5	1.2	—	mA
		5V	V_{OL}=0.5V	1.3	2.6	—	mA
I_{OH1}	DATA, BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	–0.4	–0.8	—	mA
		5V	V_{OH}=4.5V	–0.9	–1.8	—	mA
I_{OL2}	LCD Common Sink Current	3V	V_{OL}=0.3V	80	150	—	μA
		5V	V_{OL}=0.5V	150	250	—	μA
I_{OH2}	LCD Common Source Current	3V	V_{OH}=2.7V	–80	–120	—	μA
		5V	V_{OH}=4.5V	–120	–200	—	μA
I_{OL3}	LCD Segment Sink Current	3V	V_{OL}=0.3V	60	120	—	μA
		5V	V_{OL}=0.5V	120	200	—	μA
I_{OH3}	LCD Segment Source Current	3V	V_{OH}=2.7V	–40	–70	—	μA
		5V	V_{OH}=4.5V	–70	–100	—	μA
R_{PH}	Pull-high Resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	40	80	150	kΩ
		5V		30	60	100	kΩ

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On-chip RC oscillator	—	256	—	kHz
		5V		—	256	—	kHz
f_{SYS2}	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f_{SYS3}	System Clock	3V	External clock source	—	256	—	kHz
		5V		—	256	—	kHz
f_{LCD}	LCD Clock	—	On-chip RC oscillator	—	f_{SYS1}/1024	—	Hz
		—	Crystal oscillator	—	f_{SYS2}/128	—	Hz
		—	External clock source	—	f_{SYS3}/1024	—	Hz
t_{COM}	LCD Common Period	—	n: Number of COM	—	n/f_{LCD}	—	s
f_{CLK1}	Serial Data Clock ($\overline{WR}$ pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
f_{TONE}	Tone Frequency	—	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t_{CS}	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	—	µs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	—	µs
			Read mode	3.34	—	—	
t_r, t_f	Rise/Fall Time Serial Data Clock Width (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time for DATA to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 2)	3V	—	—	120	—	ns
		5V					
t_{su1}	Setup Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{h1}	Hold Time for $\overline{CS}$ to $\overline{WR}$, $\overline{RD}$ Clock Width (Figure 3)	3V	—	—	100	—	ns
		5V					

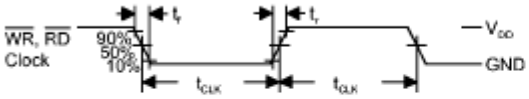


Figure 1

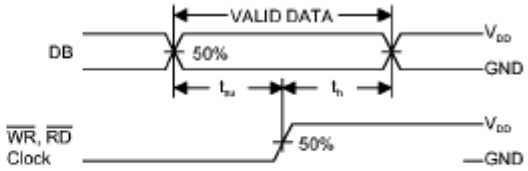


Figure 2

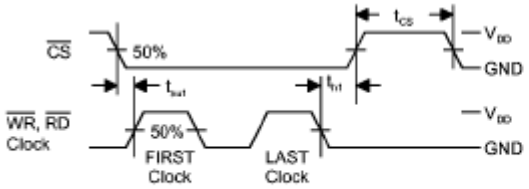
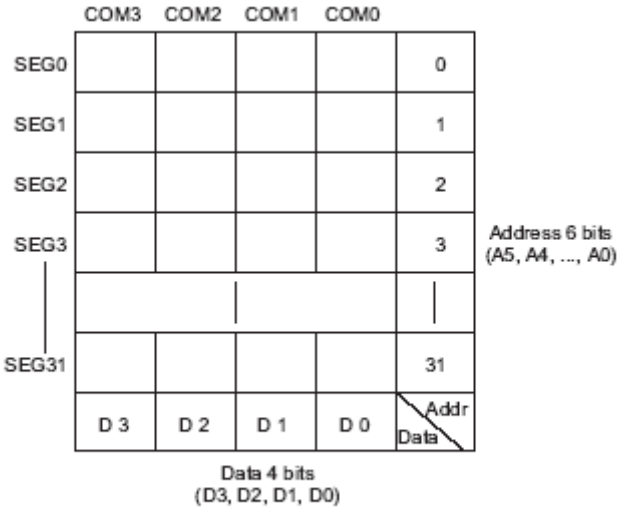


Figure 3

Functional Description

Display Memory -RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



RAM Mapping

System Oscillator

The AIP31621 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the AIP31621 is at the SYS DIS state.

Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the $\overline{IRQ}$ output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{WDT} = \frac{32KHz}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz. If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default pre-scaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the $\overline{IRQ}$ pin). After the TIMER EN command is transferred, the WDT is disconnected from the $\overline{IRQ}$ pin, and the output of the time base generator is connected to the $\overline{IRQ}$ pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator is cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to the WDT EN or the TIMER EN command respectively. Before executing the $\overline{IRQ}$ EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued. After the $\overline{IRQ}$ output is disabled the $\overline{IRQ}$ pin will remain at the floating state. The $\overline{IRQ}$ output can be enabled or disabled by executing the $\overline{IRQ}$ EN

or the $\overline{IRQ}$ DIS command, respectively. The $\overline{IRQ}$ EN makes the output of the time base generator or of the WDT time-out flag appear on the $\overline{IRQ}$ pin. The configuration of the time $\overline{IRQ}$ base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions. On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the AIP31621 will continue working until system power fails or the external clock source is removed. After the system power on, the $\overline{IRQ}$ will be disabled.

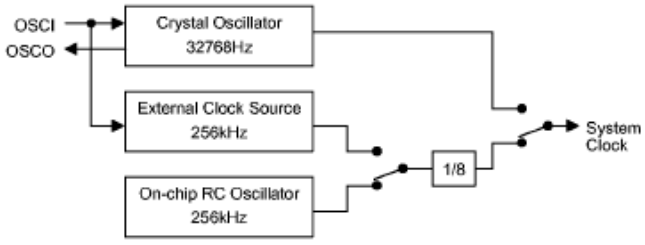
Tone Output

A simple tone generator is implemented in the AIP31621. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$, which are used to generate a single tone. By executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and $\overline{BZ}$, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the $\overline{BZ}$ outputs will remain at low level.

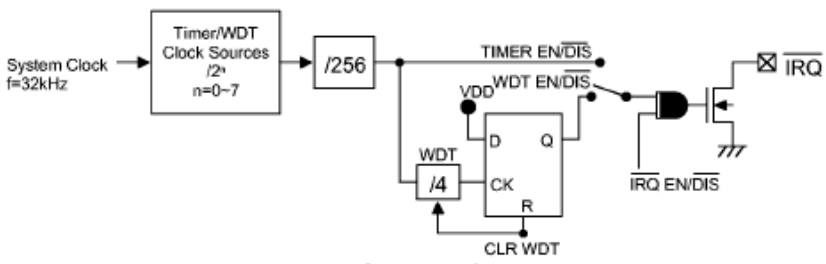
LCD Driver

The AIP31621 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the AIP31621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the AIP31621 can be compatible with most types of LCD panels.



System oscillator configuration



Timer and WDT configurations

Name	Command Code	Function
LCD OFF	**100** 00000010X	Turn off LCD outputs
LCD ON	**100** 00000011X	Turn on LCD outputs
BIAS & COM	**100** 0010abXcX	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

Command Format

The AIP31621 can be configured by the S/W setting. There are two mode commands to configure the AIP31621 resources and to transfer the LCD display data. The configuration mode of the AIP31621 is called command mode, and its command mode ID is 100. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

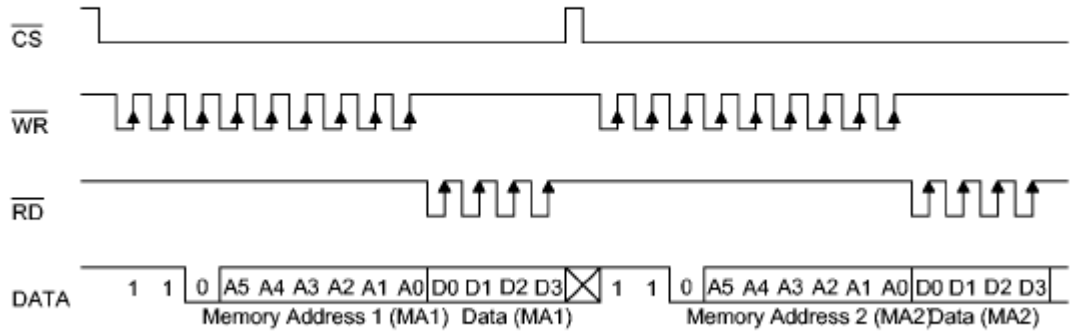
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely 1 0 0, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to " 1 " and the previous operation mode will be reset also. Once the $\overline{CS}$ pin returns to "0" a new operation mode ID should be issued first.

Interfacing

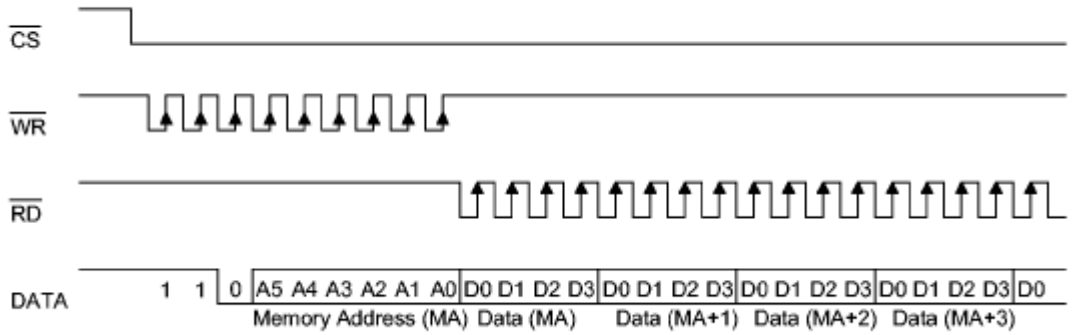
Only four lines are required to interface with the AIP31621. The $\overline{CS}$ line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the AIP31621. If the $\overline{CS}$ pin is set to 1, the data and command issued between the host controller and the AIP31621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the AIP31621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The $\overline{RD}$ line is the READ clock input. Data in the RAM are clocked out on the falling edge of the $\overline{RD}$ signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the $\overline{RD}$ signal. The $\overline{WR}$ line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the AIP31621 on the rising edge of the $\overline{WR}$ signal. There is an optional $\overline{IRQ}$ line to be used as an interface between the host controller and the AIP31621. The $\overline{IRQ}$ pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the $\overline{IRQ}$ pin of the AIP31621.

Timing Diagrams

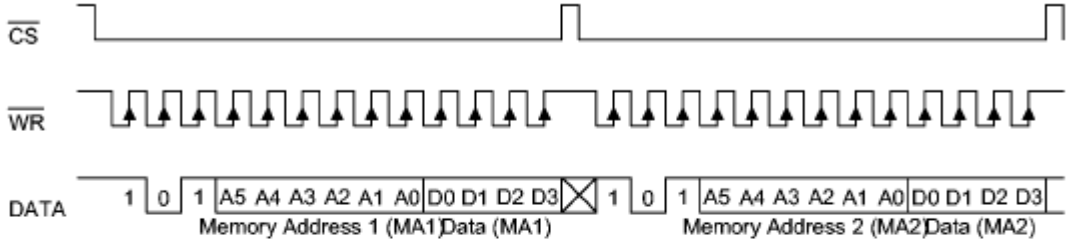
READ mode (command code : 1 1 0)



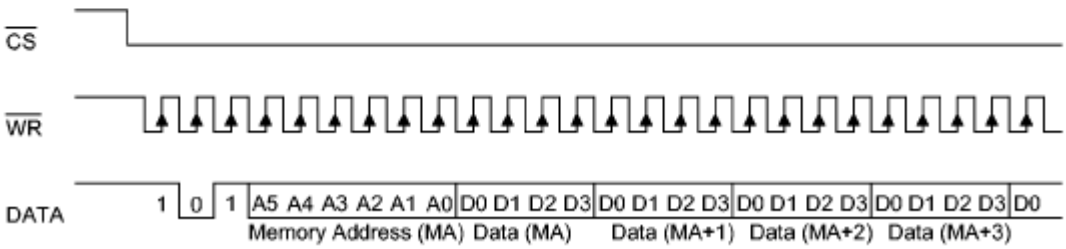
READ mode (successive address reading)



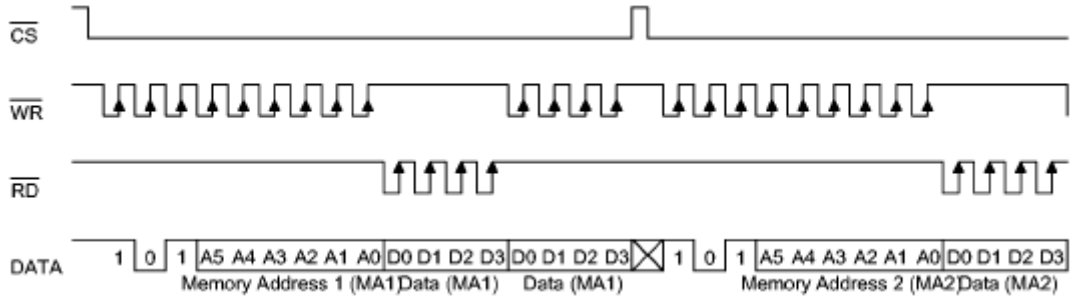
WRITE mode (command code : 1 0 1)



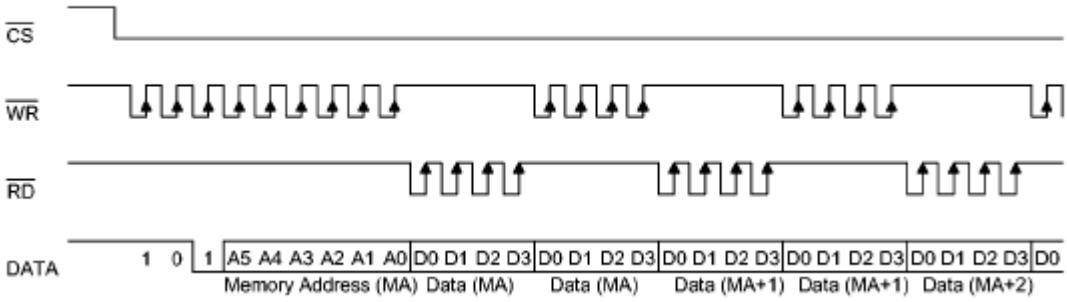
WRITE mode (successive address writing)



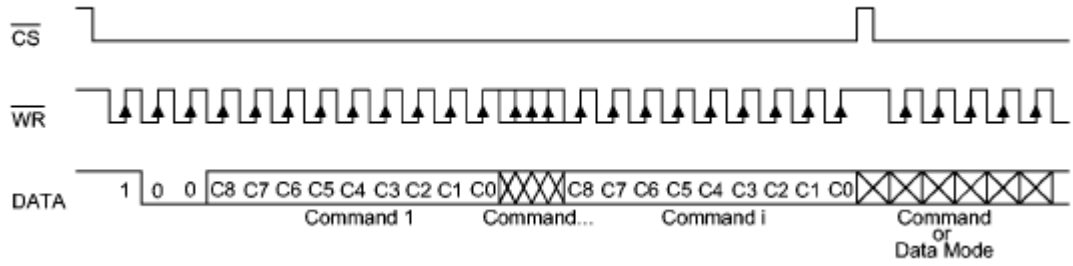
READ-MODIFY-WRITE mode (command code : 1 0 1)



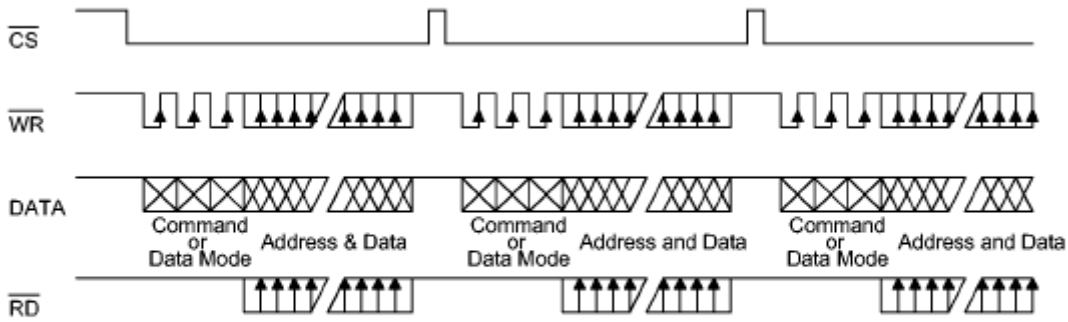
READ-MODIFY-WRITE mode (successive address accessing)



Command mode (command code : 1 0 0)



Mode (data and command mode)



Note: It is recommended that the host controller should read in the data from the DATA line between the rising edge of the $\overline{RD}$ line and the falling edge of the next $\overline{RD}$ line.

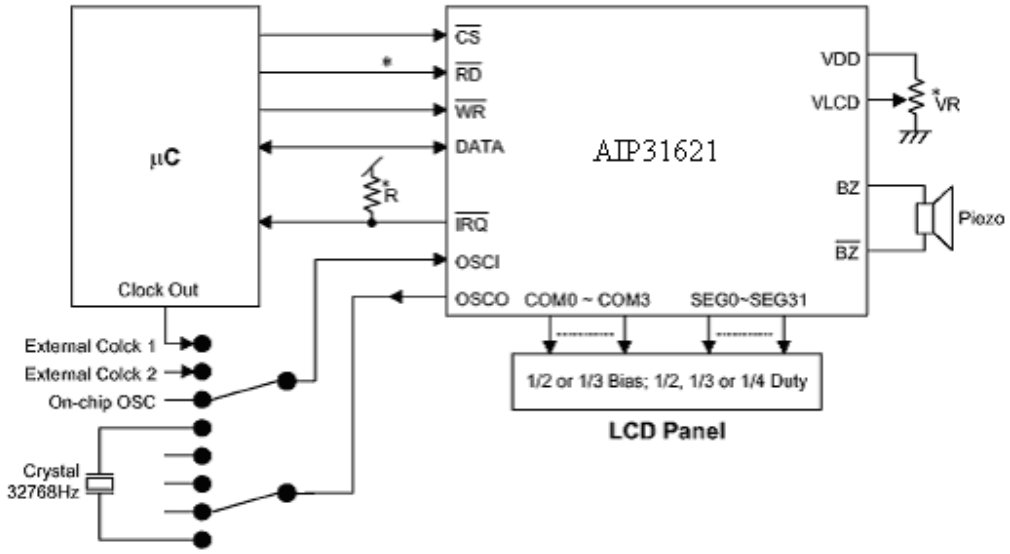
Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	1 0 0	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	1 0 0	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	1 0 0	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	1 0 0	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	1 0 0	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	1 0 0	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	1 0 0	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	1 0 0	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	1 0 0	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	1 0 0	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	1 0 0	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes

Name	ID	Command Code	D/C	Function	Def.
$\overline{IRQ}$ EN	**1 0 0**	100X-1XXX-X	C	Enable $\overline{IRQ}$ output	
F1	**1 0 0**	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	**1 0 0**	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	**1 0 0**	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	**1 0 0**	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2 s	
F16	**1 0 0**	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4 s	
F32	**1 0 0**	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8 s	
F64	**1 0 0**	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16 s	
F128	**1 0 0**	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32 s	Yes
TEST	**1 0 0**	1110-0000-X	C	Test mode, user don't use.	
NORMAL	**1 0 0**	1110-0011-X	C	Normal mode	Yes

Application Circuits

Host Controller with an AIP31621 Display System



Note: The connection of $\overline{IRQ}$ and $\overline{RD}$ RD pin can be selected depending on the requirement of the µC

The voltage applied to V_{LCD} pin must be lower than V_{DD}.

Adjust VR to fit LCD display, at V_{DD}=5V, V_{LCD}=4V, VR=15k_20%.

Adjust R (external pull-high resistance) to fit user's time base clock.

Package Information（SSOP48-300-0.6）

Dimensions / Symbol	Min.(mm)	Max.(mm)	Dimensions / Symbol	Min.(mm)	Max.(mm)
A	15.77	15.97	C3	0.2	0.4
A1	0.20	0.35	C4	0.12	0.25
A2	0.635TYP		D	1.41TYP	
A3	0.5TYP		D1	0.61	0.91
A4	10.2TYP		h	0.381	0.635
B	10.01	10.61	φ1	2.2TYP	
B1	7.39	7.59	θ1	15° TYP	
B2	8.6TYP		θ2	15° TYP	
C	2.41	2.78	θ3	4° TYP	
C1	2.18	2.38	θ4	8° TYP	
C2	1.067TYP