APPENDIX SUMMARY

Reference	Item
APPENDIX I	SSD1357Z Die Pad Floor Plan
APPENDIX II	SSD1357 Bump Die Pad Coordinates
APPENDIX III	SSD1357 Command Table and Command Description

Appendix I: SSD1357Z Die Pad Floor Plan

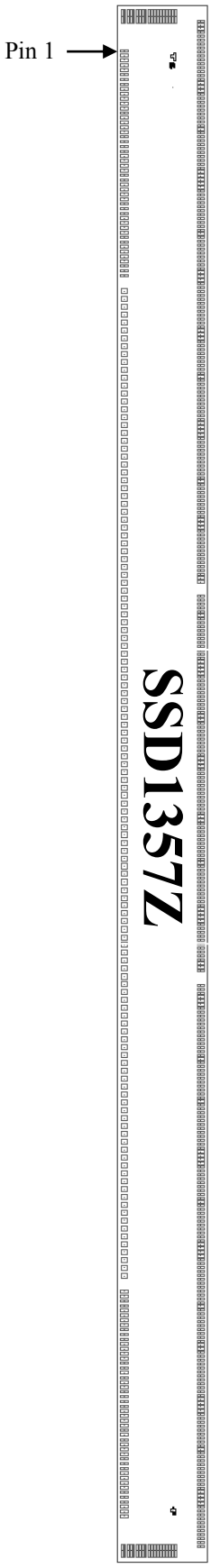


Figure 1-1: – SSD1357Z Die drawing

Die size	10.90 mm +/- 0.05mm x 1.01 mm+/- 0.05mm
Die thickness	250 +/- 15um
Min I/O pad pitch	55um
Min SEG pad pitch	27um
Min COM pad pitch	33.4um
Bump height	Nominal 12 um

Bump size		
Pad#	X[um]	Y[um]
1~48, 175~222	18	90
223~241, 632~650	90	18
49~174	35	67
242~631	15	80

Alignment mark	Position	Size
+ shape	(5077.5, 112.5)	56.25um x 56.25um
T shape	(-5077.5, 112.5)	56.25um x 56.25um

Error!

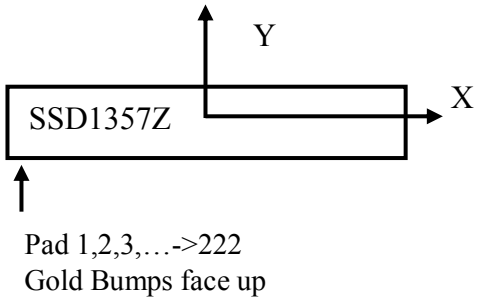
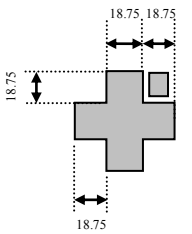
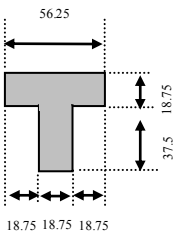


Figure 1-2: SSD1357Z alignment mark dimension



Center: (5077.5, 112.5)
Size: 56.25 x 56.25 m^2



Center: (-5077.5, 112.5)
Size: 56.25 x 56.25 m^2

Appendix II: SSD1357 Bump Die Pad Coordinates

Table 1 : SSD1357 Bump Die Pad Coordinates

Pin Number	Pin Name	X	Y
1	VLSS	-5116.8	-425.9
2	COM82	-5083.4	-425.9
3	COM83	-5050	-425.9
4	COM84	-5016.6	-425.9
5	COM85	-4983.2	-425.9
6	COM86	-4949.8	-425.9
7	COM87	-4916.4	-425.9
8	COM88	-4883	-425.9
9	COM89	-4849.6	-425.9
10	COM90	-4816.2	-425.9
11	COM91	-4782.8	-425.9
12	COM92	-4749.4	-425.9
13	COM93	-4716	-425.9
14	COM94	-4682.6	-425.9
15	COM95	-4649.2	-425.9
16	COM96	-4615.8	-425.9
17	COM97	-4582.4	-425.9
18	COM98	-4549	-425.9
19	COM99	-4515.6	-425.9
20	COM100	-4482.2	-425.9
21	COM101	-4448.8	-425.9
22	COM102	-4415.4	-425.9
23	COM103	-4382	-425.9
24	COM104	-4348.6	-425.9
25	COM105	-4315.2	-425.9
26	COM106	-4281.8	-425.9
27	COM107	-4248.4	-425.9
28	COM108	-4215	-425.9
29	COM109	-4181.6	-425.9
30	COM110	-4148.2	-425.9
31	COM111	-4114.8	-425.9
32	COM112	-4081.4	-425.9
33	COM113	-4048	-425.9
34	COM114	-4014.6	-425.9
35	COM115	-3981.2	-425.9
36	COM116	-3947.8	-425.9
37	COM117	-3914.4	-425.9
38	COM118	-3881	-425.9
39	COM119	-3847.6	-425.9
40	COM120	-3814.2	-425.9
41	COM121	-3780.8	-425.9
42	COM122	-3747.4	-425.9
43	COM123	-3714	-425.9
44	COM124	-3680.6	-425.9
45	COM125	-3647.2	-425.9
46	COM126	-3613.8	-425.9
47	COM127	-3580.4	-425.9
48	NC	-3547	-425.9
49	NC	-3437.5	-424.5
50	NC	-3382.5	-424.5
51	NC	-3327.5	-424.5
52	NC	-3272.5	-424.5
53	NC	-3217.5	-424.5
54	NC	-3162.5	-424.5
55	NC	-3107.5	-424.5
56	NC	-3052.5	-424.5
57	NC	-2997.5	-424.5
58	NC	-2942.5	-424.5
59	NC	-2887.5	-424.5
60	NC	-2832.5	-424.5
61	NC	-2777.5	-424.5
62	NC	-2722.5	-424.5
63	VLSS	-2667.5	-424.5
64	VLSS	-2612.5	-424.5
65	VLSS	-2557.5	-424.5
66	VLSS	-2502.5	-424.5
67	VSL	-2447.5	-424.5
68	VSL	-2392.5	-424.5
69	VSL	-2337.5	-424.5
70	VCOMH	-2282.5	-424.5
71	VCOMH	-2227.5	-424.5
72	VCOMH	-2172.5	-424.5
73	VCOMH	-2117.5	-424.5
74	VCOMH	-2062.5	-424.5
75	VCOMH	-2007.5	-424.5
76	VP	-1952.5	-424.5
77	VP	-1897.5	-424.5
78	VP	-1842.5	-424.5
79	VP	-1787.5	-424.5
80	VP	-1732.5	-424.5
81	VCC	-1677.5	-424.5
82	VCC	-1622.5	-424.5
83	VCC	-1567.5	-424.5
84	VCC	-1512.5	-424.5
85	IREF	-1457.5	-424.5
86	T0	-1402.5	-424.5
87	T1	-1347.5	-424.5
88	VSS	-1292.5	-424.5
89	VSS	-1237.5	-424.5
90	BGGND	-1182.5	-424.5
91	VBREF	-1127.5	-424.5
92	VDD	-1072.5	-424.5
93	VDD	-1017.5	-424.5
94	VDD	-962.5	-424.5
95	VDD	-907.5	-424.5
96	FR	-852.5	-424.5
97	CL	-797.5	-424.5
98	VLL	-742.5	-424.5
99	RES#	-687.5	-424.5
100	D/C#	-632.5	-424.5
101	CS#	-577.5	-424.5
102	VLL	-522.5	-424.5
103	CLS	-467.5	-424.5
104	VLH	-412.5	-424.5
105	BS2	-357.5	-424.5
106	VLL	-302.5	-424.5
107	BS1	-247.5	-424.5
108	VLH	-192.5	-424.5
109	BS0	-137.5	-424.5
110	VLL	-82.5	-424.5
111	R/W#(WR#)	-27.5	-424.5
112	E(RD#)	27.5	-424.5
113	VLH	82.5	-424.5
114	D_SEL	137.5	-424.5
115	VLL	192.5	-424.5
116	VDD	247.5	-424.5
117	VDD	302.5	-424.5
118	VDD	357.5	-424.5
119	VDD	412.5	-424.5
120	VPP	467.5	-424.5
121	VPP	522.5	-424.5
122	D0	577.5	-424.5
123	D1	632.5	-424.5
124	D2	687.5	-424.5
125	D3	742.5	-424.5
126	D4	797.5	-424.5
127	D5	852.5	-424.5
128	D6	907.5	-424.5
129	D7	962.5	-424.5
130	D8	1017.5	-424.5
131	D9	1072.5	-424.5
132	D10	1127.5	-424.5
133	D11	1182.5	-424.5
134	D12	1237.5	-424.5
135	D13	1292.5	-424.5
136	D14	1347.5	-424.5
137	D15	1402.5	-424.5
138	VLL	1457.5	-424.5
139	VCC	1512.5	-424.5
140	VCC	1567.5	-424.5
141	VCC	1622.5	-424.5
142	VCC	1677.5	-424.5
143	VP	1732.5	-424.5
144	VP	1787.5	-424.5
145	VP	1842.5	-424.5
146	VP	1897.5	-424.5
147	VP	1952.5	-424.5
148	VP	2007.5	-424.5
149	VCOMH	2062.5	-424.5
150	VCOMH	2117.5	-424.5
151	VCOMH	2172.5	-424.5
152	VCOMH	2227.5	-424.5
153	VCOMH	2282.5	-424.5
154	VSL	2337.5	-424.5
155	VSL	2392.5	-424.5
156	VSL	2447.5	-424.5
157	VLSS	2502.5	-424.5
158	VLSS	2557.5	-424.5
159	VLSS	2612.5	-424.5
160	VLSS	2667.5	-424.5
161	NC	2722.5	-424.5
162	NC	2777.5	-424.5
163	NC	2832.5	-424.5
164	NC	2887.5	-424.5
165	NC	2942.5	-424.5
166	NC	2997.5	-424.5
167	NC	3052.5	-424.5
168	NC	3107.5	-424.5
169	NC	3162.5	-424.5
170	NC	3217.5	-424.5
171	NC	3272.5	-424.5
172	NC	3327.5	-424.5
173	NC	3382.5	-424.5
174	NC	3437.5	-424.5
175	NC	3547	-425.9
176	COM63	3580.4	-425.9
177	COM62	3613.8	-425.9
178	COM61	3647.2	-425.9
179	COM60	3680.6	-425.9
180	COM59	3714	-425.9
181	COM58	3747.4	-425.9
182	COM57	3780.8	-425.9
183	COM56	3814.2	-425.9
184	COM55	3847.6	-425.9
185	COM54	3881	-425.9
186	COM53	3914.4	-425.9
187	COM52	3947.8	-425.9
188	COM51	3981.2	-425.9
189	COM50	4014.6	-425.9
190	COM49	4048	-425.9
191	COM48	4081.4	-425.9
192	COM47	4114.8	-425.9
193	COM46	4148.2	-425.9
194	COM45	4181.6	-425.9
195	COM44	4215	-425.9
196	COM43	4248.4	-425.9
197	COM42	4281.8	-425.9
198	COM41	4315.2	-425.9
199	COM40	4348.6	-425.9
200	COM39	4382	-425.9
201	COM38	4415.4	-425.9
202	COM37	4448.8	-425.9
203	COM36	4482.2	-425.9
204	COM35	4515.6	-425.9
205	COM34	4549	-425.9
206	COM33	4582.4	-425.9
207	COM32	4615.8	-425.9
208	COM31	4649.2	-425.9
209	COM30	4682.6	-425.9
210	COM29	4716	-425.9
211	COM28	4749.4	-425.9
212	COM27	4782.8	-425.9
213	COM26	4816.2	-425.9
214	COM25	4849.6	-425.9
215	COM24	4883	-425.9
216	COM23	4916.4	-425.9
217	COM22	4949.8	-425.9
218	COM21	4983.2	-425.9
219	COM20	5016.6	-425.9
220	COM19	5050	-425.9
221	COM18	5083.4	-425.9
222	VLSS	5116.8	-425.9
223	NC	5356.9	-451.9
224	COM17	5356.9	-418.5
225	COM16	5356.9	-385.1
226	COM15	5356.9	-351.7
227	COM14	5356.9	-318.3
228	COM13	5356.9	-284.9
229	COM12	5356.9	-251.5
230	COM11	5356.9	-218.1
231	COM10	5356.9	-184.7
232	COM9	5356.9	-151.3
233	COM8	5356.9	-117.9
234	COM7	5356.9	-84.5
235	COM6	5356.9	-51.1
236	COM5	5356.9	-17.7
237	COM4	5356.9	15.7
238	COM3	5356.9	49.1
239	COM2	5356.9	82.5
240	COM1	5356.9	115.9

Pin Number	Pin Name	X	Y
241	COM0	5356.9	149.3
242	NC	5324.5	434
243	SA0	5297.5	434
244	SB0	5270.5	434
245	SC0	5243.5	434
246	SA1	5216.5	434
247	SB1	5189.5	434
248	SC1	5162.5	434
249	SA2	5135.5	434
250	SB2	5108.5	434
251	SC2	5081.5	434
252	SA3	5054.5	434
253	SB3	5027.5	434
254	SC3	5000.5	434
255	SA4	4973.5	434
256	SB4	4946.5	434
257	SC4	4919.5	434
258	SA5	4892.5	434
259	SB5	4865.5	434
260	SC5	4838.5	434
261	SA6	4811.5	434
262	SB6	4784.5	434
263	SC6	4757.5	434
264	SA7	4730.5	434
265	SB7	4703.5	434
266	SC7	4676.5	434
267	SA8	4649.5	434
268	SB8	4622.5	434
269	SC8	4595.5	434
270	SA9	4568.5	434
271	SB9	4541.5	434
272	SC9	4514.5	434
273	SA10	4487.5	434
274	SB10	4460.5	434
275	SC10	4433.5	434
276	SA11	4406.5	434
277	SB11	4379.5	434
278	SC11	4352.5	434
279	SA12	4325.5	434
280	SB12	4298.5	434
281	SC12	4271.5	434
282	SA13	4244.5	434
283	SB13	4217.5	434
284	SC13	4190.5	434
285	SA14	4163.5	434
286	SB14	4136.5	434
287	SC14	4109.5	434
288	SA15	4082.5	434
289	SB15	4055.5	434
290	SC15	4028.5	434
291	SA16	4001.5	434
292	SB16	3974.5	434
293	SC16	3947.5	434
294	SA17	3920.5	434
295	SB17	3893.5	434
296	SC17	3866.5	434
297	SA18	3839.5	434
298	SB18	3812.5	434
299	SC18	3785.5	434
300	SA19	3758.5	434
301	SB19	3731.5	434
302	SC19	3704.5	434
303	SA20	3677.5	434
304	SB20	3650.5	434
305	SC20	3623.5	434
306	SA21	3596.5	434
307	SB21	3569.5	434
308	SC21	3542.5	434
309	SA22	3515.5	434
310	SB22	3488.5	434
311	SC22	3461.5	434
312	SA23	3434.5	434
313	SB23	3407.5	434
314	SC23	3380.5	434
315	SA24	3353.5	434
316	SB24	3326.5	434
317	SC24	3299.5	434
318	SA25	3272.5	434
319	SB25	3245.5	434
320	SC25	3218.5	434

Pin Number	Pin Name	X	Y
321	SA26	3191.5	434
322	SB26	3164.5	434
323	SC26	3137.5	434
324	SA27	3110.5	434
325	SB27	3083.5	434
326	SC27	3056.5	434
327	SA28	3029.5	434
328	SB28	3002.5	434
329	SC28	2975.5	434
330	SA29	2948.5	434
331	SB29	2921.5	434
332	SC29	2894.5	434
333	SA30	2867.5	434
334	SB30	2840.5	434
335	SC30	2813.5	434
336	SA31	2786.5	434
337	SB31	2759.5	434
338	SC31	2732.5	434
339	SA32	2705.5	434
340	SB32	2678.5	434
341	SC32	2651.5	434
342	SA33	2624.5	434
343	SB33	2597.5	434
344	SC33	2570.5	434
345	SA34	2543.5	434
346	SB34	2516.5	434
347	SC34	2489.5	434
348	SA35	2462.5	434
349	SB35	2435.5	434
350	SC35	2408.5	434
351	SA36	2381.5	434
352	SB36	2354.5	434
353	SC36	2327.5	434
354	SA37	2300.5	434
355	SB37	2273.5	434
356	SC37	2246.5	434
357	SA38	2219.5	434
358	SB38	2192.5	434
359	SC38	2165.5	434
360	SA39	2138.5	434
361	SB39	2111.5	434
362	SC39	2084.5	434
363	SA40	2057.5	434
364	SB40	2030.5	434
365	SC40	2003.5	434
366	SA41	1976.5	434
367	SB41	1949.5	434
368	SC41	1922.5	434
369	SA42	1895.5	434
370	SB42	1868.5	434
371	SC42	1841.5	434
372	SA43	1814.5	434
373	SB43	1787.5	434
374	SC43	1760.5	434
375	SA44	1733.5	434
376	SB44	1706.5	434
377	SC44	1679.5	434
378	SA45	1652.5	434
379	SB45	1625.5	434
380	SC45	1598.5	434
381	SA46	1571.5	434
382	SB46	1544.5	434
383	SC46	1517.5	434
384	SA47	1490.5	434
385	SB47	1463.5	434
386	SC47	1436.5	434
387	VCC	1409.5	434
388	VCC	1309.5	434
389	SA48	1282.5	434
390	SB48	1255.5	434
391	SC48	1228.5	434
392	SA49	1201.5	434
393	SB49	1174.5	434
394	SC49	1147.5	434
395	SA50	1120.5	434
396	SB50	1093.5	434
397	SC50	1066.5	434
398	SA51	1039.5	434
399	SB51	1012.5	434
400	SC51	985.5	434

Pin Number	Pin Name	X	Y
401	SA52	958.5	434
402	SB52	931.5	434
403	SC52	904.5	434
404	SA53	877.5	434
405	SB53	850.5	434
406	SC53	823.5	434
407	SA54	796.5	434
408	SB54	769.5	434
409	SC54	742.5	434
410	SA55	715.5	434
411	SB55	688.5	434
412	SC55	661.5	434
413	SA56	634.5	434
414	SB56	607.5	434
415	SC56	580.5	434
416	SA57	553.5	434
417	SB57	526.5	434
418	SC57	499.5	434
419	SA58	472.5	434
420	SB58	445.5	434
421	SC58	418.5	434
422	SA59	391.5	434
423	SB59	364.5	434
424	SC59	337.5	434
425	SA60	310.5	434
426	SB60	283.5	434
427	SC60	256.5	434
428	SA61	229.5	434
429	SB61	202.5	434
430	SC61	175.5	434
431	SA62	148.5	434
432	SB62	121.5	434
433	SC62	94.5	434
434	SA63	67.5	434
435	SB63	40.5	434
436	SC63	13.5	434
437	SA64	-13.5	434
438	SB64	-40.5	434
439	SC64	-67.5	434
440	SA65	-94.5	434
441	SB65	-121.5	434
442	SC65	-148.5	434
443	SA66	-175.5	434
444	SB66	-202.5	434
445	SC66	-229.5	434
446	SA67	-256.5	434
447	SB67	-283.5	434
448	SC67	-310.5	434
449	SA68	-337.5	434
450	SB68	-364.5	434
451	SC68	-391.5	434
452	SA69	-418.5	434
453	SB69	-445.5	434
454	SC69	-472.5	434
455	SA70	-499.5	434
456	SB70	-526.5	434
457	SC70	-553.5	434
458	SA71	-580.5	434
459	SB71	-607.5	434
460	SC71	-634.5	434
461	SA72	-661.5	434
462	SB72	-688.5	434
463	SC72	-715.5	434
464	SA73	-742.5	434
465	SB73	-769.5	434
466	SC73	-796.5	434
467	SA74	-823.5	434
468	SB74	-850.5	434
469	SC74	-877.5	434
470	SA75	-904.5	434
471	SB75	-931.5	434
472	SC75	-958.5	434
473	SA76	-985.5	434
474	SB76	-1012.5	434
475	SC76	-1039.5	434
476	SA77	-1066.5	434
477	SB77	-1093.5	434
478	SC77	-1120.5	434
479	SA78	-1147.5	434
480	SB78	-1174.5	434

Pin Number	Pin Name	X	Y
481	SC78	-1201.5	434
482	SA79	-1228.5	434
483	SB79	-1255.5	434
484	SC79	-1282.5	434
485	VCC	-1309.5	434
486	VCC	-1409.5	434
487	SA80	-1436.5	434
488	SB80	-1463.5	434
489	SC80	-1490.5	434
490	SA81	-1517.5	434
491	SB81	-1544.5	434
492	SC81	-1571.5	434
493	SA82	-1598.5	434
494	SB82	-1625.5	434
495	SC82	-1652.5	434
496	SA83	-1679.5	434
497	SB83	-1706.5	434
498	SC83	-1733.5	434
499	SA84	-1760.5	434
500	SB84	-1787.5	434
501	SC84	-1814.5	434
502	SA85	-1841.5	434
503	SB85	-1868.5	434
504	SC85	-1895.5	434
505	SA86	-1922.5	434
506	SB86	-1949.5	434
507	SC86	-1976.5	434
508	SA87	-2003.5	434
509	SB87	-2030.5	434
510	SC87	-2057.5	434
511	SA88	-2084.5	434
512	SB88	-2111.5	434
513	SC88	-2138.5	434
514	SA89	-2165.5	434
515	SB89	-2192.5	434
516	SC89	-2219.5	434
517	SA90	-2246.5	434
518	SB90	-2273.5	434
519	SC90	-2300.5	434
520	SA91	-2327.5	434
521	SB91	-2354.5	434
522	SC91	-2381.5	434
523	SA92	-2408.5	434
524	SB92	-2435.5	434
525	SC92	-2462.5	434
526	SA93	-2489.5	434
527	SB93	-2516.5	434
528	SC93	-2543.5	434
529	SA94	-2570.5	434
530	SB94	-2597.5	434
531	SC94	-2624.5	434
532	SA95	-2651.5	434
533	SB95	-2678.5	434
534	SC95	-2705.5	434
535	SA96	-2732.5	434
536	SB96	-2759.5	434
537	SC96	-2786.5	434
538	SA97	-2813.5	434
539	SB97	-2840.5	434
540	SC97	-2867.5	434
541	SA98	-2894.5	434
542	SB98	-2921.5	434
543	SC98	-2948.5	434
544	SA99	-2975.5	434
545	SB99	-3002.5	434
546	SC99	-3029.5	434
547	SA100	-3056.5	434
548	SB100	-3083.5	434
549	SC100	-3110.5	434
550	SA101	-3137.5	434
551	SB101	-3164.5	434
552	SC101	-3191.5	434
553	SA102	-3218.5	434
554	SB102	-3245.5	434
555	SC102	-3272.5	434
556	SA103	-3299.5	434
557	SB103	-3326.5	434
558	SC103	-3353.5	434
559	SA104	-3380.5	434
560	SB104	-3407.5	434

Pin Number	Pin Name	X	Y
561	SC104	-3434.5	434
562	SA105	-3461.5	434
563	SB105	-3488.5	434
564	SC105	-3515.5	434
565	SA106	-3542.5	434
566	SB106	-3569.5	434
567	SC106	-3596.5	434
568	SA107	-3623.5	434
569	SB107	-3650.5	434
570	SC107	-3677.5	434
571	SA108	-3704.5	434
572	SB108	-3731.5	434
573	SC108	-3758.5	434
574	SA109	-3785.5	434
575	SB109	-3812.5	434
576	SC109	-3839.5	434
577	SA110	-3866.5	434
578	SB110	-3893.5	434
579	SC110	-3920.5	434
580	SA111	-3947.5	434
581	SB111	-3974.5	434
582	SC111	-4001.5	434
583	SA112	-4028.5	434
584	SB112	-4055.5	434
585	SC112	-4082.5	434
586	SA113	-4109.5	434
587	SB113	-4136.5	434
588	SC113	-4163.5	434
589	SA114	-4190.5	434
590	SB114	-4217.5	434
591	SC114	-4244.5	434
592	SA115	-4271.5	434
593	SB115	-4298.5	434
594	SC115	-4325.5	434
595	SA116	-4352.5	434
596	SB116	-4379.5	434
597	SC116	-4406.5	434
598	SA117	-4433.5	434
599	SB117	-4460.5	434
600	SC117	-4487.5	434
601	SA118	-4514.5	434
602	SB118	-4541.5	434
603	SC118	-4568.5	434
604	SA119	-4595.5	434
605	SB119	-4622.5	434
606	SC119	-4649.5	434
607	SA120	-4676.5	434
608	SB120	-4703.5	434
609	SC120	-4730.5	434
610	SA121	-4757.5	434
611	SB121	-4784.5	434
612	SC121	-4811.5	434
613	SA122	-4838.5	434
614	SB122	-4865.5	434
615	SC122	-4892.5	434
616	SA123	-4919.5	434
617	SB123	-4946.5	434
618	SC123	-4973.5	434
619	SA124	-5000.5	434
620	SB124	-5027.5	434
621	SC124	-5054.5	434
622	SA125	-5081.5	434
623	SB125	-5108.5	434
624	SC125	-5135.5	434
625	SA126	-5162.5	434
626	SB126	-5189.5	434
627	SC126	-5216.5	434
628	SA127	-5243.5	434
629	SB127	-5270.5	434
630	SC127	-5297.5	434
631	NC	-5324.5	434
632	COM64	-5356.9	149.3
633	COM65	-5356.9	115.9
634	COM66	-5356.9	82.5
635	COM67	-5356.9	49.1
636	COM68	-5356.9	15.7
637	COM69	-5356.9	-17.7
638	COM70	-5356.9	-51.1
639	COM71	-5356.9	-84.5
640	COM72	-5356.9	-117.9

Pin Number	Pin Name	X	Y
641	COM73	-5356.9	-151.3
642	COM74	-5356.9	-184.7
643	COM75	-5356.9	-218.1
644	COM76	-5356.9	-251.5
645	COM77	-5356.9	-284.9
646	COM78	-5356.9	-318.3
647	COM79	-5356.9	-351.7
648	COM80	-5356.9	-385.1
649	COM81	-5356.9	-418.5
650	NC	-5356.9	-451.9

Appendix III: SSD1357 Command Table and Command Description

1 COMMAND TABLE

Table 1-1: SSD1357 Command Table

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	A0 A[7:0] B[7:0]	1 A_7 0	0 A_6 0	1 A_5 0	0 A_4 0	0 A_3 0	0 A_2 0	0 A_1 0	0 A_0 0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 127 is mapped to SEG0 A[2]=0b, Color sequence: A B C [reset] A[2]=1b, Color sequence is swapped: C B A A[3]=0b, Reserved [reset] A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] A[7:6] Set Color Depth, 00b: 256color 01b: 65k color [reset] 10b: 262k color 11b Pseudo 262k color, 16-bit format 2 Refer to Product Preview Table 6-6 for details

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~127. [reset=00h]
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-127. [reset=00h]
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 2~30 DCLK(s) clocks [reset=0100b] A[3:0]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 = 30DCLKs A[7:4] Phase 2 period of 2~30 DCLK(s) clocks [reset=1000b] A[7:4]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 =30DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0000b], divide by DIVSET where A[3:0] → DIVSET 0000 → divide by 1 0001 → divide by 2 0010 → divide by 4 0011 → divide by 8 0100 → divide by 16 0101 → divide by 32 0110 → divide by 64 0111 → divide by 128 1000 → divide by 256 >=1001 → invalid A[7:4] Oscillator frequency, frequency increases as level increases [reset=0010b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS .... 1000 8 DCLKS [reset] .... 1111 15 DCLKS
1	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		
0	B8	1	0	1	1	1	0	0	0	Master Look Up Table for Gray Scale Pulse width (Color A,B,C)	The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d). A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A62[7:0]: Gamma Setting for GS62, A63[7:0]: Gamma Setting for GS63 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS62 < Setting of GS63 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input only, color A, B, C will follow the master LUT. (5) When command BCh is input, it selects individual LUT for color A, GS1~31A; When command BDh is input, it selects individual LUT for color C, GS1~31C (6) To select individual LUT for color B, A and C, command B8h should be input before command BCh and BDh,
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A62[7:0]	$A62_7$	$A62_6$	$A62_5$	$A62_4$	$A62_3$	$A62_2$	$A62_1$	$A62_0$		
1	A63[7:0]	$A63_7$	$A63_6$	$A63_5$	$A63_4$	$A63_3$	$A63_2$	$A63_1$	$A63_0$		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: **Color A**: GS1A = 0 DCLK; GS2A = 4 DCLK; GS3A = 8 DCLK; ... ; GS31A = 120 DCLK **Color B**: GS1B = 0 DCLK; GS2B = 2 DCLK; GS3B = 4 DCLK; ... ; GS62B = 122 DCLK; GS63B = 124 DCLK **Color C**: GS1C = 0 DCLK; GS2C = 4 DCLK; GS3C = 8 DCLK; ... ; GS31C = 120 DCLK
0 1	BB A[4:0]	1 0	0 0	1 0	1 A_4	1 A_3	0 A_2	1 A_1	1 A_0	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 11110b] A[4:0] / Hex code / pre-charge voltage: 00000 / 00h / 0.10 x V_{CC} : / : / : 11110 / 1Eh / 0.50 x V_{CC} [reset] 11111 / 1Fh / 0.5133 x V_{CC} **Note** (1)Pre-charge voltage level must be smaller than COM deselect voltage level
0 1 1 1 1 1 1 1	BC A1[7:0] A2[7:0] . . . A30[7:0] A31[7:0]	1 $A1_7$ $A2_7$ . . . $A30_7$ $A31_7$	0 $A1_6$ $A2_6$ . . . $A30_6$ $A31_6$	1 $A1_5$ $A2_5$ . . . $A30_5$ $A31_5$	1 $A1_4$ $A2_4$ . . . $A30_4$ $A31_4$	1 $A1_3$ $A2_3$ . . . $A30_3$ $A31_3$	1 $A1_2$ $A2_2$ . . . $A30_2$ $A31_2$	0 $A1_1$ $A2_1$ . . . $A30_1$ $A31_1$	0 $A1_0$ $A2_0$ . . . $A30_0$ $A31_0$	Individual Look Up Table for Gray Scale Pulse width (Color A)	The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color A. A1[7:0]: Gamma Setting for GS1A, A2[7:0]: Gamma Setting for GS2A, : A62[7:0]: Gamma Setting for GS30A, A63[7:0]: Gamma Setting for GS31A **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for color A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BD	1	0	1	1	1	1	0	1	Individual Look Up Table for Gray Scale Pulse width (Color C)	The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color C. A1[7:0]: Gamma Setting for GS1C, A2[7:0]: Gamma Setting for GS2C, : A62[7:0]: Gamma Setting for GS30C, A63[7:0]: Gamma Setting for GS31C **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for color A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A30[7:0]	$A30_7$	$A30_6$	$A30_5$	$A30_4$	$A30_3$	$A30_2$	$A30_1$	$A30_0$		
1	A31[7:0]	$A31_7$	$A31_6$	$A31_5$	$A31_4$	$A31_3$	$A31_2$	$A31_1$	$A31_0$		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Set COM deselect voltage level [reset = 05h] **A[2:0]** / **Hex code** / **V_{COMH}** 000 / 00h / 0.72 x V_{CC} : / : / : 101 / 05h / 0.82 x V_{CC} [reset] : / : / : 111 / 07h / 0.86 x V_{CC}
1	A[2:0]	0	0	0	0	0	A_2	A_1	A_0		
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=7Fh] B[7:0] Contrast Value Color B [reset=7Fh] C[7:0] Contrast Value Color C [reset=7Fh]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] : 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset]
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0] MUX ratio 4MUX ~ 128MUX, [reset=127], (Range from 3 to 127)
1	A[6:0]	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	FD A[7:0]	1 A_7	1 A_6	1 A_5	1 A_4	1 A_3	1 A_2	0 A_1	1 A_0	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12h, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16h, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Note
(1) "*" stands for "Don't care".

Table 1-2: SSD1357 Graphic Acceleration Command List

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	96	1	0	0	1	0	1	1	0	Horizontal Scroll	A[7:0] = 00000000b No scrolling A[7:0] = 00000001b to 00111111b Scroll towards SEG127 with 1 column offset A[7:0] = 01000000b to 11111111b Scroll towards SEG0 with 1 column offset B[6:0] : start row address C[7:0] : end row address D[6:0] : Reserved (reset=00h) E[1:0] : scrolling time interval 00b Invalid 01b normal 10b slow 11b slowest **Note** Operates during display ON.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[6:0]	0	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	0	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[6:0]	0	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[1:0]	0	0	0	0	0	0	E_1	E_0		
0	9E	1	0	0	1	1	1	1	0	Stop Moving	Stop horizontal scroll **Note** After sending 9Eh command to stop the scrolling action, the ram data needs to be rewritten
0	9F	1	0	0	1	1	1	1	1	Start Moving	Start horizontal scroll

Note

(2) "*" stands for "Don't care".

2 COMMAND DESCRIPTION

2.1 Set Column Address (15h)

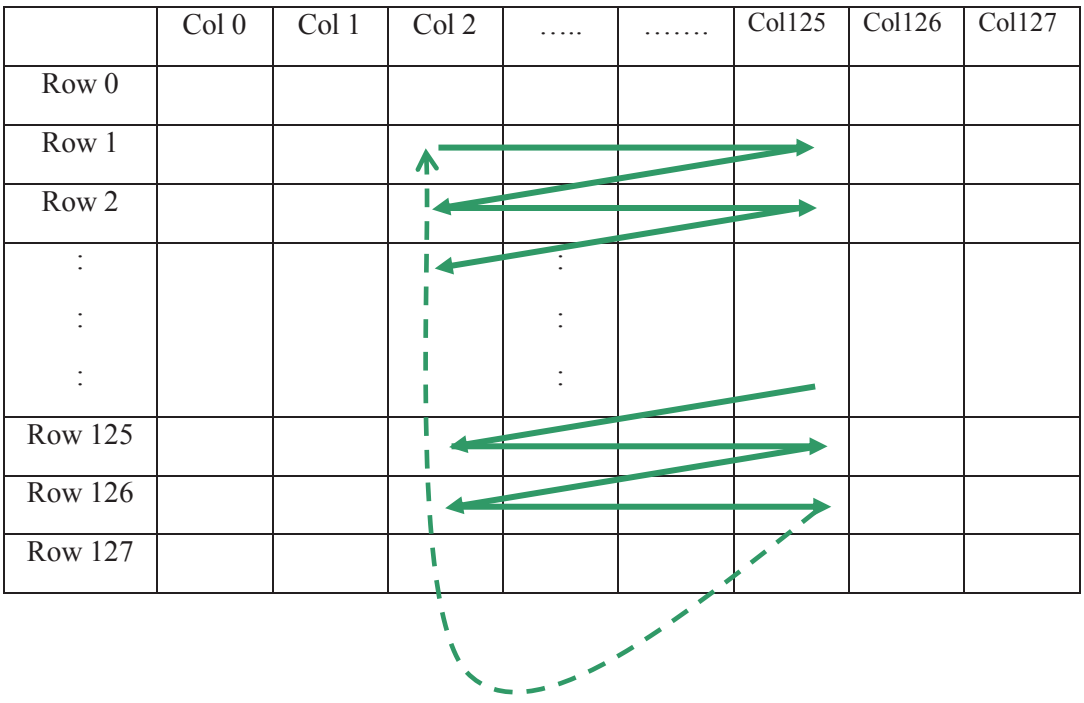
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

2.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 125, row start address is set to 1 and row end address is set to 126. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 125 and from row 1 to row 126 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation(*solid line in Figure 2-1*). Whenever the column address pointer finishes accessing the end column 125, it is reset back to column 2 and row address is automatically increased by 1(*solid line in Figure 2-1*). While the end row 126 and end column 125 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2(*dotted line in Figure 2-1*).

Figure 2-1 : Example of Column and Row Address Pointer Movement



2.3 Write RAM Command (5Ch)

After entering this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

2.4 Read RAM Command (5Dh)

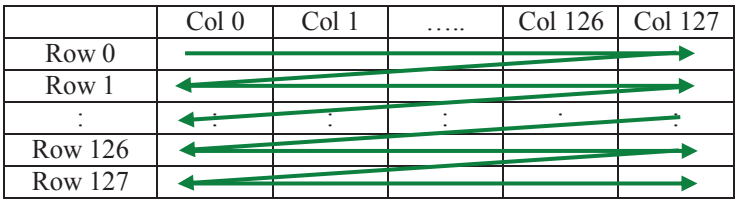
After entering this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

2.5 Set Re-map & Dual COM Line Mode (A0h)

This command has multiple configurations and each bit setting is described as follows:

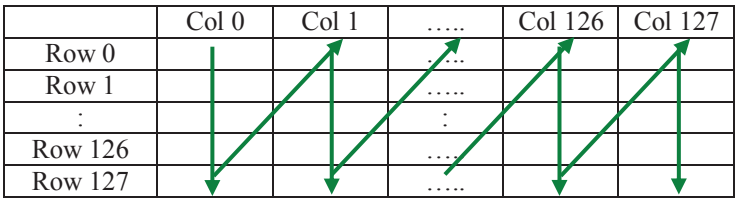
- Address increment mode (A[0])
  When A[0] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 2-2.

Figure 2-2 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 2-3.

Figure 2-3: Address Pointer Movement of Vertical Address Increment Mode

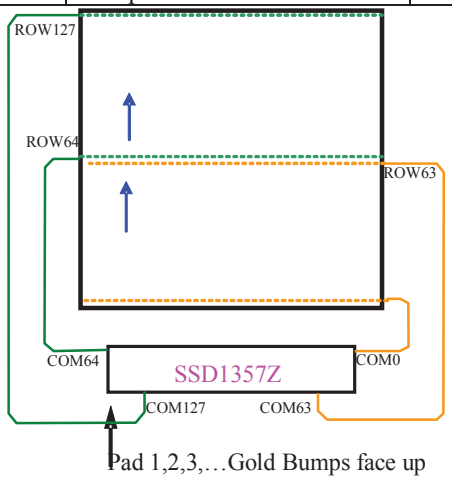


- Column Address Remap (A[1])
  This command bit is made for increasing the layout flexibility of segment signals in OLED module with segment arranged from left to right (when A[1] is set to 0) or vice versa (when A[1] is set to 1), as demonstrated in Figure 2-4.
  A[1] = 0 (reset): RAM Column 0 ~ 127 maps to Col0~Col127
  A[1] = 1: RAM Column 0 ~ 127 maps to Col127~Col0

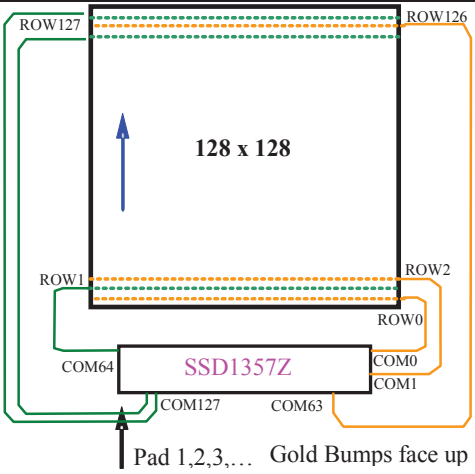
- Color Remap (A[2])
  A[2] = 0 (reset): color sequence A → B → C
  A[2] = 1: color sequence C → B → A
- COM scan direction Remap (A[4])
  This command bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
  A[1] = 0 (reset): Scan from up to down
  A[1] = 1: Scan from bottom to up
  Details of pin arrangement can be found in Figure 2-4.
- Odd even split of COM pins (A[5])
  This command bit can set the odd even arrangement of COM pins.
  A[5] = 0 (reset): Disable COM split odd even, pin assignment of common is in sequential as
  COM127 COM126...COM 65 COM64...SEG479...SEG0...COM0 COM1...COM62 COM63
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM127 COM125...COM3 COM1...SEG479...SEG0...COM0 COM2...COM124 COM126
  Details of pin arrangement can be found in Figure 2-4.

Figure 2-4 : COM Pins Hardware Configuration (MUX ratio: 128)

A[5] =0	A[3]=0	A[4]=0
Disable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM0 to COM127



A[5] =1	A[3]=0	A[4]=0
Enable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM0 to COM127



- Display color mode (A[7:6])
  Select either 262k, 65k or 256 color mode.

2.6 Set Display Start Line (A1h)

This command is used to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 2-5 shows an example of using this command when MUX ratio = 128 and MUX ratio = 100 and Display Start Line = 28. In there, "Row" means the graphic display data RAM row.

Figure 2-5 : Example of Set Display Start Line with no Remap

	128	128	100	100	MUX ratio (CAh)
COM Pin	0	28	0	28	Display start line (A1h)
COM0	Row0	Row28	Row0	Row28	
COM1	Row1	Row29	Row1	Row29	
COM2	Row2	Row30	Row2	Row30	
COM3	Row3	Row31	Row3	Row31	
COM4	Row4	Row32	Row4	Row32	
COM5	Row5	Row33	Row5	Row33	
COM6	Row6	Row34	Row6	Row34	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
COM95	Row95	Row123	Row95	Row124	
COM96	Row96	Row124	Row96	Row125	
COM97	Row97	Row125	Row97	Row126	
COM98	Row98	Row126	Row98	Row127	
COM99	Row99	Row127	Row99	Row0	
COM100	Row100	Row0	-	-	
COM101	Row101	Row1	-	-	
COM102	Row102	Row2	-	-	
COM103	Row103	Row3	-	-	
COM104	Row104	Row4	-	-	
COM105	Row105	Row5	-	-	
COM106	Row106	Row6	-	-	
COM107	Row107	Row7	-	-	
COM108	Row108	Row8	-	-	
COM109	Row109	Row9	-	-	
COM110	Row110	Row10	-	-	
COM111	Row111	Row11	-	-	
COM112	Row112	Row12	-	-	
COM113	Row113	Row13	-	-	
COM114	Row114	Row14	-	-	
COM115	Row115	Row15	-	-	
COM116	Row116	Row16	-	-	
COM117	Row117	Row17	-	-	
COM118	Row118	Row18	-	-	
COM119	Row119	Row19	-	-	
COM120	Row120	Row20	-	-	
COM121	Row121	Row21	-	-	
COM122	Row122	Row22	-	-	
COM123	Row123	Row23	-	-	
COM124	Row124	Row24	-	-	
COM125	Row125	Row25	-	-	
COM126	Row126	Row26	-	-	
COM127	Row127	Row27	-	-	
Display example	 (a)	 (b)	 (c)	 (d)	 (GDDARAM)	

2.7 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-127. For example, to move the COM16 towards the COM0 direction for 16 lines, A[7:0] should be given by 00010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 2-6 : Example of Set Display Offset with no Remap

	a	b	c	Case
	128	96	96	MUX ratio (CAh)
	0	0	32	Display offset (A2h A[7:0])
COM0	Row0	Row0	Row32	
COM1	Row1	Row1	Row33	
COM2	Row2	Row2	Row34	
:	:	:	:	
COM61	Row61	Row61	Row93	
COM62	Row62	Row62	Row94	
COM63	Row63	Row63	Row95	
COM64	Row64	Row64	-	
COM65	Row65	Row65	-	
COM66	Row66	Row66	-	
:	:	:	:	
COM93	Row93	Row93	-	
COM94	Row94	Row94	-	
COM95	Row95	Row95	-	
COM96	Row96	-	Row0	
COM97	Row97	-	Row1	
COM98	Row98	-	Row2	
:	:	:	:	
COM125	Row125	-	Row29	
COM126	Row126	-	Row30	
COM127	Row127	-	Row31	
Display example	 (a)	 (c)	 (d)	 (GDDARAM)

2.8 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

- All OFF (A4h)
  Force the entire display to be at gray scale level "GS0" regardless of the contents of the display data RAM as shown in Figure 2-7.

Figure 2-7 : Example of Entire Display OFF

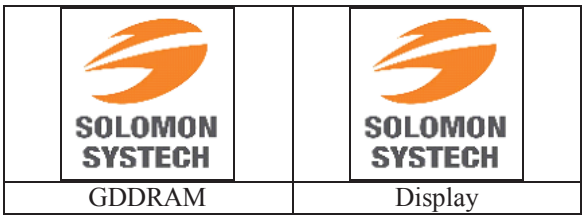
- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale "GS63" regardless of the contents of the display data RAM as shown in Figure 2-8.

Figure 2-8 : Example of Entire Display ON

- Set Entire Display OFF (A6h)

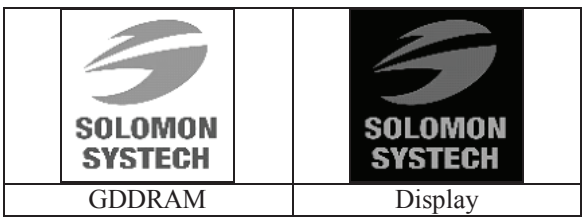
  Reset the above effect and turn the data to ON at the corresponding gray level. Figure 2-9 shows an example of Normal Display.

Figure 2-9 : Example of Normal Display



- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" ↔ "GS63", "GS1" ↔ "GS62", …
  Figure 2-10 shows an example of inverse display.

Figure 2-10 : Example of Inverse Display



2.9 Set Sleep mode ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is OFF (command AEh), the segment is in V_{SS} state and common is in high impedance state.

2.10 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 2 to 30 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 2 to 30 in the unit of 2DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P.

2.11 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 8, with reset value =0. Please refer to Product Preview Section 6.3 for the detail relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

2.12 Set Second Pre-charge period (B6h)

This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 1 to 15 DCLK's.

2.13 Look Up Table for Gray Scale Pulse width (B8h, BCh, BDh)

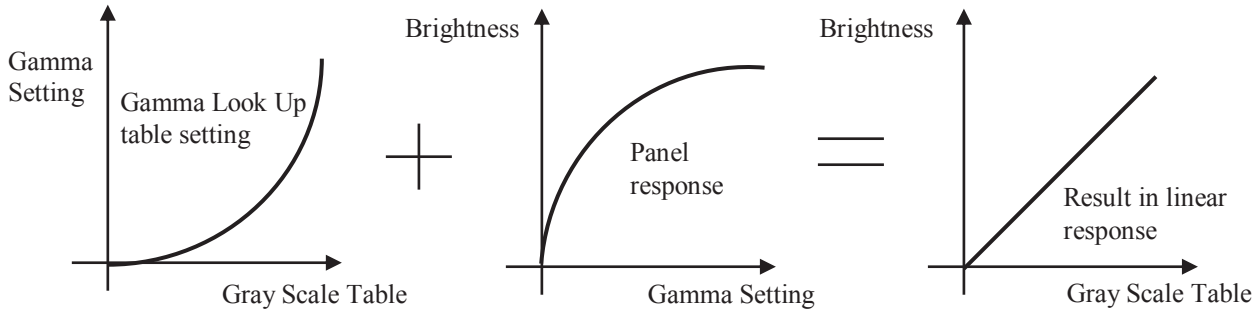
This command is used to set each individual gray scale level of Color A, B and C for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON.

Following the command B8h, the user has to set the gray scale setting for GS1B, GS2B, …, GS62B, GS63B one by one in sequence for LUT of color B. GS1 can be set as gamma setting 0, which means there is only pre-charge phase but no current drive phase. Refer to Product Preview Section 6.8 for details. Command B8h should be input before command BCh and BDh, to select LUT for color B, A and C.

After setting B8h command, BCh and BDh commands are used to set gray scale setting for color A and color C respectively. Following the command BCh, the user has to set the gray scale setting for GS1A, GS2A, …, GS30A, GS31A one by one in sequence for LUT of color A. While following the command BDh, the user has to set the gray scale setting for GS1C, GS2C, …, GS30C, GS31C one by one in sequence for LUT of color C.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 2-) can compensate this effect.

Figure 2-12 : Example of Gamma correction by Gamma Look Up table setting



2.14 Use Built-in Linear LUT (B9h)

This single byte command reloads the preset linear Gray Scale table. For color B, GS0 =Gamma Setting 0, GS1 = Gamma Setting 0, GS2 = Gamma Setting 2, GS3 = Gamma Setting 4,... GS62 = Gamma Setting 122, GS63 = Gamma Setting 124. Refer to Product Preview Section 6.8 for details.

2.15 Set Pre-charge voltage (BBh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC}.

2.16 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}.

2.17 Set Contrast Current for Color A,B,C (C1h)

This command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

2.18 Master Contrast Current Control (C7h)

This double byte command is to control the segment output current by a scaling factor. The chip has 16 master control steps, with the factor ranges from 1 [0000b] to 16 [1111b – default]. The smaller the master current value, the dimmer the OLED panel display is set.
For example, if original segment output current is 160uA at scale factor = 16, setting scale factor to 8 would reduce the current to 80uA.

2.19 Set Multiplex Ratio (CAh)

This double byte command switches default 1:128 multiplex mode to any multiplex mode from 4 to 128. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h. Figure 2-5 and Figure 2-6 show examples of setting the multiplex ratio through command CAh.

2.20 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the "Lock" state. And the driver IC will then respond to the command and memory access.