SiS9255

Projected Capacitive

Touch-Screen Micro Processor

Data sheet

Rev. 1.2
August 18, 2015

Revision History

Date	Rev	Description
April 23, 2012	0.7	Initial Release
May 07, 2012	0.8	Update Table1
July 24, 2012	0.9	Update General Description
March 19, 2014	1.0-	Modify typo on 4.6 USB interface
July 15, 2014	1.1	Update IC Marking Information
August 18, 2015	1.2	Add examples of Serial Shipping Number

Contents

Figures

Tables

1 General Description

With accumulated PC-based chipset experiences and innovative technologies, SiS has delivered the best performance platforms and recognized as a top Stable Image Chipset Solution provider over the past decades. To further catch ride with the popularity of touch-screen devices launching, SiS9255 was developed to provide an optimal touch screen solution to OEM and ODM vendors for the new generation platform applications.

SiS9255, a 32bit RISC touch-screen panel processor with the 12bits Analog-to-Digital Converter (12bits ADC) provides 52 pins TX, and 32 pins RX for supporting up to 10.1" projected capacitive touch sensor. SiS9255 provides both USB and I2C interface for communicating with host system. An embedded UART port is designed for further debugging and specific R&D applications. Implemented Watchdog Timer and Event Timer serve add-on-value functions for flexibility and creativity. Besides, Power on Demand technology design effectively reduces power-consumption to meet environmental protection requirements. More than that, GPIO feature ensures expandability on both H/W and S/W applications. Taking advantage of above features, SiS9255 enables designers to create new usage model of touch-screen products such as PAD, Tablet PC, Game Console… etc

The embedded 12-bit ADC feature allows users to experience an operating environment of high resolution and high sampling rate which meets the Windows 8's criterion. This extraordinary design is just right for those user-oriented vendors to deliver real-time and seamless playback. The high speed MCU with a filtering management algorithm implements to manage vivid gestures for enabling more direct and natural interaction in your applications. To effective filter out the unexpected coupling noise by hand/fingers operation on LCD/LED panel, SiS9255 has implemented a unique know-how based on the perfect architecture of its H/W, firmware and embedded filters. With its advanced technology algorithm, it can automatically adjust and compensate the sensing methodology to ensure the good touch quality, sensitivity and response-time under various changing humidity, temperature and other environmental factors.

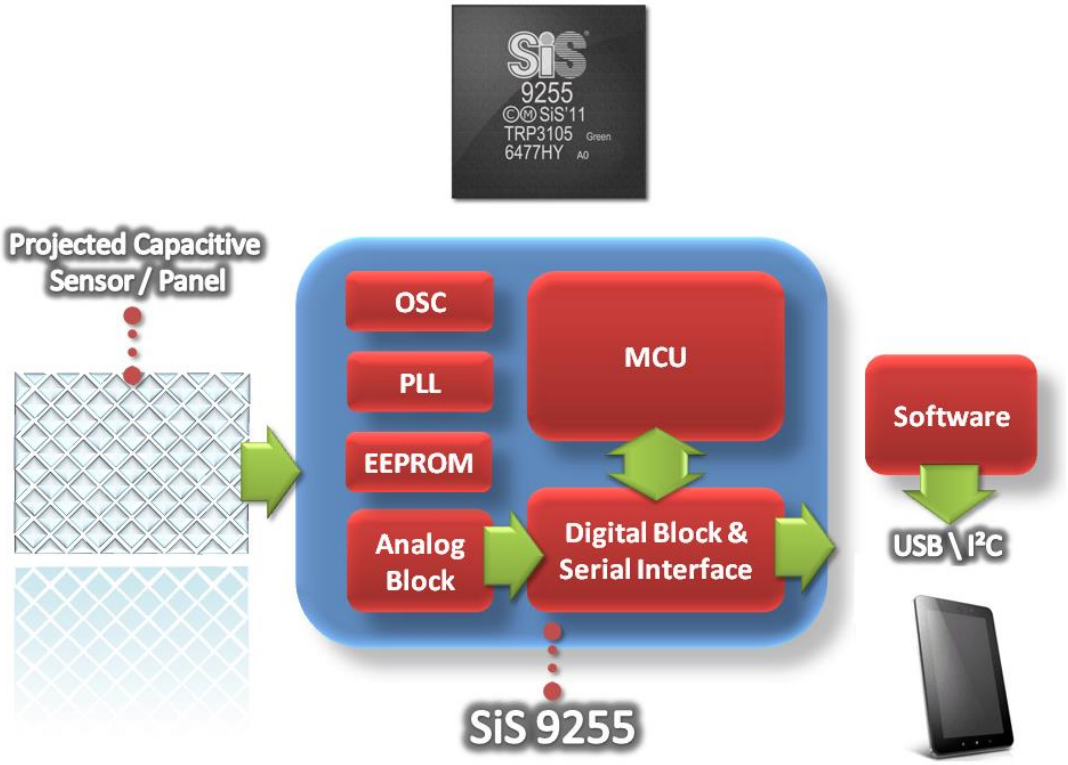


Figure 1 SiS9255 System Diagram

2 Features

■ High Performance RISC Processor

- Embedded high performance 32-bit processor.
- Supports frequency scaling up to 96MHz system clock
- 16K Byte instruction cache
- 24K Byte Data SRAM.
- Supports Interrupt controller
- Support WatchDog timer
- Support Event Timers
- Embedded 64KB Flash ROM
- Internal 12MHz clock

■ Serial Peripheral Interface Master/Slave Controller

- USB 2.0 Compliant
- Support I2C Master/Slave interface
- Support UART port
- Up to 4 GPIO channel

■ Analog System

- Support up to 52 pins TX, 32 pins RX sensing pads.
- Dual 12 bits resolution Analog-to-Digital Converter.
- Support dynamic Power On Demand scheme for power saving at full loading, idle and sleep mode.

■ 132 Pins BGA Green Package

3 Pin Assignment

SiS9255 Top Side View

	1	2	3	4	5	6	7	8	9	10	11	12	
A		TX49	TX47	TX43	TX39	TX36	TX32	TX28	TX25	VSS	USBD+	GPIO2	A
B	TX51	TX50	TX48	TX45	TX41	TX37	TX34	TX30	TX26	REXT	USBD-	GPIO1	B
C	C4N	C4P	HVDD	TX44	TX40	TX38	TX33	TX29	TX27	OVDD	I2C_CLK	I2C_DA	C
D	C3N	C3P	CHVDD	TX46	TX42		TX35	TX31	NC	INT	UART_TX	UART_RX	D
E	C2N	C2P	LVDD	LVDD	LVSS	VSS	VSS	VSS		RESET#	GPIO3	GPIO4	E
F	C1N	C1P	TX2		LVSS	VSS	VSS	VSS		OVDD	Test1	RX31	F
G	TX0	TX1	TX5		LVSS	VSS	VSS	VSS		RX28	RX29	RX30	G
H	TX3	TX4	TX7		LVSS	VSS	VSS	VSS		RX25	RX26	RX27	H
J	TX6	TX8	TX9			RX3	RX7	RX9		RX22	RX23	RX24	J
K	TX10	TX11	TX12	TX19	TX22	RX1	RX5	AVSS	AVDD	RX18	RX20	RX21	K
L	TX13	TX14	TX17	TX20	TX23	RX2	RX6	RX10	RX11	RX14	RX16	RX19	L
M	TX15	TX16	TX18	TX21	TX24	RX0	RX4	RX8	RX12	RX13	RX15	RX17	M
	1	2	3	4	5	6	7	8	9	10	11	12	

SiS9255 Bottom Side View

	12	11	10	9	8	7	6	5	4	3	2	1	
A	GPIO2	USBD+	VSS	TX25	TX28	TX32	TX36	TX39	TX43	TX47	TX49		A
B	GPIO1	USBD-	REXT	TX26	TX30	TX34	TX37	TX41	TX45	TX48	TX50	TX51	B
C	I2C_DA	I2C_CLK	OVDD	TX27	TX29	TX33	TX38	TX40	TX44	HVDD	C4P	C4N	C
D	UART_RX	UART_TX	INT	NC	TX31	TX35		TX42	TX46	CHVDD	C3P	C3N	D
E	GPIO4	GPIO3	RESET#		VSS	VSS	VSS	LVSS	LVDD	LVDD	C2P	C2N	E
F	RX31	Test1	OVDD		VSS	VSS	VSS	LVSS		TX2	C1P	C1N	F
G	RX30	RX29	RX28		VSS	VSS	VSS	LVSS		TX5	TX1	TX0	G
H	RX27	RX26	RX25		VSS	VSS	VSS	LVSS		TX7	TX4	TX3	H
J	RX24	RX23	RX22		RX9	RX7	RX3			TX9	TX8	TX6	J
K	RX21	RX20	RX18	AVDD	AVSS	RX5	RX1	TX22	TX19	TX12	TX11	TX10	K
L	RX19	RX16	RX14	RX11	RX10	RX6	RX2	TX23	TX20	TX17	TX14	TX13	L
M	RX17	RX15	RX13	RX12	RX8	RX4	RX0	TX24	TX21	TX18	TX16	TX15	M
	12	11	10	9	8	7	6	5	4	3	2	1	

4 Pin Description

ADC interface

Pin Name	Pin Attr	Description
TX0	Out	Sense signal output pin
TX1	Out	Sense signal output pin
TX2	Out	Sense signal output pin
TX3	Out	Sense signal output pin
TX4	Out	Sense signal output pin
TX5	Out	Sense signal output pin
TX6	Out	Sense signal output pin
TX7	Out	Sense signal output pin
TX8	Out	Sense signal output pin
TX9	Out	Sense signal output pin
TX10	Out	Sense signal output pin
TX11	Out	Sense signal output pin
TX12	Out	Sense signal output pin
TX13	Out	Sense signal output pin
TX14	Out	Sense signal output pin
TX15	Out	Sense signal output pin
TX16	Out	Sense signal output pin
TX17	Out	Sense signal output pin
TX18	Out	Sense signal output pin
TX19	Out	Sense signal output pin
TX20	Out	Sense signal output pin
TX21	Out	Sense signal output pin
TX22	Out	Sense signal output pin
TX23	Out	Sense signal output pin
TX24	Out	Sense signal output pin
TX25	Out	Sense signal output pin
TX26	Out	Sense signal output pin
TX27	Out	Sense signal output pin
TX28	Out	Sense signal output pin
TX29	Out	Sense signal output pin
TX30	Out	Sense signal output pin
TX31	Out	Sense signal output pin
TX32	Out	Sense signal output pin
TX33	Out	Sense signal output pin
TX34	Out	Sense signal output pin
TX35	Out	Sense signal output pin
TX36	Out	Sense signal output pin
TX37	Out	Sense signal output pin
TX38	Out	Sense signal output pin
TX39	Out	Sense signal output pin
TX40	Out	Sense signal output pin
TX41	Out	Sense signal output pin
TX42	Out	Sense signal output pin

TX43	Out	Sense signal output pin
TX44	Out	Sense signal output pin
TX45	Out	Sense signal output pin
TX46	Out	Sense signal output pin
TX47	Out	Sense signal output pin
TX48	Out	Sense signal output pin
TX49	Out	Sense signal output pin
TX50	Out	Sense signal output pin
TX51	Out	Sense signal output pin
RX0	In	Sense signal input pin
RX1	In	Sense signal input pin
RX2	In	Sense signal input pin
RX3	In	Sense signal input pin
RX4	In	Sense signal input pin
RX5	In	Sense signal input pin
RX6	In	Sense signal input pin
RX7	In	Sense signal input pin
RX8	In	Sense signal input pin
RX9	In	Sense signal input pin
RX10	In	Sense signal input pin
RX11	In	Sense signal input pin
RX12	In	Sense signal input pin
RX13	In	Sense signal input pin
RX14	In	Sense signal input pin
RX15	In	Sense signal input pin
RX16	In	Sense signal input pin
RX17	In	Sense signal input pin
RX18	In	Sense signal input pin
RX19	In	Sense signal input pin
RX20	In	Sense signal input pin
RX21	In	Sense signal input pin
RX22	In	Sense signal input pin
RX23	In	Sense signal input pin
RX24	In	Sense signal input pin
RX25	In	Sense signal input pin
RX26	In	Sense signal input pin
RX27	In	Sense signal input pin
RX28	In	Sense signal input pin
RX29	In	Sense signal input pin
RX30	In	Sense signal input pin
RX31	In	Sense signal input pin

Pin Description

Pin Name	Pin Attr	Description
INT	Out	Interrupt pin sending request to HOST
RESET#	In	Low active power on reset signal
Test1	PWR	External capacitor is required

C1P	PWR	Connect to external capacitor
C1N	PWR	Connect to external capacitor
C2P	PWR	Connect to external capacitor
C2N	PWR	Connect to external capacitor
C3P	PWR	Connect to external capacitor
C3N	PWR	Connect to external capacitor
C4P	PWR	Connect to external capacitor
C4N	PWR	Connect to external capacitor
HVDD	PWR	Connect to external capacitor
CHVDD	PWR	Connect to external capacitor

I2C Interface

Pin Name	Pin Attr	Description
I2C_CLK	In/Out	I2C serial clock input/output
I2C_DA	In/Out	I2C serial data input/output

GPIO Interface

Pin Name	Pin Attr	Description
GPIO1	In/Out	General purpose input/output port
GPIO2	In/Out	General purpose input/output port
GPIO3	In/Out	General purpose input/output port
GPIO4	In/Out	General purpose input/output port

UART Interface

Pin Name	Pin Attr	Description
UART_RX	In	Incoming Data from a master
UART_TX	Out	Outgoing Data to a slave

USB Interface

Pin Name	Pin Attr	Description
USBD+	In/Out	USB Data+
USBD-	In/Out	USB Data-
REXT	BIAS	4.7K ohm Pull Low

Power and Ground Signals

Name	Volt	Power Plane	Type Attr
OVDD	3.3V	MAIN	Digital
VSS	0V	GROUND	Digital
LVDD	3.3V	MAIN	Analog
LVSS	0V	GROUND	Analog
AVDD	3.3V	MAIN	Analog
AVSS	0V	GROUND	Analog

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 1 shows SIS9255 stress ratings only. Extended exposure to the maximum ratings might degrade device reliability. Although SIS9255 has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

Table 1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
Tstorage	Storage Temperature	-40	90	°C	
Ta	Ambient Operating Temperature	-20	85	°C	1
OVDD LVDD AVDD	3.3V Supply Voltage	-0.3	3.6	V	

NOTES:

1. The range of Ta means the normal operating under both active and idle mode.

5.2 DC Characteristics

OVDD=3.3V+/-5%, LVDD=3.3V+/-5%, AVDD=3.3V+/-5%,

AVSS=VSS=GND=0V,

Table 2 DC Characteristics of I/O Interface

Symbol	Parameter	Min	Max	Unit	Notes
VIH_TTL	TTL Input High Voltage	2	OVDD+0.3	V	1
VIL_TTL	TTL Input Low Voltage	-0.3	0.8	V	1
VOH_TTL	TTL Output High Voltage	0.9* OVDD		V	1
VOL_TTL	TTL Output Low Voltage		0.45	V	1
IOH_TTL	TTL Output High Current	-4		mA	1
IOL_TTL	TTL Output Low Voltage		4	mA	1

NOTES:

1. Parameter applies to following pins:
   GPIO[3:0], I2C_*, UART_*, INT and RESET#.

5.3 Packing Information

Table 3 Packing Info.

Not take off the seal (Al Bag)			Take off the seal (Al Bag)		
Preserved conditions		Storage life	General Preserved conditions		Storage life
Temperature	Humidity		Temperature	Humidity	
(℃)	(%RH)		(℃)	(%RH)	
0 ~ 40 ℃	＜ 90%RH	12 Months	25 ± 5 ℃	＜ 60%RH	168 Hours

6 Mechanical Dimension

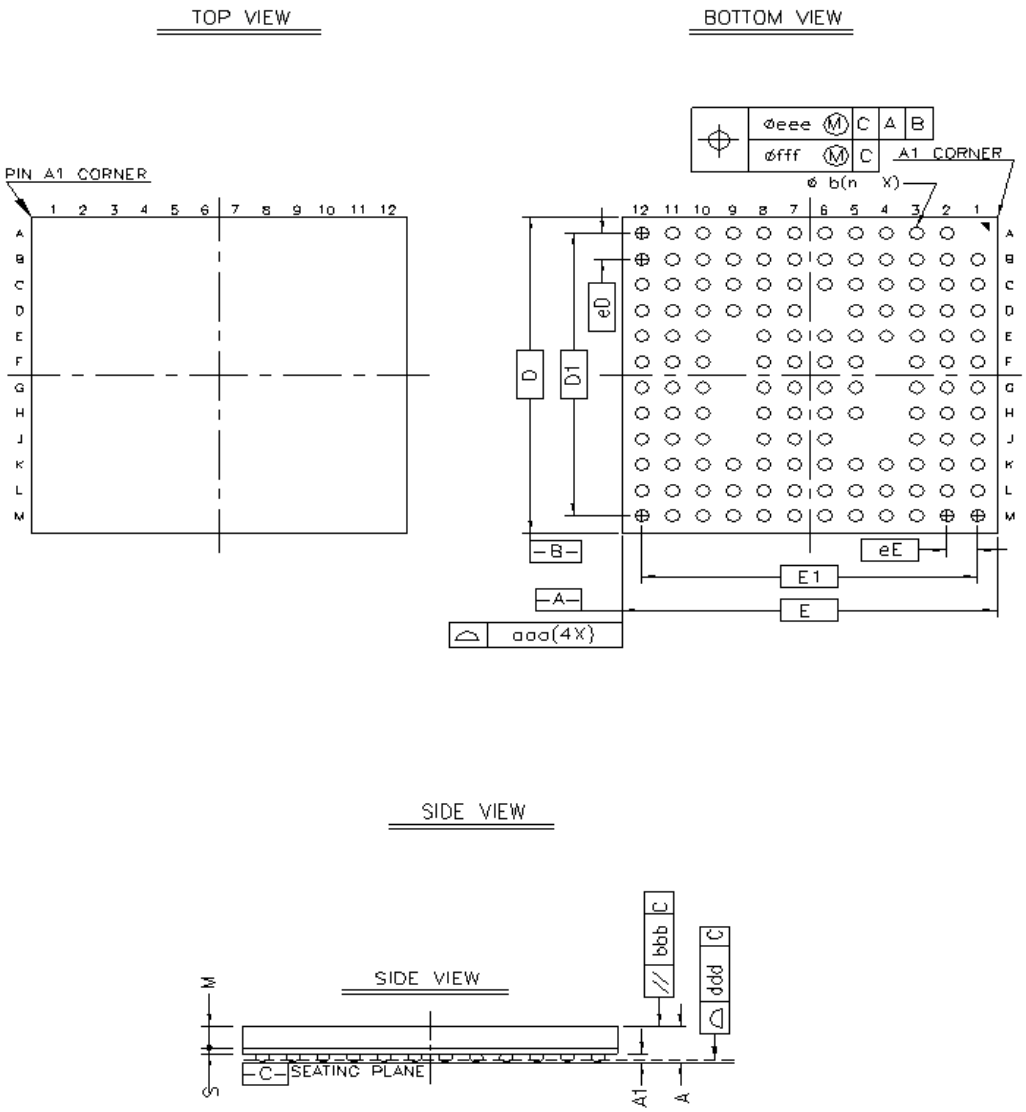


Table 4 Package Dimension

		Symbol	Common Dimensions
Package :			STK TFBGA
Body Size:	X	E	8.000
	Y	D	8.000
Ball Pitch :	X	eE	0.650
	Y	eD	0.650
Total Thickness :		A	0.91 ± 0.13 Typ.
Mold Thickness		M	0.530 Ref.
Substrate Thickness :		S	0.170 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.270 ~ 0.370
Package Edge Tolerance :		aaa	0.150
Mold Flatness		bbb	0.200
Coplanarity		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	132
Edge Ball Center to Center :	X	E1	7.150
	Y	D1	7.150

7 IC Marking Information

Topside Mark

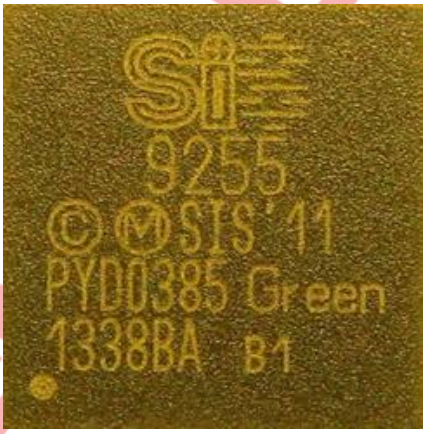
Logo

Part No. **9255**

Copyright ©Ⓜ**SiS'11**

XXXXXXX Green

ZZZZYY WW



Description

- **W :** Chip Version
- **X :** Lot No. (within 3 letters and 4 number)
- **Y :** Internal Control No.
- **Z :** Date Code

8 Serial Shipping Number

The serial shipping number will be shown on the shipping box as below. Normally, the serial shipping number shows in Figure 2.

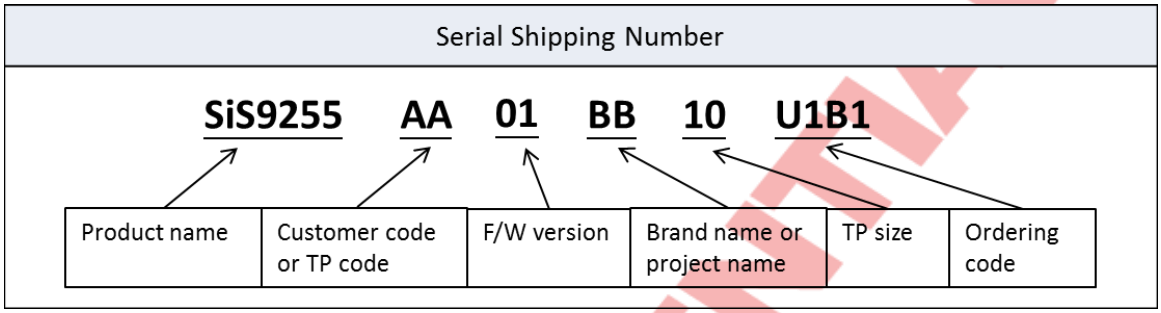


Figure2 Serial Shipping Number 1

If the same branding is using the same TP vendor but has many projects, the serial shipping number can be optionally used as below in Figure 3

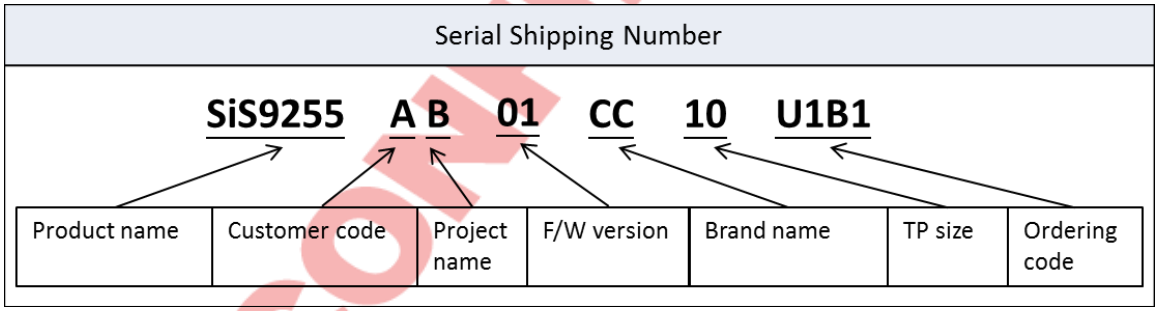


Figure 3 Serial Shipping Number 2

9 Copyright Notice

Trademarks

SiS is a registered trademark of Silicon Integrated Systems Corp.

All brand or product names mentioned are trademarks or registered trademarks of their respective holders.

Disclaimer

Silicon Integrated Systems Corp. makes no representations or warranties regarding the Contents of this manual. We reserve the right to revise the manual or make changes in the specifications of the product described within it at any time without notice and without obligation to notify any person of such revision or change. The information contained in this manual is provided for the general use by our customers. Our customers should be aware that the personal computer field is the subject of many patents. Our customers should ensure that they take appropriate action so that their use of our products does not infringe upon any patents. It is the policy of Silicon Integrated Systems Corp. to respect the valid patent rights of third parties and not to infringe upon or assist others to infringe upon such rights.

Restricted Rights Legend

Use, duplication, or disclosure by the Government is subject to restrictions set forth in subparagraph (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at 252.277-7013.