Application Note for FT5x16 CTPM

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Project name	Touch panel
Version	1.0
Release date	May 28,2012
Owner	J.H. Kuo
Classification	Confidential
Approval	

R3-B4-A, South Area, Shenzhen Hi-Tech Industrial Park,
Shenzhen, Guangdong, P.R. China
ZIP: 518057
T +86 755 26588222
F +86 755 26712499
E support@focaltech-systems.com

www.focaltech-systems.com

Revision History

Date	Version	List of changes	Author + Signature
May 28,2012	1.0	Initial draft.	J.H. Kuo

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Terminology

CTP – Capacitive touch panel

CTPM – Capacitive touch panel module

TX – Transmitter

RX – Receiver

1. CTPM interface to Host

Figure 1-1 shows how CTPM communicates with host device. I²C interface supported by FT5x16 that is two-wire serial bus consisting of data line SDA and SCL clock line, used for serial data transferring between host and slave device.

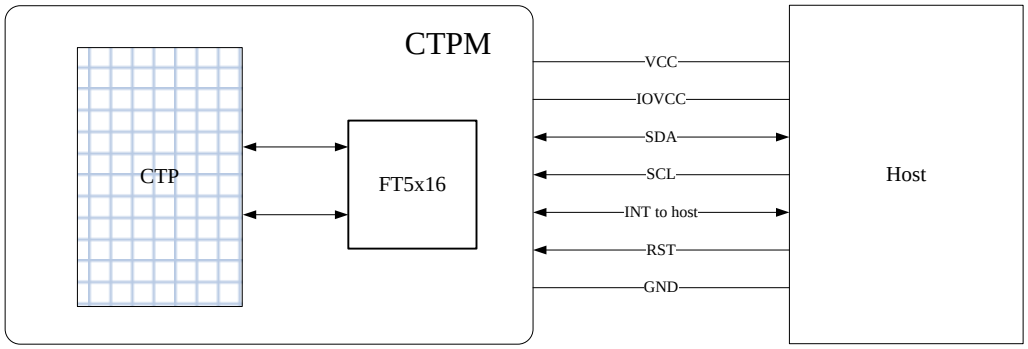


Figure 1-1 CTPM and Host connection

INT port and RST port form the control interface. The INT port controlled by FT5x16 will send out an interrupt request signal to the host when there is a valid touch on CTP. The INT port also has another input function that host can wake up FT5x16 from the Hibernate mode. Host can send the reset signal to CTPM via RST port to reset the FT5x16 if needed. The Power Supply voltage of CTPM ranges from 2.8V to 3.6V, and the interface supply voltage named IOVCC ranges from 1.8V to 3.6V. For details, please refer to Table 1-1.

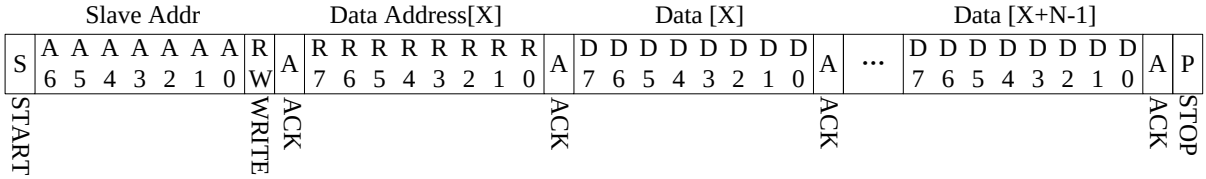
Table 1-1 Description for CTPM and Host interface

Port Name	Description
VCC	CTPM power supply, ranges from 2.8V to 3.6V.
IOVCC	CTPM interface power supply for digital I/O circuit, ranges from 1.8V to 3.6V.
SDA	I²C data input and output.
SCL	I²C clock input.
INT	The interrupt request signal from CTPM to Host. The wake up signal from host to CTPM, active low and the low pulse width ranges from 0.5ms to 1ms.
RST	The reset signal from host to CTPM, active low, and the low pulse width should be more than or equal to 1ms.
GND	Power ground.

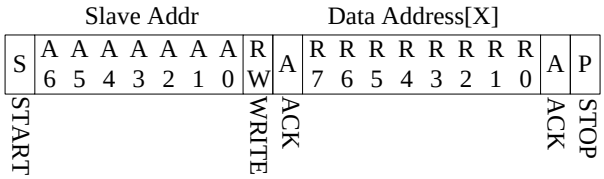
1.1 I²C Read/Write Interface description

It is important to note that the SDA and SCL must connect with a pull-high resistor respectively before you read/write I²C data.

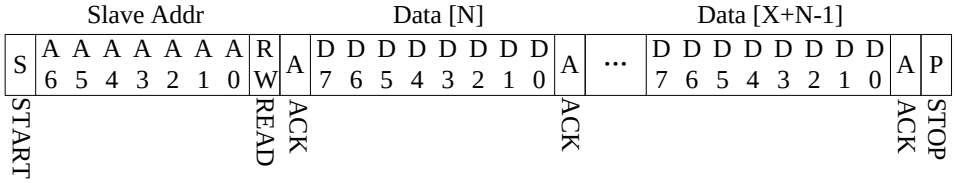
Write N bytes to I²C slave



Set Data Address



Read X bytes from I^{2}C Slave



1.2 Interrupt/Wake-up signal from CTPM to Host

As for standard CTPM, host needs to use both interrupt signal and I^{2}C interface to get the touch data. CTPM will output an interrupt request signal to the host when there is a valid touch. Then host can get the touch data via I^{2}C interface. If there is no valid touch detected, the INT will output high level, and the host does not need to read the touch data. There are two kinds of method to use interrupt: interrupt trigger and interrupt polling.

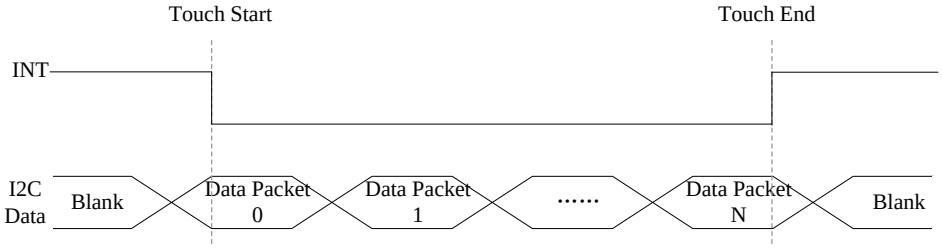


Figure 1-2 Interrupt polling mode

As for interrupt polling mode, INT will always be pulled to low level when there is a valid touch point, and be high level when a touch finished.

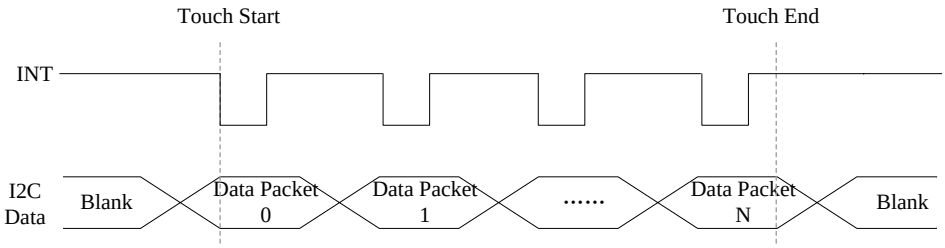


Figure 1-3 Interrupt trigger mode

While for interrupt trigger mode, INT signal will be set to low if there is a touch detected. But whenever an update of valid touch data, CTPM will produce a valid pulse on INT port for INT signal, and host can read the touch data periodically according to the frequency of this pulse. In this mode, the pulse frequency is the touch data updating rate.

When CTPM stays in hibernate mode, the INT port will act as a pull-high input port and wait for an

external wake up signal. Host may send out a low pulse to wake up CTPM from the hibernate mode. The wake-up low pulse width ranges from 0.5 ms to 1 ms, the reason for this is that the INT port will act as an interrupt request signal output port after wake-up.

1.3 Reset signal from Host to CTPM

Host can send the reset signal via RST port to reset FT5x16. The reset signal should not be set to low while in normal running mode, but when programming flash, the RST port must be connected to GND. The RST port can also be used to active the CTPM in hibernate mode. Note that the reset pulse width should be more than 1ms.

2. Standard Application circuit of FT5x16

Table 2-1 is a brief summary of the FT5x16 application features. Figure2-1, Figure2-2, demonstrates the typical FT5x16 application schematic respectively. It consists of Capacitive Touch Panel (CTP), FT5x16 chip, and some peripheral components. According to the size of CTPM, you can choose the number of channels needed.

Table 2-1 Brief features of FT5X16

IC Type	**FT5216GM7**	**FT5316DME**
Operating Voltage(V)	2.8 ~ 3.6	2.8 ~ 3.6
IOVCC(V)	1.8 ~ 3.6	1.8 ~ 3.6
Channel	16 TX + 10 RX	21 TX + 12 RX
Panel Size	<3.7”	3.7” ~ 5.0”
Touch points	5	5
Interface	I2C/SPI	I2C/SPI
Report rate	>60Hz	>60Hz
Package (mm)	5*5 QFN40	6*6 QFN48

2.1 FT5216GM7 typical application schematic for voltage of 2.8~3.6V

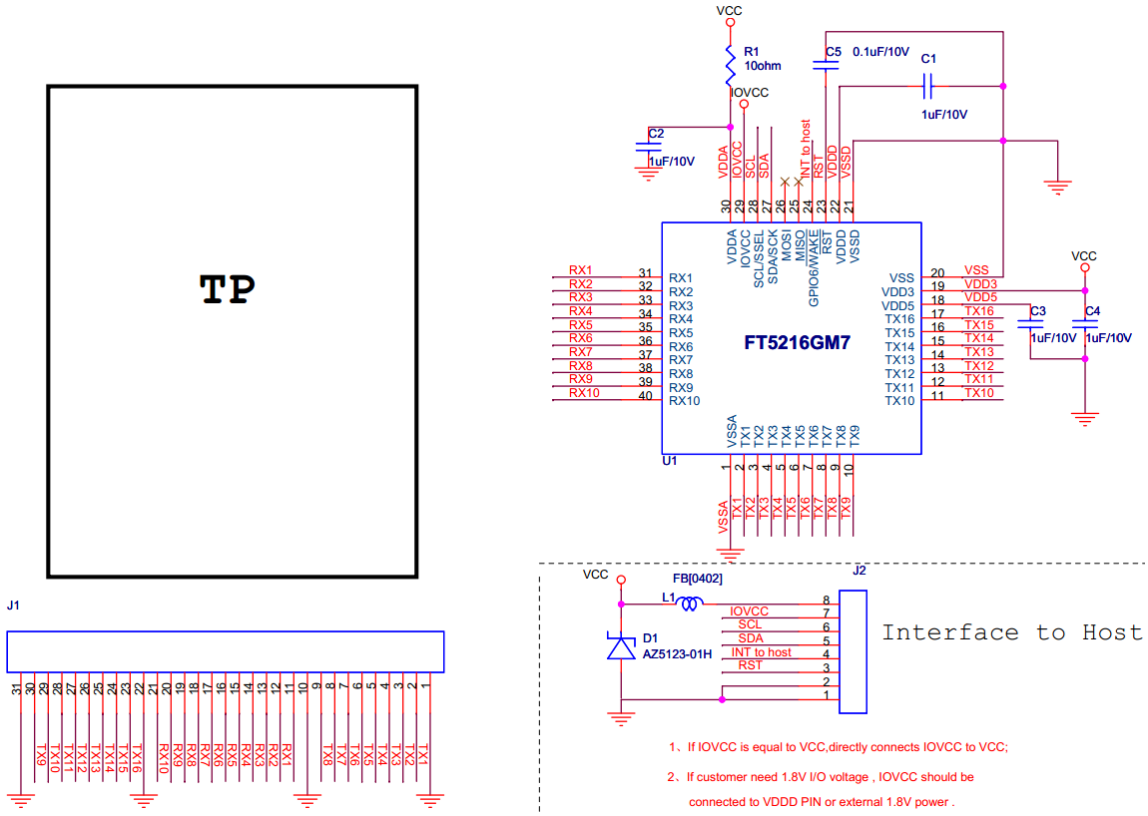


Figure 2-1 FT5216GM7 typical application schematic for voltage of 2.8~3.6V

2.2 FT5316DME typical application schematic for voltage of 2.8~3.6V

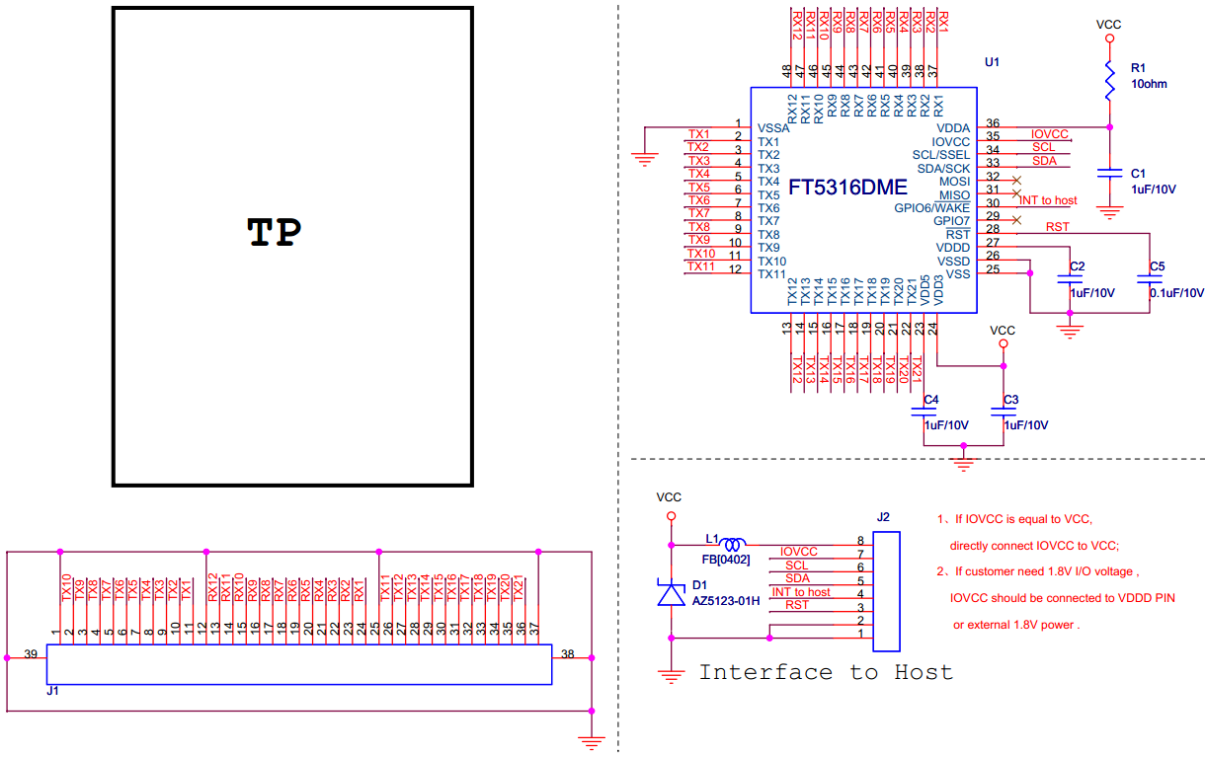


Figure 2-2 FT5316DME typical application schematic for voltage of 2.8~3.6V

3. CTPM Register Mapping

This chapter describes the standard CTPM communication registers in address order for operating mode. The most detailed descriptions of the standard products communication registers are in the register definitions section of each chapter.

3.1 Operating Mode

The CTP is fully functional as a touch screen controller in operating mode. The access address to read and write is just logical address which is not enforced by hardware or firmware. Here is the operating mode register map.

Operating Mode Register Map

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Host Access
Op,00h	DEVIDE_MODE		Device Mode[2:0]							RW
Op,01h	GEST_ID	Gesture ID[7:0]								R
Op,02h	TD_STATUS	Frame remaining or number of events (Win7 protocol)				Number of touch points[3:0]				R
Op,03h	TOUCH1_XH	1st Event Flag				1st Touch X Position[11:8]				R
Op,04h	TOUCH1_XL	1st Touch X Position[7:0]								R
Op,05h	TOUCH1_YH	1st Touch ID[3:0]				1st Touch Y Position[11:8]				R
Op,06h	TOUCH1_YL	1st Touch Y Position[7:0]								R
Op,07h	TOUCH1_WEIGHT	1st Touch Weight[7:0]								R
Op,08h	TOUCH1_MISC	1st Touch Area[3:0]				1st Touch Direction [1:0]		1st Touch Speed [1:0]		R
Op,09h	TOUCH2_XH	2nd Event Flag				2nd Touch X Position[11:8]				R
Op,0Ah	TOUCH2_XL	2nd Touch X Position[7:0]								R
Op,0Bh	TOUCH2_YH	2nd Touch ID[3:0]				2nd Touch Y Position[11:8]				R
Op,0Ch	TOUCH2_YL	2nd Touch Y Position[7:0]								R
Op,0Dh	TOUCH2_WEIGHT	2nd Touch Weight[7:0]								R
Op,0Eh	TOUCH2_MISC	2nd Touch Area[3:0]				2nd Touch Direction [1:0]		2nd Touch Speed [1:0]		R
Op,0Fh	TOUCH3_XH	3rd Event Flag				3rd Touch X Position[11:8]				R
Op,10h	TOUCH3_XL	3rd Touch X Position[7:0]								R
Op,11h	TOUCH3_YH	3rd Touch ID[3:0]				3rd Touch Y Position[11:8]				R
Op,12h	TOUCH3_YL	3rd Touch Y Position[7:0]								R
Op,13h	TOUCH3_WEIGHT	3rd Touch Weight[7:0]								R
Op,14h	TOUCH3_MISC	3rd Touch Area[3:0]				3rd Touch Direction [1:0]		3rd Touch Speed [1:0]		R
Op,15h	TOUCH4_XH	4th Event Flag				4th Touch X Position[11:8]				R
Op,16h	TOUCH4_XL	4th Touch X Position[7:0]								R
Op,17h	TOUCH4_YH	4th Touch ID[3:0]				4th Touch Y				R

			Position[11:8]		
Op,18h	TOUCH4_YL	4th Touch Y Position[7:0]			R
Op,19h	TOUCH4_WEIGHT	4th Touch Weight[7:0]			R
Op,1Ah	TOUCH4_MISC	4th Touch Area[3:0]	4thTouch Direction [1:0]	4thTouch Speed [1:0]	R
Op,1Bh	TOUCH5_XH	5thEvent Flag	5th Touch X Position[11:8]		R
Op,1Ch	TOUCH5_XL	5th Touch X Position[7:0]			R
Op,1Dh	TOUCH5_YH	5th Touch ID[3:0]	5th Touch Y Position[11:8]		R
Op,1Eh	TOUCH5_YL	5th Touch Y Position[7:0]			R
Op,1Fh	TOUCH5_WEIGHT	5th Touch Weight[7:0]			R
Op,20h	TOUCH5_MISC	5th Touch Area[3:0]	5thTouch Direction [1:0]	5thTouch Speed [1:0]	R
Op,21h	Reserved				
…	…				
Op,7Fh	Reserved				
Op,80h	ID_G_THGROUP	Valid touching detect threshold.			R/W
Op,81h	ID_G_THPEAK	Valid touching peak detect threshold.			R/W
Op,82h	ID_G_THCAL	The threshold when calculating the focus of touching.			R/W
Op,83h	ID_G_COMPENSATE_STATUS	This register describes status of compensation.			R
Op,84h	ID_G_COMPENSATE_FLAG	This register describes flag of compensation.			R
Op,85h	ID_G_THDIFF	The threshold whether the coordinate is different from the original			R/W
Op,86h	ID_G_CTRL			Power control mode[1:0]	R/W
Op,87h	ID_G_TIME_ENTER_MONITOR	The timer of entering monitor status			R/W
Op,88h	ID_G_PERIODACTIVE		Period Active[3:0]		R/W
Op,89h	ID_G_PERIODMONITOR	The timer of entering idle while in monitor status			R/W
Op,8Ah	ID_G_SCAN_RATE	This register describes rate of scan.			R
Op,8Bh	ID_G_CHARGER_STATE	This register describes state of charger.			R
Op,8Ch	ID_G_SCAN_REGB	This register describes REGB of scan.			R
Op,8Dh	ID_G_SCAN_CAP	This register describes cap of scan.			R
Op,8Eh	ID_G_SCAN_FILTERMODE	This register describes filter mode of scan.			R
Op,8Fh	ID_G_SCAN_REFRESH	This register describes flag of scan refresh.			R
Op,90h	ID_G_MOVSTH_I	This register describes state flag of move			R/W
Op,91h	ID_G_MOVSTH_N	This register describes state flag of move			R/W
Op,92h	ID_G_LEFT_RIGHT_OFFSET	Maximum of the distance of X axis of the valid move up, move down gesture.			R/W
Op,93h	ID_G_UP_DOWN_OFFSET	Maximum of the distance of Y axis of the valid move left, move right gesture.			R/W
Op,94h	ID_G_DISTANCE_LEFT_RIGHT	Minimum of the distance of X axis of the valid move left, move right gesture.			R/W
Op,95h	ID_G_DISTANCE_UP_DOWN	Minimum of the distance of Y axis of the valid move up, move down gesture.			R/W
Op,96h	Reserved				
Op,97h	ID_G_ZOOM_DIS_SQR	The threshold of valid Zoom In, Zoom Out gesture			R/W
Op,98h	ID_G_MAX_X_HIGH	maximum resolution of X axis high byte			R/W

Op,99h	ID_G_MAX_X_LOW	maximum resolution of X axis low byte	R/W
Op,9Ah	ID_G_MAX_Y_HIGH	maximum resolution of Y axis high byte	R/W
Op,9Bh	ID_G_MAX_Y_LOW	maximum resolution of Y axis low byte	R/W
Op,9Ch	ID_G_K_X_HIGH	the resolution coefficient of X axis high byte	R/W
Op,9Dh	ID_G_K_X_LOW	the resolution coefficient of X axis low byte	R/W
Op,9Eh	ID_G_K_Y_HIGH	the resolution coefficient of Y axis high byte	R/W
Op,9Fh	ID_G_K_Y_LOW	the resolution coefficient of Y axis low byte	R/W
Op,A0h	ID_G_AUTO_CLB_MODE	auto calibration mode	R/W
Op,A1h	ID_G_LIB_VERSION_H	Firmware Library Version H byte	R
Op,A2h	ID_G_LIB_VERSION_L	Firmware Library Version L byte	R
Op,A3h	ID_G_CIPHER	Chip vendor ID	R
Op,A4h	ID_G_MODE	the interrupt status to host	R
Op,A5h	ID_G_PMODE	Power Consume Mode	R
Op,A6h	ID_G_FIRMID	Firmware ID	R
Op,A7h	ID_G_STATE	Running State	R/W
Op,A8h	ID_G_VENODRID	CTPM Vendor ID	R
Op,A9h	ID_G_ERR	Error Code	R
Op,AAh	ID_G_CLB	Configure TP module during calibration in Test Mode	R/W
Op,ABh	ID_G_STATIC_TH	The threshold of touching static status	R/W
Op,ACh	ID_G_MID_SPEED_TH	The threshold of touching normal speed status	R/W
Op,ADh	ID_G_HIGH_SPEED_TH	The threshold of touching high speed status	R/W
Op,AEh	ID_G_DRAW_LINE_TH	The threshold of the maximum distance between two points	R/W
Op,AFh	ID_G_RELEASE_CODE_ID	This register describes the firmware release id of the application.	R
Op,B0h	ID_G_FACE_DEC_MODE	This register is used to configure the face detect mode of TPM	R/W
Op,B1h			
Op,B2h	ID_G_PRESIZE_EN	This register describes the pressure and size status to host	R/W
Op,B3h	ID_G_BIGAREA_PEAK_TH	This register is used to configure the min peak threshold value of the big area	R/W
Op,B4h	ID_G_BIGAREA_PEAK_NUM	This register is used to configure the min peak number value of the big area	R/W
…	…		
Op,FDh	Reserved		
Op,FEh	LOG_MSG_CNT	The log MSG count	R
Op,FFh	LOG_CUR_CHA	Current character of log message, will point to the next character when one character is read.	R

3.1.1 DEVICE_MODE

This is the device mode register, which is configured to determine the current mode of the chip.

Address	Bit Address	Register Name	Description
Op,00h	6:4	Device Mode [2:0]	000b Normal operating Mode 001b System Information Mode (Reserved) 100b FACTORY MODE0 (Reserved) 110b FACTORY MODE1 (Reserved)

3.1.2 GEST_ID

This register describes the gesture of a valid touch.

Address	Bit Address	Register Name	Description
Op,01h	7:0	Gesture ID[7:0]	Gesture ID 0x10 Move Up 0x14 Move Right 0x18 Move Down

			0x1C Move Left 0x48 Zoom In 0x49 Zoom Out 0x00 No Gesture

3.1.3 TD_STATUS

This register is the Touch Data status register.

Address	Bit Address	Register Name	Description
Op,02h	3:0	Number of touch points [3:0]	How many points detected. 1- 5 is valid.
	7:4	Frame remaining [7:4] or number of events	Frame remaining after host's reading (0-9 is valid) or number of events (1-5 is valid)

3.1.4 TOUCHn_XH (n:1-5)

This register describes MSB of the X coordinate of the nth touch point and the corresponding event flag.

Address	Bit Address	Register Name	Description
Op,03h ~ Op,1Bh	7:6	Event Flag	00b: Press Down 01b: Lift Up 10b: Contact 11b: No event
	5:4		Reserved
	3:0	Touch X Position [11:8]	MSB of Touch X Position in pixels

3.1.5 TOUCHn_XL (n:1-5)

This register describes LSB of the X coordinate of the nth touch point.

Address	Bit Address	Register Name	Description
Op,04h ~ Op,1Ch	7:0	Touch X Position [7:0]	LSB of the Touch X Position in pixels

3.1.6 TOUCHn_YH (n:1-5)

This register describes MSB of the Y coordinate of the nth touch point and corresponding touch ID.

Address	Bit Address	Register Name	Description
Op,05h ~ Op,1Dh	7:4	Touch ID[3:0]	Touch ID of Touch Point (0-4 is valid)
	3:0	Touch Y Position [11:8]	MSB of Touch Y Position in pixels

3.1.7 TOUCHn_YL (n:1-5)

This register describes LSB of the Y coordinate of the nth touch point.

Address	Bit Address	Register Name	Description
Op,06h ~ Op,1Eh	7:0	Touch Y Position [7:0]	LSB of the Touch Y Position in pixels

3.1.8 TOUCHn_ WEIGHT (n:1-5)

This register describes weight of the nth touch point.

Address	Bit Address	Register Name	Description
Op,07h ~ Op,1Fh	7:0	Touch Weight[7:0]	The value of touch Weight

3.1.9 TOUCHn_ MISC (n:1-5)

This register describes the miscellaneous information of the nth touch point.

Address	Bit Address	Register Name	Description
Op,08h	7:4	Touch Area[7:4]	The valid touching area
~	3:2	Touch Direction	0: up

Op,20h			1:down 2:left 3:right
	1:0	Touch Speed	0: static 1: normal speed 2: high speed

3.1.10 ID_G_THGROUP

This register describes valid touching detect threshold.

Address	Bit Address	Register Name	Description
Op,80h	7:0	ID_G_THGROUP	The actual value will be 4 times of the register's value. Default: 120/4

3.1.11 ID_G_THPEAK

This register describes valid touching peak detect threshold.

Address	Bit Address	Register Name	Description
Op,81h	7:0	ID_G_ THPEAK	Default: 60

3.1.12 ID_G_THCAL

This register describes threshold when calculating the focus of touching.

Address	Bit Address	Register Name	Description
Op,82h	7:0	ID_G_THCAL	Default: 16

3.1.13 ID_G_ COMPENSATE_STATUS

This register describes status of compensation.

Address	Bit Address	Register Name	Description
Op,83h	7:0	ID_G_ COMPENSATE_STATUS	Default: 0

3.1.14 ID_G_COMPENSATE_FLAG

This register describes flag of compensation.

Address	Bit Address	Register Name	Description
Op,84h	7:0	ID_G_COMPENSATE_FLAG	Default: 6

3.1.15 ID_G_THDIFF

This register describes threshold whether the coordinate is different from the original.

Address	Bit Address	Register Name	Description
Op,85h	7:0	ID_G_ THDIFF	The actual value must be 16 times of the register's value. Default : 128

3.1.16 ID_G_CTRL

This register describes the running mode of microcontroller controlled by host.

Address	Bit Address	Register Name	Description
Op,86h	7:0	ID_G_CTRL	0: monitor disabled 1: monitor enabled

3.1.17 ID_G_TIMEENTERMONITOR

This register describes the time delay value when entering monitor status.

Address	Bit Address	Register Name	Description
Op,87h	7:0	ID_G_TIMEENTERMONITOR	Default: 10

3.1.18 ID_G_PERIODACTIVE

This register describes the period of active status, it should be less than 15.

Address	Bit Address	Register Name	Description
Op,88h	7:0	ID_G_PERIODACTIVE	Report rate. Ranges from 3 to 14, default 6

			(60Hz).

3.1.19 ID_G_PERIODMONITOR

This register describes period of monitor status, it should not be less than 20.

Address	Bit Address	Register Name	Description
Op,89h	7:0	ID_G_PERIODMONITOR	Default: 20

3.1.20 ID_G_SCAN_RATE

This register describes rate of scan.

Address	Bit Address	Register Name	Description
Op,8Ah	7:0	ID_G_SCAN_RATE	Default: 2

3.1.21 ID_G_CHARGER_STATE

This register describes state of charger.

Address	Bit Address	Register Name	Description
Op,8Bh	7:0	ID_G_CHARGER_STATE	State of charger. Default: 1

3.1.22 ID_G_SCAN_REGB

This register describes REGB of scan.

Address	Bit Address	Register Name	Description
Op,8Ch	7:0	ID_G_SCAN_REGB	The REGB of scan.

3.1.23 ID_G_SCAN_CAP

This register describes Cap of scan.

Address	Bit Address	Register Name	Description
Op,8Dh	7:0	ID_G_SCAN_CAP	Default: xx

3.1.24 ID_G_SCAN_FILTER_MODE

This register describes filter mode of scan.

Address	Bit Address	Register Name	Description
Op,8Eh	7:0	ID_G_SCAN_FILTER_MODE	Default: xx

3.1.25 ID_G_SCAN_REFRESH

This register describes flag of scan refresh.

Address	Bit Address	Register Name	Description
Op,8Fh	7:0	ID_G_SCAN_REFRESH	Default: 0

3.1.26 ID_G_MOVSTH_I

This register describes state flag of move.

Address	Bit Address	Register Name	Description
Op,90h	7:0	ID_G_MOVSTH_I	Default: 2

3.1.27 ID_G_MOVSTH_N

This register describes state flag of move.

Address	Bit Address	Register Name	Description
Op,91h	7:0	ID_G_MOVSTH_N	Default: 1

3.1.28 ID_G_LEFT_RIGHT_OFFSET

This register is only used in the mode of continuous reporting gesture to host while valid gesture produced.

Address	Bit Address	Register Name	Description
Op,92h	7:0	ID_G_LEFT_RIGHT_OFFSET	The maximum distance on X axis to produce Up, Down gesture. Default: 50

3.1.29 ID_G_UP_DOWN_OFFSET

This register is only used in the mode of continuous reporting gesture to host while valid gesture produced.

Address	Bit Address	Register Name	Description
Op,93h	7:0	ID_G_UP_DOWN_OFFSET	The maximum distance on Y axis to produce Left, Right gesture. Default: 50

3.1.30 ID_G_DISTANCE_LEFT_RIGHT

This register is only used in the mode of continuous reporting gesture to host while valid gesture produced.

Address	Bit Address	Register Name	Description
Op,94h	7:0	ID_G_DISTANCE_LEFT_RIGHT	The minimum distance on X axis to produce Left, Right gesture. Default: 50

3.1.31 ID_G_DISTANCE_UP_DOWN

This register is only used in the mode of continuous reporting gesture to host while valid gesture produced.

Address	Bit Address	Register Name	Description
Op,95h	7:0	ID_G_DISTANCE_UP_DOWN	The minimum distance on Y axis to produce Up, Down gesture. Default: 50

3.1.32 ID_G_ZOOM_DIS_SQR

This register describes minimum square of distance while zoom in or out used in both reporting mode.

Address	Bit Address	Register Name	Description
Op,97h	7:0	ID_G_ZOOM_DIS_SQR	The minimum distance to produce Zoom In or Out used in both reporting mode.

3.1.33 ID_G_MAX_X_HIGH

This register describes the resolution of X axis high byte.

Address	Bit Address	Register Name	Description
Op,98h	7:0	ID_G_MAX_X_HIGH	MSB of the resolution of X axis.

3.1.34 ID_G_MAX_X_LOW

This register describes the resolution of X axis low byte.

Address	Bit Address	Register Name	Description
Op,99h	7:0	ID_G_MAX_X_LOW	LSB of the resolution of X axis.

3.1.35 ID_G_MAX_Y_HIGH

This register describes the resolution of Y axis high byte.

Address	Bit Address	Register Name	Description
Op,9Ah	7:0	ID_G_MAX_Y_HIGH	MSB of the resolution of Y axis.

3.1.36 ID_G_MAX_Y_LOW

This register describes the resolution of Y axis low byte.

Address	Bit Address	Register Name	Description
Op,9Bh	7:0	ID_G_MAX_Y_LOW	LSB of the resolution of Y axis.

3.1.37 ID_G_K_X_HIGH

This register describes the resolution coefficient of X axis high byte.

Address	Bit Address	Register Name	Description
Op,9Ch	7:0	ID_G_K_X_HIGH	MSB of the resolution coefficient of X axis.

3.1.38 ID_G_K_X_LOW

This register describes the resolution coefficient of X axis low byte.

Address	Bit Address	Register Name	Description
Op,9Dh	7:0	ID_G_K_X_LOW	LSB of the resolution coefficient of X axis

3.1.39 ID_G_K_Y_HIGH

This register describes the resolution coefficient of Y axis high byte.

Address	Bit Address	Register Name	Description

Op,9Eh	7:0	ID_G_K_Y_HIGH	MSB of the resolution coefficient of Y axis

3.1.40 ID_G_K_Y_LOW

This register describes the resolution coefficient of Y axis low byte.

Address	Bit Address	Register Name	Description
Op,9Fh	7:0	ID_G_K_Y_LOW	LSB of the resolution coefficient of Y axis

3.1.41 ID_G_AUTO_CLB_MODE

This register describes auto calibration mode.

Address	Bit Address	Register Name	Description
Op,A0h	7:0	ID_G_AUTO_CLB_MODE	8'h00: enable auto calibration 8'hff: disable auto calibration

3.1.42 ID_G_LIB_VERSION_H

This register describes library version high byte.

Address	Bit Address	Register Name	Description
Op,A1h	7:0	ID_G_LIB_VERSION_H	R: xx

3.1.43 ID_G_LIB_VERSION_L

This register describes library version low byte.

Address	Bit Address	Register Name	Description
Op,A2h	7:0	ID_G_LIB_VERSION_L	R: xx

3.1.44 ID_G_CIPHER

This register describes vendor's chip id.

Address	Bit Address	Register Name	Description
Op,A3h	7:0	ID_G_CIPHER	R: 0x0a

3.1.45 ID_G_MODE

This register describes the interrupt status to host.

Address	Bit Address	Register Name	Description
Op,A4h	7:0	ID_G_MODE	0: Polling mode 1: Trigger mode

3.1.46 ID_G_PMODE

This register describes the power consumption mode of the CTPM when in running status.

Address	Bit Address	Register Name	Description
Op,A5h	7:0	ID_G_PMODE	0: active 1: monitor 3: hibernate(deep sleep)

3.1.47 ID_G_FIRM_ID

This register describes the firmware id of the application.

Address	Bit Address	Register Name	Description
Op,A6h	7:0	ID_G_FIRM_ID	R: 0x06

3.1.48 ID_G_STATE

This register is used to configure the running mode of CTPM.

Address	Bit Address	Register Name	Description
Op,A7h	7:0	ID_G_STATE	0: configure 1: work 2: calibration 3: factory 4: auto calibration

3.1.49 ID_G_VENODRID

This register describes vendor's chip id

Address	Bit Address	Register Name	Description
Op,A8h	7:0	ID_G_VENODRID	R: 0x79

3.1.50 ID_G_ERR

This register describes the error code when the CTPM is running.

Address	Bit Address	Register Name	Description
Op,A9h	7:0	ID_G_ERR	ERR Code 8'h01: OK 8'h03: chip register writing inconsistent with reading 8'h05: chip start fail 8'h1A: no match among the basic input(such as TX_ORDER) while calibration

3.1.51 ID_G_CLB

This register is used to configure the TPM when Calibration

Address	Bit Address	Register Name	Description
Op,AAh	7:0	ID_G_CLB	Mapping the Array of G_Bank1, total length is NUM_TX+NUM_RX+1. The array address increases 1 after every write.

3.1.52 ID_G_STATIC_TH

This register is used to configure the static rate threshold value.

Address	Bit Address	Register Name	Description
Op,ABh	7:0	ID_G_STATIC_TH	Auto report rate: static rate threshold value.

3.1.53 ID_G_MID_SPEED_TH

This register is used to configure the mid speed rate threshold value

Address	Bit Address	Register Name	Description
Op,ACh	7:0	ID_G_MID_SPEED_TH	Auto report rate: mid_speed rate threshold value.

3.1.54 ID_G_HIGH_SPEED_TH

This register is used to configure the high speed rate threshold value.

Address	Bit Address	Register Name	Description
Op,ADh	7:0	ID_G_HIGH_SPEED_TH	Auto report rate: high speed rate threshold value.

3.1.55 ID_G_DRAW_LINE_TH

This register is used to configure the maximum distance between two points when drawing line.

Address	Bit Address	Register Name	Description
Op,AEh .	7:0	ID_G_DRAW_LINE_TH	The maximum distance between two points when drawing line, the bigger, the drawing speed faster

3.1.56 ID_G_RELEASE_CODE_ID

Address	Bit Address	Register Name	Description
Op,AFh	7:0	ID_G_RELEASE_CODE_ID	R:0x01

3.1.57 ID_G_FACE_DEC_MODE

This register is used to configure the face detect mode of CTPM

Address	Bit Address	Register Name	Description
Op,B0h	7:0	ID_G_FACE_DEC_MODE	R:xx

3.1.58 ID_G_PRESIZE_EN

This register describes the pressure and size status to host.

Address	Bit Address	Register Name	Description
Op,B2h	7:0	ID_G_PRESIZE_EN	0: enable to host 1: disable to host

3.1.59 ID_G_BIGAREA_PEAK_TH

This register is used to configure the min peak threshold value of the big area

Address	Bit Address	Register Name	Description
Op,B3h	7:0	ID_G_BIGAREA_PEAK_TH	The min value to be decided as the big point Default: 100

3.1.60 ID_G_BIGAREA_PEAK_NUM

This register is used to configure the min peak number value of the big area

Address	Bit Address	Register Name	Description
Op,B4h	7:0	ID_G_BIGAREA_PEAK_NUM	The min value big point of the big area Default: 50

4. Communication between host and CTPM

4.1 Communication Contents

The data Host received from the CTPM through I^2C interface are different depend on the configuration in Device Mode Register of the CTPM. Please refer to Section 3---CTPM Register Mapping.

4.2 I^2C Example Code

```
//////////////////////////////////////////////////////////////////
// I2C write bytes to device.
//
// Arguments: ucSlaveAdr - slave address
//                    ucSubAdr - sub address
//                    pBuf - pointer of buffer
//                    ucBufLen - length of buffer
//////////////////////////////////////////////////////////////////
void i2cBurstWriteBytes(BYTE ucSlaveAdr, BYTE ucSubAdr, BYTE *pBuf, BYTE ucBufLen)
{
    BYTE ucDummy; // loop dummy
    ucDummy = I2C_ACCESS_DUMMY_TIME;
    while(ucDummy--)
    {
        if (i2c_AccessStart(ucSlaveAdr, I2C_WRITE) == FALSE)
            continue;
        if (i2c_SendByte(ucSubAdr) == I2C_NON_ACKNOWLEDGE) // check non-acknowledge
            continue;
        while(ucBufLen--) // loop of writting data
        {
            i2c_SendByte(*pBuf); // send byte
            pBuf++; // next byte pointer
        } // while
        break;
```

```
    } // while
    i2c_Stop();
}

//////////////////////////////////////////////////////////////////
// I2C read bytes from device.
//
// Arguments: ucSlaveAdr - slave address
//                    ucSubAdr - sub address
//                    pBuf - pointer of buffer
//                    ucBufLen - length of buffer
//////////////////////////////////////////////////////////////////
void i2cBurstReadBytes(BYTE ucSlaveAdr, BYTE ucSubAdr, BYTE *pBuf, BYTE ucBufLen)
{
    BYTE ucDummy; // loop dummy

    ucDummy = I2C_ACCESS_DUMMY_TIME;
    while(ucDummy--)
    {
        if (i2c_AccessStart(ucSlaveAdr, I2C_WRITE) == FALSE)
            continue;
        if (i2c_SendByte(ucSubAdr) == I2C_NON_ACKNOWLEDGE) // check non-acknowledge
            continue;
        if (i2c_AccessStart(ucSlaveAdr, I2C_READ) == FALSE)
            continue;
        while(ucBufLen--) // loop to burst read
        {
            *pBuf = i2c_ReceiveByte(ucBufLen); // receive byte
            pBuf++; // next byte pointer
        } // while
        break;
    } // while
    i2c_Stop();
}

//////////////////////////////////////////////////////////////////
// I2C read current bytes from device.
//
// Arguments: ucSlaveAdr - slave address
//                pBuf - pointer of buffer
//                ucBufLen - length of buffer
//////////////////////////////////////////////////////////////////
void i2cBurstCurrentBytes(BYTE ucSlaveAdr, BYTE *pBuf, BYTE ucBufLen)
{
```

```
    BYTE ucDummy; // loop dummy

    ucDummy = I2C_ACCESS_DUMMY_TIME;
    while(ucDummy--)
    {
        if (i2c_AccessStart(ucSlaveAdr, I2C_READ) == FALSE)
            continue;
        while(ucBufLen--) // loop to burst read
        {
            *pBuf = i2c_ReceiveByte(ucBufLen); // receive byte
            pBuf++; // next byte pointer
        } // while
        break;
    } // while
    i2c_Stop();
}
```