FT7311

True Multi-Touch Capacitive Touch Panel Controller

INTRODUCTION

The FT7311 is single-chip capacitive touch panel controllers with built-in enhanced Micro-controller unit (MCU).It provides the benefits of full screen common mode scan technology, fast response time and high level of accuracy. It can drive capacitive type touch panel with up to 15 driving and 24 sensing lines.

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- FT7311 Supports up to 15TX + 24 RX
- Support up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor, Sleep)
- Support >100Hz sampling rate
- Auto-calibration
- Support IIC (up to 400kbits/sec) interface
- Power
  - 2.7 to 3.6V Operating Voltage
  - IOVCC supports from 1.71V to 3.6V
- Built-in 64KB Flash
- Single Channel(TX or RX)resistance: Up to 100K Ω
- Single Channel (transmit/receive) Capacitance: 40pF
- 12-Bit ADC Accuracy
- Features “short I/O ” testing for sense pins
- Supports various type of panels with no ground shielding layer
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -40°C to +85°C
- ESD : HBM +/- 3KV, , CDM +/- 850V
- Life cycle guarantee 5+
- Package:
  - QFN56L 6x6x0.6mm, 0.35mm/pitch

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1 OVERVIEW

1.1 Typical Applications

FT7311 provides a wide range of applications with a set of buttons up to a 2D touch sensing device. It's powerful design for below applications.

- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable media players
- Digital cameras

FT7311 support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Smart Phone TP Size (16:9)
FT7311 DQQ	QFN 56L 6x6x0.6mm Pitch =0.35mm	15	24	39	≤5.5", Sensor Pitch:5mm

2 FUNCTIONAL BLOCK DESCRIPTIONS

2.1 Architecture Overview

Figure2-1 shows the architecture of FT7311.

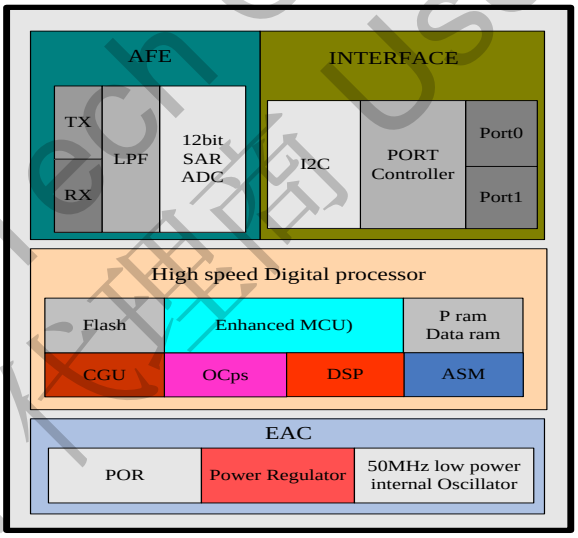


Figure 2-1 System Architecture Diagram

The FT7311 has five main functional parts below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.
Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches

reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT7311 from the Sleep mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.5V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.

2.2 MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

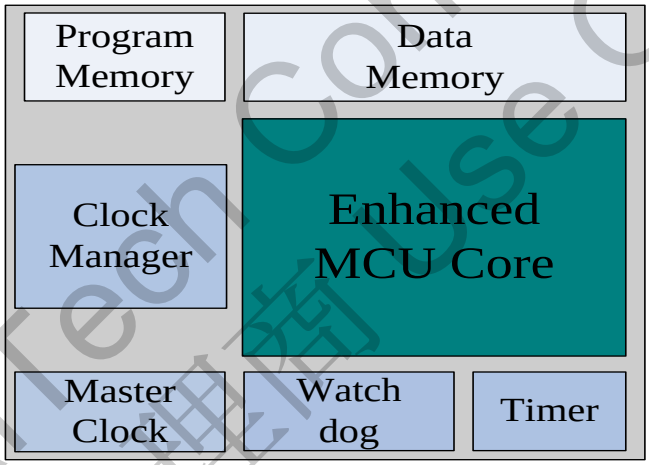


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT7311 offers following three modes:

- **Active Mode**

In active mode, the frame scan rate is 0~120Hz.The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT7311 shall enter the Active mode immediately. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In Sleep mode, it shall only respond to the “RESET”, “INT” signal from the host processor.

2.4 Host Interface

Figure 2-3 shows the interface between a host processor and FT7311. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT7311 to the Host

- Reset Signal from the Host to FT7311

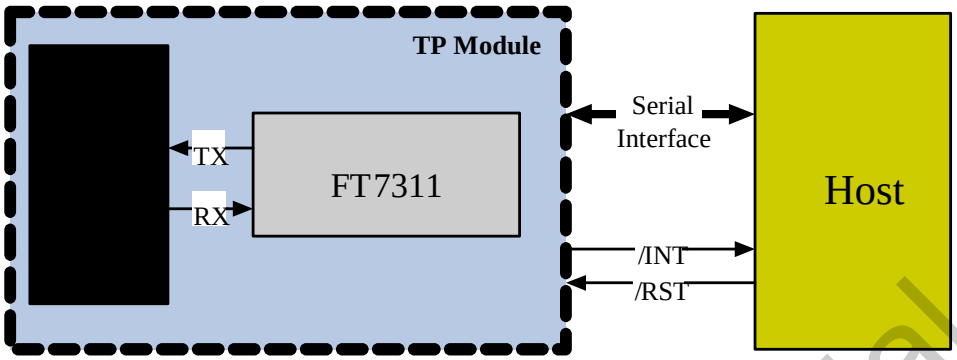


Figure 2-3 Host Interface Diagram

The serial interface of FT7311 is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT7311 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT7311 from the Sleep mode. After resetting, FT7311 shall enter the Active mode.

2.5 Serial Interface

FT7311 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

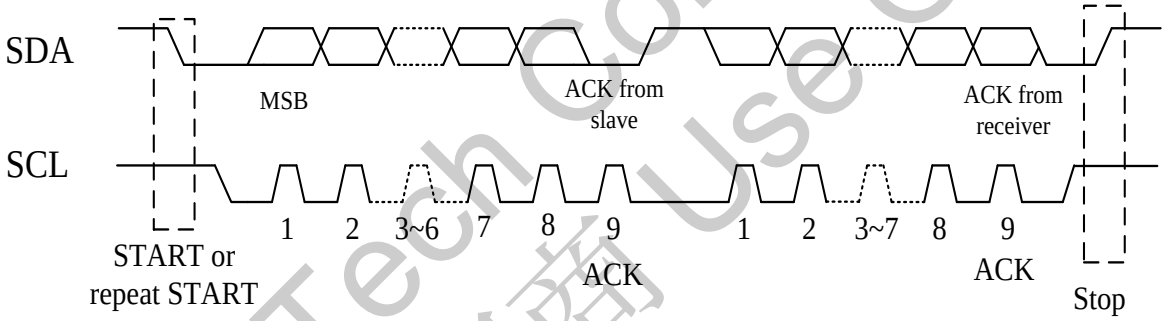


Figure 2-4 I2C Serial Data Transfer Format

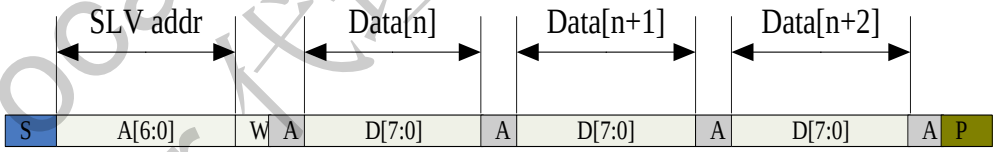


Figure 2-5 I2C master write, slave read

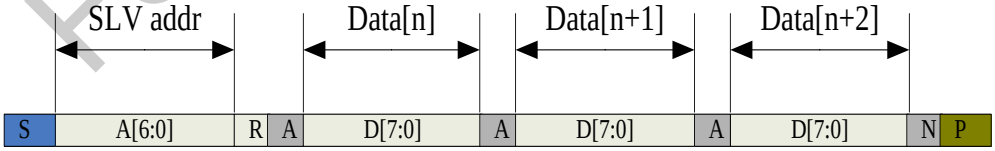


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup time for STOP condition	0.6		us
Rise time of both SDA and SCL signals	20	300	ns
Fall time of both SDA and SCL signals	20x (VDD/5.5V)	300	ns

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.7 ~ 3.6	V	1
I/O Digital Voltage	IOVCC	1.71~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT7311 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD3 (high) ≥VSSLF (low)

3.2 DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low –level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high –level voltage	VOH	V	IOH=3mA	0.7 x IOVCC	--	--	
Output low –level voltage	VOL	V	IOL=4.5mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption （Normal operation mode）	Ioprr	mA	VDD3 = 3V Ta=25℃	--	11	--	
Current consumption （Monitor mode）	Imon	mA	VDD3 = 3V Ta=25℃	--	0.43	--	
Current consumption （Sleep mode）	Islp	uA	VDD3 = 3V Ta=25℃	--	42	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Step-up output voltage	VDD10	V	VDD3= 2.8V		0.5		
Output voltage	VDD5	V	VDD3= 2.8V	5		6.25	
Output voltage	VDD10	V	VDD3= 2.8V	7		11.5	
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This sample data is intended for design guidance only. Values shown are typical for a 15Tx × 24Rx sensor configured at 80 Hz report rate.Actual current will depend on the particular sensor design and firmware options.

3.3 AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25℃	49	50	51	

Table 3-3 AC Characteristics of TX & RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	
TX output rise time	Ttxr		--	210	--	nS	
TX output fall time	Ttxf		--	210	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

3.4 **I/O Ports Circuits**

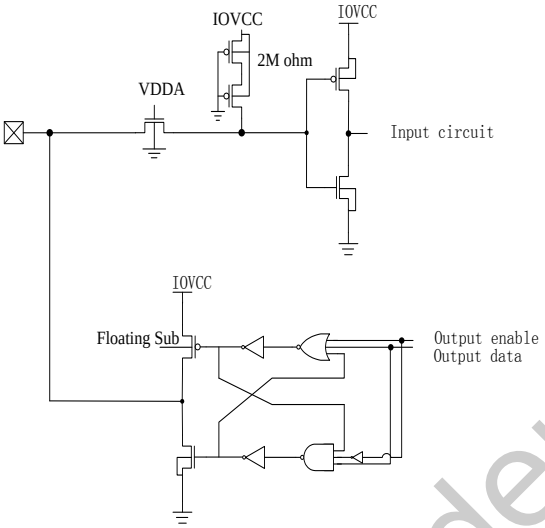


Figure 3-1 General Purpose *In/Out Port Circuit*.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

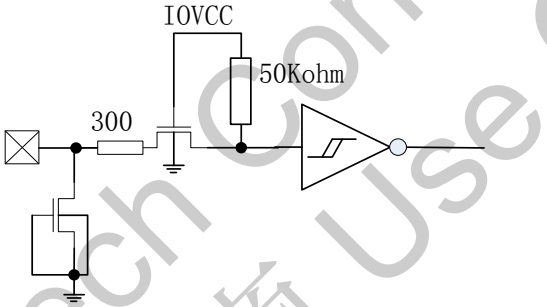


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

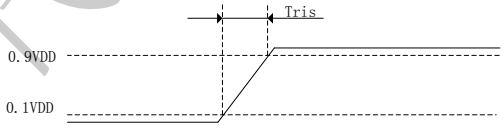


Figure 3-3 Power on time

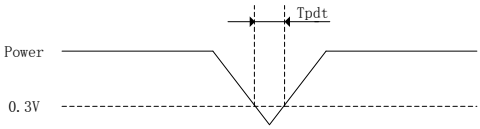


Figure 3-4 Power Cycle requirement

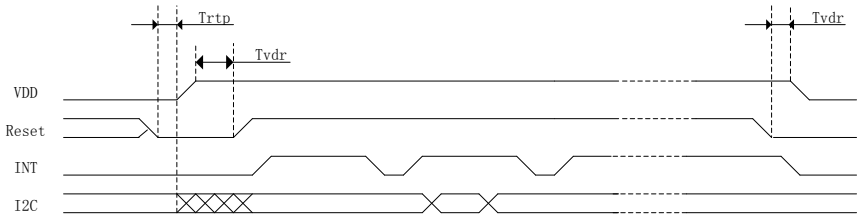


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

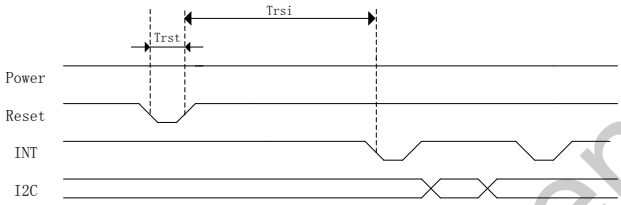


Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

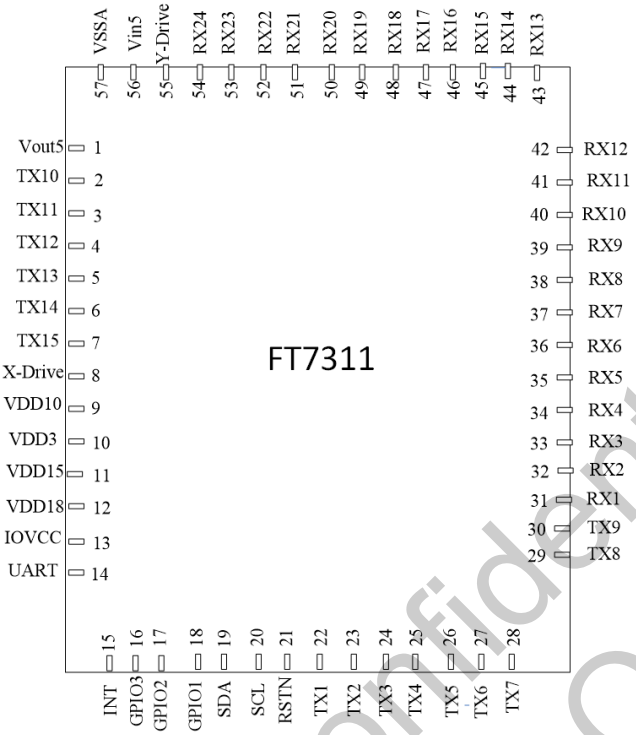
4 PIN CONFIGURATIONS

Pin List of FT7311

Table 4-1 Pin Definition

Name	Type	Description	
	FT7311		
RX24	54	I	Receiver input pins
RX23	53	I	Receiver input pins
RX22	52	I	Receiver input pins
RX21	51	I	Receiver input pins
RX20	50	I	Receiver input pins
RX19	49	I	Receiver input pins
RX18	48	I	Receiver input pins
RX17	47	I	Receiver input pins
RX16	46	I	Receiver input pins
RX15	45	I	Receiver input pins
RX14	44	I	Receiver input pins
RX13	43	I	Receiver input pins
RX12	42	I	Receiver input pins
RX11	41	I	Receiver input pins
RX10	40	I	Receiver input pins
RX9	39	I	Receiver input pins
RX8	38	I	Receiver input pins
RX7	37	I	Receiver input pins
RX6	36	I	Receiver input pins
RX5	35	I	Receiver input pins
RX4	34	I	Receiver input pins
RX3	33	I	Receiver input pins
RX2	32	I	Receiver input pins
RX1	31	I	Receiver input pins
VDD5_IN	56	PWR	internal generated 5V power supply, A 1μF ceramic capacitor to ground is required.
VSSLF	57	PWR	Analog ground
VDD5_Out	1	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
X-Drive	8	NC	
Y-Drive	55	NC	
TX10	2	O	Transmit output pin
TX11	3	O	Transmit output pin
TX12	4	O	Transmit output pin
TX13	5	O	Transmit output pin
TX14	6	O	Transmit output pin
TX15	7	O	Transmit output pin
VDD10	9	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD3	10	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.

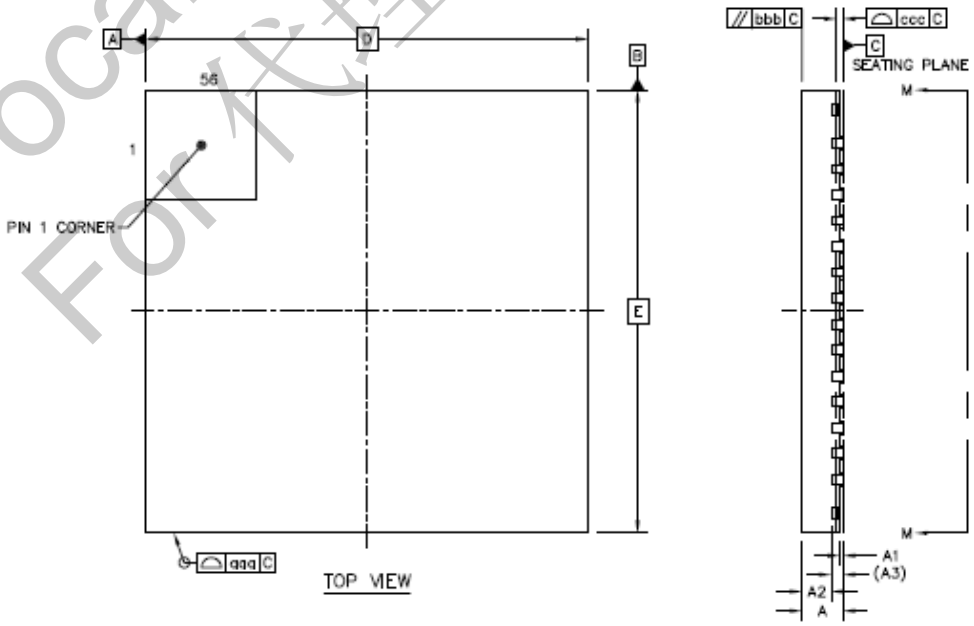
VDD15	11	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
VDD18	12	PWR	digital power supply, A 1μF ceramic capacitor to ground is required.
IOVCC	13	PWR	I/O power supply
INT	15	I/O	Interrupt request to the host, or Wakeup request from the host.
UART	14	I/O	UART port
GPIO1	18	I/O	General Purpose Input/Output port Support PS2_CLK
GPIO2	17	I/O	General Purpose Input/Output port Support PS2_Data
GPIO3	16	I/O	General Purpose Input/Output port
SDA	19	I/O	I2C data input and output
SCL	20	I/O	I2C clock input
RSTN	21	I	External Reset, Low is active
TX1	22	O	Transmit output pin
TX2	23	O	Transmit output pin
TX3	24	O	Transmit output pin
TX4	25	O	Transmit output pin
TX5	26	O	Transmit output pin
TX6	27	O	Transmit output pin
TX7	28	O	Transmit output pin
TX8	29	O	Transmit output pin
TX9	30	O	Transmit output pin

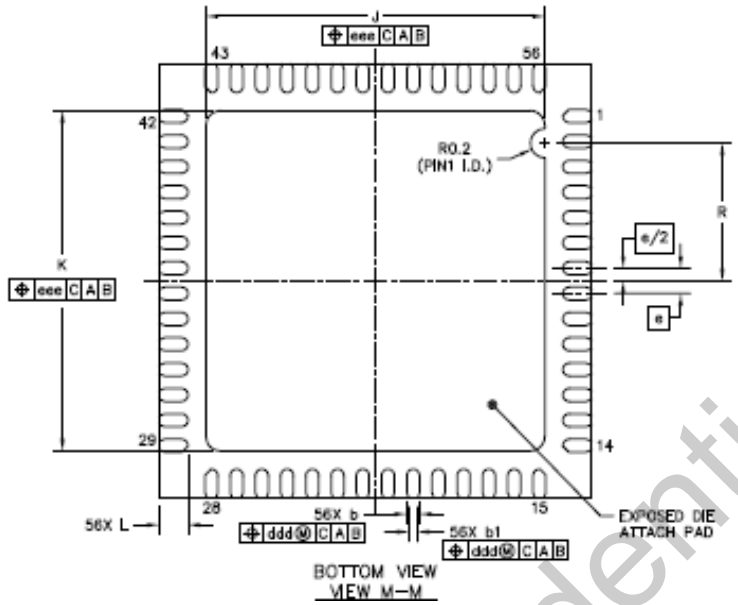


FT7311 Package Diagram

5 PACKAGE INFORMATION

5.1 Package Information of QFN-6x6-56L Package





Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.4	----
L/F Thickness		A3		0.152 REF	
Lead Width		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
Body Size	X	D		6 BSC	
	Y	E		6 BSC	
Lead Pitch		e		0.35 BSC	
EP Size	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
Lead Length		L	0.35	0.4	0.45
		R	1.45	1.55	1.65
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Co Planarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	

Appendix: IC Revision history of FT7311 Specification

Version	Change Items	Effective Date
1.0	1st Preliminary	5th-Jan-17
1.1	Updated ESD and Life cycle guarantee	10th-Sept-17

END OF DATASHEET