DATA SHEET

FT5X26

True Multi-Touch
Capacitive Touch Panel controller

Nov. 28, 2019

Version: 1.6

Table of Contents

PAGE

INTRODUCTION

The FT5X26 is single-chip capacitive touch panel controllers with built-in enhanced Micro-controller unit (MCU). It provides the benefits of full screen common mode scan technology,fast response time and high level of accuracy.It can drive capacitive type touch panel with up to 35 driving and 21 sensing lines.

FEATURES

- Mutual Capacitive Sensing Techniques
- 5426 Supports up to 28TX + 16 RX
- 5526 Supports up to 35TX + 21 RX
- Support up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor,Sleep)
- Support >100Hz sampling rate
- Auto-calibration
- Support IIC (up to 400kbits/sec) interface
- Power
  - 2.7 to 3.6V Operating Voltage
  - IOVCC supports from 1.8V to 3.6V
- Built-in 64KB(000)/128KB(003) Flash
- Single Channel(TX or RX) resistance:Up to100K Ω
- Single Channel (transmit / receive) Capacitance: 40pF
- 12-Bit ADC Accuracy
- Features “short I/O ” testing for sense pins
- Supports various type of panels with no ground shielding layer
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -40°C to +85°C
- Package:
  - QFN56L 6x6x0.6mm, 0.35mm/pitch
  - QFN68L 8x8x0.8mm, 0.4mm/pitch

1.OVERVIEW

1.1. Typical Applications

FT5X26 accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device.

It ‘s powerful design for below applications.

- Tablets
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras

FT5X26 support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for Tablet TP Size (16:9)	Flash Size
FT5426	QFN56L6x6x0.6mm Pitch =0.35mm	28	16	44	≦8”, Sensor Pitch:6.4mm	64KB(-000）128KB(-003)
FT5526	QFN 68L8x8x0.8mm Pitch =0.4mm	35	21	56	≦10.1”, Sensor Pitch:6.4mm	64KB(-000) 128KB(-003)

2. FUNCTIONAL DESCRIPTION

2.1. Architectural Overview

Figure2-1 shows the overall architecture for theFT5X26.

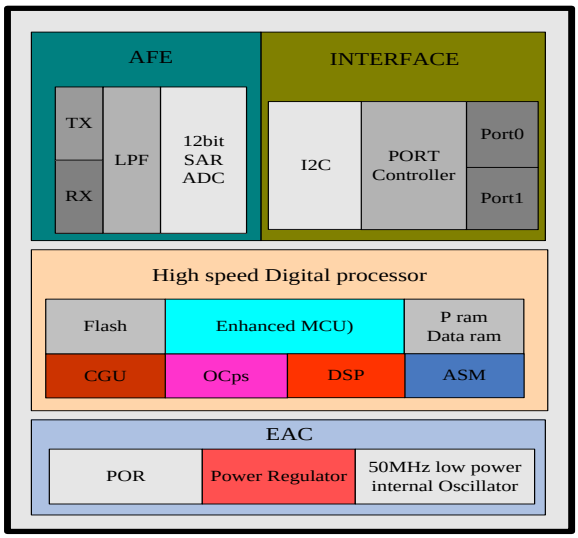


Figure 2-1 SystemArchitecture Diagram

The FT5X26 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU with DSP accelerator

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.

Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently.

Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wakeup the FT5X26 from the Sleep mode.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply
- Power On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.

2.2. MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

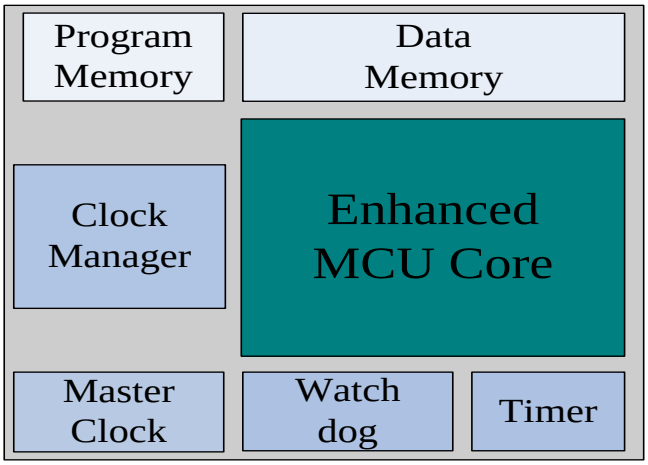


Figure 2-2 MCUBlock Diagram

2.3. Operation Modes

FT5X26 offers following three modes:

- **Active Mode**

When in this mode, FT5X26 actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT5X26 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5X26 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the “RESET” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4. Host Interface

Figure 2-3shows the interface between a host processor and FT5X26. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5X26 to the Host
- Reset Signal from the Host to FT5X26

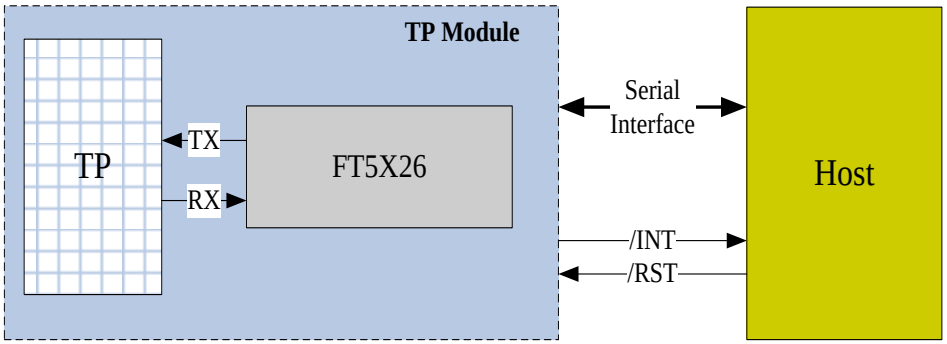


Figure 2-3 HostInterface Diagram

The serial interfaceofFT5X26 is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5X26 to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5X26 from the Sleep mode. After resetting, FT5X26 shall enter the Active mode.

2.5. Serial Interface

FT5X26 supports the I2C interfaces, which can be used by a host processor or other devices.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

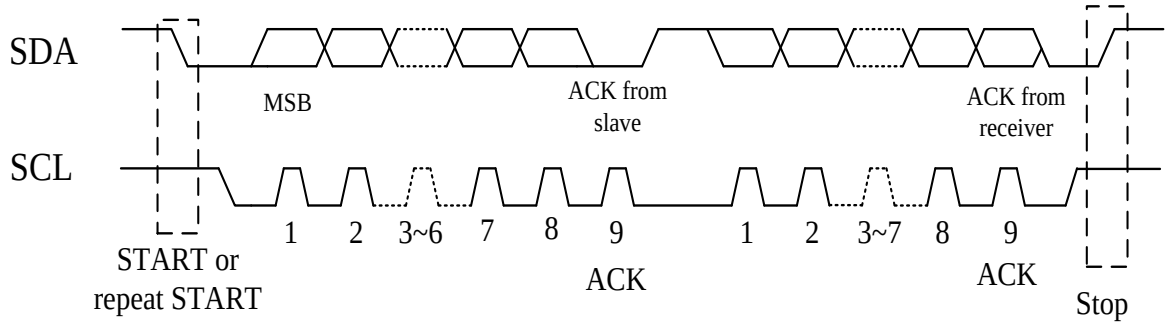


Figure 2-4 I2C Serial Data Transfer Format

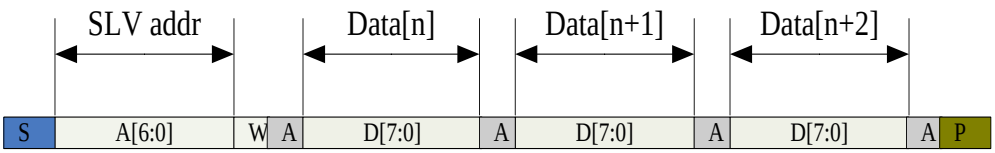


Figure 2-5I2C master write, slave read

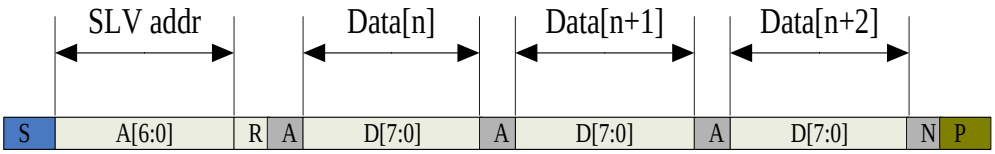


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

3.ELECTRICAL SPECIFICATIONS

3.1. Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSSLF	2.7 ~ +3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.8~ +3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT5X26 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

2. Make sure VDD3 (high) ≥VSSLF (low)

3.2. DC Characteristics

Table 3-2DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V	IOH=3mA	0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V	IOL=4.5mA	--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA	Vin=0~VDD3	-1	--	1	
Current consumption （Normal operation mode）	Iopr	mA	VDD3 = 2.8V Ta=25℃	--	12.76	--	
Current consumption （Monitor mode）	Imon	mA	VDD3 = 2.8V Ta=25℃	--	0.43	--	
Current consumption （Sleep mode）	Islp	uA	VDD3 = 2.8V Ta=25℃	--	42	--	
Step-up output voltage	VDD5	V	VDD3= 2.8V		0.25		
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes: This consumption data is intended for design guidance only. Actual current will depend on the particular sensor design and firmware options.

3.3. AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3 = 2.8V; Ta=25℃	49	50	51	

Table 3-3 AC Characteristics of TX &RX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	
TX output rise time	Ttxr		--	210	--	nS	
TX output fall time	Ttxf		--	210	--	nS	
RX input voltage	Trxi		1.2	--	1.6	V	

3.4. I/OPortsCircuits

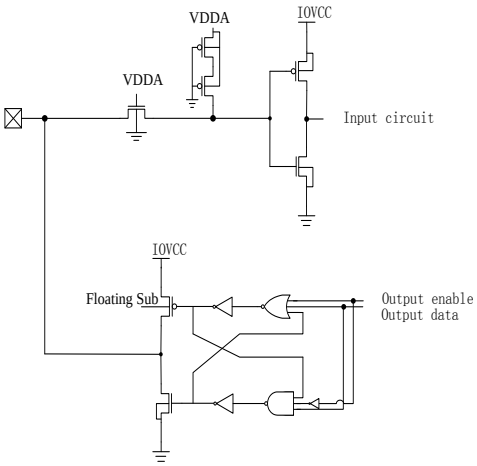


*Figure 3-1*General Purpose*In/Out Port Circuit*.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

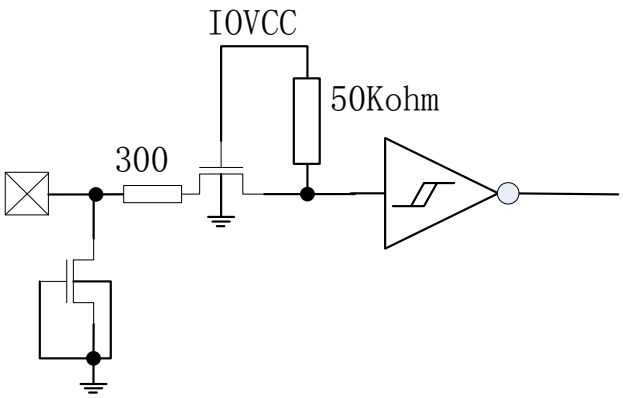


Figure 3-2 Reset Input Port Circuits

3.5. Power On/Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

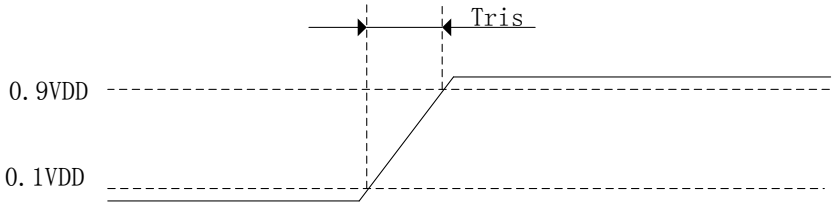


Figure 3-3 Power on time

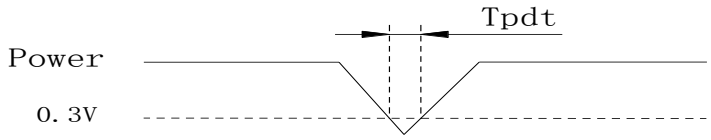


Figure 3-4 Power Cycle requirement

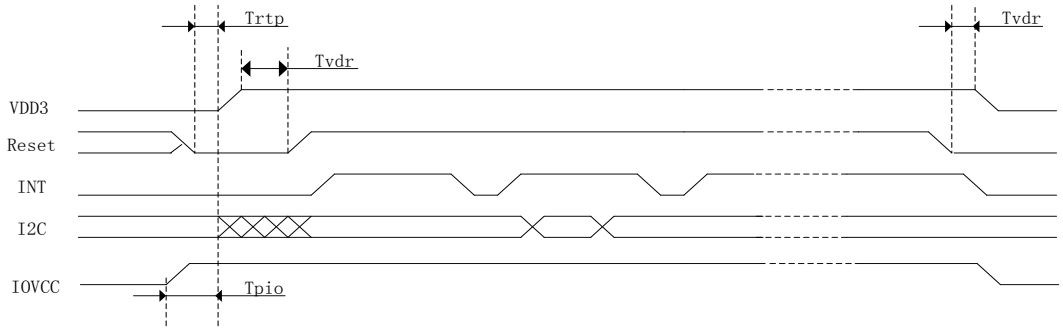


Figure 3-5 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

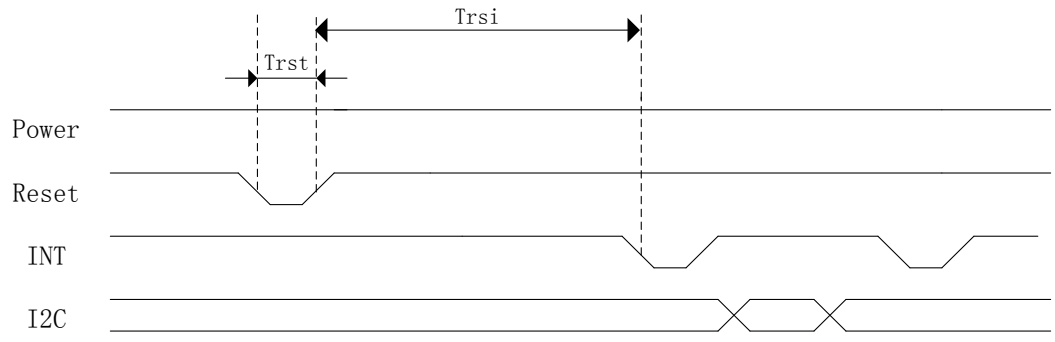


Figure 3-6 Reset Sequence

Table 3-5Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

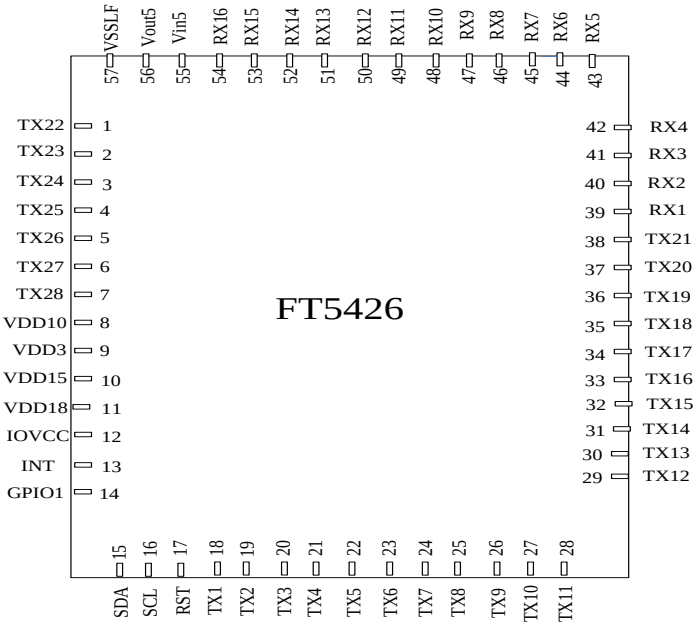
4.PIN CONFIGURATIONS

Pin List of FT5X26

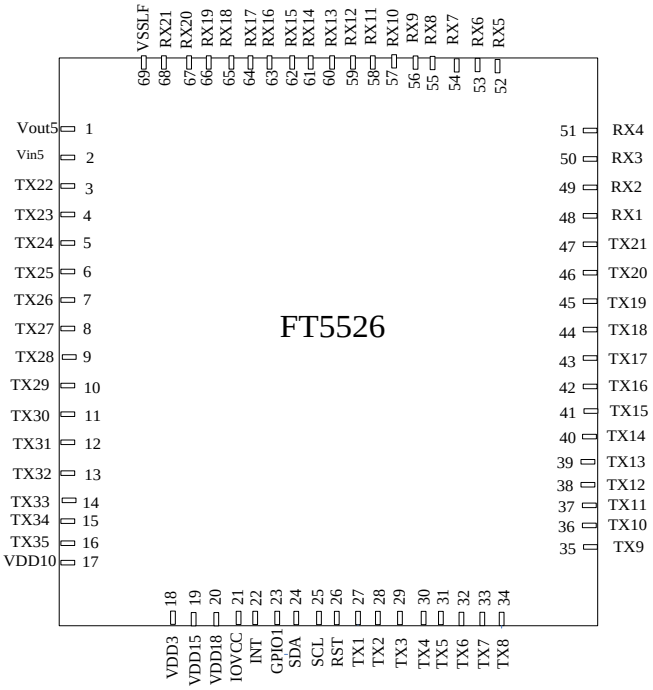
Table 4-1 Pin Definition

Name	Pin No.		Type	Description
	FT5426	FT5526		
RX21		68	I	Receiver input pins
RX20		67	I	Receiver input pins
RX19		66	I	Receiver input pins
RX18		65	I	Receiver input pins
RX17		64	I	Receiver input pins
RX16	54	63	I	Receiver input pins
RX15	53	62	I	Receiver input pins
RX14	52	61	I	Receiver input pins
RX13	51	60	I	Receiver input pins
RX12	50	59	I	Receiver input pins
RX11	49	58	I	Receiver input pins
RX10	48	57	I	Receiver input pins
RX9	47	56	I	Receiver input pins
RX8	46	55	I	Receiver input pins
RX7	45	54	I	Receiver input pins
RX6	44	53	I	Receiver input pins
RX5	43	52	I	Receiver input pins
RX4	42	51	I	Receiver input pins
RX3	41	50	I	Receiver input pins
RX2	40	49	I	Receiver input pins
RX1	39	48	I	Receiver input pins
VDD5_IN	55	1	PWR	internal generated 5V power supply, A 1μF ceramic capacitor to ground is required.
VSSLF	57	69	PWR	Analog ground
VDD5_Out	56	2	PWR	digital power supply, A 1μF ceramiccapacitor to ground is required.
TX10	27	36	O	Transmit output pin
TX11	28	37	O	Transmit output pin
TX12	29	38	O	Transmit output pin
TX13	30	39	O	Transmit output pin
TX14	31	40	O	Transmit output pin
TX15	32	41	O	Transmit output pin
TX16	33	42	O	Transmit output pin
TX17	34	43	O	Transmit output pin
TX18	35	44	O	Transmit output pin
TX19	36	45	O	Transmit output pin
TX20	37	46	O	Transmit output pin
TX21	38	47	O	Transmit output pin
TX22	1	3	O	Transmit output pin

Name	Pin No.		Type	Description
	FT5426	FT5526		
TX23	2	4	O	Transmit output pin
TX24	3	5	O	Transmit output pin
TX25	4	6	O	Transmit output pin
TX26	5	7	O	Transmit output pin
TX27	6	8	O	Transmit output pin
TX28	7	9	O	Transmit output pin
TX29		10	O	Transmit output pin
TX30		11	O	Transmit output pin
TX31		12	O	Transmit output pin
TX32		13	O	Transmit output pin
TX33		14	O	Transmit output pin
TX34		15	O	Transmit output pin
TX35		16	O	Transmit output pin
VDD10	8	17	PWR	digital power supply, A 1μF ceramiccapacitor to ground is required.
VDD3	9	18	PWR	digital power supply, A 1μF ceramiccapacitor to ground is required.
VDD15	10	19	PWR	digital power supply, A 1μF ceramiccapacitor to ground is required.
VDD18	11	20	PWR	digital power supply, A 1μF ceramiccapacitor to ground is required.
IOVCC	12	21	PWR	I/O power supply
INT	13	22	I/O	Interrupt request to the host, or Wakeup request from the host.
GPIO1	14	23	I/O	
SDA	15	24	I/O	I2C data input and output
SCL	16	25	I/O	I2C clock input
RSTN	17	26	I	External Reset, Low is active
TX1	18	27	O	Transmit output pin
TX2	19	28	O	Transmit output pin
TX3	20	29	O	Transmit output pin
TX4	21	30	O	Transmit output pin
TX5	22	31	O	Transmit output pin
TX6	23	32	O	Transmit output pin
TX7	24	33	O	Transmit output pin
TX8	25	34	O	Transmit output pin
TX9	26	35	O	Transmit output pin



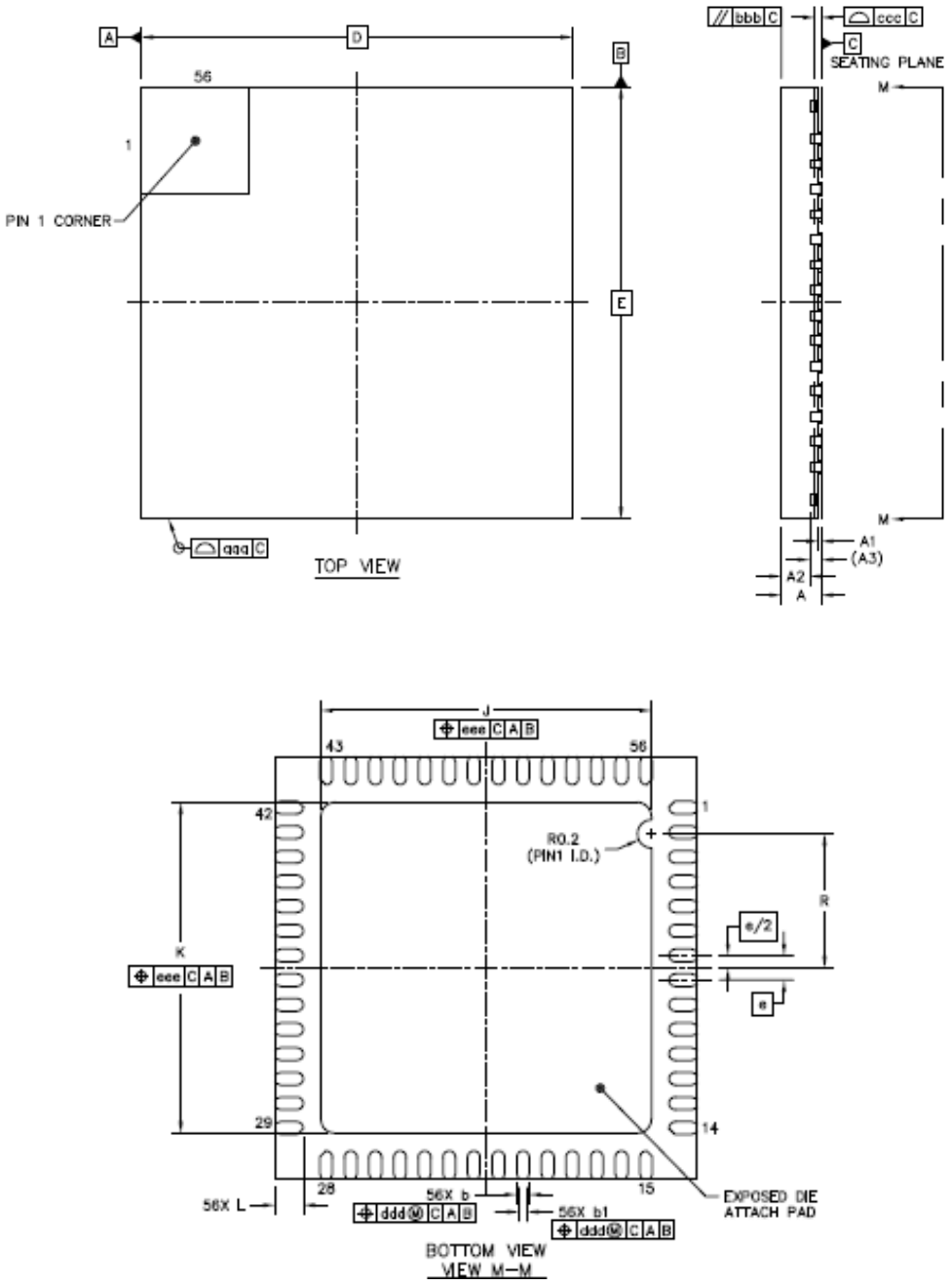
FT5426 Package Diagram



FT5526 Package Diagram

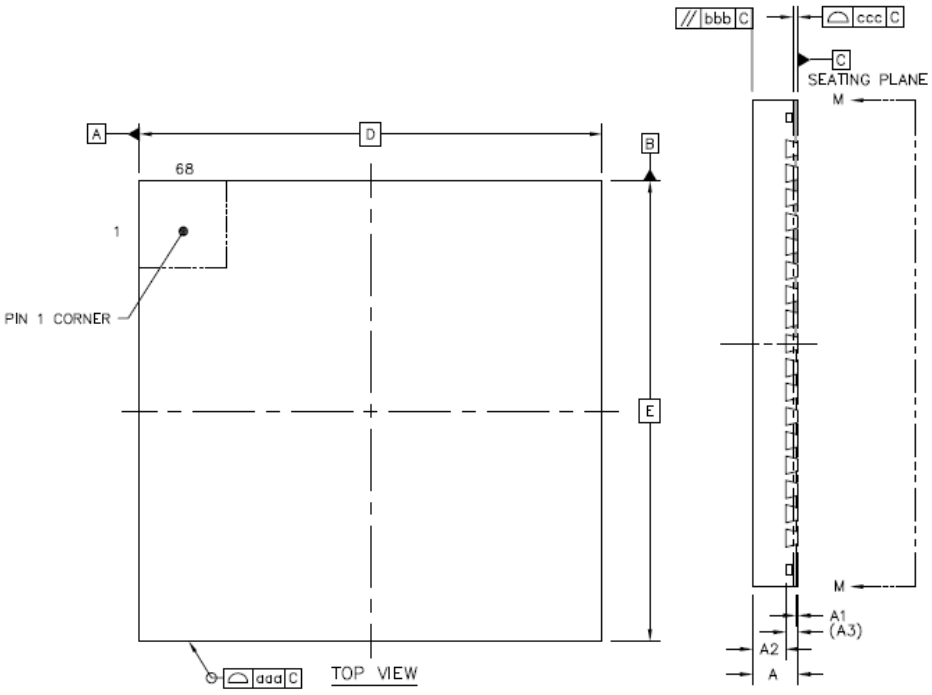
5.PACKAGE INFORMATION

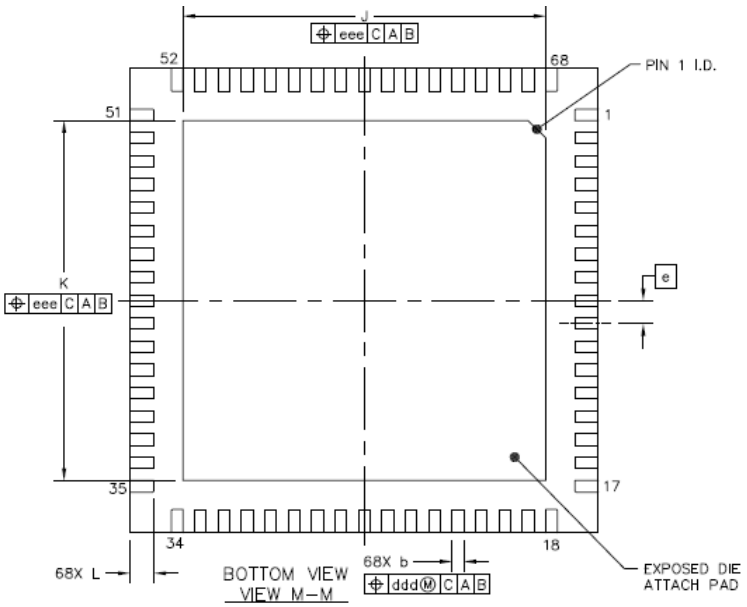
5.1. Package Information of QFN-6x6-56L Package



Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.4	----
L/F Thickness		A3	0.152 REF		
Lead Width		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
Body Size	X	D	6 BSC		
	Y	E	6 BSC		
Lead Pitch		e	0.35 BSC		
EP Size	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
Lead Length		L	0.35	0.4	0.45
		R	1.45	1.55	1.65
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Co Planarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

5.2. Package Information of QFN-8x8-68L Package





Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.7	0.75	0.8
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.55	0.57
L/F Thickness		A3	0.203 REF		
Lead Width		b	0.15	0.2	0.25
Body Size	X	D	8 BSC		
	Y	E	8 BSC		
Lead Pitch		e	0.4 BSC		
EP Size	X	J	6.1	6.2	6.3
	Y	K	6.1	6.2	6.3
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Co Planarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

6.PACKAGE INFORMATION

Product Name	Package Type	# TX Pins	# RX Pins
FT5426-000/-003	QFN-56L	28	16
FT5526-000/-003	QFN-68L	35	21

7.DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by FocalTech Systems are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. FocalTech Systems makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, FocalTech Systems MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. FocalTech Systems reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by FocalTech Systems for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

8.REVISION HISTORY

Date	Revision #	Description	Page	Auditor
28-Nov-19	1.6	Add FT5426-003	5	MKT
12-Aug-18	1.5	1. Corrected version 1.4 Description: FT5726 changed to FT5526-003 2. updated “Built-in 64KB(000)/128KB(003) Flash”	4 22	MKT
15-FEB-18	1.4	Add FT5726-003	/	MKT
18-JAN-16	1.3	Updated Figure 3-5 Power on Sequence	/	MKT
4-FEB-15	1.2	1. Removed FT5426 package information 2. updated Table 3-2 3. updated Figure 3-1 4. updated Figure 3-2	/	MKT
12-NOV-14	1.1	Updated the pin definition of FT5426	/	MKT
23-SEPT-14	1.0	1. Removed Hibernation 2. updated Tpon<=200ms 3. updated Trsi<=200ms 4. updatedI2C Timing Characteristics	/	MKT
10-AUG-14	0.02	Updated Table 3-2DC Characteristics	/	MKT
27-JUN-14	0.01	1st Preliminary	/	MKT