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ILI9881C-05

Amorphous TFT LCD Single-Chip Driver 800(RGB) x 1280 Resolution, 16.7M-color Without Internal GRAM

Specification

Version: V100
Document No: ILI9881C-05_DTS_V100_20200226_TSBUMP

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1. Introduction

The ILI9881C-05 is a 16.7M single-chip (SOC) driver. It is comprised of a 2404-channel source driver (S1~S2400 and SDUM[3:0]), a gate-IC-less level shifter and a power supply circuit to drive a dot-matrix TFT LCD with 800 (RGB) x 1280 dots at maximum.

The ILI9881C-05 can configure functions via the MIPI[1] DSI[2] Interface; transmit video data via MIPI DSI Interface. The ILI9881C-05 supports three kinds of data types, i.e., 16-bit, 18-bit and 24-bit, for video image display in MIPI DSI interfaces. In the MIPI DSI high-speed mode, the ILI9881C-05 also provides three user-selectable hardware structures:

- Two data lane supports up to 850Mbps on the MIPI DSI link
- Three data lanes support up to 750Mbps on the MIPI DSI link
- Four data lanes support up to 650Mbps on the MIPI DSI link

The ILI9881C-05 can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The ILI9881C-05 supports 8 colors (Idle Mode: 8-color low power mode) display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

[1] *MIPI: Mobile Industry Processor Interface*

[2] *DSI: Display Serial Interface*

2. Features

- Display resolution options:
  - 800 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)
  - 768 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)
  - 720 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)
  - 600 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)

- Display color modes
  - Full color mode:

    16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
  - Reduced color modes:

    262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)

    65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)

- Display module:
  - Supports 2404 source channel outputs (S1~S2400 and SDUM[3:0])
  - Supports gate control signals to gate driver in the panel
  - Supports 1-dot , 2-dot , 4-dot , N/4-dot , N/8-dot , N/16-dot , N/32-dot , column , Zig-Zag inversion
  - Gamma correction (1 preset Gamma curve)
  - On module VCOM control

- Display interface types:
  - DSI interface (DSI version 1.01 and D-PHY version 1.00):

    2 data lane / maximum speed 850Mbps

    3 data lanes / maximum speed 750Mbps

    4 data lanes / maximum speed 650Mbps

- Power saving modes:
  - Sleep mode

- Other on-chip functions/Miscellaneous
  - Software programmable color depth mode
  - Oscillator for display clock generation
  - DC VCOM voltage generator and adjustment
  - CABC (Content Adaptive Brightness Control) function
  - DGC (Digital Gamma Correction) function
  - IIE (Impressive Image Enhancement) function
  - VGH/VGL voltage generator for gate control signal in panel
  - Gate control signals to gate driver in panel (GIP)
  - OTP (One-Time Programming) memory store initialization register settings
  - Provide 3 times to store DC VCOM value setting and ID1 ~ ID3
  - BIST (Built-In Self-Test Pattern) mode function

- Input power:
  - VCI = 2.5V ~ 6.6V
  - VDDI = 1.65V ~ 3.6V

- VCC1 = 1.65V ~ 6.6V
- VCC2 = 1.65V ~ 6.6V
- VDDAM = 1.65V ~ 3.6V
- VSP = 4.5V ~ 6.6V
- VSN = -6.6V ~ -4.5V
- OTP programming voltage (MTP_PWR): 8.5V

- Source/VCOM/Gate power supply voltage:
  - VCL-GND = -3.0V ~ -2.3V
  - DC VCOM = -4.0V ~ -0.2V (12mV/step); 0V
  - VREG1OUT = 3.5V ~ 5.6V (Positive source output voltage level)
  - VREG2OUT = -5.6V ~ -3.5V (Negative source output voltage level)
  - VGH-GND = 8V ~ 18V (Positive gate driver output voltage level)
  - VGL-GND = -7V ~ -18V (Negative gate driver output voltage level)

3. Device Overview

3.1. Block Diagram

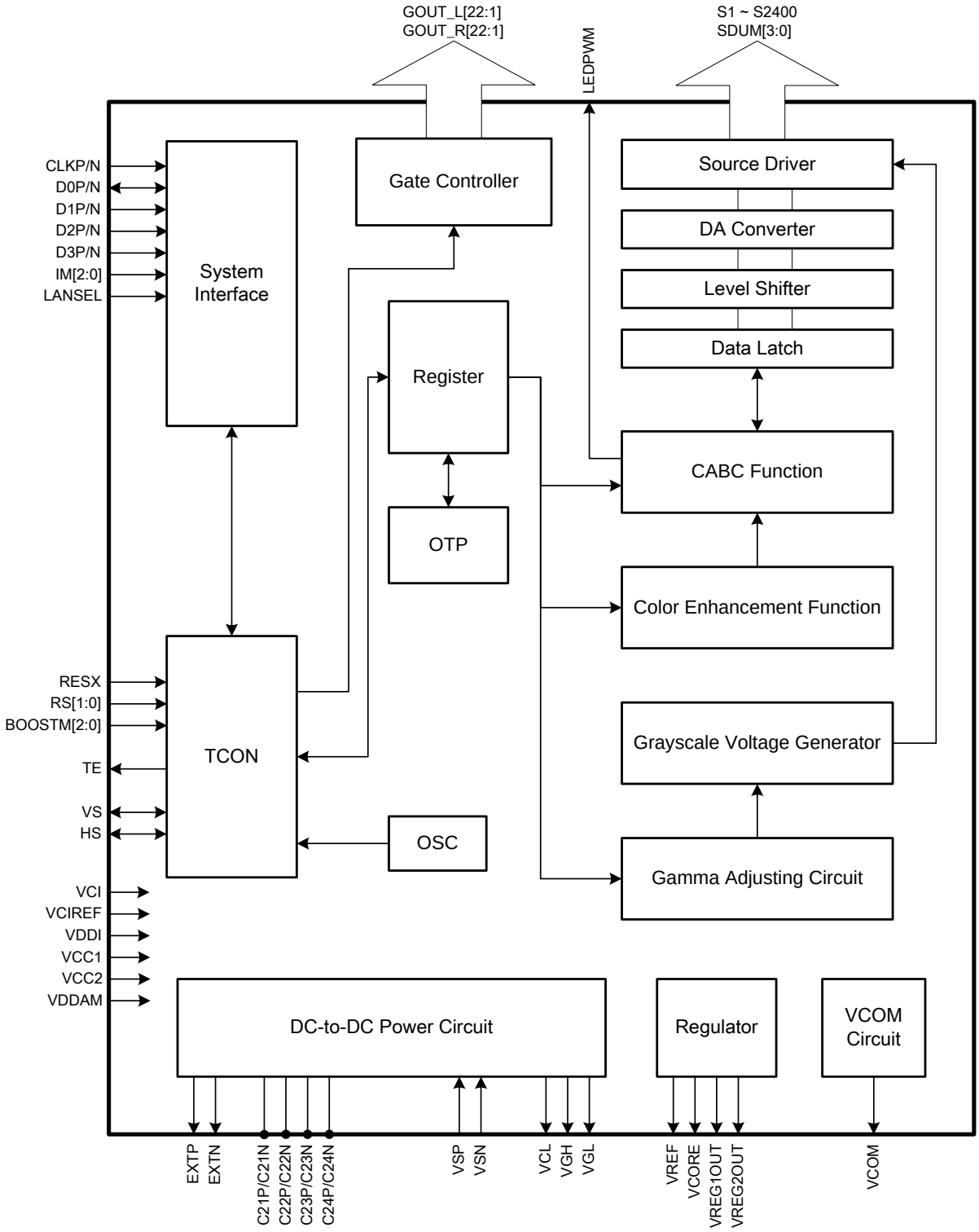


Figure 1: Block Diagram

3.2. Block Function Description

3.2.1. System Interface

The ILI9881C-05 supports DSI interfaces. The interface mode and the lane number of DSI interface can be selected by hardware pins IM[2:0], LANSEL and control register MIPI_LANE_SEL (Page4_R00h).

3.2.2. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage that corresponds to the grayscale level set in the Gamma correction register. The ILI9881C-05 can display 16.7M colors at maximum.

3.2.3. TCON

The TCON generates timing signals for internal circuits. Timing for display operations are outputted separately so that they do not interfere with each other.

3.2.4. OSC

The ILI9881C-05 incorporates with an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.5. Source Driver Circuit

The LCD display driver circuit consists of a 2404-output source driver (S1~S2400 and SDUM[3:0]). The display pattern data is latched when 800RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.6. Gate Controller Circuit

The panel control circuit outputs GOUT_L/R[22:1] signals at either the VGH or VGL level.

3.2.7. DC-to-DC Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to the register setting.

3.2.8. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

3.3. Pin Descriptions

Table 1: Pin Definition

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td colspan="4">Global Control Pins</td></tr>
<tr><td>IM[2:0]</td><td>I</td><td>VDDI</td><td>- Interface mode select pins.
Notes:
(1) IM[2:0] pins are used to configure lane sequence and polarity
(2) The bottom table is an example for MIPI 4 lane setting
<table>
<tr><th colspan="3">External Pad Set</th><th colspan="5">Configuration of MIPI Lane</th></tr>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>D0P/N Pin</th><th>D1P/N Pin</th><th>CLKP/N Pin</th><th>D2P/N Pin</th><th>D3P/N Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>D3P/N</td><td>D2P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>D3N/P</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>D3P/N</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D2P/N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>D3N/P</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D2N/P</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr>
</table></td></tr>
<tr><td>RS[1:0]</td><td>I</td><td>VDDI</td><td>- Resolution selection pins.
<table>
<tr><th>RS1</th><th>RS0</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr>
<tr><td>0</td><td>1</td><td>768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr>
<tr><td>1</td><td>0</td><td>720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr>
<tr><td>1</td><td>1</td><td>600 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr>
</table></td></tr>
<tr><td>LANSEL</td><td>I</td><td>VDDI</td><td>- MIPI DSI Lane number selection pin
LANSEL=”1”, MIPI DSI is 2 Lane mode
LANSEL=”0”, MIPI DSI is 3 or 4 Lane mode
Note: Please reference “Table 2 DSI Interface Lane Mode Selection”</td></tr>
<tr><td>BOOSTM[2:0]</td><td>I</td><td>VDDI</td><td>- Power type selection pins
<table>
<tr><th>Page4_R6Eh
DI_PWR_REG</th><th>BOOSTM2</th><th>BOOSTM1</th><th>BOOSTM0</th><th>NOTE</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Power Mode 2A
External VDDI, VSP and VSN (VCI=VSP)
Note 1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Power Mode 4
External VDDI, VCI, VSP and VSN</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>0</td><td>Power Mode 3
External VDDI and VCI (with ILI4003)</td></tr>
<tr><td colspan="4">prohibited</td><td>-</td></tr>
</table>
The default value of DI_PWR_REG is “1”.
Note 1: VCI and VSP pads must be connected by external metal path.</td></tr>
<tr><td>RESX</td><td>I</td><td>VDDI</td><td>- The external reset input
Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.
Fix to VDDI level when not in use.</td></tr>
<tr><td>TE</td><td>O</td><td>VDDI</td><td>- Tearing effect output pin.
Leave the pin open when not in use.</td></tr>
<tr><td>VS</td><td>I/O</td><td>VDDI</td><td>- Touch synchronization signal (VSOUT).
Fix to VSS level when not in use.</td></tr>
<tr><td>HS</td><td>I/O</td><td>VDDI</td><td>- Touch synchronization signal (HSOUT).
Fix to VSS level when not in use.</td></tr>
<tr><td>LEDPWM</td><td>O</td><td>VDDI</td><td>- LCD backlight control PWM output pin.
Leave the pin open when not in use.</td></tr>
<tr><td colspan="4">DSI Interface Signal Pins</td></tr>
<tr><td>CLKP
CLKN</td><td>I</td><td>LVDSVDD</td><td>- MIPI DSI differential clock pair
Leave it open or fix to LVDSVSS level when not in use.</td></tr>
<tr><td>D0P
D0N</td><td>I/O</td><td>LVDSVDD</td><td>- MIPI DSI differential data pair. (Data lane 0)
Leave it open or fix to LVDSVSS level when not in use.</td></tr>
</table>

D1P D1N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 1) Leave it open or fix to LVDSVSS level when not in use.
D2P D2N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 2) Leave it open or fix to LVDSVSS level when not in use.
D3P D3N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 3) Leave it open or fix to LVDSVSS level when not in use.
Source / Panel Control / VCOM Signal Pins			
S[2400:1]	O	Analog	- Output source driver signals. The D/A converted 256-gray-scale analog voltage output. Source output mapping with different resolution Disaply resulation / Source channels 800 (RGB) / S1 ~ S2400 768 (RGB) / S1 ~ S1152, S1249 ~ S2400 720 (RGB) / S1 ~ S1080, S1321 ~ S2400 600 (RGB) / S1 ~ S960, S1441 ~ S2400 800 (RGB) + Zig-Zag / S1 ~ S2400, SDUM[2:1]
SDUM[3:0]	O	Analog	- Dummy Source Leave the pin open when not in use.
GOUT_L[22:1]	O	Analog	- Gate control signals for panel in left side of IC Leave the pin open when not in use.
GOUT_R[22:1]	O	Analog	- Gate control signals for panel in right side of IC Leave the pin open when not in use.
VCOM	O	Analog	- Regulator output for common voltage of panel Connect to a stabilizing capacitor between VCOM and VSSA.
Power Supply Pins			
VCI	I	Power Supply	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 6.6V
VCIREF	I	Power Supply	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 6.6V
VDDI	I	Power Supply	- Power supply for I/O pads. Connect to an external power supply of 1.65V to 3.6V
VCC1	I	Power Supply	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 6.6V
VCC2	I	Power Supply	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 6.6V
VDDAM	I	Power Supply	- Power supply for MIPI DSI regulator. Connect to an external power supply of 1.65V to 3.6V
VSP	I	Power Supply	- Input voltage from step-up circuit. Connect to an external power supply of 4.5V to 6.6V
VSN	I	Power Supply	- Input voltage from step-up circuit. Connect to an external power supply of -4.5V to -6.6V.
VSSA	I	Ground	- System ground for the analog circuit In the case of COG, connect to GND on the FPC to prevent noise.
VSSREF	I	Ground	- System ground for the analog circuit In the case of COG, connect to GND on the FPC to prevent noise.
LVDSVSS	I	Ground	- System ground for MIPI DSI analog ground In the case of COG, connect to GND on the FPC to prevent noise.
VSS	I	Ground	- System ground for digital circuit In the case of COG, connect to GND on the FPC to prevent noise.
MTP_PWR	I	Power Supply	- Input power for OTP programming. MTP_PWR=8. 5V When not under programming, let MTP_PWR float or connect to ground.
DC-to-DC Circuit Pins			
VREG1OUT	O	Analog	- Regulator output voltage from VSP, It's for positive gray scale voltage. Connect to a stabilizing capacitor between GVDD and VSSA.
VREG2OUT	O	Analog	- Regulator output voltage from VSN, It's for negative gray scale voltage. Connect to a stabilizing capacitor between NGVDD and VSSA.
VCL	O	Analog	- Output voltage from step-up circuit

			Connect to a stabilizing capacitor between VCL and VSSA.
VGH	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGH and VSSA.
VGL	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGL and VSSA.
EXTP	O	VCI	- Control signal output to generate VSP
EXTN	O	VCI	- Control signal output to generate VSN
LVDSVDD	O	Analog	- MIPI DSI regulator output
VREF	O	Analog	- Reference voltage from internal band gap circuit (1.8V typical)
VCORE	O	Analog	- Internal logic regulator output (1.5V typical) Connect to a stabilizing capacitor between VCORE and VSSA.
C21P/ C21N C22P / C22N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGH level.
C23P / C23N C24P / C24N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGL level.
Test / Dummy Pins			
PCLK	I	VDDI	- Test pins Unused pins should be left open.
D[7:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
TEST[5:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
TOUT[3:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
VTESTOUTP	O	Analog	- Analog test output pin Let it open.
VTESTOUTN	O	Analog	- Analog test output pin Let it open.
CSX	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
DCX	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
SCL	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
SDI	I	VDDI	- Test pins Leave the pin open when not in use.
SDO	O	VDDI	- Test pins Leave the pin open when not in use.
TE1	O	VDDI	- Test pins. Leave the pin open when not in use.
C31P	-	-	- Dummy pins Let it open.
VCOMR	-	-	- Dummy pins Let it open.
VGLO2DUMMY	-	-	- Dummy pins Let it open.
DUMMYR1	-	Analog	- dummy pins Propose to connect these two pads separately when use for bonding resistance measurement
VSSDUMMY	-	-	- Dummy pins Let it open.
DUMMY[85:3]	-	-	- Dummy pins Let it open.
DUMMYN	-	-	- Dummy pins Let it open.
DUMMYP	-	-	- Dummy pins Let it open.
VGLO1	O	Analog	- Dummy pins

			Let it open.
C41P / C41N C42P / C42N	-	-	- Dummy pins Let it open.

3.4. Pin Assignment

Chip Size: 27840 um x 875 um

Pad Location: Pad Center.

Coordinate Origin: Chip center

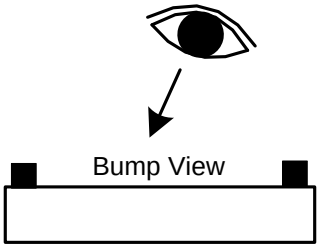
Bump Size:

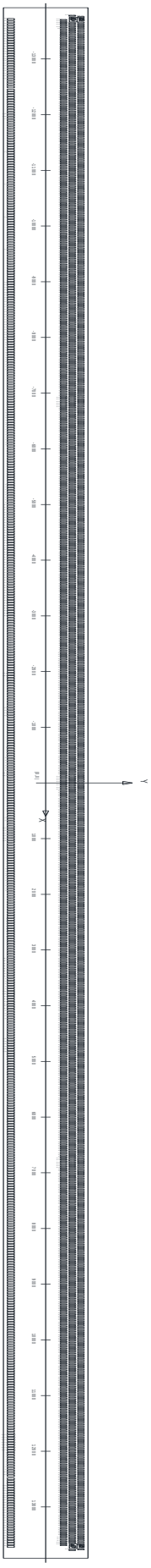
1. 30um x 73um

   Pad 1 to 610.

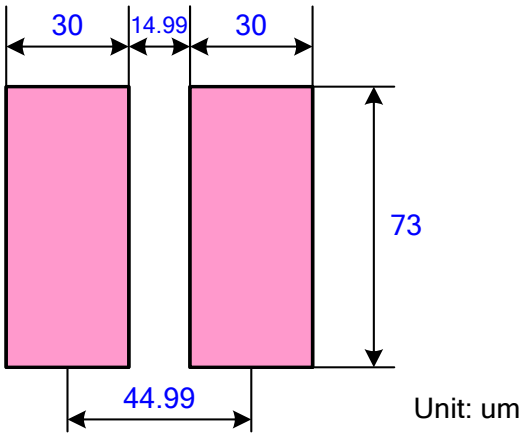
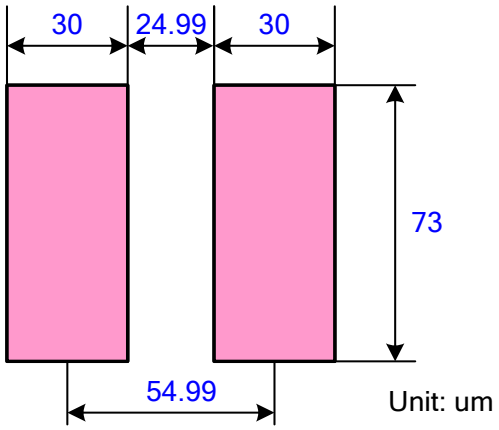
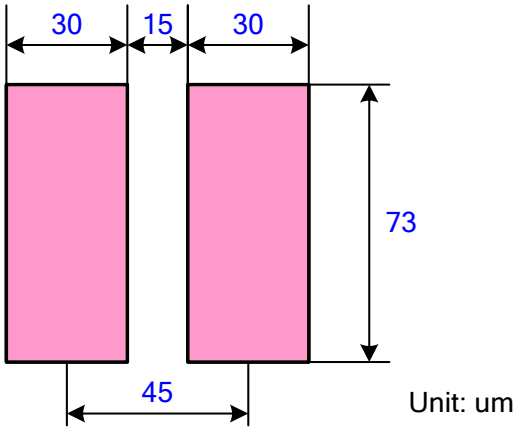
2. 16um x 65um

   Pad 611 to 3102.

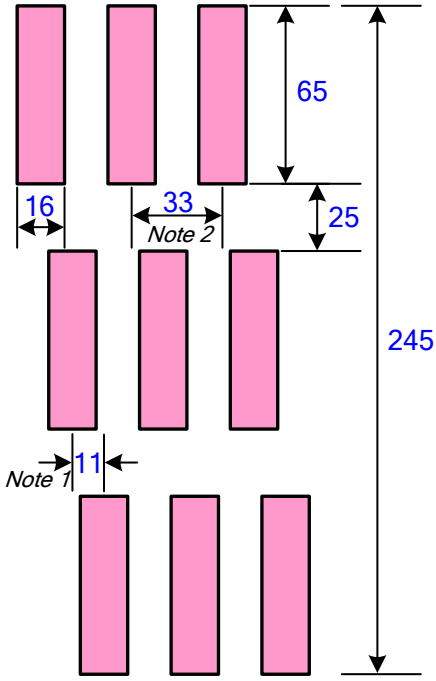




3.5. Bump Arrangement

Input PAD (No. 1~28, 29~305, 306~582, 583~610)	
Input PAD (No. 28~29, 582~583)	
Input PAD (No. 305~306)	

Output PAD
(No. 611~3102)

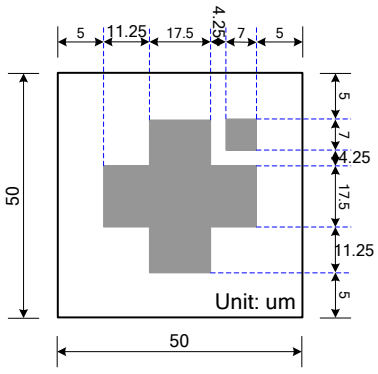


Notes:

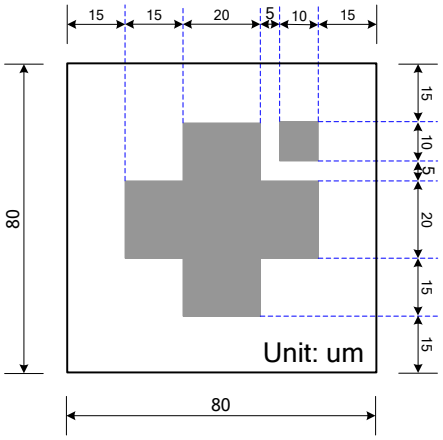
1. Pad has temperature compensation design, so the space may be 11um or 10.99um.

2. Pad has temperature compensation design, so the space may be 33um or 32.99um.

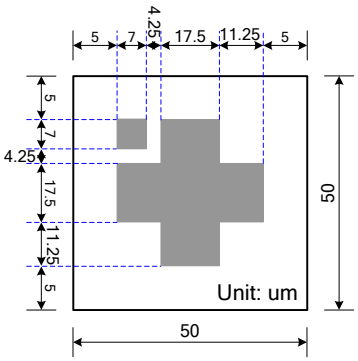
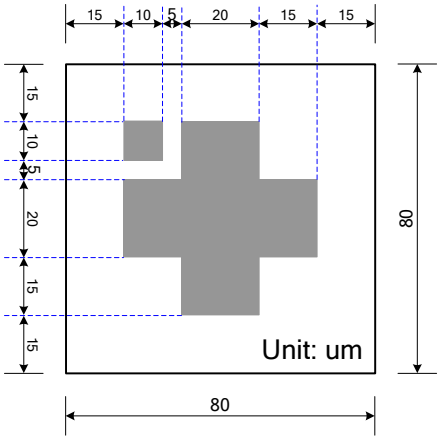
Alignment mark R



Alignment mark: (13706,372.5)



Alignment mark: (13706,285.5)

Alignment mark L	 Alignment mark: (-13706,372.5)  Alignment mark: (-13706,285.5)

3.6. Pad Coordination

No.	Name	X	Y
1	DUMMY1	-13709.46	-361
2	DUMMY1	-13664.47	-361
3	DUMMY1	-13619.48	-361
4	GOUT_L[1]	-13574.49	-361
5	GOUT_L[2]	-13529.5	-361
6	GOUT_L[3]	-13484.51	-361
7	GOUT_L[4]	-13439.52	-361
8	GOUT_L[5]	-13394.53	-361
9	GOUT_L[6]	-13349.54	-361
10	GOUT_L[7]	-13304.55	-361
11	GOUT_L[8]	-13259.56	-361
12	GOUT_L[9]	-13214.57	-361
13	GOUT_L[10]	-13169.58	-361
14	GOUT_L[11]	-13124.59	-361
15	GOUT_L[12]	-13079.6	-361
16	GOUT_L[13]	-13034.61	-361
17	GOUT_L[14]	-12989.62	-361
18	GOUT_L[15]	-12944.63	-361
19	GOUT_L[16]	-12899.64	-361
20	GOUT_L[17]	-12854.65	-361
21	GOUT_L[18]	-12809.66	-361
22	GOUT_L[19]	-12764.67	-361
23	GOUT_L[20]	-12719.68	-361
24	GOUT_L[21]	-12674.69	-361
25	GOUT_L[22]	-12629.7	-361
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27	VCOM	-12539.72	-361
28	VCOM	-12494.73	-361
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253	D[2]	-2361.98	-361
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257	D[0]	-2182.02	-361
258	HS	-2137.03	-361
259	HS	-2092.04	-361
260	VS	-2047.05	-361
261	VS	-2002.06	-361
262	VSSDUMMY	-1957.07	-361
263	VSSDUMMY	-1912.08	-361
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265	PCLK	-1822.1	-361
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271	SCL	-1552.16	-361
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274	SDO	-1417.19	-361
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277	LEDPWM	-1282.22	-361
278	LEDPWM	-1237.23	-361
279	LEDPWM	-1192.24	-361
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282	TE	-1057.27	-361
283	TE	-1012.28	-361
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288	TE1	-787.33	-361
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291	TE1	-652.36	-361
292	RESX	-607.37	-361
293	RESX	-562.38	-361
294	RESX	-517.39	-361
295	RESX	-472.4	-361
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298	TEST[3]	-337.43	-361
299	TEST[2]	-292.44	-361
300	TEST[1]	-247.45	-361
301	TEST[0]	-202.46	-361
302	VSSDUMMY	-157.47	-361
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307	VDDI	67.49	-361
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310	IM[2]	202.46	-361
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315	VDDI	427.41	-361
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354	VSS	2182.02	-361
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612	DUMMY87	13763.37	365
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614	DUMMY89	13664.39	365
615	DUMMY80	13653.39	185
616	DUMMY81	13642.4	275
617	DUMMY82	13631.4	365
618	DUMMY3	13620.4	185
619	DUMMY4	13609.4	275
620	DUMMY5	13598.41	365
621	DUMMY6	13587.41	185
622	DUMMY7	13576.41	275
623	DUMMY8	13565.41	365
624	DUMMY9	13554.42	185
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626	SDUM[2]	13532.42	365
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1013	S[2014]	9276.39	365
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1042	S[1985]	8957.46	275
1043	S[1984]	8946.46	365
1044	S[1983]	8935.47	185
1045	S[1982]	8924.47	275
1046	S[1981]	8913.47	365
1047	S[1980]	8902.47	185
1048	S[1979]	8891.48	275
1049	S[1978]	8880.48	365
1050	S[1977]	8869.48	185
1051	S[1976]	8858.48	275
1052	S[1975]	8847.49	365
1053	S[1974]	8836.49	185
1054	S[1973]	8825.49	275
1055	S[1972]	8814.49	365
1056	S[1971]	8803.5	185
1057	S[1970]	8792.5	275
1058	S[1969]	8781.5	365
1059	S[1968]	8770.5	185
1060	S[1967]	8759.51	275
1061	S[1966]	8748.51	365
1062	S[1965]	8737.51	185
1063	S[1964]	8726.51	275
1064	S[1963]	8715.52	365
1065	S[1962]	8704.52	185
1066	S[1961]	8693.52	275
1067	S[1960]	8682.52	365
1068	S[1959]	8671.53	185
1069	S[1958]	8660.53	275
1070	S[1957]	8649.53	365
1071	S[1956]	8638.53	185
1072	S[1955]	8627.54	275
1073	S[1954]	8616.54	365
1074	S[1953]	8605.54	185
1075	S[1952]	8594.54	275
1076	S[1951]	8583.55	365
1077	S[1950]	8572.55	185
1078	S[1949]	8561.55	275
1079	S[1948]	8550.55	365
1080	S[1947]	8539.56	185
1081	S[1946]	8528.56	275
1082	S[1945]	8517.56	365
1083	S[1944]	8506.56	185
1084	S[1943]	8495.57	275
1085	S[1942]	8484.57	365
1086	S[1941]	8473.57	185
1087	S[1940]	8462.57	275
1088	S[1939]	8451.58	365
1089	S[1938]	8440.58	185
1090	S[1937]	8429.58	275
1091	S[1936]	8418.58	365
1092	S[1935]	8407.59	185
1093	S[1934]	8396.59	275
1094	S[1933]	8385.59	365
1095	S[1932]	8374.59	185
1096	S[1931]	8363.6	275
1097	S[1930]	8352.6	365
1098	S[1929]	8341.6	185
1099	S[1928]	8330.6	275
1100	S[1927]	8319.61	365

No.	Name	X	Y
1101	S[1926]	8308.61	185
1102	S[1925]	8297.61	275
1103	S[1924]	8286.61	365
1104	S[1923]	8275.62	185
1105	S[1922]	8264.62	275
1106	S[1921]	8253.62	365
1107	S[1920]	8242.62	185
1108	S[1919]	8231.63	275
1109	S[1918]	8220.63	365
1110	S[1917]	8209.63	185
1111	S[1916]	8198.63	275
1112	S[1915]	8187.64	365
1113	S[1914]	8176.64	185
1114	S[1913]	8165.64	275
1115	S[1912]	8154.64	365
1116	S[1911]	8143.65	185
1117	S[1910]	8132.65	275
1118	S[1909]	8121.65	365
1119	S[1908]	8110.65	185
1120	S[1907]	8099.66	275
1121	S[1906]	8088.66	365
1122	S[1905]	8077.66	185
1123	S[1904]	8066.66	275
1124	S[1903]	8055.67	365
1125	S[1902]	8044.67	185
1126	S[1901]	8033.67	275
1127	S[1900]	8022.67	365
1128	S[1899]	8011.68	185
1129	S[1898]	8000.68	275
1130	S[1897]	7989.68	365
1131	S[1896]	7978.68	185
1132	S[1895]	7967.69	275
1133	S[1894]	7956.69	365
1134	S[1893]	7945.69	185
1135	S[1892]	7934.69	275
1136	S[1891]	7923.7	365
1137	S[1890]	7912.7	185
1138	S[1889]	7901.7	275
1139	S[1888]	7890.7	365
1140	S[1887]	7879.71	185
1141	S[1886]	7868.71	275
1142	S[1885]	7857.71	365
1143	S[1884]	7846.71	185
1144	S[1883]	7835.72	275
1145	S[1882]	7824.72	365
1146	S[1881]	7813.72	185
1147	S[1880]	7802.72	275
1148	S[1879]	7791.73	365
1149	S[1878]	7780.73	185
1150	S[1877]	7769.73	275
1151	S[1876]	7758.73	365
1152	S[1875]	7747.74	185
1153	S[1874]	7736.74	275
1154	S[1873]	7725.74	365
1155	S[1872]	7714.74	185
1156	S[1871]	7703.75	275
1157	S[1870]	7692.75	365
1158	S[1869]	7681.75	185
1159	S[1868]	7670.75	275
1160	S[1867]	7659.76	365
1161	S[1866]	7648.76	185
1162	S[1865]	7637.76	275
1163	S[1864]	7626.76	365
1164	S[1863]	7615.77	185
1165	S[1862]	7604.77	275
1166	S[1861]	7593.77	365
1167	S[1860]	7582.77	185
1168	S[1859]	7571.78	275
1169	S[1858]	7560.78	365
1170	S[1857]	7549.78	185
1171	S[1856]	7538.78	275
1172	S[1855]	7527.79	365
1173	S[1854]	7516.79	185
1174	S[1853]	7505.79	275
1175	S[1852]	7494.79	365
1176	S[1851]	7483.8	185
1177	S[1850]	7472.8	275
1178	S[1849]	7461.8	365
1179	S[1848]	7450.8	185
1180	S[1847]	7439.81	275
1181	S[1846]	7428.81	365
1182	S[1845]	7417.81	185
1183	S[1844]	7406.81	275
1184	S[1843]	7395.82	365
1185	S[1842]	7384.82	185
1186	S[1841]	7373.82	275
1187	S[1840]	7362.82	365
1188	S[1839]	7351.83	185
1189	S[1838]	7340.83	275
1190	S[1837]	7329.83	365
1191	S[1836]	7318.83	185
1192	S[1835]	7307.84	275
1193	S[1834]	7296.84	365
1194	S[1833]	7285.84	185
1195	S[1832]	7274.84	275
1196	S[1831]	7263.85	365
1197	S[1830]	7252.85	185
1198	S[1829]	7241.85	275
1199	S[1828]	7230.85	365
1200	S[1827]	7219.86	185

No.	Name	X	Y
1201	S[1826]	7208.86	275
1202	S[1825]	7197.86	365
1203	S[1824]	7186.86	185
1204	S[1823]	7175.87	275
1205	S[1822]	7164.87	365
1206	S[1821]	7153.87	185
1207	S[1820]	7142.87	275
1208	S[1819]	7131.88	365
1209	S[1818]	7120.88	185
1210	S[1817]	7109.88	275
1211	S[1816]	7098.88	365
1212	S[1815]	7087.89	185
1213	S[1814]	7076.89	275
1214	S[1813]	7065.89	365
1215	S[1812]	7054.89	185
1216	S[1811]	7043.9	275
1217	S[1810]	7032.9	365
1218	S[1809]	7021.9	185
1219	S[1808]	7010.9	275
1220	S[1807]	6999.91	365
1221	S[1806]	6988.91	185
1222	S[1805]	6977.91	275
1223	S[1804]	6966.91	365
1224	S[1803]	6955.92	185
1225	S[1802]	6944.92	275
1226	S[1801]	6933.92	365
1227	DUMMY11	6922.92	185
1228	DUMMY12	6911.93	275
1229	DUMMY13	6900.93	365
1230	DUMMY14	6889.93	185
1231	DUMMY15	6878.93	275
1232	DUMMY16	6867.94	365
1233	DUMMY17	6856.94	185
1234	DUMMY18	6845.94	275
1235	DUMMY19	6834.94	365
1236	DUMMY20	6823.95	185
1237	DUMMY21	6812.95	275
1238	DUMMY22	6801.95	365
1239	DUMMY23	6790.95	185
1240	DUMMY24	6779.96	275
1241	DUMMY25	6768.96	365
1242	DUMMY26	6757.96	185
1243	DUMMY27	6746.96	275
1244	DUMMY28	6735.97	365
1245	S[1800]	6724.97	185
1246	S[1799]	6713.97	275
1247	S[1798]	6702.97	365
1248	S[1797]	6691.98	185
1249	S[1796]	6680.98	275
1250	S[1795]	6669.98	365
1251	S[1794]	6658.98	185
1252	S[1793]	6647.99	275
1253	S[1792]	6636.99	365
1254	S[1791]	6625.99	185
1255	S[1790]	6614.99	275
1256	S[1789]	6604	365
1257	S[1788]	6593	185
1258	S[1787]	6582	275
1259	S[1786]	6571	365
1260	S[1785]	6560.01	185
1261	S[1784]	6549.01	275
1262	S[1783]	6538.01	365
1263	S[1782]	6527.01	185
1264	S[1781]	6516.02	275
1265	S[1780]	6505.02	365
1266	S[1779]	6494.02	185
1267	S[1778]	6483.02	275
1268	S[1777]	6472.03	365
1269	S[1776]	6461.03	185
1270	S[1775]	6450.03	275
1271	S[1774]	6439.03	365
1272	S[1773]	6428.04	185
1273	S[1772]	6417.04	275
1274	S[1771]	6406.04	365
1275	S[1770]	6395.04	185
1276	S[1769]	6384.05	275
1277	S[1768]	6373.05	365
1278	S[1767]	6362.05	185
1279	S[1766]	6351.05	275
1280	S[1765]	6340.06	365
1281	S[1764]	6329.06	185
1282	S[1763]	6318.06	275
1283	S[1762]	6307.06	365
1284	S[1761]	6296.07	185
1285	S[1760]	6285.07	275
1286	S[1759]	6274.07	365
1287	S[1758]	6263.07	185
1288	S[1757]	6252.08	275
1289	S[1756]	6241.08	365
1290	S[1755]	6230.08	185
1291	S[1754]	6219.08	275
1292	S[1753]	6208.09	365
1293	S[1752]	6197.09	185
1294	S[1751]	6186.09	275
1295	S[1750]	6175.09	365
1296	S[1749]	6164.1	185
1297	S[1748]	6153.1	275
1298	S[1747]	6142.1	365
1299	S[1746]	6131.1	185
1300	S[1745]	6120.11	275

No.	Name	X	Y
1301	S[1744]	6109.11	365
1302	S[1743]	6098.11	185
1303	S[1742]	6087.11	275
1304	S[1741]	6076.12	365
1305	S[1740]	6065.12	185
1306	S[1739]	6054.12	275
1307	S[1738]	6043.12	365
1308	S[1737]	6032.13	185
1309	S[1736]	6021.13	275
1310	S[1735]	6010.13	365
1311	S[1734]	5999.13	185
1312	S[1733]	5988.14	275
1313	S[1732]	5977.14	365
1314	S[1731]	5966.14	185
1315	S[1730]	5955.14	275
1316	S[1729]	5944.15	365
1317	S[1728]	5933.15	185
1318	S[1727]	5922.15	275
1319	S[1726]	5911.15	365
1320	S[1725]	5900.16	185
1321	S[1724]	5889.16	275
1322	S[1723]	5878.16	365
1323	S[1722]	5867.16	185
1324	S[1721]	5856.17	275
1325	S[1720]	5845.17	365
1326	S[1719]	5834.17	185
1327	S[1718]	5823.17	275
1328	S[1717]	5812.18	365
1329	S[1716]	5801.18	185
1330	S[1715]	5790.18	275
1331	S[1714]	5779.18	365
1332	S[1713]	5768.19	185
1333	S[1712]	5757.19	275
1334	S[1711]	5746.19	365
1335	S[1710]	5735.19	185
1336	S[1709]	5724.2	275
1337	S[1708]	5713.2	365
1338	S[1707]	5702.2	185
1339	S[1706]	5691.2	275
1340	S[1705]	5680.21	365
1341	S[1704]	5669.21	185
1342	S[1703]	5658.21	275
1343	S[1702]	5647.21	365
1344	S[1701]	5636.22	185
1345	S[1700]	5625.22	275
1346	S[1699]	5614.22	365
1347	S[1698]	5603.22	185
1348	S[1697]	5592.23	275
1349	S[1696]	5581.23	365
1350	S[1695]	5570.23	185
1351	S[1694]	5559.23	275
1352	S[1693]	5548.24	365
1353	S[1692]	5537.24	185
1354	S[1691]	5526.24	275
1355	S[1690]	5515.24	365
1356	S[1689]	5504.25	185
1357	S[1688]	5493.25	275
1358	S[1687]	5482.25	365
1359	S[1686]	5471.25	185
1360	S[1685]	5460.26	275
1361	S[1684]	5449.26	365
1362	S[1683]	5438.26	185
1363	S[1682]	5427.26	275
1364	S[1681]	5416.27	365
1365	S[1680]	5405.27	185
1366	S[1679]	5394.27	275
1367	S[1678]	5383.27	365
1368	S[1677]	5372.28	185
1369	S[1676]	5361.28	275
1370	S[1675]	5350.28	365
1371	S[1674]	5339.28	185
1372	S[1673]	5328.29	275
1373	S[1672]	5317.29	365
1374	S[1671]	5306.29	185
1375	S[1670]	5295.29	275
1376	S[1669]	5284.3	365
1377	S[1668]	5273.3	185
1378	S[1667]	5262.3	275
1379	S[1666]	5251.3	365
1380	S[1665]	5240.31	185
1381	S[1664]	5229.31	275
1382	S[1663]	5218.31	365
1383	S[1662]	5207.31	185
1384	S[1661]	5196.32	275
1385	S[1660]	5185.32	365
1386	S[1659]	5174.32	185
1387	S[1658]	5163.32	275
1388	S[1657]	5152.33	365
1389	S[1656]	5141.33	185
1390	S[1655]	5130.33	275
1391	S[1654]	5119.33	365
1392	S[1653]	5108.34	185
1393	S[1652]	5097.34	275
1394	S[1651]	5086.34	365
1395	S[1650]	5075.34	185
1396	S[1649]	5064.35	275
1397	S[1648]	5053.35	365
1398	S[1647]	5042.35	185
1399	S[1646]	5031.35	275
1400	S[1645]	5020.36	365

No.	Name	X	Y
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1402	S[1643]	4998.36	275
1403	S[1642]	4987.36	365
1404	S[1641]	4976.37	185
1405	S[1640]	4965.37	275
1406	S[1639]	4954.37	365
1407	S[1638]	4943.37	185
1408	S[1637]	4932.38	275
1409	S[1636]	4921.38	365
1410	S[1635]	4910.38	185
1411	S[1634]	4899.38	275
1412	S[1633]	4888.39	365
1413	S[1632]	4877.39	185
1414	S[1631]	4866.39	275
1415	S[1630]	4855.39	365
1416	S[1629]	4844.4	185
1417	S[1628]	4833.4	275
1418	S[1627]	4822.4	365
1419	S[1626]	4811.4	185
1420	S[1625]	4800.41	275
1421	S[1624]	4789.41	365
1422	S[1623]	4778.41	185
1423	S[1622]	4767.41	275
1424	S[1621]	4756.42	365
1425	S[1620]	4745.42	185
1426	S[1619]	4734.42	275
1427	S[1618]	4723.42	365
1428	S[1617]	4712.43	185
1429	S[1616]	4701.43	275
1430	S[1615]	4690.43	365
1431	S[1614]	4679.43	185
1432	S[1613]	4668.44	275
1433	S[1612]	4657.44	365
1434	S[1611]	4646.44	185
1435	S[1610]	4635.44	275
1436	S[1609]	4624.45	365
1437	S[1608]	4613.45	185
1438	S[1607]	4602.45	275
1439	S[1606]	4591.45	365
1440	S[1605]	4580.46	185
1441	S[1604]	4569.46	275
1442	S[1603]	4558.46	365
1443	S[1602]	4547.46	185
1444	S[1601]	4536.47	275
1445	S[1600]	4525.47	365
1446	S[1599]	4514.47	185
1447	S[1598]	4503.47	275
1448	S[1597]	4492.48	365
1449	S[1596]	4481.48	185
1450	S[1595]	4470.48	275
1451	S[1594]	4459.48	365
1452	S[1593]	4448.49	185
1453	S[1592]	4437.49	275
1454	S[1591]	4426.49	365
1455	S[1590]	4415.49	185
1456	S[1589]	4404.5	275
1457	S[1588]	4393.5	365
1458	S[1587]	4382.5	185
1459	S[1586]	4371.5	275
1460	S[1585]	4360.51	365
1461	S[1584]	4349.51	185
1462	S[1583]	4338.51	275
1463	S[1582]	4327.51	365
1464	S[1581]	4316.52	185
1465	S[1580]	4305.52	275
1466	S[1579]	4294.52	365
1467	S[1578]	4283.52	185
1468	S[1577]	4272.53	275
1469	S[1576]	4261.53	365
1470	S[1575]	4250.53	185
1471	S[1574]	4239.53	275
1472	S[1573]	4228.54	365
1473	S[1572]	4217.54	185
1474	S[1571]	4206.54	275
1475	S[1570]	4195.54	365
1476	S[1569]	4184.55	185
1477	S[1568]	4173.55	275
1478	S[1567]	4162.55	365
1479	S[1566]	4151.55	185
1480	S[1565]	4140.56	275
1481	S[1564]	4129.56	365
1482	S[1563]	4118.56	185
1483	S[1562]	4107.56	275
1484	S[1561]	4096.57	365
1485	S[1560]	4085.57	185
1486	S[1559]	4074.57	275
1487	S[1558]	4063.57	365
1488	S[1557]	4052.58	185
1489	S[1556]	4041.58	275
1490	S[1555]	4030.58	365
1491	S[1554]	4019.58	185
1492	S[1553]	4008.59	275
1493	S[1552]	3997.59	365
1494	S[1551]	3986.59	185
1495	S[1550]	3975.59	275
1496	S[1549]	3964.6	365
1497	S[1548]	3953.6	185
1498	S[1547]	3942.6	275
1499	S[1546]	3931.6	365
1500	S[1545]	3920.61	185

No.	Name	X	Y
1501	S[1544]	3909.61	275
1502	S[1543]	3898.61	365
1503	S[1542]	3887.61	185
1504	S[1541]	3876.62	275
1505	S[1540]	3865.62	365
1506	S[1539]	3854.62	185
1507	S[1538]	3843.62	275
1508	S[1537]	3832.63	365
1509	S[1536]	3821.63	185
1510	S[1535]	3810.63	275
1511	S[1534]	3799.63	365
1512	S[1533]	3788.64	185
1513	S[1532]	3777.64	275
1514	S[1531]	3766.64	365
1515	S[1530]	3755.64	185
1516	S[1529]	3744.65	275
1517	S[1528]	3733.65	365
1518	S[1527]	3722.65	185
1519	S[1526]	3711.65	275
1520	S[1525]	3700.66	365
1521	S[1524]	3689.66	185
1522	S[1523]	3678.66	275
1523	S[1522]	3667.66	365
1524	S[1521]	3656.67	185
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1531	S[1514]	3579.68	275
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1546	S[1499]	3414.72	275
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1555	S[1490]	3315.74	275
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1567	S[1478]	3183.77	275
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1591	S[1454]	2919.83	275
1592	S[1453]	2908.84	365
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1609	S[1436]	2721.88	275
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1943	S[1126]	-951.28	365
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2006	S[1063]	-1644.12	365
2007	S[1062]	-1655.12	185
2008	S[1061]	-1666.12	275
2009	S[1060]	-1677.12	365
2010	S[1059]	-1688.11	185
2011	S[1058]	-1699.11	275
2012	S[1057]	-1710.11	365
2013	S[1056]	-1721.11	185
2014	S[1055]	-1732.1	275
2015	S[1054]	-1743.1	365
2016	S[1053]	-1754.1	185
2017	S[1052]	-1765.1	275
2018	S[1051]	-1776.09	365
2019	S[1050]	-1787.09	185
2020	S[1049]	-1798.09	275
2021	S[1048]	-1809.09	365
2022	S[1047]	-1820.08	185
2023	S[1046]	-1831.08	275
2024	S[1045]	-1842.08	365
2025	S[1044]	-1853.08	185
2026	S[1043]	-1864.07	275
2027	S[1042]	-1875.07	365
2028	S[1041]	-1886.07	185
2029	S[1040]	-1897.07	275
2030	S[1039]	-1908.06	365
2031	S[1038]	-1919.06	185
2032	S[1037]	-1930.06	275
2033	S[1036]	-1941.06	365
2034	S[1035]	-1952.05	185
2035	S[1034]	-1963.05	275
2036	S[1033]	-1974.05	365
2037	S[1032]	-1985.05	185
2038	S[1031]	-1996.04	275
2039	S[1030]	-2007.04	365
2040	S[1029]	-2018.04	185
2041	S[1028]	-2029.04	275
2042	S[1027]	-2040.03	365
2043	S[1026]	-2051.03	185
2044	S[1025]	-2062.03	275
2045	S[1024]	-2073.03	365
2046	S[1023]	-2084.02	185
2047	S[1022]	-2095.02	275
2048	S[1021]	-2106.02	365
2049	S[1020]	-2117.02	185
2050	S[1019]	-2128.01	275
2051	S[1018]	-2139.01	365
2052	S[1017]	-2150.01	185
2053	S[1016]	-2161.01	275
2054	S[1015]	-2172	365
2055	S[1014]	-2183	185
2056	S[1013]	-2194	275
2057	S[1012]	-2205	365
2058	S[1011]	-2215.99	185
2059	S[1010]	-2226.99	275
2060	S[1009]	-2237.99	365
2061	S[1008]	-2248.99	185
2062	S[1007]	-2259.98	275
2063	S[1006]	-2270.98	365
2064	S[1005]	-2281.98	185
2065	S[1004]	-2292.98	275
2066	S[1003]	-2303.97	365
2067	S[1002]	-2314.97	185
2068	S[1001]	-2325.97	275
2069	S[1000]	-2336.97	365
2070	S[999]	-2347.96	185
2071	S[998]	-2358.96	275
2072	S[997]	-2369.96	365
2073	S[996]	-2380.96	185
2074	S[995]	-2391.95	275
2075	S[994]	-2402.95	365
2076	S[993]	-2413.95	185
2077	S[992]	-2424.95	275
2078	S[991]	-2435.94	365
2079	S[990]	-2446.94	185
2080	S[989]	-2457.94	275
2081	S[988]	-2468.94	365
2082	S[987]	-2479.93	185
2083	S[986]	-2490.93	275
2084	S[985]	-2501.93	365
2085	S[984]	-2512.93	185
2086	S[983]	-2523.92	275
2087	S[982]	-2534.92	365
2088	S[981]	-2545.92	185
2089	S[980]	-2556.92	275
2090	S[979]	-2567.91	365
2091	S[978]	-2578.91	185
2092	S[977]	-2589.91	275
2093	S[976]	-2600.91	365
2094	S[975]	-2611.9	185
2095	S[974]	-2622.9	275
2096	S[973]	-2633.9	365
2097	S[972]	-2644.9	185
2098	S[971]	-2655.89	275
2099	S[970]	-2666.89	365
2100	S[969]	-2677.89	185

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2103	S[966]	-2710.88	185
2104	S[965]	-2721.88	275
2105	S[964]	-2732.88	365
2106	S[963]	-2743.87	185
2107	S[962]	-2754.87	275
2108	S[961]	-2765.87	365
2109	S[960]	-2776.87	185
2110	S[959]	-2787.86	275
2111	S[958]	-2798.86	365
2112	S[957]	-2809.86	185
2113	S[956]	-2820.86	275
2114	S[955]	-2831.85	365
2115	S[954]	-2842.85	185
2116	S[953]	-2853.85	275
2117	S[952]	-2864.85	365
2118	S[951]	-2875.84	185
2119	S[950]	-2886.84	275
2120	S[949]	-2897.84	365
2121	S[948]	-2908.84	185
2122	S[947]	-2919.83	275
2123	S[946]	-2930.83	365
2124	S[945]	-2941.83	185
2125	S[944]	-2952.83	275
2126	S[943]	-2963.82	365
2127	S[942]	-2974.82	185
2128	S[941]	-2985.82	275
2129	S[940]	-2996.82	365
2130	S[939]	-3007.81	185
2131	S[938]	-3018.81	275
2132	S[937]	-3029.81	365
2133	S[936]	-3040.81	185
2134	S[935]	-3051.8	275
2135	S[934]	-3062.8	365
2136	S[933]	-3073.8	185
2137	S[932]	-3084.8	275
2138	S[931]	-3095.79	365
2139	S[930]	-3106.79	185
2140	S[929]	-3117.79	275
2141	S[928]	-3128.79	365
2142	S[927]	-3139.78	185
2143	S[926]	-3150.78	275
2144	S[925]	-3161.78	365
2145	S[924]	-3172.78	185
2146	S[923]	-3183.77	275
2147	S[922]	-3194.77	365
2148	S[921]	-3205.77	185
2149	S[920]	-3216.77	275
2150	S[919]	-3227.76	365
2151	S[918]	-3238.76	185
2152	S[917]	-3249.76	275
2153	S[916]	-3260.76	365
2154	S[915]	-3271.75	185
2155	S[914]	-3282.75	275
2156	S[913]	-3293.75	365
2157	S[912]	-3304.75	185
2158	S[911]	-3315.74	275
2159	S[910]	-3326.74	365
2160	S[909]	-3337.74	185
2161	S[908]	-3348.74	275
2162	S[907]	-3359.73	365
2163	S[906]	-3370.73	185
2164	S[905]	-3381.73	275
2165	S[904]	-3392.73	365
2166	S[903]	-3403.72	185
2167	S[902]	-3414.72	275
2168	S[901]	-3425.72	365
2169	S[900]	-3436.72	185
2170	S[899]	-3447.71	275
2171	S[898]	-3458.71	365
2172	S[897]	-3469.71	185
2173	S[896]	-3480.71	275
2174	S[895]	-3491.7	365
2175	S[894]	-3502.7	185
2176	S[893]	-3513.7	275
2177	S[892]	-3524.7	365
2178	S[891]	-3535.69	185
2179	S[890]	-3546.69	275
2180	S[889]	-3557.69	365
2181	S[888]	-3568.69	185
2182	S[887]	-3579.68	275
2183	S[886]	-3590.68	365
2184	S[885]	-3601.68	185
2185	S[884]	-3612.68	275
2186	S[883]	-3623.67	365
2187	S[882]	-3634.67	185
2188	S[881]	-3645.67	275
2189	S[880]	-3656.67	365
2190	S[879]	-3667.66	185
2191	S[878]	-3678.66	275
2192	S[877]	-3689.66	365
2193	S[876]	-3700.66	185
2194	S[875]	-3711.65	275
2195	S[874]	-3722.65	365
2196	S[873]	-3733.65	185
2197	S[872]	-3744.65	275
2198	S[871]	-3755.64	365
2199	S[870]	-3766.64	185
2200	S[869]	-3777.64	275

No.	Name	X	Y
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2203	S[866]	-3810.63	275
2204	S[865]	-3821.63	365
2205	S[864]	-3832.63	185
2206	S[863]	-3843.62	275
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2208	S[861]	-3865.62	185
2209	S[860]	-3876.62	275
2210	S[859]	-3887.61	365
2211	S[858]	-3898.61	185
2212	S[857]	-3909.61	275
2213	S[856]	-3920.61	365
2214	S[855]	-3931.6	185
2215	S[854]	-3942.6	275
2216	S[853]	-3953.6	365
2217	S[852]	-3964.6	185
2218	S[851]	-3975.59	275
2219	S[850]	-3986.59	365
2220	S[849]	-3997.59	185
2221	S[848]	-4008.59	275
2222	S[847]	-4019.58	365
2223	S[846]	-4030.58	185
2224	S[845]	-4041.58	275
2225	S[844]	-4052.58	365
2226	S[843]	-4063.57	185
2227	S[842]	-4074.57	275
2228	S[841]	-4085.57	365
2229	S[840]	-4096.57	185
2230	S[839]	-4107.56	275
2231	S[838]	-4118.56	365
2232	S[837]	-4129.56	185
2233	S[836]	-4140.56	275
2234	S[835]	-4151.55	365
2235	S[834]	-4162.55	185
2236	S[833]	-4173.55	275
2237	S[832]	-4184.55	365
2238	S[831]	-4195.54	185
2239	S[830]	-4206.54	275
2240	S[829]	-4217.54	365
2241	S[828]	-4228.54	185
2242	S[827]	-4239.53	275
2243	S[826]	-4250.53	365
2244	S[825]	-4261.53	185
2245	S[824]	-4272.53	275
2246	S[823]	-4283.52	365
2247	S[822]	-4294.52	185
2248	S[821]	-4305.52	275
2249	S[820]	-4316.52	365
2250	S[819]	-4327.51	185
2251	S[818]	-4338.51	275
2252	S[817]	-4349.51	365
2253	S[816]	-4360.51	185
2254	S[815]	-4371.5	275
2255	S[814]	-4382.5	365
2256	S[813]	-4393.5	185
2257	S[812]	-4404.5	275
2258	S[811]	-4415.49	365
2259	S[810]	-4426.49	185
2260	S[809]	-4437.49	275
2261	S[808]	-4448.49	365
2262	S[807]	-4459.48	185
2263	S[806]	-4470.48	275
2264	S[805]	-4481.48	365
2265	S[804]	-4492.48	185
2266	S[803]	-4503.47	275
2267	S[802]	-4514.47	365
2268	S[801]	-4525.47	185
2269	S[800]	-4536.47	275
2270	S[799]	-4547.46	365
2271	S[798]	-4558.46	185
2272	S[797]	-4569.46	275
2273	S[796]	-4580.46	365
2274	S[795]	-4591.45	185
2275	S[794]	-4602.45	275
2276	S[793]	-4613.45	365
2277	S[792]	-4624.45	185
2278	S[791]	-4635.44	275
2279	S[790]	-4646.44	365
2280	S[789]	-4657.44	185
2281	S[788]	-4668.44	275
2282	S[787]	-4679.43	365
2283	S[786]	-4690.43	185
2284	S[785]	-4701.43	275
2285	S[784]	-4712.43	365
2286	S[783]	-4723.42	185
2287	S[782]	-4734.42	275
2288	S[781]	-4745.42	365
2289	S[780]	-4756.42	185
2290	S[779]	-4767.41	275
2291	S[778]	-4778.41	365
2292	S[777]	-4789.41	185
2293	S[776]	-4800.41	275
2294	S[775]	-4811.4	365
2295	S[774]	-4822.4	185
2296	S[773]	-4833.4	275
2297	S[772]	-4844.4	365
2298	S[771]	-4855.39	185
2299	S[770]	-4866.39	275
2300	S[769]	-4877.39	365

No.	Name	X	Y
2301	S[768]	-4888.39	185
2302	S[767]	-4899.38	275
2303	S[766]	-4910.38	365
2304	S[765]	-4921.38	185
2305	S[764]	-4932.38	275
2306	S[763]	-4943.37	365
2307	S[762]	-4954.37	185
2308	S[761]	-4965.37	275
2309	S[760]	-4976.37	365
2310	S[759]	-4987.36	185
2311	S[758]	-4998.36	275
2312	S[757]	-5009.36	365
2313	S[756]	-5020.36	185
2314	S[755]	-5031.35	275
2315	S[754]	-5042.35	365
2316	S[753]	-5053.35	185
2317	S[752]	-5064.35	275
2318	S[751]	-5075.34	365
2319	S[750]	-5086.34	185
2320	S[749]	-5097.34	275
2321	S[748]	-5108.34	365
2322	S[747]	-5119.33	185
2323	S[746]	-5130.33	275
2324	S[745]	-5141.33	365
2325	S[744]	-5152.33	185
2326	S[743]	-5163.32	275
2327	S[742]	-5174.32	365
2328	S[741]	-5185.32	185
2329	S[740]	-5196.32	275
2330	S[739]	-5207.31	365
2331	S[738]	-5218.31	185
2332	S[737]	-5229.31	275
2333	S[736]	-5240.31	365
2334	S[735]	-5251.3	185
2335	S[734]	-5262.3	275
2336	S[733]	-5273.3	365
2337	S[732]	-5284.3	185
2338	S[731]	-5295.29	275
2339	S[730]	-5306.29	365
2340	S[729]	-5317.29	185
2341	S[728]	-5328.29	275
2342	S[727]	-5339.28	365
2343	S[726]	-5350.28	185
2344	S[725]	-5361.28	275
2345	S[724]	-5372.28	365
2346	S[723]	-5383.27	185
2347	S[722]	-5394.27	275
2348	S[721]	-5405.27	365
2349	S[720]	-5416.27	185
2350	S[719]	-5427.26	275
2351	S[718]	-5438.26	365
2352	S[717]	-5449.26	185
2353	S[716]	-5460.26	275
2354	S[715]	-5471.25	365
2355	S[714]	-5482.25	185
2356	S[713]	-5493.25	275
2357	S[712]	-5504.25	365
2358	S[711]	-5515.24	185
2359	S[710]	-5526.24	275
2360	S[709]	-5537.24	365
2361	S[708]	-5548.24	185
2362	S[707]	-5559.23	275
2363	S[706]	-5570.23	365
2364	S[705]	-5581.23	185
2365	S[704]	-5592.23	275
2366	S[703]	-5603.22	365
2367	S[702]	-5614.22	185
2368	S[701]	-5625.22	275
2369	S[700]	-5636.22	365
2370	S[699]	-5647.21	185
2371	S[698]	-5658.21	275
2372	S[697]	-5669.21	365
2373	S[696]	-5680.21	185
2374	S[695]	-5691.2	275
2375	S[694]	-5702.2	365
2376	S[693]	-5713.2	185
2377	S[692]	-5724.2	275
2378	S[691]	-5735.19	365
2379	S[690]	-5746.19	185
2380	S[689]	-5757.19	275
2381	S[688]	-5768.19	365
2382	S[687]	-5779.18	185
2383	S[686]	-5790.18	275
2384	S[685]	-5801.18	365
2385	S[684]	-5812.18	185
2386	S[683]	-5823.17	275
2387	S[682]	-5834.17	365
2388	S[681]	-5845.17	185
2389	S[680]	-5856.17	275
2390	S[679]	-5867.16	365
2391	S[678]	-5878.16	185
2392	S[677]	-5889.16	275
2393	S[676]	-5900.16	365
2394	S[675]	-5911.15	185
2395	S[674]	-5922.15	275
2396	S[673]	-5933.15	365
2397	S[672]	-5944.15	185
2398	S[671]	-5955.14	275
2399	S[670]	-5966.14	365
2400	S[669]	-5977.14	185

No.	Name	X	Y
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2403	S[666]	-6010.13	185
2404	S[665]	-6021.13	275
2405	S[664]	-6032.13	365
2406	S[663]	-6043.12	185
2407	S[662]	-6054.12	275
2408	S[661]	-6065.12	365
2409	S[660]	-6076.12	185
2410	S[659]	-6087.11	275
2411	S[658]	-6098.11	365
2412	S[657]	-6109.11	185
2413	S[656]	-6120.11	275
2414	S[655]	-6131.1	365
2415	S[654]	-6142.1	185
2416	S[653]	-6153.1	275
2417	S[652]	-6164.1	365
2418	S[651]	-6175.09	185
2419	S[650]	-6186.09	275
2420	S[649]	-6197.09	365
2421	S[648]	-6208.09	185
2422	S[647]	-6219.08	275
2423	S[646]	-6230.08	365
2424	S[645]	-6241.08	185
2425	S[644]	-6252.08	275
2426	S[643]	-6263.07	365
2427	S[642]	-6274.07	185
2428	S[641]	-6285.07	275
2429	S[640]	-6296.07	365
2430	S[639]	-6307.06	185
2431	S[638]	-6318.06	275
2432	S[637]	-6329.06	365
2433	S[636]	-6340.06	185
2434	S[635]	-6351.05	275
2435	S[634]	-6362.05	365
2436	S[633]	-6373.05	185
2437	S[632]	-6384.05	275
2438	S[631]	-6395.04	365
2439	S[630]	-6406.04	185
2440	S[629]	-6417.04	275
2441	S[628]	-6428.04	365
2442	S[627]	-6439.03	185
2443	S[626]	-6450.03	275
2444	S[625]	-6461.03	365
2445	S[624]	-6472.03	185
2446	S[623]	-6483.02	275
2447	S[622]	-6494.02	365
2448	S[621]	-6505.02	185
2449	S[620]	-6516.02	275
2450	S[619]	-6527.01	365
2451	S[618]	-6538.01	185
2452	S[617]	-6549.01	275
2453	S[616]	-6560.01	365
2454	S[615]	-6571	185
2455	S[614]	-6582	275
2456	S[613]	-6593	365
2457	S[612]	-6604	185
2458	S[611]	-6614.99	275
2459	S[610]	-6625.99	365
2460	S[609]	-6636.99	185
2461	S[608]	-6647.99	275
2462	S[607]	-6658.98	365
2463	S[606]	-6669.98	185
2464	S[605]	-6680.98	275
2465	S[604]	-6691.98	365
2466	S[603]	-6702.97	185
2467	S[602]	-6713.97	275
2468	S[601]	-6724.97	365
2469	DUMMY53	-6735.97	185
2470	DUMMY54	-6746.96	275
2471	DUMMY55	-6757.96	365
2472	DUMMY56	-6768.96	185
2473	DUMMY57	-6779.96	275
2474	DUMMY58	-6790.95	365
2475	DUMMY59	-6801.95	185
2476	DUMMY60	-6812.95	275
2477	DUMMY61	-6823.95	365
2478	DUMMY62	-6834.94	185
2479	DUMMY63	-6845.94	275
2480	DUMMY64	-6856.94	365
2481	DUMMY65	-6867.94	185
2482	DUMMY66	-6878.93	275
2483	DUMMY67	-6889.93	365
2484	DUMMY68	-6900.93	185
2485	DUMMY69	-6911.93	275
2486	DUMMY70	-6922.92	365
2487	S[600]	-6933.92	185
2488	S[599]	-6944.92	275
2489	S[598]	-6955.92	365
2490	S[597]	-6966.91	185
2491	S[596]	-6977.91	275
2492	S[595]	-6988.91	365
2493	S[594]	-6999.91	185
2494	S[593]	-7010.9	275
2495	S[592]	-7021.9	365
2496	S[591]	-7032.9	185
2497	S[590]	-7043.9	275
2498	S[589]	-7054.89	365
2499	S[588]	-7065.89	185
2500	S[587]	-7076.89	275

No.	Name	X	Y
2501	S[586]	-7087.89	365
2502	S[585]	-7098.88	185
2503	S[584]	-7109.88	275
2504	S[583]	-7120.88	365
2505	S[582]	-7131.88	185
2506	S[581]	-7142.87	275
2507	S[580]	-7153.87	365
2508	S[579]	-7164.87	185
2509	S[578]	-7175.87	275
2510	S[577]	-7186.86	365
2511	S[576]	-7197.86	185
2512	S[575]	-7208.86	275
2513	S[574]	-7219.86	365
2514	S[573]	-7230.85	185
2515	S[572]	-7241.85	275
2516	S[571]	-7252.85	365
2517	S[570]	-7263.85	185
2518	S[569]	-7274.84	275
2519	S[568]	-7285.84	365
2520	S[567]	-7296.84	185
2521	S[566]	-7307.84	275
2522	S[565]	-7318.83	365
2523	S[564]	-7329.83	185
2524	S[563]	-7340.83	275
2525	S[562]	-7351.83	365
2526	S[561]	-7362.82	185
2527	S[560]	-7373.82	275
2528	S[559]	-7384.82	365
2529	S[558]	-7395.82	185
2530	S[557]	-7406.81	275
2531	S[556]	-7417.81	365
2532	S[555]	-7428.81	185
2533	S[554]	-7439.81	275
2534	S[553]	-7450.8	365
2535	S[552]	-7461.8	185
2536	S[551]	-7472.8	275
2537	S[550]	-7483.8	365
2538	S[549]	-7494.79	185
2539	S[548]	-7505.79	275
2540	S[547]	-7516.79	365
2541	S[546]	-7527.79	185
2542	S[545]	-7538.78	275
2543	S[544]	-7549.78	365
2544	S[543]	-7560.78	185
2545	S[542]	-7571.78	275
2546	S[541]	-7582.77	365
2547	S[540]	-7593.77	185
2548	S[539]	-7604.77	275
2549	S[538]	-7615.77	365
2550	S[537]	-7626.76	185
2551	S[536]	-7637.76	275
2552	S[535]	-7648.76	365
2553	S[534]	-7659.76	185
2554	S[533]	-7670.75	275
2555	S[532]	-7681.75	365
2556	S[531]	-7692.75	185
2557	S[530]	-7703.75	275
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2559	S[528]	-7725.74	185
2560	S[527]	-7736.74	275
2561	S[526]	-7747.74	365
2562	S[525]	-7758.73	185
2563	S[524]	-7769.73	275
2564	S[523]	-7780.73	365
2565	S[522]	-7791.73	185
2566	S[521]	-7802.72	275
2567	S[520]	-7813.72	365
2568	S[519]	-7824.72	185
2569	S[518]	-7835.72	275
2570	S[517]	-7846.71	365
2571	S[516]	-7857.71	185
2572	S[515]	-7868.71	275
2573	S[514]	-7879.71	365
2574	S[513]	-7890.7	185
2575	S[512]	-7901.7	275
2576	S[511]	-7912.7	365
2577	S[510]	-7923.7	185
2578	S[509]	-7934.69	275
2579	S[508]	-7945.69	365
2580	S[507]	-7956.69	185
2581	S[506]	-7967.69	275
2582	S[505]	-7978.68	365
2583	S[504]	-7989.68	185
2584	S[503]	-8000.68	275
2585	S[502]	-8011.68	365
2586	S[501]	-8022.67	185
2587	S[500]	-8033.67	275
2588	S[499]	-8044.67	365
2589	S[498]	-8055.67	185
2590	S[497]	-8066.66	275
2591	S[496]	-8077.66	365
2592	S[495]	-8088.66	185
2593	S[494]	-8099.66	275
2594	S[493]	-8110.65	365
2595	S[492]	-8121.65	185
2596	S[491]	-8132.65	275
2597	S[490]	-8143.65	365
2598	S[489]	-8154.64	185
2599	S[488]	-8165.64	275
2600	S[487]	-8176.64	365

No.	Name	X	Y
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2604	S[483]	-8220.63	185
2605	S[482]	-8231.63	275
2606	S[481]	-8242.62	365
2607	S[480]	-8253.62	185
2608	S[479]	-8264.62	275
2609	S[478]	-8275.62	365
2610	S[477]	-8286.61	185
2611	S[476]	-8297.61	275
2612	S[475]	-8308.61	365
2613	S[474]	-8319.61	185
2614	S[473]	-8330.6	275
2615	S[472]	-8341.6	365
2616	S[471]	-8352.6	185
2617	S[470]	-8363.6	275
2618	S[469]	-8374.59	365
2619	S[468]	-8385.59	185
2620	S[467]	-8396.59	275
2621	S[466]	-8407.59	365
2622	S[465]	-8418.58	185
2623	S[464]	-8429.58	275
2624	S[463]	-8440.58	365
2625	S[462]	-8451.58	185
2626	S[461]	-8462.57	275
2627	S[460]	-8473.57	365
2628	S[459]	-8484.57	185
2629	S[458]	-8495.57	275
2630	S[457]	-8506.56	365
2631	S[456]	-8517.56	185
2632	S[455]	-8528.56	275
2633	S[454]	-8539.56	365
2634	S[453]	-8550.55	185
2635	S[452]	-8561.55	275
2636	S[451]	-8572.55	365
2637	S[450]	-8583.55	185
2638	S[449]	-8594.54	275
2639	S[448]	-8605.54	365
2640	S[447]	-8616.54	185
2641	S[446]	-8627.54	275
2642	S[445]	-8638.53	365
2643	S[444]	-8649.53	185
2644	S[443]	-8660.53	275
2645	S[442]	-8671.53	365
2646	S[441]	-8682.52	185
2647	S[440]	-8693.52	275
2648	S[439]	-8704.52	365
2649	S[438]	-8715.52	185
2650	S[437]	-8726.51	275
2651	S[436]	-8737.51	365
2652	S[435]	-8748.51	185
2653	S[434]	-8759.51	275
2654	S[433]	-8770.5	365
2655	S[432]	-8781.5	185
2656	S[431]	-8792.5	275
2657	S[430]	-8803.5	365
2658	S[429]	-8814.49	185
2659	S[428]	-8825.49	275
2660	S[427]	-8836.49	365
2661	S[426]	-8847.49	185
2662	S[425]	-8858.48	275
2663	S[424]	-8869.48	365
2664	S[423]	-8880.48	185
2665	S[422]	-8891.48	275
2666	S[421]	-8902.47	365
2667	S[420]	-8913.47	185
2668	S[419]	-8924.47	275
2669	S[418]	-8935.47	365
2670	S[417]	-8946.46	185
2671	S[416]	-8957.46	275
2672	S[415]	-8968.46	365
2673	S[414]	-8979.46	185
2674	S[413]	-8990.45	275
2675	S[412]	-9001.45	365
2676	S[411]	-9012.45	185
2677	S[410]	-9023.45	275
2678	S[409]	-9034.44	365
2679	S[408]	-9045.44	185
2680	S[407]	-9056.44	275
2681	S[406]	-9067.44	365
2682	S[405]	-9078.43	185
2683	S[404]	-9089.43	275
2684	S[403]	-9100.43	365
2685	S[402]	-9111.43	185
2686	S[401]	-9122.42	275
2687	S[400]	-9133.42	365
2688	S[399]	-9144.42	185
2689	S[398]	-9155.42	275
2690	S[397]	-9166.41	365
2691	S[396]	-9177.41	185
2692	S[395]	-9188.41	275
2693	S[394]	-9199.41	365
2694	S[393]	-9210.4	185
2695	S[392]	-9221.4	275
2696	S[391]	-9232.4	365
2697	S[390]	-9243.4	185
2698	S[389]	-9254.39	275
2699	S[388]	-9265.39	365
2700	S[387]	-9276.39	185

No.	Name	X	Y
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2702	S[385]	-9298.38	365
2703	S[384]	-9309.38	185
2704	S[383]	-9320.38	275
2705	S[382]	-9331.38	365
2706	S[381]	-9342.37	185
2707	S[380]	-9353.37	275
2708	S[379]	-9364.37	365
2709	S[378]	-9375.37	185
2710	S[377]	-9386.36	275
2711	S[376]	-9397.36	365
2712	S[375]	-9408.36	185
2713	S[374]	-9419.36	275
2714	S[373]	-9430.35	365
2715	S[372]	-9441.35	185
2716	S[371]	-9452.35	275
2717	S[370]	-9463.35	365
2718	S[369]	-9474.34	185
2719	S[368]	-9485.34	275
2720	S[367]	-9496.34	365
2721	S[366]	-9507.34	185
2722	S[365]	-9518.33	275
2723	S[364]	-9529.33	365
2724	S[363]	-9540.33	185
2725	S[362]	-9551.33	275
2726	S[361]	-9562.32	365
2727	S[360]	-9573.32	185
2728	S[359]	-9584.32	275
2729	S[358]	-9595.32	365
2730	S[357]	-9606.31	185
2731	S[356]	-9617.31	275
2732	S[355]	-9628.31	365
2733	S[354]	-9639.31	185
2734	S[353]	-9650.3	275
2735	S[352]	-9661.3	365
2736	S[351]	-9672.3	185
2737	S[350]	-9683.3	275
2738	S[349]	-9694.29	365
2739	S[348]	-9705.29	185
2740	S[347]	-9716.29	275
2741	S[346]	-9727.29	365
2742	S[345]	-9738.28	185
2743	S[344]	-9749.28	275
2744	S[343]	-9760.28	365
2745	S[342]	-9771.28	185
2746	S[341]	-9782.27	275
2747	S[340]	-9793.27	365
2748	S[339]	-9804.27	185
2749	S[338]	-9815.27	275
2750	S[337]	-9826.26	365
2751	S[336]	-9837.26	185
2752	S[335]	-9848.26	275
2753	S[334]	-9859.26	365
2754	S[333]	-9870.25	185
2755	S[332]	-9881.25	275
2756	S[331]	-9892.25	365
2757	S[330]	-9903.25	185
2758	S[329]	-9914.24	275
2759	S[328]	-9925.24	365
2760	S[327]	-9936.24	185
2761	S[326]	-9947.24	275
2762	S[325]	-9958.23	365
2763	S[324]	-9969.23	185
2764	S[323]	-9980.23	275
2765	S[322]	-9991.23	365
2766	S[321]	-10002.22	185
2767	S[320]	-10013.22	275
2768	S[319]	-10024.22	365
2769	S[318]	-10035.22	185
2770	S[317]	-10046.21	275
2771	S[316]	-10057.21	365
2772	S[315]	-10068.21	185
2773	S[314]	-10079.21	275
2774	S[313]	-10090.2	365
2775	S[312]	-10101.2	185
2776	S[311]	-10112.2	275
2777	S[310]	-10123.2	365
2778	S[309]	-10134.19	185
2779	S[308]	-10145.19	275
2780	S[307]	-10156.19	365
2781	S[306]	-10167.19	185
2782	S[305]	-10178.18	275
2783	S[304]	-10189.18	365
2784	S[303]	-10200.18	185
2785	S[302]	-10211.18	275
2786	S[301]	-10222.17	365
2787	S[300]	-10233.17	185
2788	S[299]	-10244.17	275
2789	S[298]	-10255.17	365
2790	S[297]	-10266.16	185
2791	S[296]	-10277.16	275
2792	S[295]	-10288.16	365
2793	S[294]	-10299.16	185
2794	S[293]	-10310.15	275
2795	S[292]	-10321.15	365
2796	S[291]	-10332.15	185
2797	S[290]	-10343.15	275
2798	S[289]	-10354.14	365
2799	S[288]	-10365.14	185
2800	S[287]	-10376.14	275

No.	Name	X	Y
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2802	S[285]	-10398.13	185
2803	S[284]	-10409.13	275
2804	S[283]	-10420.13	365
2805	S[282]	-10431.13	185
2806	S[281]	-10442.12	275
2807	S[280]	-10453.12	365
2808	S[279]	-10464.12	185
2809	S[278]	-10475.12	275
2810	S[277]	-10486.11	365
2811	S[276]	-10497.11	185
2812	S[275]	-10508.11	275
2813	S[274]	-10519.11	365
2814	S[273]	-10530.1	185
2815	S[272]	-10541.1	275
2816	S[271]	-10552.1	365
2817	S[270]	-10563.1	185
2818	S[269]	-10574.09	275
2819	S[268]	-10585.09	365
2820	S[267]	-10596.09	185
2821	S[266]	-10607.09	275
2822	S[265]	-10618.08	365
2823	S[264]	-10629.08	185
2824	S[263]	-10640.08	275
2825	S[262]	-10651.08	365
2826	S[261]	-10662.07	185
2827	S[260]	-10673.07	275
2828	S[259]	-10684.07	365
2829	S[258]	-10695.07	185
2830	S[257]	-10706.06	275
2831	S[256]	-10717.06	365
2832	S[255]	-10728.06	185
2833	S[254]	-10739.06	275
2834	S[253]	-10750.05	365
2835	S[252]	-10761.05	185
2836	S[251]	-10772.05	275
2837	S[250]	-10783.05	365
2838	S[249]	-10794.04	185
2839	S[248]	-10805.04	275
2840	S[247]	-10816.04	365
2841	S[246]	-10827.04	185
2842	S[245]	-10838.03	275
2843	S[244]	-10849.03	365
2844	S[243]	-10860.03	185
2845	S[242]	-10871.03	275
2846	S[241]	-10882.02	365
2847	S[240]	-10893.02	185
2848	S[239]	-10904.02	275
2849	S[238]	-10915.02	365
2850	S[237]	-10926.01	185
2851	S[236]	-10937.01	275
2852	S[235]	-10948.01	365
2853	S[234]	-10959.01	185
2854	S[233]	-10970	275
2855	S[232]	-10981	365
2856	S[231]	-10992	185
2857	S[230]	-11003	275
2858	S[229]	-11013.99	365
2859	S[228]	-11024.99	185
2860	S[227]	-11035.99	275
2861	S[226]	-11046.99	365
2862	S[225]	-11057.98	185
2863	S[224]	-11068.98	275
2864	S[223]	-11079.98	365
2865	S[222]	-11090.98	185
2866	S[221]	-11101.97	275
2867	S[220]	-11112.97	365
2868	S[219]	-11123.97	185
2869	S[218]	-11134.97	275
2870	S[217]	-11145.96	365
2871	S[216]	-11156.96	185
2872	S[215]	-11167.96	275
2873	S[214]	-11178.96	365
2874	S[213]	-11189.95	185
2875	S[212]	-11200.95	275
2876	S[211]	-11211.95	365
2877	S[210]	-11222.95	185
2878	S[209]	-11233.94	275
2879	S[208]	-11244.94	365
2880	S[207]	-11255.94	185
2881	S[206]	-11266.94	275
2882	S[205]	-11277.93	365
2883	S[204]	-11288.93	185
2884	S[203]	-11299.93	275
2885	S[202]	-11310.93	365
2886	S[201]	-11321.92	185
2887	S[200]	-11332.92	275
2888	S[199]	-11343.92	365
2889	S[198]	-11354.92	185
2890	S[197]	-11365.91	275
2891	S[196]	-11376.91	365
2892	S[195]	-11387.91	185
2893	S[194]	-11398.91	275
2894	S[193]	-11409.9	365
2895	S[192]	-11420.9	185
2896	S[191]	-11431.9	275
2897	S[190]	-11442.9	365
2898	S[189]	-11453.89	185
2899	S[188]	-11464.89	275
2900	S[187]	-11475.89	365

No.	Name	X	Y
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2902	S[185]	-11497.88	275
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2904	S[183]	-11519.88	185
2905	S[182]	-11530.88	275
2906	S[181]	-11541.87	365
2907	S[180]	-11552.87	185
2908	S[179]	-11563.87	275
2909	S[178]	-11574.87	365
2910	S[177]	-11585.86	185
2911	S[176]	-11596.86	275
2912	S[175]	-11607.86	365
2913	S[174]	-11618.86	185
2914	S[173]	-11629.85	275
2915	S[172]	-11640.85	365
2916	S[171]	-11651.85	185
2917	S[170]	-11662.85	275
2918	S[169]	-11673.84	365
2919	S[168]	-11684.84	185
2920	S[167]	-11695.84	275
2921	S[166]	-11706.84	365
2922	S[165]	-11717.83	185
2923	S[164]	-11728.83	275
2924	S[163]	-11739.83	365
2925	S[162]	-11750.83	185
2926	S[161]	-11761.82	275
2927	S[160]	-11772.82	365
2928	S[159]	-11783.82	185
2929	S[158]	-11794.82	275
2930	S[157]	-11805.81	365
2931	S[156]	-11816.81	185
2932	S[155]	-11827.81	275
2933	S[154]	-11838.81	365
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2935	S[152]	-11860.8	275
2936	S[151]	-11871.8	365
2937	S[150]	-11882.8	185
2938	S[149]	-11893.79	275
2939	S[148]	-11904.79	365
2940	S[147]	-11915.79	185
2941	S[146]	-11926.79	275
2942	S[145]	-11937.78	365
2943	S[144]	-11948.78	185
2944	S[143]	-11959.78	275
2945	S[142]	-11970.78	365
2946	S[141]	-11981.77	185
2947	S[140]	-11992.77	275
2948	S[139]	-12003.77	365
2949	S[138]	-12014.77	185
2950	S[137]	-12025.76	275
2951	S[136]	-12036.76	365
2952	S[135]	-12047.76	185
2953	S[134]	-12058.76	275
2954	S[133]	-12069.75	365
2955	S[132]	-12080.75	185
2956	S[131]	-12091.75	275
2957	S[130]	-12102.75	365
2958	S[129]	-12113.74	185
2959	S[128]	-12124.74	275
2960	S[127]	-12135.74	365
2961	S[126]	-12146.74	185
2962	S[125]	-12157.73	275
2963	S[124]	-12168.73	365
2964	S[123]	-12179.73	185
2965	S[122]	-12190.73	275
2966	S[121]	-12201.72	365
2967	S[120]	-12212.72	185
2968	S[119]	-12223.72	275
2969	S[118]	-12234.72	365
2970	S[117]	-12245.71	185
2971	S[116]	-12256.71	275
2972	S[115]	-12267.71	365
2973	S[114]	-12278.71	185
2974	S[113]	-12289.7	275
2975	S[112]	-12300.7	365
2976	S[111]	-12311.7	185
2977	S[110]	-12322.7	275
2978	S[109]	-12333.69	365
2979	S[108]	-12344.69	185
2980	S[107]	-12355.69	275
2981	S[106]	-12366.69	365
2982	S[105]	-12377.68	185
2983	S[104]	-12388.68	275
2984	S[103]	-12399.68	365
2985	S[102]	-12410.68	185
2986	S[101]	-12421.67	275
2987	S[100]	-12432.67	365
2988	S[99]	-12443.67	185
2989	S[98]	-12454.67	275
2990	S[97]	-12465.66	365
2991	S[96]	-12476.66	185
2992	S[95]	-12487.66	275
2993	S[94]	-12498.66	365
2994	S[93]	-12509.65	185
2995	S[92]	-12520.65	275
2996	S[91]	-12531.65	365
2997	S[90]	-12542.65	185
2998	S[89]	-12553.64	275
2999	S[88]	-12564.64	365
3000	S[87]	-12575.64	185

No.	Name	X	Y
3001	S[86]	-12586.64	275
3002	S[85]	-12597.63	365
3003	S[84]	-12608.63	185
3004	S[83]	-12619.63	275
3005	S[82]	-12630.63	365
3006	S[81]	-12641.62	185
3007	S[80]	-12652.62	275
3008	S[79]	-12663.62	365
3009	S[78]	-12674.62	185
3010	S[77]	-12685.61	275
3011	S[76]	-12696.61	365
3012	S[75]	-12707.61	185
3013	S[74]	-12718.61	275
3014	S[73]	-12729.6	365
3015	S[72]	-12740.6	185
3016	S[71]	-12751.6	275
3017	S[70]	-12762.6	365
3018	S[69]	-12773.59	185
3019	S[68]	-12784.59	275
3020	S[67]	-12795.59	365
3021	S[66]	-12806.59	185
3022	S[65]	-12817.58	275
3023	S[64]	-12828.58	365
3024	S[63]	-12839.58	185
3025	S[62]	-12850.58	275
3026	S[61]	-12861.57	365
3027	S[60]	-12872.57	185
3028	S[59]	-12883.57	275
3029	S[58]	-12894.57	365
3030	S[57]	-12905.56	185
3031	S[56]	-12916.56	275
3032	S[55]	-12927.56	365
3033	S[54]	-12938.56	185
3034	S[53]	-12949.55	275
3035	S[52]	-12960.55	365
3036	S[51]	-12971.55	185
3037	S[50]	-12982.55	275
3038	S[49]	-12993.54	365
3039	S[48]	-13004.54	185
3040	S[47]	-13015.54	275
3041	S[46]	-13026.54	365
3042	S[45]	-13037.53	185
3043	S[44]	-13048.53	275
3044	S[43]	-13059.53	365
3045	S[42]	-13070.53	185
3046	S[41]	-13081.52	275
3047	S[40]	-13092.52	365
3048	S[39]	-13103.52	185
3049	S[38]	-13114.52	275
3050	S[37]	-13125.51	365
3051	S[36]	-13136.51	185
3052	S[35]	-13147.51	275
3053	S[34]	-13158.51	365
3054	S[33]	-13169.5	185
3055	S[32]	-13180.5	275
3056	S[31]	-13191.5	365
3057	S[30]	-13202.5	185
3058	S[29]	-13213.49	275
3059	S[28]	-13224.49	365
3060	S[27]	-13235.49	185
3061	S[26]	-13246.49	275
3062	S[25]	-13257.48	365
3063	S[24]	-13268.48	185
3064	S[23]	-13279.48	275
3065	S[22]	-13290.48	365
3066	S[21]	-13301.47	185
3067	S[20]	-13312.47	275
3068	S[19]	-13323.47	365
3069	S[18]	-13334.47	185
3070	S[17]	-13345.46	275
3071	S[16]	-13356.46	365
3072	S[15]	-13367.46	185
3073	S[14]	-13378.46	275
3074	S[13]	-13389.45	365
3075	S[12]	-13400.45	185
3076	S[11]	-13411.45	275
3077	S[10]	-13422.45	365
3078	S[9]	-13433.44	185
3079	S[8]	-13444.44	275
3080	S[7]	-13455.44	365
3081	S[6]	-13466.44	185
3082	S[5]	-13477.43	275
3083	S[4]	-13488.43	365
3084	S[3]	-13499.43	185
3085	S[2]	-13510.43	275
3086	S[1]	-13521.42	365
3087	SDUM[1]	-13532.42	185
3088	SDUM[0]	-13543.42	275
3089	DUMMY73	-13554.42	365
3090	DUMMY74	-13565.41	185
3091	DUMMY75	-13576.41	275
3092	DUMMY76	-13587.41	365
3093	DUMMY77	-13598.41	185
3094	DUMMY78	-13609.4	275
3095	DUMMY79	-13620.4	365
3096	DUMMY83	-13631.4	185
3097	DUMMY84	-13642.4	275
3098	DUMMY85	-13653.39	365
3099	DUMMY90	-13664.39	185
3100	DUMMY91	-13697.38	185

No.	Name	X	Y
3101	DUMMY92	-13752.37	365
3102	DUMMY93	-13774.37	275
3103	Alignment mark L1	13706	372.5
3104	Alignment mark L2	13706	285.5
3105	Alignment mark R1	-13706	372.5
3106	Alignment mark R2	-13706	285.5

4. System Interface

4.1. DSI System Interface

4.1.1. General Description

The pad mapping of MIPI DSI interface is set by IM[2:0] pin, LANSEL pins and MIPI_LANE_SEL register(as below table).

Table 2: DSI Interface Lane Mode Selection

External Pad Set				Register	Configuration of MIPI Lane				
LANSEL	IM2	IM1	IM0	Page4_R00h MIPI_LANE_SEL	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	0	1	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	1	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	1	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
0	1	0	0	1	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	1	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
0	1	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
1	0	0	0	1	-	-	CLKP/N	D1P/N	D0P/N
1	0	0	1	1	-	-	CLKN/P	D1N/P	D0N/P
1	0	1	0	1	D0P/N	D1P/N	CLKP/N	-	-
1	0	1	1	1	D0N/P	D1N/P	CLKN/P	-	-
1	1	0	0	1	-	D0P/N	CLKP/N	D1P/N	-
1	1	0	1	1	-	D0N/P	CLKN/P	D1N/P	-
1	1	1	0	1	-	D1P/N	CLKP/N	D0P/N	-
1	1	1	1	1	-	D1N/P	CLKN/P	D0N/P	-
0	0	0	0	0	-	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	0	-	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	0	D0P/N	D1P/N	CLKP/N	D2P/N	-
0	0	1	1	0	D0N/P	D1N/P	CLKN/P	D2N/P	-
0	1	0	0	0	-	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	0	-	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	0	D2P/N	D1P/N	CLKP/N	D0P/N	-
0	1	1	1	0	D2N/P	D1N/P	CLKN/P	D0N/P	-
Others					Reserved				

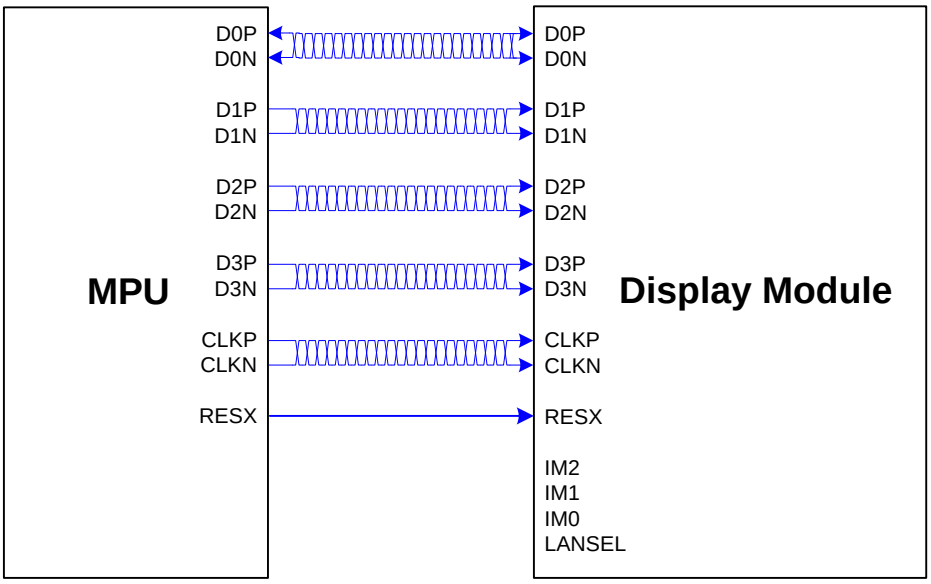


Figure 2: DSI System Interface Diagram

The communication is separated into two different levels between the MCU and the display module:

- Low level communication is done on the interface level.
- High level communication is done on the packet level.

4.1.2. Interface Level Communication

4.1.2.1. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 3: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. *Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.*
2. *If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.*
3. *n = 0, 1, 2 and 3 (D1P/N, D2 P/N and D3 P/N lanes only for HS-0 and HS-1)*

4.1.2.2. DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane are in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM).These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

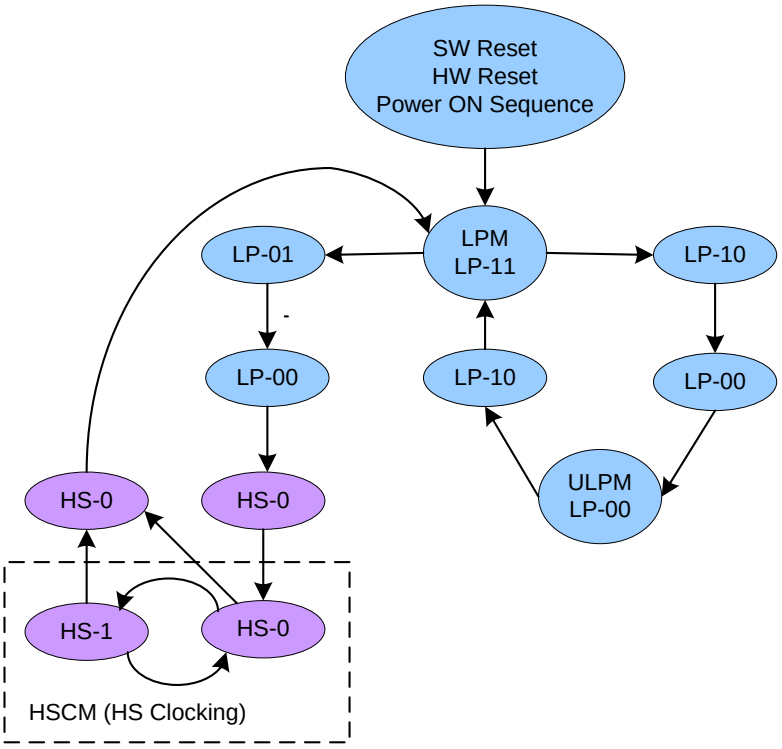


Figure 3: Clock lane Power Modes

4.1.2.2.1. Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11

2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

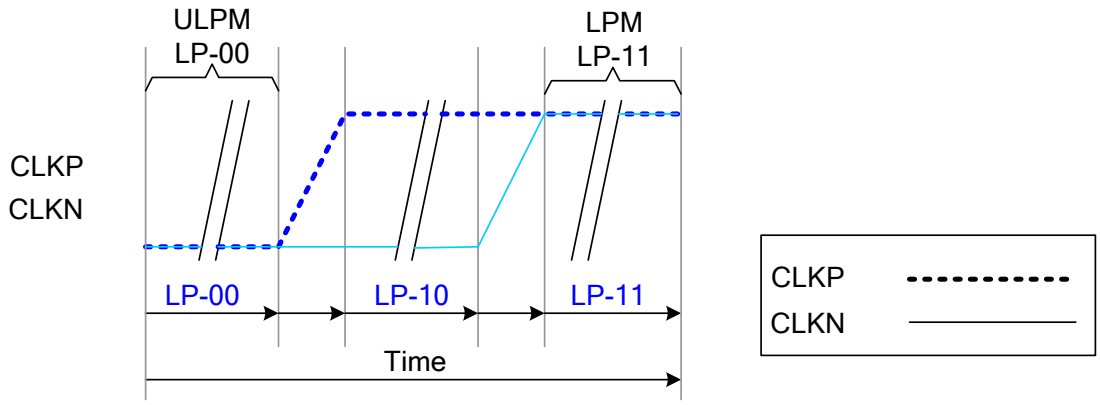


Figure 4: From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM). This sequence is illustrated below.

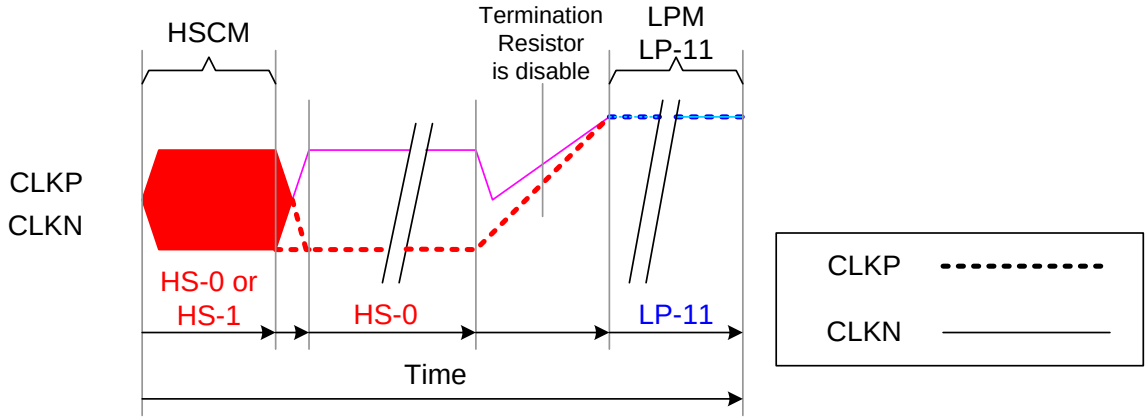


Figure 5: From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated in the flow chart below.

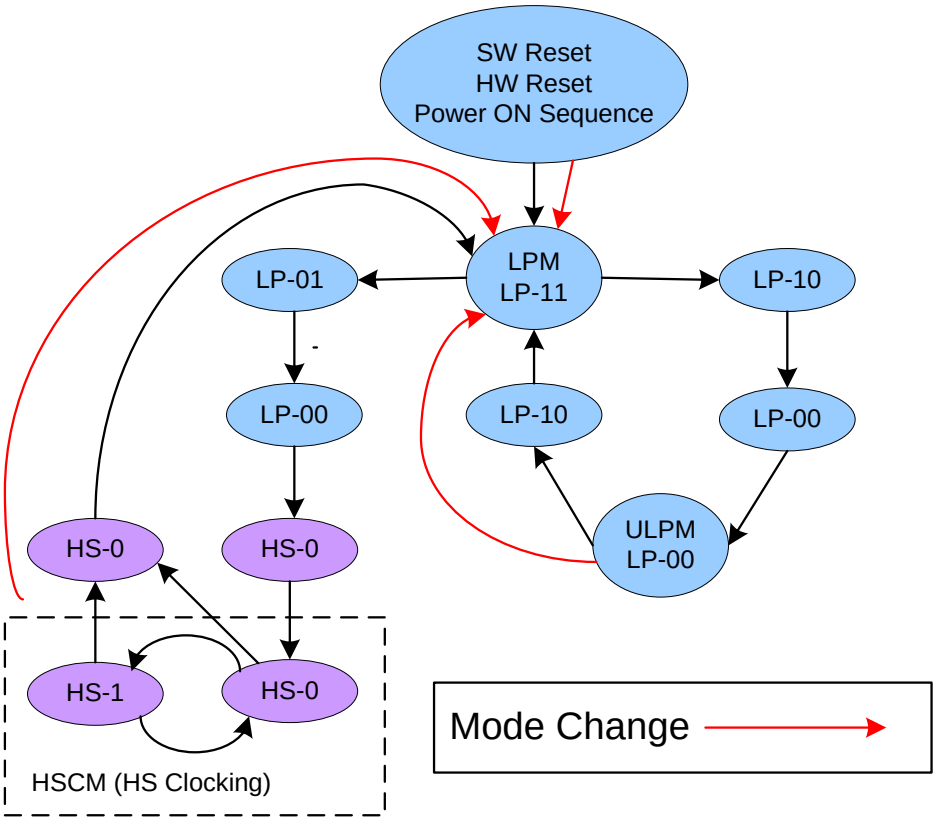


Figure 6: All Three Mode Changes to LPM

4.1.2.2.2. Ultra-Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Ultra-Low power Mode (ULPM) when CLK lanes enter the LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

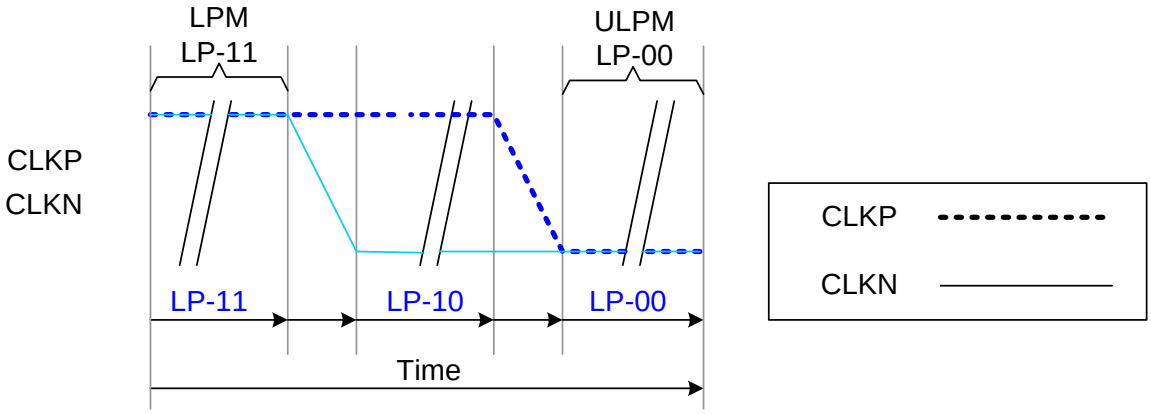


Figure 7: From LPM to ULPM

The mode change is also illustrated below.

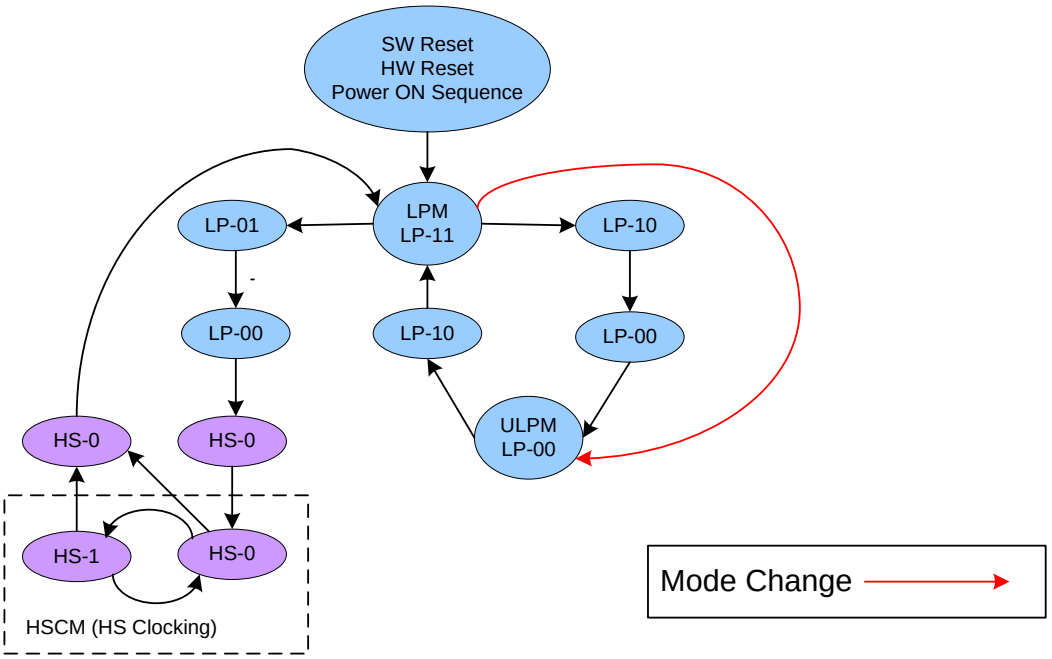


Figure 8: Mode Change from LPM to ULPM

4.1.2.2.3. High-Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

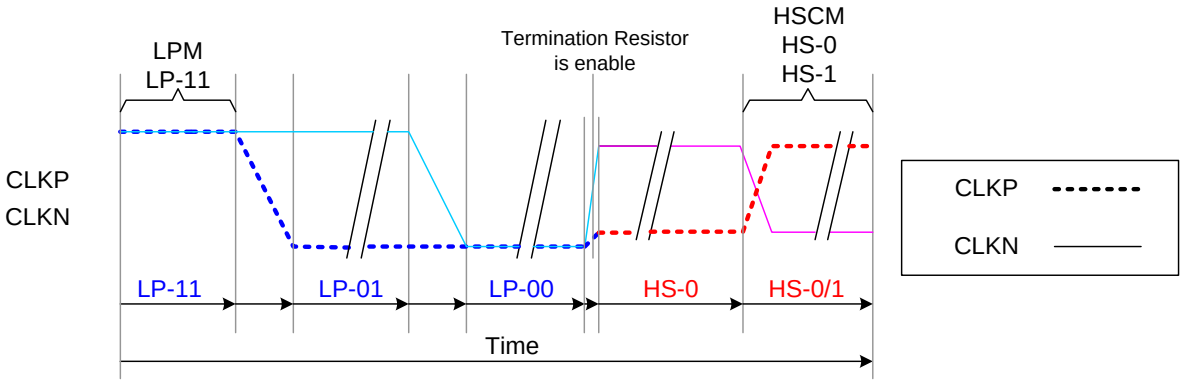


Figure 9: From LPM to HSCM

The mode change is also illustrated below.

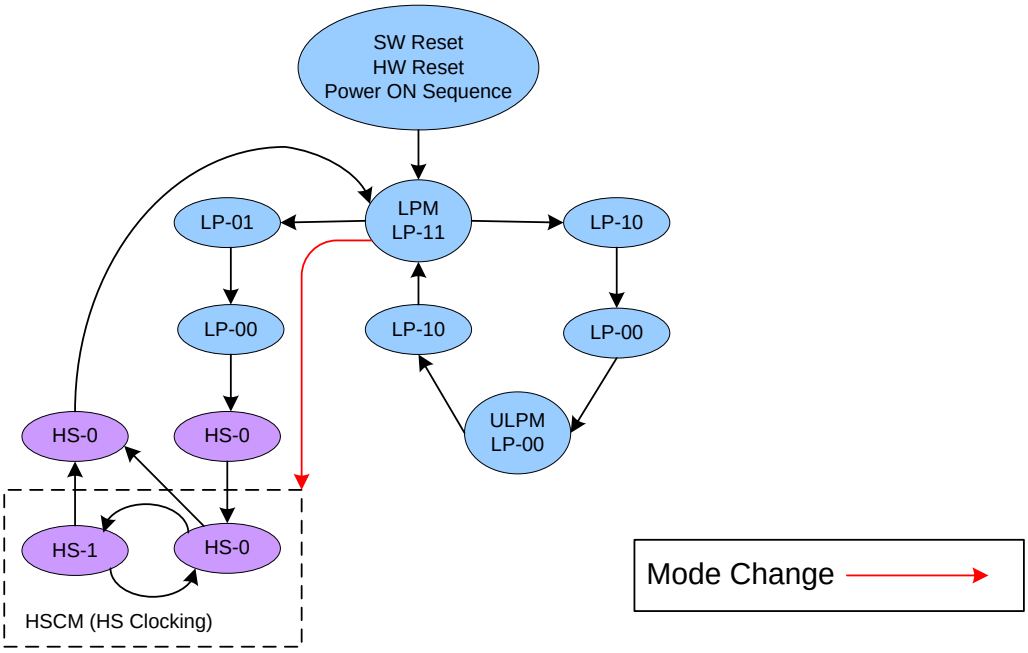


Figure 10: Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

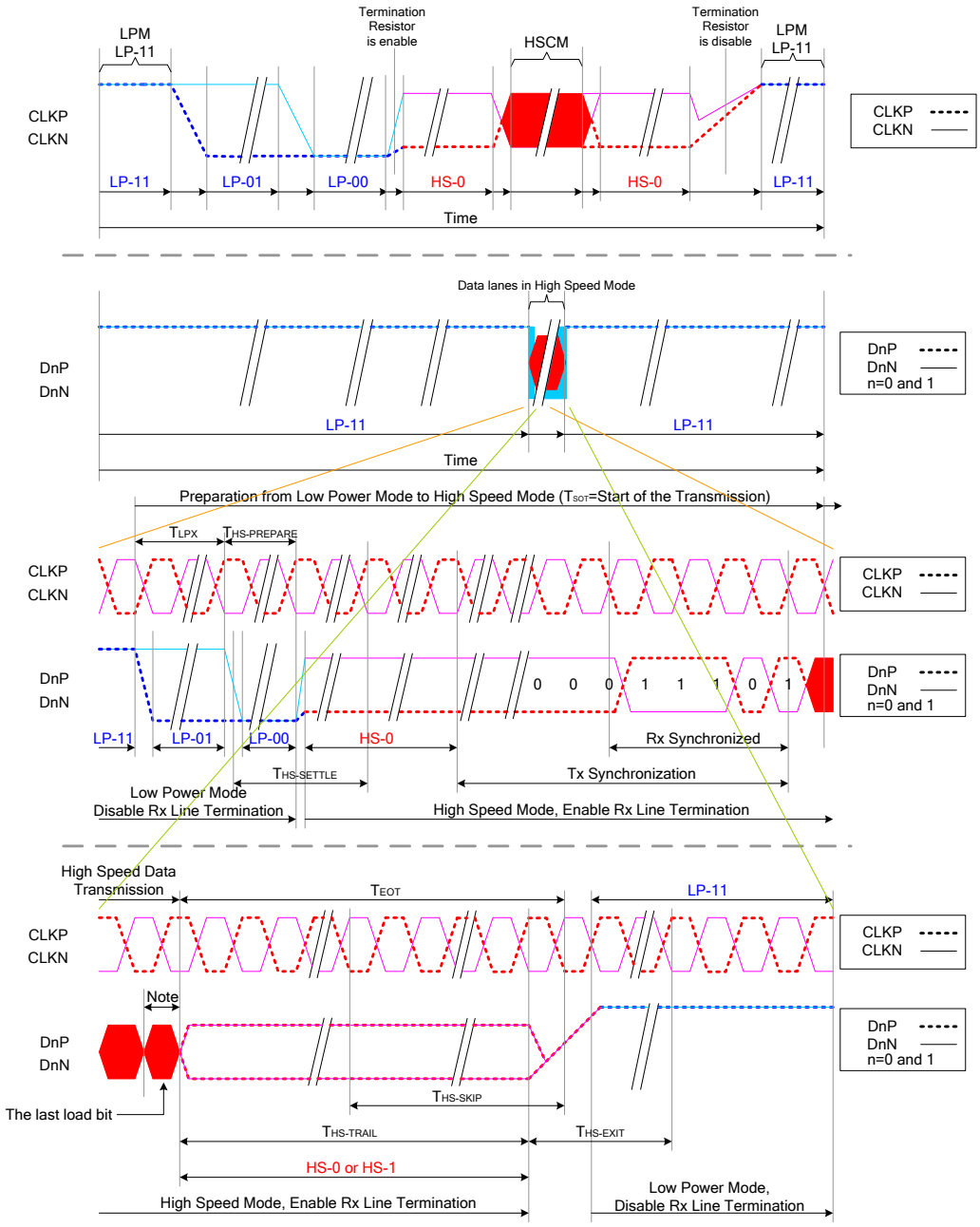


Figure 11: High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.1.2.3. DSI Data Lanes

4.1.2.3.1. General

D3P/N, D2P/N, D1P/N and D0P/N Data Lanes can be driven into different modes:

- Escape Mode (Only D0P/N data lane is used)
- High-Speed Data Transmission (all data lanes are used)
- Bus Turnaround Request (Only D0P/N data lane are used)

These modes and their entering codes are defined in the following table.

Table 4: Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode[1]	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission[2]	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request[3]	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

4.1.2.3.2. Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- Drive data lanes to “Ultra-Low Power State” (ULPS),
- Indicate “Remote Application Reset” (RAR), which can reset the display module,
- Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

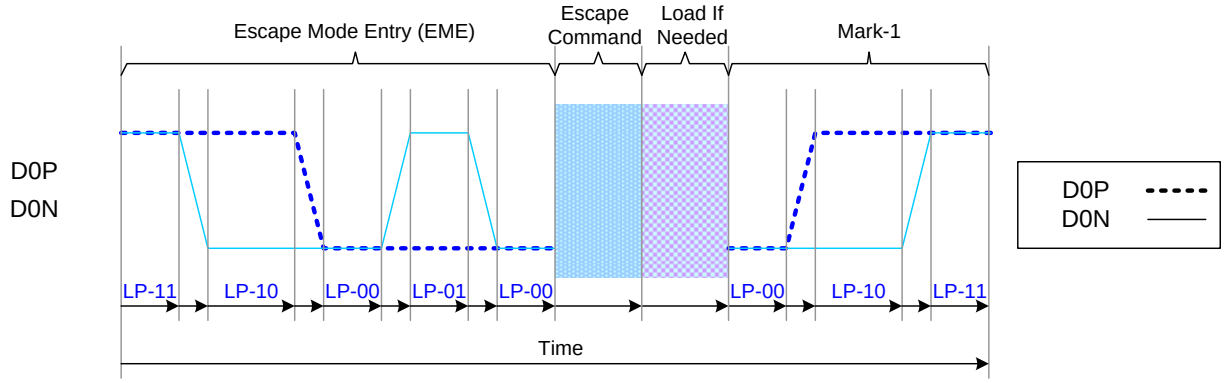


Figure 12 General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in Table 5: Escape Commands.

An example of the Mode type Escape Command is 'Ultra-Low Power Mode', where the MCU instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Table 5: Escape Commands

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, Note 1	Mode	1001 1111 b	-	-
Undefined-2, Note 1	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Unknown-5, Note 1	Trigger	1010 0000 b	-	-

Notes:

1. This Escape command support is not implemented on the display module.

2. n = 1

3. x = Supported

4. - = Not Supported

4.1.2.3.2.1. Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module also uses the same sequence when it sends data to the MCU. The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
  - ✧ One or more bytes (one byte = 8 bit)
  - ✧ Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

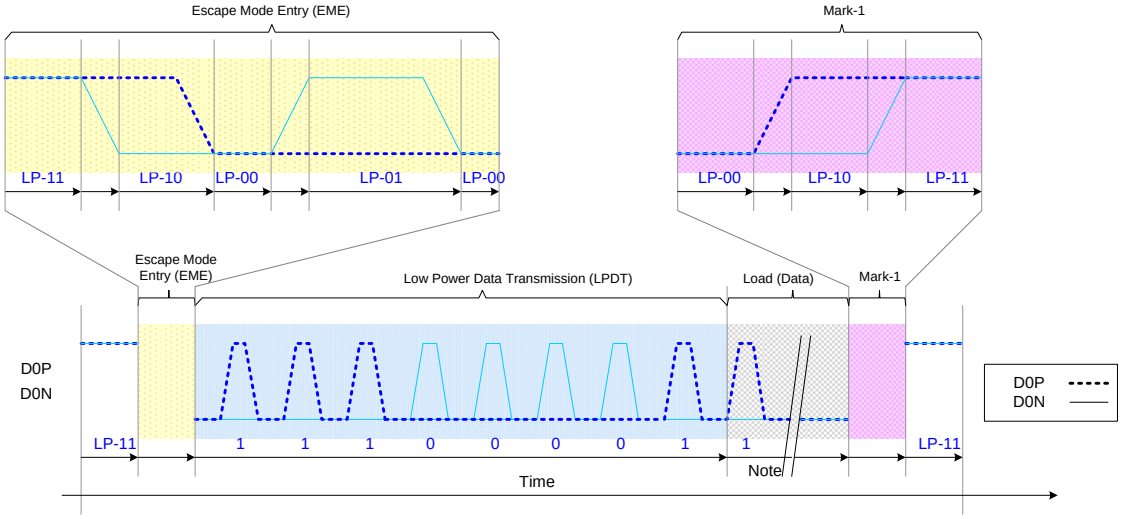


Figure 13: Low-Power Data Transmission (LPDT)

Note: *Load (Data) presents that the first bit is the logical 1 in this example.*

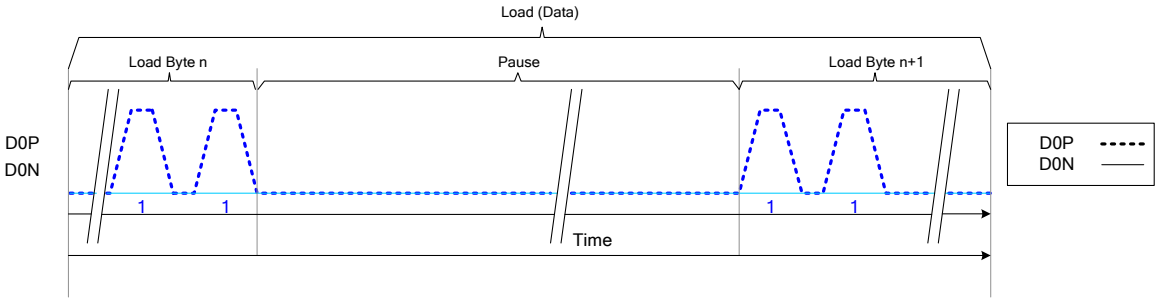


Figure 14: Pause (Example)

4.1.2.3.2.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

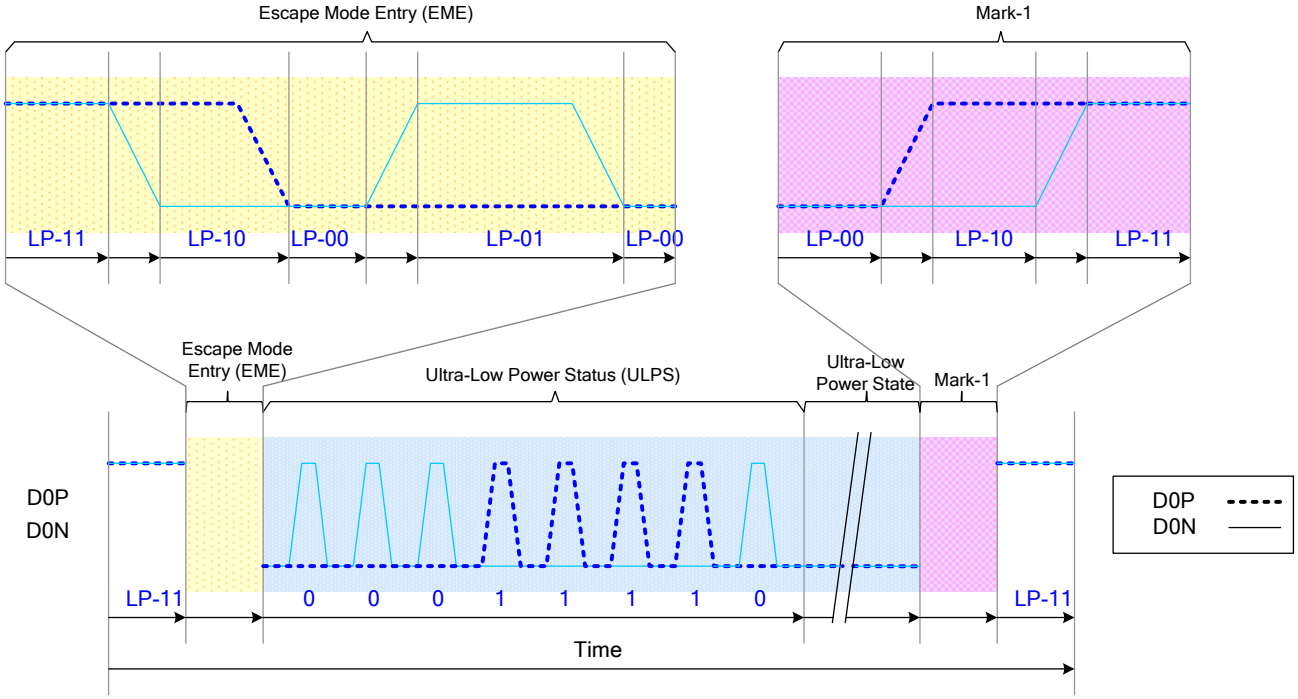


Figure 15: Ultra-Low Power State (ULPS)

4.1.2.3.2.3. Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

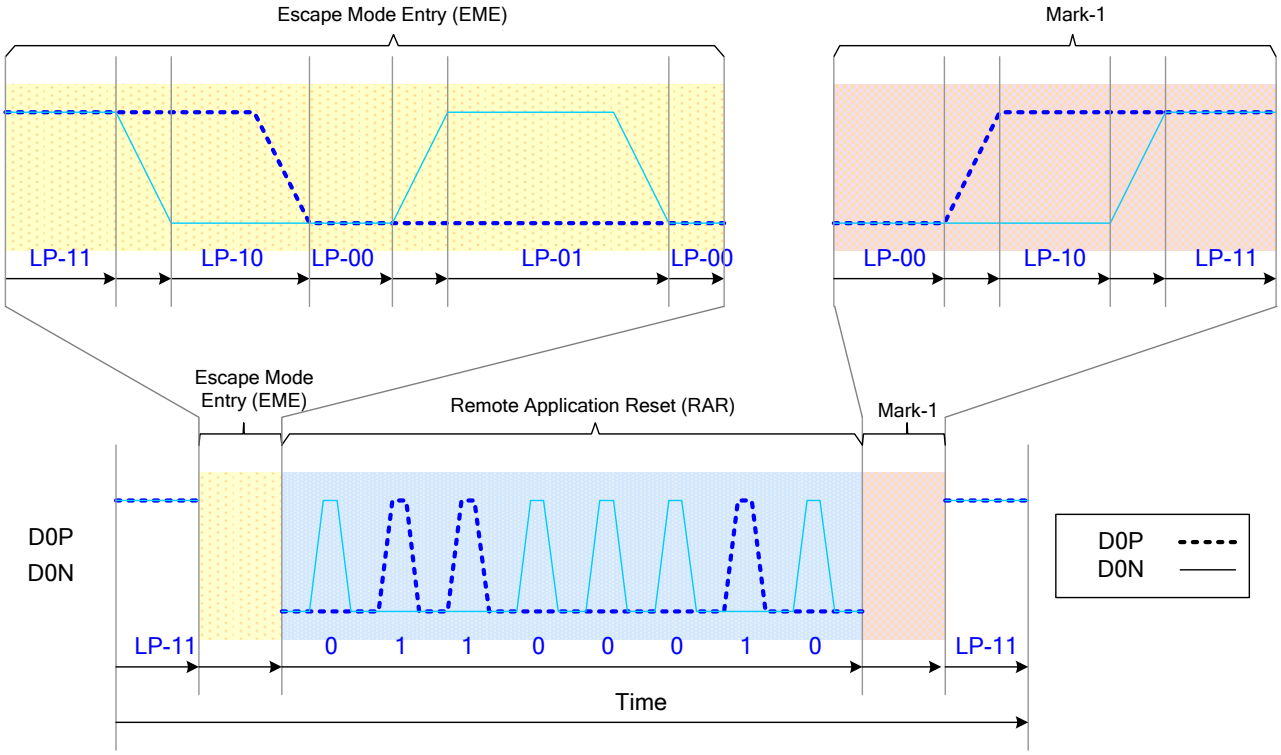


Figure 16: Remote Application Reset (RAR)

4.1.2.3.2.4. Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

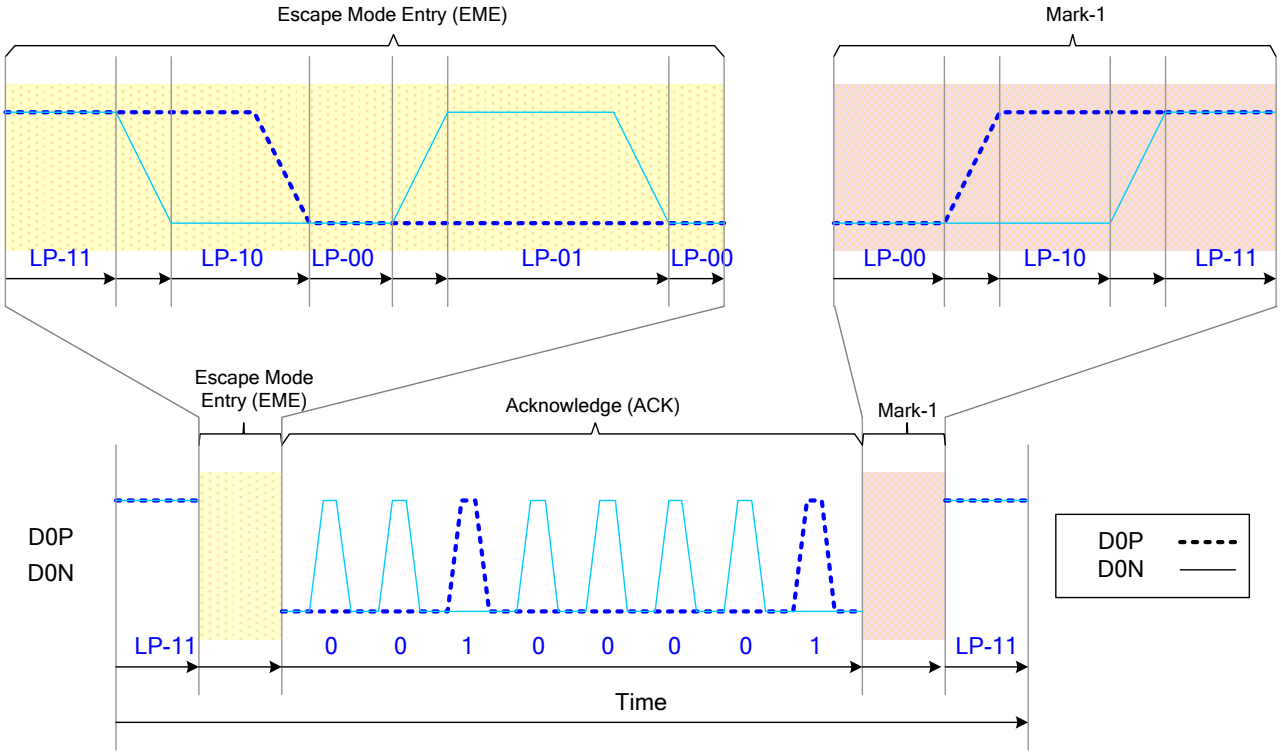


Figure 17: Acknowledge (ACK)

4.1.2.3.3. High-Speed Data Transmission (HSDT)

4.1.2.3.3.1. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “4.1.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

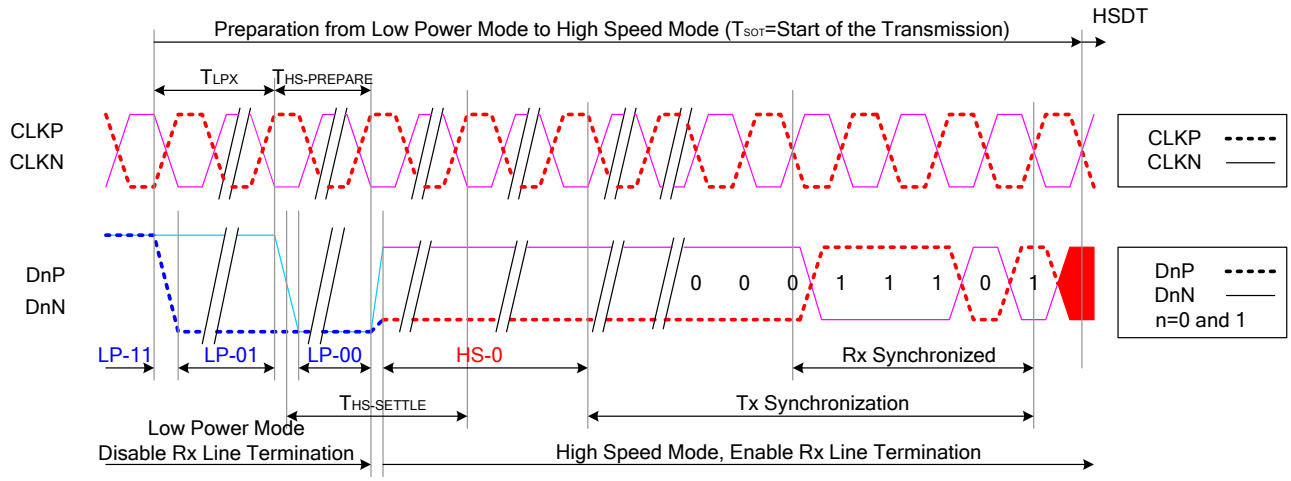


Figure 18: Entering High-Speed Data Transmission (TSOT of HSDT)

4.1.2.3.3.2. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D3P/N, D2P/N, D1P/N and D0P/N are in the LP-11 mode. See more information in the section “4.1.2.2.3 High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
  - ✧ MCU changes to HS-1, if the last load bit is HS-0
  - ✧ MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

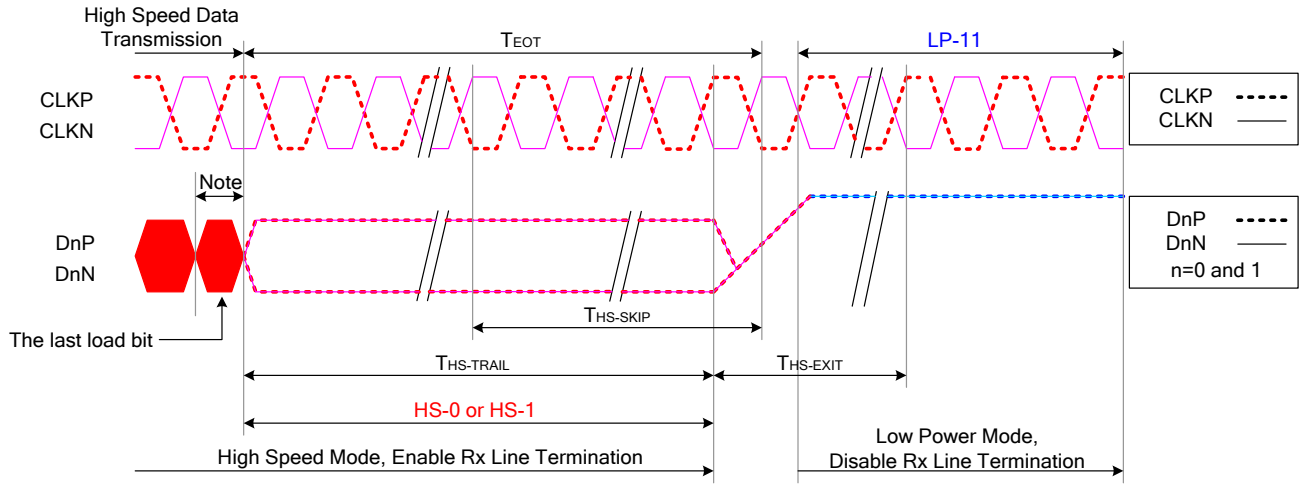


Figure 19: Leaving High-Speed Data Transmission (TEOT of HSDT)

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.1.2.3.3.3. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “4.1.3.1 Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

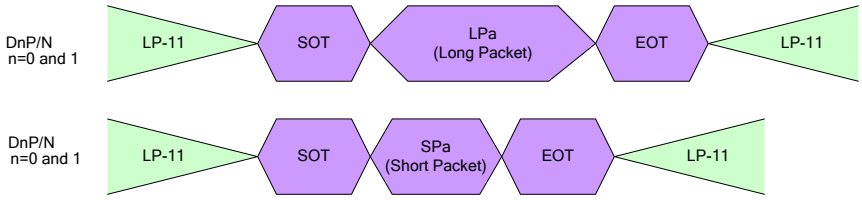


Figure 20: Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

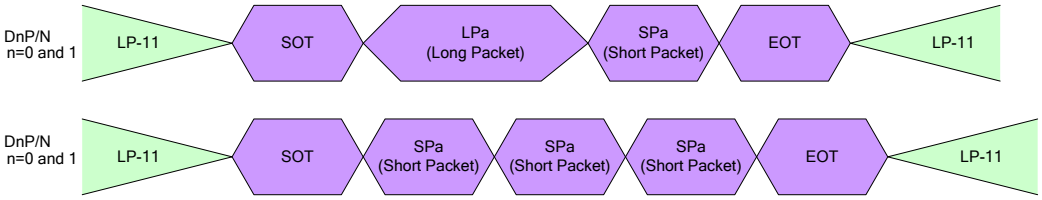


Figure 21: Multiple Packets in High-Speed Data Transmission – Examples

Table 6: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet in High-Speed Data Transmission (HSDT) are as follows.

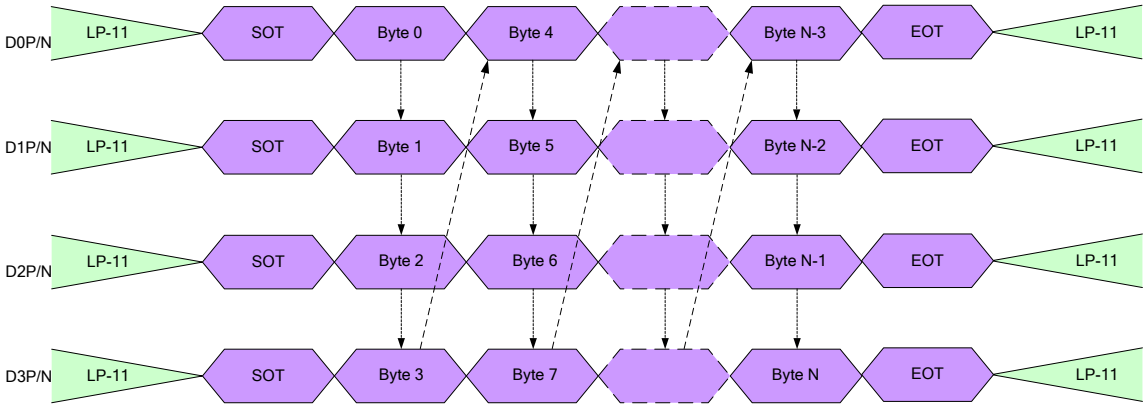


Figure 22: Number of Bytes, N, transmitted is an integer multiple of the number of lanes

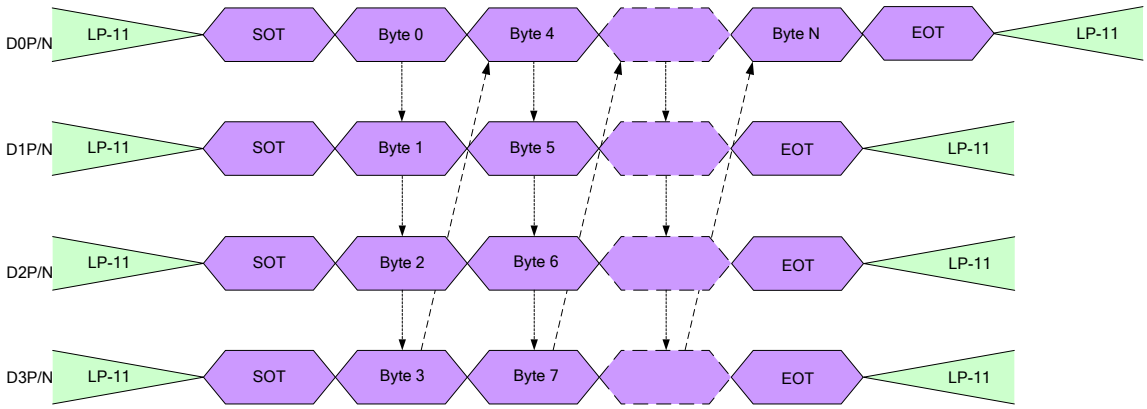


Figure 23: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1)

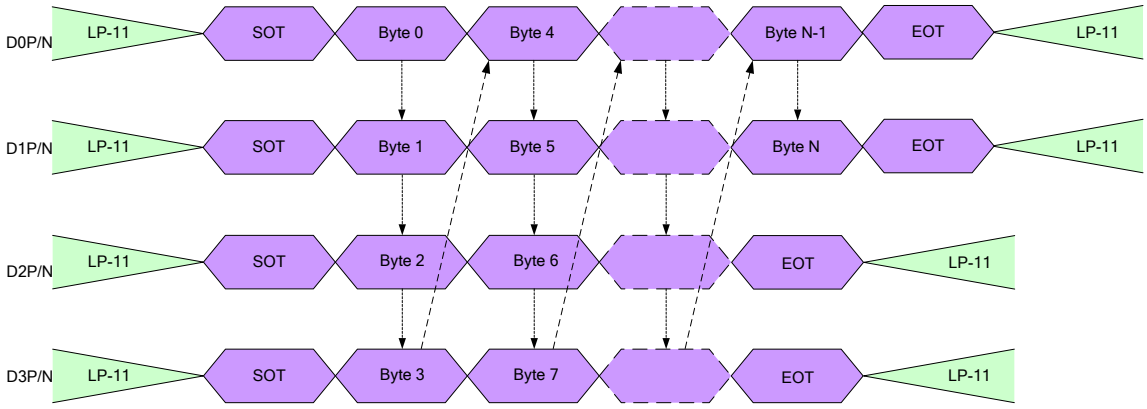


Figure 24: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2)

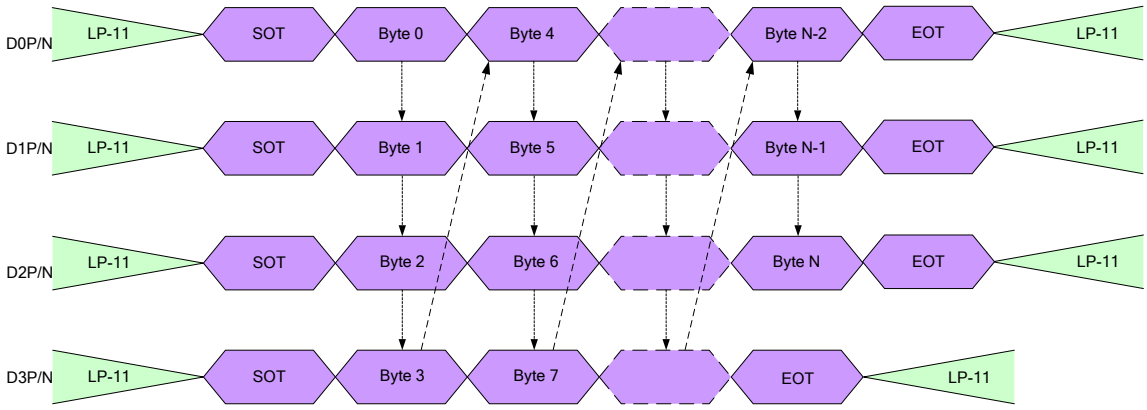


Figure 25: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 3)

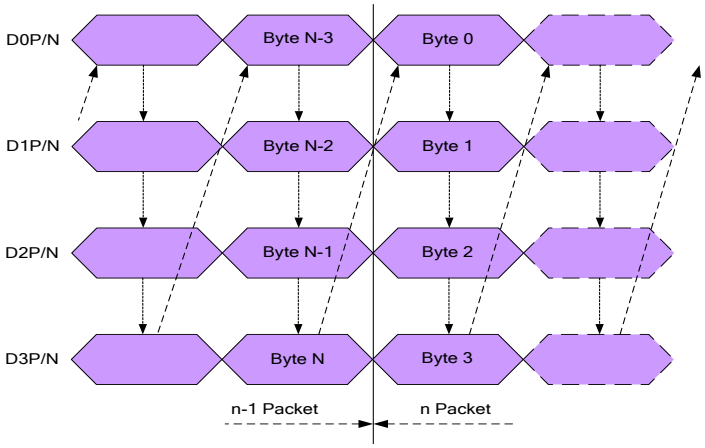


Figure 26: Continuous Multiple Packets in HSDT when Number of Bytes is Equal on Data Lanes at the End of the Packet

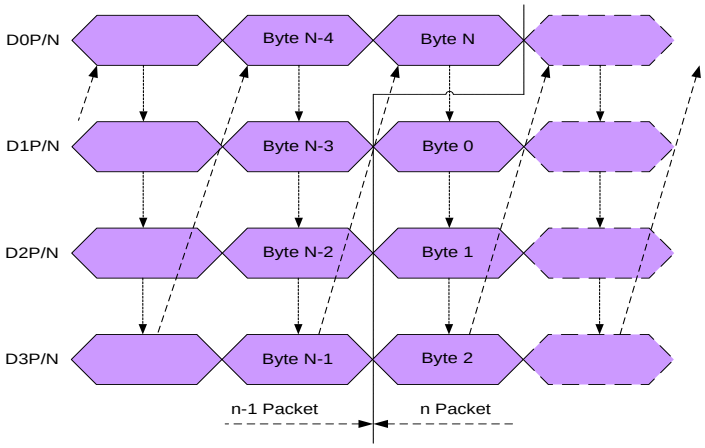


Figure 27: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 1)

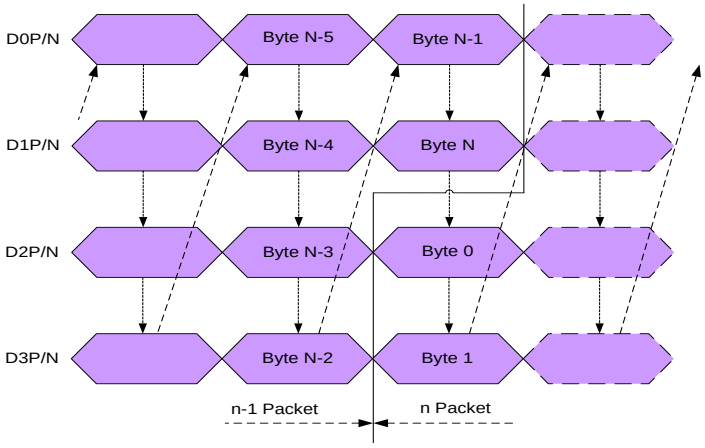


Figure 28: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 2)

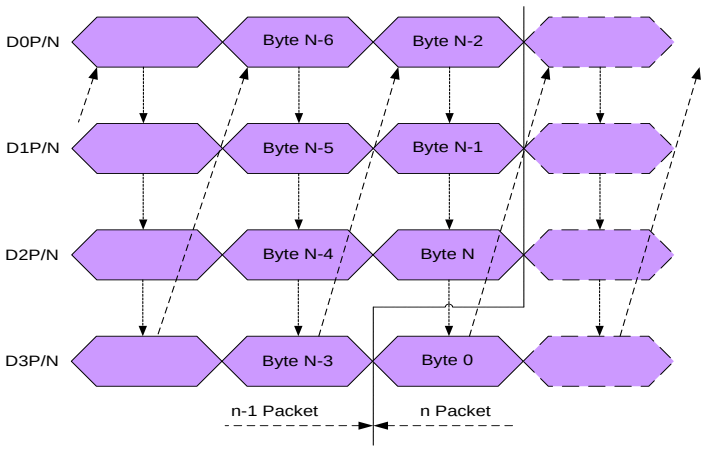


Figure 29: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 3)

4.1.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module.

The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

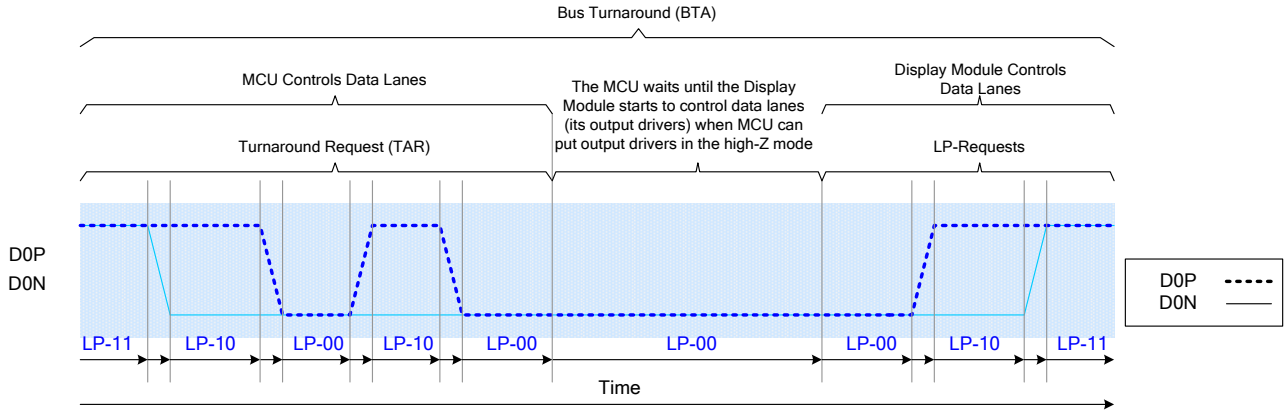


Figure 30: Bus Turnaround Procedure

MCU and display module terms can be switched in Figure 30 if the Bus Turnaround (BTA) is from the display module to the MCU.

4.1.3. Packet Level Communication

4.1.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

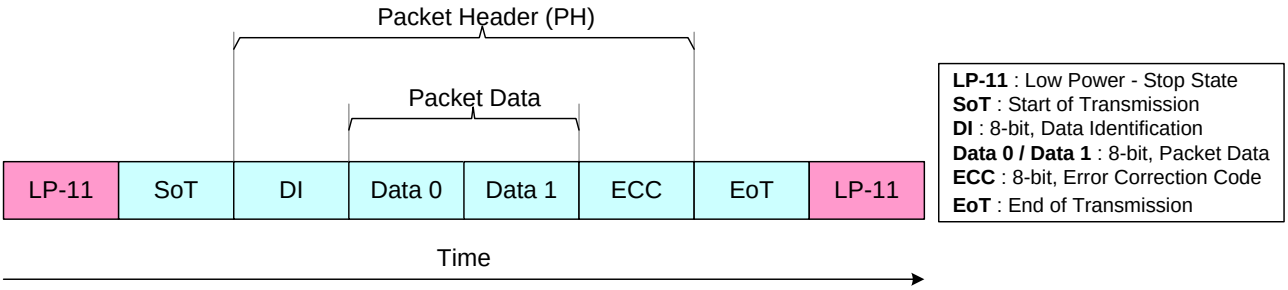


Figure 31: Short Packet (SPa) Structure

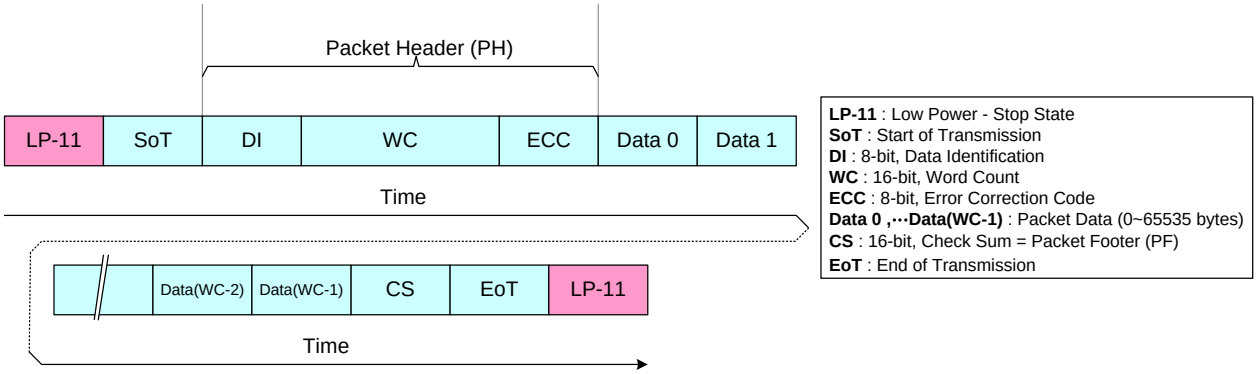


Figure 32: Long Packet (LPa) Structure

Notes:

1. *Figure 31 and Figure 32 present a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).*
2. *The other possibility is that SoT, EoT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g.*
   - *LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11*
   - *LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11*
   - *LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11*

4.1.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

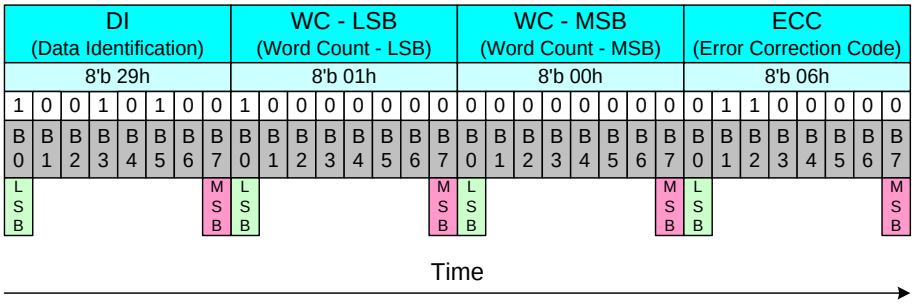


Figure 33: Bit Order of the Byte on Packets

4.1.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

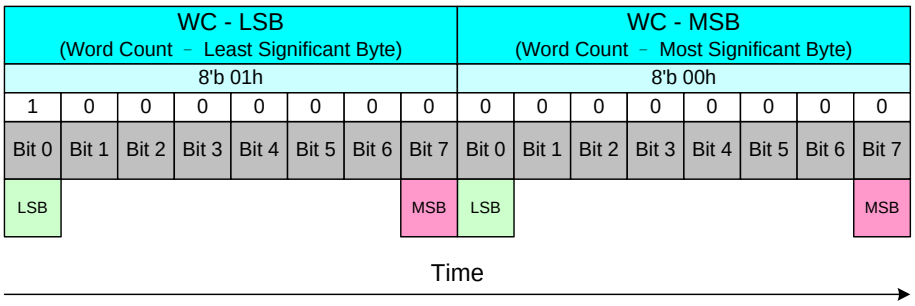


Figure 34: Byte Order of the Multiple Byte Information on Packets

4.1.3.1.3. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

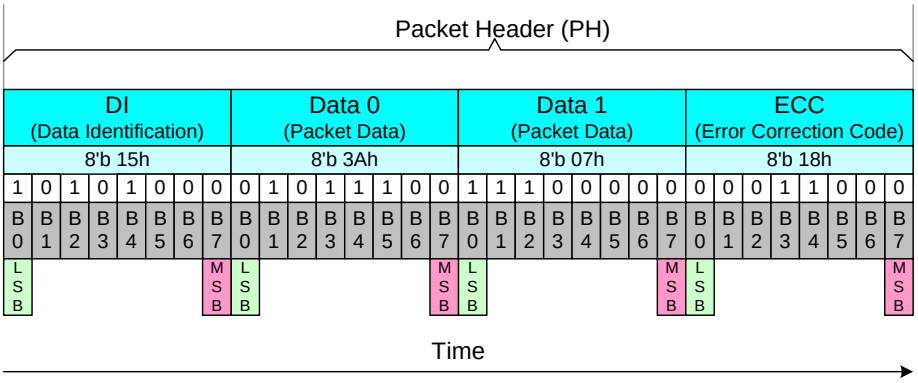


Figure 35: Packet Header (PH) in a Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

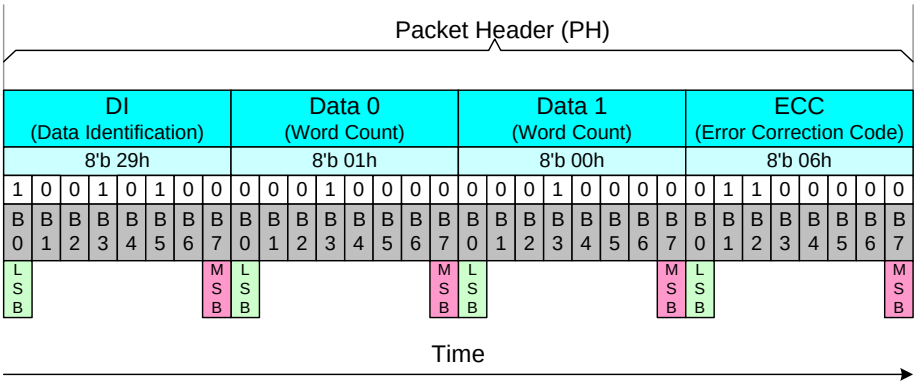


Figure 36: Packet Header (PH) in a Long Packet (LPa)

4.1.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated, see the figure below.

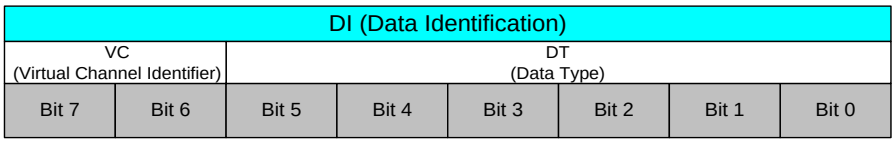


Figure 37: Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

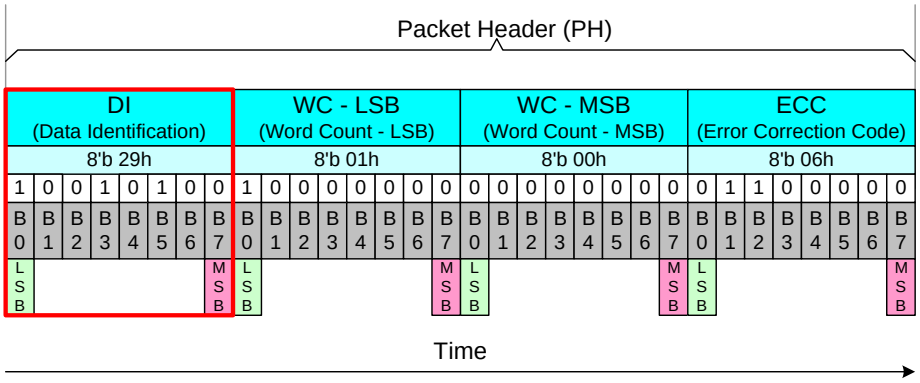


Figure 38: Data Identification (DI) on the Packet Header (PH)

4.1.3.1.3.1.1. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7…6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

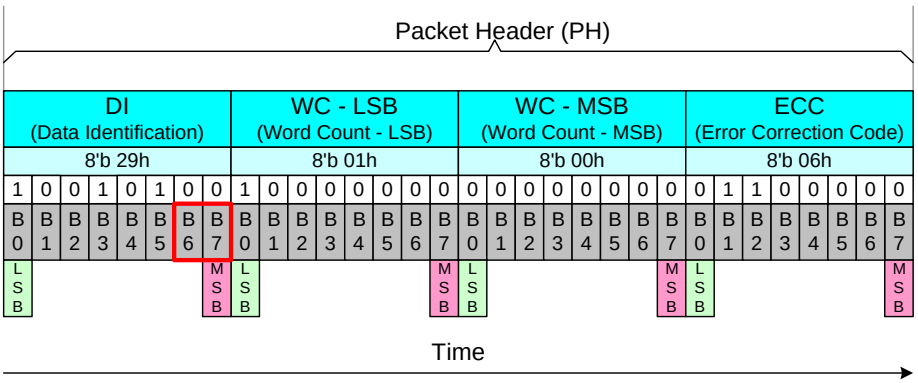


Figure 39: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

- The MCU uses the virtual channel 0 when it sends packets to the ILI9881C-05
- The ILI9881C-05 also uses the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

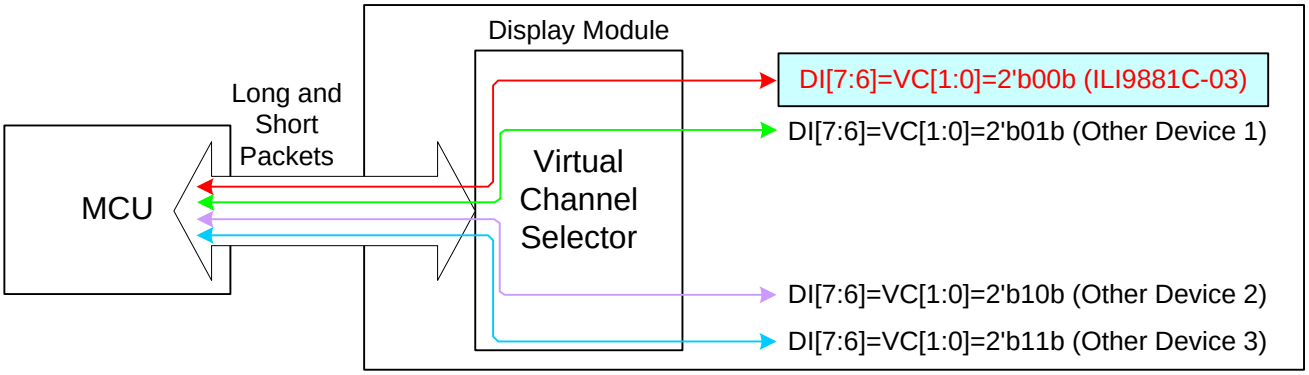


Figure 40: Virtual Channel (VC) Configuration

Virtual Channel (VC) is always 0 (DI [7..6] = VC [1..0] = 00b) when the MCU sends “End of Transmission Packet” to the display module. See the section “4.1.3.2.1.7 End of Transmission Packet (EoTP)”.

This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1..0]) is 00b for the ILI9881C-05.

4.1.3.1.3.1.2. Data Type (DT)

Data Type (DT) is a part of Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

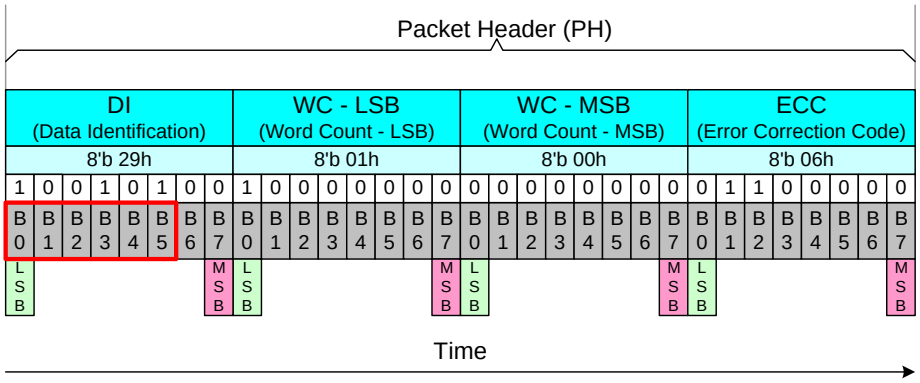


Figure 41: Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

Table 7: Data Type (DT) from the MCU to the Display Module

From the MCU to the Display Module								
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**
0	0	0	0	0	1	01	Sync Event, V Sync Start	SPa (Short Packet)
0	1	0	0	0	1	11	Sync Event, V Sync End	SPa (Short Packet)
1	0	0	0	0	1	21	Sync Event, H Sync Start	SPa (Short Packet)
1	1	0	0	0	1	31	Sync Event, H Sync End	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP) Note1	SPa (Short Packet)
0	0	0	0	1	0	02	Color Mode Off Command	SPa (Short Packet)
0	1	0	0	1	0	12	Color Mode On Command	SPa (Short Packet)
1	0	0	0	1	0	22	Shut Down Peripheral Command	SPa (Short Packet)
1	1	0	0	1	0	32	Turn On Peripheral Command	SPa (Short Packet)
0	0	0	0	1	1	03	Generic Short WRITE, no parameters	SPa (Short Packet)
0	1	0	0	1	1	13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
1	0	0	0	1	1	23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
0	0	0	1	0	0	04	Generic Short READ, no parameters	SPa (Short Packet)
0	1	0	1	0	0	14	Generic Short READ, 1 parameters	SPa (Short Packet)
1	0	0	1	0	0	24	Generic Short READ, 2 parameters	SPa (Short Packet)
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)
0	0	1	0	0	1	09	Null Packet, No Data, Note2	LPa (Long Packet)
0	1	1	0	0	1	19	Blanking Packet, no data	LPa (Long Packet)
1	0	1	0	0	1	29	Generic Long Write	LPa (Long Packet)
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)
0	0	1	1	1	0	0E	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	LPa (Long Packet)
0	1	1	1	1	0	1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	0	1	1	1	0	2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	1	1	1	1	0	3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
x	x	0	0	0	0	x0	DO NOT USE	
x	x	1	1	1	1	xF	All unspecified codes are reserved	

Notes:

1. *This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.*
2. *This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.*

Table 8: Data Type (DT) from the Display Module to the MCU

From the Display Module to the MCU								
Bit5	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Hex**	**Description**	**Short/Long Packet**
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP)	SPa (Short Packet)
0	1	0	0	0	1	11	Generic Short READ Response, 1 byte returned	SPa (Short Packet)
0	1	0	0	1	0	12	Generic Short READ Response, 2 byte returned	SPa (Short Packet)
0	1	1	0	1	0	1A	Generic Long READ Response	LPa (Long Packet)
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)

The receiver will ignore other Data Types (DT) if they are not defined in Table 7 and Table 8.

4.1.3.1.3.2. Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

Packet Data (PD) information:

• Data 0: 26hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)

• Data 1: 01hex (DCS's parameter)

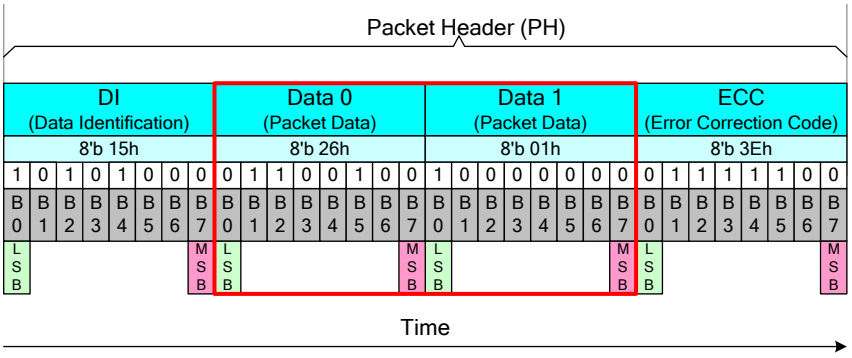


Figure 42: Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

• Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)

• Data 1: 00hex (Null)

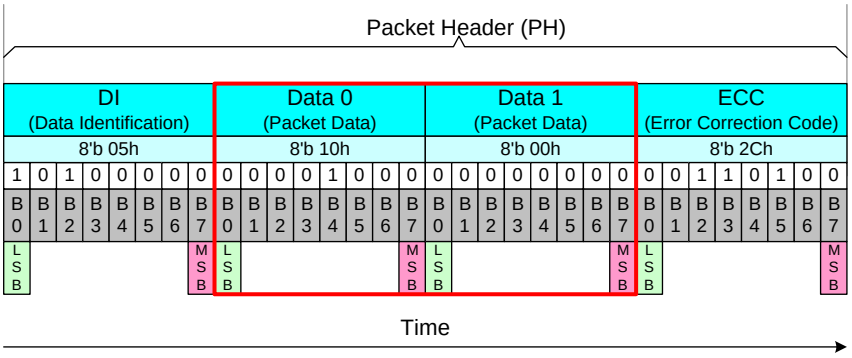


Figure 43: Packet Data (PD) for Short Packet (SPa), 1 Byte Information

4.1.3.1.3.3. Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 45. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

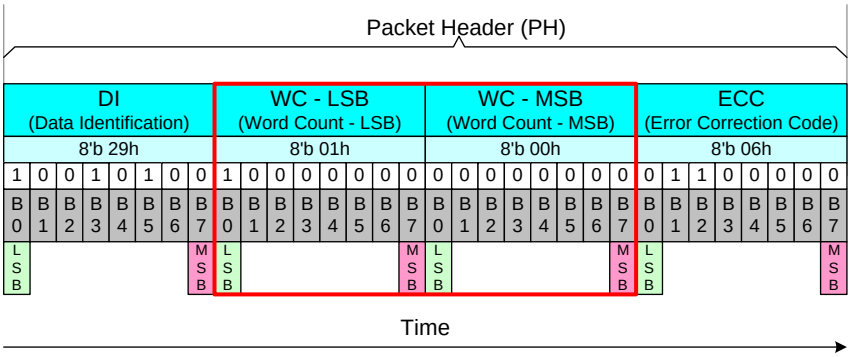


Figure 44: Word Count (WC) in a Long Packet (LPa)

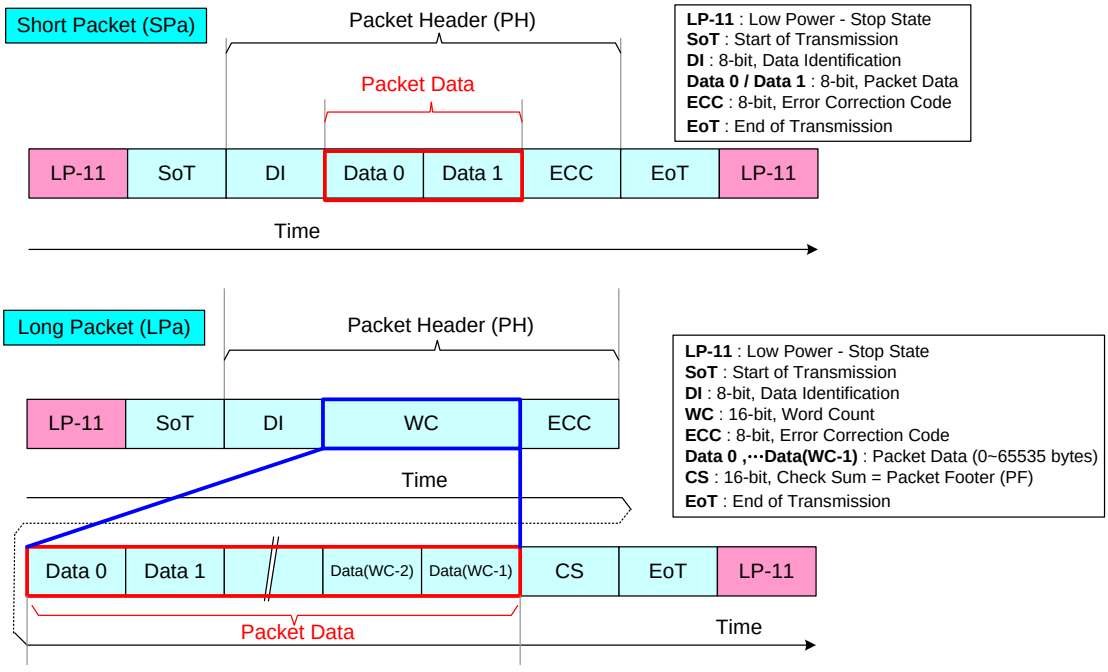


Figure 45: Packet Data in Short and Long Packets

4.1.3.1.3.4. Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])

D [23…0] and P [7…0] are illustrated for reference purposes below.

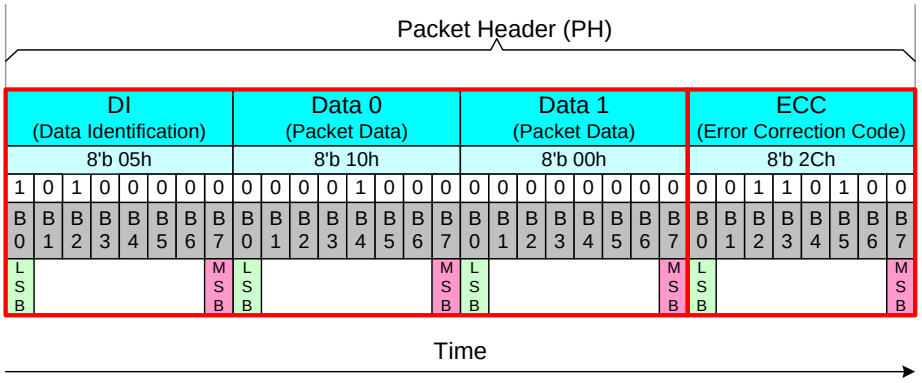


Figure 46: D [23…0] and P [7…0] in a Short Packet (SPa)

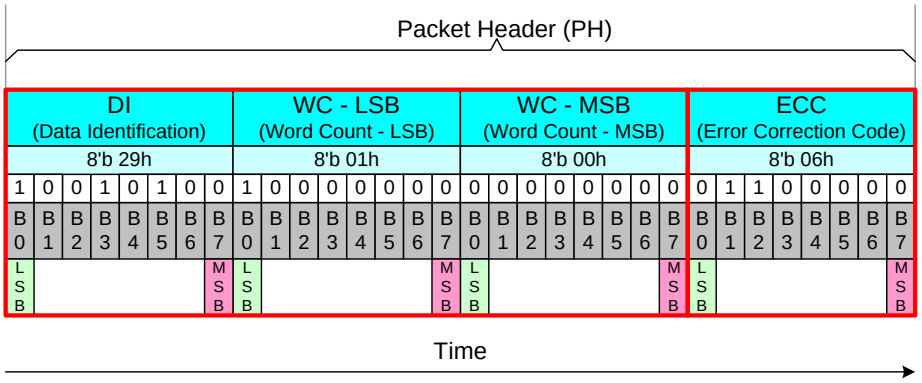


Figure 47: D [23…0] and P [7…0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits are needed (P [5…0]) for Error Correction Code (ECC).

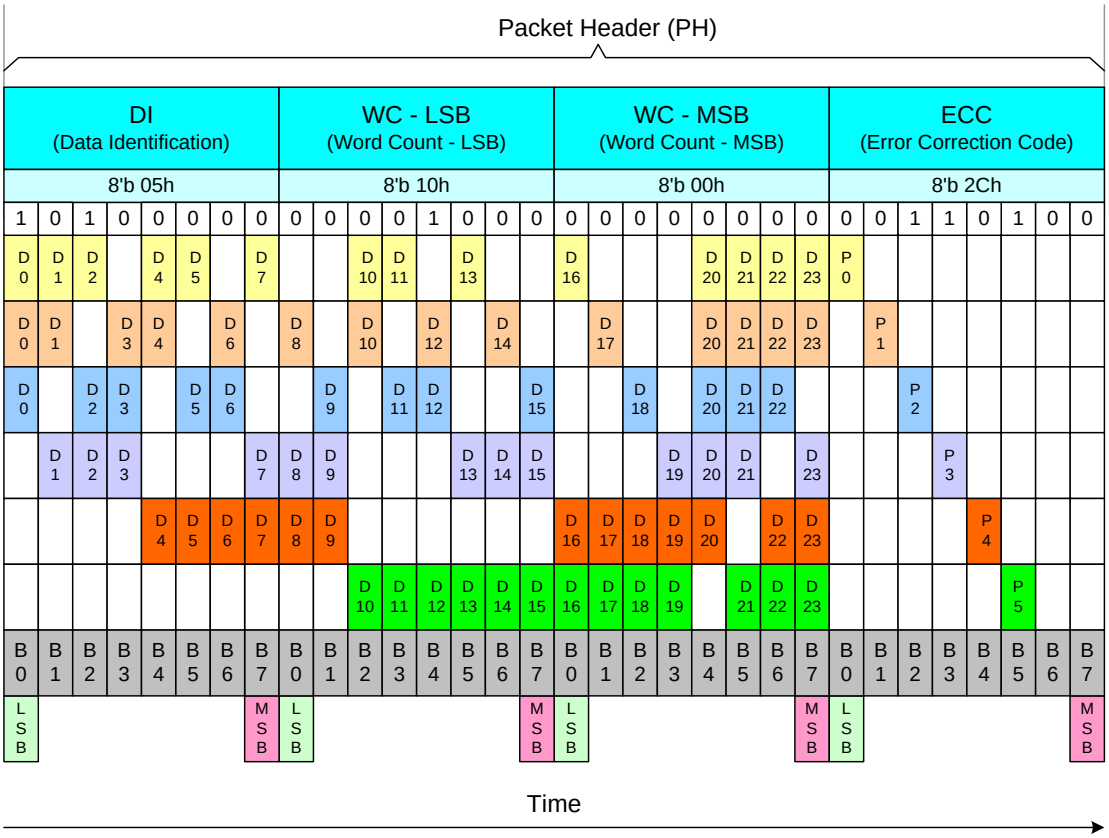


Figure 48: XOR Function on a Short Packet (SPa)

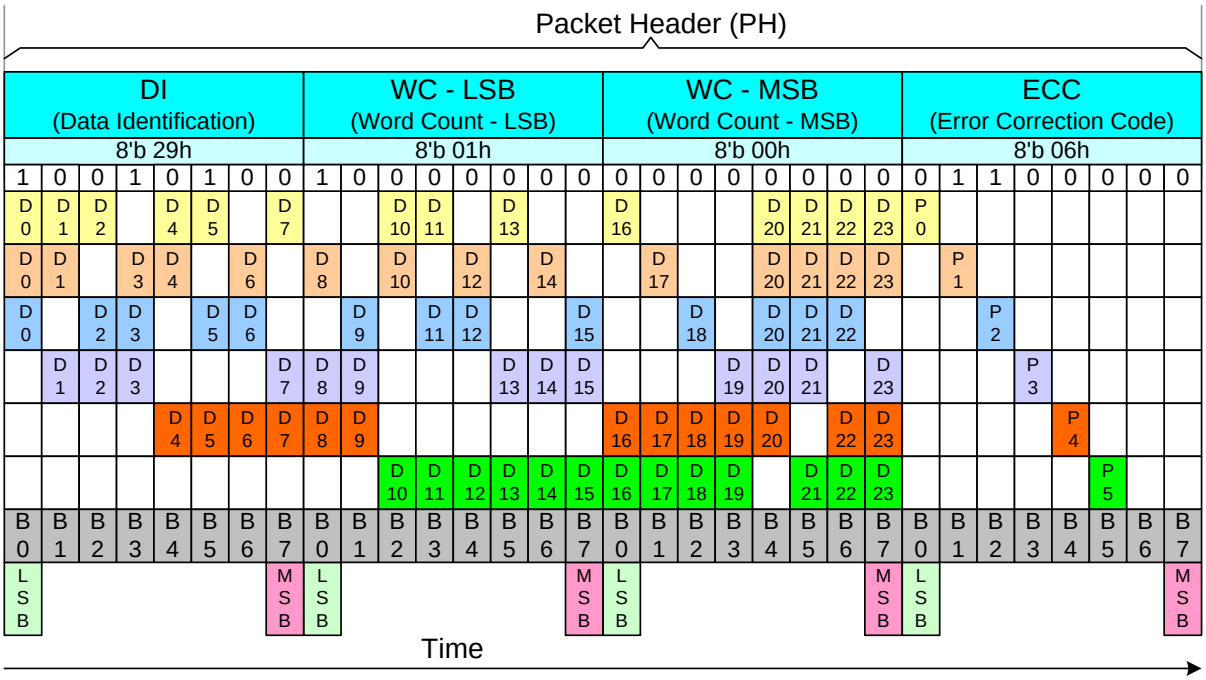


Figure 49: XOR Function on a Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D [23…0] and Error Correction Code (ECC) P [7…0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7…0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

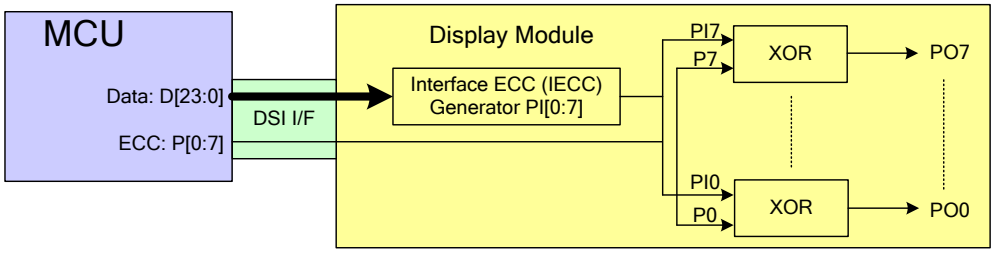


Figure 50: Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D [23…0]) and ECC (P [7…0]) are correctly received if the value of the PO [7…0]) is 00h.

The sent data bits (D [23…0]) and ECC (P [7…0]) are not correctly received if the value of the PO [7…0]) is not 00h.

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7…0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 51: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7…0]	1	1	0	0	0	0	0	0	03h
IECC PI[7…0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7…0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 52: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

Table 9: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7…0] is in Table 9, and the receiver can correct this one bit error

because this found value also defines the location of the corrupt bit, e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), that is not correct, is D [3]

More than one error is detected if the value of the PO [7…0] is not in Table 9,for example, PO [7…0] = 0Ch.

4.1.3.1.4. Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “4.1.3.1.3.3 Word Count (WC) in a Long Packet (LPa)”.

4.1.3.1.5. Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.

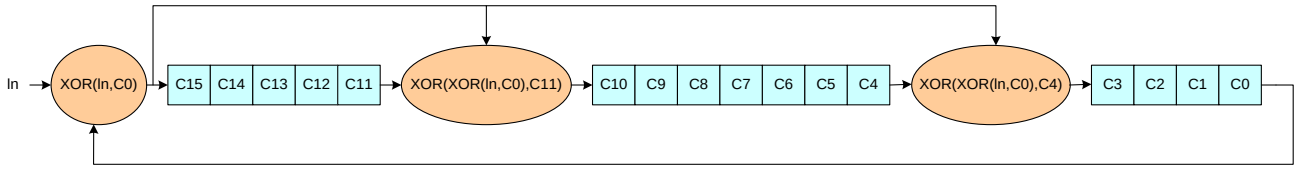
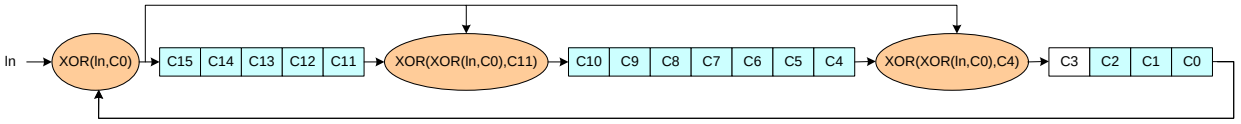


Figure 53: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11(Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4(Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1 byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 54: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated

below.

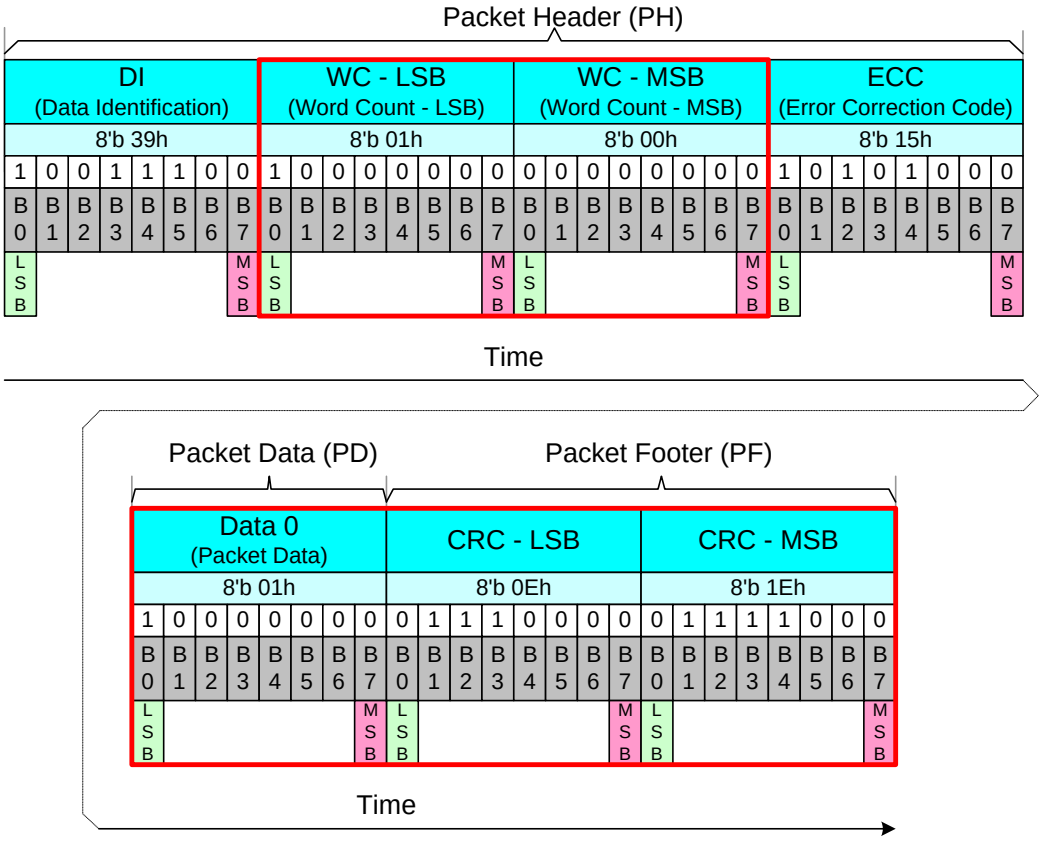


Figure 55: Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

4.1.3.2. Packet Transmissions

4.1.3.2.1. Packet from the MCU to the Display Module

4.1.3.2.1.1. Display Command Set (DCS)

Display Command Set (DCS), defined in the section “5.3Page 0 Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

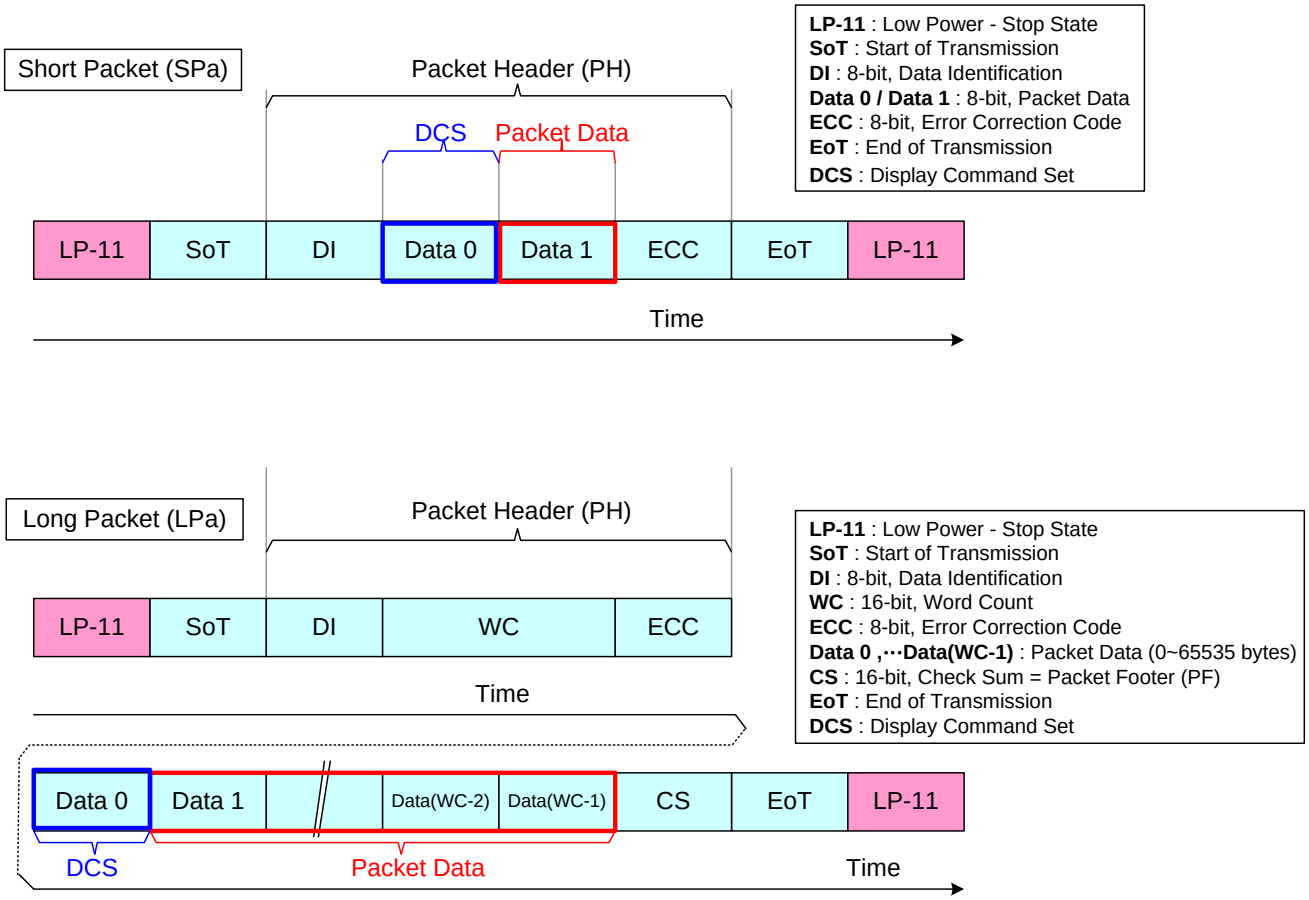


Figure 56: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

4.1.3.2.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

"Display Command Set (DCS) Write, No Parameter", which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Table 10: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)
Stop Transition (59h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0101b
- Packet Data (PD)
  - ✧ Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

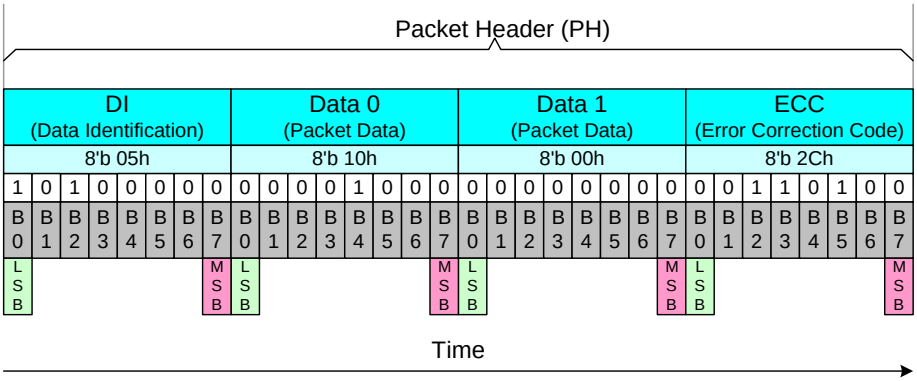


Figure 57: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

4.1.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 11: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Curve Set (26h)
Tearing Effect Line ON(35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Power Save (55h)

Note: One Subpixel has been written

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 01 0101b
- Packet Data (PD)
  - ✧ Data 0: "Gamma Set (26h)", Display Command Set (DCS)
  - ✧ Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

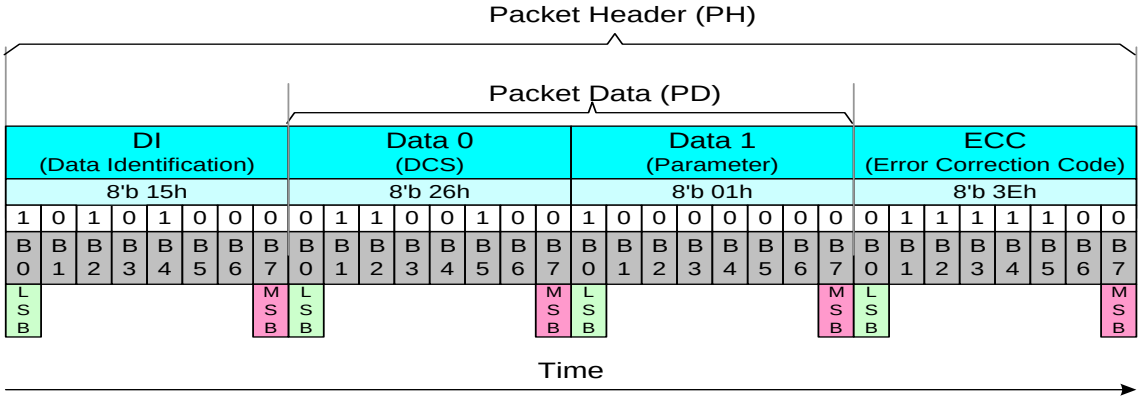


Figure 58: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

4.1.3.2.1.4. Display Command Set (DCS) Write Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Table 12: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), Note 1
Software Reset (01h), Note 1
Sleep In(10h), Note 1
Sleep Out (11h), Note 1
Normal Display Mode On (13h), Note 1
All Pixel Off (22h) , Note 1
All Pixel On (23h) , Note 1
Gamma Curve Set (26h), Note 2
Display Off (28h), Note 1
Display ON (29h), Note 1
Tearing Effect Line OFF (34h), Note 1
Tearing Effect Line ON (35h), Note 2
Memory Access Control (36h), Note 2
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
Interface Pixel Format (3Ah), Note 2
Set Tear Scan Line(44h),
Write Display Brightness (51h), Note 2
Write CTRL Display (53h), Note 2
Write Power Save(55h), Note 2
Stop Transition (59h), Note 1
Write CABC Minimum Brightness (5Eh) , Note 2
Set Transition Time(68h)

Notes:

1. Short Packet (SPa) can also be used; See the section "4.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)".

2. Short Packet (SPa) can also be used; See the section "4.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)".

A Long Packet (LPa) with one command (No Parameter) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

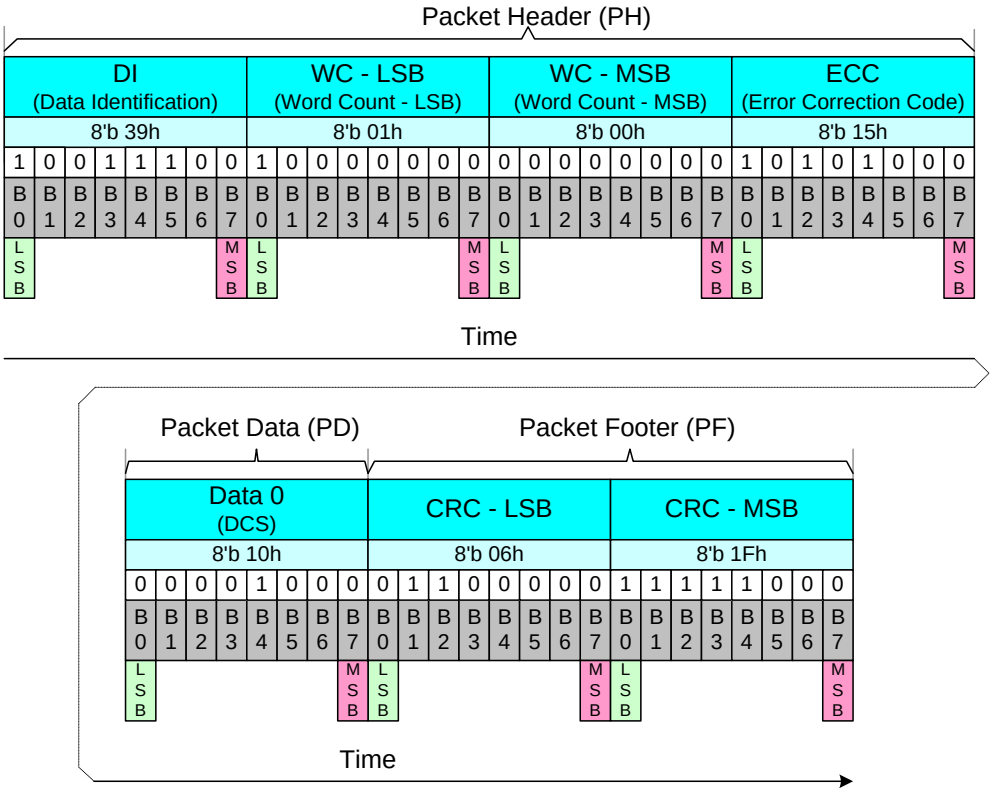


Figure 59: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
  - ✧ Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

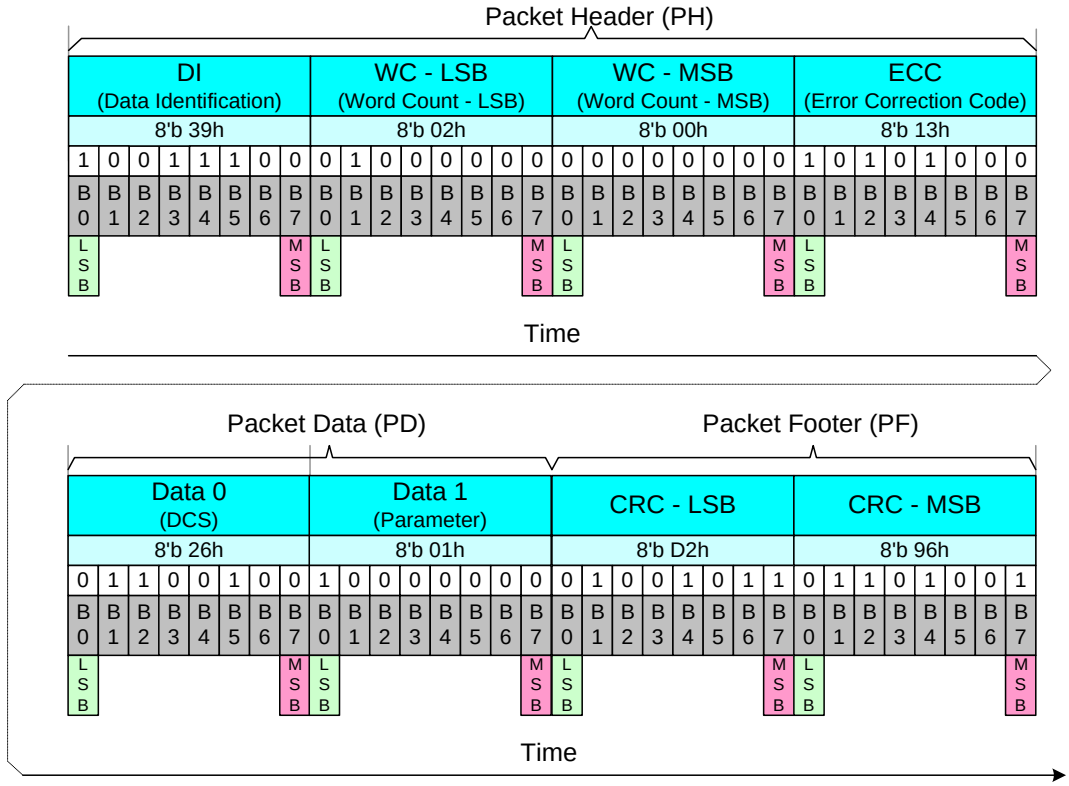


Figure 60: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: “Column Address Set (2Ah)” (For example only), Display Command Set (DCS)
  - ✧ Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - ✧ Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - ✧ Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - ✧ Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

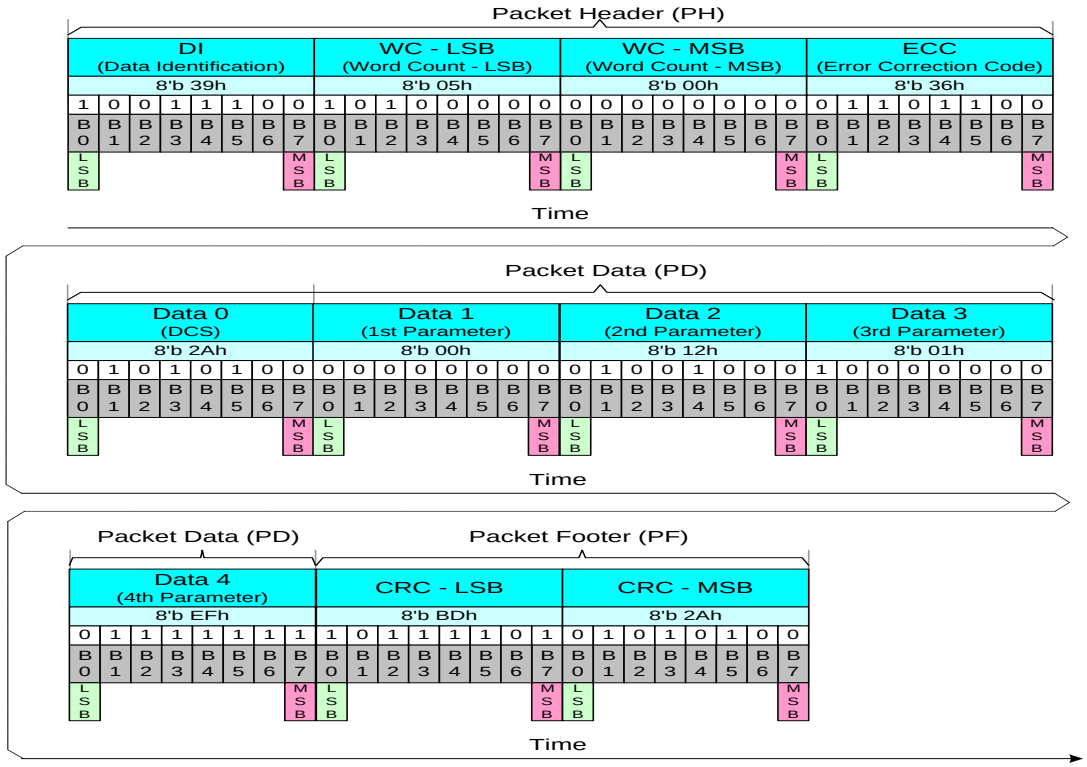


Figure 61: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

4.1.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 13: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Get Tear Scan Line(45h)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Power Save (56h)
Read CABC Minimum Brightness (5Fh)
Get Transition Time(69h)
Read DDB Start (A1h)
Read DDB Continue (A8h)
Read First Checksum(AAh)
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This sequence is illustrated for reference purposes below.

Step 1:

The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 11 0111b
- Maximum Return Packet Size (MRPS)
  - ✧ Data 0: 01hex
  - ✧ Data 1: 00hex
- Error Correction Code (ECC)

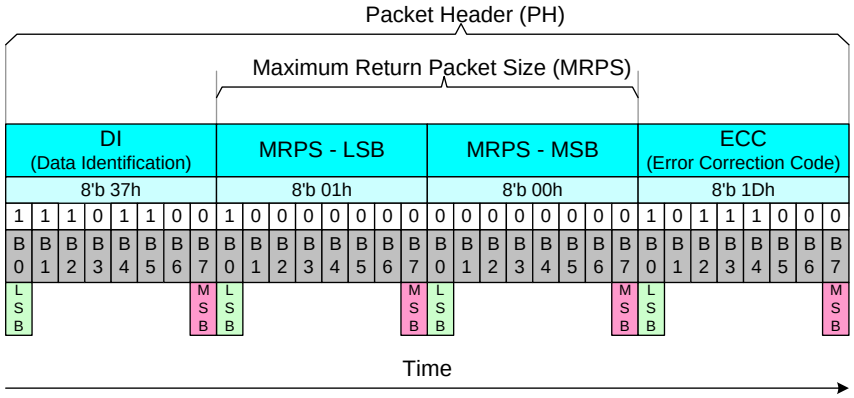


Figure 62: Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MCU wants to receive the value of the "Read ID1 (DAh)" from the display module when the MCU sends "Display Command Set (DCS) Read, No Parameter" to the display module.

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0110b
- Packet Data (PD)
  - ✧ Data 0: "Read ID1 (DAh)", Display Command Set (DCS)
  - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

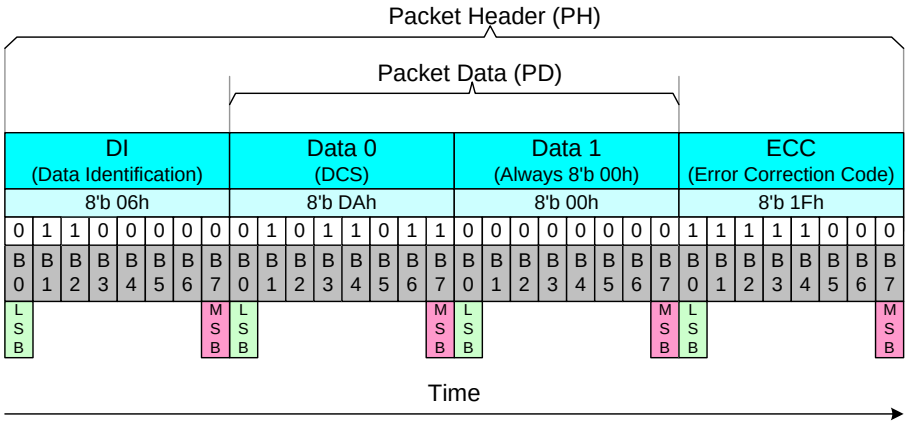


Figure 63: Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section "4.1.3.2.2.2 Acknowledge with Error Report (AwER)".

2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

4.1.3.2.1.6. Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: 89hex (Random data)
  - ✧ Data 1: 23hex (Random data)
  - ✧ Data 2: 12hex (Random data)
  - ✧ Data 3: A2hex (Random data)
  - ✧ Data 4: E2hex (Random data)
- Packet Footer (PF)

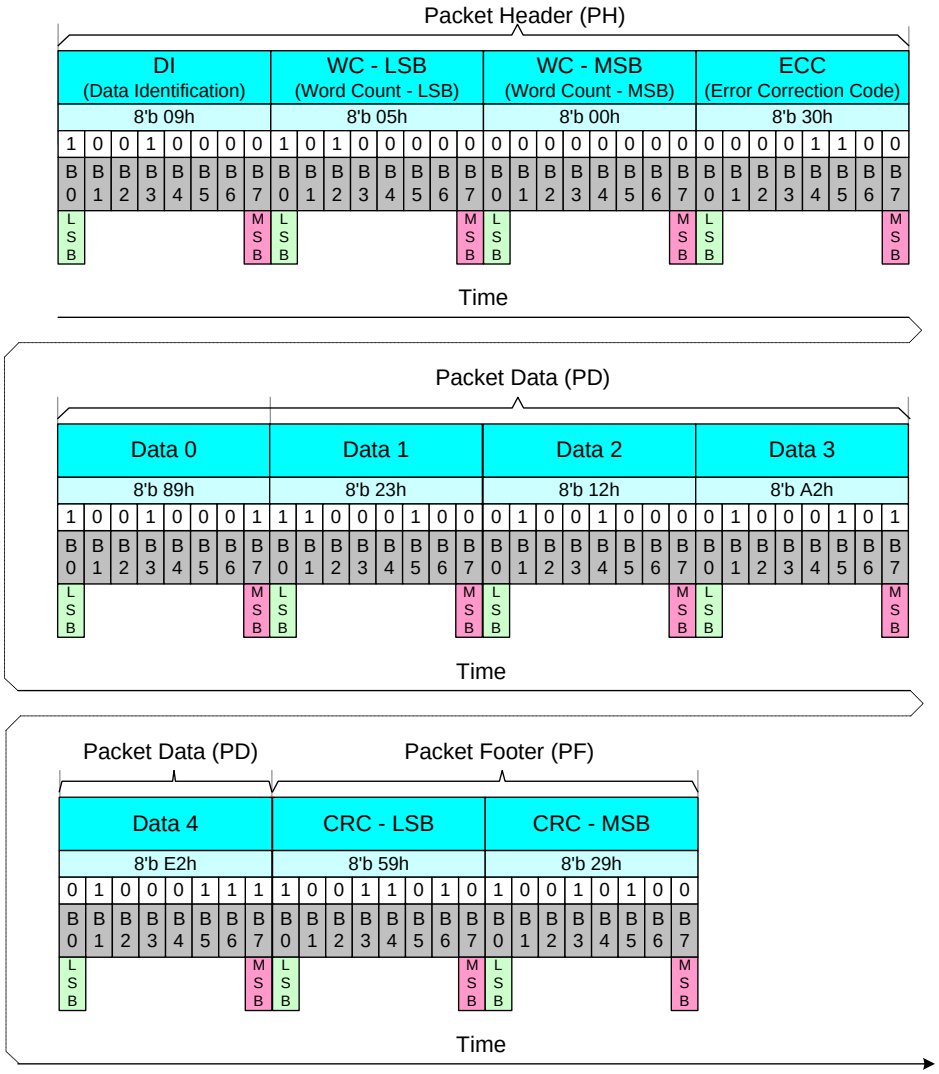


Figure 64: Null Packet, No Data (NP-L) - Example

4.1.3.2.1.7. End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before "End of Transmission" (EoT).

The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module does or does not receive "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 14: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	Support With and Without EoTP	Support With and Without EoTP
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - ✧ Data 0: 0Fhex
  - ✧ Data 1: 0Fhex
- Error Correction Code (ECC)
  - ✧ ECC: 01hex

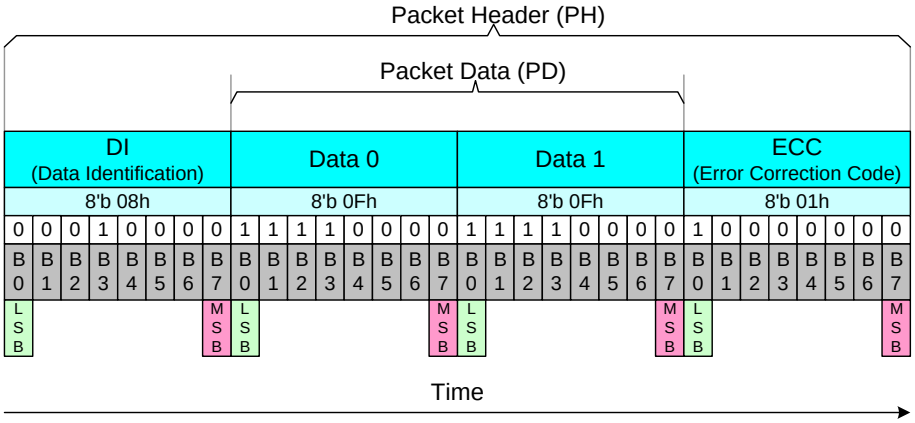


Figure 65: End of Transmission Packet (EoTP)

Some examples of the “End of Transmission Packet” (EoTP) are illustrated for reference purposes below.

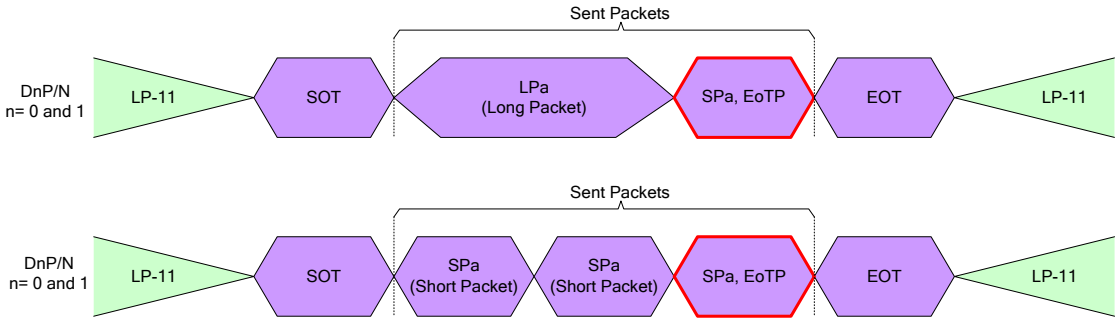


Figure 66: End of Transmission Packet (EoTP)-Examples

4.1.3.2.2. Packet from the Display Module to the MCU

4.1.3.2.2.1. Used Packet types

The display module always uses Short Packets (SPa) or Longs Packet (LPa) when returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the section "4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)") or an Acknowledge with Error Report (See the section "4.1.3.2.2.2 Acknowledge with Error Report (AwER)").

The used packet type is defined on Data Type (DT). See the section "4.1.3.1.3.1.2 Data Type (DT)". If the maximum size of the Packet Data (PD) could be sent in one packet, the display module should not send returned bytes in several packets. Both cases are illustrated for reference purposes below.

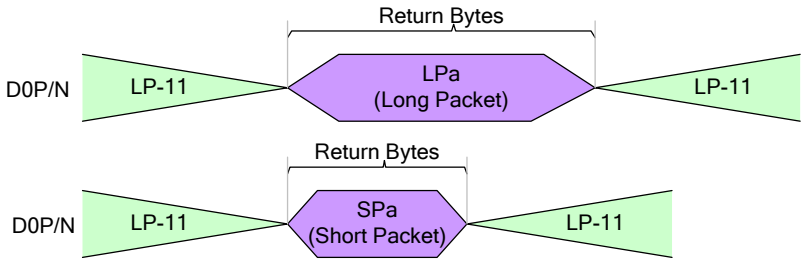


Figure 67: Return Bytes in Single Packet

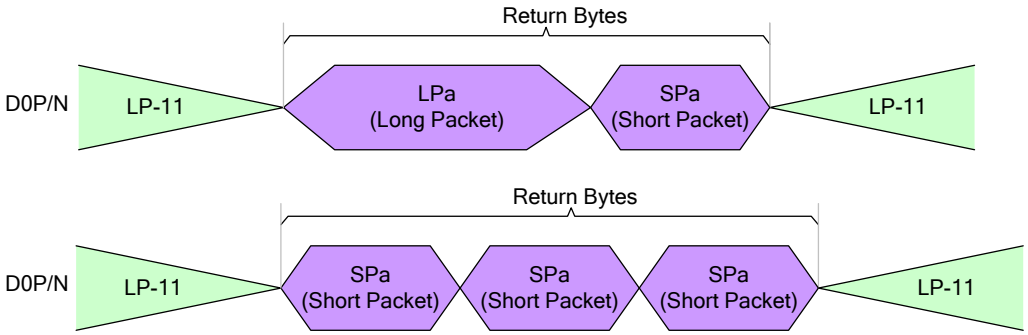


Figure 68: Return Bytes in Several Packets – Not Allowed

EXCEPTION:

The display module will return 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (See section "4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)"), which is detected and corrected a single bit error by the EEC (See bit 8 in Table 15). These returned packets are illustrated for reference purposes below.

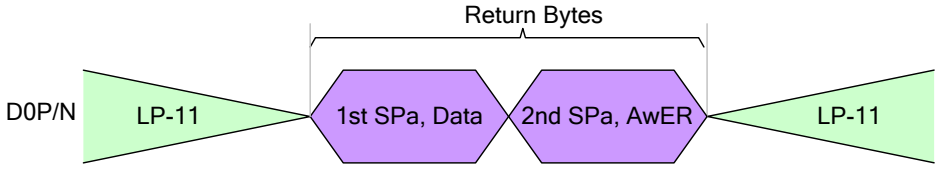


Figure 69: Exception when Returned Bytes in Several Packets

AwER = Acknowledge with Error Report

4.1.3.2.2.2. Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Table 15: Error Report (AwER) Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 00 0010b
- Packet Data (PD)
  - ✧ Bit 8: ECC Error, single-bit (detected and corrected)
  - ✧ AwER: 0100h
- Error Correction Code (ECC)

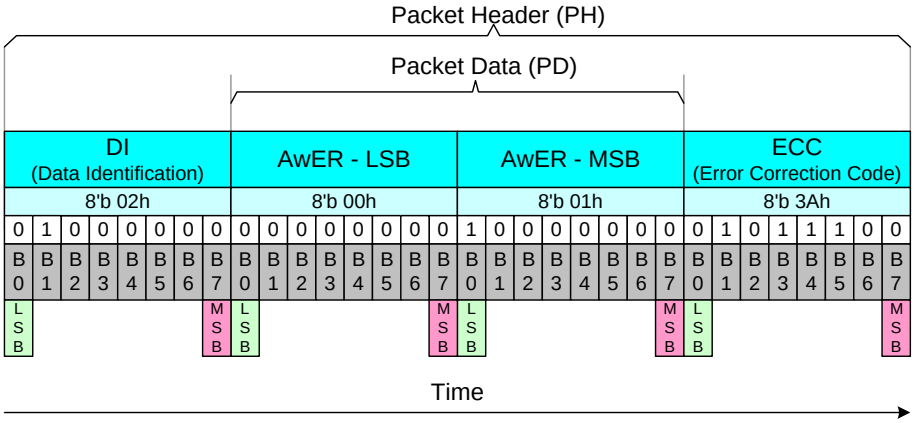


Figure 70: Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

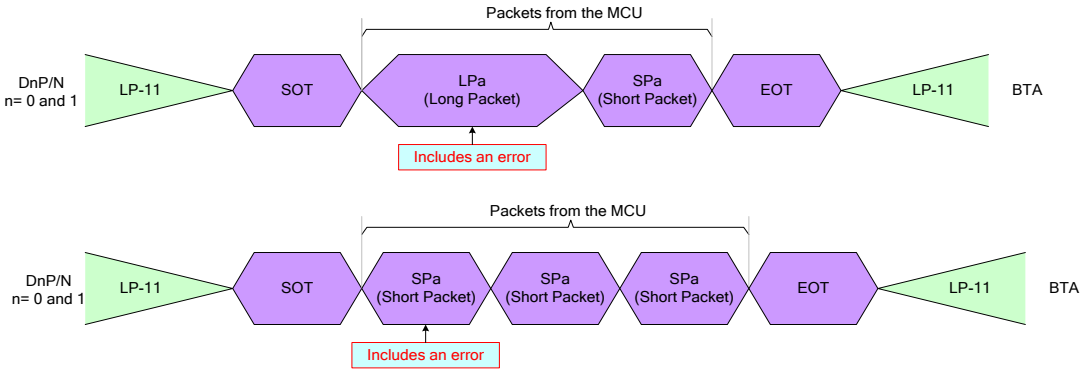


Figure 71: Errors Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands. The bit D0 of the “Read Display Signal Mode (0Eh)” command will be set to 1 if a received packet includes an error.

The amount of packets, which include an ***ECC*** *or* ***CRC*** error, is calculated in the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h and set the bit D0 of the “Read Display Signal Mode (0Eh)” command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.

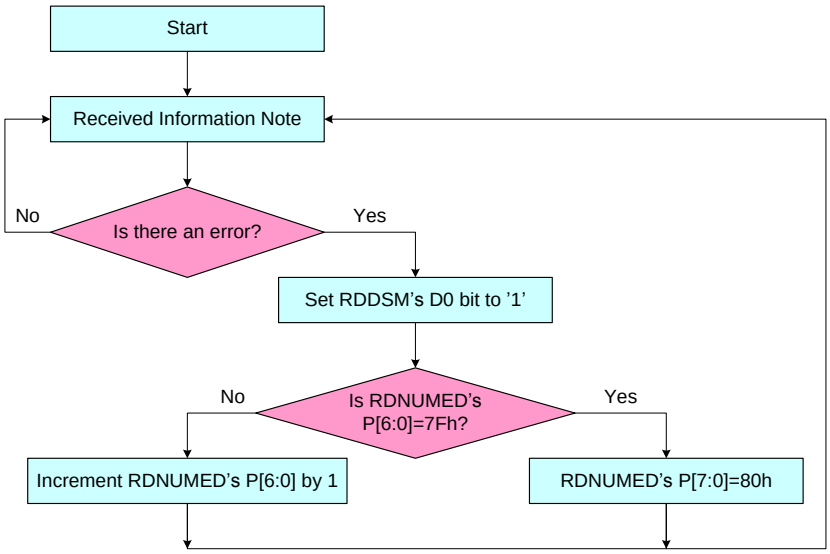


Figure 72: Flow Chart for Errors on DSI

Notes:

1. *This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.*
2. *CRC or ECC error*

4.1.3.2.2.3. DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
  - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - ✧ Data 0: 89hex
  - ✧ Data 1: 23hex
  - ✧ Data 2: 12hex
  - ✧ Data 3: A2hex
  - ✧ Data 4: E2hex
- Packet Footer (PF)

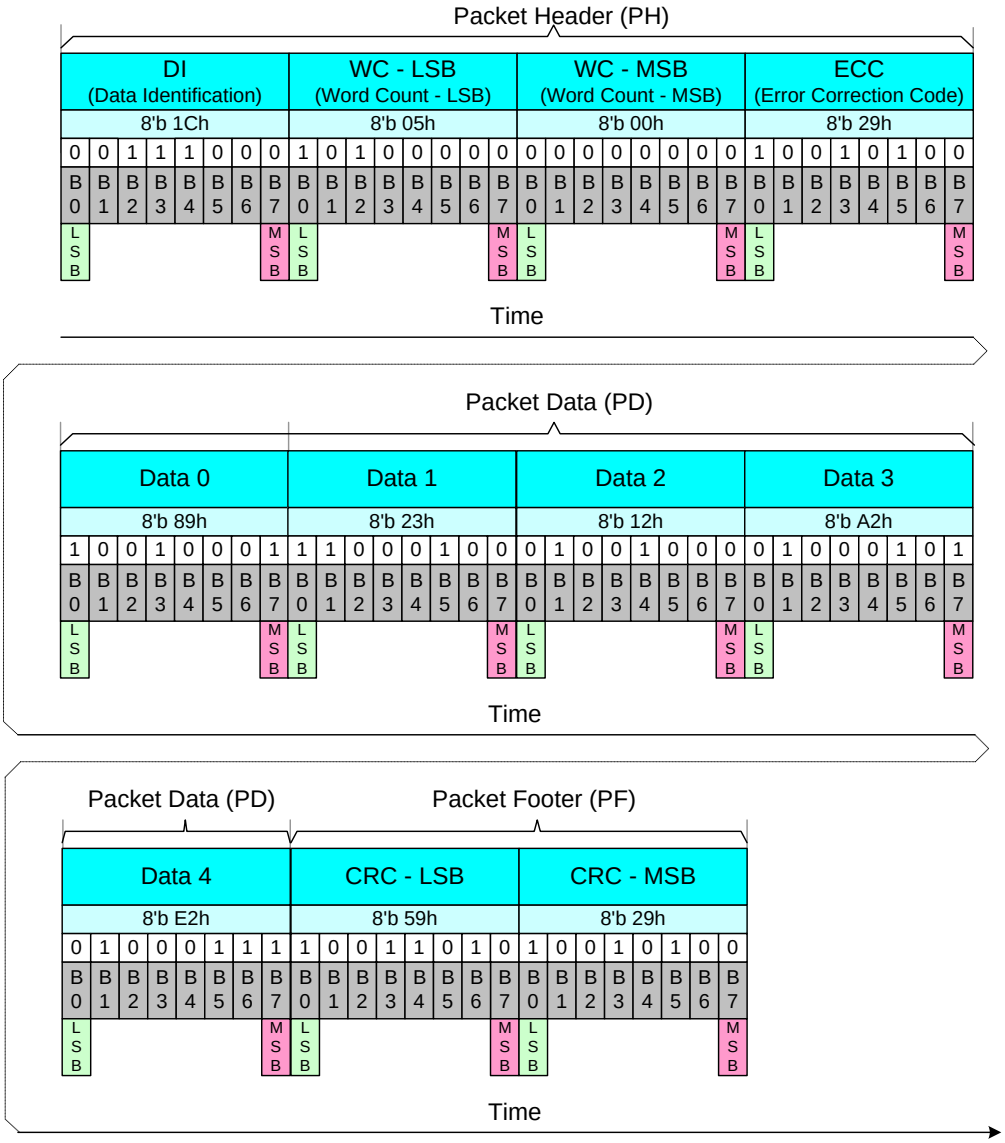


Figure 73: DCS Read Long Response (DCSRR-L) - Example

4.1.3.2.2.4. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
  - ✧ Data 0: 45hex
  - ✧ Data 1: 00hex (Always)
- Error Correction Code (ECC)

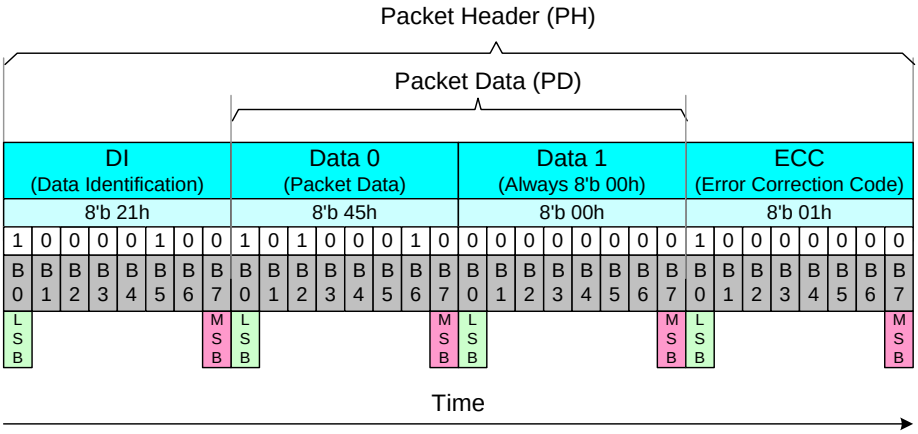


Figure 74: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

4.1.3.2.2.5. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - ✧ Virtual Channel (VC, DI [7…6]): 00b
  - ✧ Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
  - ✧ Data 0: 45hex
  - ✧ Data 1: 32hex
- Error Correction Code (ECC)

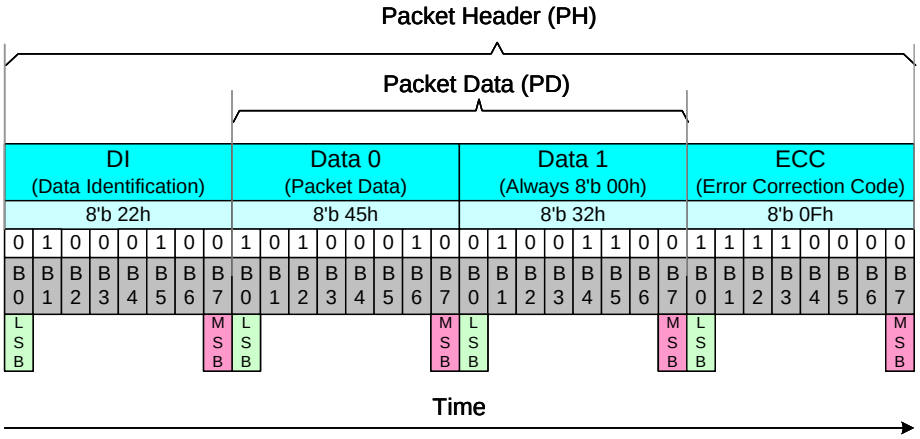


Figure 75: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

4.1.3.3. Communication Sequences

4.1.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “4.1.2 Interface Level Communication” and “4.1.3 Packet Level Communication”. This communication sequence description is for DSI data lanes (D3P/N, D2P/N, D1P/N and D0P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “4.1.2.2 DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Table 16: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 17: Packet Level Communication for MCU-sourced Packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	VSS	Short Packet	Sync Event, V Sync Start
	VSE	Short Packet	Sync Event, V Sync End
	HSS	Short Packet	Sync Event, H Sync Start
	HSE	Short Packet	Sync Event, H Sync End
	EoTP	Short Packet	End of Transmission Packet (EoTP) Note1
	CMOFF	Short Packet	Color Mode Off Command
	CMON	Short Packet	Color Mode On Command
	SDNP	Short Packet	Shut Down Peripheral Command
	TONP	Short Packet	Turn On Peripheral Command
	GENWN-S	Short Packet	Generic Short WRITE, no parameters
	GENW1-S	Short Packet	Generic Short WRITE, 1 parameters
	GENW2-S	Short Packet	Generic Short WRITE, 2 parameters
	GENRN-S	Short Packet	Generic Short READ, no parameters
	GENR1-S	Short Packet	Generic Short READ, 1 parameters
	GENR2-S	Short Packet	Generic Short READ, 2 parameters
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data, Note2
	BLK-L	Long Packet	Blanking Packet, no data
	GENW-L	Long Packet	Generic Long Write
	DCSW-L	Long Packet	DCS Write Long
	PKPS16	Long Packet	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
	PKPS18	Long Packet	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	LPKPS18	Long Packet	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	PKPS24	Long Packet	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Table 18: Packet Level Communication for Peripheral-sourced packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
Display Module (ILI9881C-04)	AwER	Short Packet	Acknowledge with Error Report
	EoTP	Short Packet	End of Transmission Packet
	GENRR1-S	Short Packet	Generic Short READ Response, 1 byte returned
	GENRR2-S	Short Packet	Generic Short READ Response, 2 byte returned
	GENRR-L	Long Packet	Generic Long READ Response
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response, 1 byte returned
	DCSRR2-S	Short Packet	DCS Read Short Response, 2 byte returned

4.1.3.3.2. Sequences

4.1.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined in the section “4.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences on how this packet is used are described in following tables.

Table 19: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 20: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 21: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.1.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined in the section “4.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences on how this packet is used are described in following tables.

Table 22: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 23: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 24: DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.1.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPa) of "Display Command Set (DCS) Write Long (DCSW-L)" is defined in the section "4.1.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)" and example sequences on how this packet is used are described in following tables.

Table 25: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 26: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 27: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	⇔	BTA	--	
16	--	LP-11	→	--	--	End

4.1.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined in the section “4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences on how this packet is used are described in following tables.

Table 28: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

Table 29: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	⇔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	⇔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

4.1.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined in the section “4.1.3.2.1.6 Null Packet, No Data (NP-L)”, and an example sequence on how this packet is used is described in the following table.

Table 30: Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.1.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined in the section “4.1.3.2.1.7 End of Transmission Packet (EoTP)”, and an example sequence on how this packet is used is described in the following table.

Table 31: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	NP-L	HSDT	→	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

4.2. Display Data Format

4.2.1. DSI Transmission Data Format

4.2.1.1. 16-bit per Pixel, Long Packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the Green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the ILI9881C-05 has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifice.

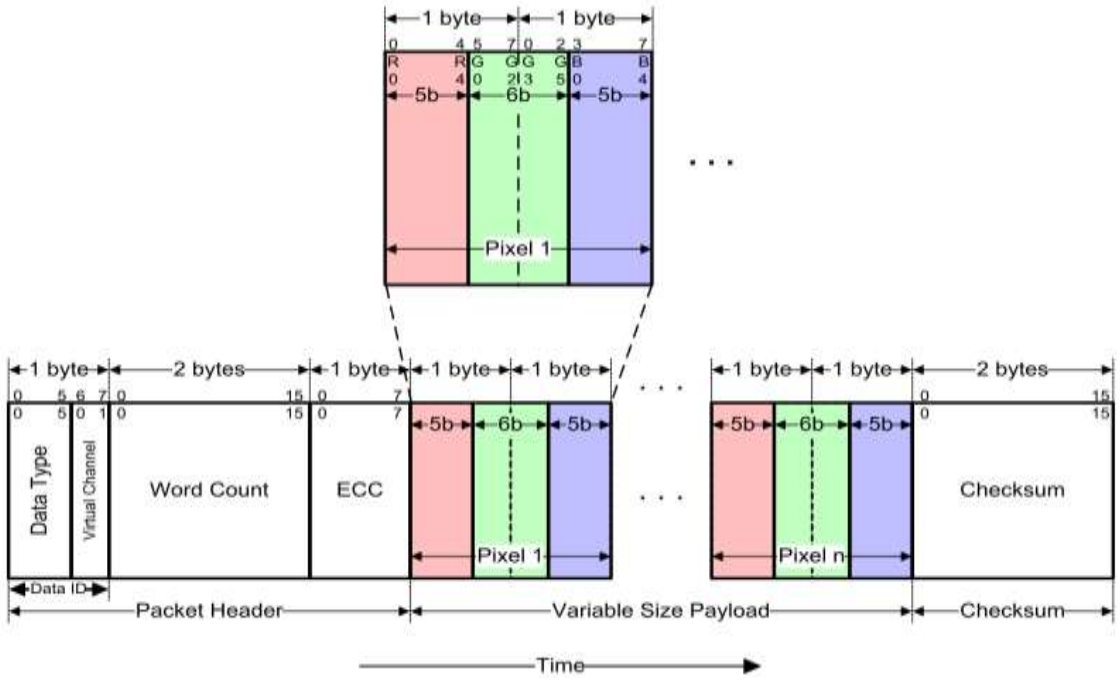


Figure 76: 16-bit per Pixel, Data Type 00 1110 (0Eh)

4.2.1.2. 18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional filled pixels at the end of the display line to make the transmitted width a

multiple of four pixels. The receiving peripheral shall not display the filled pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission. With this format, the total line width (displayed and non-displayed pixels) should be a multiple of four pixels (nine bytes).

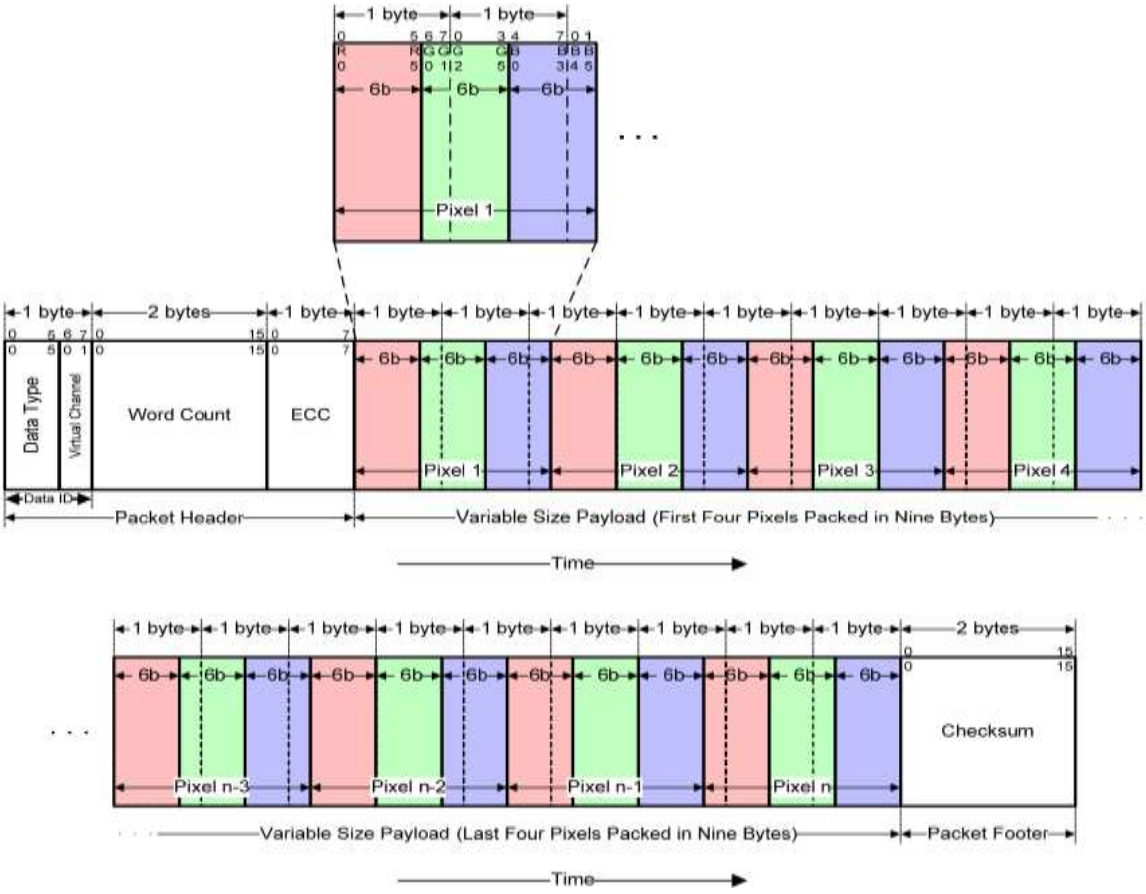


Figure 77: 18-bit per Pixel, Data Type = 01 1110 (1Eh)

4.2.1.3. 18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

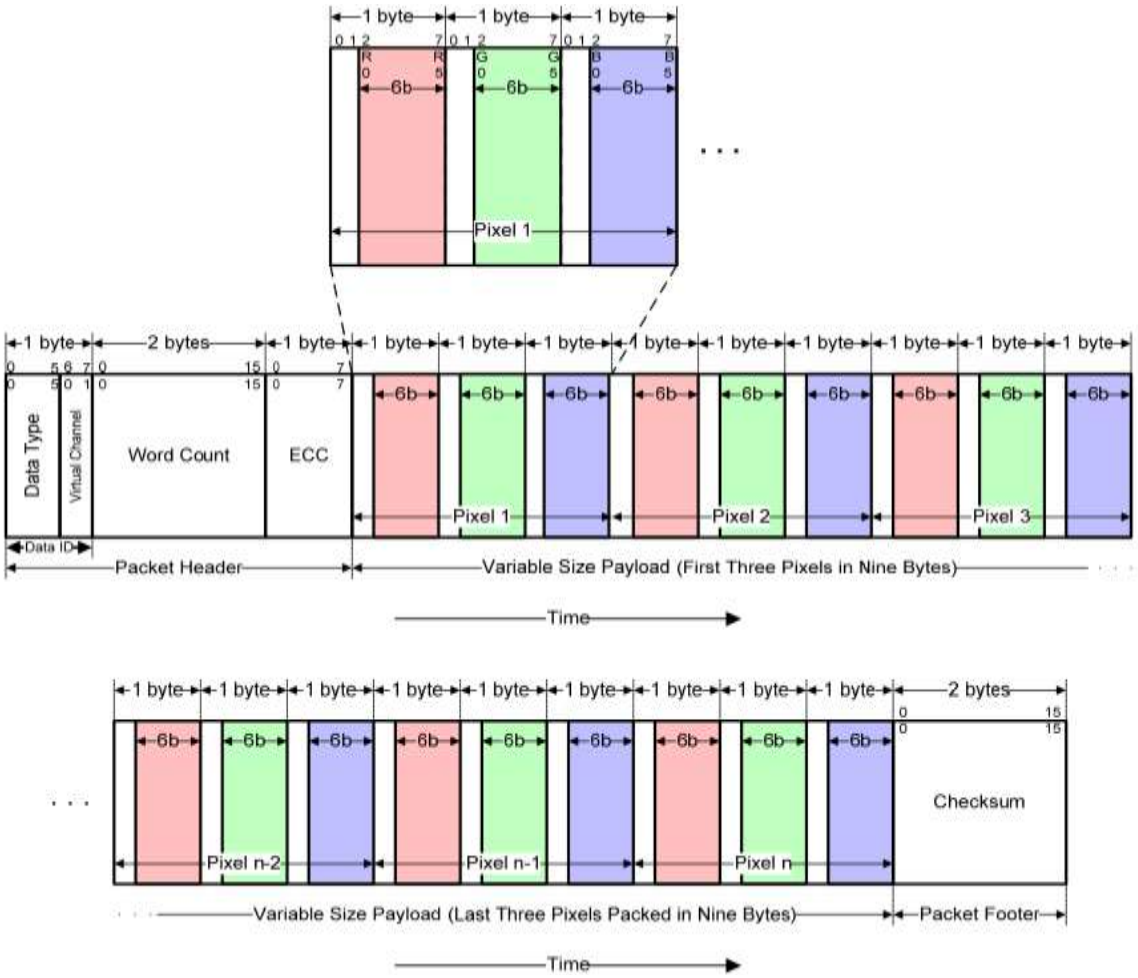


Figure 78: 18-bit per Pixel, Data Type = 10 1110 (2Eh)

4.2.1.4. 24-bit per Pixel, Long Packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

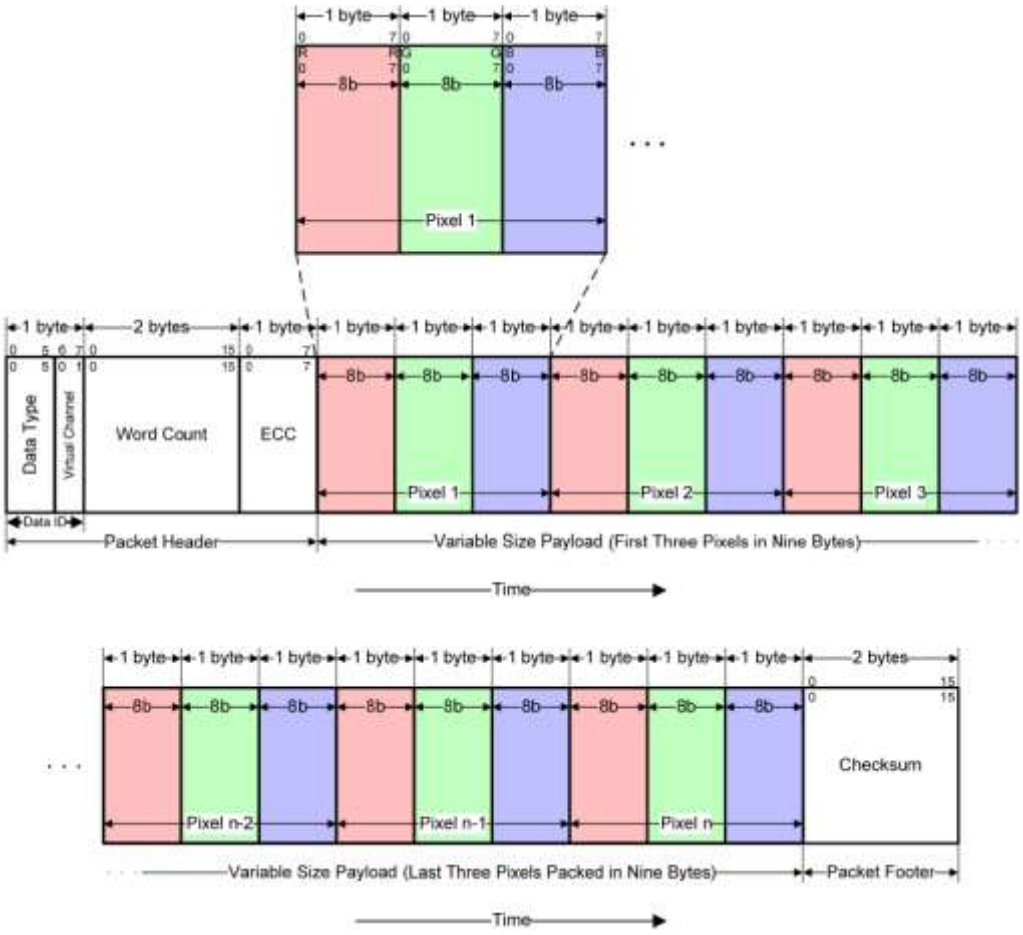


Figure 79: 24-bit per Pixel, Data Type = 11 1110 (3Eh)

4.2.2. 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

Table 32 below lists settings for 24-bit data mapping. Set the EPF[1:0] bits function, which defines three types of data formats for 24-bit data (pixel data r, g, b) mapping.

Table 32: 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

EPF[1:0]	Expand 16-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)	Expand 18-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)
00	0 is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h0} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h0} (Note3): that the data are converted as follows. 16-bit color data R [4:0] = 5'h1F, G [5:0] = 6'h3F, B [4:0] = 5'h1F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF	0 is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h0} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h0} (Note1): that the data are converted as follows. 18-bit color data R [5:0] = 6'h3F, G [5:0] = 6'h3F ,B [5:0] = 6'h3F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF
01	1 is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h7} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h7} (Note4): that the data are converted as follows. 16-bit color data R [4:0] = 5'h0, G [5:0] = 6'h0, B [4:0] = 5'h0 →24-bit pixel data r, g, b [7:0] = 24'h000000	1 is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h3} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h3} (Note2): that the data are converted as follows. 18-bit color data R [5:0] = 6'h0, G [5:0] = 6'h0, B [5:0] = 6'h0 →24-bit pixel data r, g, b [7:0] = 24'h000000
10	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], R [4:2]} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], B [4:2]}	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], R [5:4]} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], B [5:4]}
11	Same as setting "EPF [1:0] = 10"	Same as setting "EPF [1:0] = 10"

	Display image data (24 bits)																							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24-bit	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18-bit EPF[1:0]=00 (Note 1)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18-bit EPF[1:0]=01 (Note 2)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18-bit EPF[1:0]=10	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16-bit EPF[1:0]=00 (Note 3)	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
16-bit EPF[1:0]=01 (Note 4)	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
16-bit EPF[1:0]=10	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

Example1: 16-bit data mapping to 24-bit, EPF[1:0] = 10

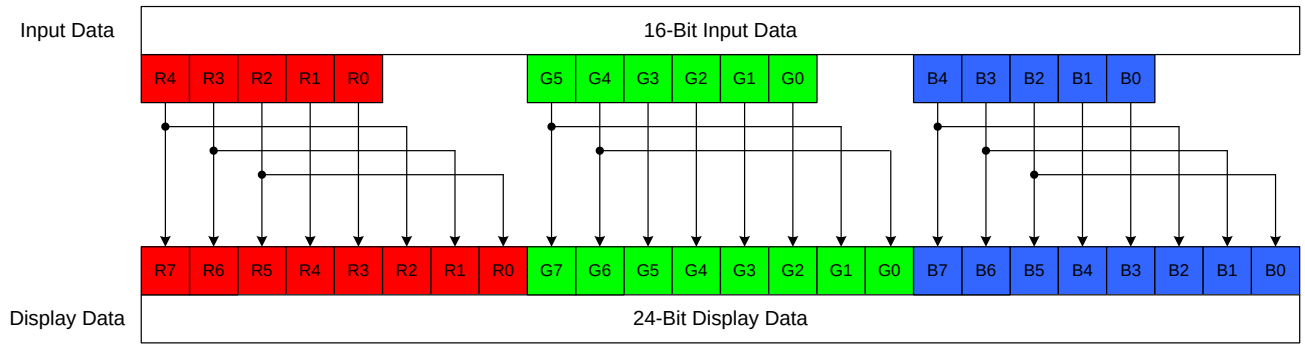


Figure 80: EPF[1:0] = 10, 16-bit Data Mapping to 24-bit

Example2: 18-bit data mapping to 24-bit, EPF[1:0] = 10

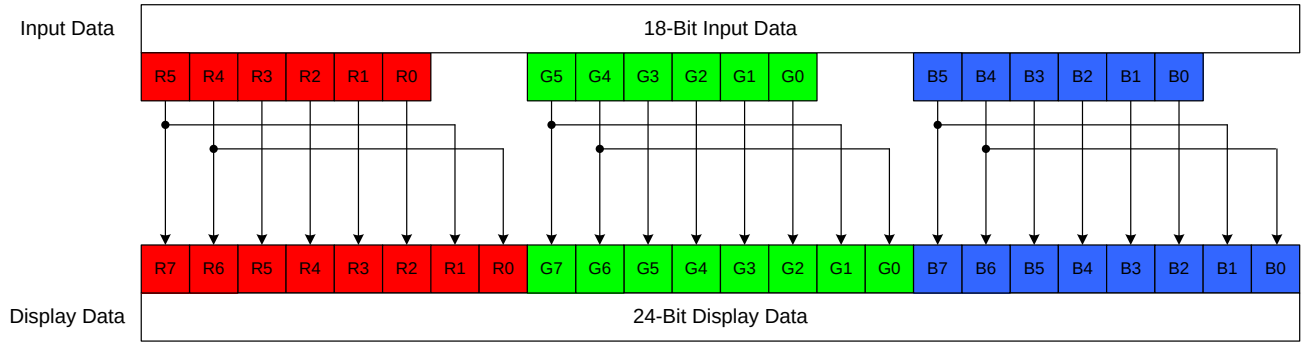


Figure 81: EPF[1:0] = 10, 18-bit Data Mapping to 24-bit

5. Command

5.1. Command Flow

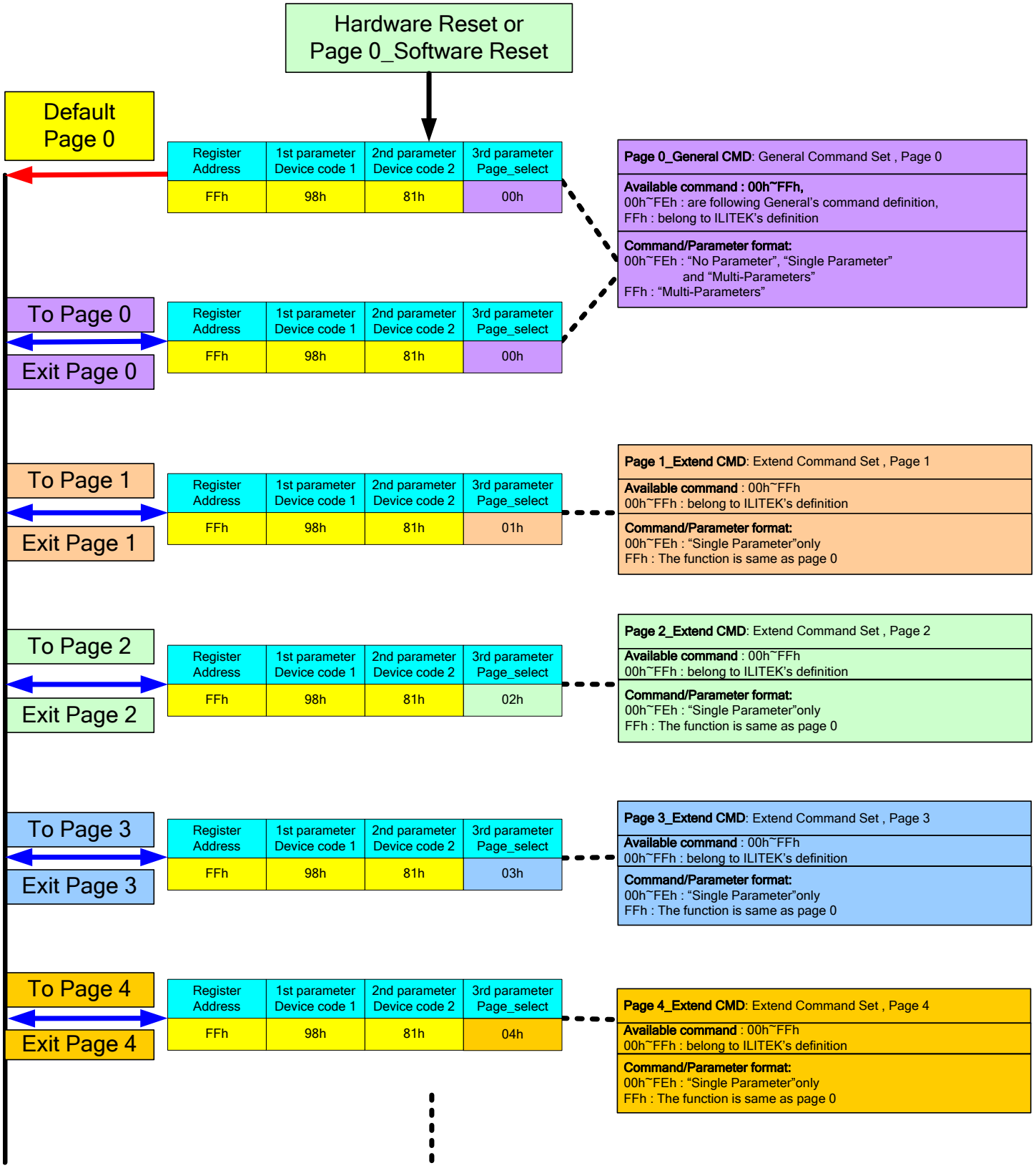


Figure 82: Command Flow

5.2. Command List

5.2.1. Page 0 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P0	00h	-	W	NOP	No Argument								-	-
P0	01h	-	W	Software Reset	No Argument								-	-
P0	05h	1st	R	Read Number of the Errors on DSI	P[7:0]								00h	-
P0	09h	1st	R	Read Display Status	D31	0	0	0	0	D26	0	D24	00h	-
		2nd	R		D23	0	0	0	D19	0	D17	D16	01h	-
		3rd	R		0	0	0	D12	D11	D10	D9	D8	00h	-
		4th	R		D7	D6	D5	0	0	0	0	D0	00h	-
P0	0Ah	1st	R	Read Display Power Mode	D7	D6	0	D4	D3	D2	0	0	08h	-
P0	0Bh	1st	R	Read Display MADCTL	0	0	0	0	D3	0	D1	D0	00h	-
P0	0Ch	1st	R	Read Pixel Format	0	0	0	0	0	D2	D1	D0	07h	
P0	0Dh	1st	R	Read Display Mode	0	0	0	D4	D3	D2	D1	D0	00h	-
P0	0Eh	1st	R	Read Display signal Mode	D7	D6	0	0	0	0	0	D0	00h	-
P0	0Fh	1st	R	Read Display Self-Diagnostic Result	D7	D6	0	0	0	0	0	D0	00h	-
P0	10h	-	W	Sleep In	No Argument								-	-
P0	11h	-	W	Sleep Out	No Argument								-	-
P0	13h	-	W	Normal Display Mode On	No Argument								-	-
P0	22h	-	W	All Pixel Off	No Argument								-	-
P0	23h	-	W	All Pixel On	No Argument								-	-
P0	26h	1st	W	Gamma Curve Set	0	0	0	0	GC[3:0]				01h	-
P0	28h	-	W	Display Off	No Argument								-	-
P0	29h	-	W	Display ON	No Argument								-	-
P0	34h	-	W	TE OFF	No Argument								-	-
P0	35h	1st	W	TE ON	0	0	0	0	0	0	0	M	00h	-
P0	36h	1st	W	Memory Access	0	0	0	0	BGR	0	SS	GS	00h	-
P0	38h	-	W	Idle Mode Off	No Argument								-	-
P0	39h	-	W	Idle Mode On	No Argument								-	-
P0	3Ah	1st	W	Interface Pixel Format	0	0	0	0	0	DBI[2:0]			07h	-
P0	44h	1st	W	Set tear scan line	0	0	0	0	0	TE_LINE[10:8]			00h	-
		2nd			TE_LINE[7:0]								00h	-
P0	45h	1st	R	Get tear scan line	0	0	0	0	0	TE_LINE[10:8]			00h	-
		2nd			TE_LINE[7:0]								00h	-
P0	51h	1st	W	Write Display Brightness	0	0	0	0	DBV[11:8]				00h	-
		2nd			DBV[7:0]								00h	-
P0	52h	1st	R	Read Display Brightness Value	0	0	0	0	DBV[11:8]				00h	-
		2nd			DBV[7:0]								00h	-
P0	53h	1st	W	Write CTRL Display	0	0	BCTRL	0	DD	BL	0	0	00h	-
P0	54h	1st	R	Read CTRL Display	0	0	BCTRL	0	DD	BL	0	0	00h	-
P0	55h	1st	W	Write Power Save	PWRSAVE[7:0]								00h	-
P0	56h	1st	R	Read Power Save	PWRSAVE[7:0]								00h	-
P0	59h	-	W	Stop Transition	No Argument								-	-
P0	5Eh	1st	W	Write CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h	-
		2nd			CMB[7:0]								00h	
P0	5Fh	1st	R	Read CABC Minimum Brightness	0	0	0	0	CMB[11:8]				00h	-
		2nd			CMB[7:0]								00h	
P0	68h	1st	W	Set Transition Time	TT_STP[7:0]								00h	-
		2nd			ST_TIM[7:0]								00h	-
P0	69h	1st	R	Get Transition Time	TT_STP[7:0]								00h	-
		2nd			ST_TIM[7:0]								00h	-

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P0	A1h	1st	R	Read the DDB from the provided location	SID[7:0]								00h	1
		2nd			SID[15:8]								00h	1
		3rd			MRID[7:0]								00h	1
		4th			MRID[15:8]								00h	1
		5th			SID2[7:0]								00h	1
		6th			SID2[15:8]								00h	1
		7th			1	1	1	1	1	1	1	1	FFh	-
P0	A8h	1st	R	Continue reading the DDB from the last read location	D1[7:0]								00h	-
		2nd			D2[7:0]								00h	-
		:			:								00h	-
		nth			Dn[7:0]								00h	-
P0	AAh	1st	R	Read First Checksum	FCS[7:0]								00h	-
P0	AFh	1st	R	Read Continue Checksum	CCS[7:0]								00h	-
P0	DAh	1st	R	Read ID1	ID1[7:0]								00h	3
P0	DBh	1st	R	Read ID2	ID2[6:0]								00h	3
P0	DCh	1st	R	Read ID3	ID3[7:0]								00h	3
P0	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								00h	-

Notes:

1. Undefined commands are treated as NOP (00h) command.

2. Commands 10h, 13h, 22h, 23h, 26h, 28h, 29h, 36h, 38h, 39h, 51h, 53h, 55h, 5Eh and 68h are updated during V-SYNC when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Commands 05h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 45h, 52h, 54h, 56h, 5Fh, 69h, A1h, A8h of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

5.2.2. Page 1 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P1	00h	1st	R	Read ID4	ID4[23:16]								98h	-
P1	01h	1st	R		ID4[15:8]								81h	-
P1	02h	1st	R		ID4[7:0]								5Ch	-
P1	22h	1st	W/R	Set Panel Operation Mode and Data Complement Setting	0	0	EPF[1:0]		BGR_PANEL	REV_PANEL	SS_PANEL	GS_PANEL	30h	1
P1	25h	1st	W/R	Blanking Porch Control	VFP[7:0]								14h	-
P1	26h	1st	W/R		VBP[7:0]								14h	-
P1	29h	1st	W/R	Touch	0	0	0	0	0	0	0	TOUCH_	00h	-
P1	2Eh	1st	W/R	Gate Number	NL[7:0]								C8h	1
P1	31h	1st	W/R	Display Inversion	0	0	0	0	DINV[3:0]				00h	1
P1	34h	1st	W/R	Dithering Enable	0	0	0	0	0	0	0	DITH_EN	00h	1
P1	40h	1st	W/R	Pump Clock Adjustment	0	EXT_CPCK_SEL[1:0		1	0	0	1	VGHL_CL	33h	1
P1	42h	1st	W/R		0	VGHL_CLK_SELA[2:0]			0	VGHL_CLK_SELB[2:0]			44h	1
P1	43h	1st	W/R		0	4002_RATIO_FREQA[2:0]			0	4002_RATIO_FREQB[2:0]			55h	1
P1	50h	1st	W/R	Power Control 1	VREG1[7:0]								95h	1
P1	51h	1st	W/R		VREG2[7:0]								95h	1
P1	52h	1st	W/R	VCOM Control 1	0	0	0	0	0	0	0	VCM1[8]	00h	3
P1	53h	1st	W/R		VCM1[7:0]								7Bh	3
P1	54h	1st	W/R		0	0	0	0	0	0	0	VCM2[8]	00h	3
P1	55h	1st	W/R		VCM2[7:0]								7Bh	3
P1	56h	1st	W/R		0	0	0	NVM2	0	0	0	NVM1	00h	-
P1	58h	1st	W/R	Entry Mode Set	LVD_EN	0	0	0	0	0	0	0	00h	1
P1	60h	1st	W/R	Source Timing Adjust	0	0	SDT[5:0]						14h	1
P1	61h	1st	W/R		0	0	CRT[5:0]						00h	1
P1	62h	1st	W/R		0	0	EQT[5:0]						19h	1
P1	63h	1st	W/R		0	0	PCT[5:0]						10h	1
P1	A0h	1st	W/R	Positive Gamma Correction	0	0	VP0[5:0]						00h	2
P1	A1h	1st	W/R		0	VP4[6:0]							0Dh	2
P1	A2h	1st	W/R		0	VP8[6:0]							1Dh	2
P1	A3h	1st	W/R		0	0	VP12[5:0]						11h	2
P1	A4h	1st	W/R		0	0	VP16[5:0]						0Ch	2
P1	A5h	1st	W/R		0	VP24[6:0]							23h	2
P1	A6h	1st	W/R		0	0	VP36[5:0]						17h	2
P1	A7h	1st	W/R		0	0	VP52[5:0]						1Ch	2
P1	A8h	1st	W/R		VP80[7:0]								82h	2
P1	A9h	1st	W/R		0	0	VP111[5:0]						21h	2
P1	AAh	1st	W/R		0	0	VP144[5:0]						2Ah	2
P1	ABh	1st	W/R		VP175[7:0]								6Bh	2
P1	ACh	1st	W/R		0	0	VP203[5:0]						19h	2
P1	ADh	1st	W/R		0	0	VP219[5:0]						14h	2
P1	AEh	1st	W/R		0	VP231[6:0]							45h	2
P1	AFh	1st	W/R		0	0	VP239[5:0]						1Dh	2
P1	B0h	1st	W/R		0	0	VP243[5:0]						23h	2
P1	B1h	1st	W/R		0	VP247[6:0]							52h	2
P1	B2h	1st	W/R		0	VP251[6:0]							63h	2
P1	B3h	1st	W/R		0	0	VP255[5:0]						39h	2
P1	B6h	1st	W/R	Pad Control	IM_SW_EN	IM_SW[2:0]			RS_SW_EN	0	RS_SW[1:0]		00h	1
P1	B7h	1st	W/R		0	0	0	0	0	0	LANSEL_SW_EN	LANSEL_SW	00h	1

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default	MTP
Page	Address	Parameter											(hex)	(times)
P1	C0h	1st	W/R	Negative Gamma Correction	0	0	VN0[5:0]						00h	2
P1	C1h	1st	W/R		0	VN4[6:0]							0Dh	2
P1	C2h	1st	W/R		0	VN8[6:0]							1Dh	2
P1	C3h	1st	W/R		0	0	VN12[5:0]						11h	2
P1	C4h	1st	W/R		0	0	VN16[5:0]						0Ch	2
P1	C5h	1st	W/R		0	VN24[6:0]							23h	2
P1	C6h	1st	W/R		0	0	VN36[5:0]						17h	2
P1	C7h	1st	W/R		0	0	VN52[5:0]						1Ch	2
P1	C8h	1st	W/R		VN80[7:0]								82h	2
P1	C9h	1st	W/R		0	0	VN111[5:0]						21h	2
P1	CAh	1st	W/R		0	0	VN144[5:0]						2Ah	2
P1	CBh	1st	W/R		VN175[7:0]								6Bh	2
P1	CCh	1st	W/R		0	0	VN203[5:0]						19h	2
P1	CDh	1st	W/R		0	0	VN219[5:0]						14h	2
P1	CEh	1st	W/R		0	VN231[6:0]							45h	2
P1	CFh	1st	W/R		0	0	VN239[5:0]						1Dh	2
P1	D0h	1st	W/R		0	0	VN243[5:0]						23h	2
P1	D1h	1st	W/R		0	VN247[6:0]							52h	2
P1	D2h	1st	W/R		0	VN251[6:0]							63h	2
P1	D3h	1st	W/R		0	0	VN255[5:0]						39h	2
P1	E0h	1st	W/R	NV Memory Write	PGM_DATA[7:0]								00h	-
P1	E1h	1st	W/R		PGM_ADR[7:0]								00h	-
P1	E2h	1st	W/R		PGM_ADR[15:8]								00h	-
P1	E3h	1st	W/R	NV Memory Protection Key	KEY[23:16]								00h	-
P1	E4h	1st	W/R		KEY[15:8]								00h	-
P1	E5h	1st	W/R		KEY[7:0]								00h	-
P1	E6h	1st	R	NV Memory Status Read	0	ID2_MK[2:0]			0	ID1_MK[2:0]			00h	-
P1	E7h	1st	R		0	0	0	0	0	ID3_MK[2:0]			00h	-
P1	E8h	1st	R		GAMMA_P_MK	GAMMA_N_MK	VCM2_MK[2:0]			VCM1_MK[2:0]			00h	-
P1	E9h	1st	R		OTP_BUSY	0	0	0	0	0	0	0	00h	-
P1	F0h	1st	W/R	Time Stamp	Time_Stamp_Week[7:0]								00h	1
P1	F1h	1st	W/R		Time_Stamp_Year[7:0]								00h	1
P1	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								01h	-

5.2.3. Page 2 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P2	03h	1st	W/R	Dynamic Backlight Control 1	0	TT_STP_MED[2:0]			1	TT_STP_LOW[2:0]			29h	1
P2	04h	1st	W/R		0	ST_TIM_LOW[2:0]			0	TT_STP_HIGH[2:0]			14h	1
P2	05h	1st	W/R		0	ST_TIM_HIGH[2:0]			0	ST_TIM_MED[2:0]			32h	1
P2	06h	1st	W/R	Dynamic Backlight Control 2	0	PWM_DUTY_PRECISION[2:0]			0	LEDPWM_POL	LEDON_POL	LEDON	00h	1
P2	07h	1st	W/R		PWM_DIV[7:0]								0Eh	1
P2	10h	1st	W/R	IIE Function Control	0	0	0	0	0	PRT_EN	SKIN_EN	0	06h	1
P2	11h	1st	W/R		0	AUTO_MEAN	0	0	CN_EN	CN_INV	SHP_EN	0	00h	1
P2	12h	1st	W/R		0	0	0	0	0	0	CN_LV[1:0]		02h	1
P2	13h	1st	W/R		0	0	1	0	SRE_MIDIV_LV[1:0		0	0	20h	1
P2	15h	1st	W/R		RGB_MEAN[7:0]								80h	1
P2	16h	1st	W/R		SRE_HYSTERESIS_EN	0	0	SRE_DIM_EN	SRE_SC_EN	SRE_CE_EN	0	0	1Ch	1
P2	17h	1st	W/R		0	SRE_OFFS[2:0]			0	SRE_DIM_STP[2:0]			01h	1
P2	18h	1st	W/R		SRE_DIM_FRAME[7:0]								08h	1
P2	19h	1st	W/R		SRE_SC_GAIN_ADJ[2:0]			SRE_HYSTERESIS_LIMIT[4:0]					C0h	1
P2	1Ah	1st	W/R	IIE Saturation Enhancement Control 1	0	0	SE_RATIO_L[5:0]						07h	1
P2	1Bh	1st	W/R		0	0	SE_RATIO_M[5:0]						09h	1
P2	1Ch	1st	W/R		0	0	SE_RATIO_H[5:0]						0Ch	1
P2	40h	1st	W/R	IIE Saturation Protection Control	0	0	0	LEVEL0_SR[4:0]					02h	1
P2	41h	1st	W/R		0	0	0	LEVEL1_SR[4:0]					04h	1
P2	42h	1st	W/R		0	0	0	LEVEL2_SR[4:0]					06h	1
P2	43h	1st	W/R		0	0	0	LEVEL3_SR[4:0]					08h	1
P2	44h	1st	W/R		0	0	0	LEVEL4_SR[4:0]					0Ah	1
P2	45h	1st	W/R		0	0	0	LEVEL5_SR[4:0]					0Ch	1
P2	46h	1st	W/R		0	0	0	LEVEL6_SR[4:0]					0Eh	1
P2	47h	1st	W/R		0	0	0	LEVEL7_SR[4:0]					0Eh	1
P2	48h	1st	W/R		0	0	0	LEVEL8_SR[4:0]					0Ch	1
P2	49h	1st	W/R		0	0	0	LEVEL9_SR[4:0]					0Ah	1
P2	4Ah	1st	W/R		0	0	0	LEVEL10_SR[4:0]					08h	1
P2	4Bh	1st	W/R		0	0	0	LEVEL11_SR[4:0]					06h	1
P2	4Ch	1st	W/R		0	0	0	LEVEL12_SR[4:0]					04h	1
P2	4Dh	1st	W/R		0	0	0	LEVEL13_SR[4:0]					03h	1
P2	4Eh	1st	W/R		0	0	0	LEVEL14_SR[4:0]					02h	1
P2	4Fh	1st	W/R		0	0	0	LEVEL15_SR[4:0]					00h	1
P2	5Ah	1st	W/R	IIE Sharpness Enhancement Control	0	0	0	SHP_RATIO[4:0]					18h	1
P2	5Bh	1st	W/R		SHP_THR_H[7:0]								64h	1
P2	5Ch	1st	W/R		SHP_THR_L[7:0]								1Eh	1
P2	60h	1st	W/R	IIE Contrast Enhancement Control	0	0	CN_00[5:0]						0Eh	1
P2	61h	1st	W/R		0	0	CN_01[5:0]						18h	1
P2	62h	1st	W/R		0	0	CN_02[5:0]						24h	1
P2	63h	1st	W/R		0	0	CN_03[5:0]						28h	1
P2	64h	1st	W/R		0	0	CN_04[5:0]						24h	1
P2	65h	1st	W/R		0	0	CN_05[5:0]						18h	1
P2	66h	1st	W/R		0	0	CN_06[5:0]						0Eh	1

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P2	D0	1st	W/R	IIE Auto White Balance 1	0	0	0	0	0	0	0	AWB_EN	00	1
P2	D1	1st	W/R	IIE Auto White Balance 2	0	0	R_AWB_1[9:8]		G_AWB_1[9:8]		B_AWB_1[9:8]		3Fh	2
P2	D2	1st	W/R		R_AWB_1[7:0]								FFh	2
P2	D3	1st	W/R		G_AWB_1[7:0]								FFh	2
P2	D4	1st	W/R		B_AWB_1[7:0]								FFh	2
P2	D5	1st	W/R	IIE Auto White Balance 3	0	0	R_AWB_2[9:8]		G_AWB_2[9:8]		B_AWB_2[9:8]		3Fh	2
P2	D6	1st	W/R		R_AWB_2[7:0]								FFh	2
P2	D7	1st	W/R		G_AWB_2[7:0]								FFh	2
P2	D8	1st	W/R		B_AWB_2[7:0]								FFh	2
P2	D9	1st	W/R	IIE Auto White Balance 4	0	0	R_AWB_3[9:8]		G_AWB_3[9:8]		B_AWB_3[9:8]		3Fh	2
P2	DA	1st	W/R		R_AWB_3[7:0]								FFh	2
P2	DB	1st	W/R		G_AWB_3[7:0]								FFh	2
P2	DC	1st	W/R		B_AWB_3[7:0]								FFh	2
P2	DD	1st	W/R	IIE Auto White Balance 5	0	0	R_AWB_4[9:8]		G_AWB_4[9:8]		B_AWB_4[9:8]		3Fh	2
P2	DE	1st	W/R		R_AWB_4[7:0]								FFh	2
P2	DF	1st	W/R		G_AWB_4[7:0]								FFh	2
P2	E0	1st	W/R		B_AWB_4[7:0]								FFh	2
P2	E1	1st	W/R	IIE Auto White Balance 6	0	0	R_AWB_5[9:8]		G_AWB_5[9:8]		B_AWB_5[9:8]		3Fh	2
P2	E2	1st	W/R		R_AWB_5[7:0]								FFh	2
P2	E3	1st	W/R		G_AWB_5[7:0]								FFh	2
P2	E4	1st	W/R		B_AWB_5[7:0]								FFh	2
P2	E5	1st	W/R	IIE Auto White Balance 7	0	0	R_AWB_6[9:8]		G_AWB_6[9:8]		B_AWB_6[9:8]		3Fh	2
P2	E6	1st	W/R		R_AWB_6[7:0]								FFh	2
P2	E7	1st	W/R		G_AWB_6[7:0]								FFh	2
P2	E8	1st	W/R		B_AWB_6[7:0]								FFh	2
P2	E9	1st	W/R	IIE Auto White Balance 8	0	0	R_AWB_7[9:8]		G_AWB_7[9:8]		B_AWB_7[9:8]		3Fh	2
P2	EA	1st	W/R		R_AWB_7[7:0]								FFh	2
P2	EB	1st	W/R		G_AWB_7[7:0]								FFh	2
P2	EC	1st	W/R		B_AWB_7[7:0]								FFh	2
P2	ED	1st	W/R	IIE Auto White Balance 9	Color_Temp_Adj[7:0]								60h	2
P2	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								02h	-

5.2.4. Page 3 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P3	01h	1st	W/R		Reserve for other setting								-	1
P3	02h	1st	W/R		Reserve for other setting								-	1
P3	03h	1st	W/R		STV_A_Rise[9:8]		Phase_STV_A[1:0]		Overlap_STV_A[2:0]				-	1
P3	04h	1st	W/R		STV_B_Rise[9:8]		Phase_STV_B[1:0]		Overlap_STV_B[2:0]				-	1
P3	05h	1st	W/R		STV_C_Rise[9:8]		Phase_STV_C[1:0]		Overlap_STV_C[2:0]				-	1
P3	06h	1st	W/R		STV_A_Rise[7:0]								-	1
P3	07h	1st	W/R		STV_B_Rise[7:0]								-	1
P3	08h	1st	W/R		STV_C_Rise[7:0]								-	1
P3	09h	1st	W/R		FTI_1_Rise[7:0]								-	1
P3	0Ah	1st	W/R		FTI_2_Rise[7:0]								-	1
P3	0Bh	1st	W/R		FTI_3_Rise[7:0]								-	1
P3	0Ch	1st	W/R		FTI_1_Fall[7:0]								-	1
P3	0Dh	1st	W/R		FTI_2_Fall[7:0]								-	1
P3	0Eh	1st	W/R		FTI_3_Fall[7:0]								-	1
P3	0Fh	1st	W/R		CLW_1_Rise[7:0]								-	1
P3	10h	1st	W/R		CLW_2_Rise[7:0]								-	1
P3	11h	1st	W/R		Reserve for other setting								-	1
P3	12h	1st	W/R		Reserve for other setting								-	1
P3	13h	1st	W/R		CLW_X_Fall[7:0]								-	1
P3	14h	1st	W/R		Reserve for other setting								-	1
P3	15h	1st	W/R		GPM_R_Stage_i[7:0]								-	1
P3	16h	1st	W/R		GPM_R_Stage_ii[7:0]								-	1
P3	17h	1st	W/R		GPM_F_Stage_i[7:0]								-	1
P3	18h	1st	W/R		GPM_F_Stage_ii[7:0]								-	1
P3	19h	1st	W/R		Reserve for other setting								-	1
P3	1Ah	1st	W/R		Reserve for other setting								-	1
P3	1Bh	1st	W/R		Reserve for other setting								-	1
P3	1Ch	1st	W/R		Reserve for other setting								-	1
P3	1Dh	1st	W/R		Reserve for other setting								-	1
P3	1Eh	1st	W/R	GIP Setting 1	GS_ENA	CLK_A_Rise[10:8]			Reserve	CLK_A_Fall[10:8]			-	1
P3	1Fh	1st	W/R		Reserve	CLK_B_Rise[10:8]			Reserve	CLK_B_Fall[10:8]			-	1
P3	20h	1st	W/R		CLK_A_Rise[7:0]								-	1
P3	21h	1st	W/R		CLK_A_Fall[7:0]								-	1
P3	22h	1st	W/R		CLK_B_Rise[7:0]								-	1
P3	23h	1st	W/R		Reserve for other setting								-	1
P3	24h	1st	W/R		CLK_Keep_Pos1[7:0]								-	1
P3	25h	1st	W/R		CLK_Keep_Pos2[7:0]								-	1
P3	26h	1st	W/R		Reserve for other setting								-	1
P3	27h	1st	W/R		Reserve for other setting								-	1
P3	28h	1st	W/R		CLK_Disable	CLK_x_Numb[2:0]			CLK_Keep	Phase_CLK[2:0]			-	1
P3	29h	1st	W/R		Reserve for other setting				Overlap_CLK[3:0]				-	1
P3	2Ah	1st	W/R		Reserve for other setting								-	1
P3	2Bh	1st	W/R		Reserve for other setting								-	1
P3	2Ch	1st	W/R		Reserve for other setting								-	1
P3	2Dh	1st	W/R		Reserve for other setting								-	1
P3	2Eh	1st	W/R		Reserve for other setting								-	1
P3	2Fh	1st	W/R		Reserve for other setting								-	1
P3	30h	1st	W/R		Reserve for other setting								-	1
P3	31h	1st	W/R		Reserve for other setting								-	1
P3	32h	1st	W/R		Reserve for other setting								-	1
P3	33h	1st	W/R		Reserve for other setting								-	1
P3	34h	1st	W/R		Reserve for other setting								-	1
P3	35h	1st	W/R		Reserve for other setting								-	1
P3	36h	1st	W/R		Reserve for other setting								-	1
P3	37h	1st	W/R		Reserve for other setting								-	1
P3	38h	1st	W/R		Reserve for other setting								-	1
P3	39h	1st	W/R		Reserve for other setting								-	1
P3	3Ah	1st	W/R		Reserve for other setting								-	1
P3	3Bh	1st	W/R		Reserve for other setting								-	1

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P3	3Ch	1st	W/R	GIP Setting 1	Reserve for other setting								-	1
P3	3Dh	1st	W/R		Reserve for other setting								-	1
P3	3Eh	1st	W/R		Reserve for other setting								-	1
P3	3Fh	1st	W/R		Reserve for other setting								-	1
P3	40h	1st	W/R		Reserve for other setting								-	1
P3	41h	1st	W/R		Reserve for other setting								-	1
P3	42h	1st	W/R		Reserve for other setting								-	1
P3	43h	1st	W/R		Reserve for other setting								-	1
P3	44h	1st	W/R		Reserve for other setting								-	1
P3	50h	1st	W/R	GIP Setting 2	STV_1_MUX[2:0]				STV_2_MUX[2:0]				-	1
P3	51h	1st	W/R		STV_3_MUX[2:0]				STV_4_MUX[2:0]				-	1
P3	52h	1st	W/R		STV_5_MUX[2:0]				STV_6_MUX[2:0]				-	1
P3	53h	1st	W/R		STV_7_MUX[2:0]				STV_8_MUX[2:0]				-	1
P3	54h	1st	W/R		STV_9_MUX[2:0]				STV_10_MUX[2:0]				-	1
P3	55h	1st	W/R		STV_11_MUX[2:0]				STV_12_MUX[2:0]				-	1
P3	56h	1st	W/R		CLK_1_MUX[2:0]				CLK_2_MUX[2:0]				-	1
P3	57h	1st	W/R		CLK_3_MUX[2:0]				CLK_4_MUX[2:0]				-	1
P3	58h	1st	W/R		CLK_5_MUX[2:0]				CLK_6_MUX[2:0]				-	1
P3	59h	1st	W/R		CLK_7_MUX[2:0]				CLK_8_MUX[2:0]				-	1
P3	5Ah	1st	W/R		CLK_9_MUX[2:0]				CLK_10_MUX[2:0]				-	1
P3	5Bh	1st	W/R		CLK_11_MUX[2:0]				CLK_12_MUX[2:0]				-	1
P3	5Ch	1st	W/R		CLK_13_MUX[2:0]				CLK_14_MUX[2:0]				-	1
P3	5Dh	1st	W/R		CLK_15_MUX[2:0]				CLK_16_MUX[2:0]				-	1
P3	5Eh	1st	W/R	GIP Setting 3	Reserve for other setting			BACKWARDS	Reserve for other setting			FORWARDS	-	1
P3	5Fh	1st	W/R		0			GOUT_01_MUX_FW[4:0]					-	1
P3	60h	1st	W/R		0			GOUT_02_MUX_FW[4:0]					-	1
P3	61h	1st	W/R		0			GOUT_03_MUX_FW[4:0]					-	1
P3	62h	1st	W/R		0			GOUT_04_MUX_FW[4:0]					-	1
P3	63h	1st	W/R		0			GOUT_05_MUX_FW[4:0]					-	1
P3	64h	1st	W/R		0			GOUT_06_MUX_FW[4:0]					-	1
P3	65h	1st	W/R		0			GOUT_07_MUX_FW[4:0]					-	1
P3	66h	1st	W/R		0			GOUT_08_MUX_FW[4:0]					-	1
P3	67h	1st	W/R		0			GOUT_09_MUX_FW[4:0]					-	1
P3	68h	1st	W/R		0			GOUT_10_MUX_FW[4:0]					-	1
P3	69h	1st	W/R		0			GOUT_11_MUX_FW[4:0]					-	1
P3	6Ah	1st	W/R		0			GOUT_12_MUX_FW[4:0]					-	1
P3	6Bh	1st	W/R		0			GOUT_13_MUX_FW[4:0]					-	1
P3	6Ch	1st	W/R		0			GOUT_14_MUX_FW[4:0]					-	1
P3	6Dh	1st	W/R		0			GOUT_15_MUX_FW[4:0]					-	1
P3	6Eh	1st	W/R		0			GOUT_16_MUX_FW[4:0]					-	1
P3	6Fh	1st	W/R		0			GOUT_17_MUX_FW[4:0]					-	1
P3	70h	1st	W/R		0			GOUT_18_MUX_FW[4:0]					-	1
P3	71h	1st	W/R		0			GOUT_19_MUX_FW[4:0]					-	1
P3	72h	1st	W/R		0			GOUT_20_MUX_FW[4:0]					-	1
P3	73h	1st	W/R		0			GOUT_21_MUX_FW[4:0]					-	1
P3	74h	1st	W/R		0			GOUT_22_MUX_FW[4:0]					-	1
P3	75h	1st	W/R		0			GOUT_01_MUX_BW[4:0]					-	1
P3	76h	1st	W/R		0			GOUT_02_MUX_BW[4:0]					-	1
P3	77h	1st	W/R		0			GOUT_03_MUX_BW[4:0]					-	1
P3	78h	1st	W/R		0			GOUT_04_MUX_BW[4:0]					-	1
P3	79h	1st	W/R		0			GOUT_05_MUX_BW[4:0]					-	1
P3	7Ah	1st	W/R		0			GOUT_06_MUX_BW[4:0]					-	1
P3	7Bh	1st	W/R		0			GOUT_07_MUX_BW[4:0]					-	1
P3	7Ch	1st	W/R		0			GOUT_08_MUX_BW[4:0]					-	1
P3	7Dh	1st	W/R		0			GOUT_09_MUX_BW[4:0]					-	1
P3	7Eh	1st	W/R		0			GOUT_10_MUX_BW[4:0]					-	1
P3	7Fh	1st	W/R		0			GOUT_11_MUX_BW[4:0]					-	1
P3	80h	1st	W/R		0			GOUT_12_MUX_BW[4:0]					-	1
P3	81h	1st	W/R		0			GOUT_13_MUX_BW[4:0]					-	1
P3	82h	1st	W/R		0			GOUT_14_MUX_BW[4:0]					-	1

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P3	83h	1st	W/R	GIP Setting 3	0			GOUT_15_MUX_BW[4:0]					-	1
P3	84h	1st	W/R		0			GOUT_16_MUX_BW[4:0]					-	1
P3	85h	1st	W/R		0			GOUT_17_MUX_BW[4:0]					-	1
P3	86h	1st	W/R		0			GOUT_18_MUX_BW[4:0]					-	1
P3	87h	1st	W/R		0			GOUT_19_MUX_BW[4:0]					-	1
P3	88h	1st	W/R		0			GOUT_20_MUX_BW[4:0]					-	1
P3	89h	1st	W/R		0			GOUT_21_MUX_BW[4:0]					-	1
P3	8Ah	1st	W/R		0			GOUT_22_MUX_BW[4:0]					-	1
P3	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								03h	-

5.2.5. Page 4 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P4	00h	1st	W/R	DSI Lanes Control	MIPI_LANE_SEL	0	0	0	0	0	0	0	80h	1
P4	0Bh	1st	W/R	SSC Function	SSC_DIG_EN	SSC_DIG_STEP[2:0]			0	0	0	0	00h	-
P4	0Eh	1st	W/R		SSC_DIG_CNT[7:0]								00h	-
P4	21h	1st	W/R	Charge-Pump Setting	DMY_PUMP	0	1	1	0	0	0	0	B0h	1
P4	26h	1st	W/R	Internal SD Timing Control	DET_TOLERANCE_OP[3:0]				0	1	1	0	76h	1
P4	27h	1st	W/R	Touch Synchronization Timing Adjust	TOUCH_OPT[1:0]		VSOD[1:0]		HSOM[1:0]		HFP_HBP_OPT	VS_PW_OPT	00h	1
P4	28h	1st	W/R		HSOD[7:0]								05h	1
P4	29h	1st	W/R		HSOHW[7:0]								19h	1
P4	2Ah	1st	W/R		VS_OUT_EN	HS_OUT_EN	VS_OUT_POL	HS_OUT_POL	0	0	STB_EN	0	F0h	1
P4	2Dh	1st	W/R	BIST Mode Function	FRM_PT[7:0]								FFh	1
P4	2Fh	1st	W/R		0	0	FRM_CYC[1:0]		0	0	0	FRM_EN	00h	1
P4	35h	1st	W/R	Source Timing Setting	0	0	0	1	HZ_OPT	1	1	1	17h	1
P4	3Ah	1st	W/R	Power Saving Control	PS_EN	PCST[6:0]							A4h	1
P4	69h	1st	W/R	Power Control 1	1	CP_VCL_CLP_OPTION_PRE[2:0]			0	1	1	1	D7h	-
P4	6Eh	1st	W/R	Power Control 2	0	DI_PWR_REG	REG1_VRH_CP[5:0]						6Ah	1
P4	6Fh	1st	W/R	Power Control 3	0	DI_CP_VGH_BH[2:0]			DI_CP_VGL_BL[2:0]			0	34h	1
P4	7Ah	1st	W/R	VREG1/2 Setting	0	0	0	DI_REG_REG1_EN_CAP	0	0	0	0	00h	1
P4	87h	1st	W/R	LVD Function 1	DI_LVD_CTL[3:0]				1	0	1	0	BAh	1
P4	88h	1st	W/R	LVD Function 2	DIS_LVD_CHK	0	0	0	1	0	1	1	8Bh	1
P4	8Bh	1st	W/R	VCOM Control 2	1	1	1	0	DI_VCM_SEL0_E	0	1	1	E3h	1
P4	8Dh	1st	W/R	Power Control 4	0	DI_VCOM_CP_VGLCLP[6:0]							14h	1
P4	B2h	1st	W/R	Reload Gamma Setting	RELOAD_GMA_EN	RELOAD_GMA_LINE8_EN	0	1	0	0	0	1	D1h	1
P4	B5h	1st	W/R	Gamma Bias Level	0	0	0	0	0	DI_GMA_GAP[2:0]			02h	1
P4	BBh	1st	W/R	TS_CTRL 1	EN_TEMP_PROCESS	0	CP_VGH_TAP_C[5:0]						1Eh	1
P4	BCh	1st	W/R		0	0	CP_VGH_TAP_L[5:0]						1Eh	1
P4	BDh	1st	W/R		0	0	CP_VGH_TAP_M[5:0]						1Eh	1
P4	BEh	1st	W/R		0	0	CP_VGH_TAP_H[5:0]						1Eh	1
P4	BFh	1st	W/R		VCOM_C[7:0]								4Ch	1
P4	C0h	1st	W/R		VCOM_L[7:0]								4Ch	1
P4	C1h	1st	W/R		VCOM_M[7:0]								4Ch	1
P4	C2h	1st	W/R		VCOM_H[7:0]								4Ch	1
P4	C4h	1st	R	Read VCOM OTP Data	0	0	0	0	0	0	0	OTP_VCM1[8]	00h	-
P4	C5h	1st	R		OTP_VCM1[7:0]								7Bh	-
P4	C6h	1st	R		0	0	0	0	0	0	0	OTP_VCM2[8]	00h	-
P4	C7h	1st	R		OTP_VCM2[7:0]								7Bh	-

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P4	C8h	1st	W/R	TS_CTRL 2	TS_TH0[7:0]								00h	-
P4	C9h	1st	W/R		TS_TH1[7:0]								00h	-
P4	CAh	1st	W/R		TS_TH2[7:0]								00h	-
P4	CBh	1st	W/R		TS_TH3[7:0]								00h	-
P4	CCh	1st	W/R		TS_TH0[9:8]		TS_TH1[9:8]		TS_TH2[9:8]		TS_TH3[9:8]		00h	1
P4	CDh	1st	W/R		TS_DEBT_OPT[3:0]				TS_HYST_OPT[3:0]				02h	1
P4	CEh	1st	W/R		EN_TS	VCOM_C [8]	VCOM_L [8]	VCOM_ M[8]	VCOM_ H[8]	1	0	0	04h	1
P4	D7h	1st	W/R	OTP Control	0	0	0	OTP_PA TH	PROG_SEL[1:0]		0	0	1C	-
P4	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								04h	-

5.2.6. Page 5 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P5	00h	1st	W/R	Fine Digital Gamma Control 1	FineOffsetR00[5:0]						GRPR_OP0[9:8]		xxh	2
P5	01h	1st	W/R		GRPR_OP0[7:0]								xxh	2
P5	02h	1st	W/R		FineOffsetR01[5:0]						GRPR_OP1[9:8]		xxh	2
P5	03h	1st	W/R		GRPR_OP1[7:0]								xxh	2
P5	04h	1st	W/R		FineOffsetR02[5:0]						GRPR_OP2[9:8]		xxh	2
P5	05h	1st	W/R		GRPR_OP1[7:0]								xxh	2
P5	06h	1st	W/R		FineOffsetR03[5:0]						GRPR_OP3[9:8]		xxh	2
P5	07h	1st	W/R		GRPR_OP3[7:0]								xxh	2
P5	08h	1st	W/R		FineOffsetR04[5:0]						GRPR_OP4[9:8]		xxh	2
P5	09h	1st	W/R		GRPR_OP4[7:0]								xxh	2
P5	:	1st	W/R		:								xxh	2
P5		1st	W/R										xxh	2
P5	38h	1st	W/R		FineOffsetR28[5:0]						GRPR_OP28[9:8]		xxh	2
P5	39h	1st	W/R		GRPR_OP28[7:0]								xxh	2
P5	3Ah	1st	W/R		0	0	0	0	0	0	GRPR_OP29[9:8]		xxh	2
P5	3Bh	1st	W/R		GRPR_OP29[7:0]								xxh	2
P5	3Ch	1st	W/R		0	0	0	0	0	0	GRPR_OP30[9:8]		xxh	2
P5	3Dh	1st	W/R		GRPR_OP30[7:0]								xxh	2
P5	3Eh	1st	W/R		0	0	0	0	0	0	GRPR_OP31[9:8]		xxh	2
P5	3Fh	1st	W/R		GRPR_OP31[7:0]								xxh	2
P5	:	1st	W/R		:								xxh	2
P5		1st	W/R										xxh	2
P5	5Ah	1st	W/R		0	0	0	0	0	0	GRPR_OP45[9:8]		xxh	2
P5	5Bh	1st	W/R		GRPR_OP45[7:0]								xxh	2
P5	85h	1st	W/R	Digital 3 Gamma Enable	0	1	0	0	EN_3G	0	0	0	40h	1
P5	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								05h	-

5.2.7. Page 6 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P6	00h	1st	W/R	Fine Digital Gamma Control 2	FineOffsetG00[5:0]						GRPG_OP0[9:8]		xxh	2
P6	01h	1st	W/R		GRPG_OP0[7:0]								xxh	2
P6	02h	1st	W/R		FineOffsetG01[5:0]						GRPG_OP1[9:8]		xxh	2
P6	03h	1st	W/R		GRPG_OP1[7:0]								xxh	2
P6	04h	1st	W/R		FineOffsetG02[5:0]						GRPG_OP2[9:8]		xxh	2
P6	05h	1st	W/R		GRPG_OP1[7:0]								xxh	2
P6	06h	1st	W/R		FineOffsetG03[5:0]						GRPG_OP3[9:8]		xxh	2
P6	07h	1st	W/R		GRPG_OP3[7:0]								xxh	2
P6	08h	1st	W/R		FineOffsetG04[5:0]						GRPG_OP4[9:8]		xxh	2
P6	09h	1st	W/R		GRPG_OP4[7:0]								xxh	2
P6	:	1st	W/R		:								xxh	2
P6		1st	W/R										xxh	2
P6	38h	1st	W/R		FineOffsetG28[5:0]						GRPG_OP28[9:8]		xxh	2
P6	39h	1st	W/R		GRPG_OP28[7:0]								xxh	2
P6	3Ah	1st	W/R		0	0	0	0	0	0	GRPG_OP29[9:8]		xxh	2
P6	3Bh	1st	W/R		GRPG_OP29[7:0]								xxh	2
P6	3Ch	1st	W/R		0	0	0	0	0	0	GRPG_OP30[9:8]		xxh	2
P6	3Dh	1st	W/R		GRPG_OP30[7:0]								xxh	2
P6	3Eh	1st	W/R		0	0	0	0	0	0	GRPG_OP31[9:8]		xxh	2
P6	3Fh	1st	W/R		GRPG_OP31[7:0]								xxh	2
P6	:	1st	W/R		:								xxh	2
P6		1st	W/R										xxh	2
P6	5Ah	1st	W/R		0	0	0	0	0	0	GRPG_OP45[9:8]		xxh	2
P6	5Bh	1st	W/R		GRPG_OP45[7:0]								xxh	2
P6	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								06h	-

5.2.8. Page 7 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P7	00h	1st	W/R	Fine Digital Gamma Control 3	FineOffsetB00[5:0]						GRPB_OP0[9:8]		xxh	2
P7	01h	1st	W/R		GRPB_OP0[7:0]								xxh	2
P7	02h	1st	W/R		FineOffsetB01[5:0]						GRPB_OP1[9:8]		xxh	2
P7	03h	1st	W/R		GRPB_OP1[7:0]								xxh	2
P7	04h	1st	W/R		FineOffsetB02[5:0]						GRPB_OP2[9:8]		xxh	2
P7	05h	1st	W/R		GRPB_OP1[7:0]								xxh	2
P7	06h	1st	W/R		FineOffsetB03[5:0]						GRPB_OP3[9:8]		xxh	2
P7	07h	1st	W/R		GRPB_OP3[7:0]								xxh	2
P7	08h	1st	W/R		FineOffsetB04[5:0]						GRPB_OP4[9:8]		xxh	2
P7	09h	1st	W/R		GRPB_OP4[7:0]								xxh	2
P7	:	1st	W/R		:								xxh	2
P7		1st	W/R										xxh	2
P7	38h	1st	W/R		FineOffsetB28[5:0]						GRPB_OP28[9:8]		xxh	2
P7	39h	1st	W/R		GRPB_OP28[7:0]								xxh	2
P7	3Ah	1st	W/R		0	0	0	0	0	0	GRPB_OP29[9:8]		xxh	2
P7	3Bh	1st	W/R		GRPB_OP29[7:0]								xxh	2
P7	3Ch	1st	W/R		0	0	0	0	0	0	GRPB_OP30[9:8]		xxh	2
P7	3Dh	1st	W/R		GRPB_OP30[7:0]								xxh	2
P7	3Eh	1st	W/R		0	0	0	0	0	0	GRPB_OP31[9:8]		xxh	2
P7	3Fh	1st	W/R		GRPB_OP31[7:0]								xxh	2
P7	:	1st	W/R		:								xxh	2
P7		1st	W/R										xxh	2
P7	5Ah	1st	W/R		0	0	0	0	0	0	GRPB_OP45[9:8]		xxh	2
P7	5Bh	1st	W/R		GRPB_OP45[7:0]								xxh	2
P7	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								07h	-

5.3. Page 0 Command Description

5.3.1. NOP (00h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>00h</td><td>-</td><td>W</td><td colspan="9">No Argument</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">00h: NOP (No Operation).
This command is an empty command. It does not have any effect on the ILI9881C-05.
However, it can be used to terminate Memory Write or Memory Write Continue as described in RAMWR (Memory Write) and RAMWRC (Memory Write Continue) Commands.</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"></td></tr>
</table>

5.3.2. Software Reset (01h)

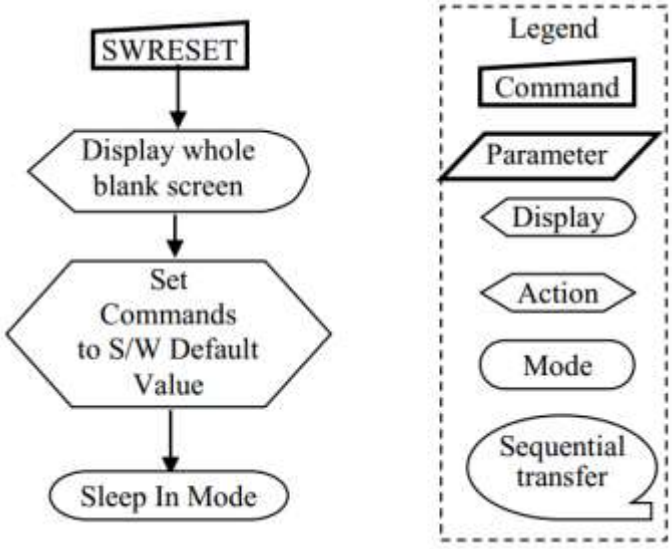
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
01h	-	W	No Argument								-
Description		01h: SWRESET (Software Reset). When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) The display is blank immediately. *Note: The Frame Memory content is kept or not by this command*									
Restriction		It is necessary to wait 5msec before sending a new command after software reset. The display module loads all factory default values of the display supplier to the registers during this 5msec. If Software Reset is applied during the Sleep Out mode, it will be necessary to wait 120msec for Sleep In sequence before sending the Sleep Out command. The Software Reset Command cannot be sent during the Sleep Out sequence.									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

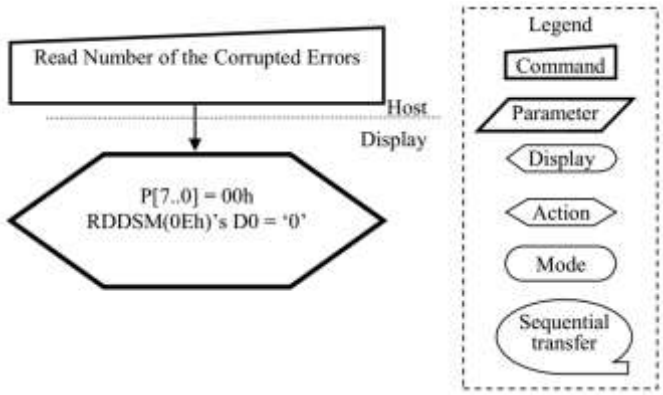
Default

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart



5.3.3. Read Number of the Errors on DSI (05h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>05h</td><td>1st</td><td>R</td><td colspan="8">P[7:0]</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="10">05h: RDNUMED (Read Number of the Errors on DSI).
The parameter indicates the amount of errors on the DSI. The more detailed description of the bits is below.
P[6..0] bits indicate the amount of the error.
P[7] is set to 1 if there is overflow with P[6..0] bits.
P[7..0] bits are set to 0 (and RDDSM (0Eh)’s D0 is set 0 at the same time) after the parameter information is sent (= the read function is completed).
See also sections: “4.1.3.2.2.2 Acknowledge with Error Report (AwER)” and “5.3.9 Read Display Signal Mode (0Eh)”.</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="10">None</td></tr>
<tr><td colspan="2">Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td colspan="2">Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
<tr><td colspan="2">Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

5.3.4. Read Display Status (09h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
09h	1st	R	D31	0	0	0	0	D26	0	D24	00h
	2nd	R	D23	0	0	0	D19	0	D17	D16	01h
	3rd	R	0	0	0	D12	D11	D10	D9	D8	00h
	4th	R	D7	D6	D5	0	0	0	0	D0	00h

Description

This command indicates the current status of the display, as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	0	Booster Off
		1	Booster On
D26	RGB/BGR order	0	RGB (When MADCTL D3 = 0)
		1	BGR (When MADCTL D3= 1)
D24	Source scan sequence	0	Source output Left to Right (When MADCTL D1 = 0)
		1	Source output Right to Left (When MADCTL D1 = 1)
D23	Gate scan sequence	0	Gate output Top to Bottom (When MADCTL D0 = 0)
		1	Gate output Bottom to Top (When MADCTL D0 = 1)
D19	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D17	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D16	Display Normal Mode On/Off	0	Display Normal Mode Off (All Pixels Off or All Pixels On mode)
		1	Display Normal Mode On
D13	Inversion status	0	Inversion Off
		1	Inversion On
D12	All Pixel On	0	Normal mode
		1	All Pixels On
D11	All Pixel Off	0	Normal mode
		1	All Pixels Off
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	TE ON/OFF	0	TE OFF
		1	TE ON
D8	Gamma Curve Selection [2:0]	000	Gamma Curve 1
D7		others	Not defined
D6			
D5	TE Mode	0	TE Mode 1
		1	TE Mode 2
D0	Parity Error on DSI	0	No Parity Error
		1	Parity Error

Restriction	None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_01h_00h_00h
S/W Reset	00h_01h_00h_00h
H/W Reset	00h_01h_00h_00h

5.3.5. Read Display Power Mode (0Ah)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Ah	1st	R	D7	D6	0	D4	D3	D2	0	0	08h

Description

0A: RDDPM (Read Display Power Mode).

This command indicates the current status of the display, as described in the table below.

Bit	Description	Value	Status
D7	Booster Voltage Status	0	Booster Off or has a fault.
		1	Booster On and working OK
D6	Idle Mode On/Off	0	Idle Mode Off
		1	Idle Mode On
D4	Sleep In/Out	0	Sleep In Mode
		1	Sleep Out Mode
D3	Display Normal Mode On/Off	0	Display Normal Mode Off
		1	Display Normal Mode On
D2	Display On/Off	0	Display is Off
		1	Display is On

Restriction

None

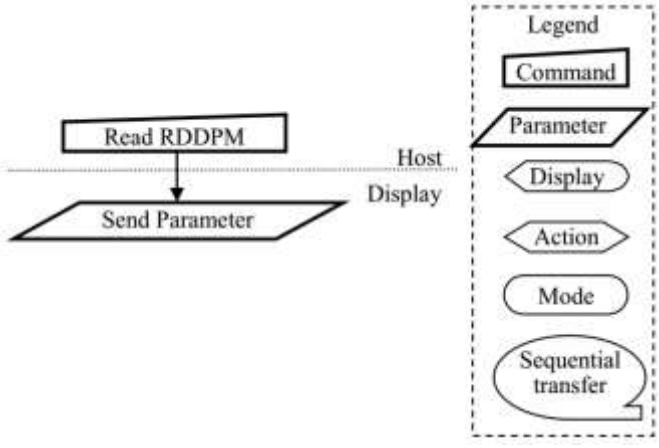
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



5.3.6. Read Display MADCTL (0Bh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Bh	1st	R	0	0	0	0	D3	0	D1	D0	00h

Description

0B: RDDMADCTL (Read Display MADCTL).

This command indicates the current status of the display, as described in the table below.

Bit	Description	Value	Status
D3	RGB/BGR Order (RGB)	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1')
D1	Source scan sequence (SS)	0	Source output Left to Right (When MADCTL D1 = '0')
		1	Source output Right to Left (When MADCTL D1 = '1')
D0	Gate scan sequence (GS)	0	Gate output Top to Bottom (When MADCTL D0 = '0')
		1	Gate output Bottom to Top (When MADCTL D0 = '1')

Note: For Bits D3, D1 and D0 also refer to 5.3.21Memory Access Control (36h).

Restriction

None

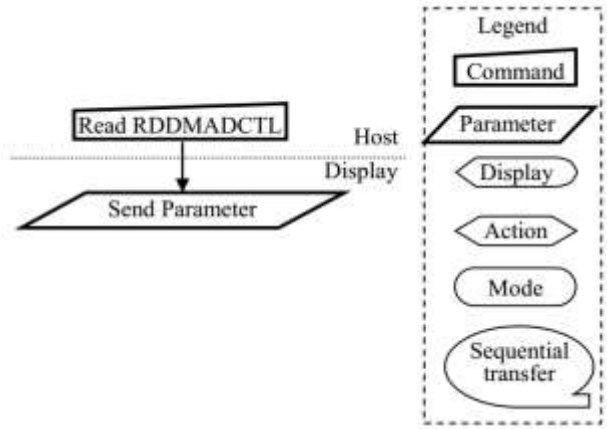
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.7. Read Display Pixel Format (0Ch)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Ch	1st	R	0	0	0	0	0	D[2:0]			07h

Description

0Ch: RDDCOLMOD (Read Display COLMOD).

This command indicates the current status of the display as described in the table below:

DBI[2:0]	Interface Pixel Format
101	16 bit/pixel
110	18 bit/pixel
111	24 bit/pixel
Others	Not defined

Note: For D[2:0] also refer to 5.3.24 Interface Pixel Format (3Ah).

Restriction

None

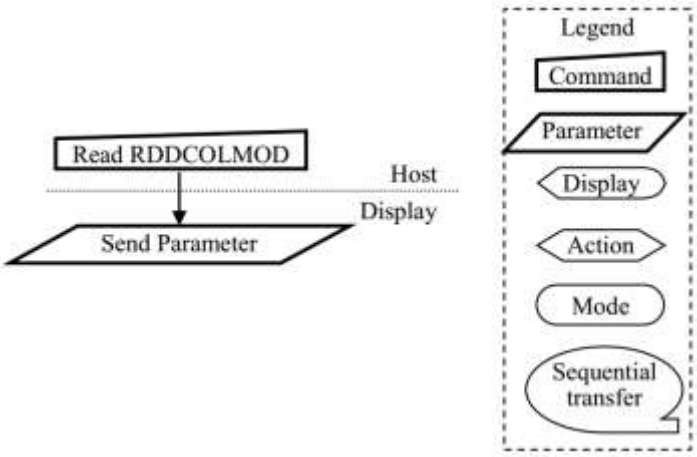
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



5.3.8. Read Display Image Mode (0Dh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Dh	1st	R	0	0	0	D4	D3	D[2:0]			00h

Description

0D: RDDIM (Read Display Image Mode).

This command indicates the Image Mode status of the display, as described in the Tables below:

Bit	Description	Value	Status
D4	All Pixels On	0	Normal Display
		1	White Display
D3	All Pixels Off	0	Normal Display
		1	Black Display

D[2:0]	Gamma Cure Selection
000	Gamma curve 1
Others	Not defined

Note: For D[2:0] also refer to "5.3.16 Gamma Set (26h)"

Restriction

None

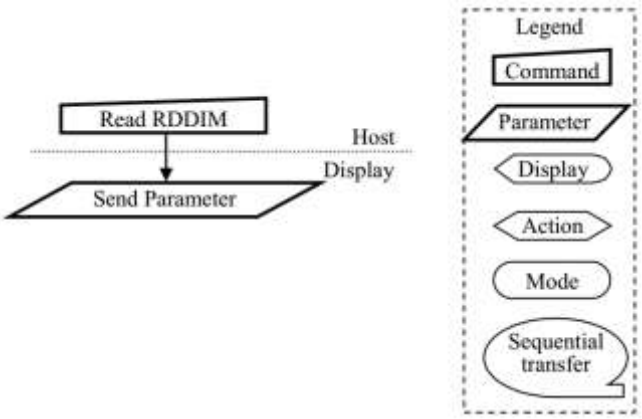
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

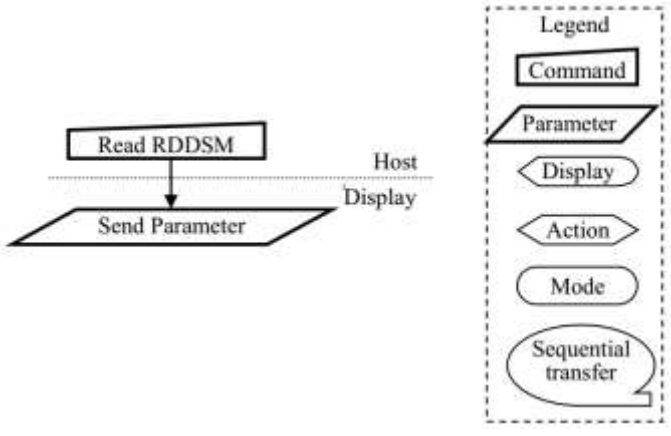
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.9. Read Display Signal Mode (0Eh)

<table>
<tr><th colspan="2">Command Page</th><th></th><th colspan="9">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>0Eh</td><td>1st</td><td>R</td><td>D7</td><td>D6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>D0</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="10">0E: RDDSM (Read Display Signal Mode).
This command indicates the current status of the display, as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D7</td><td rowspan="2">Tearing Effect Line On/Off</td><td>0</td><td>Tearing Effect Line Off</td></tr>
<tr><td>1</td><td>Tearing Effect On</td></tr>
<tr><td rowspan="2">D6</td><td rowspan="2">Tearing Effect Line Output Mode</td><td>0</td><td>Tearing Effect Line Mode 1</td></tr>
<tr><td>1</td><td>Tearing Effect Line Mode 2</td></tr>
</table>
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td rowspan="2">D0</td><td rowspan="2">Error on DSI</td><td>0</td><td>No Error on DSI</td></tr>
<tr><td>1</td><td>Error on DSI</td></tr>
</table>
See also sections: “4.1.3.2.2.2 Acknowledge with Error Report (AwER)” and “5.3.3 Read Number of the Errors on DSI (05h)”.
Note: For Bit D6, also refer to 5.3.20Tearing Effect Line On (35h).</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="10">None</td></tr>
<tr><td colspan="2">Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td colspan="2">Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td colspan="2">Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

5.3.10. Read Display Self-Diagnostic Result (0Fh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
0Fh	1st	R	D7	D6	0	0	0	0	0	D0	00h

Description

0F: RDDSDR (Read Display Self-Diagnostic Result).

This command indicates the status of the display self-diagnostic results after the Sleep Out command, as described in the table below:

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit when the EEPROM and register values are the same.
D6	Functionality Detection	Invert the D6 bit when the chip meets user's functionality requirements.
D0	Checksums Comparison	0 = Checksums are the same 1 = Checksums are not the same

Restriction

It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read Bit D0 value.

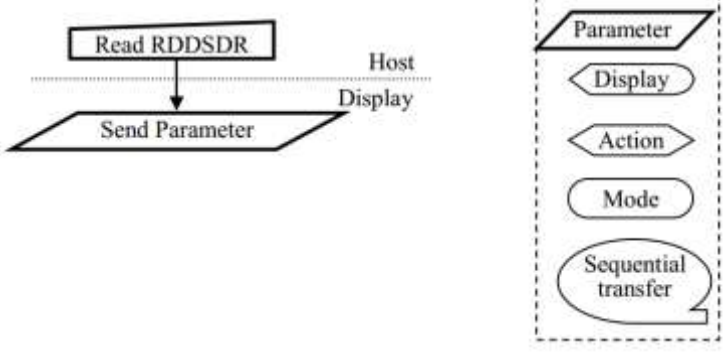
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.11. Sleep In (10h)

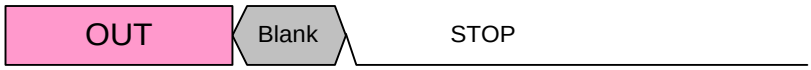
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
10h	-	W	No Argument								-

Description

10h: SLPIN (Sleep In).

This command causes the ILI9881C-05 to enter the minimum power consumption mode.

In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.



MCU interface and memory are still working and the memory can keep its contents.

Ambient light based control is off.

Backlights and display are off.

Dimming function does not work when there is changing mode from Sleep Out to Sleep In.

Restriction

This command has no effect when the module is already in the Sleep In mode. To leave the Sleep In Mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable. It is necessary to wait 120msec after sending the Sleep Out command (when in the Sleep In Mode) before the Sleep In command can be sent.

Register Availability

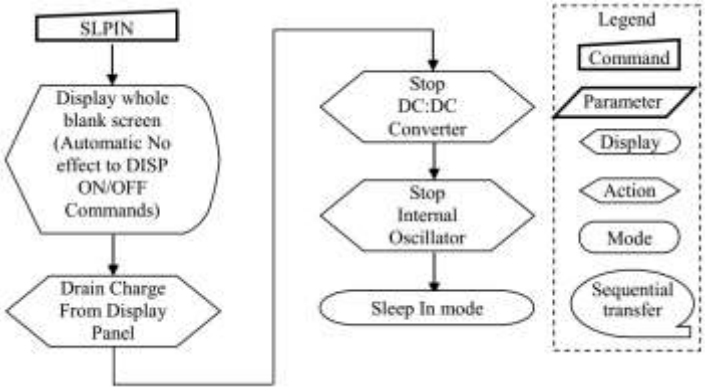
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

It takes 120msec to get into Sleep In mode after SLPIN command issued.



5.3.12. Sleep Out (11h)

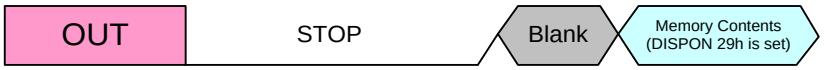
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
11h	-	W	No Argument								-

Description

11h: SLPOUT (Sleep Out).

This command turns off the sleep mode.

In this mode, the DC/DC converter is enabled, the Internal oscillator is started, and the panel scanning is started.



Restriction

This command has no effect when the module is already in the Sleep Out mode. To leave the Sleep Out mode, only the Sleep In command (10h), SW Reset Command (01h) or HW Reset are workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable.

The Driver IC loads all display supplier's factory default values to the registers during this 5msec. There cannot be any abnormal visual effect on the display image if factory default and register values are the same when this load is done and when the Driver IC is already in the Sleep Out mode. During this 5msec, the Driver IC also performs self-diagnostic functions.

It is necessary to wait 120msec after sending the Sleep In command (when in the Sleep Out mode) before the Sleep Out command can be sent.

Register Availability

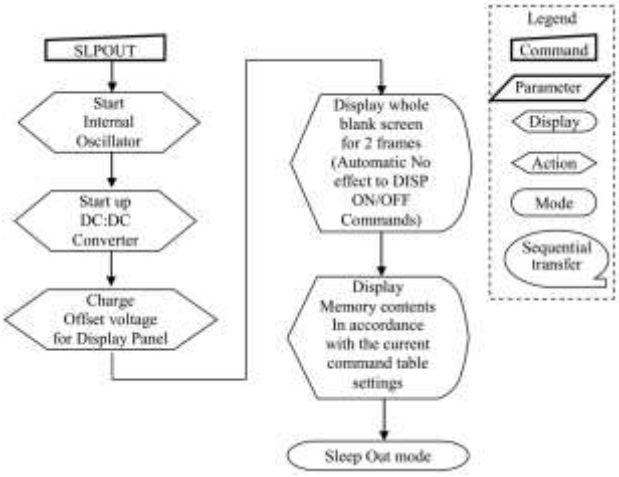
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In Mode
S/W Reset	Sleep In Mode
H/W Reset	Sleep In Mode

Flow Chart

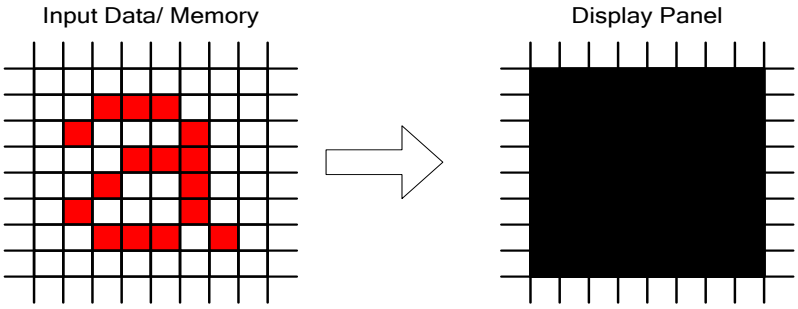
It takes 120msec to become Sleep Out mode after SLPOUT command issued.



5.3.13. Normal Display Mode On (13h)

<table>
<tr><th colspan="2">Command Page</th><th></th><th colspan="9">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>13h</td><td>-</td><td>W</td><td colspan="8">No Argument</td><td>-</td></tr>
<tr><td colspan="3">Description</td><td colspan="9">13h: NORON (Normal Display Mode On).
This command returns the display to normal mode.</td></tr>
<tr><td colspan="3">Restriction</td><td colspan="9">This command has no effect when the Normal Display Mode is active.</td></tr>
<tr><td colspan="3">Register Availability</td><td colspan="9"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td colspan="3">Default</td><td colspan="9"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On</td></tr></table></td></tr>
<tr><td colspan="3">Flow Chart</td><td colspan="9"></td></tr>
</table>

5.3.14. All Pixel Off (22h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
22h	-	W	No Argument								-
Description			22h: ALLPOFF (All Pixels Off). This command turns the display panel black in 'Sleep Out' mode and a status bit of the 'Read Display Image Mode' register (0Dh) can be read. This command makes no change of contents of the input data (or frame memory). This command does not change any other status.  'All Pixels On' or 'Normal Display Mode On' commands are used to leave this mode. When ILI9881C-05 works in 'Idle Mode On' and 'Sleep Out' state, the display panel is showing the content of the frame memory after 'Normal Display Mode On' commands.								
Restriction			This command has no effect when module is already in all pixels off mode.								

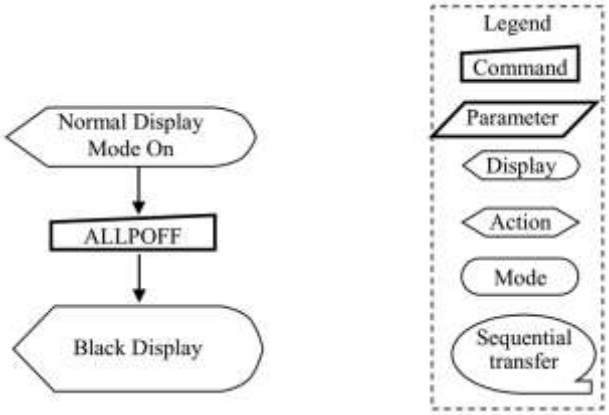
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

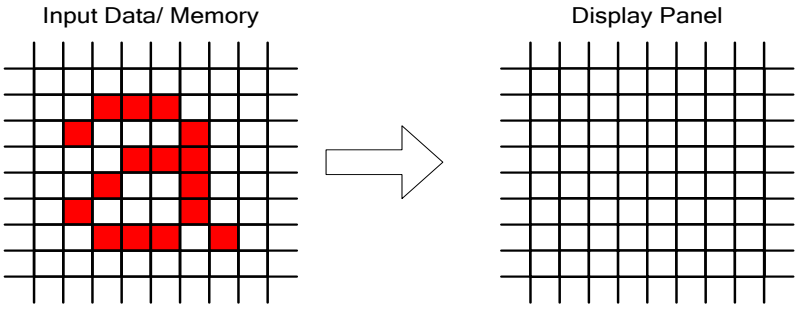
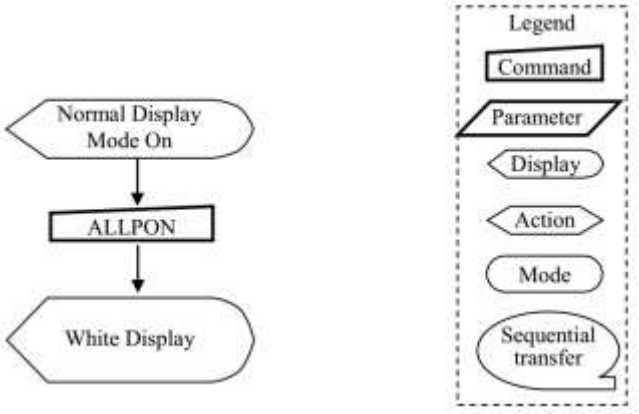
Default

Status	Default Value
Power On Sequence	OFF
S/W Reset	OFF
H/W Reset	OFF

Flow Chart



5.3.15. All Pixel On (23h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
23h	-	W	No Argument								-
Description		23h: ALLPON (All Pixels On). This command turns the display panel white in 'Sleep out' mode and a status bit of the 'Read Display Image Mode' register (0Dh) can be read. This command makes no change of contents of the input data (or frame memory). This command does not change any other status.  'All Pixels Off' or 'Normal Display Mode On' commands are used to leave this mode. When ILI9881C-05 works in 'Idle Mode On' and 'Sleep Out' state, the display panel is showing the content of the frame memory after 'Normal Display Mode On' commands.								
Restriction		This command has no effect when module is already in all pixels on mode.									
Register Availability		<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default		<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>S/W Reset</td><td>OFF</td></tr><tr><td>H/W Reset</td><td>OFF</td></tr></table>									
Flow Chart											

5.3.16. Gamma Set (26h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
26h	1st	W	0	0	0	0	GC [3:0]				01h

Description

26h: GAMSET (Gamma Set).

This command is used to select the desired Gamma curve for the current display. A maximum of 1 fixed Gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table below:

GC [3:0]	Curve Selected
1h	Gamma curve 1
Other	Reserved

Note: All others value are undefined.

Restriction

Values of GC [3:0] not shown in the table above are invalid and will not change the current selected Gamma curve until a valid value is received.

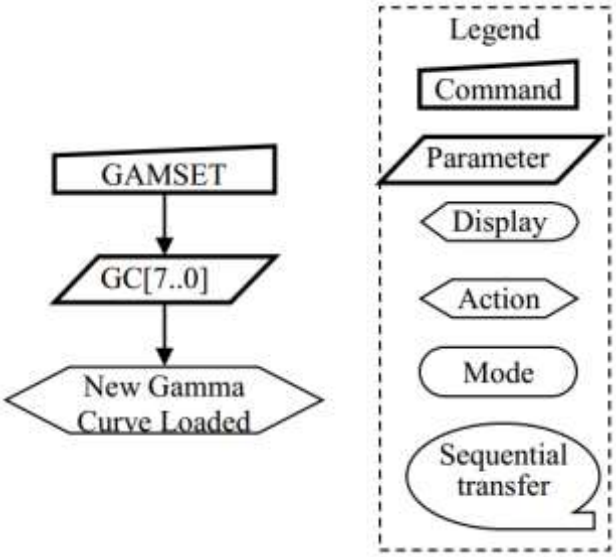
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

Flow Chart



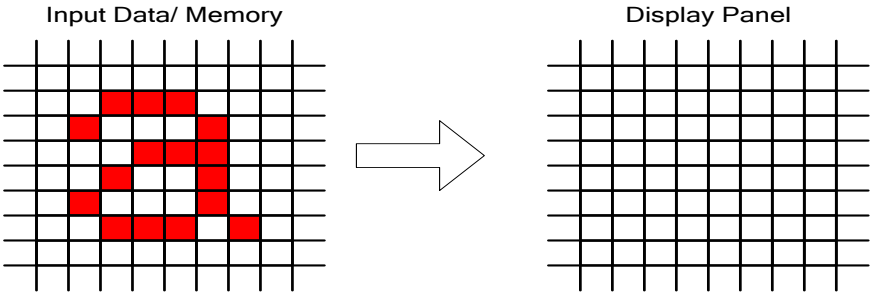
5.3.17. Display Off (28h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
28h	-	W	No Argument								-

Description

28h: DISPOFF (Display Off)

This command is used to enter into the Display Off mode. Output from the input data (or frame memory) is disabled and a blank page inserted. This command makes no change of contents of the input data (or frame memory) and does not change any other status. There will be no abnormal visible effect on the display.



Restriction

This command has no effect when the module is already in the Display Off mode.

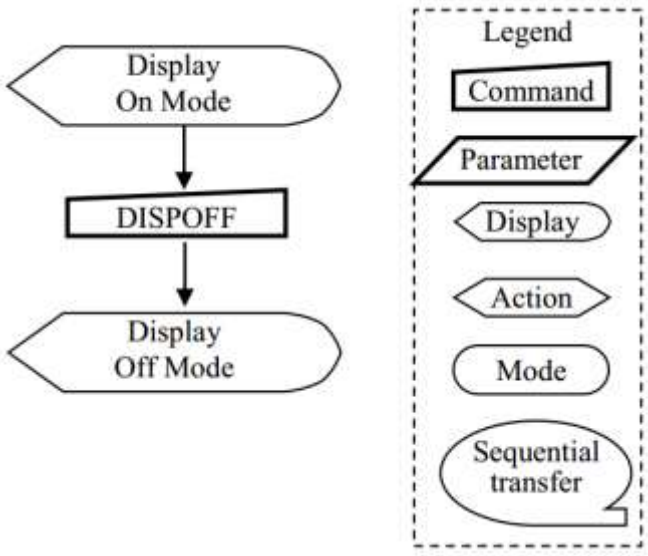
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



5.3.18. Display ON (29h)

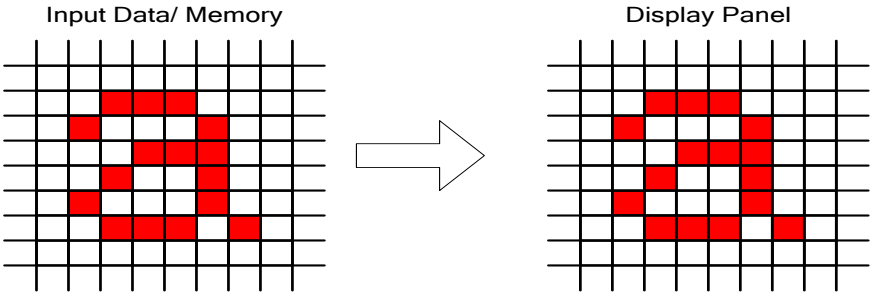
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
29h	-	W	No Argument								-

Description

29h: DISPON (Display On).

This command is used to recover from the Display Off mode. Output from the input data (or frame memory) is enabled.

This command makes no change of contents of the input data (or frame memory) and does not change any other status.



Restriction

This command has no effect when the ILI9881C-05 is already in the Display On mode.

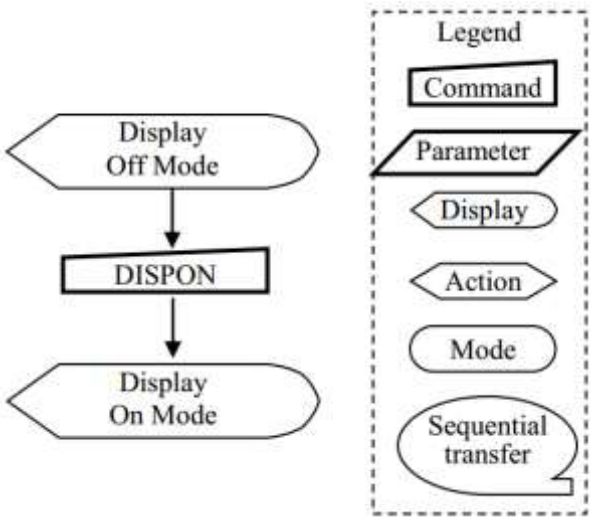
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



5.3.19. Tearing Effect Line Off (34h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
34h	-	W	No Argument								-
Description	34h: TEOFF (Tearing Effect Line OFF). This command is used to turn off the Display module's Tearing Effect output signal from the TE signal line.										
Restriction	This command has no effect when the Tearing Effect output is already off.										

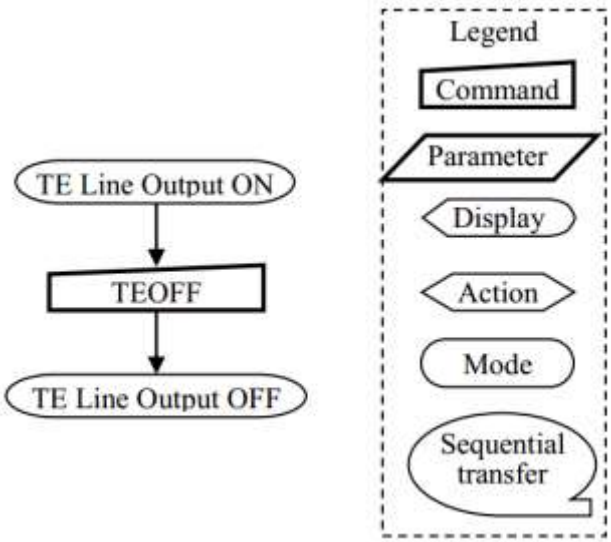
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



5.3.20. Tearing Effect Line On (35h)

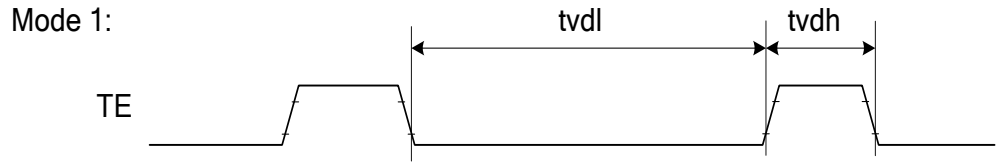
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
35h	1st	W	0	0	0	0	0	0	0	M	00

Description

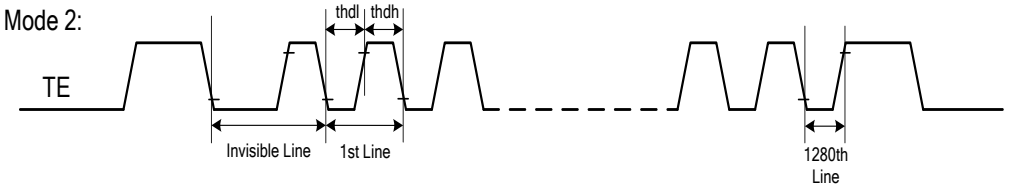
35h: TEON (Tearing Effect Line ON).

This command is used to turn on the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**: The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:



Note : The Tearing Effect Output line shall be low when the display module is in Sleep mode

Restriction

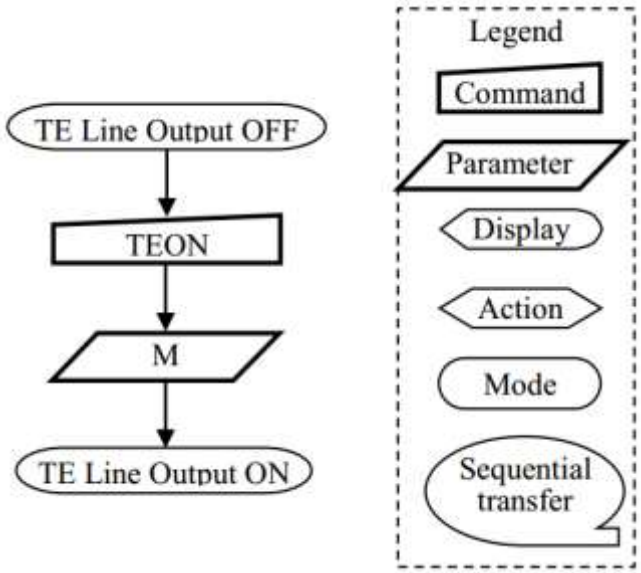
This command has no effect when the Tearing Effect output is already ON.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart	

5.3.21. Memory Access Control (36h)

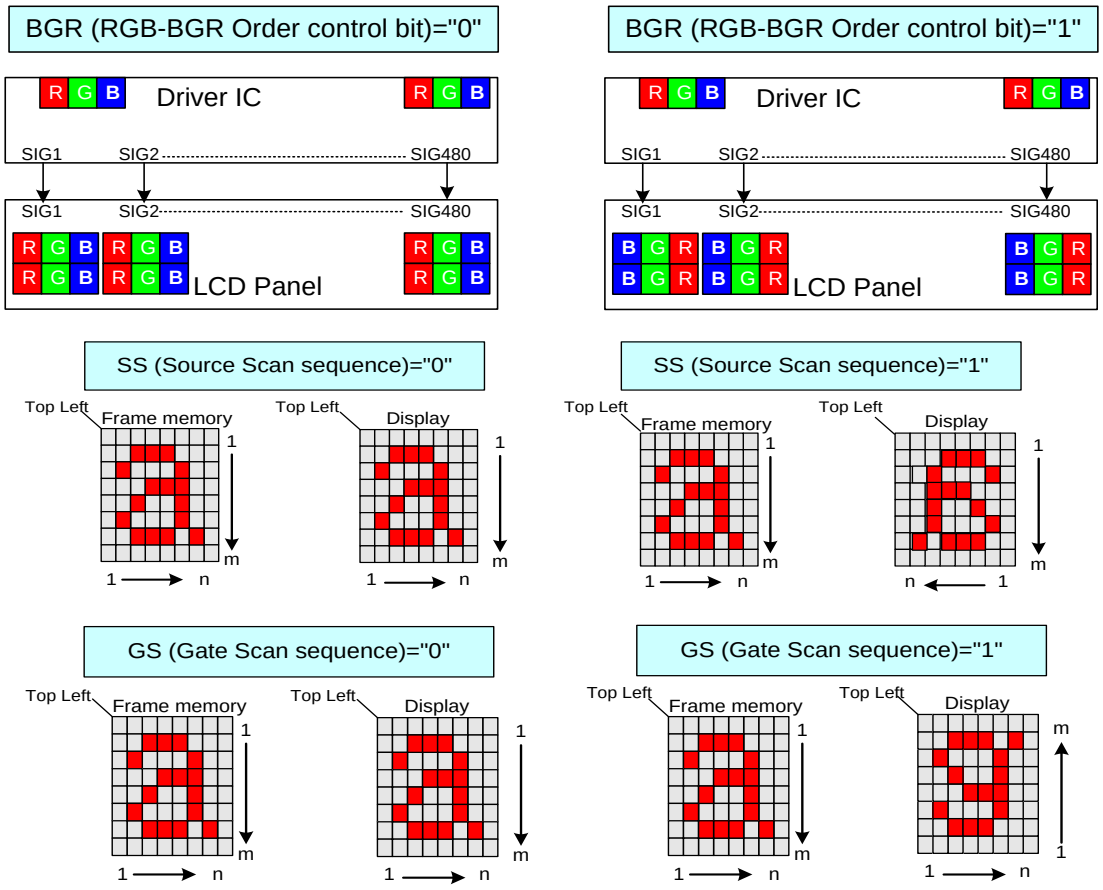
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
36h	1st	W	0	0	0	0	BGR	0	SS	GS	00h

Description

36h: MADCTL (Memory Access Control).

This command makes no change on the other status of the driver.

Bit	Symbol	Name	Description
D3	BGR	RGB/BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
D1	SS	Flip Horizontal (SS)	Select the Source driver scan direction on the panel module
D0	GS	Flip Vertical (GS)	Select the Gate driver scan direction on the panel module



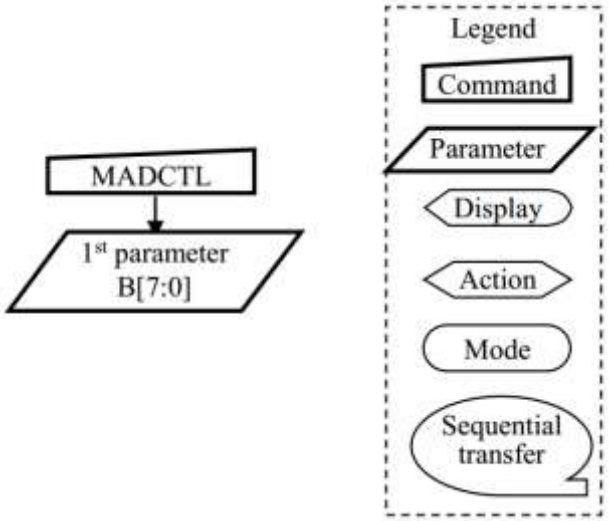
Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart	

5.3.22. Idle Mode Off (38h)

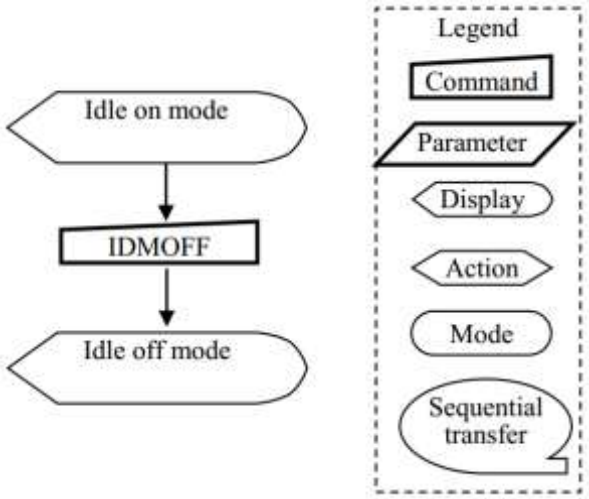
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
38h	-	W	No Argument								-
Description	38h: IDMOFF (Idle mode off). This command causes the Display module to exit the Idle mode. In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.										
Restriction	This command has no effect when the module is already in the Idle Mode Off.										
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



5.3.23. Idle Mode On (39h)

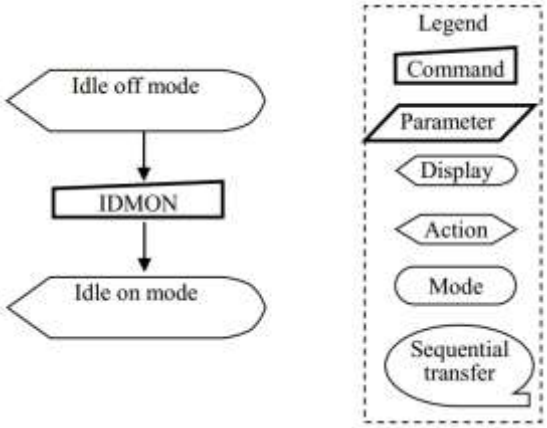
Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
39h	-	W	No Argument								-
Description	39h: IDMON (Idle mode on). This command is used to enter into the Idle Mode On. In the Idle Mode On, color expression is reduced. The display panel shows de-compressed content of frame memory in the Idle Mode On and Sleep Out states.										
Restriction	This command has no effect when the module is already in the Idle Mode On.										
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



5.3.24. Interface Pixel Format (3Ah)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
3Ah	1st	W	0	0	0	0	0	DBI[2:0]			07h

Description

3A: COLMOD (Interface Pixel Format).

This command is used to define the format of RGB picture data, which is to be transferred via the MIPI DSI Command Mode. The formats are shown in the table:

Interface Format	DBI[2:0]
Not Defined	000
Not Defined	001
Not Defined	010
Not Defined	011
Not Defined	100
16 bit/pixel	101
18 bit/pixel	110
24 bit/pixel	111

Restriction

There is no visible effect until the Frame Memory is written to.

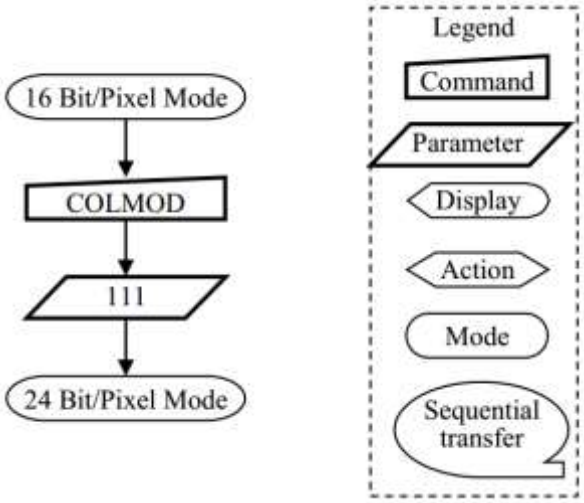
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

Flow Chart



5.3.25. Set_Tear_Scanline (44h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
44h	1st	W	0	0	0	0	0	TE_LINE[10:8]			00h
	2nd	W	TE_LINE[7:0]								00h

Description

44h: SET_TEAR_SCANLINE.

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N.

The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. After issuing a set_tear_scanline command to the display module, the Tearing Effect output signal, e.g. as in DBI-2 systems, shall be a delayed version of V-Blanking information as illustrated by below figure.

In other words, the TE pulse width needs to be identical with normal mode Vsync related TE pulse.

Note that set_tear_scanline with N = 0 is equivalent to set_tear_on with M = 0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

This command takes affect on the frame following the current frame.

Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous set_tear_on, or set_tear_scanline, command until the end of the frame.

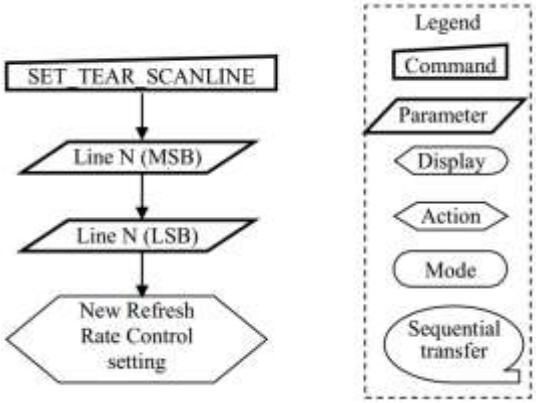
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	No

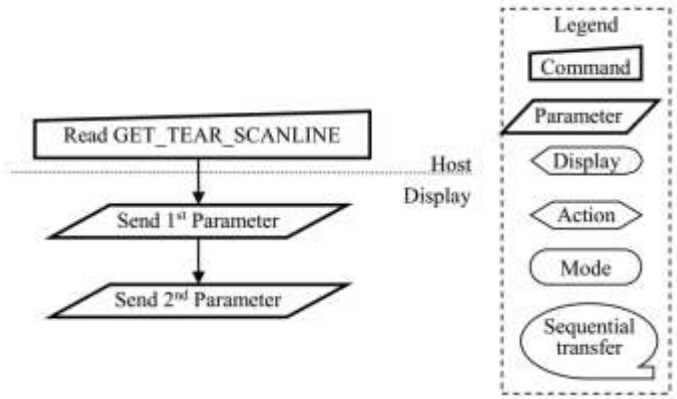
Default

Status	Default Value
Power On Sequence	N=0
S/W Reset	N=0
H/W Reset	N=0

Flow Chart



5.3.26. Get_Tear_Scanline (45h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
45h	1st	R	0	0	0	0	0	TE_LINE[10:8]			00h
	2nd	R	TE_LINE[7:0]								00h
Description			45h: GET_TEAR_SCANLINE. This command returns setting value of Set_Tear_Scanline command (44h).								
Restriction			None								
Register Availability			Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: No								
Default			Status: Power On Sequence — Default Value: N=0 Status: S/W Reset — Default Value: N=0 Status: H/W Reset — Default Value: N=0								
Flow Chart											

5.3.27. Write Display Brightness Value (51h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
51h	1st	W	0	0	0	0	DBV[11:8]				00h
	2nd	W	DBV[7:0]								00h
Description		51h: WRDISBV (Write Display Brightness). This command is used to adjust the brightness value of the display. DBV[11:0]: 12 bit, for display brightness of manual brightness setting and the CABC in the ILI9881C-05. PWM output signal and LEDPWM pin will control the LED driver IC in order to control the display brightness. In principle relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.									
Restriction		None									

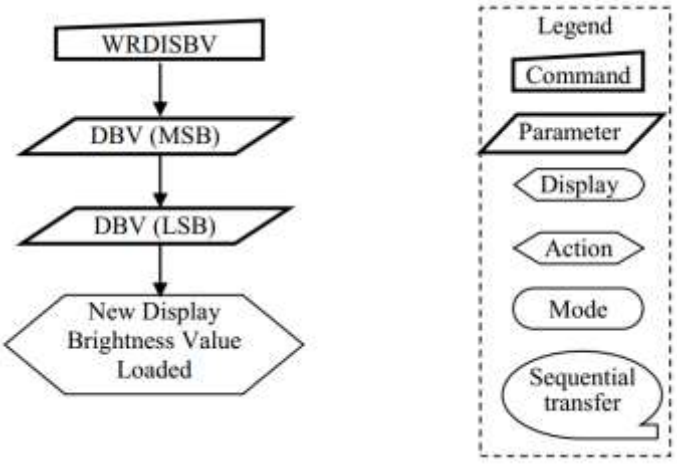
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

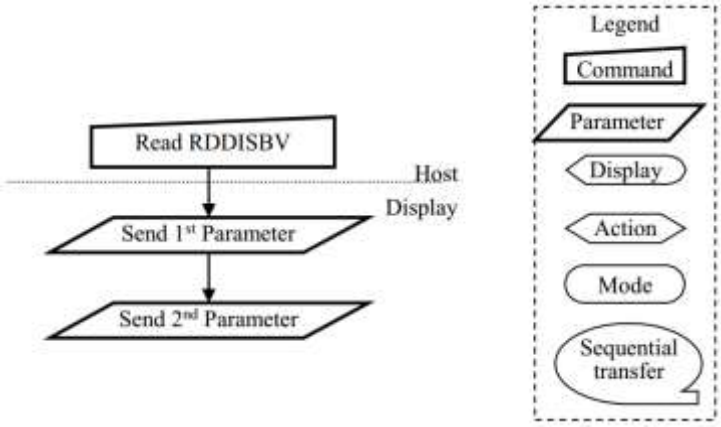
Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.3.28. Read Display Brightness Value (52h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
52h	1st	R	0	0	0	0	DBV[11:8]				00h
	2nd	R	DBV[7:0]								00h
Description		52h: RDDISBV (Read Display Brightness Value). This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness. DBV[11:0] is reset when display is in sleep-in mode. DBV[11:0] is '0' when bit BCTRL of "5.3.29Write CTRL Display Value (53h)" command is '0'. DBV[11:0] is manual set brightness specified with "5.3.29Write CTRL Display Value (53h)" command when bit BCTRL is '1'.									
Restriction		None									
Register Availability		<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>									
Default		<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h_00h</td></tr><tr><td>S/W Reset</td><td>00h_00h</td></tr><tr><td>H/W Reset</td><td>00h_00h</td></tr></table>									
Flow Chart											

5.3.29. Write CTRL Display Value (53h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
53h	1st	W	0	0	BCTRL	0	DD	BL	0	0	00h

Description

53h: WRCTRLD (Write Control Display).

This command is used to control the display brightness.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block Off (DBV[11:0] = 0000h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0.

When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.

Restriction

None

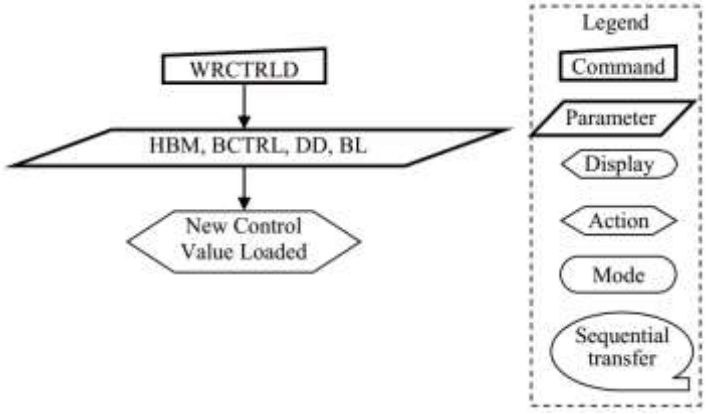
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.30. Read CTRL Display Value (54h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
54h	1st	R	0	0	BCTRL	0	DD	BL	0	0	00h

Description

54h: RDCTRLD (Read Control Value Display).

This command returns the display brightness control values.

BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block Off (DBV[11:0] = 0000h)
1	Brightness Control Block On (DBV[11:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming Off
1	Display Dimming On

BL: Backlight Control On/Off

BL	Description
0	Backlight Control Off
1	Backlight Control On

Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0.

When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.

Restriction

None

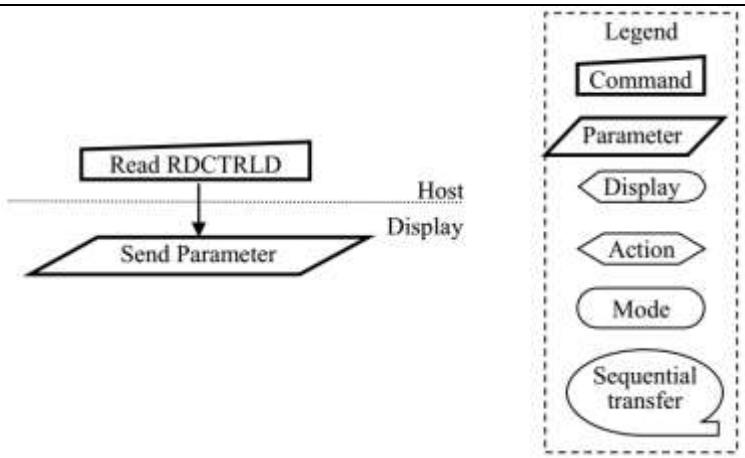
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.31. Write Power Save (55h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
55h	1st	W	PWRSAVE[7:0]								00h

Description

55h: PWRSAVE (Write Power Save).

This command is used to write the settings for power save control functionalities.

PWRSAVE[7:0]	Function	Note
00000000	Power Save Off	-
00000001	Power Save Low	Conservative Setting of CABC/DBLC
00000010	Power Save Medium	Medium Setting of CABC/DBLC
00000011	Power Save High	Aggressive Setting of CABC/DBLC
1000XXXX	IE On – Low	Low Enhancement of LCD
1001XXXX	IE On – Medium	Medium Enhancement of LCD
1011XXXX	IE On – High	High Enhancement of LCD
0100XXXX	SRE - Low	Sunlight readability enhancement
0101XXXX	SRE - Medium	Sunlight readability enhancement
0110XXXX	SRE - High	Sunlight readability enhancement
Others	Reserved	-

CABC = Content Adaptive Brightness Control

DBLC = Dynamic Backlight Control

IE = Image Enhancement

Restriction

None

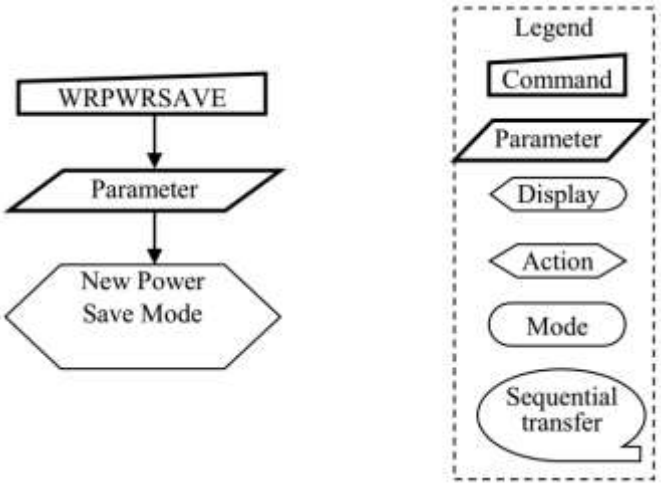
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.32. Read Power Save (56h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
56h	1st	R	PWRSAVE[7:0]								00h

Description

56h: RDPWRSAVE (Read Power Save).

This command is used to read the settings for power save control functionalities.

PWRSAVE[7:0]	Function	Note
00000000	Power Save Off	-
00000001	Power Save Low	Conservative Setting of CABC/DBLC
00000010	Power Save Medium	Medium Setting of CABC/DBLC
00000011	Power Save High	Aggressive Setting of CABC/DBLC
1000XXXX	IE On – Low	Low Enhancement of LCD
1001XXXX	IE On – Medium	Medium Enhancement of LCD
1011XXXX	IE On – High	High Enhancement of LCD
0100XXXX	SRE - Low	Sunlight readability enhancement
0101XXXX	SRE - Medium	Sunlight readability enhancement
0110XXXX	SRE - High	Sunlight readability enhancement
Others	Reserved	-

CABC = Content Adaptive Brightness Control

DBLC = Dynamic Backlight Control

IE = Image Enhancement

Restriction

None

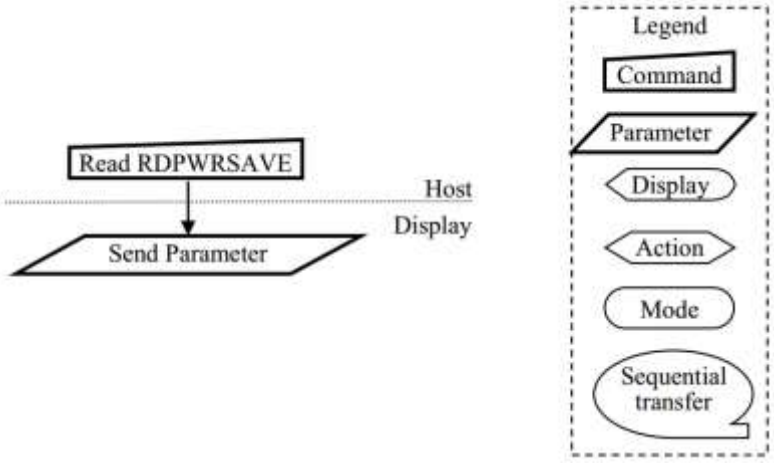
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.33. Stop Transition (59h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
59h	-	W	No Argument								-
Description	59h: STOP_TR (Stop Transition). When DD bit status of "5.3.29Write CTRL Display Value (53h)" register is '1', applying this command instantly stops the ongoing transition of Display Dimming. When display module receives this command, the current output value stays active.										
Restriction	This command has no effect when Display Dimming transition is not active.										

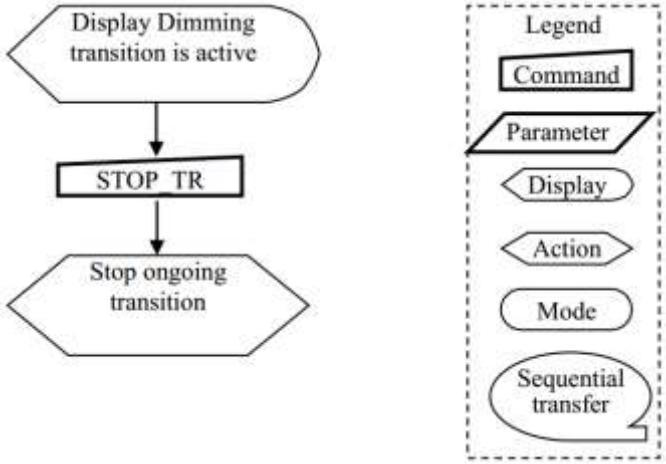
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Off
S/W Reset	Off
H/W Reset	Off

Flow Chart



5.3.34. Write CABC Minimum Brightness (5Eh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Eh	1st	W	0	0	0	0	CMB[11:8]				00h
	2nd	W	CMB[7:0]								00h
Description	5Eh: WRCABCMB (Write CABC minimum brightness). This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 0000h value means the lowest brightness for CABC and 0FFFh value means the highest brightness for CABC.										
Restriction	None										

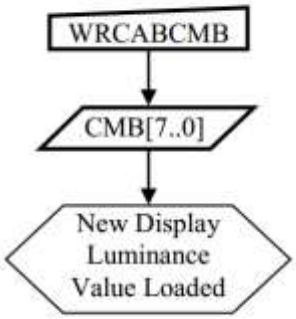
Register Availability

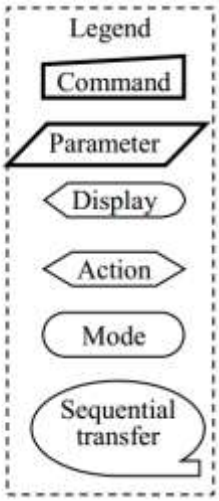
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart





5.3.35. Read CABC Minimum Brightness (5Fh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Fh	1st	R	0	0	0	0	CMB[11:8]				00h
	2nd	R	CMB[7:0]								00h
Description	5Fh: RDCABCMB (Read CABC Minimum Brightness). This command returns the minimum brightness value of CABC function. In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness. CMB[11:0] is CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command.										
Restriction	None										

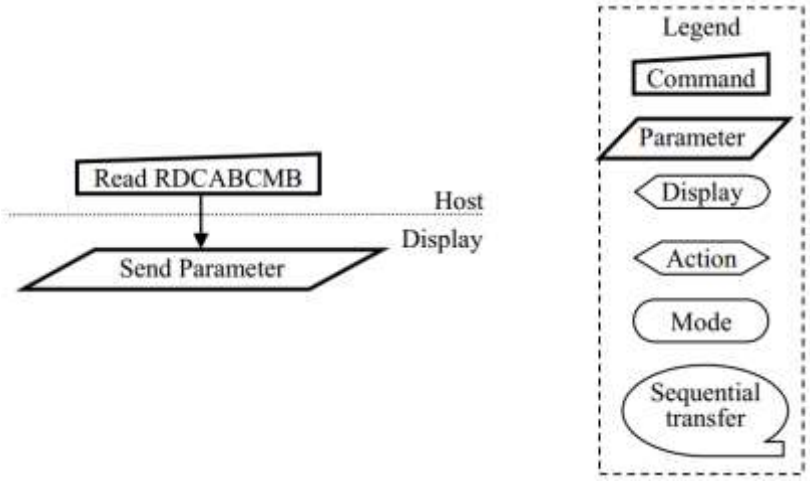
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

Flow Chart



5.3.36. Set Transition Time (68h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
68h	1st	W	TT_STP[7:0]								00h
	2nd	W	ST_TIM[7:0]								00h

Description

68h: SET_TT (Set Transition Time).

This command controls the total transition time of Display Dimming function.

Transition time is adjusted with two parameters, defining as follows:

1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.

TT_STP [7:0]	Description
00h	1 step
01h	2 step
02h	4 step
03h	8 step
04h	16 step
05h	32 step
06h	64 step
07h	128 step
08h	256 step
09h	512 step
0Ah	1024 step
0Bh	2048 step
0Ch	4096 step
Others	Reserved

2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.

ST_TIM [7:0]	Description
00h	1 frame
01h	1 frame
02h	2 frame
03h	3 frame
04h	4 frame
05h	5 frame
:	:
:	:
FBh	251 frame
FCh	252 frame
FDh	253 frame
FEh	254 frame
FFh	255 frame

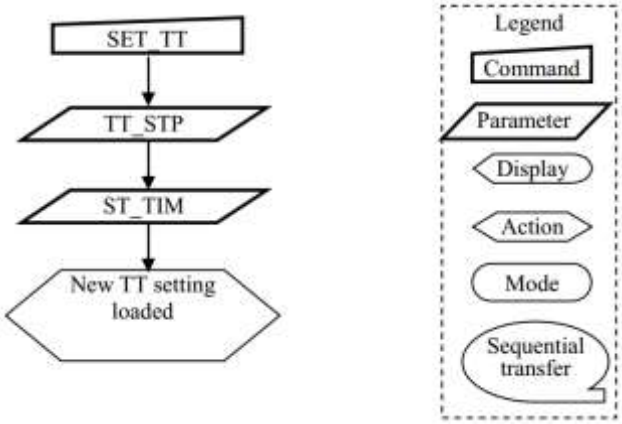
Thereby, total transition time for dimming can be calculated as follows:

TT_STP [7:0] * ST_TIM [7:0] = TT, where TT unit is frame. Value 0000h means the transition is instant

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

5.3.37. Get Transition Time (69h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
69h	1st	R	TT_STP[7:0]								00h
	2nd	R	ST_TIM[7:0]								00h

Description

69h: GET_TT (Get Transition Time Value).

This readout returns the Transition Time value of Display Dimming function, described in section “5.3.36Set Transition Time (68h)”.

Transition time is adjusted with two parameters, defining as follows:

1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.

TT_STP [7:0]	Description
00h	1 step
01h	2 step
02h	4 step
03h	8 step
04h	16 step
05h	32 step
06h	64 step
07h	128 step
08h	256 step
09h	512 step
0Ah	1024 step
0Bh	2048 step
0Ch	4096 step
Others	Reserved

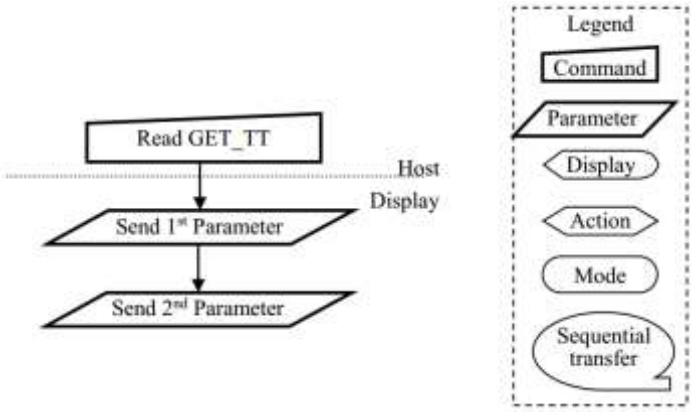
2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.

ST_TIM [7:0]	Description
00h	1 frame
01h	1 frame
02h	2 frame
03h	3 frame
04h	4 frame
05h	5 frame
:	:
:	:
FBh	251 frame
FCh	252 frame
FDh	253 frame
FEh	254 frame
FFh	255 frame

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

5.3.38. Read DDB Start (A1h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A1h	1st	R	SID[7:0]								0000h
	2nd	R	SID[15:8]								
	3rd	R	MRID[7:0]								0000h
	4th	R	MRID[15:8]								
	5th	R	SID2[7:0]								0000h
	6th	R	SID2[15:8]								
	7th	R	1	1	1	1	1	1	1	1	FFh

Description

A1h: RDDDBS (Read DDB Start).

This command reads the supplier identification and display module mode/revision information.

Note: This information is not the same as which "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands return.

Parameter 1: SID[7:0] LCD module's manufacturer ID.

Parameter 2: SID[15:8] LCD module/driver version ID.

Parameter 3: MRID[7:0] LCD module/driver ID.

Parameter 4: MRID[15:8] IC version code.

Parameter 5: SID2[7:0]

Parameter 6: SID2[15:8]

Parameter 7: FFh - Exit code – there is no more data in the Descriptor Block

This read sequence can be interrupted by any command and it can be continued by the Read DDB Continue (A8h) command. For example, RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.

Note: Maximum DDB data length is 4 bytes with OTP program.

Restriction

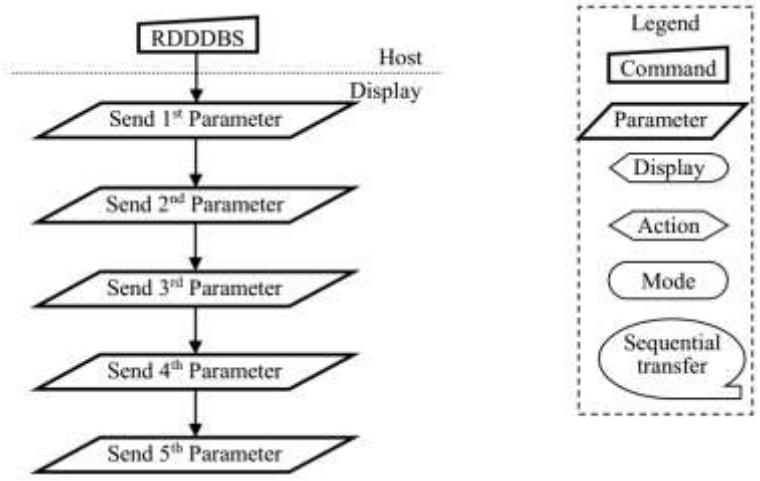
None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h_00h_00h_00h_FFh
S/W Reset	00h_00h_00h_00h_00h_00h_FFh
H/W Reset	00h_00h_00h_00h_00h_00h_FFh

Flow Chart	

5.3.39. Read DDB Continue (A8h)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A8h	1st	R	D1[7:0]								00h
	2nd	R	D2[7:0]								00h
	:	R	:								00h
	Nth	R	Dn[7:0]								00h
Description			A8h: RDDDBC (Read DDB Continue). This command is used to read the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command								
Restriction			None								

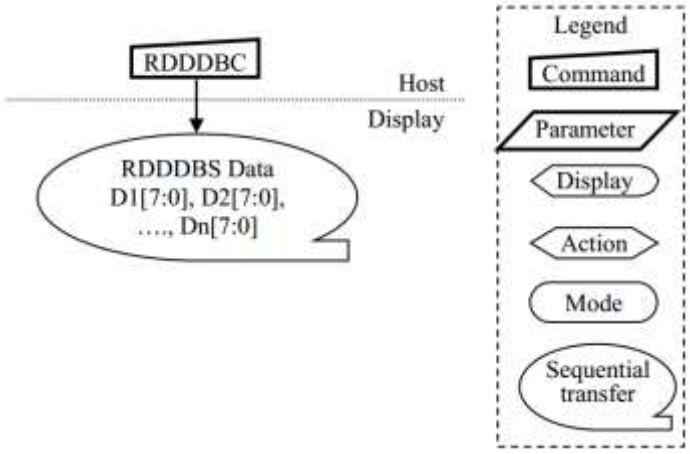
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.40. Read First Checksum (AAh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AAh	1st	R	FCS[7:0]								00h
Description	AAh: RDFCS (Read First Checksum). This command returns the first checksum what has been calculated from Page 0 area registers after the write access to those registers has been done.										
Restriction	It will be necessary to wait 150ms after there is the last write access on Page 0 area registers before there can read this checksum value.										

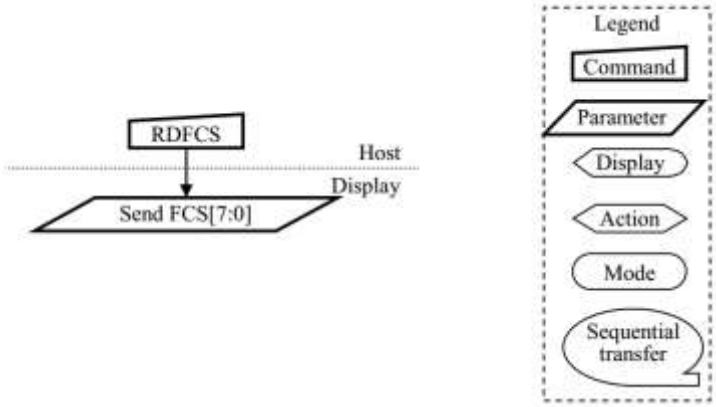
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.41. Read Continue Checksum (AFh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
AFh	1st	R	CCS[7:0]								00h
Description	AFh: RDCCS (Read Continue Checksum). This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from Page 0 area registers after the write access to those registers has been done.										
Restriction	It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read this checksum value in the first time.										

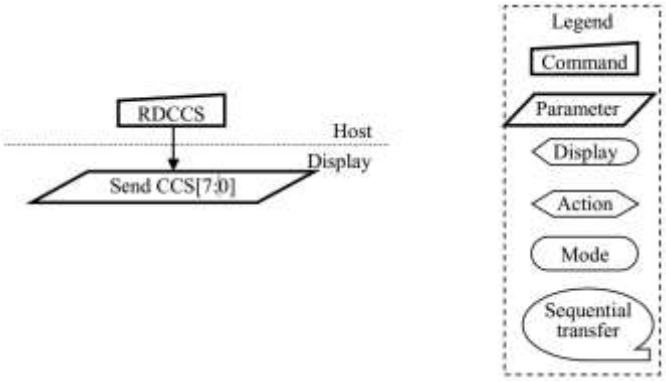
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.42. Read ID1 (DAh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
DAh	1st	R	ID1[7:0]								00h
Description		Dah: RDID1 (Read ID1). This read byte identifies the display module's manufacturer. The ID1[7:0] is programmed by the OTP function.									
Restriction		None									

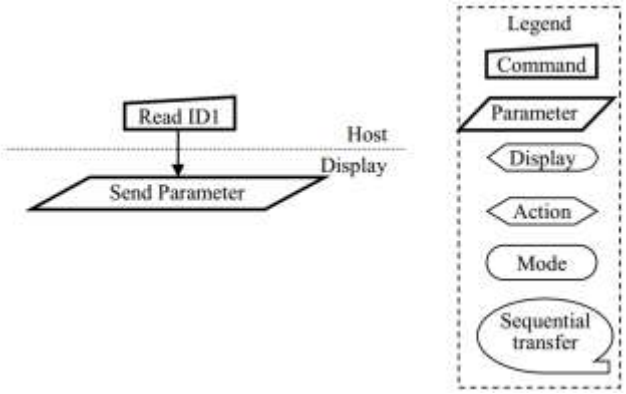
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

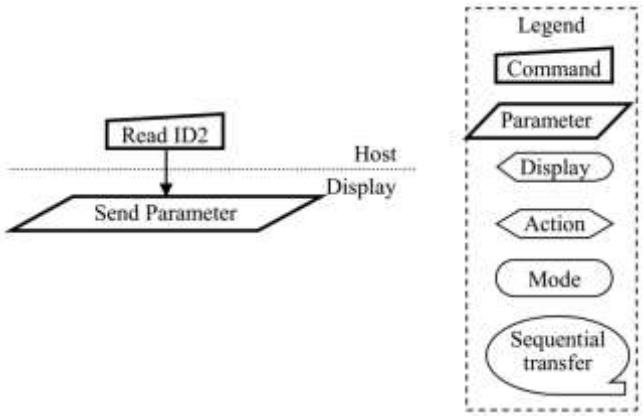
Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.43. Read ID2 (DBh)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 0</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>DBh</td><td>1st</td><td>R</td><td colspan="8">ID2[7:0]</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="10">DBh: RDID2 (Read ID2).
This read byte is used to track the display module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.
The ID2[7:0] is programmed by the OTP function.</td></tr>
<tr><td colspan="2">Restriction</td><td colspan="10">None</td></tr>
<tr><td colspan="2">Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td colspan="2">Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>00h</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
<tr><td colspan="2">Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

5.3.44. Read ID3 (DCh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
DCh	1st	R	ID3[7:0]								00h
Description		DCh: RDID3 (Read ID3). This read byte identifies the display module/driver. The ID3[7:0] is programmed by the OTP function.									
Restriction		None									

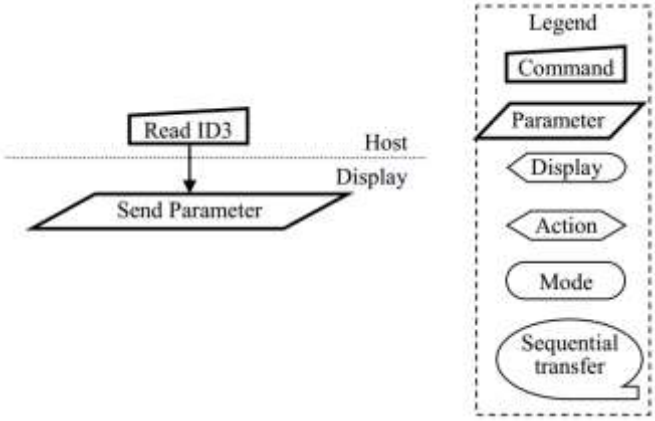
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



5.3.45. EXTC Command Set Enable Register (FFh)

Command Page			Page 0								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								00h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

5.4. Page 1 Command Description

5.4.1. Read ID4 (00h~02h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
00h	1st	R	ID4[23:16]								98h
01h	1st	R	ID4[15:8]								81h
02h	1st	R	ID4[7:0]								5Ch
Description		**ID4[23:0] :** mean the IC model name.									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	98h_81h_5Ch
S/W Reset	98h_81h_5Ch
H/W Reset	98h_81h_5Ch

5.4.2. Set Panel Operation Mode and Data Complement Setting (22h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 1</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th colspan="2">D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>22h</td><td>1st</td><td>W/R</td><td>0</td><td>0</td><td colspan="2">EPF[1:0]</td><td></td><td>BGR_PANEL</td><td>REV_PANEL</td><td>SS_PANEL</td><td>GS_PANEL</td><td>30h</td></tr>
<tr><td>Description</td><td colspan="12">
This command defines the panel operation mode

EPF[1:0]: Set the data format from 16/18-bit (R,G,B) to 24-bit (r, g, b) that is mapping into the internal circuit.

See section “4.2.2 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation” for detail description.

BGR_PANEL:
<table>
<tr><th>Symbol</th><th>Name</th><th>Description</th></tr>
<tr><td>BGR_PANEL</td><td>Panel RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr>
</table>
REV_ PANEL: Normally white or normally black panel select.
<table>
<tr><th>REV_PANEL</th><th>Panel</th><th>Data</th><th>Color</th><th>Source</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">Normally black</td><td>0x00</td><td>Black</td><td>Smallest gamma voltage</td></tr>
<tr><td>0xFF</td><td>White</td><td>Largest gamma voltage</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">normally white</td><td>0x00</td><td>Black</td><td>Largest gamma voltage</td></tr>
<tr><td>0xFF</td><td>White</td><td>Smallest gamma voltage</td></tr>
</table>
SS_ PANEL: Select the shift direction of outputs from the source driver.
<table>
<tr><th>SS_PANEL</th><th>Source Output Scan Direction</th></tr>
<tr><td>0</td><td>Forward</td></tr>
<tr><td>1</td><td>Backward</td></tr>
</table>
GS_ PANEL: Select the shift direction of outputs from the gate driver.
<table>
<tr><th>GS_PANEL</th><th>Gate Output Scan Direction</th></tr>
<tr><td>0</td><td>Top → Bottom</td></tr>
<tr><td>1</td><td>Bottom → Top</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value
(Before OTP program)</th></tr>
<tr><td>Power On Sequence</td><td>30h</td></tr>
<tr><td>S/W Reset</td><td>30h</td></tr>
<tr><td>H/W Reset</td><td>30h</td></tr>
</table>
</td></tr>
</table>

5.4.3. Blanking Porch Control (25h~26h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
25h	1st	W/R	VFP[7:0]								14h
26h	1st	W/R	VBP[7:0]								14h

Description

VFP[7:0] / VBP[7:0]: The VFP[7:0] and VBP[7:0] bits specify the line number of vertical front and back porch period respectively in the non-Video Mode.

VFP[7:0] VBP[7:0]	Number of HSYNC of front/back porch (Dec.)
00000000	Setting prohibited
00000001	Setting prohibited
00000010	2
00000011	3
:	:
00001110	14 (VFP[7:0] /VBP[7:0] default)
:	:
11111101	253
11111110	254
11111111	255

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	14h_14h
S/W Reset	14h_14h
H/W Reset	14h_14h

5.4.4. Touch Synchronization Control (29h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
29h	1st	W/R	0	0	0	0	0	0	0	TOUCH_ VHSYNC	00h
Description		**TOUCH_VHSYNC:** Enable VSOUT / HSOUT signal output.									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

5.4.5. Gate Number (2Eh)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Eh	1st	W/R	NL[7:0]								C8h

Description

NL[7:0]: Set the number of lines.

NL[7:0]	NL Output
00h	0
01h	1
02h	2
03h	3
:	:
FCh	252
FDh	253
FEh	254
FFh	255

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C8h
S/W Reset	C8h
H/W Reset	C8h

5.4.6. Gate Number (2Fh)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Fh	1st	W/R	Add_1024	0	0	0	0	0	0	Add_two	00h

Description

Set the gate line number of LCD follow below formula.

Add_1024: The line number add 1024

Add_two: The line number add two

Add_1024	Add_two	The Gate Line Number of the LCD
0	0	4NL+480
0	1	4NL+480+2
1	0	4NL+480+1024
1	1	4NL+480+1024+2

Example:

1,) NL set to “C8h”, Add_1024 set to “0h” & Add_two set to “0h” then, The Line Number for the LCD is 1280。(4*200+480 = 1280)

2,) NL set to “F0h”, Add_1024 set to “0h” & Add_two set to “0h” then, The Line Number for the LCD is 1440。(4*240+480 = 1440)

3,) NL set to “04h”, Add_1024 set to “1h” & Add_two set to “0h” then, The Line Number for the LCD is 1520。(4*4+480+1024 = 1520)

4,) NL set to “0Eh”, Add_1024 set to “1h” & Add_two set to “0h” then, The Line Number for the LCD is 1560。(4*14+480+1024 = 1560)

5,) The Maximum of Gate Line is 1600, NL set to “18h”, Add_1024 set to “1h” & Add_two set to “0h” then, The Line Number for the LCD is 1600。(4*24+480+1024 = 1600)

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Display Inversion Control (31h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
31h	1st	W/R	0	0	0	0	DINV[3:0]				00h

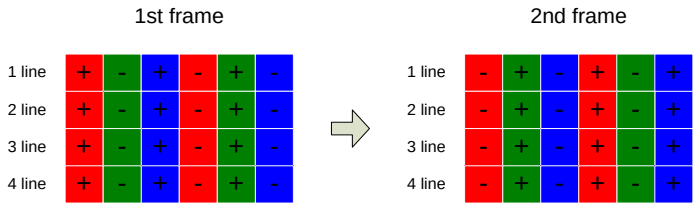
Description

DINV[3:0]: Set Inversion mode

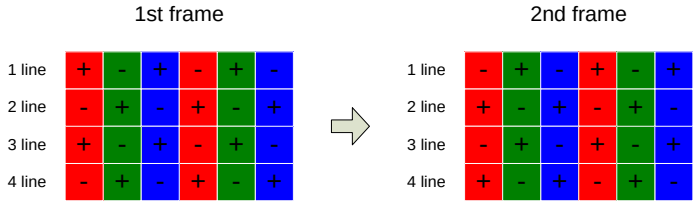
DINV[3:0]	Inversion
0h	Column inversion
1h	1-dot inversion
2h	2-dot inversion
3h	3-dot inversion
4h	4-dot inversion
5h	N/4-dot inversion Note
6h	N/8-dot inversion Note
7h	N/16-dot inversion Note
8h	N/32-dot inversion Note
9h	Zig-Zag inversion Type 1
Ah	Zig-Zag inversion Type 2
Bh	Zig-Zag inversion Type 3
Ch	Zig-Zag inversion Type 4
Others	Reserved

Note : N=The line number of the LCD (setting by NL[7:0])

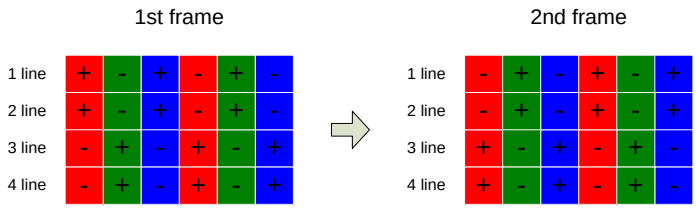
Column Inversion



1-Dot Inversion



2-Dot Inversion



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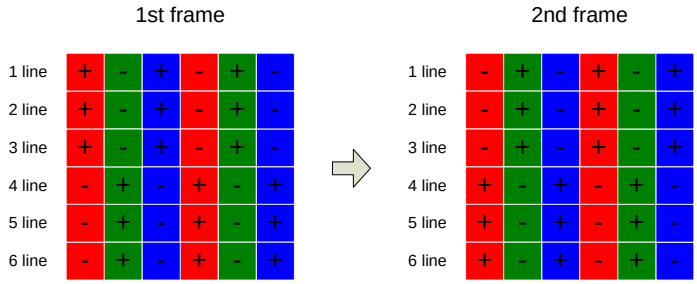
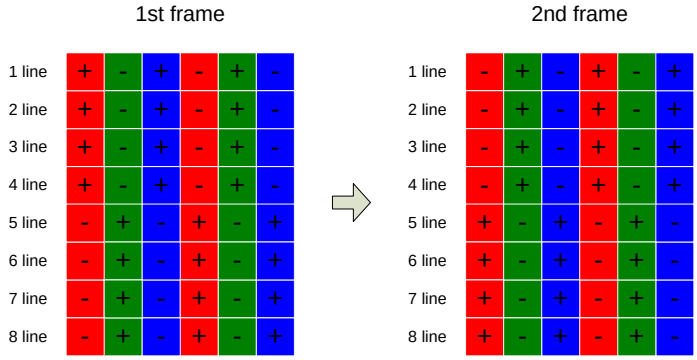
3-Dot Inversion


4-Dot Inversion


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<tr><td>Restriction</td><td>None</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
</table>

5.4.7. Dithering Enable (34h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
34h	1st	W/R	0	0	0	0	0	0	0	DITH_EN	00h
Description		**DITH_EN:** 0 : dithering function disable 1 : dithering function enable									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

5.4.8. Pump Clock Adjustment (40h~43h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
40h	1st	W/R	0	EXT_CPCK_SEL[1:0]		1	0	0	1	VGHL_CLK_EN	33h
42h	1st	W/R	0	VGHL_CLK_SELA[2:0]			0	VGHL_CLK_SELB[2:0]			44h
43h	1st	W/R	0	4002_RATIO_FREQA[2:0]			0	4002_RATIO_FREQB[2:0]			55h

Description

EXT_CPCK_SEL[1:0]: Pumping clock control signals selection to external control IC (ILI4003).Set the register before Sleep Out(R11h), when external pumping control be used.

EXT_CPCK_SEL[1:0]	EXTP & EXTN Output
0h	Output x 1.5 waveform
1h	Output x 2 waveform
2h	Output x 3 waveform
3h	Output Low (power down)

VGHL_CLK_EN: Enable the pumping cycle of step-up circuit of VGH and VGL.

VGHL_CLK_SELA[2:0]: Selects the pumping cycle of step-up circuit of VGH and VGL in the Normal Mode.

VGHL_CLK_SELB[2:0]: Selects the pumping cycle of step-up circuit of VGH and VGL in the Idle Mode.

4002_RATIO_FREQA[2:0]: Selects the pumping cycle of step-up circuit of external control IC (ILI4003) in the Normal Mode.

4002_RATIO_FREQB[2:0]: Selects the pumping cycle of step-up circuit of external control IC (ILI4003) in the Idle Mode.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

VGHL_CLK_SELA[2:0], VGHL_CLK_SELB[2:0]	Pumping cycle
0h	16H
1h	8H
2h	4H
3h	2H
4h	1H
5h	1/2H
Others	Reserved

4002_RATIO_FREQA[2:0], 4002_RATIO_FREQB[2:0]	Pumping cycle
0h	16H
1h	8H
2h	4H
3h	2H
4h	1H
5h	1/2H
6h	1/4H
7h	1/8H

Restriction	None

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>33h_44h_55h</td></tr>
<tr><td>S/W Reset</td><td>33h_44h_55h</td></tr>
<tr><td>H/W Reset</td><td>33h_44h_55h</td></tr>
</table>
</td></tr>
</table>

5.4.9. Power Control 1 (50h~51h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
50h	1st	W/R	VREG1[7:0]								95h
51h	1st	W/R	VREG2[7:0]								95h

Description

VREG1[7:0]: Set the VREG1OUT voltage for positive Gamma. (12mV/step)

VREG1[7:0]	VREG1OUT voltage (V)
42h	3.504
43h	3.516
44h	3.528
45h	3.540
46h	3.552
47h	3.564
:	:
94h	4.488
95h	4.500
96h	4.512
:	:
E8h	5.496
E9h	5.508
EAh	5.520
:	:
EFh	5.580
F0h	5.592
F1h	5.604
:	:
08h	5.628
09h	5.640
0Ah	5.652
:	:
0Dh	5.688
0Eh	5.700
0Fh	5.712
:	:
12h	5.748
13h	5.760
14h	5.772
15h	5.784
16h	5.796
17h	5.808
Other	Reserved

VREG2[7:0]: Set the VREG2OUT voltage for negative Gamma. (12mV/step)

VREG2[7:0]	VREG2OUT voltage (V)
42h	-3.564
43h	-3.576
44h	-3.588
45h	-3.600
46h	-3.612
47h	-3.624
:	:
94h	-4.548
95h	-4.560
96h	-4.572
:	:
E8h	-5.556
E9h	-5.568
EAh	-5.580
:	:
EFh	-5.640
F0h	-5.652
F1h	-5.664
:	:
08h	-5.688
09h	-5.700
0Ah	-5.712
:	:
0Dh	-5.748
0Eh	-5.760
0Fh	-5.772
:	:
12h	-5.808
13h	-5.820
14h	-5.832
15h	-5.844
16h	-5.856
17h	-5.868
Other	Reserved

Restriction	None

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
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<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>95h_95h</td></tr>
<tr><td>S/W Reset</td><td>95h_95h</td></tr>
<tr><td>H/W Reset</td><td>95h_95h</td></tr>
</table>
</td></tr>
</table>

VCOM Control 1 (52h~56h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
52h	1st	W/R	0	0	0	0	0	0	0	VCM1[8]	00h
53h	1st	W/R	VCM1[7:0]								7Bh
54h	1st	W/R	0	0	0	0	0	0	0	VCM2[8]	00h
55h	1st	W/R	VCM2[7:0]								7Bh
56h	1st	R	0	0	0	NVM2	0	0	0	NVM1	00h

Description

VCM1[8:0]: Set the VCOM level used for vertical forward scan (GS_PANEL= 1'b0), when NV memory isn't programmed. (12mV/step)

VCM2[8:0]: Set the VCOM level used for vertical backward scan (GS_PANEL= 1'b1), when NV memory isn't programmed. (12mV/step)

VCM1[8:0] VCM2[8:0]	VCOM voltage (V)
010h	-0.204
011h	-0.216
012h	-0.228
013h	-0.24
014h	-0.252
015h	-0.264
:	:
07Ah	-1.476
07Bh	-1.488
07Ch	-1.5
:	:
149h	-3.96
14Ah	-3.972
14Bh	-3.984
14Ch	-3.996
14Dh	-4.008
Others	Reserved

Note: VCOM ≧ VSN + 0.5V

NVM1 : Selection of the VCM source setting used for vertical forward scan (GS_PANEL= 1'b0). When the NV memory is programmed, the NVM1 will be set as '1' automatically.

0 : Register Page 1 R52h and R53h for VCM setting

1 : Register Page 4 RC4h and RC5h for VCM setting

NVM2 : Selection of the VCM source setting used for vertical backward scan (GS_PANEL= 1'b1). When the NV memory is programmed, the NVM2 will be set as '1' automatically.

0 : Register 54h and 55h for VCM setting

1 : Register Page 4 RC6h and RC7h for VCM setting

Note : If 1-byte program , VCOM OTP program address is register pg1_cmd_52h~55h,

If auto program, VCOM OTP program address is register pg4_cmd_C4h~C7h,

Restriction: None

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_7Bh_00h_7Bh_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_7Bh_00h_7Bh_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_7Bh_00h_7Bh_00h</td></tr>
</table>
</td></tr>
</table>

5.4.10. Entry Mode Set (58h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
58h	1st	W/R	LVD_EN	0	0	0	0	0	0	0	00h

Description

LVD_EN: Low voltage detection control.

LVD	Low voltage detection
0	Enable
1	Disable

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

5.4.11. Source Timing Adjust (60h~63h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
60h	1st	W/R	0	0	SDT[5:0]						14h
61h	1st	W/R	0	0	CRT[5:0]						00h
62h	1st	W/R	0	0	EQT[5:0]						19h
63h	1st	W/R	0	0	PCT[5:0]						10h

Description

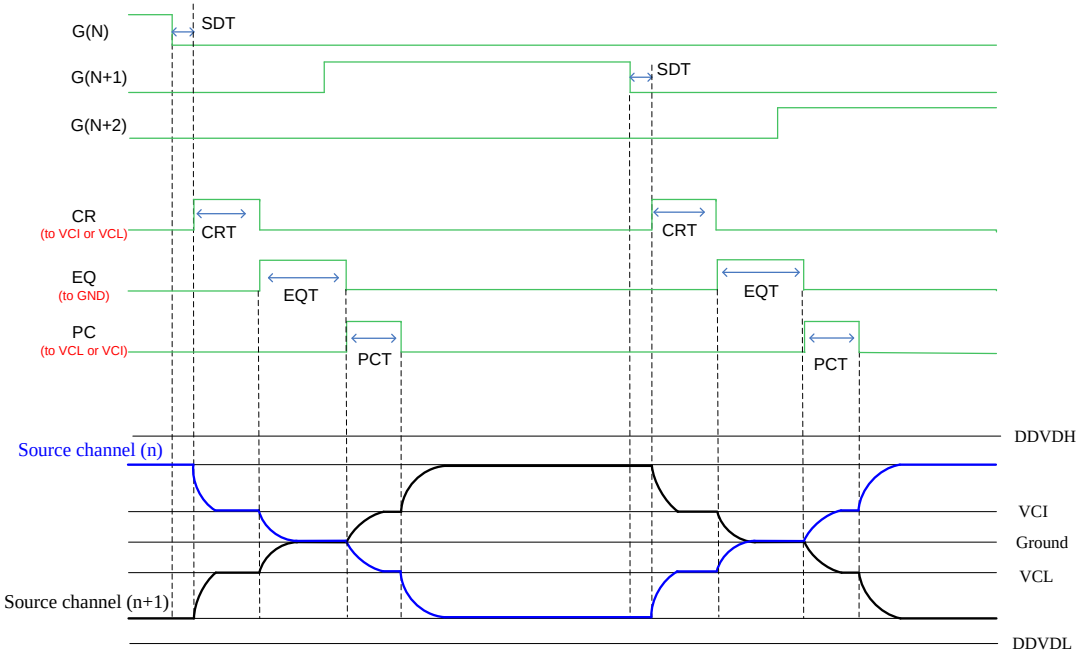
SDT[5:0]: Source SD timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

CRT[5:0]: Source CR timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

EQT[5:0]: Source EQ timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 8 to 71 time scales.

PCT[5:0]: Source PC timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

Note: T_{OP_CLK}: 62.5ns



Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	14h_00h_19h_10h
S/W Reset	14h_00h_19h_10h
H/W Reset	14h_00h_19h_10h

5.4.12. Positive Gamma Correction (A0h~B3h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
A0h	1st	W/R	0	0	VP0[5:0]						00h
A1h	1st	W/R	0	VP4[6:0]							0Dh
A2h	1st	W/R	0	VP8[6:0]							1Dh
A3h	1st	W/R	0	0	VP12[5:0]						11h
A4h	1st	W/R	0	0	VP16[5:0]						0Ch
A5h	1st	W/R	0	VP24[6:0]							23h
A6h	1st	W/R	0	0	VP36[5:0]						17h
A7h	1st	W/R	0	0	VP52[5:0]						1Ch
A8h	1st	W/R	VP80[7:0]								82h
A9h	1st	W/R	0	0	VP111[5:0]						21h
AAh	1st	W/R	0	0	VP144[5:0]						2Ah
ABh	1st	W/R	VP175[7:0]								6Bh
ACh	1st	W/R	0	0	VP203[5:0]						19h
ADh	1st	W/R	0	0	VP219[5:0]						14h
AEh	1st	W/R	0	VP231[6:0]							45h
AFh	1st	W/R	0	0	VP239[5:0]						1Dh
B0h	1st	W/R	0	0	VP243[5:0]						23h
B1h	1st	W/R	0	VP247[6:0]							52h
B2h	1st	W/R	0	VP251[6:0]							63h
B3h	1st	W/R	0	0	VP255[5:0]						39h

Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.
Restriction	None
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h

5.4.13. Pad Control (B6h~B7h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B6h	1st	W/R	IM_SW_EN	IM_SW[2:0]			RS_SW_EN	0	RS_SW[1:0]		00h
B7h	1st	W/R	0	0	0	0	0	0	LANSEL_SW_EN	LANSEL_SW	00h

Description

IM_SW_EN: Enable/Disable the lane sequence and polarity from internal command setting. The external hardware pin IM[2:0] has no effect when IM_SW_EN is "1".

IM_SW[2:0]: Set the configuration of lane sequence and polarity. (The bottom table is an example for MIPI 4 lane setting)

Internal Pad Control			Configuration of MIPI Lane				
IM_SW2	IM_SW1	IM_SW0	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P

RS_SW_EN: Enable/Disable the resolution from internal command setting. The external hardware pin RS[1:0] has no effect when RS_SW_EN is "1".

RS_SW[1:0]: Set the resolution.

RS_SW1	RS_SW0	Resolution
0	0	800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line
0	1	768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line
1	0	720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line
1	1	600 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line

LANSEL_SW_EN: Enable/Disable the lane number from internal command setting. The external hardware pin LANSEL has no effect when LANSEL_SW_EN is "1".

LANSEL_SW: Set the lane number.

LANSEL_SW="1", MIPI DSI is 2 Lane mode
LANSEL_SW="0", MIPI DSI is 3 or 4 Lane mode

Note: Please reference "Table 2: DSI Interface Lane Mode Selection"

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

5.4.14. Negative Gamma Correction (C0h~D3h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C0h	1st	W/R	0	0	VN0[5:0]						00h
C1h	1st	W/R	0	VN4[6:0]							0Dh
C2h	1st	W/R	0	VN8[6:0]							1Dh
C3h	1st	W/R	0	0	VN12[5:0]						11h
C4h	1st	W/R	0	0	VN16[5:0]						0Ch
C5h	1st	W/R	0	VN24[6:0]							23h
C6h	1st	W/R	0	0	VN36[5:0]						17h
C7h	1st	W/R	0	0	VN52[5:0]						1Ch
C8h	1st	W/R	VN80[7:0]								82h
C9h	1st	W/R	0	0	VN111[5:0]						21h
CAh	1st	W/R	0	0	VN144[5:0]						2Ah
CBh	1st	W/R	VN175[7:0]								6Bh
CCh	1st	W/R	0	0	VN203[5:0]						19h
CDh	1st	W/R	0	0	VN219[5:0]						14h
CEh	1st	W/R	0	VN231[6:0]							45h
CFh	1st	W/R	0	0	VN239[5:0]						1Dh
D0h	1st	W/R	0	0	VN243[5:0]						23h
D1h	1st	W/R	0	VN247[6:0]							52h
D2h	1st	W/R	0	VN251[6:0]							63h
D3h	1st	W/R	0	0	VN255[5:0]						39h

Description	Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.
Restriction	None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h 2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h

5.4.15. NV Memory Write (E0h~E2h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E0h	1st	W/R	PGM_DATA[7:0]								00h
E1h	1st	W/R	PGM_ADR[7:0]								00h
E2h	1st	W/R	PGM_ADR[15:8]								00h

Description

This command is used to program or read the NV memory data.

After a successful OTP operation, the information of PGM_DATA[7:0] will be programmed to the NV memory.

PGM_DATA[7:0]: The programmed data.

PGM_ADR[15:0]: Set the address of the NV memory for programming data. See chapter 14 “NV Memory Programming Flow”.

PGM_ADR[15:0]	Programming data
1h	ID1
2h	ID2
3h	ID3
4h	VCM1[8]
5h	VCM1[7:0]
6h	VCM2[8]
7h	VCM2[7:0]
8h	VREG1[7:0]
9h	VREG2[7:0]
68h~7Bh	REGAM0_P~ REGAM255_P
7Ch~8Fh	REGAM0_N~ REGAM255_N

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h
S/W Reset	00h_00h_00h
H/W Reset	00h_00h_00h

5.4.16. NV Memory Protection Key (E3h~E5h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E3h	1st	W/R	KEY[23:16]								00h
E4h	1st	W/R	KEY[15:8]								00h
E5h	1st	W/R	KEY[7:0]								00h
Description		**KEY[23:0]:** NV memory programming protection key. Write an OTP data to PGM_DATA[7:0], this KEY[23:0] must set 0x55AA66h to enable OTP programming. If the KEY[23:0] is not 0x55AA66h, the NV Memory program will be aborted.									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_00h
S/W Reset	00h_00h_00h
H/W Reset	00h_00h_00h

5.4.17. NV Memory Status Read (E6h~E9h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
E6h	1st	R	0	ID2_MK[2:0]			0	ID1_MK[2:0]			00h
E7h	1st	R	0	0	0	0	0	ID3_MK[2:0]			00h
E8h	1st	R	GAMMA P_MK	GAMMA N_MK	VCM2_MK[2:0]			VCM1_MK[2:0]			00h
E9h	1st	R	OTP_BU SY	0	0	0	0	0	0	0	00h

Description

These registers uses a mark to record the NV memory programmed time. The bits are increase "+1" automatically after writing the PGM_DATA [7:0] to the NV memory.

ID1_MK[2:0]/ID2_MK[2:0]:

ID1_MK[2:0] / ID2_MK[2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

ID3_MK[2:0]:

ID3_MK[2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

VCM1_MK[2:0] /VCM2_MK[2:0]:

VCM1_MK[2:0] / VCM2_MK[2:0]			Description
0	0	0	No Programmed
0	0	1	Programmed 1 time already
0	1	1	Programmed 2 times already
1	1	1	Programmed 3 times already

GAMP_MK / GAMN_MK :

GAMP_MK / GAMN_MK	Description
0	No Programmed
1	Programmed 1 time already

OTP BUSY: The status bit of the NV memory programming.

OTP_BUSY	The Status of NV Memory
0	Idle
1	Busy

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	00h_00h_00h_00h
S/W Reset	00h_00h_00h_00h
H/W Reset	00h_00h_00h_00h

5.4.18. Time Stamp (F0h~F1h)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
F0h	1st	W/R	Time_Stamp_Week[7:0]								00h
F1h	1st	W/R	Time_Stamp_Year[7:0]								00h
Description		This command identifies the display module's manufacture date **Time_Stamp_Week[7:0]:** Week of manufacture. **Time_Stamp_Year[7:0]:** Year of manufacture.									
Restriction											
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h
S/W Reset	00h_00h
H/W Reset	00h_00h

5.4.19. EXTC Command Set Enable Register (FFh)

Command Page			Page 1								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								01h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	01h
S/W Reset	01h
H/W Reset	01h

5.5. Page 2 Command Description

5.5.1. Dynamic Backlight Control 1 (03h~05h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
03h	1st	W/R	0	TT_STP_MED[2:0]			1	TT_STP_LOW[2:0]			29h
04h	1st	W/R	0	ST_TIM_LOW[2:0]			0	TT_STP_HIGH[2:0]			14h
05h	1st	W/R	0	ST_TIM_HIGH[2:0]			0	ST_TIM_MED[2:0]			32h

Description

TT_STP_HIGH[2:0]: This parameter is used set the dimming transition step for CABC high enhancement.

TT_STP_MED[2:0]: This parameter is used set the dimming transition step for CABC medium enhancement.

TT_STP_LOW[2:0]: This parameter is used set the dimming transition step for CABC low enhancement.

TT_STP_HIGH[2:0] TT_STP_MED[2:0] TT_STP_LOW[2:0]	Description
0h	1 step
1h	2 step
2h	4 step
3h	8 step
4h	16 step
5h	32 step
6h	64 step
7h	128 step

ST_TIM_HIGH[2:0]: This parameter is used set the dimming time for CABC high enhancement.

ST_TIM_ MED[2:0]: This parameter is used set the dimming time for CABC medium enhancement.

ST_TIM_ LOW[2:0]: This parameter is used set the dimming time for CABC low enhancement.

ST_TIM_HIGH[2:0] ST_TIM_MED[2:0] ST_TIM_LOW[2:0]	Description
0h	1 frame
1h	2 frame
2h	4 frame
3h	8 frame
4h	16 frame
5h	32 frame
6h	64 frame
7h	128 frame

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	29h_14h_32h
S/W Reset	29h_14h_32h
H/W Reset	29h_14h_32h

5.5.2. Dynamic Backlight Control 2 (06h~07h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
06h	1st	W/R	0	PWM_DUTY_PRECISION[2:0]			0	LEDPWM_POL	LEDON_POL	LEDON	00h
07h	1st	W/R	PWM_DIV[7:0]								0Eh

Description

LEDON: The bit is used to define LEDON enable.

LEDON_POL: The bit is used to define polarity of LEDON.

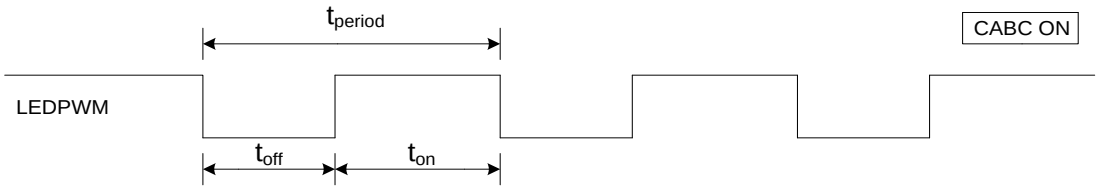
LEDPWM_POL: The bit is used to define polarity of LEDPWM signal.

BL	LEDPWM_POL	LEDPWM pin
0	0	Always low
0	1	Always high
1	0	Original polarity of LEDPWM signal
1	1	Inversed polarity of LEDPWM signal

PWM_DUTY_PRECISION[2:0] / PWM_DIV[7:0]: LEDPWM output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period is calculated using the following equation.

$$f_{LEDPWM} = \frac{32\ MHz}{(\text{PWM\_DIV}[7:0]+1) \times PWM\_DUTY\_PRECISION}$$

PWM_DUTY_PRECISION[2:0]	*PWM_DUTY_PRECISION*	$f_{LEDPWM\ (MAX)}$ (PWM_DIV[7:0]=0)	$f_{LEDPWM\ (min)}$ (PWM_DIV[7:0]=255)
0h	4096	7.8 KHz	31 Hz
1h	2048	15.6 KHz	61 Hz
2h	1024	31.2 KHz	122 Hz
3h	512	62.5 KHz	244 Hz
4h	256	125 KHz	488 Hz
5h~7h	Reserved	X	X



Note : The output frequency tolerance of internal frequency divider in CABC is ±10%

X = void.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_0Eh
S/W Reset	00h_0Eh
H/W Reset	00h_0Eh

5.5.3. IIE Function Control (10h~19h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
10h	1st	W/R	0	0	0	0	0	PRT_EN	SKIN_EN	0	06h
11h	1st	W/R	0	AUTO_MEAN	0	0	CN_EN	CN_INV	SHP_EN	0	00h
12h	1st	W/R	0	0	0	0	0	0	CN_LV[1:0]		02h
13h	1st	W/R	0	0	1	0	SRE_MIDIV_LV[1:0]		0	0	20h
15h	1st	W/R	RGB_MEAN[7:0]								80h
16h	1st	W/R	SRE_HYSTERESIS_EN	0	0	SRE_DIM_EN	SRE_SC_EN	SRE_CE_EN	0	0	1Ch
17h	1st	W/R	0	SRE_OFFS[2:0]			0	SRE_DIM_STP[2:0]			01h
18h	1st	W/R	SRE_DIM_FRAME[7:0]								08h
19h	1st	W/R	SRE_SC_GAIN_ADJ[2:0]			SRE_HYSTERESIS_LIMIT[4:0]					C0h

Description

PRT_EN: Enable the over-saturation protection of saturation enhancement.

SKIN_EN: Enable the skin-tone protection of saturation enhancement.

AUTO_MEAN: Enable auto image mean calculation RGB_MEAN[7:0] is not available when AUTO_MEAN=1h.

CN_EN: Enable contrast enhancement.

CN_INV: Select contrast enhancement Function.

CN_INV	Contrast Function
0	Contrast increase
1	Contrast decrease

SHP_EN: Enable sharpness enhancement.

CN_LV[1:0] : Define contrast enhancement level.

SRE_MIDIV_LV[1:0] : Define SRE medium level enhancement select.

SRE_MIDIV_LV[1:0]	Enhancement level
00h / 11h	Level_M
01h	Level_H
10h	Level_L

RGB_MEAN[7:0]: Setting image mean value, available when AUTO_MEAN=0h.

SRE_HYSTERESIS_EN: SRE hysteresis mode enable signal.

SRE_DIM_EN: SRE dimming function enable signal.

SRE_SC_EN: SRE saturation compensation enable.

SRE_CE_EN: SRE contrast enhancement enable.

SRE_OFFS[2:0]: SRE offset value

SRE_DIM_STP[2:0]: Setting the number of dimming steps for transition

SRE_DIM_STP[2:0]	Description
0h	2 step
1h	4 step
2h	8 step
3h	16 step
4h	32 step
5h	64 step
6h	128 step
7h	256 step

SRE_DIM_FRAME[7:0]: Setting the step time as frame units for each dimming step

	<table><tr><th>SRE_DIM_FRAME[7:0]</th><th>Description</th></tr><tr><td>0h~2h</td><td>2 frame</td></tr><tr><td>3</td><td>4 frame</td></tr><tr><td>4</td><td>4 frame</td></tr><tr><td>5</td><td>5 frame</td></tr><tr><td>6</td><td>6 frame</td></tr><tr><td>:</td><td>:</td></tr><tr><td>:</td><td>:</td></tr><tr><td>254</td><td>254 frame</td></tr><tr><td>255</td><td>255 frame</td></tr></table> **SRE_SC_GAIN_ADJ[2:0]:** SRE saturation compensation gain value **SRE_HYSTERESIS_LIMIT[4:0]:** SRE hysteresis limit value when hysteresis mode on
Restriction	None
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>06h_00h_02h_20h_80h_1Ch_01h_08h_C0h</td></tr><tr><td>S/W Reset</td><td>06h_00h_02h_20h_80h_1Ch_01h_08h_C0h</td></tr><tr><td>H/W Reset</td><td>06h_00h_02h_20h_80h_1Ch_01h_08h_C0h</td></tr></table>

5.5.4. IIE Saturation Enhancement Control 1 (1Ah~1Ch)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
1Ah	1st	W/R	0	0	SE_RATIO_L[5:0]						07h
1Bh	1st	W/R	0	0	SE_RATIO_M[5:0]						09h
1Ch	1st	W/R	0	0	SE_RATIO_H[5:0]						0Ch

Description

SE_RATIO_L[5:0]: Define low saturation enhancement level of User Command 55h (Page0_R55h).

SE_RATIO_M[5:0]: Define medium saturation enhancement level of User Command 55h (Page0_R55h).

SE_RATIO_H[5:0]: Define high saturation enhancement level of User Command 55h (Page0_R55h).

$$Saturation_{enhanced} = Saturation_{original} + (Saturation_{original} \times SE\_RATIO)$$

SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)	SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)
00h	0.0	10h	1.0
01h	0.0625	11h	1.0625
02h	0.125	12h	1.125
03h	0.1875	13h	1.1875
04h	0.25	14h	1.25
05h	0.3125	15h	1.3125
06h	0.375	16h	1.375
07h	0.4375	17h	1.4375
08h	0.5	18h	1.5
09h	0.5625	19h	1.5625
0Ah	0.625	1Ah	1.625
0Bh	0.6875	1Bh	1.6875
0Ch	0.75	1Ch	1.75
0Dh	0.8125	1Dh	1.8125
0Eh	0.875	1Eh	1.875
0Fh	0.9375	1Fh	1.9375

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	07h_09h_0Ch
S/W Reset	07h_09h_0Ch
H/W Reset	07h_09h_0Ch

5.5.5. IIE Saturation Protection Control (40h~4Fh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
40h	1st	W/R	0	0	0	LEVEL0_SR[4:0]					02h
41h	1st	W/R	0	0	0	LEVEL1_SR[4:0]					04h
42h	1st	W/R	0	0	0	LEVEL2_SR[4:0]					06h
43h	1st	W/R	0	0	0	LEVEL3_SR[4:0]					08h
44h	1st	W/R	0	0	0	LEVEL4_SR[4:0]					0Ah
45h	1st	W/R	0	0	0	LEVEL5_SR[4:0]					0Ch
46h	1st	W/R	0	0	0	LEVEL6_SR[4:0]					0Eh
47h	1st	W/R	0	0	0	LEVEL7_SR[4:0]					0Eh
48h	1st	W/R	0	0	0	LEVEL8_SR[4:0]					0Ch
49h	1st	W/R	0	0	0	LEVEL9_SR[4:0]					0Ah
4Ah	1st	W/R	0	0	0	LEVEL10_SR[4:0]					08h
4Bh	1st	W/R	0	0	0	LEVEL11_SR[4:0]					06h
4Ch	1st	W/R	0	0	0	LEVEL12_SR[4:0]					04h
4Dh	1st	W/R	0	0	0	LEVEL13_SR[4:0]					03h
4Eh	1st	W/R	0	0	0	LEVEL14_SR[4:0]					02h
4Fh	1st	W/R	0	0	0	LEVEL15_SR[4:0]					00h

Description

This register is used to restrict the enhancement gain of saturation enhancement. This function is able to use when PRT_EN=1.

LEVEL0_SR[4:0]: Adjust the weight value of saturation steps 0~15.

LEVEL1_SR[4:0]: Adjust the weight value of saturation steps 16~31.

LEVEL2_SR[4:0]: Adjust the weight value of saturation steps 32~47.

LEVEL3_SR[4:0]: Adjust the weight value of saturation steps 48~63.

LEVEL4_SR[4:0]: Adjust the weight value of saturation steps 64~79.

LEVEL5_SR[4:0]: Adjust the weight value of saturation steps 80~95.

LEVEL6_SR[4:0]: Adjust the weight value of saturation steps 96~111.

LEVEL7_SR[4:0]: Adjust the weight value of saturation steps 128~143.

LEVEL8_SR[4:0]: Adjust the weight value of saturation steps 144~159.

LEVEL9_SR[4:0]: Adjust the weight value of saturation steps 160~175.

LEVEL10_SR[4:0]: Adjust the weight value of saturation steps 176~191.

LEVEL11_SR[4:0]: Adjust the weight value of saturation steps 192~207.

LEVEL12_SR[4:0]: Adjust the weight value of saturation steps 208~223.

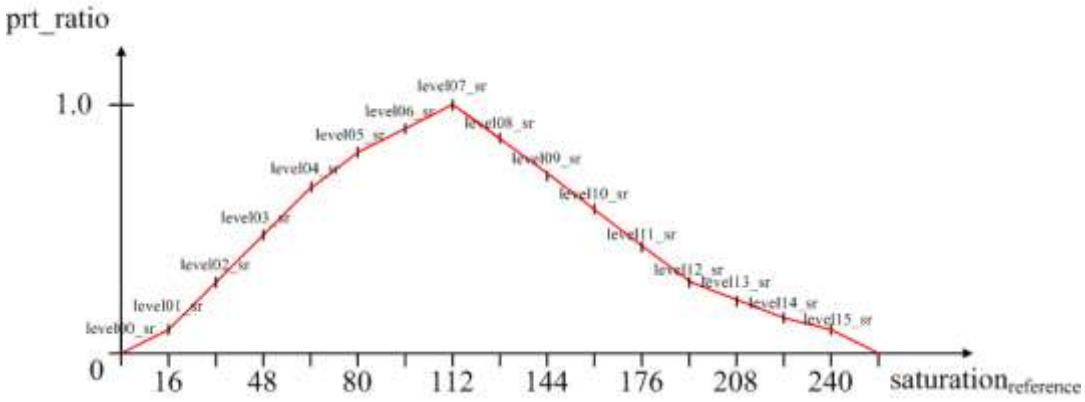
LEVEL13_SR[4:0]: Adjust the weight value of saturation steps 224~239.

LEVEL14_SR[4:0]: Adjust the weight value of saturation steps 240~255.

LEVEL15_SR[4:0]: Adjust the weight value of saturation steps 256.

$$Saturation_{enhanced} = Saturation_{original} + (Saturation_{original} \times SE\_RATIO \times PRT\_RATIO)$$

$$PRT\_RATIO = 0 \sim 1.0$$

<table>
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td>None</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td></tr>
<tr><td>S/W Reset</td><td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td></tr>
<tr><td>H/W Reset</td><td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td></tr>
</table>
</td></tr>
</table>

5.5.6. IIE Sharpness Enhancement Control (5Ah~5Ch)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Ah	1st	W/R	0	0	0	SHP_RATIO[4:0]					18h
5Bh	1st	W/R	SHP_THR_H[7:0]								64h
5Ch	1st	W/R	SHP_THR_L[7:0]								1Eh

Description

This register sets the enhancement level of the sharpness enhancement. This function is able to use when SHP_EN=1

SHP_RATIO[4:0]: Adjust the ratio of sharpness enhancement.

$$Y_{enh} = Y_{org} + (Y_{org} – blur(Y_{org})) \times SHP\_RATIO$$

SHP_RATIO[4:0]	Ratio (Dec)	SHP_RATIO[4:0]	Ratio (Dec)
00h	0.0	10h	2.0
01h	0.125	11h	2.125
02h	0.25	12h	2.25
03h	0.375	13h	2.375
04h	0.5	14h	2.5
05h	0.625	15h	2.625
06h	0.75	16h	2.75
07h	0.875	17h	2.875
08h	1.0	18h	3.0
09h	1.125	19h	3.125
0Ah	1.25	1Ah	3.25
0Bh	1.375	1Bh	3.375
0Ch	1.5	1Ch	3.5
0Dh	1.625	1Dh	3.625
0Eh	1.75	1Eh	3.75
0Fh	1.875	1Fh	3.875

SHP_THR_H[7:0]: Define Sharpness enhancement upper bound threshold.

SHP_THR_L[7:0]: Define Sharpness enhancement lower bound threshold.

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	18h_64h_1Eh
S/W Reset	18h_64h_1Eh
H/W Reset	18h_64h_1Eh

5.5.7. IIE Contrast Enhancement Control (60h~66h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
60h	1st	W/R	0	0	CN_00[5:0]						0Eh
61h	1st	W/R	0	0	CN_01[5:0]						18h
62h	1st	W/R	0	0	CN_02[5:0]						24h
63h	1st	W/R	0	0	CN_03[5:0]						28h
64h	1st	W/R	0	0	CN_04[5:0]						24h
65h	1st	W/R	0	0	CN_05[5:0]						18h
66h	1st	W/R	0	0	CN_06[5:0]						0Eh

Description

This register sets the weight value of the turning point of contrast gain cure. This function is able to use when CN_EN=1

CN_00[5:0]: Adjust the weight of S curve ratio of turning point 1.

CN_01[5:0]: Adjust the weight of S curve ratio of turning point 2.

CN_02[5:0]: Adjust the weight of S curve ratio of turning point 3.

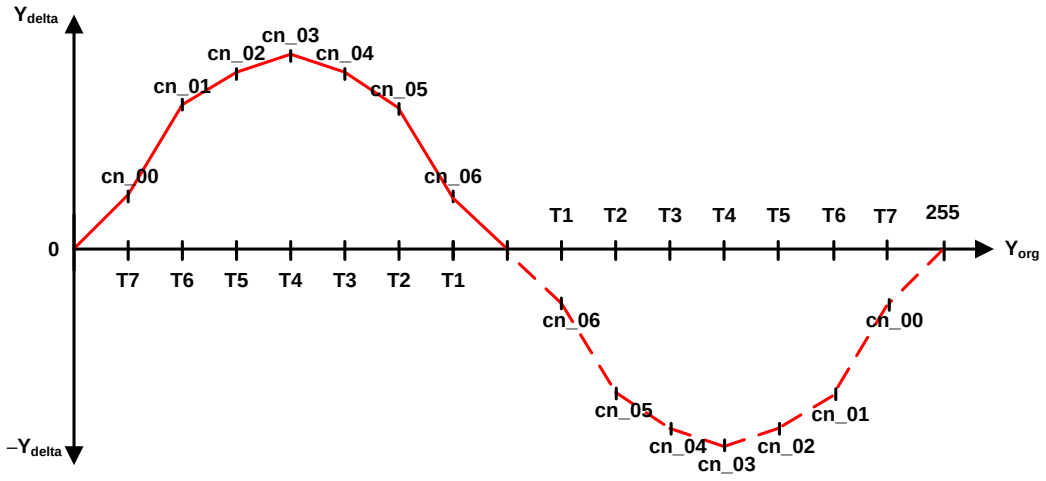
CN_03[5:0]: Adjust the weight of S curve ratio of turning point 4.

CN_04[5:0]: Adjust the weight of S curve ratio of turning point 5.

CN_05[5:0]: Adjust the weight of S curve ratio of turning point 6.

CN_06[5:0]: Adjust the weight of S curve ratio of turning point 7.

$$Y_{enh} = Y_{org} + Y_{delta}$$



Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0Eh_18h_24h_28h_24h_18h_0Eh
S/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh
H/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh

5.5.8. IIE Auto White Balance 1 (D0h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
D0h	1st	W/R	0	0	0	0	0	0	0	AWB_EN	00h
Description		**AWB_EN :** Enable AWB function, active high.									
Restriction		To enable this command, “EXTC Command Set enable register (FFh) “must set first.									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

5.5.9. IIE Auto White Balance 2 (D1h~D4h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
D1h	1st	W/R	0	0	R_AWB_1[9:8]		G_AWB_1[9:8]		B_AWB_1[9:8]		3Fh
D2h	1st	W/R	R_AWB_1[7:0]								FFh
D3h	1st	W/R	G_AWB_1[7:0]								FFh
D4h	1st	W/R	B_AWB_1[7:0]								FFh
Description			**R_AWB_1[9:0] :** Adjust the drop level of red. R = R x (1 + R_AWB_1)/1024 **G_AWB_1[9:0] :** Adjust the drop level of green. G = G x (1 + G_AWB_1)/1024 **B_AWB_1[9:0] :** Adjust the drop level of blue. B = B x (1 + B_AWB_1)/1024								
Restriction			To enable this command, “EXTC Command Set enable register (FFh) “must set first.								

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.10. IIE Auto White Balance 3 (D5~D8)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
D5h	1st	W/R	0	0	R_AWB_2[9:8]		G_AWB_2[9:8]		B_AWB_2[9:8]		3Fh
D6h	1st	W/R	R_AWB_2[7:0]								FFh
D7h	1st	W/R	G_AWB_2[7:0]								FFh
D8h	1st	W/R	B_AWB_2[7:0]								FFh

Description

R_AWB_2[9:0] : Adjust the drop level of red. R = R x (1 + R_AWB_2)/1024

G_AWB_2[9:0] : Adjust the drop level of green. G = G x (1 + G_AWB_2)/1024

B_AWB_2[9:0] : Adjust the drop level of blue. B = B x (1 + B_AWB_2)/1024

Restriction

To enable this command, “EXTC Command Set enable register (FFh) “must set first.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.11. IIE Auto White Balance 4 (D9h~DCh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
D9h	1st	W/R	0	0	R_AWB_3[9:8]		G_AWB_3[9:8]		B_AWB_3[9:8]		3Fh
DAh	1st	W/R	R_AWB_3[7:0]								FFh
DBh	1st	W/R	G_AWB_3[7:0]								FFh
DCh	1st	W/R	B_AWB_3[7:0]								FFh
Description			**R_AWB_3[9:0] :** Adjust the drop level of red. R = R x (1 + R_AWB_3)/1024 **G_AWB_3[9:0] :** Adjust the drop level of green. G = G x (1 + G_AWB_3)/1024 **B_AWB_3[9:0] :** Adjust the drop level of blue. B = B x (1 + B_AWB_3)/1024								
Restriction			To enable this command, “EXTC Command Set enable register (FFh) “must set first.								

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.12. IIE Auto White Balance 5 (DDh~E0h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
DDh	1st	W/R	0	0	R_AWB_4[9:8]		G_AWB_4[9:8]		B_AWB_4[9:8]		3Fh
DEh	1st	W/R	R_AWB_4[7:0]								FFh
DFh	1st	W/R	G_AWB_4[7:0]								FFh
E0h	1st	W/R	B_AWB_4[7:0]								FFh
Description			**R_AWB_4[9:0] :** Adjust the drop level of red. R = R x (1 + R_AWB_4)/1024 **G_AWB_4[9:0] :** Adjust the drop level of green. G = G x (1 + G_AWB_4)/1024 **B_AWB_4[9:0] :** Adjust the drop level of blue. B = B x (1 + B_AWB_4)/1024								
Restriction			To enable this command, “EXTC Command Set enable register (FFh) “must set first.								

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.13. IIE Auto White Balance 6 (E1h~E4h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
E1h	1st	W/R	0	0	R_AWB_5[9:8]		G_AWB_5[9:8]		B_AWB_5[9:8]		3Fh
E2h	1st	W/R	R_AWB_5[7:0]								FFh
E3h	1st	W/R	G_AWB_5[7:0]								FFh
E4h	1st	W/R	B_AWB_5[7:0]								FFh
Description			**R_AWB_5[9:0] :** Adjust the drop level of red. R = R x (1 + R_AWB_5)/1024 **G_AWB_5[9:0] :** Adjust the drop level of green. G = G x (1 + G_AWB_5)/1024 **B_AWB_5[9:0] :** Adjust the drop level of blue. B = B x (1 + B_AWB_5)/1024								
Restriction			To enable this command, “EXTC Command Set enable register (FFh) “must set first.								

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.14. IIE Auto White Balance 7 (E5h~E8h)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
E5h	1st	W/R	0	0	R_AWB_6[9:8]		G_AWB_6[9:8]		B_AWB_6[9:8]		3Fh
E6h	1st	W/R	R_AWB_6[7:0]								FFh
E7h	1st	W/R	G_AWB_6[7:0]								FFh
E8h	1st	W/R	B_AWB_6[7:0]								FFh
Description			**R_AWB_6[9:0] :** Adjust the drop level of red. R = R x (1 + R_AWB_6)/1024 **G_AWB_6[9:0] :** Adjust the drop level of green. G = G x (1 + G_AWB_6)/1024 **B_AWB_6[9:0] :** Adjust the drop level of blue. B = B x (1 + B_AWB_6)/1024								
Restriction			To enable this command, “EXTC Command Set enable register (FFh) “must set first.								

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.15. IIE Auto White Balance 8 (E9h~ECh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Defaut**
E9h	1st	W/R	0	0	R_AWB_7[9:8]		G_AWB_7[9:8]		B_AWB_7[9:8]		3Fh
EAh	1st	W/R	R_AWB_7[7:0]								FFh
EBh	1st	W/R	G_AWB_7[7:0]								FFh
ECh	1st	W/R	B_AWB_7[7:0]								FFh
Description			**R_AWB_7[9:0] :** Adjust the drop level of red. R = R x (1 + R_AWB_7)/1024 **G_AWB_7[9:0] :** Adjust the drop level of green. G = G x (1 + G_AWB_7)/1024 **B_AWB_7[9:0] :** Adjust the drop level of blue. B = B x (1 + B_AWB_7)/1024								
Restriction			To enable this command, “EXTC Command Set enable register (FFh) “must set first.								

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	3Fh_FFh_FFh_FFh
S/W Reset	3Fh_FFh_FFh_FFh
H/W Reset	3Fh_FFh_FFh_FFh

5.5.16. IIE Auto White Balance 9 (EDh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
EDh	1st	W/R	Color_Temp_Adj[7:0]								60h

Description

Color_Temp_Adj : Adjust color temperature.

Color_Temp_Adj[7:0]	Adjust Value
7'h00	AWB_1
7'h01	AWB_1 * (31/32) + AWB_2 * (1/32)
7'h02	AWB_1 * (30/32) + AWB_2 * (2/32)
….	…..
7'h1F	AWB_1 * (1/32) + AWB_2 * (31/32)
7'h20	AWB_2
7'h21	AWB_2 * (31/32) + AWB_3 * (1/32)
7'h22	AWB_2 * (30/32) + AWB_3 * (2/32)
….	…..
7'h3F	AWB_2 * (1/32) + AWB_3 * (31/32)
7'h40	AWB_3
7'h41	AWB_3 * (31/32) + AWB_4 * (1/32)
7'h42	AWB_3 * (30/32) + AWB_4 * (2/32)
….	…..
7'h5F	AWB_3 * (1/32) + AWB_4 * (31/32)
7'h60	AWB_4
7'h61	AWB_4 * (31/32) + AWB_5 * (1/32)
7'h62	AWB_4 * (30/32) + AWB_5 * (2/32)
….	…..
7'h7F	AWB_4 * (1/32) + AWB_5 * (31/32)
7'h80	AWB_5
7'h81	AWB_5 * (31/32) + AWB_6 * (1/32)
7'h82	AWB_5 * (30/32) + AWB_6 * (2/32)
….	…..
7'h9F	AWB_5 * (1/32) + AWB_6 * (31/32)
7'hA0	AWB_6
7'hA1	AWB_6 * (31/32) + AWB_7 * (1/32)
7'hA2	AWB_6 * (30/32) + AWB_7 * (2/32)
….	…..
7'hBF	AWB_6 * (1/32) + AWB_7 * (31/32)
7'hC0	AWB_7
7'hC1	Reserved
….	….
7'hFF	Reserved

Restriction: To enable this command, "EXTC Command Set enable register (FFh) "must set first.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

Status	Default Value
Power On Sequence	60h
S/W Reset	60h
H/W Reset	60h

5.5.17. EXTC Command Set Enable Register (FFh)

Command Page			Page 2								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								02h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

5.6. Page 3 Command Description

5.6.1. GIP Setting 1 (01h~44h)

Command Page			Page 3								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	1st	W/R	Reserve for other setting								-
02h	1st	W/R	Reserve for other setting								-
03h	1st	W/R	STV_A_Rise[9:8]		Phase_STV_A[1:0]		Overlap_STV_A[2:0]				-
04h	1st	W/R	STV_B_Rise[9:8]		Phase_STV_B[1:0]		Overlap_STV_B[2:0]				-
05h	1st	W/R	STV_C_Rise[9:8]		Phase_STV_C[1:0]		Overlap_STV_C[2:0]				-
06h	1st	W/R	STV_A_Rise[7:0]								-
07h	1st	W/R	STV_B_Rise[7:0]								-
08h	1st	W/R	STV_C_Rise[7:0]								-
09h	1st	W/R	FTI_1_Rise[7:0]								-
0Ah	1st	W/R	FTI_2_Rise[7:0]								-
0Bh	1st	W/R	FTI_3_Rise[7:0]								-
0Ch	1st	W/R	FTI_1_Fall[7:0]								-
0Dh	1st	W/R	FTI_2_Fall[7:0]								-
0Eh	1st	W/R	FTI_3_Fall[7:0]								-
0Fh	1st	W/R	CLW_1_Rise[7:0]								-
10h	1st	W/R	CLW_2_Rise[7:0]								-
11h	1st	W/R	Reserve for other setting								-
12h	1st	W/R	Reserve for other setting								-
13h	1st	W/R	CLW_X_Fall[7:0]								-
14h	1st	W/R	Reserve for other setting								-
15h	1st	W/R	GPM_R_Stage_i[7:0]								-
16h	1st	W/R	GPM_R_Stage_ii[7:0]								-
17h	1st	W/R	GPM_F_Stage_i[7:0]								-
18h	1st	W/R	GPM_F_Stage_ii[7:0]								-
19h	1st	W/R	Reserve for other setting								-
1Ah	1st	W/R	Reserve for other setting								-
1Bh	1st	W/R	Reserve for other setting								-
1Ch	1st	W/R	Reserve for other setting								-
1Dh	1st	W/R	Reserve for other setting								-
1Eh	1st	W/R	GS_ENA	CLK_A_Rise[10:8]			Reserve for other setting	CLK_A_Fall[10:8]			-
1Fh	1st	W/R	Reserve for other setting	CLK_B_Rise[10:8]			Reserve for other setting	CLK_B_Fall[10:8]			-
20h	1st	W/R	CLK_A_Rise[7:0]								-
21h	1st	W/R	CLK_A_Fall[7:0]								-
22h	1st	W/R	CLK_B_Rise[7:0]								-
23h	1st	W/R	Reserve for other setting								-
24h	1st	W/R	CLK_Keep_Pos1[7:0]								-
25h	1st	W/R	CLK_Keep_Pos2[7:0]								-
26h	1st	W/R	Reserve for other setting								-
27h	1st	W/R	Reserve for other setting								-
28h	1st	W/R	CLK_Disable	CLK_x_Numb[2:0]			CLK_Keep	Phase_CLK[2:0]			-
29h	1st	W/R	Reserve for other setting				Overlap_CLK[3:0]				-
2Ah	1st	W/R	Reserve for other setting								-
2Bh	1st	W/R	Reserve for other setting								-
2Ch	1st	W/R	Reserve for other setting								-
2Dh	1st	W/R	Reserve for other setting								-
2Eh	1st	W/R	Reserve for other setting								-

2Fh	1st	W/R	Reserve for other setting	-
30h	1st	W/R	Reserve for other setting	-
31h	1st	W/R	Reserve for other setting	-
32h	1st	W/R	Reserve for other setting	-
33h	1st	W/R	Reserve for other setting	-
34h	1st	W/R	Reserve for other setting	-
35h	1st	W/R	Reserve for other setting	-
36h	1st	W/R	Reserve for other setting	-
37h	1st	W/R	Reserve for other setting	-
38h	1st	W/R	Reserve for other setting	-
39h	1st	W/R	Reserve for other setting	-
3Ah	1st	W/R	Reserve for other setting	-
3Bh	1st	W/R	Reserve for other setting	-
3Ch	1st	W/R	Reserve for other setting	-
3Dh	1st	W/R	Reserve for other setting	-
3Eh	1st	W/R	Reserve for other setting	-
3Fh	1st	W/R	Reserve for other setting	-
40h	1st	W/R	Reserve for other setting	-
41h	1st	W/R	Reserve for other setting	-
42h	1st	W/R	Reserve for other setting	-
43h	1st	W/R	Reserve for other setting	-
44h	1st	W/R	Reserve for other setting	-

Description

GS_ENA : Internal gate reverse function.

GS_ENA	Description
0	On
1	Off

CLK_X_Numb[2:0] : Number of CLK reverse.(internal gate reverse function)

CLK_X_Numb[2:0]	Number of CLK
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Note: Normally, set CLK_x_Numb[2:0] = Phase_CLK[2:0]

CLK_Disable : reg_CLK_Keep_PosX setting.

CLK_Disable	Description
0	Enable
1	Disable

CLK_Keep : CLK toggle continuously.

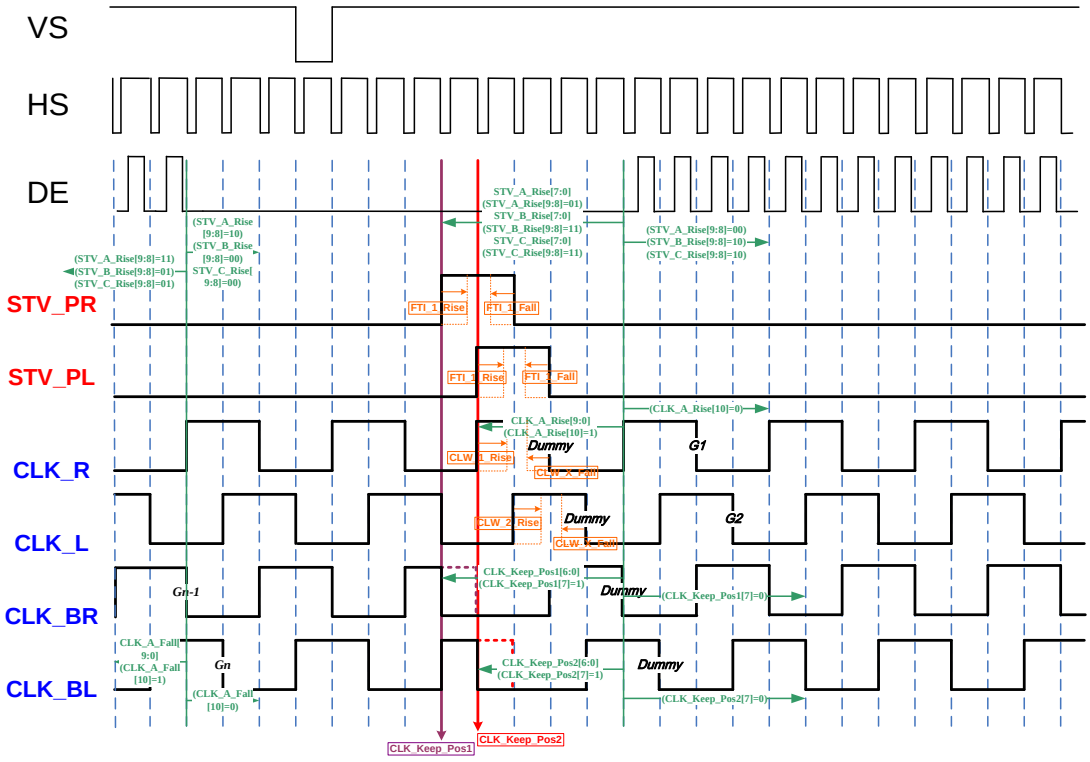
CLK_Keep	Description
0	Not Keep CLK
1	Keep CLK

FTI_n_Rise[7:0] / CLW_n_Rise[7:0] / CLW_x_Fall[7:0] / FTI_n_Fall[7:0] , n = 1 ~ 3

GPM_R_Stage_i[7:0] / GPM_R_Stage_i[7:0] / GPM_F_Stage_i[7:0] / GPM_F_Stage_ii[7:0] :

FTI_n_Rise[7:0] / CLW_n_Rise[7:0] / CLW_x_Fall[7:0] / FTI_n_Fall[7:0] / GPM_R_Stage_i[7:0] / GPM_R_Stage_i[7:0] / GPM_F_Stage_i[7:0] / GPM_F_Stage_ii[7:0]	OP_CLK
8'h00	0 * T_{OP_CLK}
8'h01	2 * T_{OP_CLK}
8'h02	4 * T_{OP_CLK}
:	:
:	:
8'hFE	508 * T_{OP_CLK}
8'hFF	510 * T_{OP_CLK}

Note1 : T_{OP_CLK} : 62.5ns



Notes: CLK_R, CLK_BR will keep VGL between CLK_Keep_Pos1 and CLK_A_Rise setting point.

CLK_L, CLK_BL will keep VGL between CLK_Keep_Pos2 and CLK_B_Rise setting point.

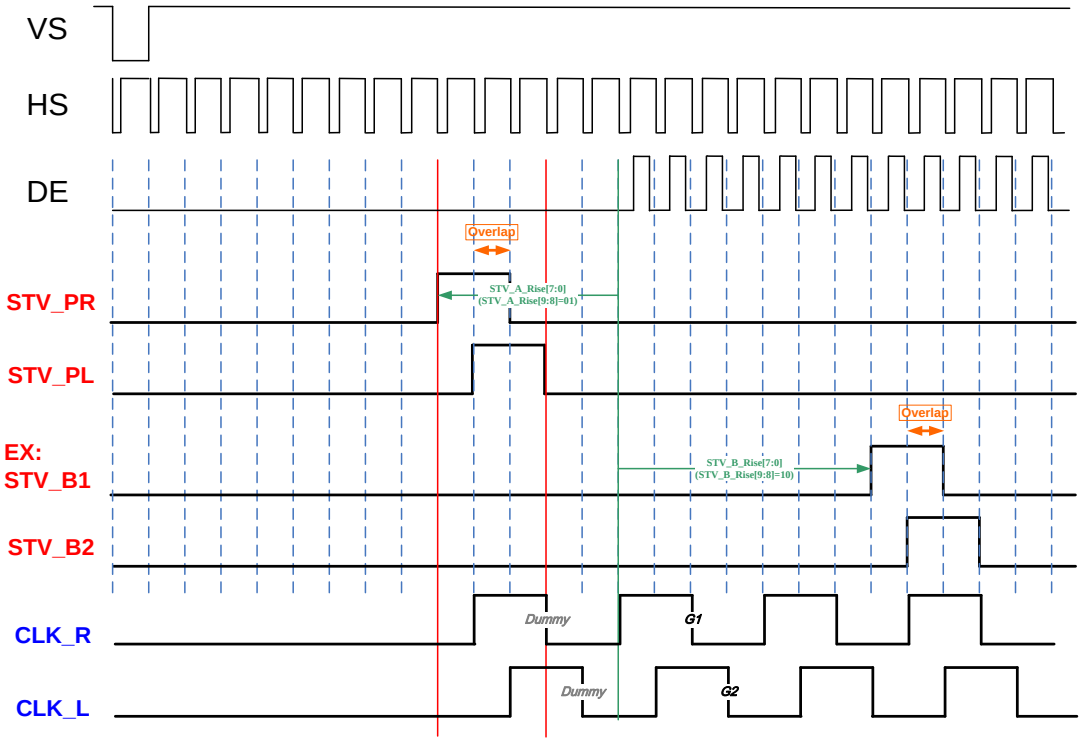
Phase_STV_A[1:0] / Phase_STV_B [1:0] / Phase_STV_C [1:0] :

Phase_STV_A[1:0] / Phase_STV_B [1:0]/ Phase_STV_C[1:0]	Number of CLK
00	1
01	2
10	3
11	4

Overlap_STV_A[2:0] / Overlap _STV_B [2:0] / Overlap _STV_C [2:0]:

Overlap_STV_A[2:0] / Overlap_STV_B[2:0] /Overlap_STV_C[2:0]	Overlap of CLK
000	1H

001	2H
010	3H
011	4H
100	5H
101	6H
110	7H
111	8H

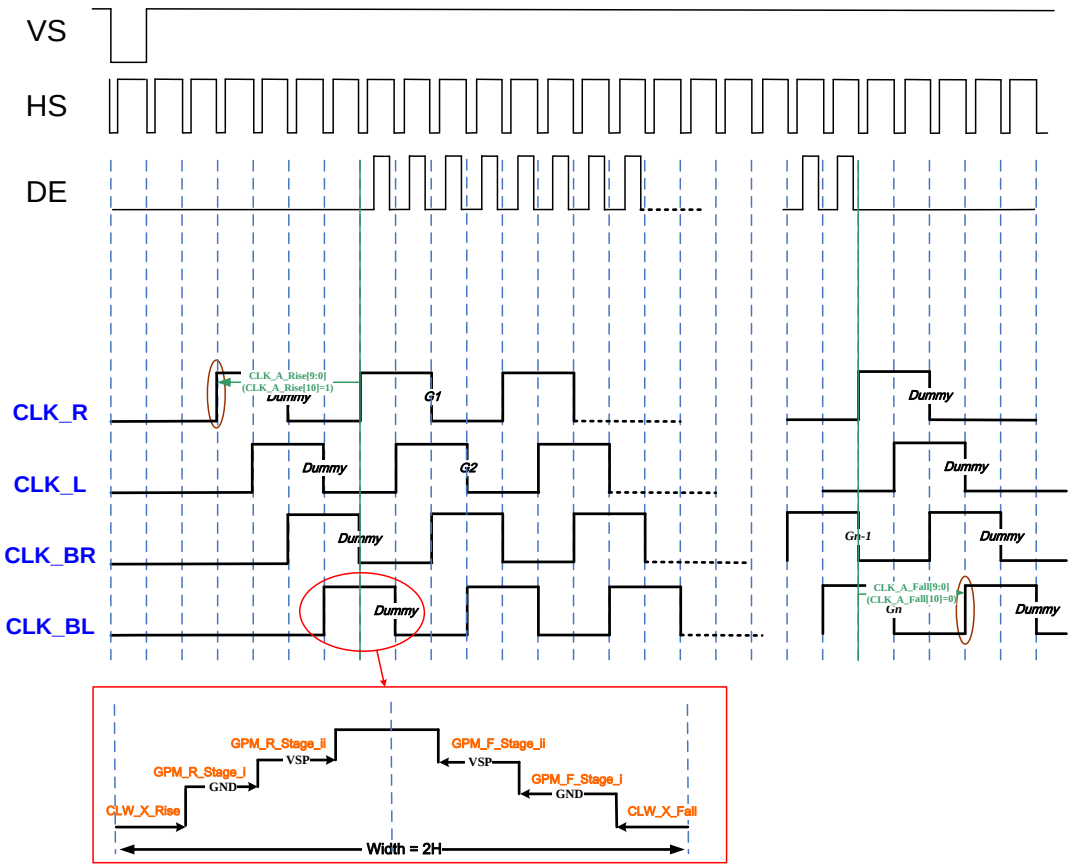


Phase_CLK[2:0] :

Phase_CLK [2:0]	Number of CLK
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Overlap_CLK[1:0] :

Overlap_CLK [2:0]	Overlap of CLK
000	1H
001	2H
010	3H
011	4H
100	5H
101	6H
110	7H
111	8H



Note : CLK_X_Fall:The last clk rising edge position

Restriction	To enable this command, “Page 3 Command Set enable register (FFh) ” must set first.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

5.6.2. GIP Setting 2 (50h~5Dh)

Command Page			Page 3								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
50h	1st	W/R	STV_1_MUX[2:0]				STV_2_MUX[2:0]				-
51h	1st	W/R	STV_3_MUX[2:0]				STV_4_MUX[2:0]				-
52h	1st	W/R	STV_5_MUX[2:0]				STV_6_MUX[2:0]				-
53h	1st	W/R	STV_7_MUX[2:0]				STV_8_MUX[2:0]				-
54h	1st	W/R	STV_9_MUX[2:0]				STV_10_MUX[2:0]				-
55h	1st	W/R	STV_11_MUX[2:0]				STV_12_MUX[2:0]				-
56h	1st	W/R	CLK_1_MUX[2:0]				CLK_2_MUX[2:0]				-
57h	1st	W/R	CLK_3_MUX[2:0]				CLK_4_MUX[2:0]				-
58h	1st	W/R	CLK_5_MUX[2:0]				CLK_6_MUX[2:0]				-
59h	1st	W/R	CLK_7_MUX[2:0]				CLK_8_MUX[2:0]				-
5Ah	1st	W/R	CLK_9_MUX[2:0]				CLK_10_MUX[2:0]				-
5Bh	1st	W/R	CLK_11_MUX[2:0]				CLK_12_MUX[2:0]				-
5Ch	1st	W/R	CLK_13_MUX[2:0]				CLK_14_MUX[2:0]				-
5Dh	1st	W/R	CLK_15_MUX[2:0]				CLK_16_MUX[2:0]				-
Description		Change GIP signal timing output pin map.									
Restriction		To enable this command, “Page 3 Command Set enable register (FFh) ” must set first.									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

5.6.3. GIP Setting 3 (5Eh~8Ah)

Command Page			Page 3								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
5Eh	1st	W/R	Reserve for other setting			BACKWARDS	Reserve for other setting			FORWARDS	-
5Fh	1st	W/R	0			GOUT_01_MUX_FW[4:0]					-
60h	1st	W/R	0			GOUT_02_MUX_FW[4:0]					-
61h	1st	W/R	0			GOUT_03_MUX_FW[4:0]					-
62h	1st	W/R	0			GOUT_04_MUX_FW[4:0]					-
63h	1st	W/R	0			GOUT_05_MUX_FW[4:0]					-
64h	1st	W/R	0			GOUT_06_MUX_FW[4:0]					-
65h	1st	W/R	0			GOUT_07_MUX_FW[4:0]					-
66h	1st	W/R	0			GOUT_08_MUX_FW[4:0]					-
67h	1st	W/R	0			GOUT_09_MUX_FW[4:0]					-
68h	1st	W/R	0			GOUT_10_MUX_FW[4:0]					-
69h	1st	W/R	0			GOUT_11_MUX_FW[4:0]					-
6Ah	1st	W/R	0			GOUT_12_MUX_FW[4:0]					-
6Bh	1st	W/R	0			GOUT_13_MUX_FW[4:0]					-
6Ch	1st	W/R	0			GOUT_14_MUX_FW[4:0]					-
6Dh	1st	W/R	0			GOUT_15_MUX_FW[4:0]					-
6Eh	1st	W/R	0			GOUT_16_MUX_FW[4:0]					-
6Fh	1st	W/R	0			GOUT_17_MUX_FW[4:0]					-
70h	1st	W/R	0			GOUT_18_MUX_FW[4:0]					-
71h	1st	W/R	0			GOUT_19_MUX_FW[4:0]					-
72h	1st	W/R	0			GOUT_20_MUX_FW[4:0]					-
73h	1st	W/R	0			GOUT_21_MUX_FW[4:0]					-
74h	1st	W/R	0			GOUT_22_MUX_FW[4:0]					-
75h	1st	W/R	0			GOUT_01_MUX_BW[4:0]					-
76h	1st	W/R	0			GOUT_02_MUX_BW[4:0]					-
77h	1st	W/R	0			GOUT_03_MUX_BW[4:0]					-
78h	1st	W/R	0			GOUT_04_MUX_BW[4:0]					-
79h	1st	W/R	0			GOUT_05_MUX_BW[4:0]					-
7Ah	1st	W/R	0			GOUT_06_MUX_BW[4:0]					-
7Bh	1st	W/R	0			GOUT_07_MUX_BW[4:0]					-
7Ch	1st	W/R	0			GOUT_08_MUX_BW[4:0]					-
7Dh	1st	W/R	0			GOUT_09_MUX_BW[4:0]					-
7Eh	1st	W/R	0			GOUT_10_MUX_BW[4:0]					-
7Fh	1st	W/R	0			GOUT_11_MUX_BW[4:0]					-
80h	1st	W/R	0			GOUT_12_MUX_BW[4:0]					-
81h	1st	W/R	0			GOUT_13_MUX_BW[4:0]					-
82h	1st	W/R	0			GOUT_14_MUX_BW[4:0]					-
83h	1st	W/R	0			GOUT_15_MUX_BW[4:0]					-
84h	1st	W/R	0			GOUT_16_MUX_BW[4:0]					-
85h	1st	W/R	0			GOUT_17_MUX_BW[4:0]					-
86h	1st	W/R	0			GOUT_18_MUX_BW[4:0]					-
87h	1st	W/R	0			GOUT_19_MUX_BW[4:0]					-
88h	1st	W/R	0			GOUT_20_MUX_BW[4:0]					-
89h	1st	W/R	0			GOUT_21_MUX_BW[4:0]					-
8Ah	1st	W/R	0			GOUT_22_MUX_BW[4:0]					-

Description

BACKWARDS : Backward Scan Exchange Mode.

BACKWARDS	Description
0	Original
1	Exchange

FORWARDS : Forward Scan Exchange Mode.

FORWARDS	Description
0	Original
1	Exchange

GOUT_XX_MUX_FW[4:0] / GOUT_XX_MUX_BW[4:0] : These setting are the output status of GOUT[1:44].

GOUT_XX_MUX_FW[4:0] / GOUT_XX_MUX_BW[4:0]	Description
00h	If the GS=0, the setting is VGL, or if GS=1, the setting is VGH
01h	If the GS=0, the setting is VGH, or if GS=1, the setting is VGL
02h	VGL
03h	GND
04h	VSP
05h	VGH
06h	MUX2_STVA1_OUT
07h	MUX2_STVA3_OUT
08h	MUX2_STVB1_OUT
09h	MUX2_STVB3_OUT
0Ah	MUX2_STVC1_OUT
0Bh	MUX2_STVC3_OUT
0Ch	MUX2_CLKA1_OUT
0Dh	MUX2_CLKA3_OUT
0Eh	MUX2_CLKA5_OUT
0Fh	MUX2_CLKA7_OUT
10h	MUX2_CLKA9_OUT
11h	MUX2_CLKA11_OUT
12h	MUX2_CLKA13_OUT
13h	MUX2_CLKA15_OUT
14h	reserved
15h	reserved
16h	reserved
17h	reserved

Note : XX mean from 01 to 22.

Restriction	To enable this command, “Page 3 Command Set enable register (FFh) ” must set first.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

5.6.4. EXTC Command Set Enable Register (FFh)

Command Page			Page 3								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								03h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	03h
S/W Reset	03h
H/W Reset	03h

5.7. Page 4 Command Description

5.7.1. DSI Lanes Control (00h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
00h	1st	W/R	MIPI_LANE_SEL	0	0	0	0	0	0	0	80h
Description			**MIPI_LANE_SEL:** MIPI DSI lane number selection *Note: When use this setting, please reference to chapter 4.1 "DSI System Interface".*								
Restriction			None								
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	80h
S/W Reset	80h
H/W Reset	80h

5.7.2. SSC Function (0Bh,0Eh)

<table>
<tr><th colspan="2">Command Page</th><th></th><th colspan="9">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th colspan="3">D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>0Bh</td><td>1st</td><td>W/R</td><td>SSC_DIG_EN</td><td colspan="4">SSC_DIG_STEP[2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>0Eh</td><td>1st</td><td>W/R</td><td colspan="9">SSC_DIG_CNT[7:0]</td><td>00h</td></tr>
<tr><td colspan="2">Description</td><td colspan="11">SSC_DIG_EN : Enable/disable the SSC(Spread Spectrum Clock) function.
SSC_DIG_STEP[2:0] : Set SSC parameter.
SSC_DIG_CNT[7:0] : Set SSC parameter.
<table>
<tr><th>SSC</th><th>Address 0Bh</th><th>Address 0Eh</th></tr>
<tr><td>±1%</td><td>80h</td><td>17h</td></tr>
<tr><td>±2%</td><td>90h</td><td>0Bh</td></tr>
<tr><td>Others</td><td>Reserved</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="11">None</td></tr>
<tr><td colspan="2">Register Availability</td><td colspan="11">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td colspan="2">Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h_00h</td></tr>
<tr><td>S/W Reset</td><td>00h_00h</td></tr>
<tr><td>H/W Reset</td><td>00h_00h</td></tr>
</table></td></tr>
</table>

5.7.3. Charge-Pump Setting (21h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
21h	1st	W/R	DMY_PUMP	0	1	1	0	0	0	0	B0h

Description

DMY_PUMP: Control the driver behavior when host stop transferring video data.

DMY_PUMP	Description
0	Charge-Pump VGH/VGL keep pumping and display shows smallest gamma voltage
1	Charge-Pump VGH/VGL keep pumping

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	B0h
S/W Reset	B0h
H/W Reset	B0h

5.7.4. Internal SD Timing Control (26h)

<table>
<tr><th colspan="3">Command Page</th><th colspan="8">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>26h</td><td>1st</td><td>W/R</td><td colspan="4">DET_TOLERANCE_OP[3:0]</td><td>0</td><td>1</td><td>1</td><td>0</td><td>76h</td></tr>
<tr><td>Description</td><td colspan="10">DET_TOLERANCE_OP[3:0]: Control internal SD timing between latch1 load into latch2.
<table><tr><th>DET_TOLERANCE_OP[3:0]</th><th>Description</th></tr><tr><td>0000</td><td>62.5ns x 1</td></tr><tr><td>0001</td><td>62.5ns x 2</td></tr><tr><td>…</td><td>…</td></tr><tr><td>1111</td><td>62.5ns x 16</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">None</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>76h</td></tr><tr><td>S/W Reset</td><td>76h</td></tr><tr><td>H/W Reset</td><td>76h</td></tr></table></td></tr>
</table>

5.7.5. Touch Synchronization Timing Adjust (27h~2Ah)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
27h	1st	W/R	TOUCH_OPT[1:0]		VSOD[1:0]		HSOM[1:0]		HFP_HBP_OPT	VS_PW_OPT	00h
28h	1st	W/R	HSOD[7:0]								05h
29h	1st	W/R	HSOHW[7:0]								19h
2Ah	1st	W/R	VS_OUT_EN	HS_OUT_EN	VS_OUT_POL	HS_OUT_POL	0	0	STB_EN	0	F0h

Description

This command controls the synchronization output. This function is able to use when Page1_R29h=01h.

TOUCH_OPT[1:0]: Select the Output Mode of synchronization (time scale: internal T_{OP_CLK})

TOUCH_OPT[1:0]	Description
0h	Off
1h	VFP+VBP
2h	Adjustable for VSOUT / HSOUT(Note 2)
3h	VFP+VBP / HFP+HBP

VSOD[1:0]: Set the VSOUT delay timing (time scale: internal T_{OP_CLK})

VSOD[1:0]	Description
0h	0 line (First line of back porch)
1h	1 line
2h	2 line
3h	3 line

HSOM[1:0]: Set the HSOUT active period (time scale: internal T_{OP_CLK})

HSOM[1:0]	Description
0h	VACT Period + VFP + VBP
1h	VACT Period
2h	VFP+VBP
3h	Reserved

HFP_HBP_OPT: Select the output source for HSOUT

HFP_HBP_OPT	Description
0	Prebuf-Source
1	HSOUT(Note 2)

VS_PW_OPT: Set the pulse width of VSOUT

VS_PW_OPT	Description
0	pulse width = 1H
1	During transition from display off to display on : pulse width = 3H During transition from display on to display off : pulse width = 2H Otherwise : pulse width = 1H

HSOD[7:0]: Set HSOUT delay timing (time scale: internal T_{OP_CLK})

HSOD[1:0]	Description
0h	0clk
1h	1clk
2h	2clk
:	:
FDh	253clk
FEh	254clk
FFh	255clk

HSOHW[7:0]: Set the high width of HSOUT (time scale: internal T_{OP_CLK})

HSOHW[1:0]	Description
0h	Reserved
1h	1clk
2h	2clk
:	:
FDh	253clk
FEh	254clk
FFh	255clk

VS_OUT_EN: VS signal output enable (1: enable, 0: disable)

HS_OUT_EN: HS signal output enable (1: enable, 0: disable)

VS_OUT_POL: VS signal polarity (1: non-inversion, 0: inversion)

HS_OUT_POL: HS signal polarity (1: non-inversion, 0: inversion)

STB_EN: touch option

Note 1: T_{OP_CLK}: 32ns

Note 2: When use this setting, please reference to chapter 16 "Touch Synchronization Signal".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_05h_19h_F0h
S/W Reset	00h_05h_19h_F0h
H/W Reset	00h_05h_19h_F0h

5.7.6. BIST Mode Function (2Dh,2Fh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
2Dh	1st	W/R	FRM_PT[7:0]								FFh
2Fh	1st	W/R	0	0	FRM_CYC[1:0]		0	0	0	FRM_EN	00h

Description

FRM_PT[7:0]: Enable/disable the pattern

FRM_PT[7:0]	Pattern
FRM_PT[0]	White
FRM_PT[1]	Black
FRM_PT[2]	Red
FRM_PT[3]	Green
FRM_PT[4]	Blue
FRM_PT[5]	Gray128
FRM_PT[6]	Gray127
FRM_PT[7]	V-Color bar

See also sections:"7 BIST Mode Function "

FRM_CYC[1:0]: Set scan cycle of each pattern

FRM_CYC[1:0]	Description
0h	64 frames
1h	128 frames
2h	256 frames
3h	512 frames

FRM_EN: Enable/disable BIST mode function

FRM_EN	Description
0	Normal display
1	Enable BIST mode

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh_00h
S/W Reset	FFh_00h
H/W Reset	FFh_00h

5.7.7. Source Timing Setting (35h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
35h	1st	W/R	0	0	0	1	HZ_OPT	1	1	1	17h

Description

HZ_OPT: Maximum source OP drive time.

HZ_OPT	Description
0	Disable
1	Enable (Before enable this function , set Page4_R3Ah_D[7]=0)

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	17h
S/W Reset	17h
H/W Reset	17h

5.7.8. Power Saving Control (3Ah)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>3Ah</td><td>1st</td><td>W/R</td><td>PS_EN</td><td colspan="7">PCST[6:0]</td><td>A4h</td></tr>
<tr><td>Description</td><td colspan="11">PS_EN: Source power saving enable
<table><tr><th>PS_EN</th><th>Description</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>PCST[6:0]: Control power saving period
<table><tr><th>PCST[6:0]</th><th>Description</th></tr><tr><td>0000000</td><td>62.5ns x 1</td></tr><tr><td>0000001</td><td>62.5ns x 2</td></tr><tr><td>0000010</td><td>62.5ns x 3</td></tr><tr><td>…</td><td>…</td></tr><tr><td>0100100</td><td>62.5ns x 37</td></tr><tr><td>Others</td><td>Inhibited</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>A4h</td></tr><tr><td>S/W Reset</td><td>A4h</td></tr><tr><td>H/W Reset</td><td>A4h</td></tr></table></td></tr>
</table>

5.7.9. Power Control 1 (69h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
69h	1st	W/R	1	CP_VCL_CLP_OPTION_PRE[2:0]			0	1	1	1	D7h

Description

CP_VCL_CLP_OPTION_PRE[2:0]: Set VCL clamp level.

CP_VCL_CLP_OPTION_PRE[2:0]	VCL clamp level (V)
0h	-3.0V
1h	-2.9V
2h	-2.8V
3h	-2.7V
4h	-2.6V
5h	-2.5V
6h	-2.4V
7h	-2.3V

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	D7h
S/W Reset	D7h
H/W Reset	D7h

5.7.10. Power Control 2 (6Eh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
6Eh	1st	W/R	0	DI_PWR_REG	REG1_VRH_CP[5:0]						6Ah

Description

DI_PWR_REG: Select the input power mode.

DI_PWR_REG	BOOSTM2	BOOSTM1	BOOSTM0	Note
0	0	0	1	Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) *Note 1*
1	0	0	1	Power Mode 4 External VDDI, VCI, VSP and VSN
X	0	1	0	Power Mode 3 External VDDI and VCI (ILI4003)
prohibited				-

Note 1: VCI and VSP pads must be connected by external metal path.

REG1_VRH_CP[5:0]: Set VGH clamp level. (0.18V/step)

REG1_VRH_CP[5:0]	VGH clamp level (V)
03h	7.98
04h	8.16
05h	8.34
06h	8.52
07h	8.7
08h	8.88
:	:
29h	14.82
2Ah	15
2Bh	15.18
:	:
39h	17.7
3Ah	17.88
3Bh	18.06
Other	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	6Ah
S/W Reset	6Ah
H/W Reset	6Ah

5.7.11. Power Control 3 (6Fh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
6Fh	1st	W/R	0	DI_CP_VGH_BH[2:0]			DI_CP_VGL_BL[2:0]			0	34h

Description

DI_CP_VGH_BH[2:0]: Set the factor used in the step-up circuits for VGH.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

DI_CP_VGH_BH[2:0]	VGH Output (power mode 3, 4)	VGH Output (power mode 2A)	Flying Capacitor
0h	Reserved	Reserved	-
1h	2*VSP	2*VSP	C21P/N + C22P/N (option)
2h	2.5*VSP	3*VSP	C21P/N + C22P/N (option)
3h	3*VSP	3*VSP	C21P/N + C22P/N (option)
4h	3.5*VSP	4*VSP	C21P/N + C22P/N
5h	4*VSP	4*VSP	C21P/N + C22P/N
6h	4.5*VSP	5*VSP	C21P/N + C22P/N
7h	5*VSP	5*VSP	C21P/N + C22P/N

DI_CP_VGL_BL[2:0]: Set the factor used in the step-up circuits for VGL. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

DI_CP_VGL_BL[2:0]	VGL Output (power mode 3, 4)	VGL Output (power mode 2A)	Flying Capacitor
0h	-1.5*VSP	-2*VSP	C23P/N + C24P/N (option)
1h	-2*VSP	-2*VSP	C23P/N + C24P/N (option)
2h	-2.5*VSP	-3*VSP	C23P/N + C24P/N (option)
3h	-3*VSP	-3*VSP	C23P/N + C24P/N (option)
4h	-3.5*VSP	-4*VSP	C23P/N + C24P/N
5h	-4*VSP	-4*VSP	C23P/N + C24P/N
6h	-4.5*VSP	-5*VSP	C23P/N + C24P/N
7h	-5*VSP	-5*VSP	C23P/N + C24P/N

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	34h
S/W Reset	34h
H/W Reset	34h

5.7.12. VREG1/2 Setting (7Ah)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
7Ah	1st	W/R	0	0	0	DI_REG_REG1_EN_CAP	0	0	0	0	00h

Description

DI_REG_REG1_EN_CAP: Using VREG1/2 external caps(1uF) enable

DI_REG_REG1_EN_CAP	Description
1	IC uses VREG1/2 caps(1uF) at FPC
0	IC doesn't use VREG1/2 caps(1uF) at FPC

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

5.7.13. LVD Function 1 (87h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
87h	1st	W/R	DI_LVD_CTL[3:0]				1	0	1	0	BAh

Description

DI_LVD_CTL[3:0]: The sensitivity adjustment of detecting when battery is removed and power voltage is low.

DI_LVD_CTL[3:0]	Description
1111	sensitivity high
1011	sensitivity medium
0010	sensitivity low
0000	disable detecting
Others	Inhibited

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	BAh
S/W Reset	BAh
H/W Reset	BAh

5.7.14. LVD Function 2 (88h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
88h	1st	W/R	DIS_LVD_CHK	0	0	0	1	0	1	1	8Bh

Description

DIS_LVD_CHK: LVD check function control.

DIS_LVD_CHK	Description
0	When LVD is detected, IC will directly turn off pump power and go into sleep in sequence
1	When LVD is detected, IC will go into normal power-off/sleep in sequence

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8Bh
S/W Reset	8Bh
H/W Reset	8Bh

5.7.15. VCOM Control (8Bh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Bh	1st	W/R	1	1	1	0	DI_VCM_SEL0_EN	0	1	1	E3h

Description

DI_VCM_SEL0_EN: Set the VCOM output mode.

DI_VCM_SEL0_EN	GS_PANEL Note	VCOM output mode
0	0	Set VCOM level by VCM1[8:0]
0	1	Set VCOM level by VCM2[8:0]
1	0	VCOM = 0V
1	1	VCOM = 0V

Note: Please reference"5.4.2 Set Panel Operation Mode and Data Complement Setting (22h)"

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	E3h
S/W Reset	E3h
H/W Reset	E3h

5.7.16. Power Control 4 (8Ch~8Dh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
8Dh	1st	W/R	0	DI_VCOM_CP_VGLCLP[6:0]							14h

Description

DI_VCOM_CP_VGLCLP[6:0]: Set VGL clamp level. (0.18V/step)

DI_VCOM_CP_VGLCLP[6:0]	VGL clamp level (V)
03h	-6.99
04h	-7.17
05h	-7.35
06h	-7.53
07h	-7.71
08h	-7.89
09h	-8.07
0Ah	-8.25
0Bh	-8.43
0Ch	-8.61
0Dh	-8.79
0Eh	-8.97
0Fh	-9.15
10h	-9.33
11h	-9.51
12h	-9.69
13h	-9.87
14h	-10.05
15h	-10.23
:	:
3Fh	-17.79
40h	-17.97
41h	-18.15
Others	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	14h
S/W Reset	14h
H/W Reset	14h

5.7.17. Reload Gamma Setting (B2h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="10">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>B2h</td><td>1st</td><td>W/R</td><td>RELOAD_GMA_EN</td><td>RELOAD_GMA_LINE8_EN</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>D1h</td></tr>
<tr><td>Description</td><td colspan="11">RELOAD_GMA_EN: Gamma setting reload enable when IC operates at sleep-out state.
<table><tr><th>RELOAD_GMA_EN</th><th>Description</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>
RELOAD_GMA_LINE8_EN: Gamma setting reload at the period of 8 line when IC operates at sleep-out state.
<table><tr><th>RELOAD_GMA_LINE8_EN</th><th>Description</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="11">None</td></tr>
<tr><td>Register Availability</td><td colspan="11"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>D1h</td></tr><tr><td>S/W Reset</td><td>D1h</td></tr><tr><td>H/W Reset</td><td>D1h</td></tr></table></td></tr>
</table>

5.7.18. Gamma Bias Level (B5h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
B5h	1st	W/R	0	0	0	0	0	DI_GMA_GAP[2:0]			02h

Description

DI_GMA_GAP[2:0]: Control the gamma bias level.

DI_GMA_GAP[2:0]	Description
111	High
110	Medium High
010	Default value
Others	inhibited

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	02h
S/W Reset	02h
H/W Reset	02h

5.7.19. Temperature Detecting Setting 1 (BBh~C2h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
BBh	1st	W/R	EN_TEMP_PROCESS	0	CP_VGH_TAP_C[5:0]						1Eh
BCh	1st	W/R	0	0	CP_VGH_TAP_L[5:0]						1Eh
BDh	1st	W/R	0	0	CP_VGH_TAP_M[5:0]						1Eh
BEh	1st	W/R	0	0	CP_VGH_TAP_H[5:0]						1Eh
BFh	1st	W/R	VCOM_C[7:0]								4Ch
C0h	1st	W/R	VCOM_L[7:0]								4Ch
C1h	1st	W/R	VCOM_M[7:0]								4Ch
C2h	1st	W/R	VCOM_H[7:0]								4Ch

Description

EN_TEMP_PROCESS / EN_TS: Enable/Disable Temperature Detecting function.

EN_TEMP_PROCESS	EN_TS	Function
0	0	Disable
1	1	Enable
Other		Reserved

CP_VGH_TAP_C[5:0]: Set VGH clamp level for Temp_Cold. (0.18V/step)

CP_VGH_TAP_L[5:0]: Set VGH clamp level for Temp_Low. (0.18V/step)

CP_VGH_TAP_M[5:0]: Set VGH clamp level for Temp_Middle. (0.18V/step)

CP_VGH_TAP_H[5:0]: Set VGH clamp level for Temp_High. (0.18V/step)

CP_VGH_TAP_C[5:0] CP_VGH_TAP_L[5:0] CP_VGH_TAP_M[5:0] CP_VGH_TAP_H[5:0]	VGH clamp level (V)
03h	7.98
04h	8.16
05h	8.34
06h	8.52
07h	8.7
08h	8.88
:	:
28h	14.64
29h	14.82
2Ah	15
2Bh	15.18
2Ch	15.36
:	:
37h	17.34
38h	17.52
39h	17.7
3Ah	17.88
3Bh	18.06
Other	Reserved

VCOM_C[8:0]: Set the VCOM level for Temp_Cold.

VCOM_L[8:0]: Set the VCOM level for Temp_Low.

VCOM_M[8:0]: Set the VCOM level for Temp_Middle.

VCOM_H[8:0]: Set the VCOM level for Temp_High.

VCOM_C[8:0] VCOM_L[8:0] VCOM_M[8:0] VCOM_H[8:0]	VCOM voltage (V)
010h	-0.204
011h	-0.216
012h	-0.228
013h	-0.24
014h	-0.252
015h	-0.264
:	:
07Ah	-1.476
07Bh	-1.488
07Ch	-1.5
:	:
149h	-3.96
14Ah	-3.972
14Bh	-3.984
14Ch	-3.996
14Dh	-4.008
Others	Reserved

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch
S/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch
H/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch

5.7.20. Read VCOM OTP Data (C4h~C7h)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C4h	1st	R	0	0	0	0	0	0	0	OTP_VCM1[8]	00h
C5h	1st	R	OTP_VCM1[7:0]								7Bh
C6h	1st	R	0	0	0	0	0	0	0	OTP_VCM2[8]	00h
C7h	1st	R	OTP_VCM2[7:0]								7Bh

Description

OTP_VCM1[8:0]: Read the VCOM1 OTP data used for vertical forward scan (GS_PANEL= 1'b0), when NV memory is programmed. (12mV/step)

OTP_VCM2[8:0]: Read the VCOM2 OTP data used for vertical backward scan (GS_PANEL= 1'b1), when NV memory is programmed. (12mV/step)

OTP_VCM1[8:0] OTP_VCM2[8:0]	VCOM voltage (V)
010h	-0.204
011h	-0.216
012h	-0.228
013h	-0.24
014h	-0.252
015h	-0.264
:	:
07Ah	-1.476
07Bh	-1.488
07Ch	-1.5
:	:
149h	-3.96
14Ah	-3.972
14Bh	-3.984
14Ch	-3.996
14Dh	-4.008
Others	Reserved

Note: VCOM ≧ VSN + 0.5V

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_7Bh_00h_7Bh
S/W Res t	00h_7Bh_00h_7Bh
H/W Reset	00h_7Bh_00h_7Bh

5.7.21. Temperature Detecting Setting 2 (C8h~CEh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
C8h	1st	W/R	TS_TH0[7:0]								00h
C9h	1st	W/R	TS_TH1[7:0]								00h
CAh	1st	W/R	TS_TH2[7:0]								00h
CBh	1st	W/R	TS_TH3[7:0]								00h
CCh	1st	W/R	TS_TH0[9:8]		TS_TH1[9:8]		TS_TH2[9:8]		TS_TH3[9:8]		00h
CDh	1st	W/R	TS_DEBT_OPT[3:0]				TS_HYST_OPT[3:0]				02h
CEh	1st	W/R	EN_TS	VCOM_C[8]	VCOM_L[8]	VCOM_M[8]	VCOM_H[8]	1	0	0	04h

Description

TS_TH0[9:0]: Set the temperature detecting range threshold for Temp_Cold.

TS_TH1[9:0]: Set the temperature detecting range threshold for Temp_Low.

TS_TH2[9:0]: Set the temperature detecting range threshold for Temp_Middle.

TS_TH3[9:0]: Set the temperature detecting range threshold for Temp_High.

TS_DEBT_OPT[3:0]: Set the de-bounce of temperature detecting range.

TS_HYST_OPT[3:0]: Set the hysteresis of temperature detecting range.

Restriction

None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h _00h _00h _00h _02h _04h
S/W Reset	00h_00h _00h _00h _00h _02h _04h
H/W Reset	00h_00h _00h _00h _00h _02h _04h

5.7.22. OTP Control (D7h)

<table>
<tr><th colspan="2">Command Page</th><th colspan="9">Page 4</th></tr>
<tr><th>Address</th><th>Parameter</th><th>W/R</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Default</th></tr>
<tr><td>D7h</td><td>1st</td><td>W/R</td><td>0</td><td>0</td><td>0</td><td>OTP_PATH</td><td colspan="2">PROG_SEL[1:0]</td><td>0</td><td>0</td><td>1Ch</td></tr>
<tr><td colspan="2">Description</td><td colspan="10">OTP_PATH:
<table><tr><th>OTP_PATH</th><th>Description</th></tr><tr><td>0</td><td>Internal VGH Programming</td></tr><tr><td>1</td><td>External MTP_PWR Programming</td></tr></table>PROG_SEL[1:0]:
<table><tr><th>PROG_SEL[1:0]</th><th>Description</th></tr><tr><td>0h</td><td>Inhibited</td></tr><tr><td>1h</td><td>Internal Programming Setting (Best Setting)</td></tr><tr><td>2h</td><td>Inhibited</td></tr><tr><td>3h</td><td>Internal Programming Setting (Default)</td></tr></table></td></tr>
<tr><td colspan="2">Restriction</td><td colspan="10">None</td></tr>
<tr><td colspan="2">Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td colspan="2">Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>1Ch</td></tr><tr><td>S/W Reset</td><td>1Ch</td></tr><tr><td>H/W Reset</td><td>1Ch</td></tr></table></td></tr>
</table>

5.7.23. EXTC Command Set Enable Register (FFh)

Command Page			Page 4								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								04h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

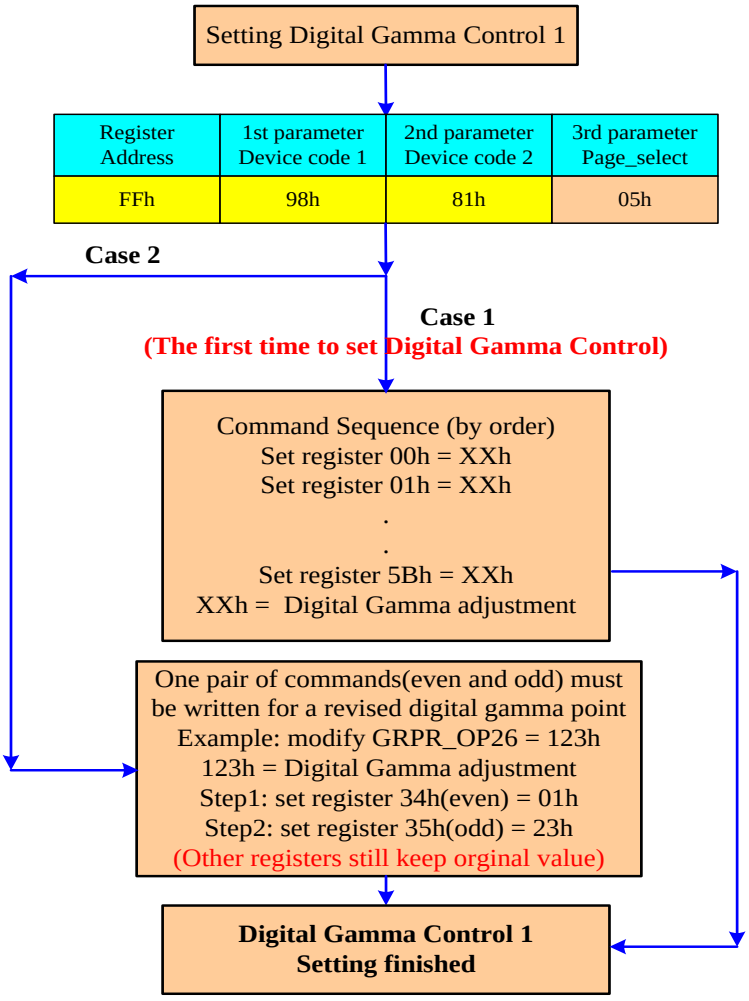
Status	Default Value
Power On Sequence	04h
S/W Reset	04h
H/W Reset	04h

5.8. Page 5 Command Description

5.8.1. Fine Digital Gamma Control 1 (00h~5Bh)

Command Page			Page 5								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W/R	FineOffsetR00[5:0]						GRPR_OP0[9:8]		XX
01h	1st	W/R	GRPR_OP0[7:0]								XX
02h	1st	W/R	FineOffsetR01[5:0]						GRPR_OP1[9:8]		XX
03h	1st	W/R	GRPR_OP1[7:0]								XX
04h	1st	W/R	FineOffsetR02[5:0]						GRPR_OP2[9:8]		XX
05h	1st	W/R	GRPR_OP2[7:0]								XX
06h	1st	W/R	FineOffsetR03[5:0]						GRPR_OP3[9:8]		XX
07h	1st	W/R	GRPR_OP3[7:0]								XX
08h	1st	W/R	FineOffsetR04[5:0]						GRPR_OP4[9:8]		XX
09h	1st	W/R	GRPR_OP4[7:0]								XX
0Ah	1st	W/R	FineOffsetR05[5:0]						GRPR_OP5[9:8]		XX
0Bh	1st	W/R	GRPR_OP5[7:0]								XX
0Ch	1st	W/R	FineOffsetR06[5:0]						GRPR_OP6[9:8]		XX
0Dh	1st	W/R	GRPR_OP6[7:0]								XX
0Eh	1st	W/R	FineOffsetR07[5:0]						GRPR_OP7[9:8]		XX
0Fh	1st	W/R	GRPR_OP7[7:0]								XX
10h	1st	W/R	FineOffsetR08[5:0]						GRPR_OP8[9:8]		XX
11h	1st	W/R	GRPR_OP8[7:0]								XX
12h	1st	W/R	FineOffsetR09[5:0]						GRPR_OP9[9:8]		XX
13h	1st	W/R	GRPR_OP9[7:0]								XX
14h	1st	W/R	FineOffsetR10[5:0]						GRPR_OP10[9:8]		XX
15h	1st	W/R	GRPR_OP10[7:0]								XX
16h	1st	W/R	FineOffsetR11[5:0]						GRPR_OP11[9:8]		XX
17h	1st	W/R	GRPR_OP11[7:0]								XX
18h	1st	W/R	FineOffsetR12[5:0]						GRPR_OP12[9:8]		XX
19h	1st	W/R	GRPR_OP12[7:0]								XX
1Ah	1st	W/R	FineOffsetR13[5:0]						GRPR_OP13[9:8]		XX
1Bh	1st	W/R	GRPR_OP13[7:0]								XX
1Ch	1st	W/R	FineOffsetR14[5:0]						GRPR_OP14[9:8]		XX
1Dh	1st	W/R	GRPR_OP14[7:0]								XX
1Eh	1st	W/R	FineOffsetR15[5:0]						GRPR_OP15[9:8]		XX
1Fh	1st	W/R	GRPR_OP15[7:0]								XX
20h	1st	W/R	FineOffsetR16[5:0]						GRPR_OP16[9:8]		XX
21h	1st	W/R	GRPR_OP16[7:0]								XX
22h	1st	W/R	FineOffsetR17[5:0]						GRPR_OP17[9:8]		XX
23h	1st	W/R	GRPR_OP17[7:0]								XX
24h	1st	W/R	FineOffsetR18[5:0]						GRPR_OP18[9:8]		XX
25h	1st	W/R	GRPR_OP18[7:0]								XX
26h	1st	W/R	FineOffsetR19[5:0]						GRPR_OP19[9:8]		XX
27h	1st	W/R	GRPR_OP19[7:0]								XX
28h	1st	W/R	FineOffsetR20[5:0]						GRPR_OP20[9:8]		XX
29h	1st	W/R	GRPR_OP20[7:0]								XX
2Ah	1st	W/R	FineOffsetR21[5:0]						GRPR_OP21[9:8]		XX
2Bh	1st	W/R	GRPR_OP21[7:0]								XX
2Ch	1st	W/R	FineOffsetR22[5:0]						GRPR_OP22[9:8]		XX
2Dh	1st	W/R	GRPR_OP22[7:0]								XX
2Eh	1st	W/R	FineOffsetR23[5:0]						GRPR_OP23[9:8]		XX
2Fh	1st	W/R	GRPR_OP23[7:0]								XX
30h	1st	W/R	FineOffsetR24[5:0]						GRPR_OP24[9:8]		XX
31h	1st	W/R	GRPR_OP24[7:0]								XX
32h	1st	W/R	FineOffsetR25[5:0]						GRPR_OP25[9:8]		XX

33h	1st	W/R	GRPR_OP25[7:0]								XX
34h	1st	W/R	FineOffsetR26[5:0]						GRPR_OP26[9:8]		XX
35h	1st	W/R	GRPR_OP26[7:0]								XX
36h	1st	W/R	FineOffsetR27[5:0]						GRPR_OP27[9:8]		XX
37h	1st	W/R	GRPR_OP27[7:0]								XX
38h	1st	W/R	FineOffsetR28[5:0]						GRPR_OP28[9:8]		XX
39h	1st	W/R	GRPR_OP28[7:0]								XX
3Ah	1st	W/R	0	0	0	0	0	0	GRPR_OP29[9:8]		XX
3Bh	1st	W/R	GRPR_OP29[7:0]								XX
3Ch	1st	W/R	0	0	0	0	0	0	GRPR_OP30[9:8]		XX
3Dh	1st	W/R	GRPR_OP30[7:0]								XX
3Eh	1st	W/R	0	0	0	0	0	0	GRPR_OP31[9:8]		XX
3Fh	1st	W/R	GRPR_OP31[7:0]								XX
40h	1st	W/R	0	0	0	0	0	0	GRPR_OP32[9:8]		XX
41h	1st	W/R	GRPR_OP32[7:0]								XX
42h	1st	W/R	0	0	0	0	0	0	GRPR_OP33[9:8]		XX
43h	1st		GRPR_OP33[7:0]								XX
44h	1st	W/R	0	0	0	0	0	0	GRPR_OP34[9:8]		XX
45h	1st		GRPR_OP34[7:0]								XX
46h	1st	W/R	0	0	0	0	0	0	GRPR_OP35[9:8]		XX
47h	1st	W/R	GRPR_OP35[7:0]								XX
48h	1st	W/R	0	0	0	0	0	0	GRPR_OP36[9:8]		XX
49h	1st	W/R	GRPR_OP36[7:0]								XX
4Ah	1st	W/R	0	0	0	0	0	0	GRPR_OP37[9:8]		XX
4Bh	1st	W/R	GRPR_OP37[7:0]								XX
4Ch	1st	W/R	0	0	0	0	0	0	GRPR_OP38[9:8]		XX
4Dh	1st	W/R	GRPR_OP38[7:0]								XX
4Eh	1st	W/R	0	0	0	0	0	0	GRPR_OP39[9:8]		XX
4Fh	1st	W/R	GRPR_OP39[7:0]								XX
50h	1st	W/R	0	0	0	0	0	0	GRPR_OP40[9:8]		XX
51h	1st	W/R	GRPR_OP40[7:0]								XX
52h	1st	W/R	0	0	0	0	0	0	GRPR_OP41[9:8]		XX
53h	1st	W/R	GRPR_OP41[7:0]								XX
54h	1st	W/R	0	0	0	0	0	0	GRPR_OP42[9:8]		XX
55h	1st	W/R	GRPR_OP42[7:0]								XX
56h	1st	W/R	0	0	0	0	0	0	GRPR_OP43[9:8]		XX
57h	1st	W/R	GRPR_OP43[7:0]								XX
58h	1st	W/R	0	0	0	0	0	0	GRPR_OP44[9:8]		XX
59h	1st	W/R	GRPR_OP44[7:0]								XX
5Ah	1st	W/R	0	0	0	0	0	0	GRPR_OP45[9:8]		XX
5Bh	1st	W/R	GRPR_OP45[7:0]								XX
FFh	1st	W	1	0	0	1	1	0	0	0	98
	2nd	W	1	0	0	0	0	0	0	1	81
	3rd	W	Page[7:0]								05
Description			**GRPR_OP0[9:0]~GRPR_OP45[9:0]:** Digital Gamma Macro-adjustment registers for red gamma curve.								



Restriction	None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_...00h_00h
S/W Reset	00h_00h_...00h_00h
H/W Reset	00h_00h_...00h_00h

5.8.2. Digital 3 Gamma Enable (85h)

Command Page			Page 5								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
85h	1st	W/R	0	1	0	0	EN_3G	0	0	0	40h
Description		**En_3G:** 0 : digital 3 gamma disable 1 : digital 3 gamma enable									
Restriction		None									
Register Availability											

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before OTP program)
Power On Sequence	40h
S/W Reset	40h
H/W Reset	40h

5.8.3. EXTC Command Set Enable Register (FFh)

Command Page			Page 5								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								05h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

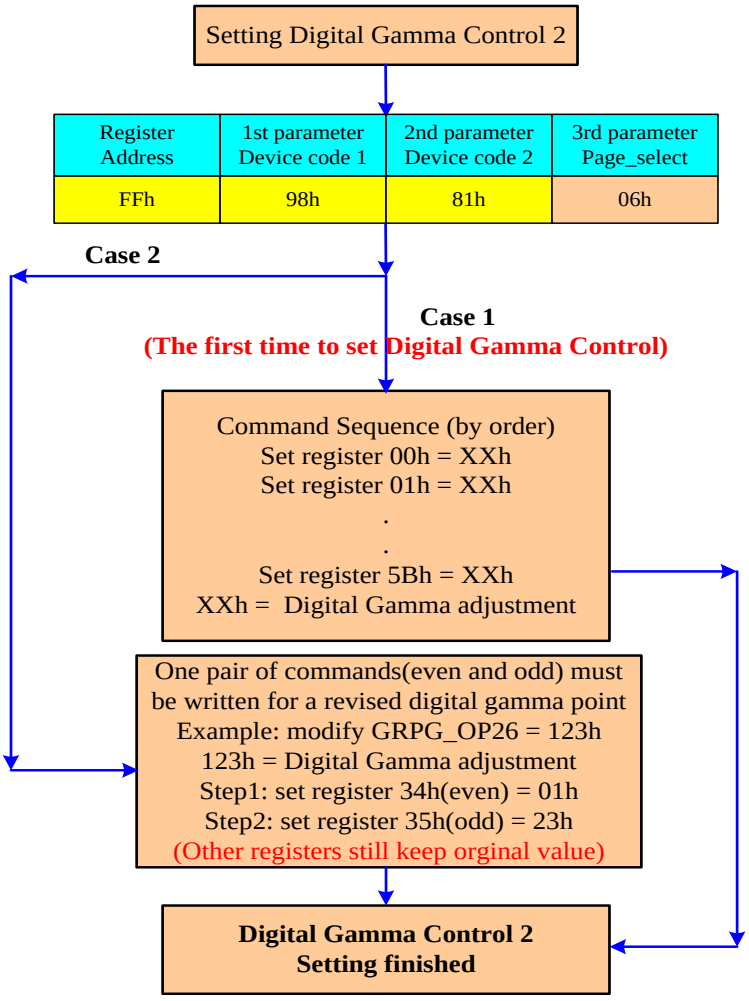
Status	Default Value
Power On Sequence	05h
S/W Reset	05h
H/W Reset	05h

5.9. Page 6 Command Description

5.9.1. Fine Digital Gamma Control 2 (00h~5Bh)

Command Page			Page 6								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W/R	FineOffsetG00[5:0]						GRPG_OP0[9:8]		XX
01h	1st	W/R	GRPG_OP0[7:0]								XX
02h	1st	W/R	FineOffsetG01[5:0]						GRPG_OP1[9:8]		XX
03h	1st	W/R	GRPG_OP1[7:0]								XX
04h	1st	W/R	FineOffsetG02[5:0]						GRPG_OP2[9:8]		XX
05h	1st	W/R	GRPG_OP2[7:0]								XX
06h	1st	W/R	FineOffsetG03[5:0]						GRPG_OP3[9:8]		XX
07h	1st	W/R	GRPG_OP3[7:0]								XX
08h	1st	W/R	FineOffsetG04[5:0]						GRPG_OP4[9:8]		XX
09h	1st	W/R	GRPG_OP4[7:0]								XX
0Ah	1st	W/R	FineOffsetG05[5:0]						GRPG_OP5[9:8]		XX
0Bh	1st	W/R	GRPG_OP5[7:0]								XX
0Ch	1st	W/R	FineOffsetG06[5:0]						GRPG_OP6[9:8]		XX
0Dh	1st	W/R	GRPG_OP6[7:0]								XX
0Eh	1st	W/R	FineOffsetG07[5:0]						GRPG_OP7[9:8]		XX
0Fh	1st	W/R	GRPG_OP7[7:0]								XX
10h	1st	W/R	FineOffsetG08[5:0]						GRPG_OP8[9:8]		XX
11h	1st	W/R	GRPG_OP8[7:0]								XX
12h	1st	W/R	FineOffsetG09[5:0]						GRPG_OP9[9:8]		XX
13h	1st	W/R	GRPG_OP9[7:0]								XX
14h	1st	W/R	FineOffsetG10[5:0]						GRPG_OP10[9:8]		XX
15h	1st	W/R	GRPG_OP10[7:0]								XX
16h	1st	W/R	FineOffsetG11[5:0]						GRPG_OP11[9:8]		XX
17h	1st	W/R	GRPG_OP11[7:0]								XX
18h	1st	W/R	FineOffsetG12[5:0]						GRPG_OP12[9:8]		XX
19h	1st	W/R	GRPG_OP12[7:0]								XX
1Ah	1st	W/R	FineOffsetG13[5:0]						GRPG_OP13[9:8]		XX
1Bh	1st	W/R	GRPG_OP13[7:0]								XX
1Ch	1st	W/R	FineOffsetG14[5:0]						GRPG_OP14[9:8]		XX
1Dh	1st	W/R	GRPG_OP14[7:0]								XX
1Eh	1st	W/R	FineOffsetG15[5:0]						GRPG_OP15[9:8]		XX
1Fh	1st	W/R	GRPG_OP15[7:0]								XX
20h	1st	W/R	FineOffsetG16[5:0]						GRPG_OP16[9:8]		XX
21h	1st	W/R	GRPG_OP16[7:0]								XX
22h	1st	W/R	FineOffsetG17[5:0]						GRPG_OP17[9:8]		XX
23h	1st	W/R	GRPG_OP17[7:0]								XX
24h	1st	W/R	FineOffsetG18[5:0]						GRPG_OP18[9:8]		XX
25h	1st	W/R	GRPG_OP18[7:0]								XX
26h	1st	W/R	FineOffsetG19[5:0]						GRPG_OP19[9:8]		XX
27h	1st	W/R	GRPG_OP19[7:0]								XX
28h	1st	W/R	FineOffsetG20[5:0]						GRPG_OP20[9:8]		XX
29h	1st	W/R	GRPG_OP20[7:0]								XX
2Ah	1st	W/R	FineOffsetG21[5:0]						GRPG_OP21[9:8]		XX
2Bh	1st	W/R	GRPG_OP21[7:0]								XX
2Ch	1st	W/R	FineOffsetG22[5:0]						GRPG_OP22[9:8]		XX
2Dh	1st	W/R	GRPG_OP22[7:0]								XX
2Eh	1st	W/R	FineOffsetG23[5:0]						GRPG_OP23[9:8]		XX
2Fh	1st	W/R	GRPG_OP23[7:0]								XX
30h	1st	W/R	FineOffsetG24[5:0]						GRPG_OP24[9:8]		XX
31h	1st	W/R	GRPG_OP24[7:0]								XX
32h	1st	W/R	FineOffsetG25[5:0]						GRPG_OP25[9:8]		XX

33h	1st	W/R	GRPG_OP25[7:0]								XX
34h	1st	W/R	FineOffsetG26[5:0]						GRPG_OP26[9:8]		XX
35h	1st	W/R	GRPG_OP26[7:0]								XX
36h	1st	W/R	FineOffsetG27[5:0]						GRPG_OP27[9:8]		XX
37h	1st	W/R	GRPG_OP27[7:0]								XX
38h	1st	W/R	FineOffsetG28[5:0]						GRPG_OP28[9:8]		XX
39h	1st	W/R	GRPG_OP28[7:0]								XX
3Ah	1st	W/R	0	0	0	0	0	0	GRPG_OP29[9:8]		XX
3Bh	1st	W/R	GRPG_OP29[7:0]								XX
3Ch	1st	W/R	0	0	0	0	0	0	GRPG_OP30[9:8]		XX
3Dh	1st	W/R	GRPG_OP30[7:0]								XX
3Eh	1st	W/R	0	0	0	0	0	0	GRPG_OP31[9:8]		XX
3Fh	1st	W/R	GRPG_OP31[7:0]								XX
40h	1st	W/R	0	0	0	0	0	0	GRPG_OP32[9:8]		XX
41h	1st	W/R	GRPG_OP32[7:0]								XX
42h	1st	W/R	0	0	0	0	0	0	GRPG_OP33[9:8]		XX
43h	1st		GRPG_OP33[7:0]								XX
44h	1st	W/R	0	0	0	0	0	0	GRPG_OP34[9:8]		XX
45h	1st		GRPG_OP34[7:0]								XX
46h	1st	W/R	0	0	0	0	0	0	GRPG_OP35[9:8]		XX
47h	1st	W/R	GRPG_OP35[7:0]								XX
48h	1st	W/R	0	0	0	0	0	0	GRPG_OP36[9:8]		XX
49h	1st	W/R	GRPG_OP36[7:0]								XX
4Ah	1st	W/R	0	0	0	0	0	0	GRPG_OP37[9:8]		XX
4Bh	1st	W/R	GRPG_OP37[7:0]								XX
4Ch	1st	W/R	0	0	0	0	0	0	GRPG_OP38[9:8]		XX
4Dh	1st	W/R	GRPG_OP38[7:0]								XX
4Eh	1st	W/R	0	0	0	0	0	0	GRPG_OP39[9:8]		XX
4Fh	1st	W/R	GRPG_OP39[7:0]								XX
50h	1st	W/R	0	0	0	0	0	0	GRPG_OP40[9:8]		XX
51h	1st	W/R	GRPG_OP40[7:0]								XX
52h	1st	W/R	0	0	0	0	0	0	GRPG_OP41[9:8]		XX
53h	1st	W/R	GRPG_OP41[7:0]								XX
54h	1st	W/R	0	0	0	0	0	0	GRPG_OP42[9:8]		XX
55h	1st	W/R	GRPG_OP42[7:0]								XX
56h	1st	W/R	0	0	0	0	0	0	GRPG_OP43[9:8]		XX
57h	1st	W/R	GRPG_OP43[7:0]								XX
58h	1st	W/R	0	0	0	0	0	0	GRPG_OP44[9:8]		XX
59h	1st	W/R	GRPG_OP44[7:0]								XX
5Ah	1st	W/R	0	0	0	0	0	0	GRPG_OP45[9:8]		XX
5Bh	1st	W/R	GRPG_OP45[7:0]								XX
FFh	1st	W	1	0	0	1	1	0	0	0	98
	2nd	W	1	0	0	0	0	0	0	1	81
	3rd	W	Page[7:0]								06
Description			**GRPG_OP0[9:0]~GRPG_OP45[9:0]:** Digital Gamma Macro-adjustment registers for green gamma curve.								



Restriction	None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_...00h_00h
S/W Reset	00h_00h_...00h_00h
H/W Reset	00h_00h_...00h_00h

5.9.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 6								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								06h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

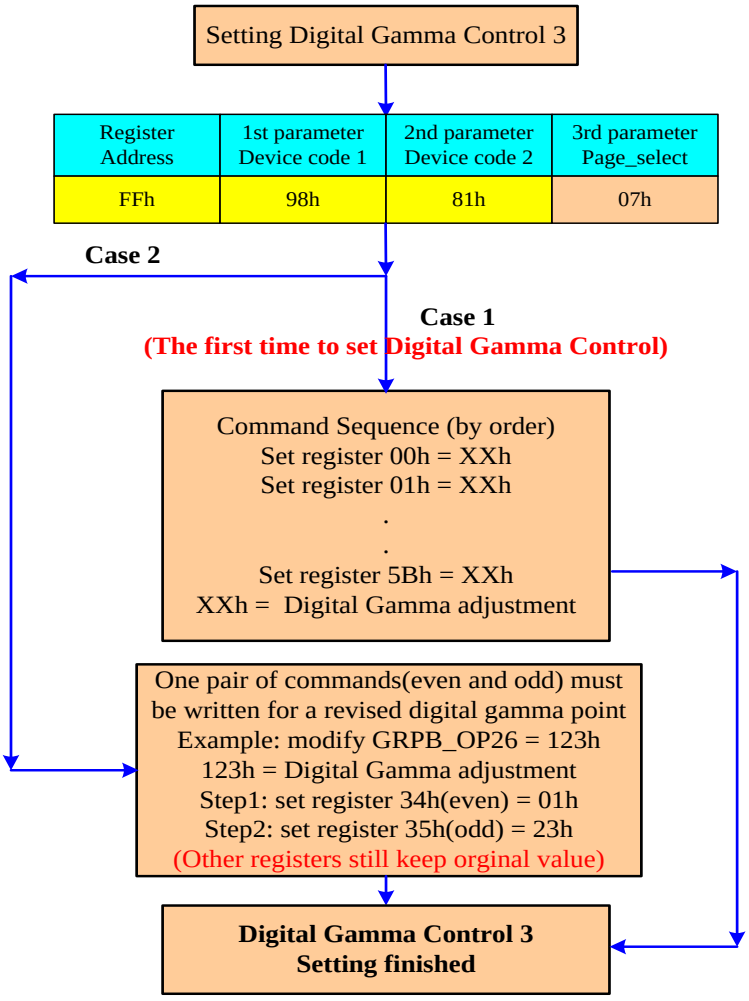
Status	Default Value
Power On Sequence	06h
S/W Reset	06h
H/W Reset	06h

5.10. Page 7 Command Description

5.10.1. Fine Digital Gamma Control 3 (00h~5Bh)

Command Page			Page 7								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W/R	FineOffsetB00[5:0]						GRPB_OP0[9:8]		XX
01h	1st	W/R	GRPB_OP0[7:0]								XX
02h	1st	W/R	FineOffsetB01[5:0]						GRPB_OP1[9:8]		XX
03h	1st	W/R	GRPB_OP1[7:0]								XX
04h	1st	W/R	FineOffsetB02[5:0]						GRPB_OP2[9:8]		XX
05h	1st	W/R	GRPB_OP2[7:0]								XX
06h	1st	W/R	FineOffsetB03[5:0]						GRPB_OP3[9:8]		XX
07h	1st	W/R	GRPB_OP3[7:0]								XX
08h	1st	W/R	FineOffsetB04[5:0]						GRPB_OP4[9:8]		XX
09h	1st	W/R	GRPB_OP4[7:0]								XX
0Ah	1st	W/R	FineOffsetB05[5:0]						GRPB_OP5[9:8]		XX
0Bh	1st	W/R	GRPB_OP5[7:0]								XX
0Ch	1st	W/R	FineOffsetB06[5:0]						GRPB_OP6[9:8]		XX
0Dh	1st	W/R	GRPB_OP6[7:0]								XX
0Eh	1st	W/R	FineOffsetB07[5:0]						GRPB_OP7[9:8]		XX
0Fh	1st	W/R	GRPB_OP7[7:0]								XX
10h	1st	W/R	FineOffsetB08[5:0]						GRPB_OP8[9:8]		XX
11h	1st	W/R	GRPB_OP8[7:0]								XX
12h	1st	W/R	FineOffsetB09[5:0]						GRPB_OP9[9:8]		XX
13h	1st	W/R	GRPB_OP9[7:0]								XX
14h	1st	W/R	FineOffsetB10[5:0]						GRPB_OP10[9:8]		XX
15h	1st	W/R	GRPB_OP10[7:0]								XX
16h	1st	W/R	FineOffsetB11[5:0]						GRPB_OP11[9:8]		XX
17h	1st	W/R	GRPB_OP11[7:0]								XX
18h	1st	W/R	FineOffsetB12[5:0]						GRPB_OP12[9:8]		XX
19h	1st	W/R	GRPB_OP12[7:0]								XX
1Ah	1st	W/R	FineOffsetB13[5:0]						GRPB_OP13[9:8]		XX
1Bh	1st	W/R	GRPB_OP13[7:0]								XX
1Ch	1st	W/R	FineOffsetB14[5:0]						GRPB_OP14[9:8]		XX
1Dh	1st	W/R	GRPB_OP14[7:0]								XX
1Eh	1st	W/R	FineOffsetB15[5:0]						GRPB_OP15[9:8]		XX
1Fh	1st	W/R	GRPB_OP15[7:0]								XX
20h	1st	W/R	FineOffsetB16[5:0]						GRPB_OP16[9:8]		XX
21h	1st	W/R	GRPB_OP16[7:0]								XX
22h	1st	W/R	FineOffsetB17[5:0]						GRPB_OP17[9:8]		XX
23h	1st	W/R	GRPB_OP17[7:0]								XX
24h	1st	W/R	FineOffsetB18[5:0]						GRPB_OP18[9:8]		XX
25h	1st	W/R	GRPB_OP18[7:0]								XX
26h	1st	W/R	FineOffsetB19[5:0]						GRPB_OP19[9:8]		XX
27h	1st	W/R	GRPB_OP19[7:0]								XX
28h	1st	W/R	FineOffsetB20[5:0]						GRPB_OP20[9:8]		XX
29h	1st	W/R	GRPB_OP20[7:0]								XX
2Ah	1st	W/R	FineOffsetB21[5:0]						GRPB_OP21[9:8]		XX
2Bh	1st	W/R	GRPB_OP21[7:0]								XX
2Ch	1st	W/R	FineOffsetB22[5:0]						GRPB_OP22[9:8]		XX
2Dh	1st	W/R	GRPB_OP22[7:0]								XX
2Eh	1st	W/R	FineOffsetB23[5:0]						GRPB_OP23[9:8]		XX
2Fh	1st	W/R	GRPB_OP23[7:0]								XX
30h	1st	W/R	FineOffsetB24[5:0]						GRPB_OP24[9:8]		XX
31h	1st	W/R	GRPB_OP24[7:0]								XX
32h	1st	W/R	FineOffsetB25[5:0]						GRPB_OP25[9:8]		XX

33h	1st	W/R	GRPB_OP25[7:0]								XX
34h	1st	W/R	FineOffsetB26[5:0]						GRPB_OP26[9:8]		XX
35h	1st	W/R	GRPB_OP26[7:0]								XX
36h	1st	W/R	FineOffsetB27[5:0]						GRPB_OP27[9:8]		XX
37h	1st	W/R	GRPB_OP27[7:0]								XX
38h	1st	W/R	FineOffsetB28[5:0]						GRPB_OP28[9:8]		XX
39h	1st	W/R	GRPB_OP28[7:0]								XX
3Ah	1st	W/R	0	0	0	0	0	0	GRPB_OP29[9:8]		XX
3Bh	1st	W/R	GRPB_OP29[7:0]								XX
3Ch	1st	W/R	0	0	0	0	0	0	GRPB_OP30[9:8]		XX
3Dh	1st	W/R	GRPB_OP30[7:0]								XX
3Eh	1st	W/R	0	0	0	0	0	0	GRPB_OP31[9:8]		XX
3Fh	1st	W/R	GRPB_OP31[7:0]								XX
40h	1st	W/R	0	0	0	0	0	0	GRPB_OP32[9:8]		XX
41h	1st	W/R	GRPB_OP32[7:0]								XX
42h	1st	W/R	0	0	0	0	0	0	GRPB_OP33[9:8]		XX
43h	1st		GRPB_OP33[7:0]								XX
44h	1st	W/R	0	0	0	0	0	0	GRPB_OP34[9:8]		XX
45h	1st		GRPB_OP34[7:0]								XX
46h	1st	W/R	0	0	0	0	0	0	GRPB_OP35[9:8]		XX
47h	1st	W/R	GRPB_OP35[7:0]								XX
48h	1st	W/R	0	0	0	0	0	0	GRPB_OP36[9:8]		XX
49h	1st	W/R	GRPB_OP36[7:0]								XX
4Ah	1st	W/R	0	0	0	0	0	0	GRPB_OP37[9:8]		XX
4Bh	1st	W/R	GRPB_OP37[7:0]								XX
4Ch	1st	W/R	0	0	0	0	0	0	GRPB_OP38[9:8]		XX
4Dh	1st	W/R	GRPB_OP38[7:0]								XX
4Eh	1st	W/R	0	0	0	0	0	0	GRPB_OP39[9:8]		XX
4Fh	1st	W/R	GRPB_OP39[7:0]								XX
50h	1st	W/R	0	0	0	0	0	0	GRPG_OP40[9:8]		XX
51h	1st	W/R	GRPB_OP40[7:0]								XX
52h	1st	W/R	0	0	0	0	0	0	GRPB_OP41[9:8]		XX
53h	1st	W/R	GRPB_OP41[7:0]								XX
54h	1st	W/R	0	0	0	0	0	0	GRPB_OP42[9:8]		XX
55h	1st	W/R	GRPB_OP42[7:0]								XX
56h	1st	W/R	0	0	0	0	0	0	GRPB_OP43[9:8]		XX
57h	1st	W/R	GRPB_OP43[7:0]								XX
58h	1st	W/R	0	0	0	0	0	0	GRPB_OP44[9:8]		XX
59h	1st	W/R	GRPB_OP44[7:0]								XX
5Ah	1st	W/R	0	0	0	0	0	0	GRPB_OP45[9:8]		XX
5Bh	1st	W/R	GRPB_OP45[7:0]								XX
FFh	1st	W	1	0	0	1	1	0	0	0	98
	2nd	W	1	0	0	0	0	0	0	1	81
	3rd	W	Page[7:0]								07
Description			**GRPB_OP0[9:0]~GRPB_OP45[9:0]:** Digital Gamma Macro-adjustment registers for blue gamma curve.								



Restriction	None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h_00h_...00h_00h
S/W Reset	00h_00h_...00h_00h
H/W Reset	00h_00h_...00h_00h

5.10.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 7								
Address	**Parameter**	**W/R**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Default**
FFh	1st	W	1	0	0	1	1	0	0	0	98h
	2nd	W	1	0	0	0	0	0	0	1	81h
	3rd	W	PAGE[7:0]								07h

Description

PAGE[7:0]: Set the command page.

PAGE[7:0]	Command Page
00h	Page 0
01h	Page 1
02h	Page 2
03h	Page 3
04h	Page 4
05h	Page 5
06h	Page 6
07h	Page 7
08h	Page 8
09h	Page 9
0Ah	Page 10
Others	Reserved

Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available

See section "5.1 Command Flow".

Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

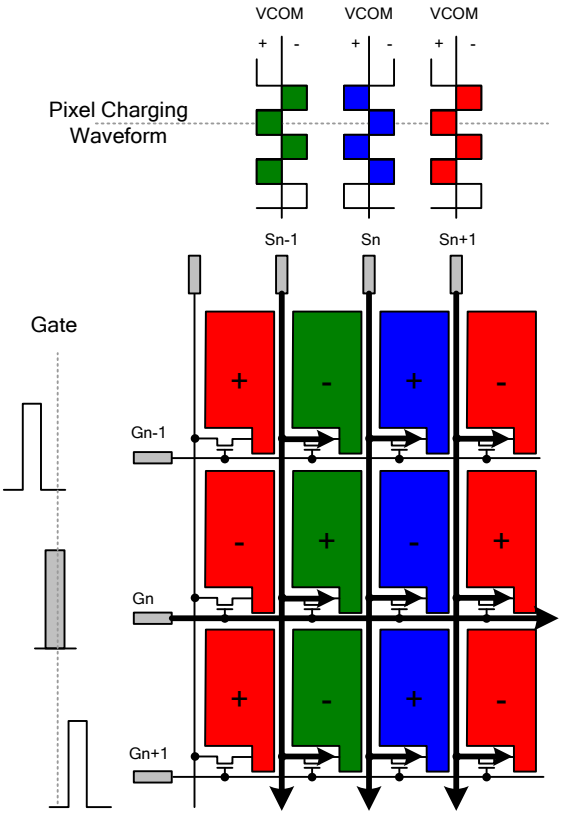
Status	Default Value
Power On Sequence	07h
S/W Reset	07h
H/W Reset	07h

6. Source Driver

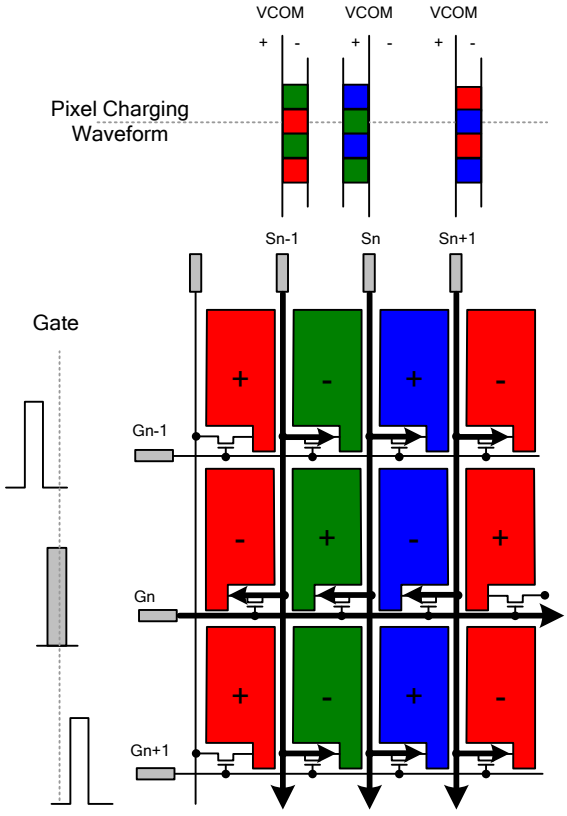
The source driver uses 2402 channels (S1~S2400 and SDUM[2:1] channels) for the Zig-zag function used for driving the source line of the TFT LCD panel. The source driver converts the digital data into the analog voltage and generates corresponding gray scale voltage output, enabling up to 16.7M colors to be displayed simultaneously. The output circuit of this source driver incorporates an operational amplifier, so that a positive and a negative voltage can be alternately outputted from each channel.

6.1. Zig-zag Inversion

Zig-zag Inversion is used to reduce the power consumption. The Zig-zag inversion decreases the switching frequency of the source related to the magnitude of power consumption. This method will have an addendum data line, SDUM.



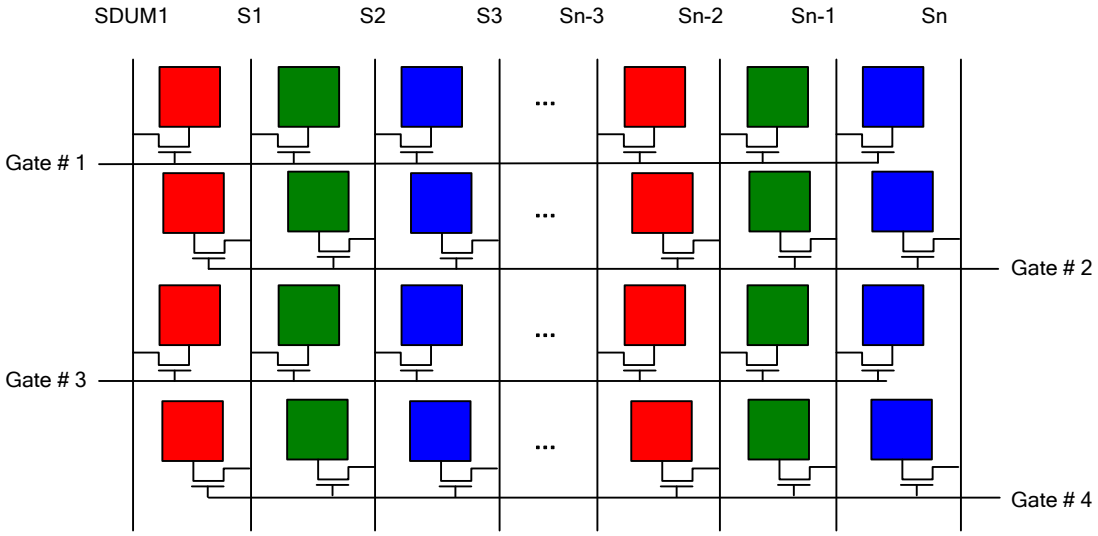
1-Dot Inversion Driving

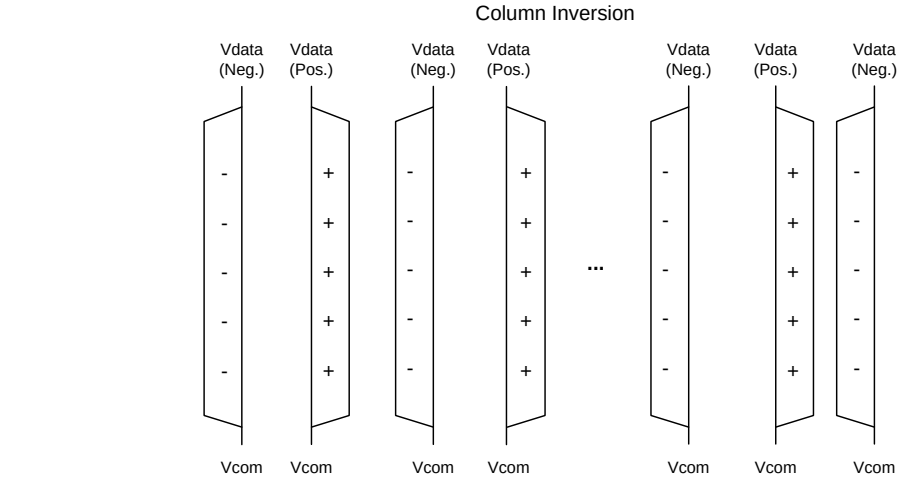


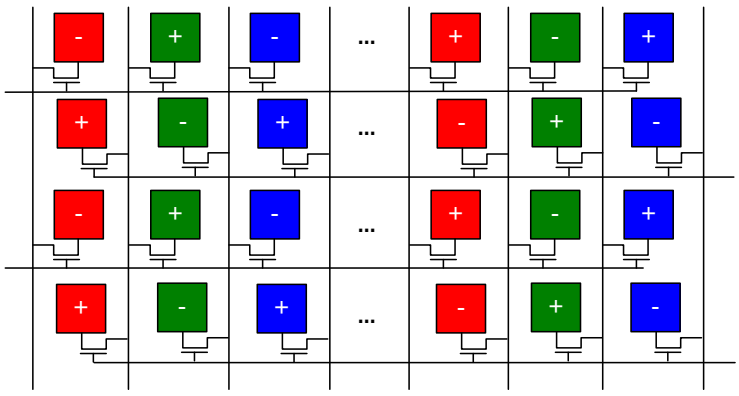
Vertical Bi-Color driving

6.2. Zig-zag Inversion Concept

The Zig-zag method uses the same polarity of data line of the column inversion to show the 1-dot inversion.







6.3. Zig-zag Inversion Source Output Method

The driving panel display method adds one sub-pixel at the Gate_Even to shift the data output.

(At the Gate_Even line, an additional data line is utilized.)

Red Pattern

	SDUM1	S1	S2	S3	S4	S5
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2

Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Green Pattern

	SDUM1	S1	S2	S3	S4	S5
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2

Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Blue Pattern

	SDUM1	S1	S2	S3	S4	S5
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2

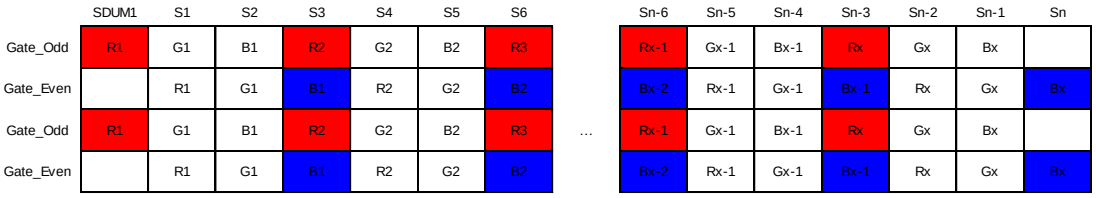
Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gx-1	Bx-1	Rx	Gx	Bx	
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

6.4. Zig-zag Inversion RED Data Display

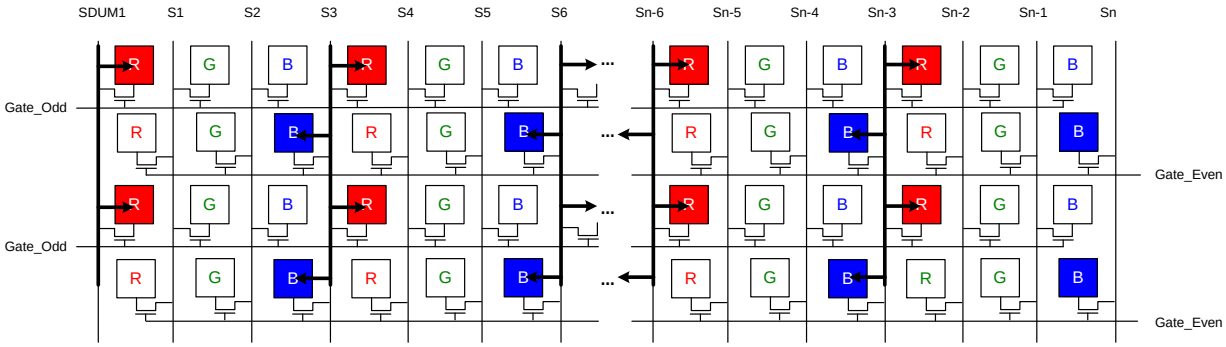
The figure below illustrates the Zig-zag inversion panel driving method for Red data input.

When driving a Red pattern, the Red and Blue sub-pixels will light up line by line according to the data signal input.

Source Output

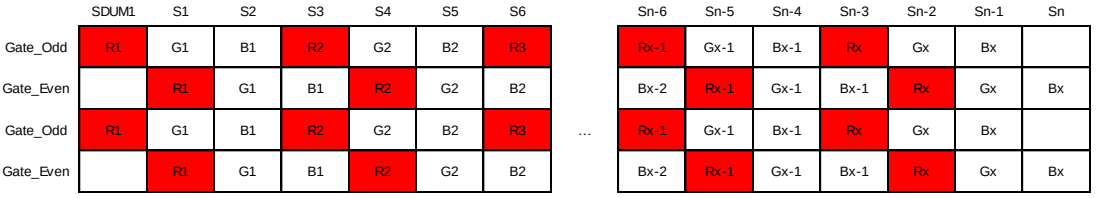


Panel Driving

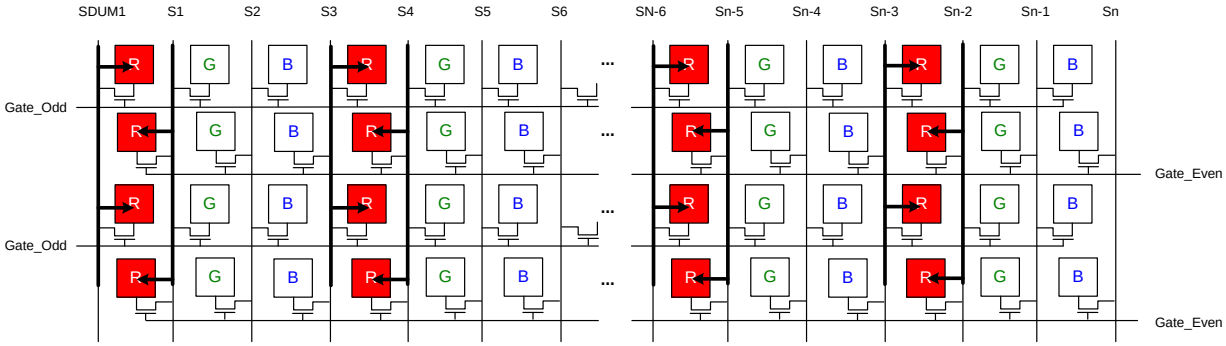


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Red data input of the Gate_Odd and the Green data input of the Gate_Even.

Source Output



Panel Driving



6.5. Zig-zag Inversion GREEN Data Display

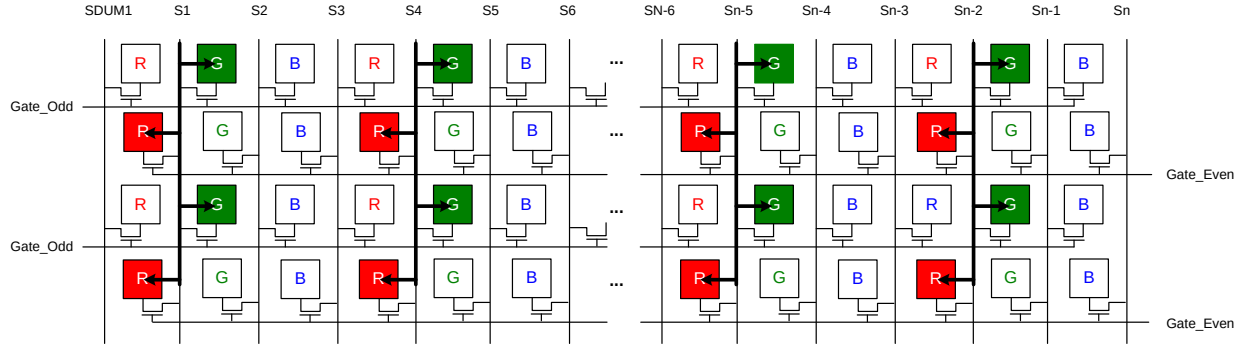
The figure below illustrates the Zig-zag inversion panel driving method for Green data input.

When driving a Green pattern, the Green and Red sub-pixels will light up line by line according to the data signal input.

Source Output

	SDUM1	S1	S2	S3	S4	S5	S6		Sn-6	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	R3		Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	R3	...	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Panel Driving

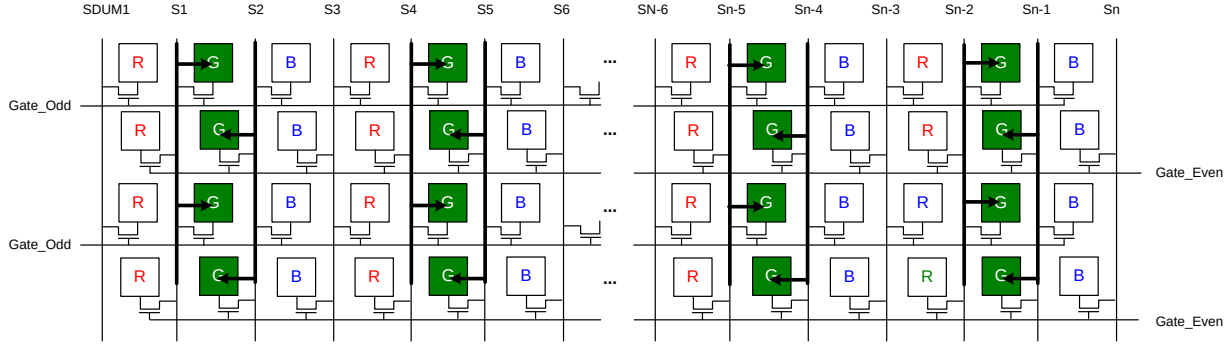


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Green data input of the Gate_Odd and the Blue data input of the Gate_Even.

Source Output

	SDUM1	S1	S2	S3	S4	S5	S6		Sn-6	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	R3		Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	R3	...	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Panel Driving



6.6. Zig-zag Inversion BLUE Data Display

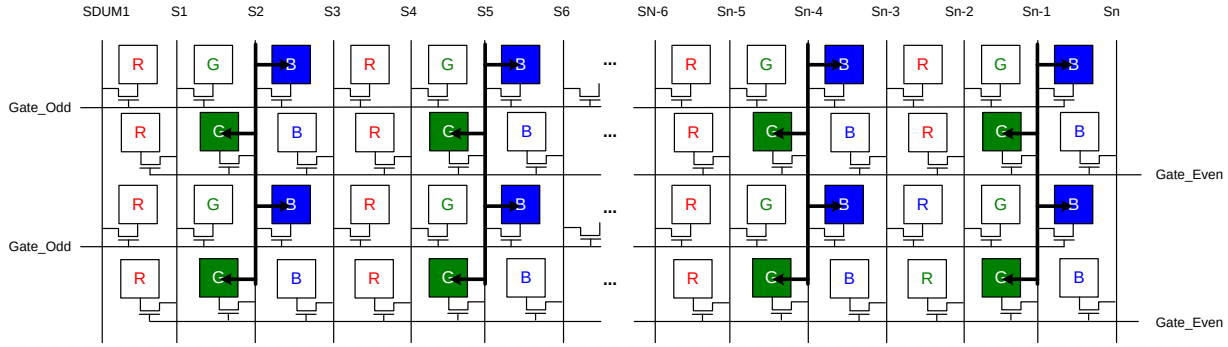
The figure below illustrates the Zig-zag inversion panel driving method for Blue data input.

When driving a Blue pattern, the Blue and Green sub-pixels will light up line by line according to the data signal input.

Source Output

	SDUM1	S1	S2	S3	S4	S5	S6		Sn-6	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	R3		Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	R3	...	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Panel Driving

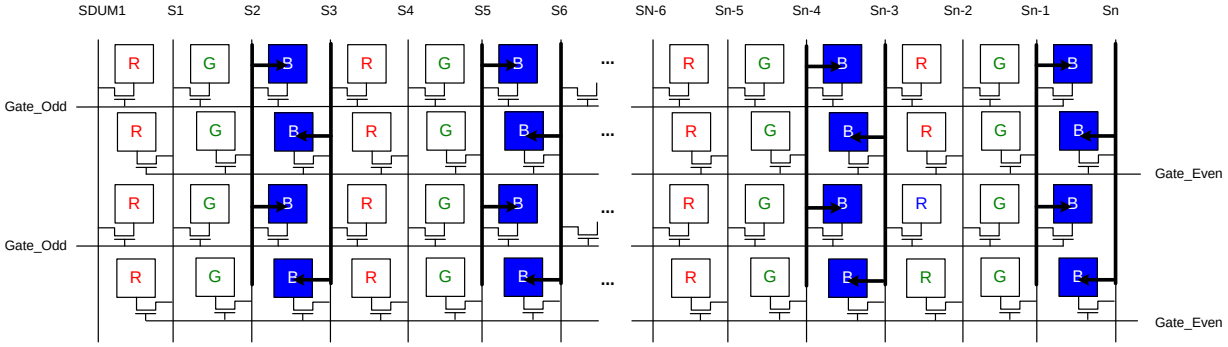


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Blue data input of the Gate_Odd and the Red data input of the Gate_Even.

Source Output

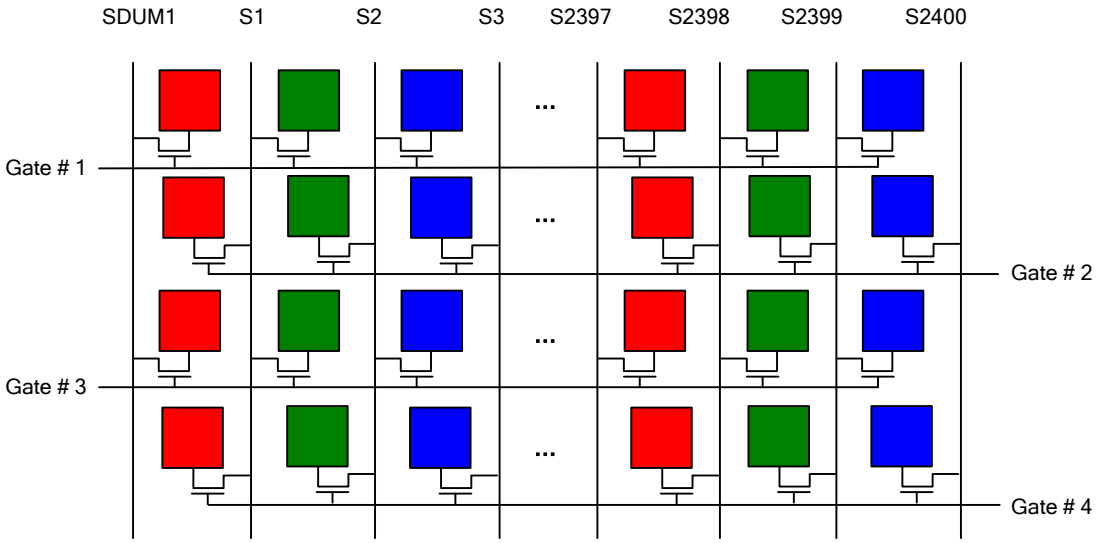
	SDUM1	S1	S2	S3	S4	S5	S6		Sn-6	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gate_Odd	R1	G1	B1	R2	G2	B2	R3		Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx
Gate_Odd	R1	G1	B1	R2	G2	B2	R3	...	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gate_Even		R1	G1	B1	R2	G2	B2		Bx-2	Rx-1	Gx-1	Bx-1	Rx	Gx	Bx

Panel Driving

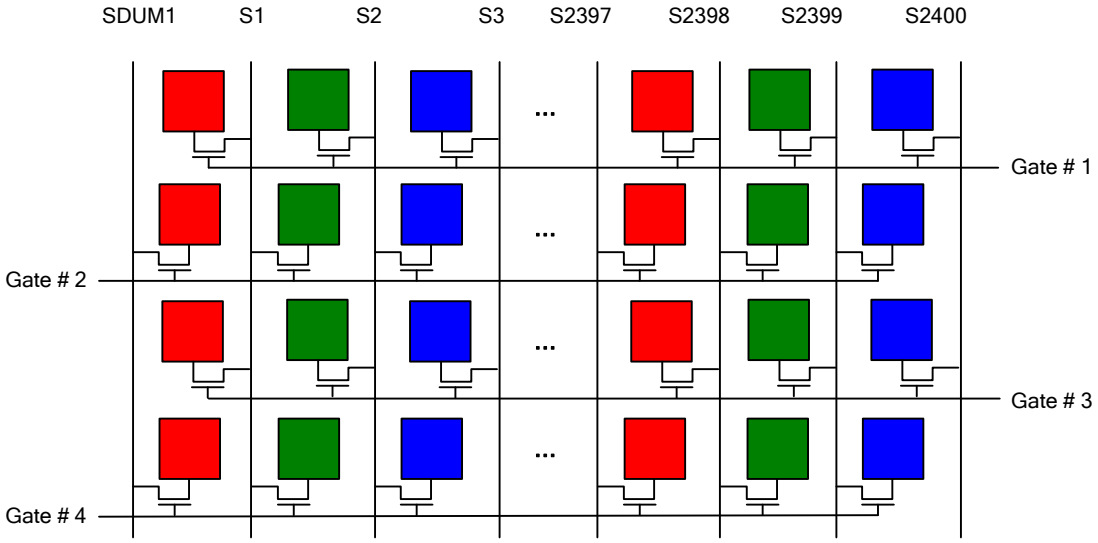


6.7. Different Zig-zag Type Panel

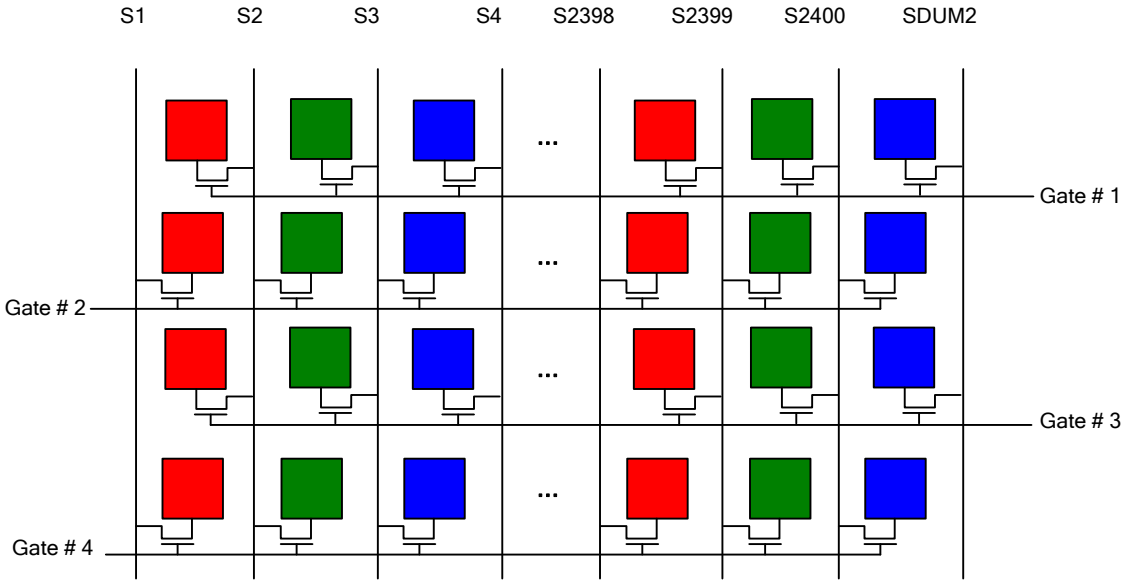
Zig-zag Type 1 (DINV[3:0] = 9h)



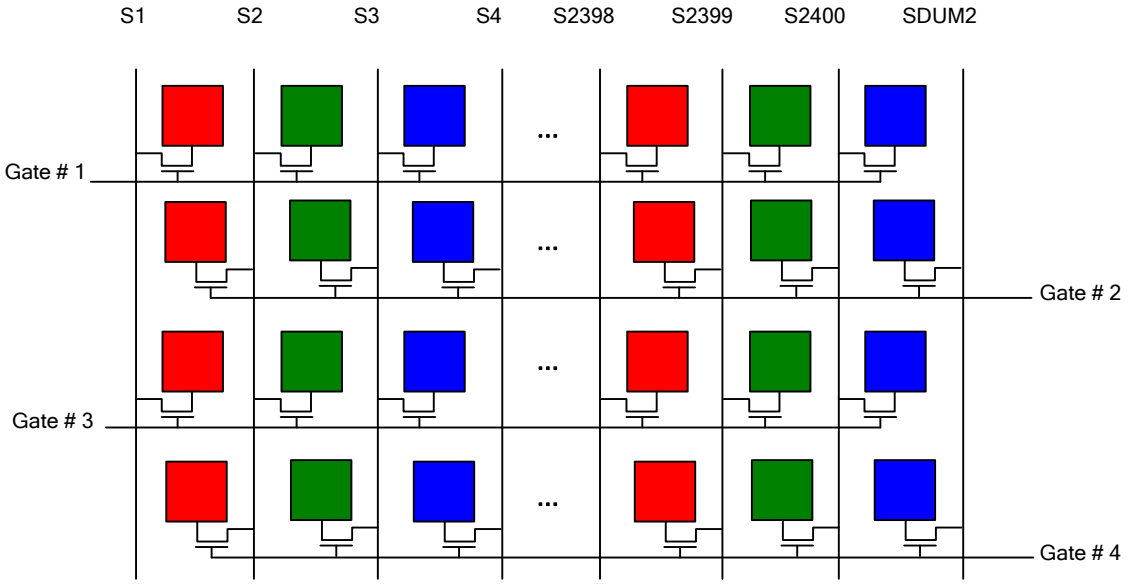
Zig-zag Type 2 (DINV[3:0] = Ah)



Zig-zag Type 3 (DINV[3:0] = Bh)



Zig-zag Type 4 (DINV[3:0] = Ch)



7. BIST Mode Function

7.1. BIST Mode Pattern

Table 33: BIST Mode Pattern

FRM_PT[0] White	FRM_PT[1] Black	FRM_PT[2] Red	FRM_PT[3] Green
FRM_PT[4] Blue	FRM_PT[5] Gray128	FRM_PT[6] Gray127	FRM_PT[7] V-Color bar

8. Content Adaptive Brightness Control (CABC) Function

The CABC, a dynamic backlight control function, drastically reduces the power consumption of the luminance source. The ILI9881C-05 will refer the gray scale content of the display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

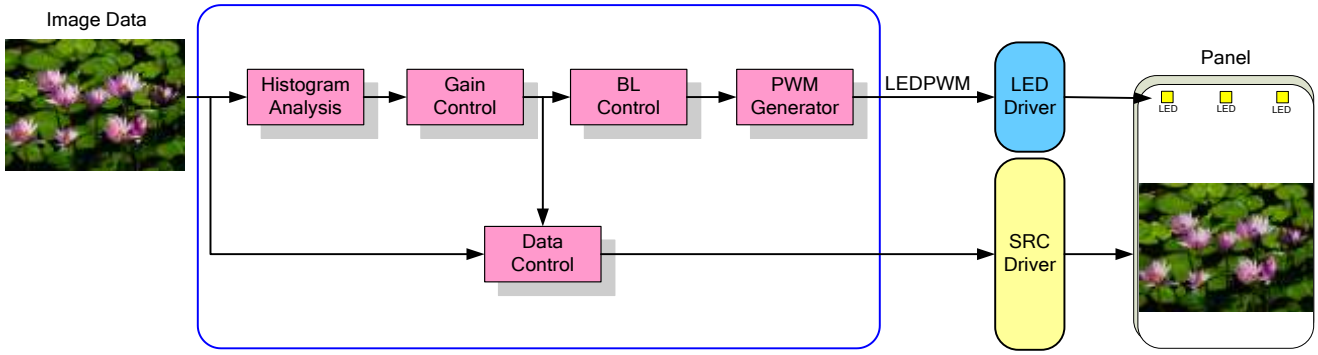


Figure 83: CABC Block Diagram

The ILI9881C-05 can calculate the backlight brightness level and send a PWM_OUT pulse to the LED driver via LEDPWM pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$f_{LEDPWM} = \frac{32\ MHz}{(\mathrm{PWM\_DIV}[7:0] + 1) \times PWM\_DUTY\_PRECISION}$$

Figure 84 is the basic timing diagram which is applied from the ILI9881C-05 in order to control the LED driver.

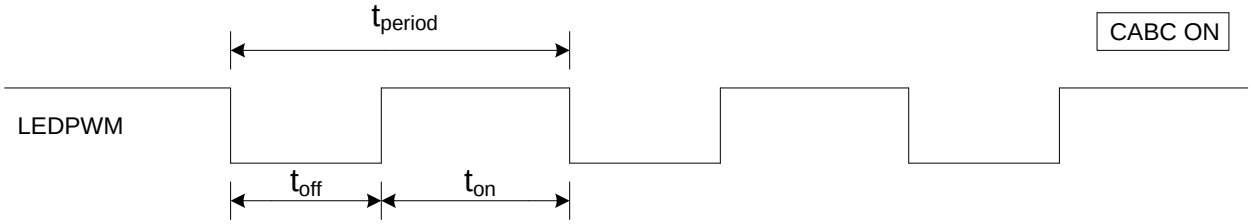


Figure 84: PWM OUT On/Off Period

9. Color Enhancement Function

9.1. Saturation Enhancement

The ILI9881C-05 provides the saturation enhancement to make the image content more vivid. The main concept in this feature is to enhance the color information on HSL domain, which includes the saturation information of each different color, show as Figure 85.

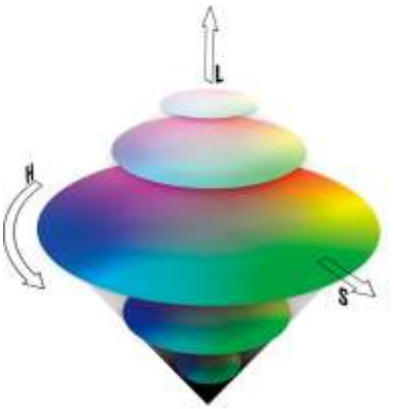


Figure 85: Saturation Enhancement : HSL model

In Figure 86, there is an example for saturation enhancement. Different enhancement levels being applied in this example.

(a) **(b)** **(c)** **(d)**

Figure 86: Saturation Enhancement Image (a) Original, (b) Low Level, (c) Medium Level, (d) High Level.

9.2. Contrast Enhancement

The contrast between the dark and light, indicate the clarity of the image content. In this design, it provides contrast enhancement to increase the difference between dark and light to achieve the high contrast image. The user can select the enhancement level by setting command, the example shows below.

(a) **(b)**

Figure 87: Contrast Enhancement Image (a) Original, (b) After enhancement

9.3. Sharpness Enhancement

Sharpness enhancement is provided to enhance the image visibility. Unlike contrast enhancement, sharpness enhancement is to strengthen the object's edge to make the object more clearly. The user can select the enhancement level by setting command, the example shows below.

(a) **(b)**

Figure 88: Sharpness Enhancement Image (a) Original, (b) After enhancement

9.4. Sunlight Readability

The sunlight readability is in order to achieve high visibility in daylight or other bright light condition. Figure 89 shows the main concept of the influence of ambient light to the LCD displayer and the solution in the high ambient light condition. In this design, it changes the image content to achieve the high visibility in the ambient light condition as shows in Figure 89(b).

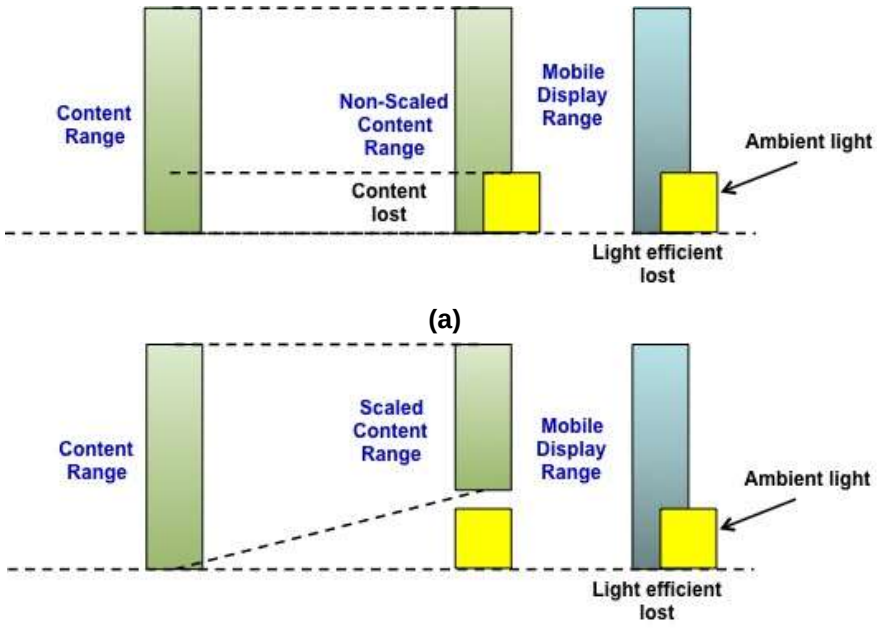


Figure 89: Sunlight Readability Concept (a) Backlight efficiency is consumed by ambient light, (b)Enhance the image content to avoid the influence.

10. Sleep Out Command and Self-Diagnostic Functions

10.1. Register Loading Detection

Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller works properly.

The display controller will compare factory values of the EEPROM and register values of the display controller (1st step: compare register and EEPROM values; 2nd step: load EEPROM value to the register). If those two values (EEPROM and register values) are the same, a bit is inverted (= increased by 1), which is defined in command Read Display Self-Diagnostic Result (0Fh) (= RDDSDR) (The used bit of this command is D7). If those values are not the same, this bit (D7) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

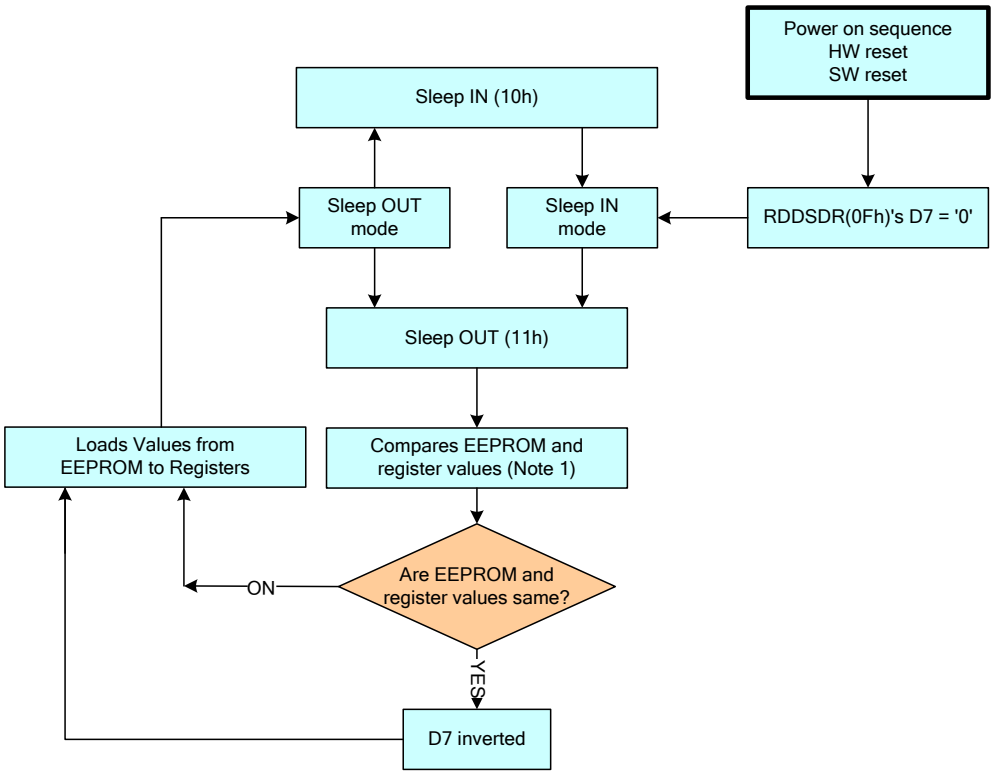


Figure 90: Register Loading Detection

Notes: *If the EEPROM and loaded register values are not compared, then they can be changed by 00h to AFh and DAh to DDh commands.*

10.2. Functionality Detection

The Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements. The internal function (the display controller) is compared to check if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (= increased by 1), defined in the command Read Display Self-Diagnostic Result (0Fh) (RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

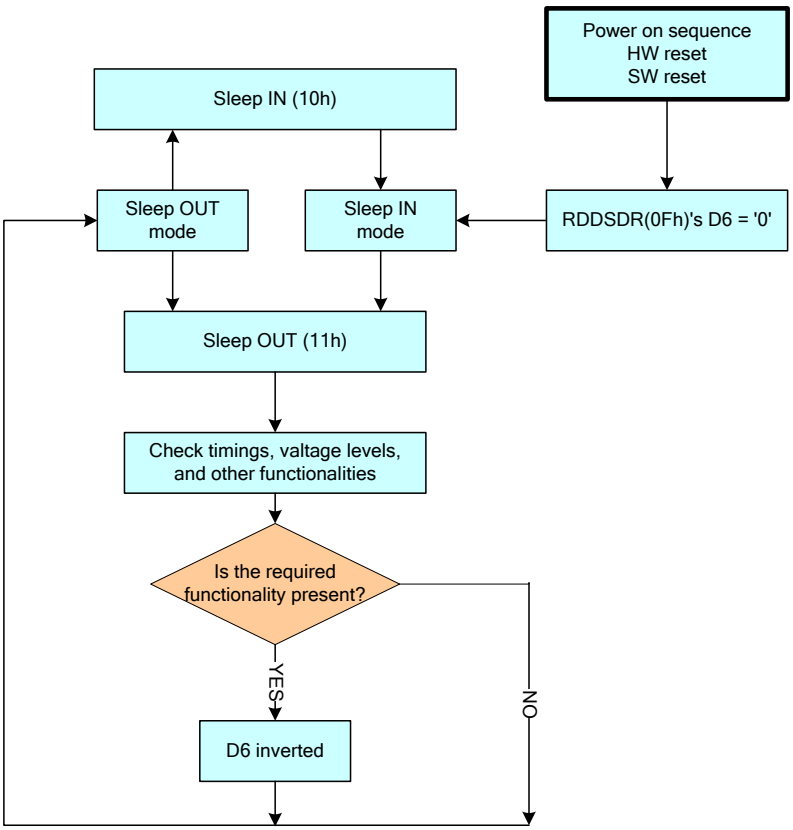


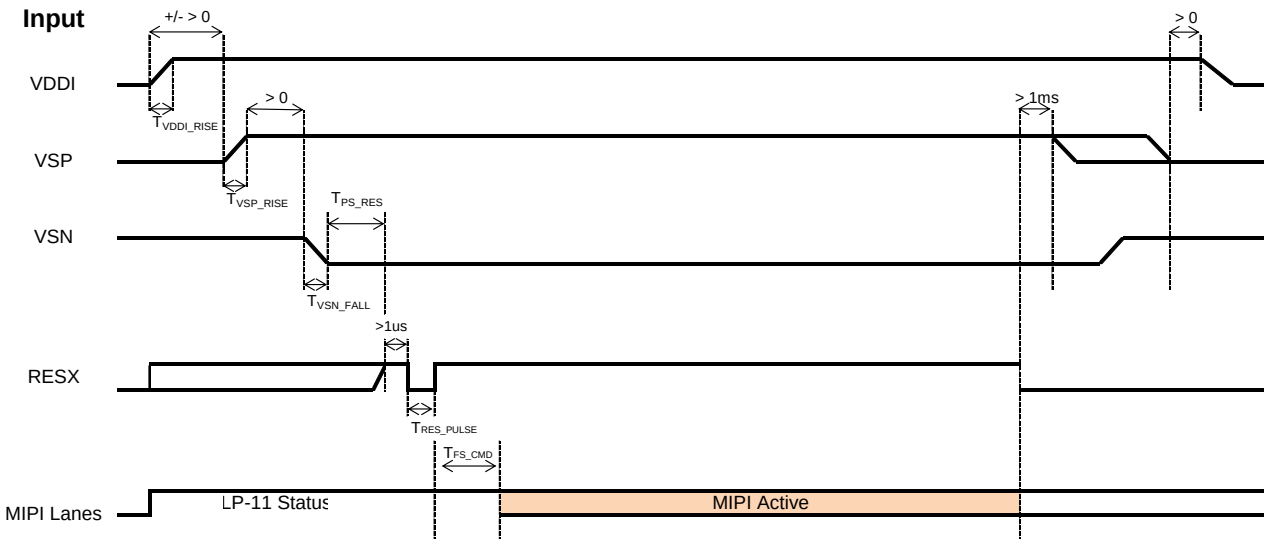
Figure 91: Functionality Detection

Notes: *When changing from the Sleep In mode to Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there will be 5msec delay for the D6's value to be valid when the Sleep Out command is sent in the Sleep Out mode.*

11. Power on/off Sequence

11.1. Power on/off sequence

11.1.1. Power Mode 2A

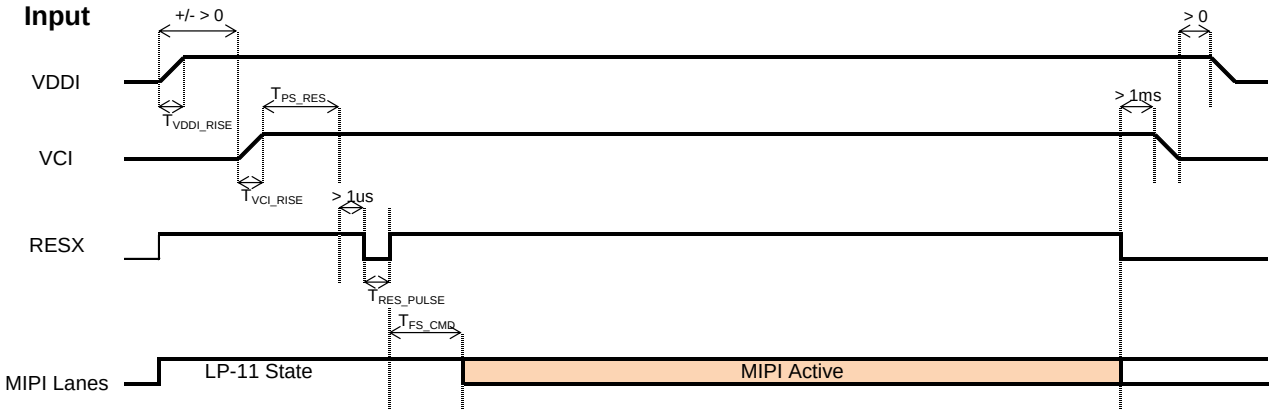


Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

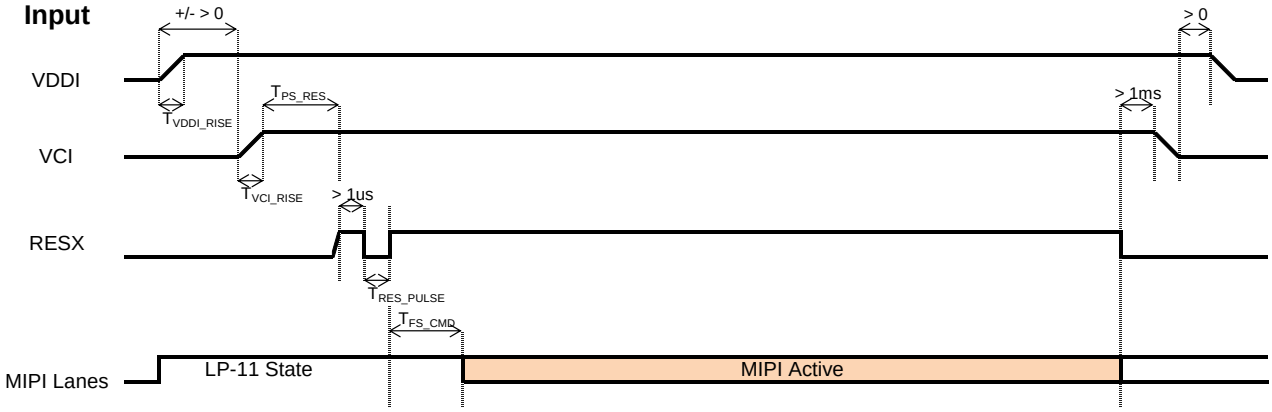
Figure 92: Power on/off sequence with Power Mode 2A

11.1.2. Power Mode 3

Case A:



Case B:

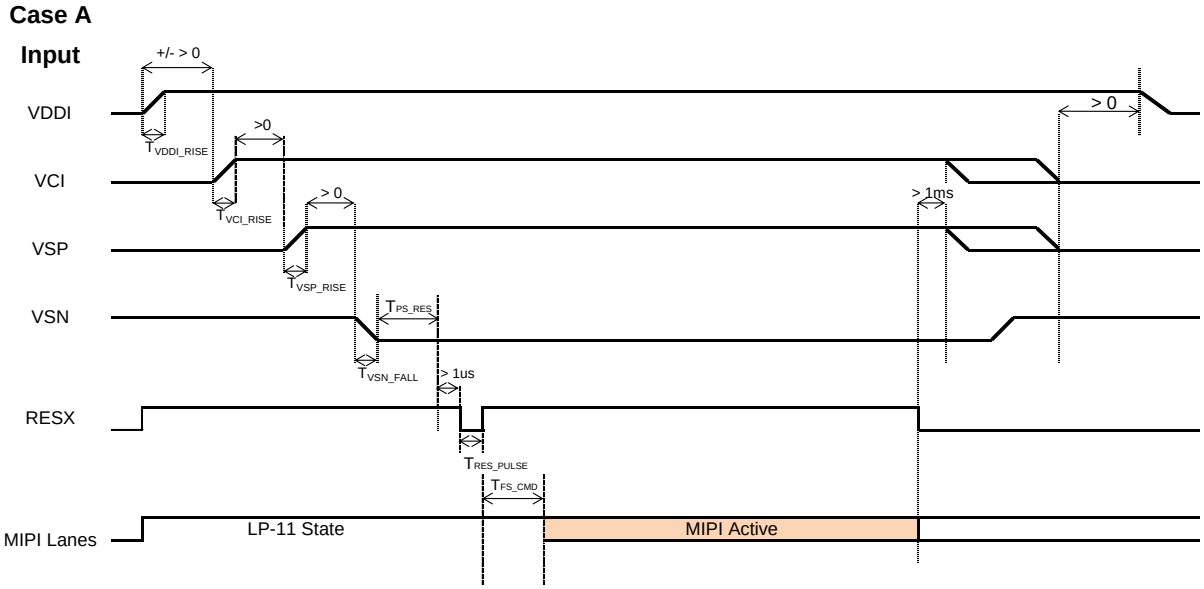


Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

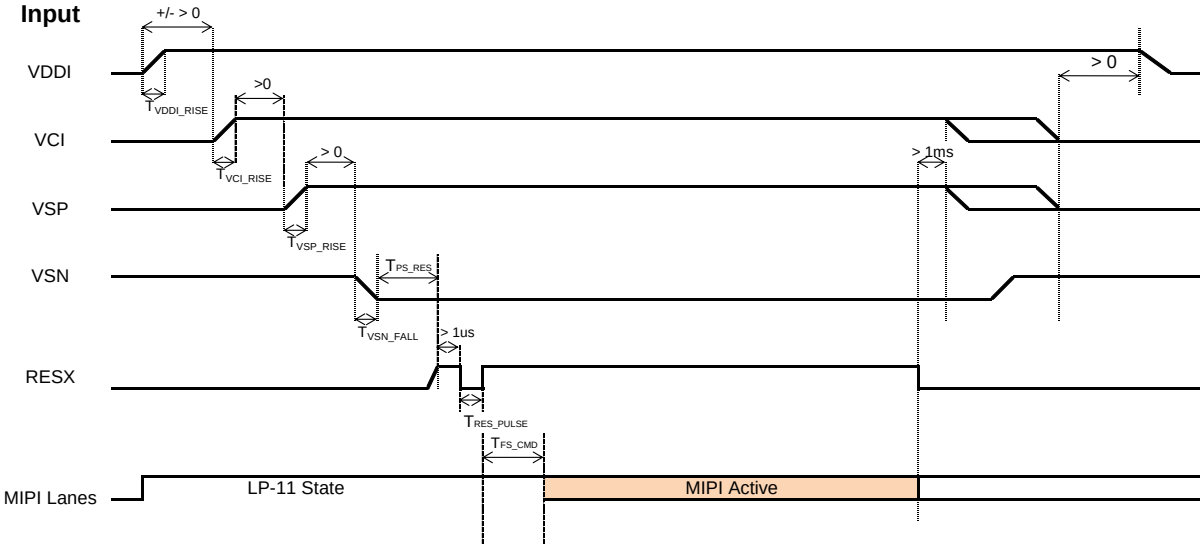
Figure 93: Power on/off sequence with Power Mode 3

11.1.3. Power Mode 4

Case A



Case B



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40			
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 94: Power on/off sequence with Power Mode 4

11.2. Uncontrolled Power Off

The uncontrolled power off means a situation when a battery is removed without the controlled power off sequence. There will not be any damages for the display module, or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, the ILI9881C-05 will force the display to become blank and will not have any abnormal visible effects within 1 second on the display and remains blank until the Power On Sequence powers it up.

12. Power Level Definition

12.1. Power Levels

4 level modes are defined in order from Maximum to Minimum Power consumption:

1. Normal Mode On (full display), Sleep Out, Idle Mode Off.
   In this mode, the display is able to show a maximum of 16.7M colors.
2. Normal Mode On (full display), Sleep Out, Idle Mode On.
   In this mode, the display is able to show a maximum of 2 colors.
3. Sleep In Mode.
   In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped.
4. Power Off Mode.
   In this mode, all input powers are removed.

Transition between modes 1-3 is controllable by MCU commands. Mode 4 is entered only when both Power supplies are removed.

12.2. Power Flow Chart

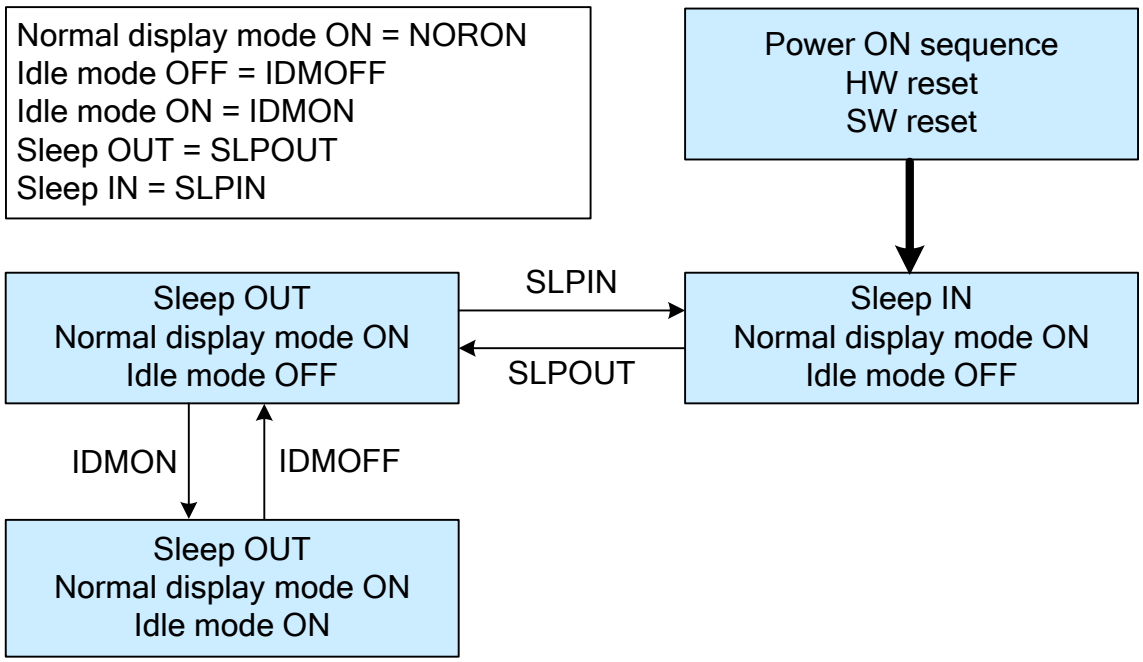


Figure 95: Power Mode Flow Chart

Notes:

1. *There is not any abnormal visual effect when one power mode changes to another power mode.*
2. *There is not any limitation, which is not specified by User, when one power mode changes to another power mode.*

13. Characteristics of I/O

13.1. Output or Bi-directional (I/O) Pins

Table 34: Characteristics of Output or Bi-directional (I/O) Pins

Pin/Line	After Power ON	After Hardware Reset	After Software Reset
D0P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
D0N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
VS	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
LEDPWM	Low	Low	Low
TE	Low	Low	Low

Note: *There will be no output from D0P, D0N, VS, HS, LEDPWM and TE during Power ON/OFF sequence, hardware reset, and software reset.*

13.2. Input Pins

Table 35: Input Pins

Pin/Line	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See chapter 11	Input valid	Input valid	Input valid	See chapter 11
IM[2:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
LANSEL	Input invalid	Input valid	Input valid	Input valid	Input invalid
RS[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
BOOSTM[2:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKP	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKN	Input invalid	Input valid	Input valid	Input valid	Input invalid
D0P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D0N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D1P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D1N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D2P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D2N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D3P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D3N	Input invalid	Input valid	Input valid	Input valid	Input invalid

14. NV Memory Programming Flow

14.1. External MTP_PWR 1-Byte Programming Flow

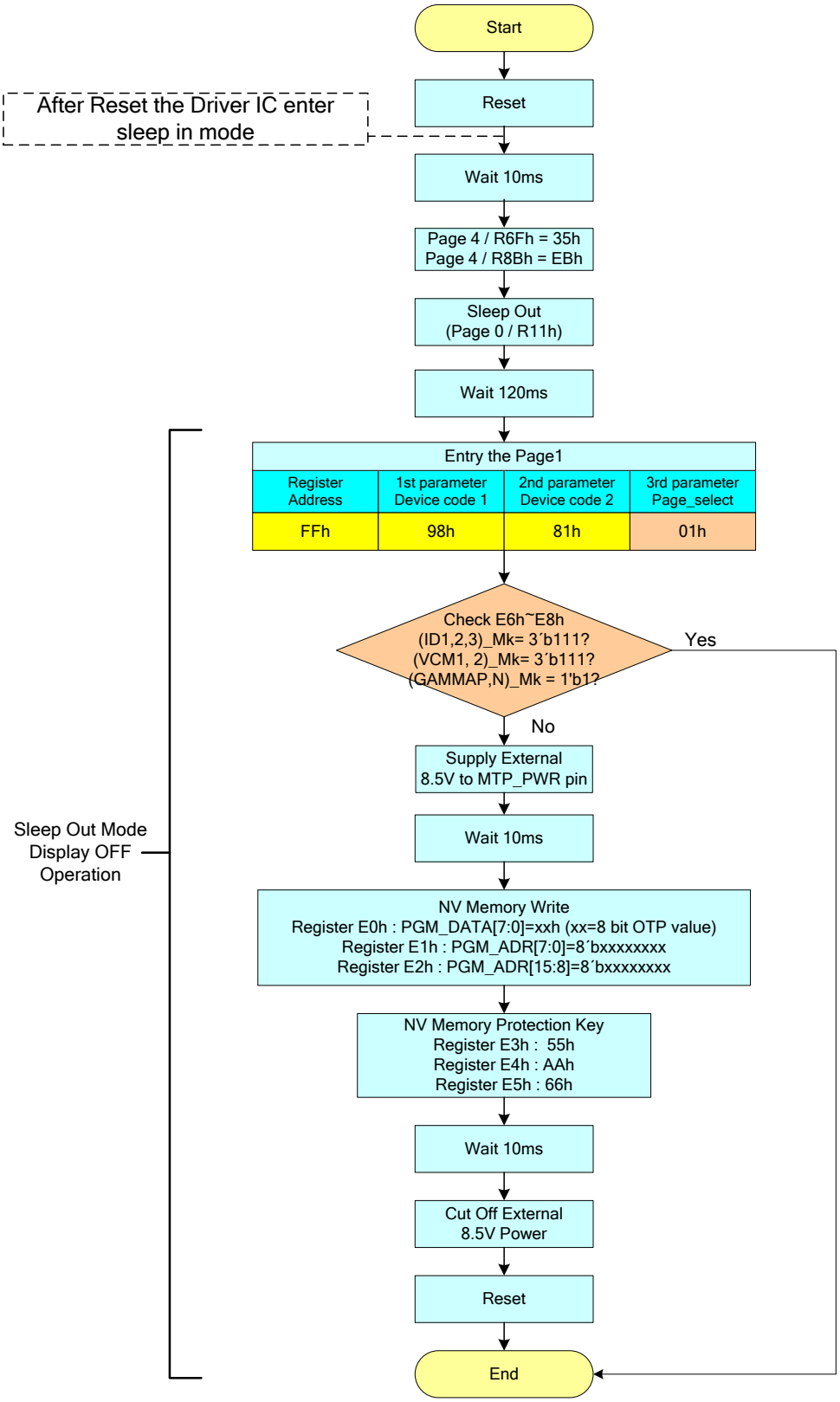
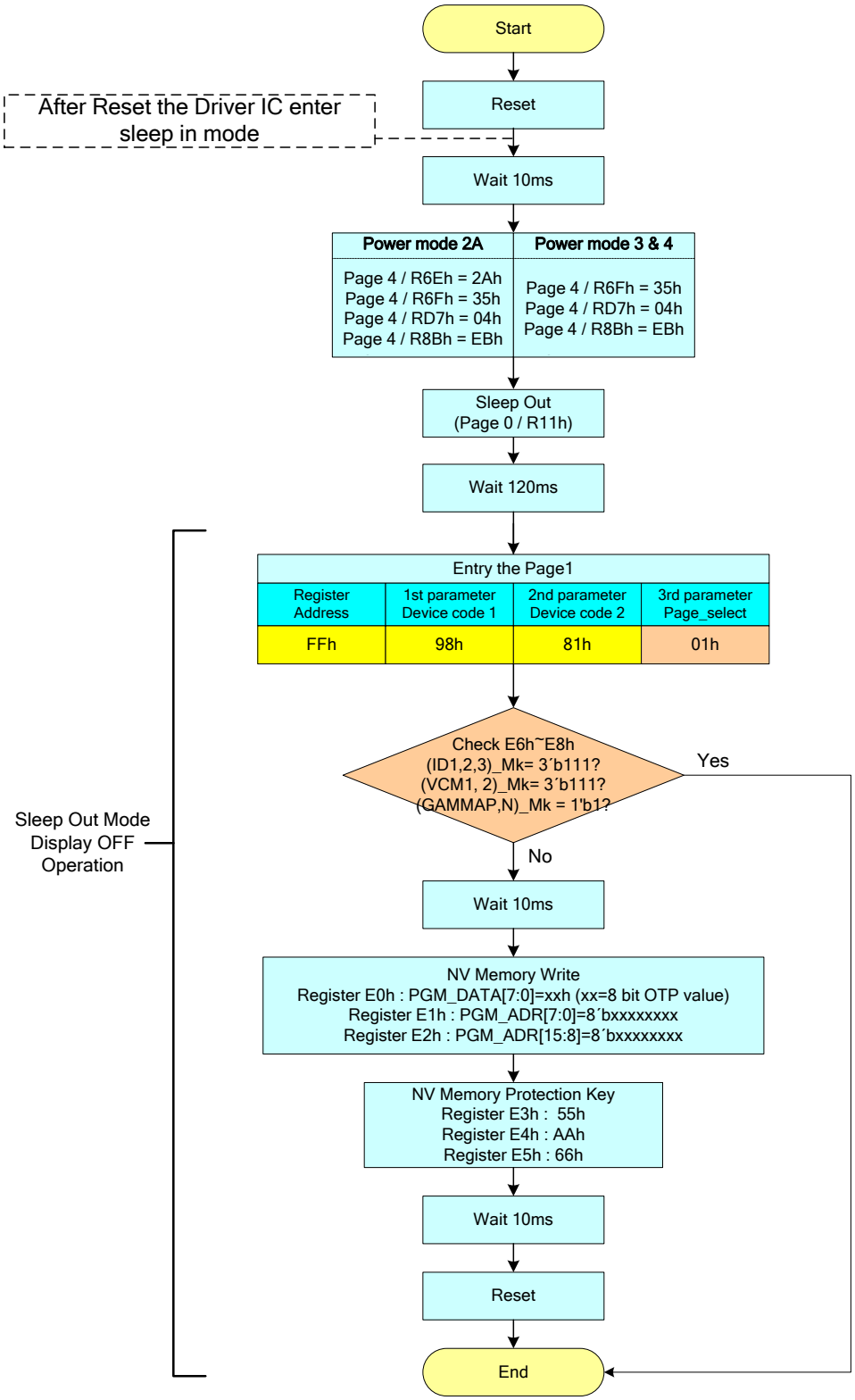


Figure 96: External MTP_PWR 1-Byte Programming Flow

14.2. Internal VGH 1-Byte Programming Flow



Note: Internal VGH Programming must operate in the Low Power mode.

Figure 97: Internal VGH 1-Byte Programming Flow

14.3. Group Programming Flow

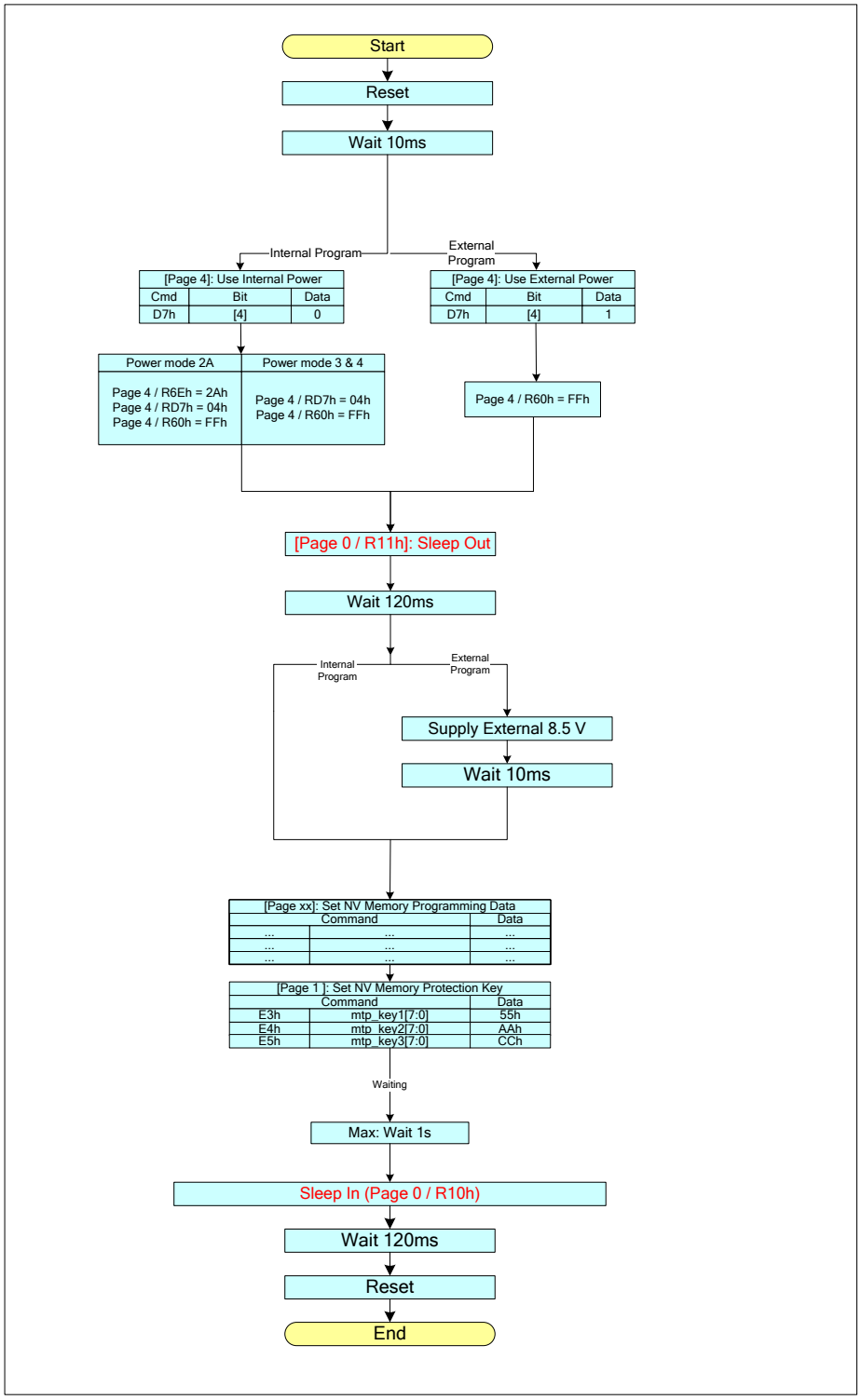


Figure 98: Group Programming Flow

Note : If 1-byte program , VCOM OTP program address is register pg1_cmd_52h~55h,

If auto program, VCOM OTP program address is register pg4_cmd_C4h~C7h

15. Gamma Correction

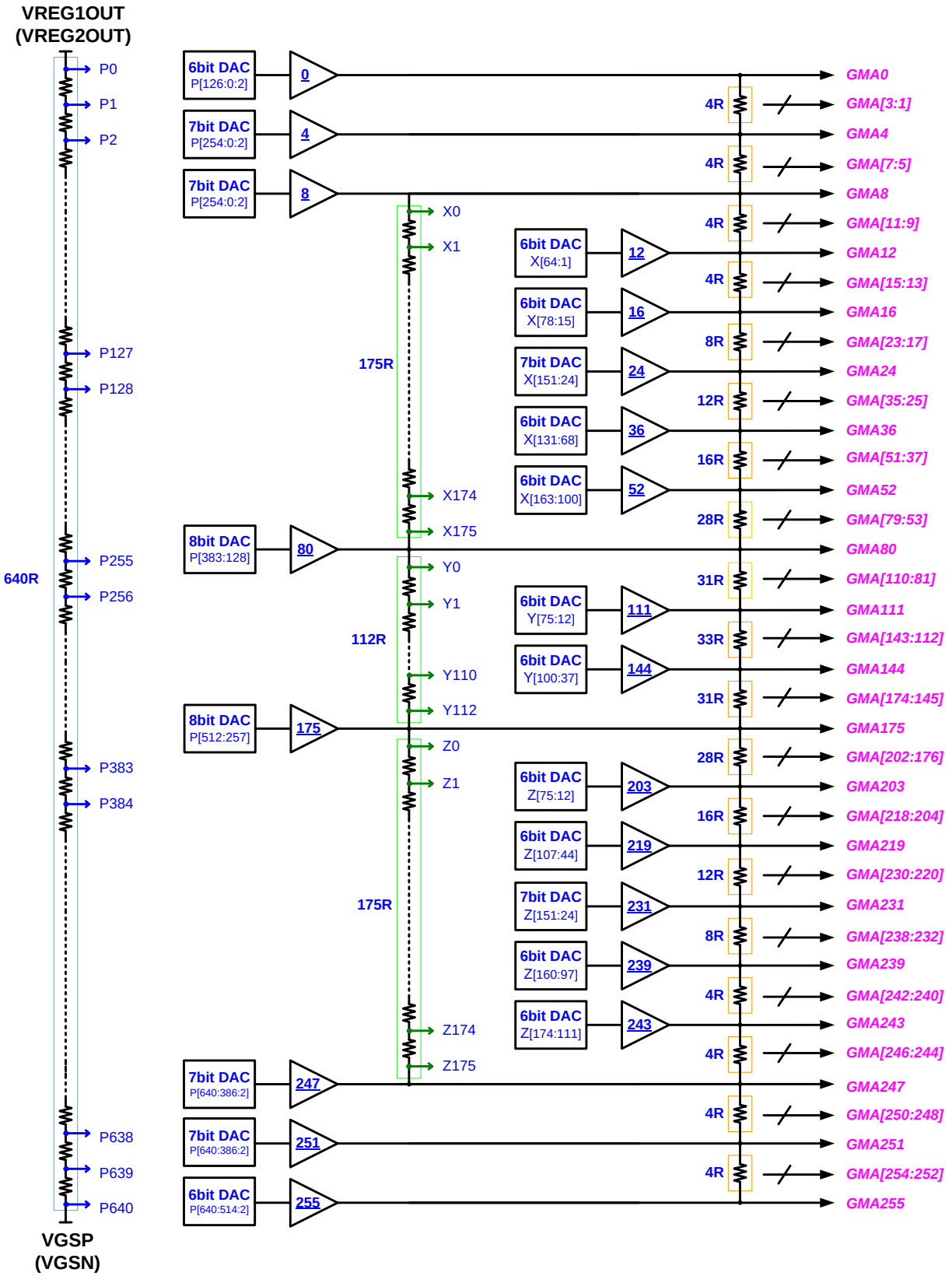


Figure 99: Gamma Architecture

16. Touch Synchronization Signal

The VS and HS pad of ILI9881C-05 can output the synchronization signals to touch sensing signal for touch panel controller. To use these signals, touch panel controller can receive touch sensing signal while avoiding display changing noise.

These signals are consist of vertical synchronization signal: VSOUT and horizontal synchronization signal: HSOUT. The level of output voltage is VDDI to GND. Each signal can adjust output timing for internal synchronization signal. The high level width of VSOUT is 1 line, and it is adjustable. VSOUT is outputted always, but HSOUT is outputted during displaying only.

(1) VSOUT output Timing

VSOUT output means internal VSYNC is starting point. VSOUT output timing can be adjusted by VSOD register. Unit is 1H.

(2) HSOUT output Timing

HSOUT output means internal source output timing is starting point. HSOUT output timing can be adjusted by HSOD register. And HSOUT high level width can be adjusted by HSOHW register.

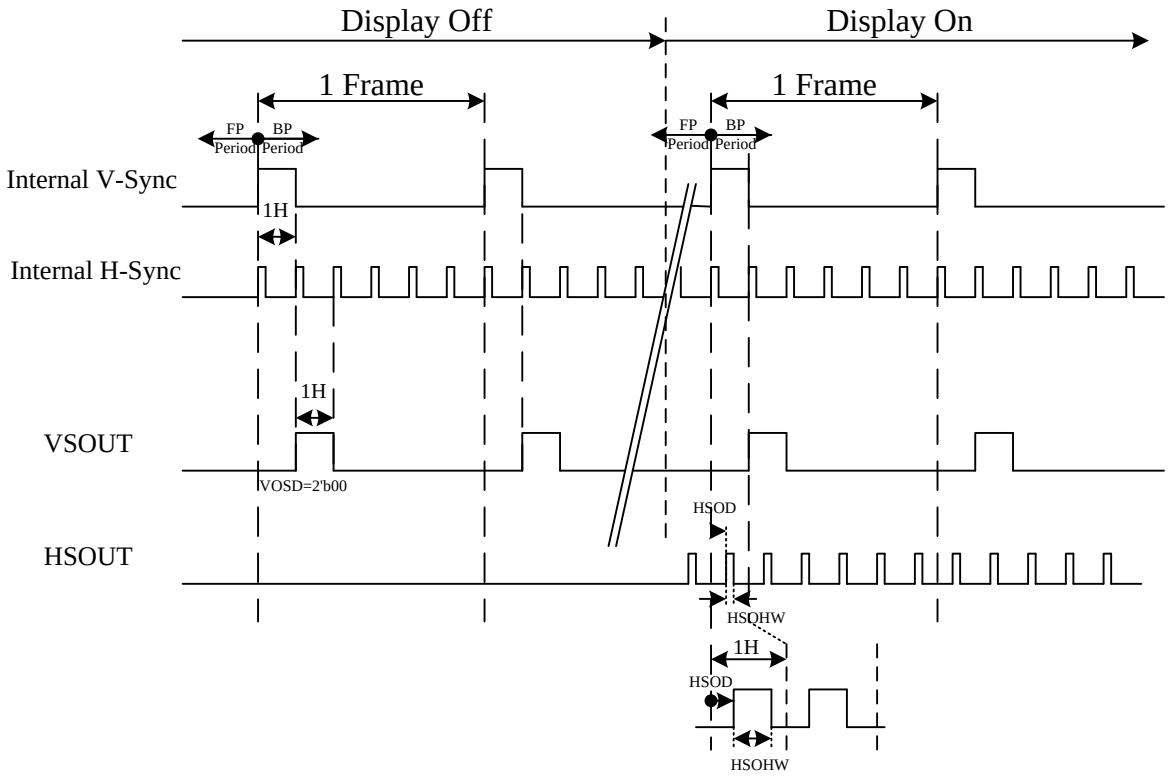


Figure 100: Touch Synchronization Signal

17. Electrical Characteristics

17.1. Absolute Maximum Ratings

The absolute maximum rating is listed in Table 36. When the ILI9881C-05 is used out of the absolute maximum ratings, it may be permanently damaged. To use the ILI9881C-05 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9881C-05 will malfunction and cause poor reliability.

Table 36: Absolute Maximum Ratings

Item	Symbol	Unit	Value
Analog Operating Voltage	VCI ~ GND	V	-0.3 ~ +7.0
Analog Operating Voltage	VCIREF ~ GND	V	-0.3 ~ +7.0
Digital Operating Voltage	VDDI ~ GND	V	-0.3 ~ +3.8
Digital Operating Voltage	VCC1 ~ GND	V	-0.3 ~ +7.0
Digital Operating Voltage	VCC2 ~ GND	V	-0.3 ~ +7.0
DSI Operating Voltage	VDDAM ~ GND	V	-0.3 ~ +3.8
OTP Supply Voltage	MTP_PWR ~ GND	V	-0.3 ~ +9.0
Supply Voltage	VSP ~ GND	V	-0.3 ~ +7.0
Supply Voltage	VSN ~ GND	V	0.3 ~ -7.0
Gate Driver High Voltage	VGH ~ GND	V	-0.3 ~ +18
Gate Driver Low Voltage	VGL ~ GND	V	0.3 ~ -18
Driver Supply Voltage	VDDI - VCL	V	≦ 6.6V
Driver Supply Voltage	VGH - VGL	V	≦ 32.0V
Input Voltage	VIN	V	-0.3 ~ VDDI + 0.3
HS Input Voltage	VHSIN	V	-0.3 ~ + 1.65
Operating Temperature	Topr	℃	-30 ~ +70
Storage Temperature	Tstg	℃	-55 ~ +110

Note: *Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.*

17.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.6	V	
Analog operating voltage	VCIREF		2.5	2.8	6.6	V	
Digital operating voltage	VDDI	-	1.65	2.8	3.6	V	
Digital operating voltage	VCC1		1.65	2.8	6.6	V	
Digital operating voltage	VCC2		1.65	2.8	6.6	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.6	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6.6	V	
Analog operating voltage	VSN	-	-6.6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	|VGH-VGL|	15	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	VSOUT(+)	-	0.3	-	VREG1OUT-0.1	V	Note4
	VSOUT(-)	-	VREG2OUT +0.1	-	-0.3	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.5	-	VSP-0.5 (VSP<=6.1) 5.6 (VSP>6.1)	V	
Negative Gamma Reference Voltage	VREG2OUT	-	VSN+0.5 (VSN>=-6.1) -5.6 (VSN<-6.1)	-	-3.5	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note3
		4.2V>Sout>0.8V	-	-	15	mV	
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note3
Standby mode current consumption							
Sleep In mode	I(VDDI SLP IN)	Ta = 25 °C VCI=2.8V VDDI=1.8V	-	35	-	uA	
	I(VCI SLP IN)		-	25	-	uA	

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Supply digital VDDI voltage equal or less than analog VCI voltage.

3. Source channel loading = 9KΩ,70pF/channel

4. The maximum value is between with Note 3 and Gamma setting value

17.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: *Ta = -30℃ to 70℃ (to +85℃ no damage)*

17.3.1. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

1.Ta = -30℃ to 70℃ (to +85℃ no damage)

2. DSI High Speed mode is off.

17.3.2. Spike/Glitch Rejection

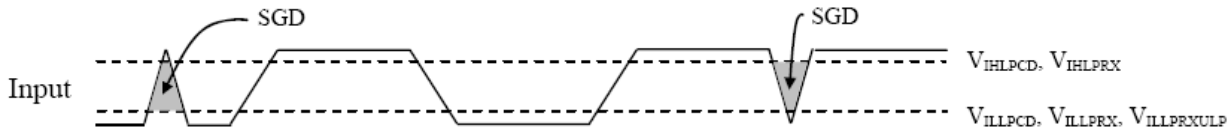


Figure 101: Spike/Glitch Rejection

Notes:

1. *A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and Interference Frequency is 450MHz (at the very least).*
2. *n = 0, 1, 2 and 3.*

Table 37: Spike/Glitch Rejection

Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, DnP/N	SGD	Input pulse rejection for DSI	-	300	Vps

17.3.3. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V

2. Includes 50mV (-50mV to 50mV) ground difference

3. Without VCMRCLKM450/VCMRDATAM450

4. Without 50mV (-50mV to 50mV) ground difference

5. n = 0 and 1

6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than VTHH (CLKP/DnP). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than VTHL (CLKN/DnN). There is undefined state if the differential voltage is less than VTHH (CLKP/DnP) and less than VTHL (CLKN/DnN). A reference figure is below.

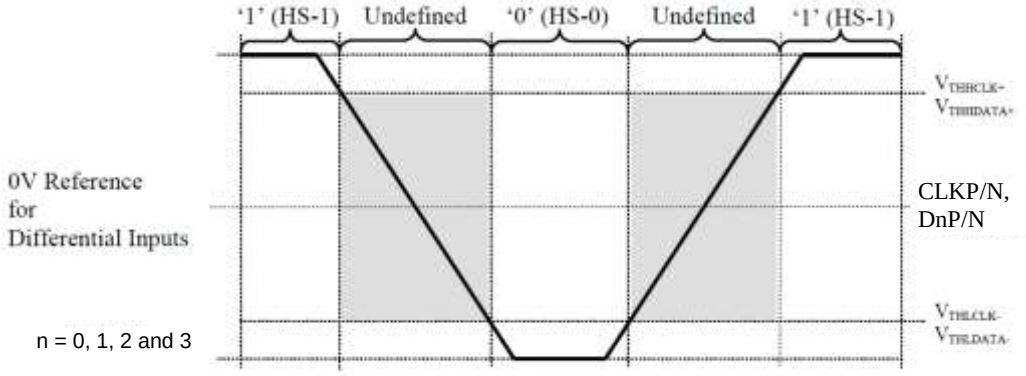
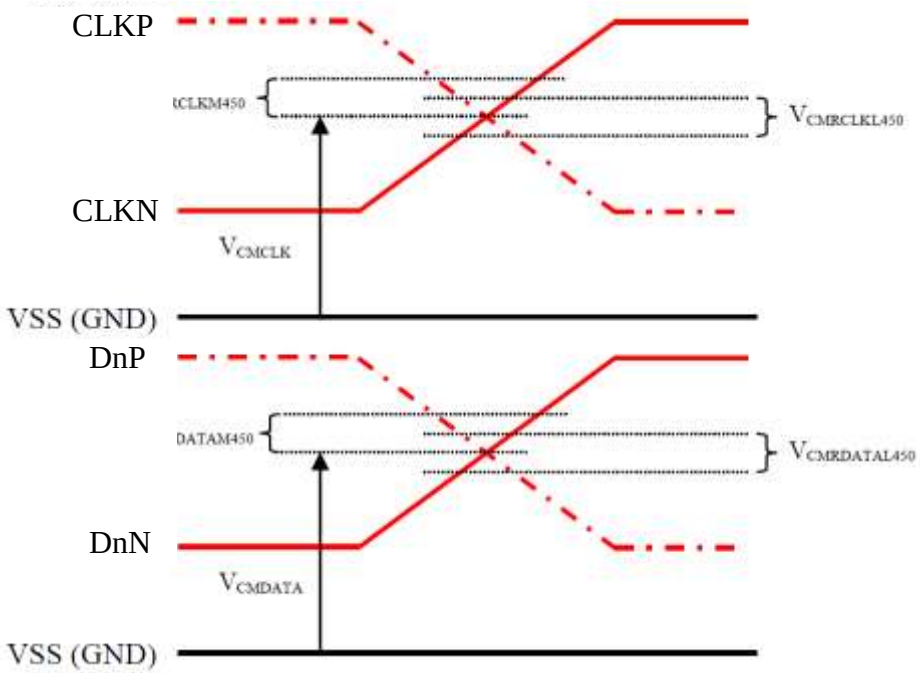


Figure 102: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range



Note: *n = 0, 1, 2 and 3*

Figure 103: Common Mode Voltage on Clock and Data Channels

The termination resistor (RTERM) of the differential DSI receiver can be driven to two different states by the receiver:

- Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)
- High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D2N or D2P <=> D3N or D1P <=> D3N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

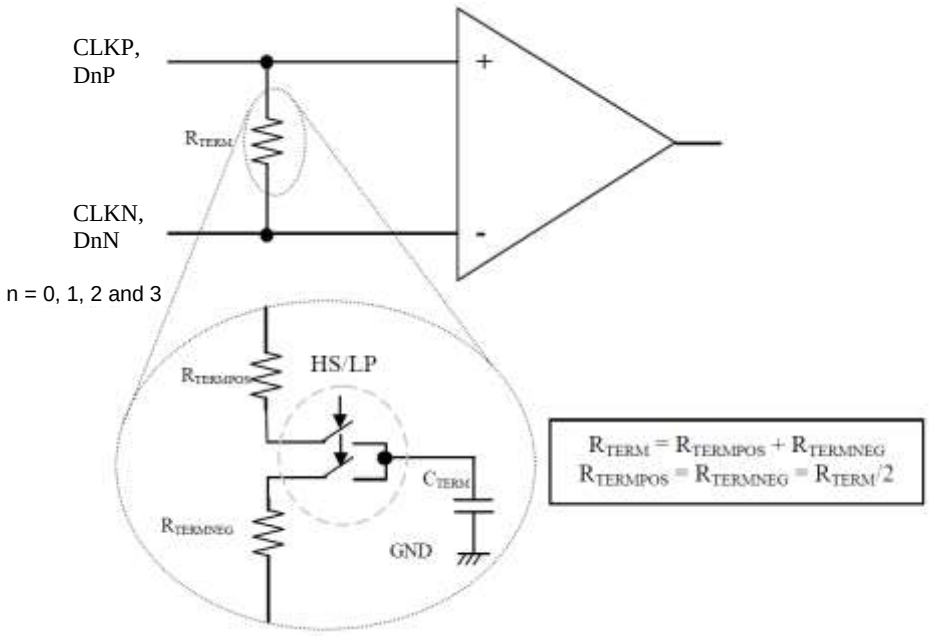


Figure 104: Differential Pair Termination Resistor on the Receiver Side

17.4. AC Characteristics

17.4.1. DSI Timing Characteristics

17.4.2. High Speed Mode – Clock Channel Timing

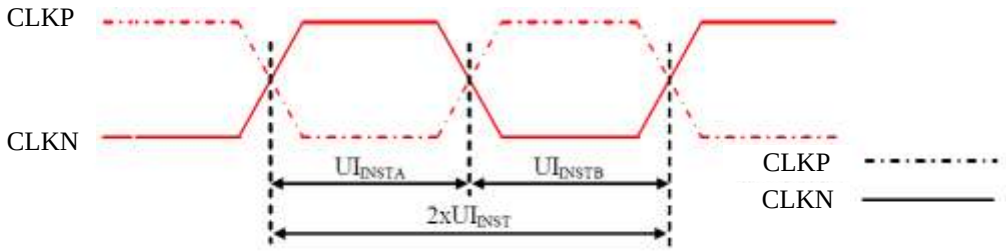


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

17.4.3. High Speed Mode – Data Clock Channel Timing

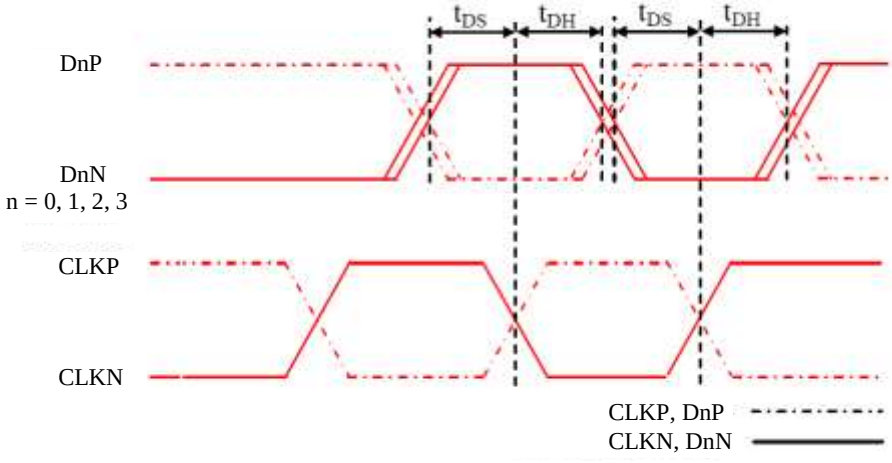


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

17.4.4. High Speed Mode – Rising and Falling Timings

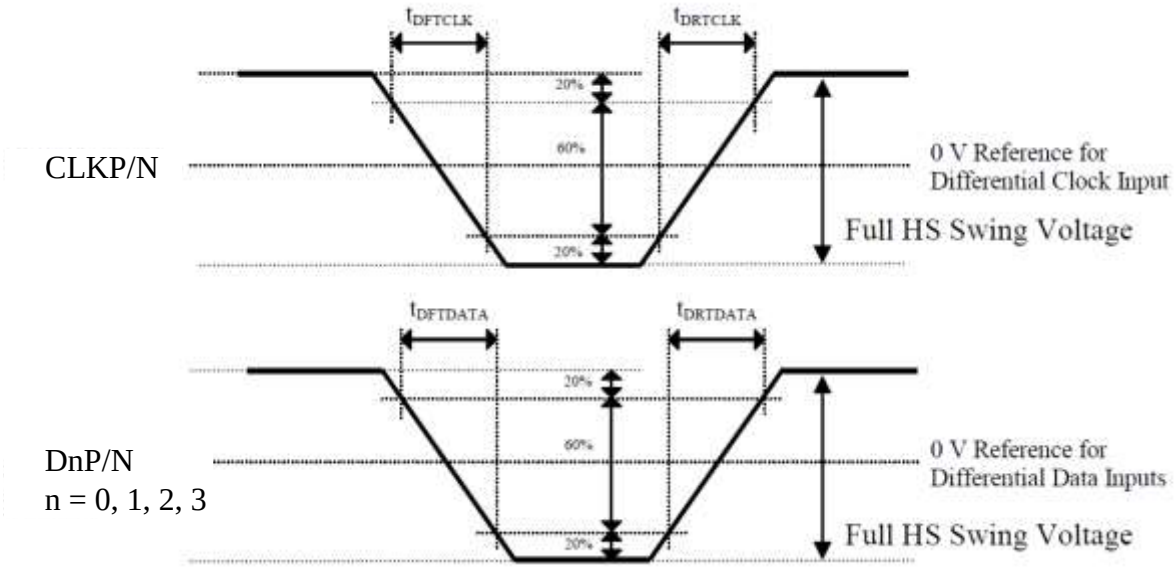


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

17.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-04) are illustrated for reference purposes below.

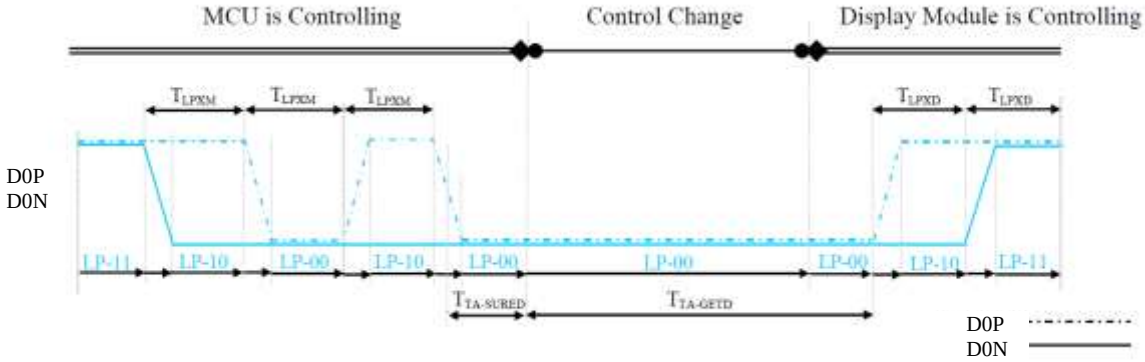


Figure 108: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-04) to the MCU are illustrated for reference purposes below.

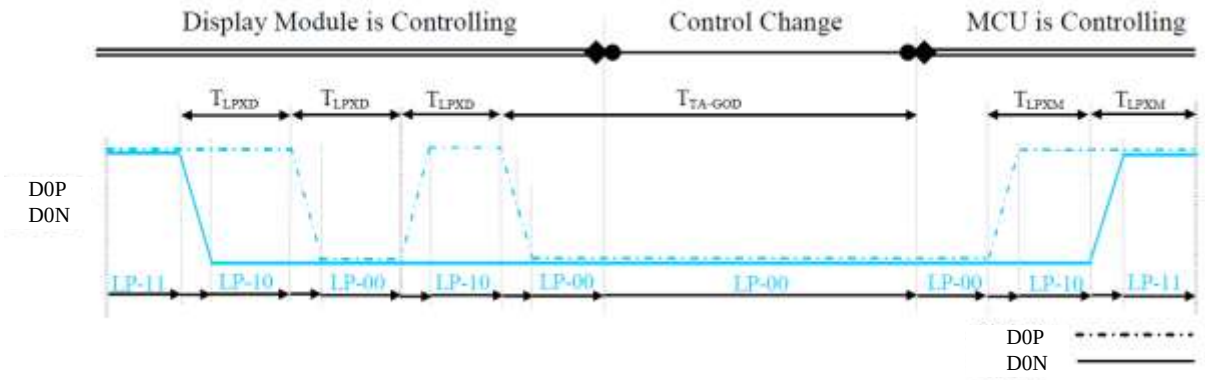


Figure 109: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C-04)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-04) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-04) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-04)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

17.4.6. Data Lanes from Low Power Mode to High Speed Mode

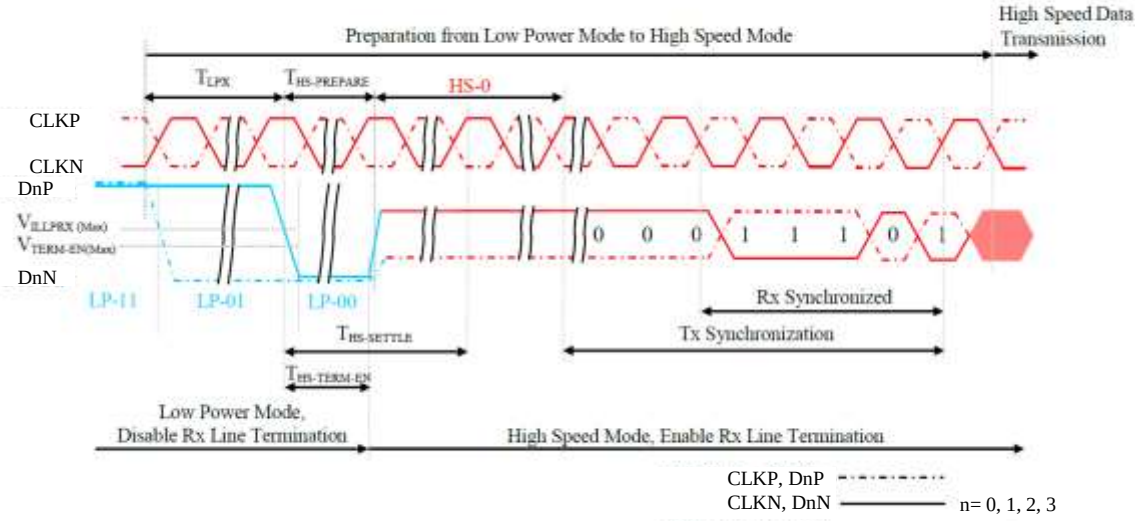


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

17.4.7. Data Lanes from High Speed Mode to Low Power Mode

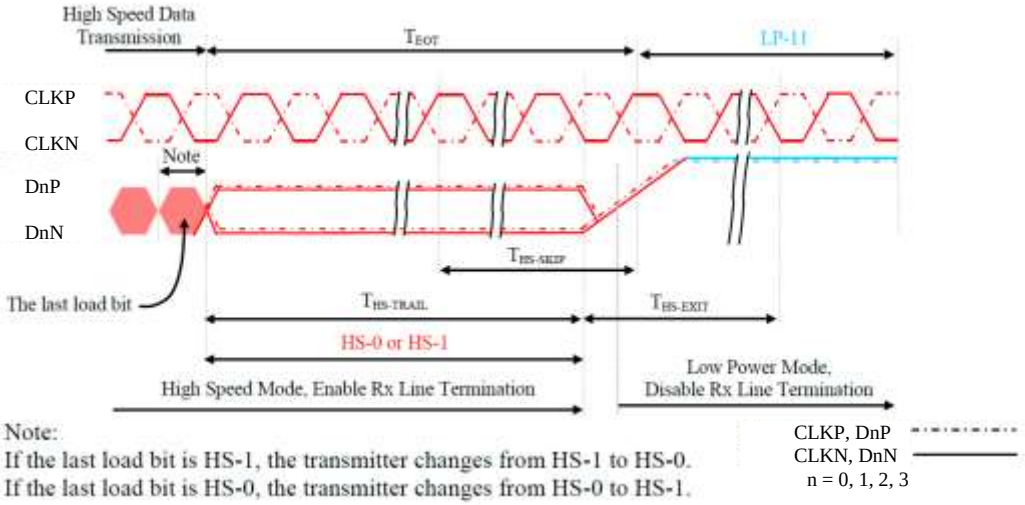


Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

17.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

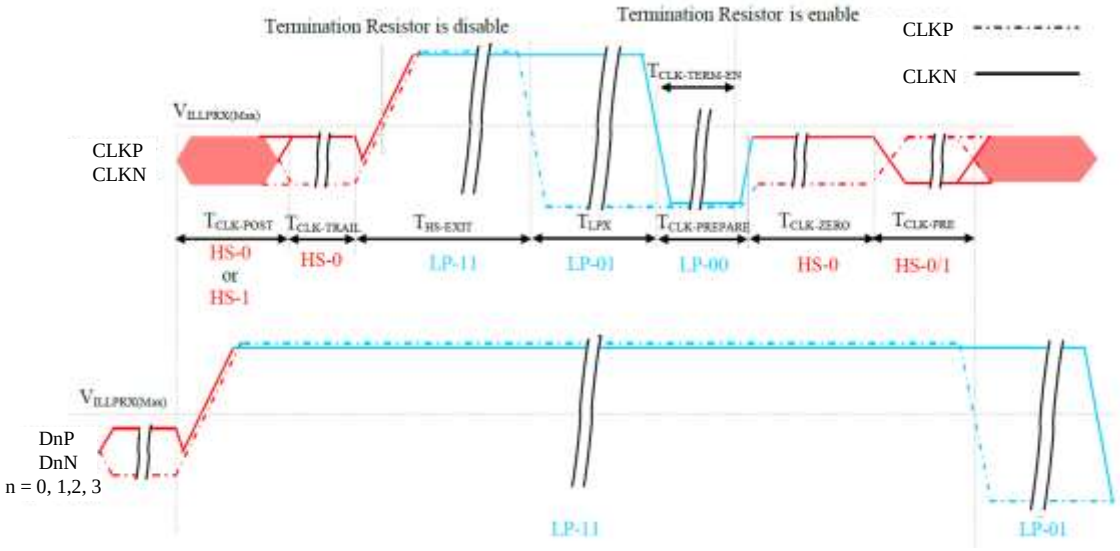
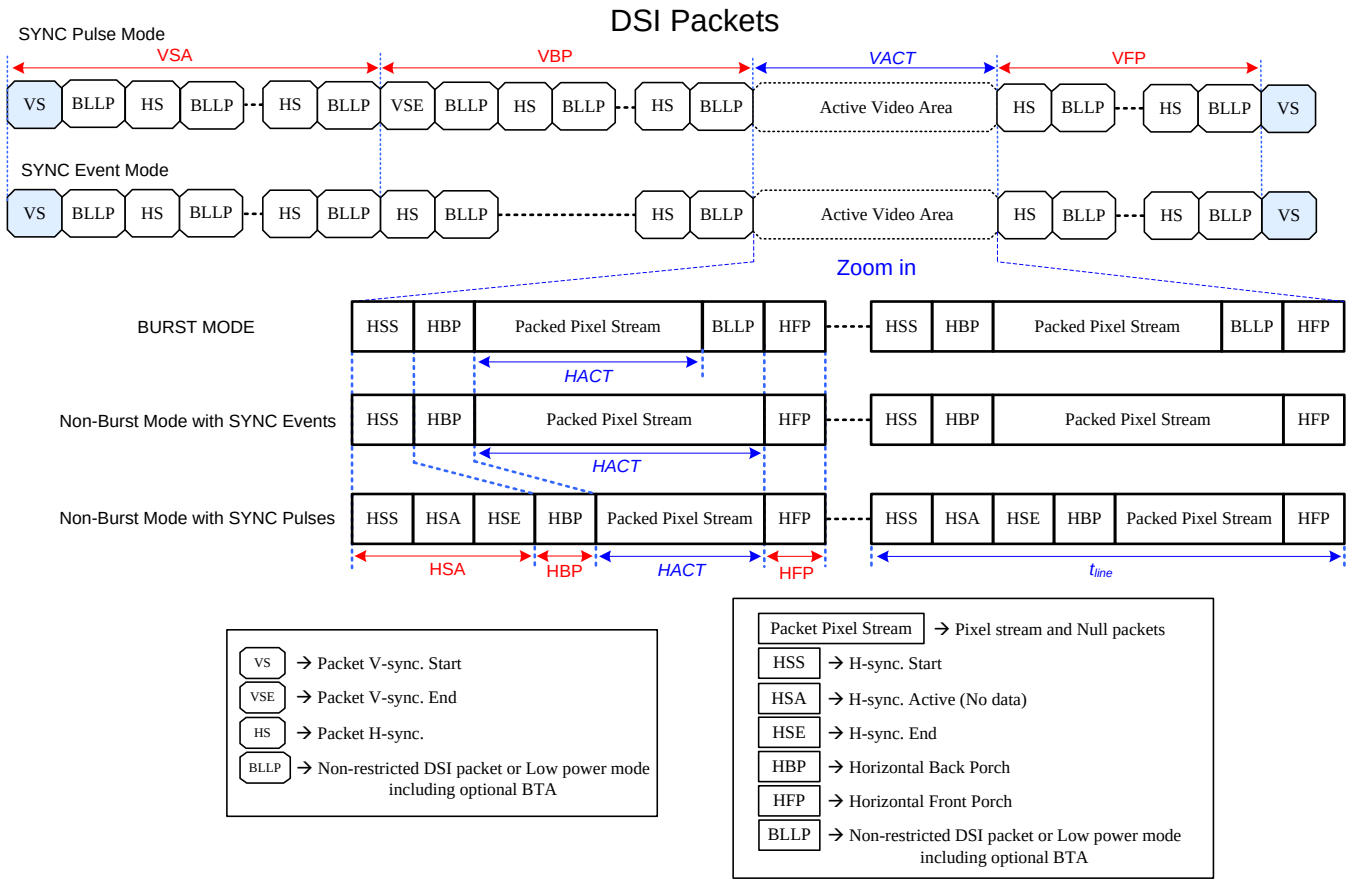


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

17.4.9. Timing for DSI video mode



VS → Packet V-sync. Start
VSE → Packet V-sync. End
HS → Packet H-sync.
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Packet Pixel Stream → Pixel stream and Null packets
HSS → H-sync. Start
HSA → H-sync. Active (No data)
HSE → H-sync. End
HBP → Horizontal Back Porch
HFP → Horizontal Front Porch
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

17.4.10. Reset Timing

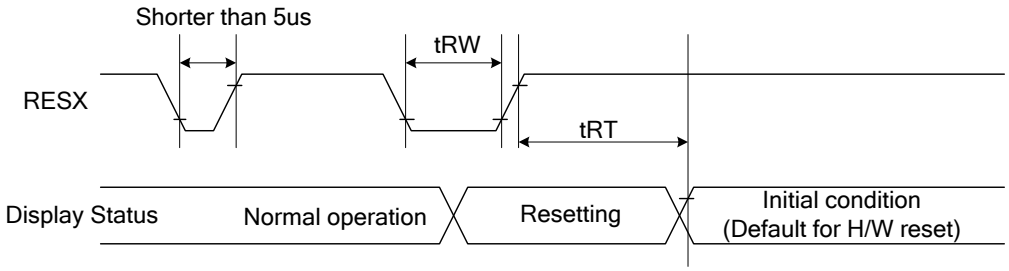


Figure 113: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

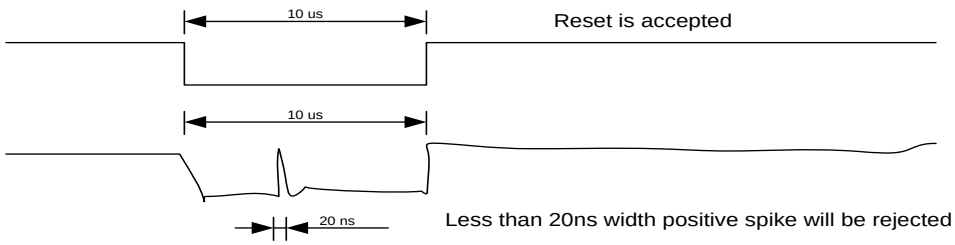


Figure 114: Positive Noise Pulse during Reset Low

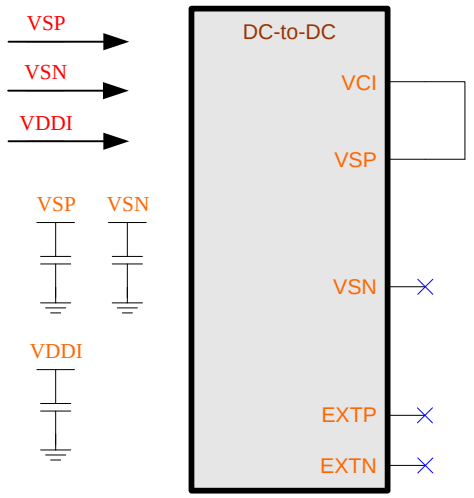
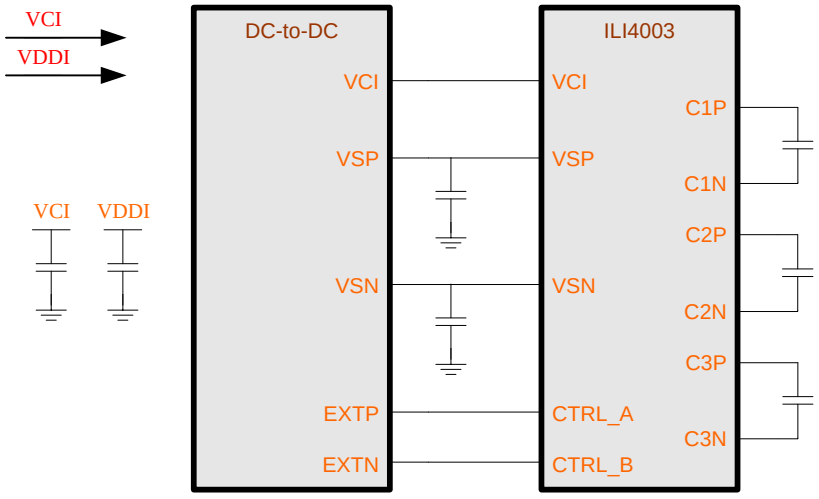
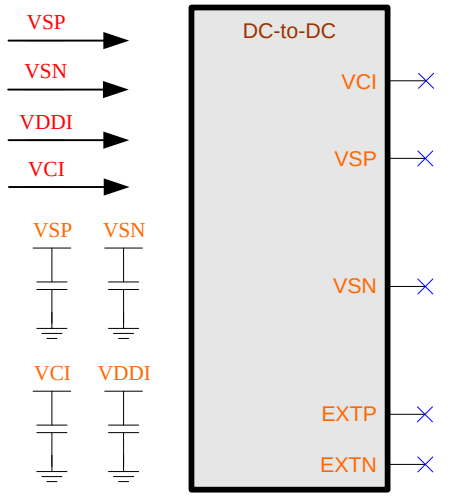
5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

18. Panel Application

18.1. Input Power Type

ILI9881C-04 supports 3 kinds of input power type as shown below.

Table 49: Different Input Power Type

Setting	Input Power Type
Power Mode 2A BOOSTM[2:0] = 1h DI_PWR_REG = 0h	
Power Mode 3 BOOSTM[2:0] = 2h DI_PWR_REG = don't care	
Power Mode 4 BOOSTM[2:0] = 1h DI_PWR_REG = 1h	

18.2. Power Mode 2A (BOOSTM[2:0] = 1h, DI_PWR_REG = 0h)

18.2.1. Power Structure

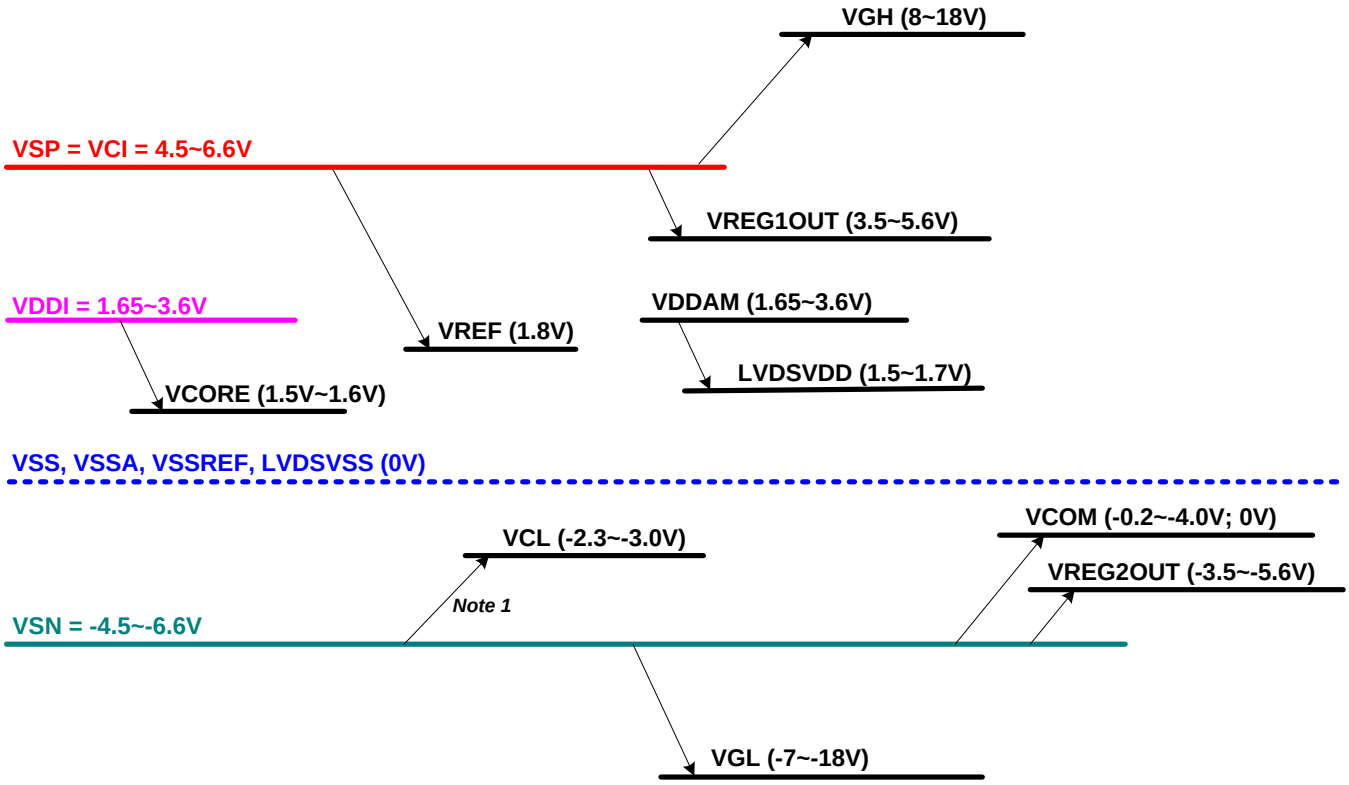


Figure 115: Power Structure of Power Mode 2A

Notes:

1. *Please refer to"5.7.11 Power Control 3 (6Fh)".*
2. *The VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.*

18.2.2. Reference Circuit

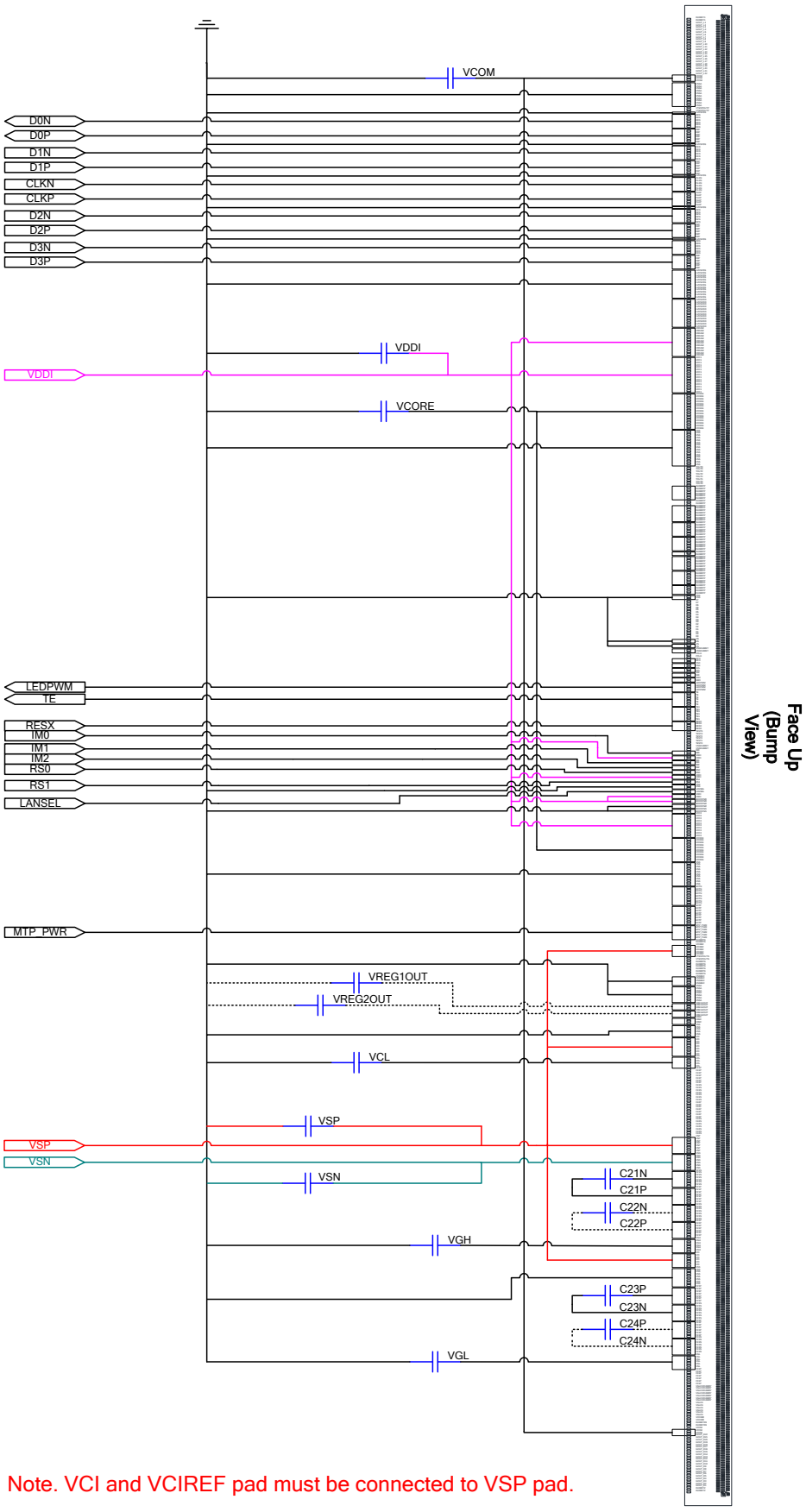


Figure 116: Reference Circuit of Power Mode 2A

18.2.3. External Component

Table 50: External Component table of Power Mode 2A

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VDDI	1.0uF / 6.3V	I/O and Digital Power	
2	VSP	2.2~4.7uF / 10V	Analog Power	
3	VSN	4.7uF / 10V	Analog Power	
4	VCORE	2.2uF / 6.3V		
5	VCL	1.0uF / 6.3V		
6	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.243)
7	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.243)
8	VCOM	2.2uF / 6.3V		
9	VGH	1.0uF / 25V		
10	VGL	1.0uF / 25V		
11	C21P/C21N	1.0uF / 16V		
12	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.242)
13	C23P/C23N	1.0uF / 16V		
14	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.242)

18.3. Power Mode 3 (BOOSTM[2:0] = 2h, DI_PWR_REG = don't care)

18.3.1. Power Structure

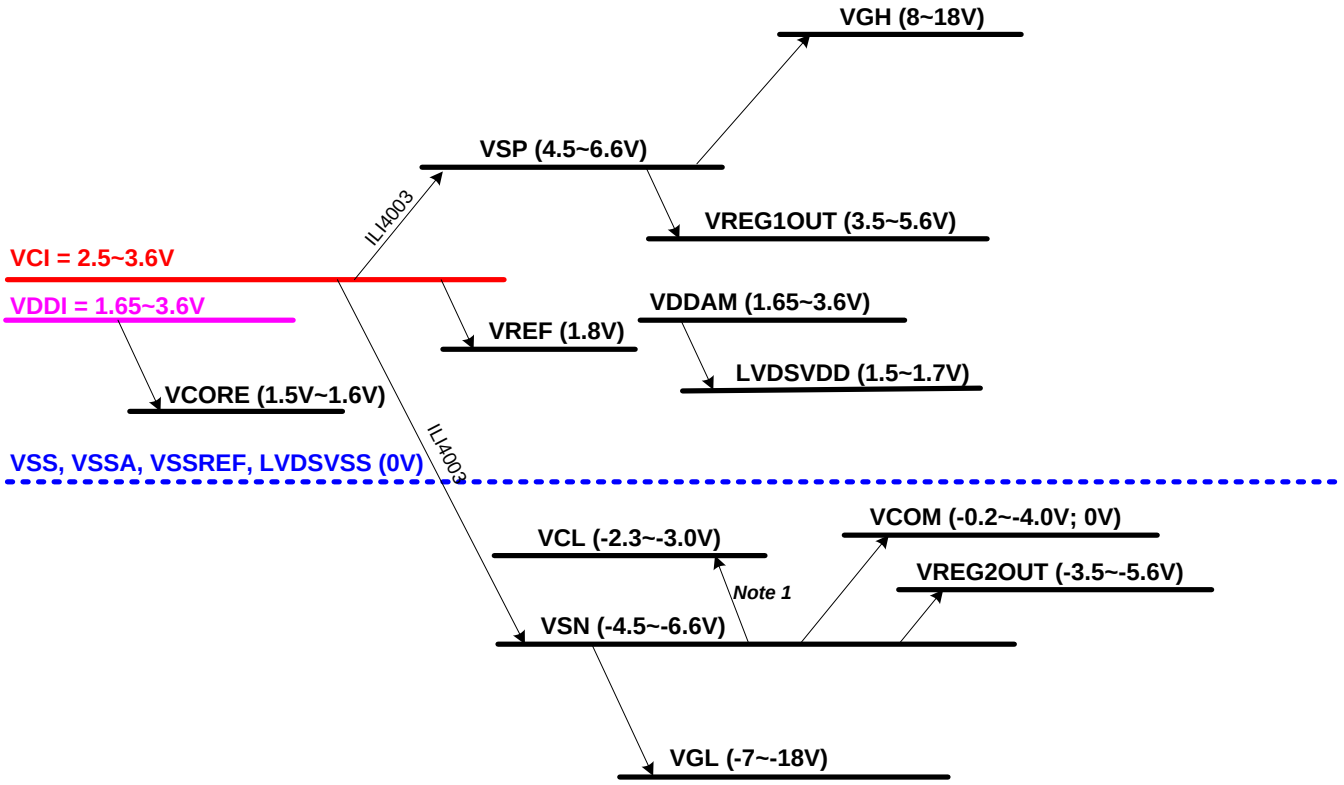


Figure 117: Power Structure of Power Mode 3

Notes:

1. *Please refer to"5.7.11 Power Control 3 (6Fh)".*
2. *The VSP, VSN, VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.*

18.3.2. Reference Circuit

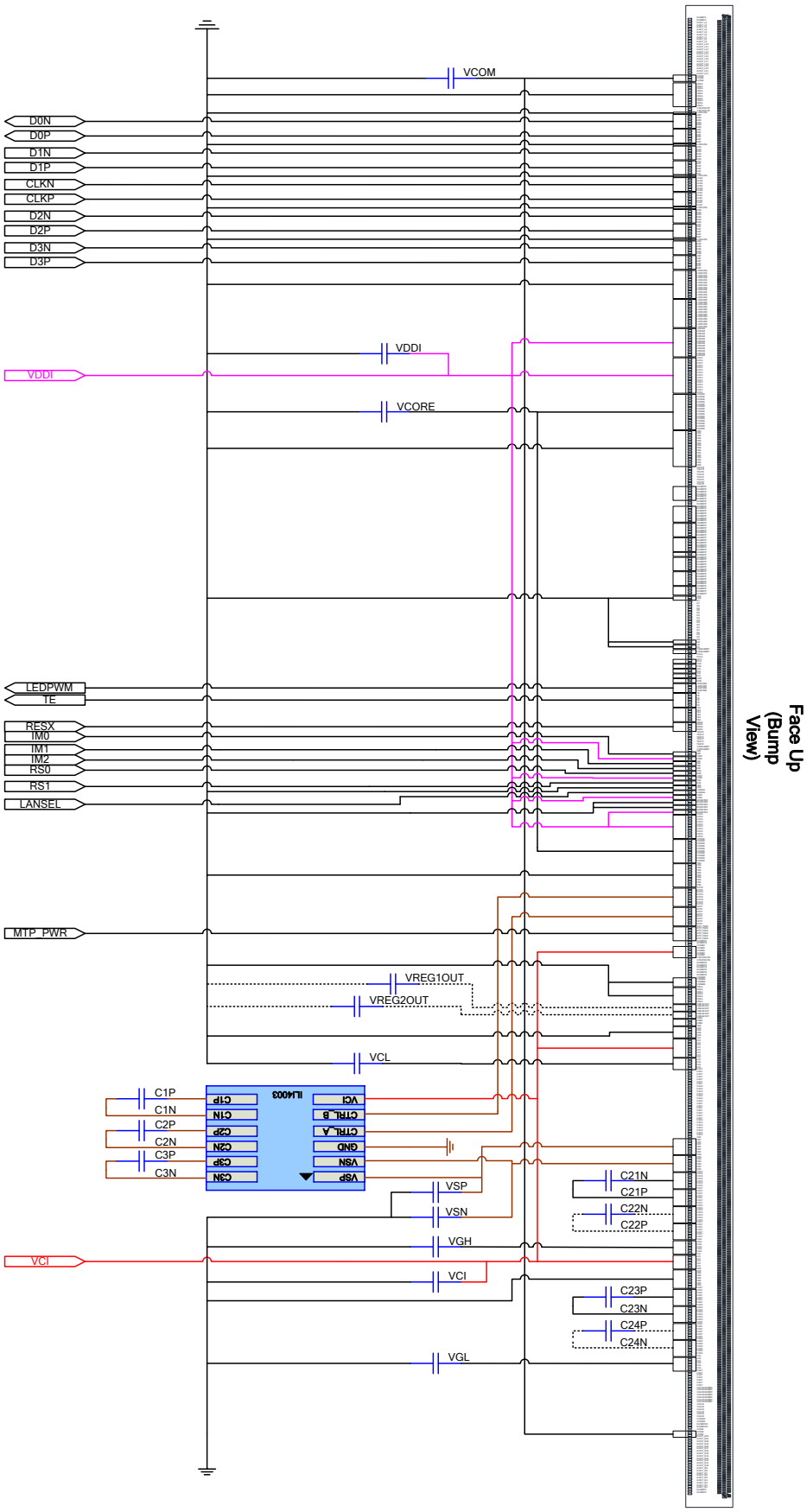


Figure 118: Reference Circuit of Power Mode 3

18.3.3. External Component

Table 51: External Component table of Power Mode 3

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VCI	1.0uF / 6.3V	Analog Power	
2	VDDI	1.0uF / 6.3V	I/O and Digital Power	
3	VSP	2.2~4.7uF / 10V		
4	VSN	2.2~4.7uF / 10V		
5	VCORE	2.2uF / 6.3V		
6	VCL	1.0uF / 6.3V		
7	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.243)
8	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.243)
9	VCOM	2.2uF / 6.3V		
10	VGH	1.0uF / 25V		
11	VGL	1.0uF / 25V		
12	C21P/C21N	1.0uF / 16V		
13	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.242)
14	C23P/C23N	1.0uF / 16V		
15	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.242)
16	Q1		ILI4003	
17	C1P/C1N	2.2uF / 6.3V		
18	C2P/C2N	2.2uF / 6.3V		
19	C3P/C3N	2.2uF / 6.3V		

18.4. Power Mode 4 (BOOSTM[2:0] = 1h, DI_PWR_REG = 1h)

18.4.1. Power Structure

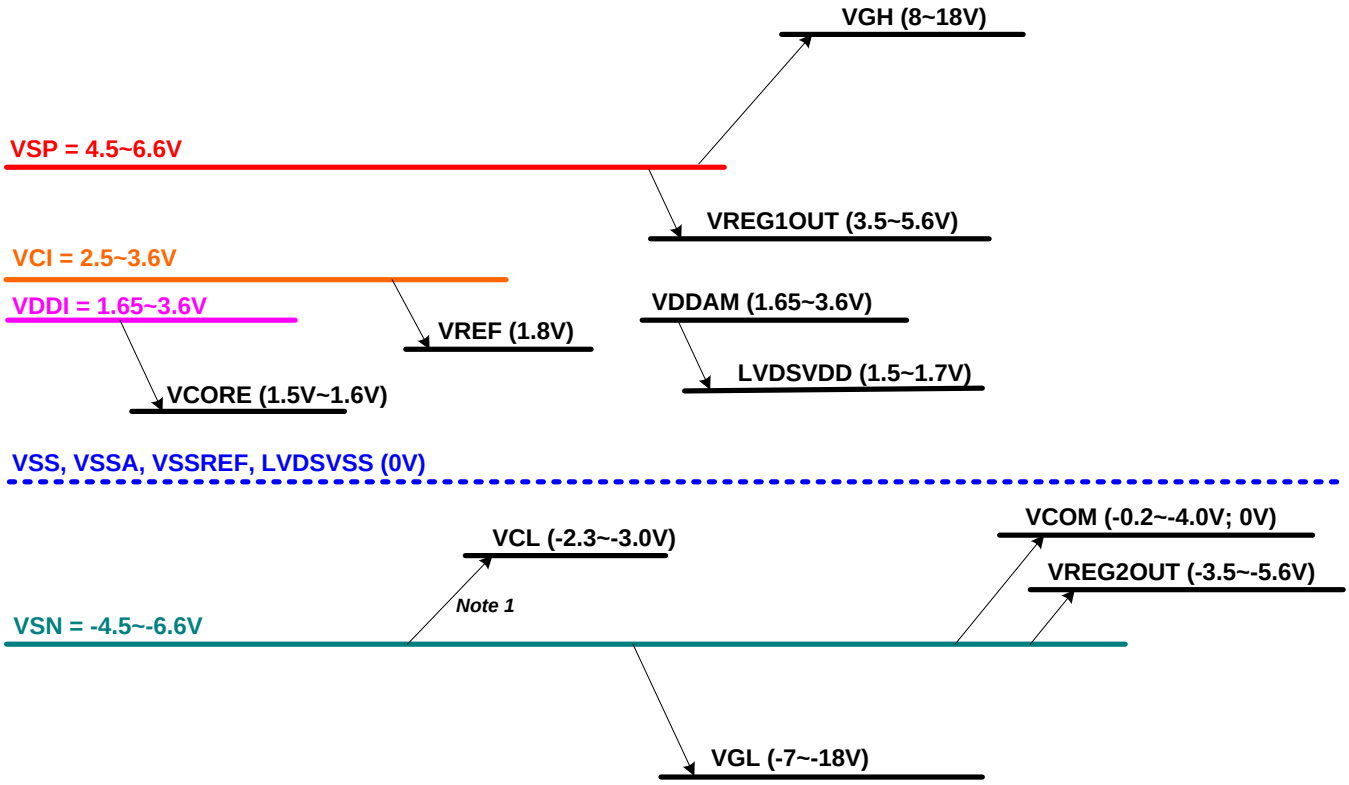


Figure 119: Power Structure of Power Mode 4

Notes:

1. *Please refer to"5.7.11 Power Control 3 (6Fh)".*
2. *The VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.*

18.4.2. Reference Circuit

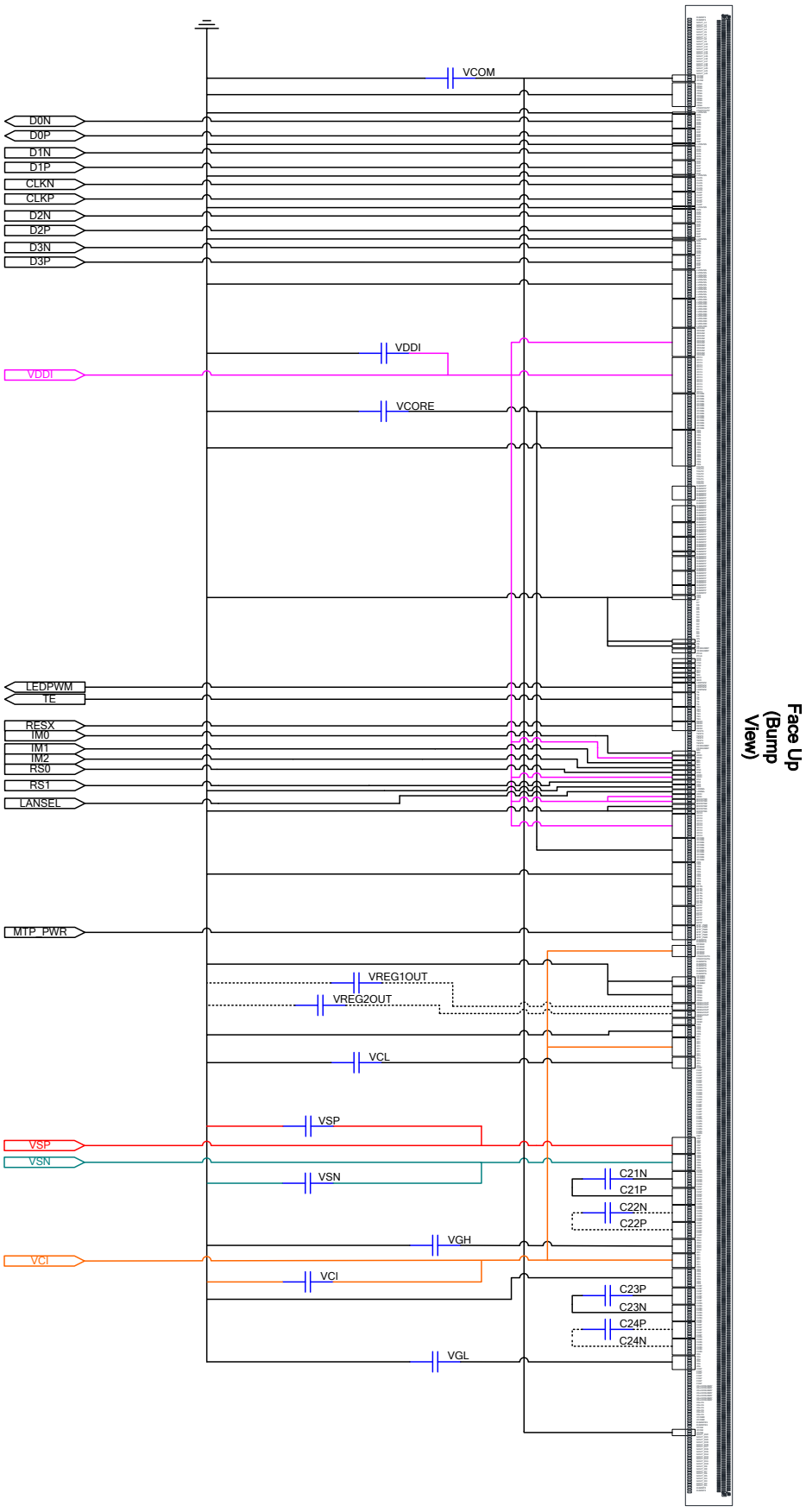


Figure 120: Reference Circuit of Power Mode 4

18.4.3. External Component

Table 52: External Component table of Power Mode 4

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VDDI	1.0uF / 6.3V	I/O and Digital Power	
2	VCI	1.0uF / 6.3V	Analog Power	
3	VSP	2.2~4.7uF / 10V	Analog Power	
4	VSN	4.7uF / 10V	Analog Power	
5	VCORE	2.2uF / 6.3V		
6	VCL	1.0uF / 6.3V		
7	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.243)
8	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.243)
9	VCOM	2.2uF / 6.3V		
10	VGH	1.0uF / 25V		
11	VGL	1.0uF / 25V		
12	C21P/C21N	1.0uF / 16V		
13	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.242)
14	C23P/C23N	1.0uF / 16V		
15	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.242)

18.5. Maximum Layout Resistance

Table 53: Maximum Layout Resistance

Pad Name	Type	Maximum series resistance	Unit
VCI	Power Supply	5	Ω
VCIREF	Power Supply	10	Ω
VDDI	Power Supply	5	Ω
VCC1	Power Supply	5	Ω
VCC2	Power Supply	5	Ω
VDDAM	Power Supply	5	Ω
VSP	Power Supply	5	Ω
VSN	Power Supply	5	Ω
VSSA	Ground	5	Ω
VSSREF	Ground	10	Ω
LVDSVSS	Ground	50	Ω
VSS	Ground	5	Ω
MTP_PWR	Power Supply	5	Ω
VREG1OUT	Analog	20	Ω
VERG2OUT	Analog	20	Ω
VCL	Analog	5	Ω
VGH	Analog	10	Ω
VGL	Analog	10	Ω
EXTP	Output	10	Ω
EXTN	Output	10	Ω
LVDSVDD	Analog	5	Ω
VREF	Analog	20	Ω
VCORE	Analog	5	Ω
C21P, C21N, C22P, C22N C23P, C23N, C24P, C24N	Step-up Capacitor	5	Ω
IM[2:0], RS[1:0] LANSEL, BOOSTM[2:0]	Input	100	Ω
RESX	Input	100	Ω
TE, TE1, LEDPWM	Output	50	Ω
CLKP, CLKN D1P, D1N D2P, D2N D3P, D3N	Input	5	Ω
D0P, D0N	Input + Output	5	Ω
CSX, DCX, SCL, SDI	Input	100	Ω
SDO	Output	100	Ω
GOUT_L[22:1] GOUT_R[22:1]	Output	10	Ω
VCOM	Analog	5	Ω
VTESTOUTP	Analog	100	Ω
VTESTOUTN	Analog	100	Ω
TOUT[3:0]	Input + Output	100	Ω
TEST[5:0]	Input + Output	100	Ω
VS, HS	Input + Output	100	Ω
PCLK	Input	100	Ω
D[7:0]	Input + Output	50	Ω

19. Liquid Crystal Power Supply Specifications

Table 54: Liquid Crystal Power Supply Specifications

Item		Description
TFT Source Driver		2404 pins , 800(RGB)
TFT Gate Driver Control Signal		44 pins
TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
Liquid Crystal Drive Output	S1 ~ 2400, SDUM[3:0]	V0 ~ V255 grayscales
	GOUT_L/R[22:1]	VGH – VGL
	VCOM	-4.0 ~ -0.2V; 0V
Input Power Voltage	VCI	2.50 ~ 6.6V
	VCIREF	2.50 ~ 6.6V
	VDDI	1.65 ~ 3.6V
	VCC1	1.65 ~ 6.6V
	VCC2	1.65 ~ 6.6V
	VDDAM	1.65 ~ 3.6V
	VSP	4.5 ~ 6.6V
	VSN	-6.6 ~ -4.5V
Liquid Crystal Drive Voltages	VGH	8.0V ~ 18.0V
	VGL	-18.0V ~ -7.0V
	VCL	-3.0V ~ -2.3V
	VGH – VGL	Max. 32.0V
Internal Step-up Circuits	VGH	2xVSP or 2.5xVSP or 3*VSP or 3.5*VSP or 4*VSP or 4.5*VSP or 5*VSP
	VGL	-1.5xVSP or -2xVSP or -2.5xVSP or -3xVSP or -3.5xVSP or -4xVSP or -4.5xVSP or -5xVSP

20. Revision History

Version No.	Date	Page	Description
V100	2020/02/26	All	New created