Integrated Solutions Technology,Inc.	Title IST1305CA1-B Specification 200 segment x16 common PMOLED Driver	文件編號 DOC# IST-RD-0319	版次 Rev 002
		生效日期 Effective Date : 2026/03/09	

Specification

資料中心參考文件用章
For Reference Only
2026.03.10
To:智晶
聯合聚晶股份有限公司
Integrated Solution Technology, Inc

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	Alex Huang 2026.03.09	Henry Tsai 2026.03.09	Bonnie Lee 2026.03.09

Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
	--	--	--	✓	✓	✓	--

文件變更履歷頁
Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
001	--	New Release	E11240006	Sean	11/26/2024
002	P56	Modify READ Mode from 0 to 1	E03260002	Alex	2026/03/09

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

DESCRIPTION

IST1305CA1-B is a 200 segment x16 common PMOLED drivers with controller specially designed for alphanumeric symbols display.It can display up to 40-Character x 2-Line.

FEATURES

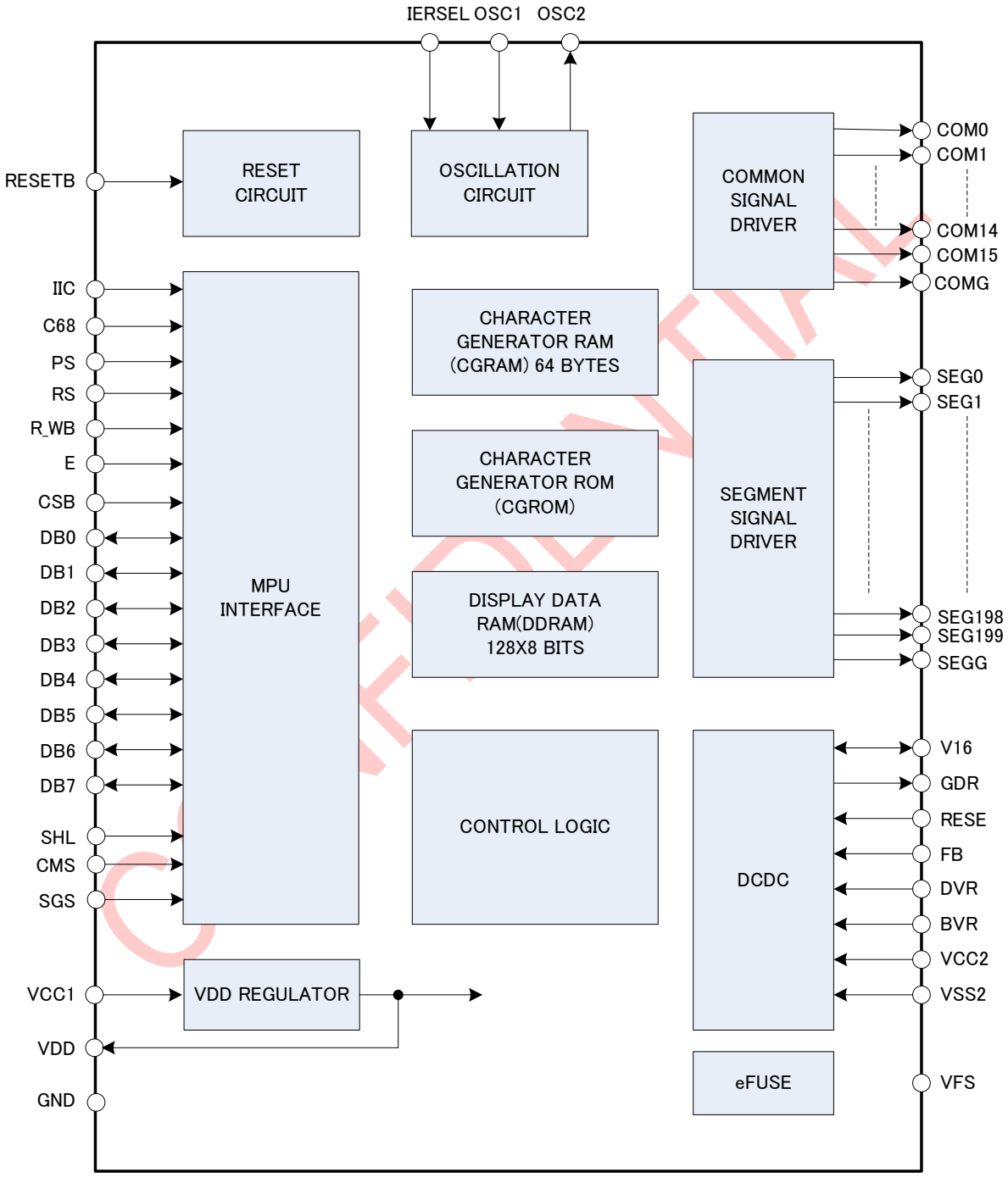
- Microprocessor Interface
  - 80/68-series 4bit/8bit parallel bi-directional interface (2Mhz@VDD=5V)
  - SPI3/SPI4 interface
  - IIC interface

- Key Features
  - 128 x8-bit Display RAM (128 characters max.)
  - 5 x8 and 5 x10 dot character selectable
  - Programmable duty cycle
    - 1/8 duty (1 display line, 5x8 dots with cursor)
    - 1/11 duty (1 display line, 5x10 dots with cursor)
    - 1/16 duty (2 display lines, 5x8 dots with cursor)
  - Build-in four sets of character generator ROM (CGROM)
    - English Japanese Character
    - English Russian Character
    - Western European Character I & II
  - Build-in 64x8-bits character generator RAM (CGRAM)
    - 8 character fonts of 5x8 dot matrix
    - 4 character fonts of 5x10 dot matrix
  - Embedded DC-DC voltage converter
  - Embedded oscillator with internal or external resistors
  - Embedded Power-On reset function
  - Package: COG (min. pitch = 28um)

- Ordering Information

Ordering Part Number	Package Form	Remark
IST1305CA1-B	COG	● Die Thickness: 250+/- 15um

BLOCK DIAGRAM



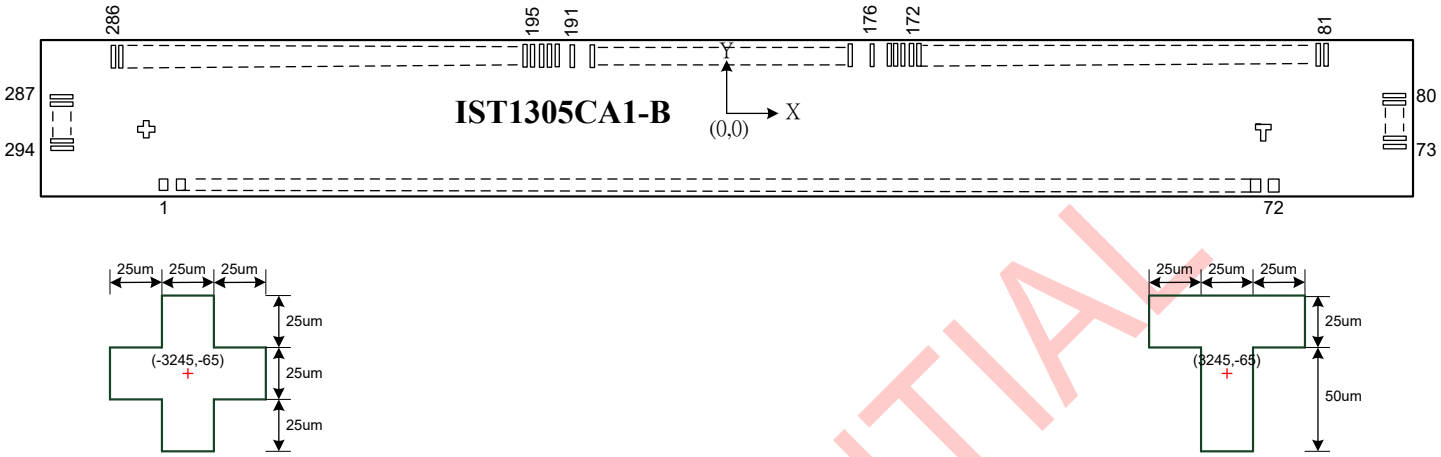
PAD DESCRIPTION

Pin	I/O	Description
SEG0 ~ SEG199	O	Segment driver output pins
COM0 ~ COM15	O	Common driver output pins
SEGG	Power	OLED SEG drive power supply (0V)
COMG	Power	OLED COM drive power supply (0V)
VCC1	Power	Logic power pin (2.7V~5.5V)
VDD	Power	Internal core power pin (connect to a stabilization capacitor)
GND	Power	Logic ground pin (0V)
VCC2	Power	DCDC buffer Power Supply (2.7 to 5.5V): This is the power supply pin for the GDR pin buffer. It must be connected when the converter is used.
VSS2	Power	DCDC buffer power supply (0V): This is the GND pin for the GDR pin buffer. It must be connected when the converter is used.
OSC1	I	Oscillator Input Pin
OSC2	O	Oscillator Output Pin
IERSEL	I	IERSEL=H : internal res oscillator IERSEL=L : external res oscillator
SHL	I	Data shift direction pin. User can this pin to decide display direction SHL=H,SEG0>>SEG199 SHL=L,SEG199>>SEG0
CSB	I	Chip select input pins Data / instruction I/O is enabled only when CSB is “L”.
RESETB	I	Reset pin. When RESETB is “L”, the chip will be initialized to it’s default state.

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>IIC,
PS,
C68</td><td>I</td><td>I/O interface configuration pins.
<table>
<tr><th>IIC</th><th>PS</th><th>C68</th><th>Interface</th><th>Relevant Pins</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>SPI3</td><td>DB7(SDI)/DB6(SDO)/DB5(SCL)/CSB</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>SPI4</td><td>DB7(SDI)/DB6(SDO)/DB5(SCL)/CSB/RS</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>8080-series</td><td>DB7~DB6/E(RDB)/R_WB(WRB)/CSB/RS</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>6800-series</td><td>DB7~DB6/E/R_WB/CSB/RS</td></tr>
<tr><td>H</td><td>H/L</td><td>H/L</td><td>IIC</td><td>DB7(SDI)/DB6(SDO)/DB5(SCL)</td></tr>
</table></td></tr>
<tr><td>RS</td><td>I</td><td>Register Select Input Pin
When this pin is set to "0", it is used as an Instruction Register.
When this pin is set to "1", it is used for as the Data Register.
When select SPI3 & IIC interface, RS need keep H.</td></tr>
<tr><td>DB0~DB7</td><td>I/O</td><td>I/O interface data pins
These pins are used for data transfer and reception between the MPU and IST1305CA1-B. DB0~DB3 are not used during a 4-bit operation. DB7 can be used as a Busy Flag.
<table>
<tr><th>Interface</th><th>Data In</th><th>Data Out</th><th>Serial Clock</th></tr>
<tr><td>SPI3</td><td>DB7(SDI)</td><td>DB6(SDO)</td><td>DB5(SCL)</td></tr>
<tr><td>SPI4</td><td>DB7(SDI)</td><td>DB6(SDO)</td><td>DB5(SCL)</td></tr>
<tr><td>8080-series</td><td>DB0 to DB7</td><td>DB0 to DB7</td><td>---</td></tr>
<tr><td>6800-series</td><td>DB0 to DB7</td><td>DB0 to DB7</td><td>---</td></tr>
<tr><td>IIC</td><td>DB7(SDI)</td><td>DB6(SDO)</td><td>DB5(SCL)</td></tr>
</table>
Unused pin need keep H.</td></tr>
<tr><td>E,
R_WB</td><td>I</td><td>Read/Write Control Input Pin
<table>
<tr><th>Interface</th><th>E</th><th>R_WB</th></tr>
<tr><td>6800-series</td><td>Data Read/Write control</td><td>Read/Write indicator</td></tr>
<tr><td>8080-series</td><td>Data read enable control (RDB)</td><td>Data write enable control (WRB)</td></tr>
</table>
When select SPI3/4 & IIC interface, E&R_WB need keep H.</td></tr>
</table>

Pin Name	I/O	Description
V16	I	This is the most positive voltage supply pin of the chip. It can be supplied externally or generated. internally by using internal DC-DC voltage converter.
RESE	I	NMOS source input pin This pin connects to the source current pin of the external NMOS of the booster circuit.
GDR	O	Gate drive pulse output pin This output pin drives the gate of external NMOS of the booster circuit.
FB	I	Feedback voltage input pin: This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level.
DVR	I	Pre charge time control
BVR	I	Brightness control pin
VFS	I	For Test , Please keep floating or VSS
CMS	I	COM output mapping selection
SGS	I	Configuration Pin, Please keep VSS

PAD CONFIGURATION



ChipSize	7100 um x 550 um(Exclude Scribe Line)	
BumpPitch	90um(min)	
	28um (min) (Pad No. = 73~175,176~294)	
	82um(min) (Pad No.= 176~191)	
Bump Space	24um (min) (Pad No. = 1~72)	
	12um (min) (Pad No. =73~175,192~294)	
	62um(min) (Pad No. = 176~191)	
Bump Size(X*Y)	66x61um2	Pad No. = 1~72
	16x95 um2	Pad No.= 73~175,192~294
	20x95um2	Pad No.= 176~191
Bump Height	9um(Typ)	
Chip Thickness	250um (Typ) +/- 15um	

PAD LOCATION

Pad No.	Pad Name	X-Co.	Y-Co.	X-Size	Y-Size	Pad No.	Pad Name	X-Co.	Y-Co.	X-Size	Y-Size
1	COMG	-3343	-236	66	61	51	DVR	1357	-236	66	61
2	COMG	-3245	-236	66	61	52	RESE	1447	-236	66	61
3	COMG	-3147	-236	66	61	53	FB	1537	-236	66	61
4	COMG	-3049	-236	66	61	54	BVR	1627	-236	66	61
5	COMG	-2951	-236	66	61	55	VCC1	1717	-236	66	61
6	SEGG	-2853	-236	66	61	56	GDR	1807	-236	66	61
7	SEGG	-2755	-236	66	61	57	VCC2	1897	-236	66	61
8	V16	-2657	-236	66	61	58	VCC2	1987	-236	66	61
9	V16	-2559	-236	66	61	59	VSS2	2077	-236	66	61
10	V16	-2461	-236	66	61	60	VSS2	2167	-236	66	61
11	V16	-2363	-236	66	61	61	V16	2265	-236	66	61
12	V16	-2265	-236	66	61	62	V16	2363	-236	66	61
13	VFS	-2167	-236	66	61	63	V16	2461	-236	66	61
14	VCC1	-2077	-236	66	61	64	V16	2559	-236	66	61
15	SHL	-1987	-236	66	61	65	V16	2657	-236	66	61
16	GND!	-1897	-236	66	61	66	SEGG	2755	-236	66	61
17	C68	-1807	-236	66	61	67	SEGG	2853	-236	66	61
18	VCC1	-1717	-236	66	61	68	COMG	2951	-236	66	61
19	PS	-1627	-236	66	61	69	COMG	3049	-236	66	61
20	GND!	-1537	-236	66	61	70	COMG	3147	-236	66	61
21	CMS	-1447	-236	66	61	71	COMG	3245	-236	66	61
22	SGS	-1357	-236	66	61	72	COMG	3343	-236	66	61
23	VCC1	-1267	-236	66	61	73	SEG<199>	3489.5	-141.1	95	16
24	IIC	-1177	-236	66	61	74	SEG<197>	3489.5	-113.1	95	16
25	GND!	-1087	-236	66	61	75	SEG<195>	3489.5	-85.1	95	16
26	RESETB	-997	-236	66	61	76	SEG<193>	3489.5	-57.1	95	16
27	DB<7>	-899	-236	66	61	77	SEG<191>	3489.5	-29.1	95	16
28	DB<6>	-801	-236	66	61	78	SEG<189>	3489.5	-1.1	95	16
29	DB<5>	-703	-236	66	61	79	SEG<187>	3489.5	26.9	95	16
30	DB<4>	-605	-236	66	61	80	SEG<185>	3489.5	54.9	95	16
31	DB<3>	-507	-236	66	61	81	SEG<183>	3329	214.5	16	95
32	DB<2>	-409	-236	66	61	82	SEG<181>	3301	214.5	16	95
33	DB<1>	-311	-236	66	61	83	SEG<179>	3273	214.5	16	95
34	DB<0>	-213	-236	66	61	84	SEG<177>	3245	214.5	16	95
35	VCC1	-115	-236	66	61	85	SEG<175>	3217	214.5	16	95
36	R_WB	-17	-236	66	61	86	SEG<173>	3189	214.5	16	95
37	E	81	-236	66	61	87	SEG<171>	3161	214.5	16	95
38	RS	179	-236	66	61	88	SEG<169>	3133	214.5	16	95
39	CSB	277	-236	66	61	89	SEG<167>	3105	214.5	16	95
40	VDD!	367	-236	66	61	90	SEG<165>	3077	214.5	16	95
41	VDD!	457	-236	66	61	91	SEG<163>	3049	214.5	16	95
42	GND!	547	-236	66	61	92	SEG<161>	3021	214.5	16	95
43	GND!	637	-236	66	61	93	SEG<159>	2993	214.5	16	95
44	GND!	727	-236	66	61	94	SEG<157>	2965	214.5	16	95
45	IERSEL	817	-236	66	61	95	SEG<155>	2937	214.5	16	95
46	VCC1	907	-236	66	61	96	SEG<153>	2909	214.5	16	95
47	VCC1	997	-236	66	61	97	SEG<151>	2881	214.5	16	95
48	VCC1	1087	-236	66	61	98	SEG<149>	2853	214.5	16	95
49	OSC2	1177	-236	66	61	99	SEG<147>	2825	214.5	16	95
50	OSC1	1267	-236	66	61	100	SEG<145>	2797	214.5	16	95

Pad No.	Pad Name	X-Co.	Y-Co.	X-Size	Y-Size	Pad No.	Pad Name	X-Co.	Y-Co.	X-Size	Y-Size
101	SEG<143>	2769	214.5	16	95	151	SEG<43>	1369	214.5	16	95
102	SEG<141>	2741	214.5	16	95	152	SEG<41>	1341	214.5	16	95
103	SEG<139>	2713	214.5	16	95	153	SEG<39>	1313	214.5	16	95
104	SEG<137>	2685	214.5	16	95	154	SEG<37>	1285	214.5	16	95
105	SEG<135>	2657	214.5	16	95	155	SEG<35>	1257	214.5	16	95
106	SEG<133>	2629	214.5	16	95	156	SEG<33>	1229	214.5	16	95
107	SEG<131>	2601	214.5	16	95	157	SEG<31>	1201	214.5	16	95
108	SEG<129>	2573	214.5	16	95	158	SEG<29>	1173	214.5	16	95
109	SEG<127>	2545	214.5	16	95	159	SEG<27>	1145	214.5	16	95
110	SEG<125>	2517	214.5	16	95	160	SEG<25>	1117	214.5	16	95
111	SEG<123>	2489	214.5	16	95	161	SEG<23>	1089	214.5	16	95
112	SEG<121>	2461	214.5	16	95	162	SEG<21>	1061	214.5	16	95
113	SEG<119>	2433	214.5	16	95	163	SEG<19>	1033	214.5	16	95
114	SEG<117>	2405	214.5	16	95	164	SEG<17>	1005	214.5	16	95
115	SEG<115>	2377	214.5	16	95	165	SEG<15>	977	214.5	16	95
116	SEG<113>	2349	214.5	16	95	166	SEG<13>	949	214.5	16	95
117	SEG<111>	2321	214.5	16	95	167	SEG<11>	921	214.5	16	95
118	SEG<109>	2293	214.5	16	95	168	SEG<9>	893	214.5	16	95
119	SEG<107>	2265	214.5	16	95	169	SEG<7>	865	214.5	16	95
120	SEG<105>	2237	214.5	16	95	170	SEG<5>	837	214.5	16	95
121	SEG<103>	2209	214.5	16	95	171	SEG<3>	809	214.5	16	95
122	SEG<101>	2181	214.5	16	95	172	SEG<1>	781	214.5	16	95
123	SEG<99>	2153	214.5	16	95	173	NC	753	214.5	16	95
124	SEG<97>	2125	214.5	16	95	174	NC	725	214.5	16	95
125	SEG<95>	2097	214.5	16	95	175	NC	697	214.5	16	95
126	SEG<93>	2069	214.5	16	95	176	COM<15>	615	214.5	20	95
127	SEG<91>	2041	214.5	16	95	177	COM<14>	533	214.5	20	95
128	SEG<89>	2013	214.5	16	95	178	COM<13>	451	214.5	20	95
129	SEG<87>	1985	214.5	16	95	179	COM<12>	369	214.5	20	95
130	SEG<85>	1957	214.5	16	95	180	COM<11>	287	214.5	20	95
131	SEG<83>	1929	214.5	16	95	181	COM<10>	205	214.5	20	95
132	SEG<81>	1901	214.5	16	95	182	COM<9>	123	214.5	20	95
133	SEG<79>	1873	214.5	16	95	183	COM<8>	41	214.5	20	95
134	SEG<77>	1845	214.5	16	95	184	COM<7>	-41	214.5	20	95
135	SEG<75>	1817	214.5	16	95	185	COM<6>	-123	214.5	20	95
136	SEG<73>	1789	214.5	16	95	186	COM<5>	-205	214.5	20	95
137	SEG<71>	1761	214.5	16	95	187	COM<4>	-287	214.5	20	95
138	SEG<69>	1733	214.5	16	95	188	COM<3>	-369	214.5	20	95
139	SEG<67>	1705	214.5	16	95	189	COM<2>	-451	214.5	20	95
140	SEG<65>	1677	214.5	16	95	190	COM<1>	-533	214.5	20	95
141	SEG<63>	1649	214.5	16	95	191	COM<0>	-615	214.5	20	95
142	SEG<61>	1621	214.5	16	95	192	NC	-697	214.5	16	95
143	SEG<59>	1593	214.5	16	95	193	NC	-725	214.5	16	95
144	SEG<57>	1565	214.5	16	95	194	NC	-753	214.5	16	95
145	SEG<55>	1537	214.5	16	95	195	SEG<0>	-781	214.5	16	95
146	SEG<53>	1509	214.5	16	95	196	SEG<2>	-809	214.5	16	95
147	SEG<51>	1481	214.5	16	95	197	SEG<4>	-837	214.5	16	95
148	SEG<49>	1453	214.5	16	95	198	SEG<6>	-865	214.5	16	95
149	SEG<47>	1425	214.5	16	95	199	SEG<8>	-893	214.5	16	95
150	SEG<45>	1397	214.5	16	95	200	SEG<10>	-921	214.5	16	95

Pad No.	Pad Name	X-Co.	Y-Co.	X-Size	Y-Size	Pad No.	Pad Name	X-Co.	Y-Co.	X-Size	Y-Size
201	SEG<12>	-949	214.5	16	95	251	SEG<112>	-2349	214.5	16	95
202	SEG<14>	-977	214.5	16	95	252	SEG<114>	-2377	214.5	16	95
203	SEG<16>	-1005	214.5	16	95	253	SEG<116>	-2405	214.5	16	95
204	SEG<18>	-1033	214.5	16	95	254	SEG<118>	-2433	214.5	16	95
205	SEG<20>	-1061	214.5	16	95	255	SEG<120>	-2461	214.5	16	95
206	SEG<22>	-1089	214.5	16	95	256	SEG<122>	-2489	214.5	16	95
207	SEG<24>	-1117	214.5	16	95	257	SEG<124>	-2517	214.5	16	95
208	SEG<26>	-1145	214.5	16	95	258	SEG<126>	-2545	214.5	16	95
209	SEG<28>	-1173	214.5	16	95	259	SEG<128>	-2573	214.5	16	95
210	SEG<30>	-1201	214.5	16	95	260	SEG<130>	-2601	214.5	16	95
211	SEG<32>	-1229	214.5	16	95	261	SEG<132>	-2629	214.5	16	95
212	SEG<34>	-1257	214.5	16	95	262	SEG<134>	-2657	214.5	16	95
213	SEG<36>	-1285	214.5	16	95	263	SEG<136>	-2685	214.5	16	95
214	SEG<38>	-1313	214.5	16	95	264	SEG<138>	-2713	214.5	16	95
215	SEG<40>	-1341	214.5	16	95	265	SEG<140>	-2741	214.5	16	95
216	SEG<42>	-1369	214.5	16	95	266	SEG<142>	-2769	214.5	16	95
217	SEG<44>	-1397	214.5	16	95	267	SEG<144>	-2797	214.5	16	95
218	SEG<46>	-1425	214.5	16	95	268	SEG<146>	-2825	214.5	16	95
219	SEG<48>	-1453	214.5	16	95	269	SEG<148>	-2853	214.5	16	95
220	SEG<50>	-1481	214.5	16	95	270	SEG<150>	-2881	214.5	16	95
221	SEG<52>	-1509	214.5	16	95	271	SEG<152>	-2909	214.5	16	95
222	SEG<54>	-1537	214.5	16	95	272	SEG<154>	-2937	214.5	16	95
223	SEG<56>	-1565	214.5	16	95	273	SEG<156>	-2965	214.5	16	95
224	SEG<58>	-1593	214.5	16	95	274	SEG<158>	-2993	214.5	16	95
225	SEG<60>	-1621	214.5	16	95	275	SEG<160>	-3021	214.5	16	95
226	SEG<62>	-1649	214.5	16	95	276	SEG<162>	-3049	214.5	16	95
227	SEG<64>	-1677	214.5	16	95	277	SEG<164>	-3077	214.5	16	95
228	SEG<66>	-1705	214.5	16	95	278	SEG<166>	-3105	214.5	16	95
229	SEG<68>	-1733	214.5	16	95	279	SEG<168>	-3133	214.5	16	95
230	SEG<70>	-1761	214.5	16	95	280	SEG<170>	-3161	214.5	16	95
231	SEG<72>	-1789	214.5	16	95	281	SEG<172>	-3189	214.5	16	95
232	SEG<74>	-1817	214.5	16	95	282	SEG<174>	-3217	214.5	16	95
233	SEG<76>	-1845	214.5	16	95	283	SEG<176>	-3245	214.5	16	95
234	SEG<78>	-1873	214.5	16	95	284	SEG<178>	-3273	214.5	16	95
235	SEG<80>	-1901	214.5	16	95	285	SEG<180>	-3301	214.5	16	95
236	SEG<82>	-1929	214.5	16	95	286	SEG<182>	-3329	214.5	16	95
237	SEG<84>	-1957	214.5	16	95	287	SEG<184>	-3489.5	54.9	95	16
238	SEG<86>	-1985	214.5	16	95	288	SEG<186>	-3489.5	26.9	95	16
239	SEG<88>	-2013	214.5	16	95	289	SEG<188>	-3489.5	-1.1	95	16
240	SEG<90>	-2041	214.5	16	95	290	SEG<190>	-3489.5	-29.1	95	16
241	SEG<92>	-2069	214.5	16	95	291	SEG<192>	-3489.5	-57.1	95	16
242	SEG<94>	-2097	214.5	16	95	292	SEG<194>	-3489.5	-85.1	95	16
243	SEG<96>	-2125	214.5	16	95	293	SEG<196>	-3489.5	-113.1	95	16
244	SEG<98>	-2153	214.5	16	95	294	SEG<198>	-3489.5	-141.1	95	16
245	SEG<100>	-2181	214.5	16	95						
246	SEG<102>	-2209	214.5	16	95						
247	SEG<104>	-2237	214.5	16	95						
248	SEG<106>	-2265	214.5	16	95						
249	SEG<108>	-2293	214.5	16	95						
250	SEG<110>	-2321	214.5	16	95						

FUNCTION DESCRIPTION

REGISTERS

IST1305CA1-B provides two types of 8-bit registers , namely : Instruction Register(IR) and Data Register(DR). The register is selected using the RSPin. When the RS pin is set to"0", the Instruction Register Type
Is selected. When RS pin is set to"1",the Data Register Type is selected. Please refer to the table below.

RS	R/WB	Operation
0	0	Instruction register write as an internal operation.
0	1	Read busy flag(DB7) and address counter (DB0 to DB6)
1	0	Data register write as an internal operation (DR to DDRAM or CGRAM)
1	1	Data register read as an internal operation(DDRAM or CGRAM to DR)

INSTRUCTION REGISTER(IR)

The Instruction Register is used to store the instruction code(i.e. Display Clear , Cursor Home and others),Display Data RAM(DDRAM)Address, and the Character Generator RAM(CGRAM)Address. Instruction register can only be written from the MPU.

DATA REGISTER(DR)

The Data Register is used as a temporary storage for data that are going to be written into the DDRAM Or CGRAM as well as those data that are going to be read from the DDRAM or CGRAM.

BUSY FLAG (BF)

The Busy Flag is used to determine whether IST1305CA1-B is idle or internally operating.WhenIST1305CA1-B is performing some internal operations, the Busy Flag issetto"1".Under this condition, the no other instruction will not be accepted. When RS Pin is set to"0" and R/WB Pin is set to"1",the Busy Flag will
be outputted to the DB7 pin.

When IST1305CA1-B is idle or has completed its previous internal operation, the Busy Flag is set to"0".The next instruction can now be processed or executed.

ADDRESS COUNTER (AC)

The address counter is used to assign the Display Data RAM(DDRAM) Address and the Character Generator RAM(CGRAM) Address. When Address information is written into the Instruction Register (IR), this Address information is sent from the Instruction Register to the Address Counter. At the same time, the nature of the Address(either CGRAM or DDRAM)is determined by the instruction.
After writing into or reading from the DDRAM or CGRAM, the Address Counter is automatically Increased or decreased by1(for Write or Read Function).It must be noted that when the RS pin is set to"0"and R/WB is set to"1",the contents of the Address Counter are outputted to the pins--DB0 to DB6.

DISPLAY DATARAM (DDRAM)

The Display Data RAM(DDRAM) is used to store the Display Data which is represented as 8-bit character code. The Display Data RAM supports an extended capacity of 128x8-bits or 128 characters.

The Display Data RAM Address(ADD) is set in the Address Counter as a hexadecimal.

	High Order Bits			Low Order Bits			
Address Counter (hex)	AC6	AC5	AC4	AC3	AC2	AC1	AC0

An example of a DDRAM Address=39 is given below.

DDRAM Address: 39						
AC6	AC5	AC4	AC3	AC2	AC1	AC0
0	1	1	1	0	0	1

1-LINE DISPLAY(N=0)

When the number of characters displayed is less than 128, the first character is displayed at the head position. The relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position(digit)	1	2	3	4	.....	126	127	128
DDRAM address (hexadecimal)	00	01	02	03	.....	7D	7E	7F

For example, when only 8 characters are displayed in one Display Line, the relationship between the DDRAM Address and position on the OLED Panel is shown below.

Display Position	1	2	3	4	5	6	7	8
DDRAM address	00	01	02	03	04	05	06	07
Shift left	01	02	03	04	05	06	07	08
Shift right	7F	00	01	02	03	04	05	06

2-LINE DISPLAY(N=1)

The Number of Characters displayed is less than 64 x 2 lines
When the number of characters displayed is less than 64x2lines, then the first character of the first and second lines are displayed starting from the head. It is important to note that every line reserve 64 x 8bits DDRAM space.1st line is 00 to 3F, second line is 40 to 7F.Please refer the figure below.

Display Position	1	2	3	4	…….	61	62	63	64
DDRAM Address (hexadecimal)	00	01	02	03	…….	3C	3D	3E	3F
	40	41	42	43	…….	7C	7D	7E	7F

For 40-Character x 2 Lines Display
When there is a Display Shift operation ,the DDRAM Address is also shifted. Please refer to the example below.

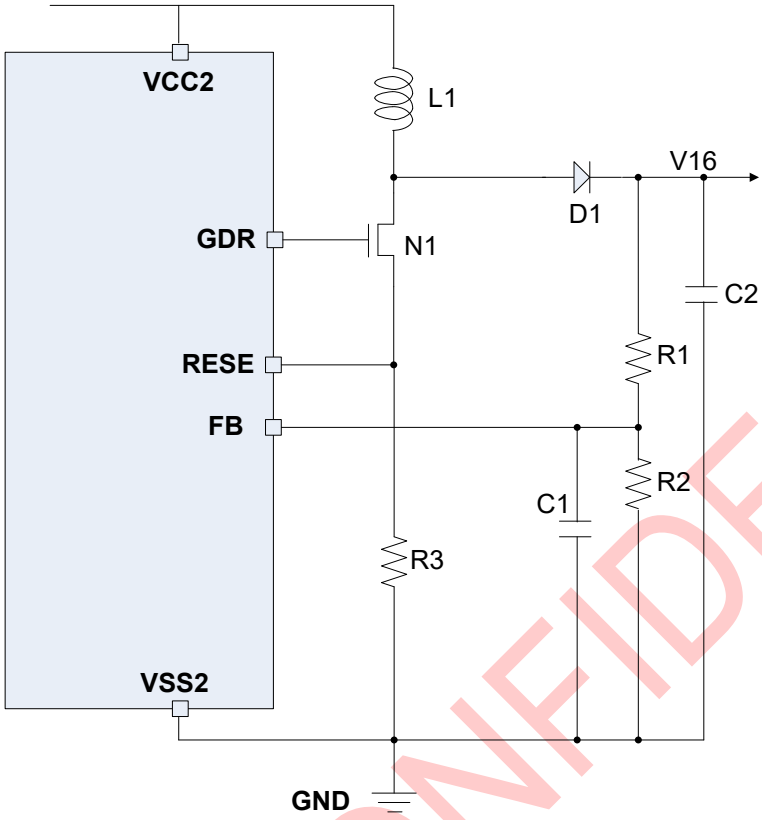
Display Position	1	2	3	4	….	18	19	20	21	22	23	….	37	38	39	40
DDRAM address (hexadecimal)	00	01	02	03	….	11	12	13	14	15	16	….	24	25	26	27
	40	41	42	43	….	51	52	53	54	55	56	….	64	65	66	67
	S0~S99								S100~S199							
Shift left	01	02	03	04	05	06	07	08	09	0A	0B	….	**25**	**26**	**27**	**28**
	41	42	43	44	45	46	47	48	49	4A	4B	….	**65**	**66**	**67**	**68**
Shift right	3F	00	01	02	03	04	05	06	07	08	09	….	**23**	**24**	**25**	**26**
	7F	40	41	42	43	44	45	46	47	48	49	….	**63**	**64**	**65**	**66**

CHARACTER GENERATOR ROM (CGROM)

The Character Generator ROM (CGROM) is used to generate either 5x8 dots or 5x10 dots character patterns from 8-bit character codes. IST1305CA1-B build in four set of font tables as “Western European I & II” , ”English Japanese”, “English Russian”. User can use software to select suitable font table **(Default “English Japanese”)**.

DC-DC VOLTAGE CONVERTER

It is a switching voltage generator circuit, designed for handheld applications. In IST1305CA1-B, internal DC- DC voltage converter accompanying with an external application circuit (shown in below) can generate a high voltage supply V16 from a low voltage supply input VCCB.V16 is the voltage supply to the OLED driver block.

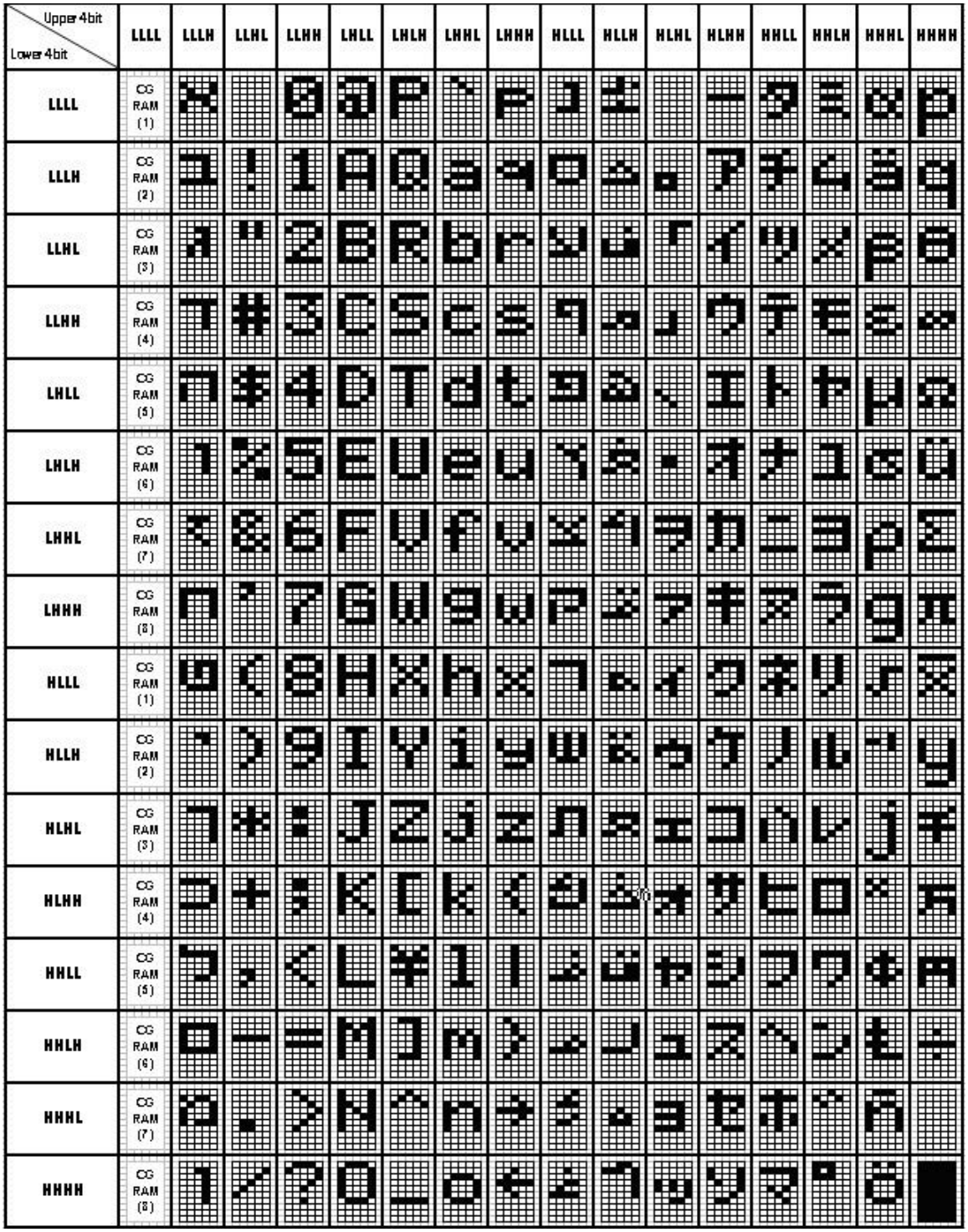


Notes:

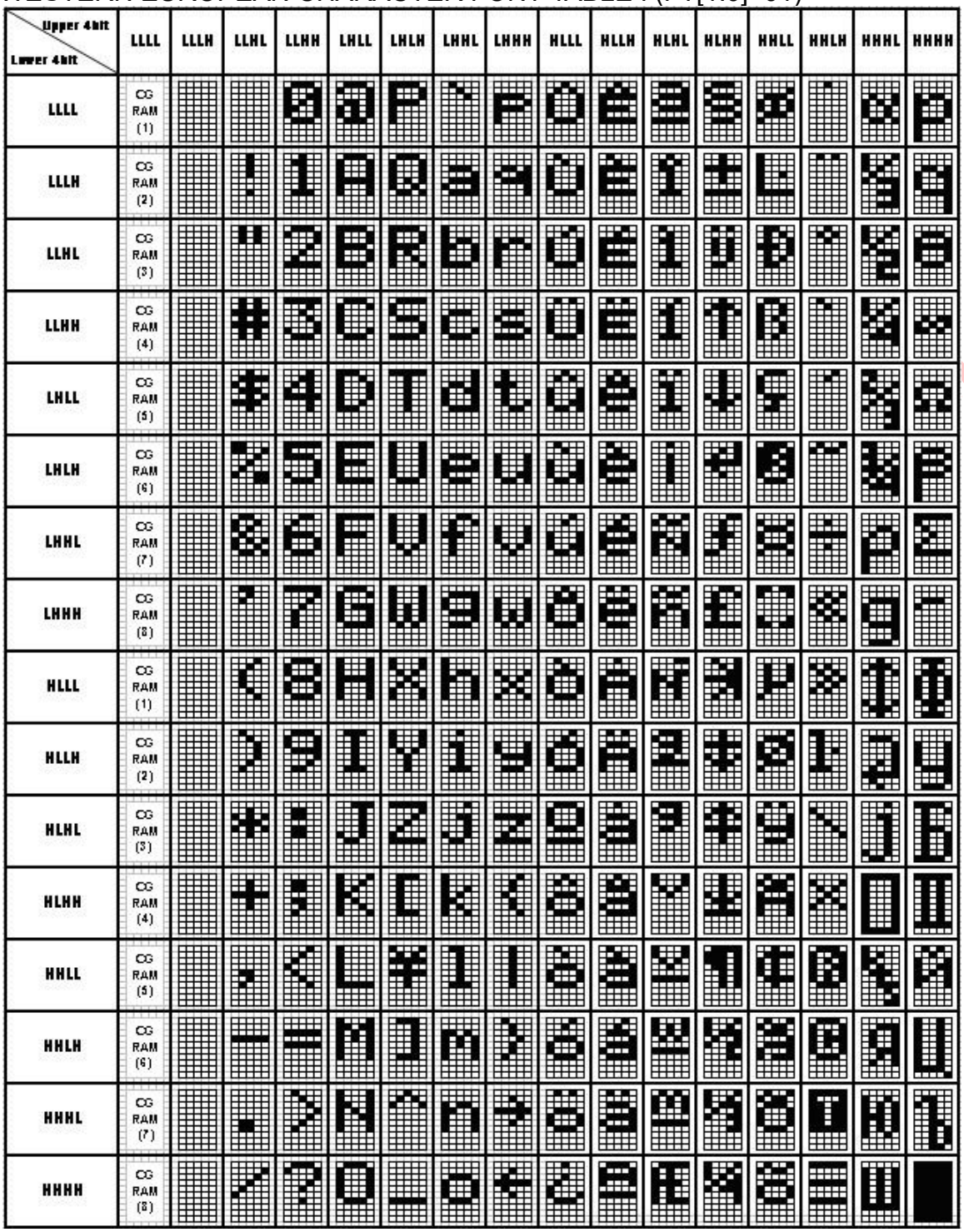
1. The DCDC external peripheral components should be adjusted depending on the loading of the exact application.
2. V16=(R1+R2)/R2x1.2
3. I_{SEG}=(VCC-2.5)/R_{BVR}

CHARACTER GENERATOR ROM (CGROM)

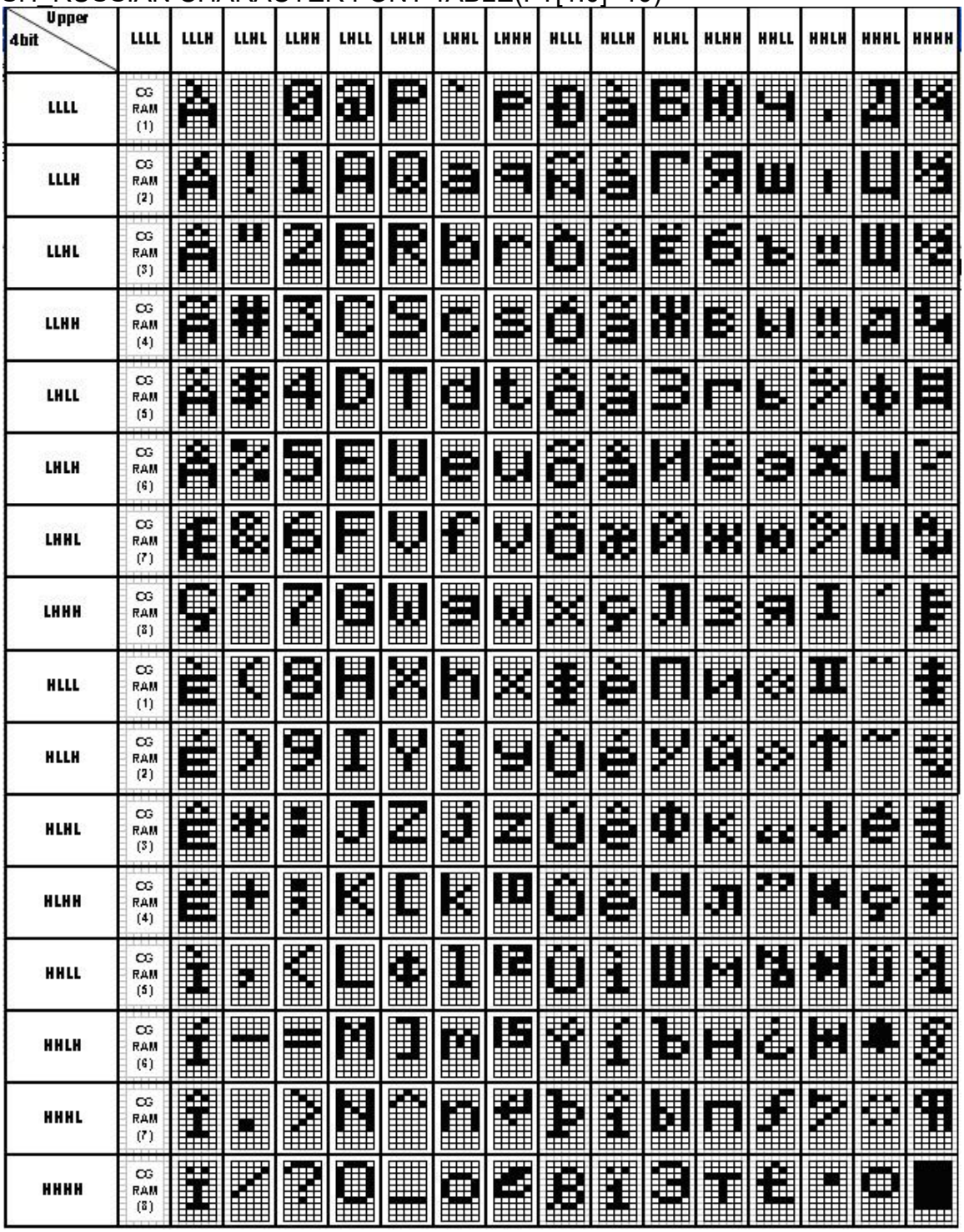
IST1305CA1-B provides four set of character font. Character font can be selected by programming FT.
ENGLISH_JAPANESE CHARACTER FONT TABLE (default FT[1:0]= 00)



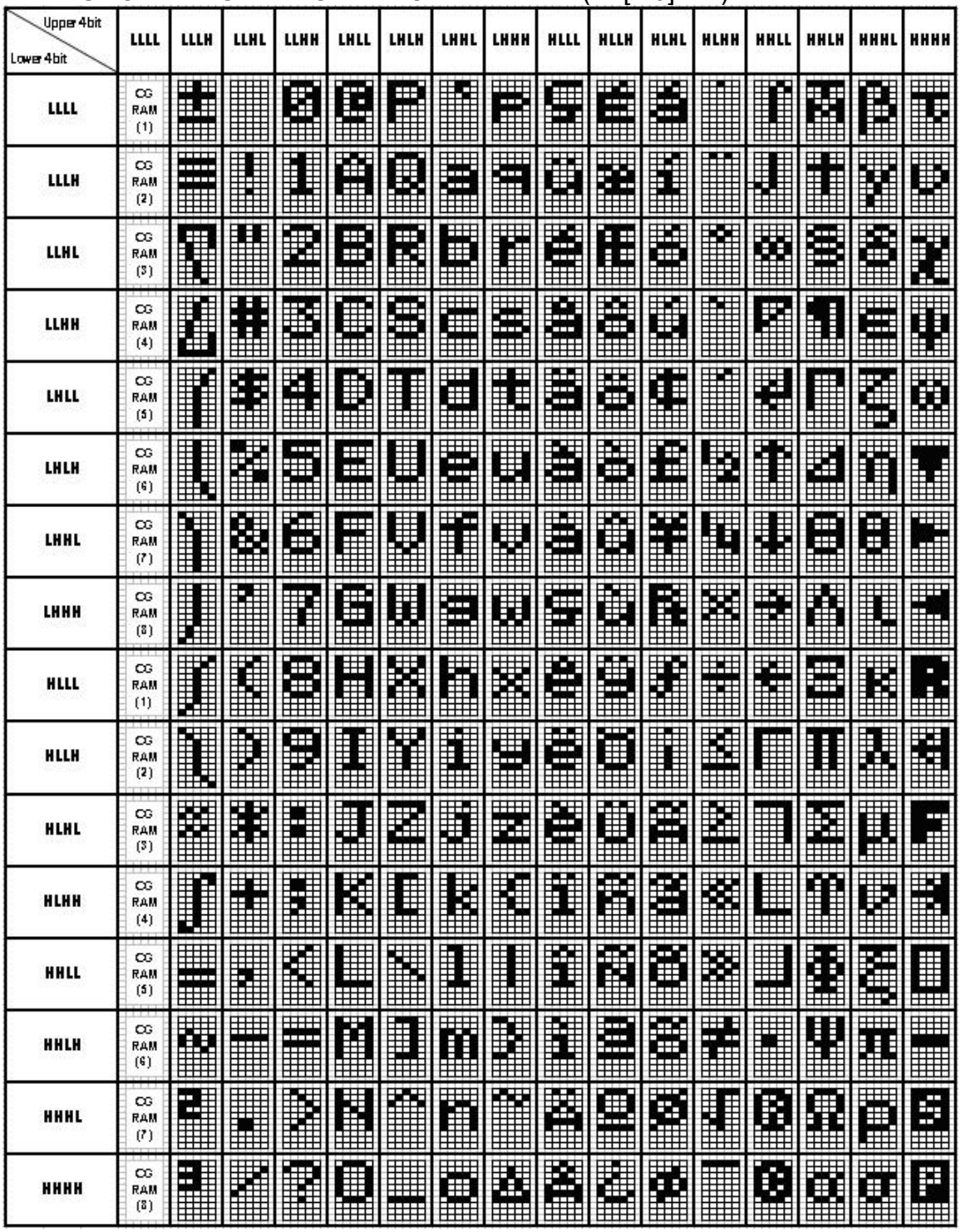
WESTERN EUROPEAN CHARACTER FONT TABLE I (FT[1:0]=01)



ENGLISH_RUSSIAN CHARACTER FONT TABLE(FT[1:0]=10)



WESTERN EUROPEAN CHARACTER FONT TABLE II (FT[1:0]=11)



CHARACTER GENERATOR RAM (CGRAM)

The Character Generator RAM(CGRAM) is used to generate either 5 x 8 dot or 5x10 dot character patterns .It can generate eight 5x8 dot character patterns or four 5x10 dot character patterns. The character patterns generated by the CGRAM can be rewritten. User-defined character patterns for the CGRAM are supported.

RELATIONSHIP BETWEEN CGRAM ADDRESS, DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS (FOR5 X 8DOT CHARACTERPATTERN)

Character Codes (DDRAM Data)									CGRAM Address							Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0		7	6	5	4	3	2	1	0	
High						Low			High				Low			High						Low		
0	0	0	0	*	0	0	0		0	0	0	0	0	0		*	*	*	1	1	1	1	0	Character pattern 1
												0	0	1		*	*	*	1	0	0	0	1	
												0	1	0		*	*	*	1	0	0	0	1	
												0	1	1		*	*	*	1	1	1	1	0	
												1	0	0		*	*	*	1	0	1	0	0	
												1	0	1		*	*	*	1	0	0	1	0	
												1	1	0		*	*	*	1	0	0	0	1	
												1	1	1		*	*	*	0	0	0	0	0	Cursor Position
0	0	0	0	*	0	0	1		0	0	1	0	0	0		*	*	*	1	0	0	0	1	Character pattern 2
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	1	1	1	1	1	
												0	1	1		*	*	*	0	0	1	0	0	
												1	0	0		*	*	*	1	1	1	1	1	
												1	0	1		*	*	*	0	0	1	0	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position
0	0	0	0	*	. . . .	. . . .	. . . .		. . . .	. . . .	. . . .	. . . .	. . . .	. . . .		*	*	*	. . . .	. . . .	. . . .	. . . .	. . . .	Character pattern 3~7
0	0	0	0	*	1	1	1		1	1	1	0	0	0		*	*	*	0	0	0	0	0	Character pattern 8
												0	0	1		*	*	*	0	1	0	1	0	
												0	1	0		*	*	*	0	0	0	0	0	
												0	1	1		*	*	*	0	0	0	0	0	
												1	0	0		*	*	*	1	0	0	0	1	
												1	0	1		*	*	*	0	1	1	1	0	
												1	1	0		*	*	*	0	0	1	0	0	
												1	1	1		*	*	*	0	0	0	0	0	Cursor position

Notes:

1.*=Not Relevant

2.The character pattern row positions correspond to the CGRAM data bits--0to4,where bit 4 is in the left position.

3.Character Code Bits 0 to 2 correspond to the CGRAM Address Bits 3 to 5(3bits:8 types)

4.If the CGRAM Data is set to "1" ,then the selection is displayed .If the CGRAM is set to "0" ,there no selection is made.

5.The CGRAM Address Bits 0 to 2 are used to define the character pattern line position .The 8th line Is the cursor position and its display is formed by the logical OR with the cursor. The 8th line CGRAM data bits 0 to 4 must be set to"0".If any of the 8th line CGRAM data bits 0 to 4 is set to"1", the corresponding display location will light up regardless of the cursor position.

6.When the Character Code Bits 4 to 7 are set to"0",then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit 3 is not relevant and will not have any effect on the character display. Because of this , the first Character Pattern shown above(R)can be displayed when the Character Code is 00H or 08H.

RELATIONSHIP BETWEEN CGRAM ADDRESS,DDRAM CHARACTER CODE AND CGRAM CHARACTER PATTERNS(FOR 5X10 DOT CHARACTER PATTERN)

Character Codes (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)								
7	6	5	4	3	2	1	0		5	4	3	2	1	0	7	6	5	4	3	2	1	0	
High						Low			High				Low		High						Low		
0	0	0	0	*	0	0	*		0	0	0	0	0	0	*	*	*	0	0	1	0	0	Character pattern 1
											0	0	0	1	*	*	*	0	1	1	1	0	
											0	0	1	0	*	*	*	1	0	1	0	1	
											0	0	1	1	*	*	*	1	0	1	0	0	
											0	1	0	0	*	*	*	0	1	1	0	0	
											0	1	0	1	*	*	*	0	0	1	1	0	
											0	1	1	0	*	*	*	0	0	1	0	1	
											0	1	1	1	*	*	*	1	0	1	0	1	
											1	0	0	0	*	*	*	0	1	1	1	0	
											1	0	0	1	*	*	*	0	0	1	0	0	
											1	0	1	0	*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1	*	*	*	*	*	*	*	*	
											1	1	0	0	*	*	*	*	*	*	*	*	
											1	1	0	1	*	*	*	*	*	*	*	*	
											1	1	1	0	*	*	*	*	*	*	*	*	
											1	1	1	1	*	*	*	*	*	*	*	*	
0	0	0	0	*	. . .	. . .	*		. . .	. . .	. . .	. . .	. . .	. . .	*	*	*	. . .	. . .	. . .	. . .	. . .	Character pattern 2~3
0	0	0	0	*	1	1	*		1	1	0	0	0	0	*	*	*	1	0	1	0	1	Character pattern 4
											0	0	0	1	*	*	*	1	1	1	1	1	
											0	0	1	0	*	*	*	1	1	1	1	1	
											0	0	1	1	*	*	*	1	1	1	1	1	
											0	1	0	0	*	*	*	0	1	1	1	0	
											0	1	0	1	*	*	*	0	0	1	0	0	
											0	1	1	0	*	*	*	0	0	1	0	0	
											0	1	1	1	*	*	*	1	0	1	0	1	
											1	0	0	0	*	*	*	0	1	1	1	0	
											1	0	0	1	*	*	*	0	0	1	0	0	
											1	0	1	0	*	*	*	*	*	*	*	*	Cursor Position
											1	0	1	1	*	*	*	*	*	*	*	*	
											1	1	0	0	*	*	*	*	*	*	*	*	
											1	1	0	1	*	*	*	*	*	*	*	*	
											1	1	1	0	*	*	*	*	*	*	*	*	
											1	1	1	1	*	*	*	*	*	*	*	*	

Notes:

1.*=Not Relevant

2.The character pattern row positions correspond to the CGRAM data bits—0 to 4,where bit 4 is in the left position.

3.Character Code Bits1and 2 correspond to the CGRAM Address Bits—4 and 5 respectively(2bits: 4types)

4.If the CGRAM Data is set to"1",then the selection is displayed. If the CGRAM is set to"0",there no selection is made.

5.The CGRAM Address Bits 0 to 3 are used to define the character pattern line position. The 11th line Is the cursor position and its display is formed by the logical OR with the cursor. The 11th line CGRAM data bits 0 to 4 must be set to "0" .If any of the11th line CGRAM data bits 0 to 4 is set to "1", the corresponding display location will light up regardless of the cursor position.

6.When the Character Code Bits 4 to 7 are set to "0" ,then the CGRAM Character Pattern is selected. It must be noted that Character Code Bit—0 and 3 are not relevant and will not have any effect on The character display. Because of this ,the Character Pattern shown above($) can be displayed when the Character Code is 00H,01H,08H or 09H.

TIMING GENERATION CIRCUIT

The timing signals for the internal circuit operations (i.e. DDRAM, CGRAM, and CGROM) are generated by the Timing Generation Circuit. The timing signals for the MPU internal operation and the RAM Read for Display are generated separately in order to prevent one from interfering with the other. This means that, for example, when the data is being written into the DDRAM, there will be no unwanted interference such as flickering in areas other than the display area.

OLED DRIVER CIRCUIT

IST1305CA1-B provides16 Common Drivers and 200 Segment Driver Outputs. When a character font and the number of lines to be displayed have been selected, the corresponding Common Drivers output the
waveform automatically. A non-selection waveform will be outputted by the rest of the Common outputs.

CURSOR/BLINK CONTROLCIRCUIT

The cursor or character blinking is generated by the Cursor/Blink Control Circuit. The cursor or the blinking will appear with the digit located at the Display Data RAM(DDRAM) Address Set in the Address Counter (AC).

	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Address counter	0	0	0	0	1	1	1

CASE1:FOR1-LINEDISPLAY

Example: When the Address Counter (AC) is set to 0EH,the cursor position is displayed at DDRAM Address 0EH.

Display position	1	2	3	4	5	.....	14	15	.....	19	20
DDRAM address (hexadecimal)	00	01	02	03	04	.....	0D	**0E**	.....	12	13

|
CursorPosition

Note: The cursor or blinking appears when the Address Counter(AC)selects the Character Generator RAM(CGRAM).When the AC selects CGRAM Address, then the cursor or the blinking is displayed in an irrelevant and meaningless position.

CASE2:FOR2-LINEDISPLAY

Example: When the Address Counter(AC) is set to 46H, the cursor position is displayed at DDRAM Address 46H.

Display position	1	2	3	4	5	6	7	8	.....	19	20
DDRAM address	00	01	02	03	04	05	06	07	.....	09	13
(hexadecimal)	40	41	42	43	44	45	46	47	.....	49	53

|

Cursor Position

Note:

The cursor or blinking appears when the Address Counter(AC) selects the Character Generator RAM (CGRAM).When the AC selects CGRAM Address , then the cursor or the blinking is displayed in an irrelevant and meaningless position.

INTERNAL RESET CIRCUIT INITIALIZATION

When power is turned ON,IST1305CA1-B is initialized automatically by an internal reset circuit. The following items are set (default) during the initialization.

1.Displayclear

2.Functionset:
DL="1":8-bit interface data
N="0": 1-line display
F="0":5x8 dot character font

3. Power turn off
PWR="0"

4.Display on/off control:
D="0":Display off
C="0":Cursor off
B="0":Blinking off

5.Entry mode set
I/D="0":Decrement by1
S="0":No shift

6. Cursor/Display shift / Pwr
S/C="0", R/L="1": Shifts cursor position to the right
Pwr="1": Internal DCDC power on

The Busy Flag(BF) is in a busy state until the initialization is completed(BF="1").The busy state will be In effect 10 ms after VDD stabilization.

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CHARACTER MODE ADDRESSING

IST1305CA1-B provides two kind of character mode. User can fill in 128 characters data (N=0, one line) or 64 characters data per line (N=1, two line) in embedded RAM to display graphic. Character mode address can be controlled by DDRAM address instruction.

Address Format	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
CA (Character Address)	1	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

(1)1-Line condition (N=0)

1	2	3	4	……	……	125	126	127	128
CA=10000000	CA=10000001	CA=10000010	CA=10000011	……	……	CA=11111100	CA=11111101	CA=11111110	CA=11111111

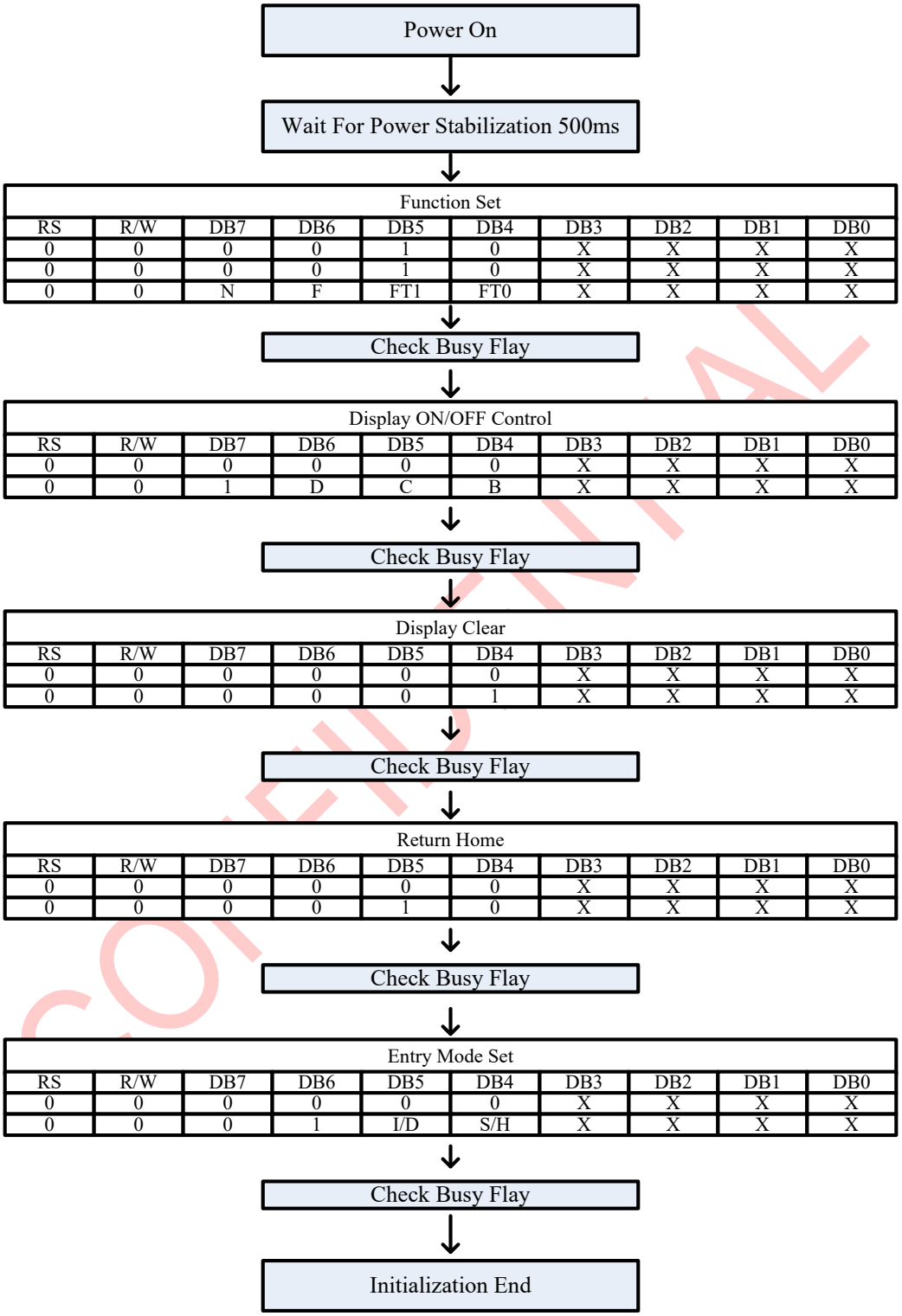
(2)2-Line condition (N=1)

1	2	3	4	……	……	61	62	63	64
CA=10000000	CA=10000001	CA=10000010	CA=10000011	……	……	CA=10111100	CA=10111101	CA=10111110	CA=10111111
CA=11000000	CA=11000001	CA=11000010	CA=11000011	……	……	CA=11111100	CA=11111101	CA=11111110	CA=11111111

INITIALIZATION BY INSTRUCTION

(1)8-bit mode

(2)4-bit mode



INSTRUCTIONS

IST1305CA1-B's Instruction Register(IR) and Data Register(DR) are the only registers that can be controlled by the MPU. Prior to the commencement of it internal operation,IST1305CA1-B temporarily stores the control information to its Instruction Register(IR) and Data Register (DR) in order to easily facilitate interface with various types of MPU. The internal operations of the IST1305CA1-B are determined by the signals(RS, R_WB,DB0 to DB7)that are sent from the MPU. These signals are categorized into 4 instructions types,
namely:

1. Function Setting Instructions(i.e. Display , Format, Data Length etc.)
2. Internal RAM Address Setting Instructions
3. Data Transfer with Internal RAM Instructions
4. Miscellaneous Function Instructions

The generally used instructions are those that execute data transfers with the internal RAM. However, when the internal RAM addresses are auto incremented/decremented by 1 after each Data Write ,the program load of the MPU is lightened. The Display Shift Instruction can be executed at the same time as the Display Data Write, thereby minimizing system development time with maximum programming efficiency.

When an instruction is being executed for an internal operation , only the Busy Flag/Address Read Instruction can be performed .The other instructions are not valid. It should be noted that during the execution of an instruction , the Busy Flag is set to"1".The Busy Flag is set to"0" when the instructions are can be accepted and executed. Therefore, the Busy Flag should be checked to make certain that BF="0"before sending another instruction from the MPU. If not , the time between the first instruction and the next instruction is longer than the time it takes to execute the instruction itself.

Instruction	Code										Description
	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display. It takes max. 6.2ms for execution this command @fosc=250KHZ
Return Home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM Address 0 into the Address Counter. Returns shifted display to original position .DDRAM contents remain unchanged.(DB0 is test bit. User should set DB0=0 all the time)
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets curs or move direction and specifies display shift (These operations are performed during data write and read.)
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets entire Display (D)ON/OFF. Sets Cursor(C) ON/OFF. Sets Blinking(B) of Cursor. Position Character.
Cursor/ Display Shift/ Mode/ Pwr/internal display control enable	0	0	0	0	0	1	S/C	R/L	0	0	S/C & R/L = Moves cursor & shifts display without changing DDRAM contents. PWR = Sets internal power on/off INT = internal or external display control select
							INT	PWR	1	1	
Function Set	0	0	0	0	1	DL	N	F	FT1	FT0	Sets inter face data length(DL). Sets number of display lines(N). Sets Character Font(F).Sets Font Table (FT) *Forbids to set FT=01 or 11 when RT1305 be operated in 4-bit interface.
Set CGRAM Address	0	0	0	1	ACG	ACG	ACG	ACG	ACG	ACG	Sets CGRAM Address. CGRAM Data is sent and received after this setting.
Set DDRAM Address	0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD	Sets DDRAM Address. The DDRAM data Is sent and received after this setting.
Read Busy Flag & Address	0	1	BF	AC	AC	AC	AC	AC	AC	AC	Reads Busy Flag(BF)indicating that internal operation is being performed. Reads Address Counter contents.
Write data into the CGRAM or DDRAM	1	0	WriteData								Writes data into the CGRAM or DDRAM
Read Data from the CGRAM or DDRAM	1	1	ReadData								Read data from the CGRAM or DDRAM

Instruction	Code										Description
	RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Enter TEST command	0	0	0	0	0	0	0	0	1	1	Enter TEST command，all test command working in this mode.
Display control	0	0	0	0	0	1	0	1	0	1	This is Special Command Please Refer Page 42. SHLi=Internal display shift mode select
	0	0	0	0	0/1	0	0	SHLi	0/1	0/1	
DVR,BVR internal or external select	0	0	0	1	1	1	0	0	PHSLC	IFENON	PHSLC=0:external DVR PHSLC=1:internal digital DVR IFENON=0:external BVR IFENON=1:internal BVR
Internal digital DVR control register	0	0	1	1	1	1	1	0	1	1	This command set DVR precharge timing. PNUM setting range 0x01~0xB3.
	0	0	PNUM	PNUM	PNUM	PNUM	PNUM	PNUM	PNUM	PNUM	
Internal BVR control register	0	0	1	1	1	1	1	0	1	0	This command set internal BVR current CT setting range 0x01~0xFF.
	0	0	CT	CT	CT	CT	CT	CT	CT	CT	
SPI4/IIC read data enable	0	0	0	1	1	1	1	1	0	0	Spi4/IIC interface read data enable
SPI4/IIC read command enable	0	0	0	1	1	1	1	1	0	1	Spi4/IIC interface read command enable
Exit test mode	0	0	0	0	0	0	0	0	0	0	This command exit test mode

Notes:

1.After the CGRAM/DDRAM Read or Write Instruction has been executed, the RAM Address Counter is incremented or decremented by 1. After the Busy Flag is turned OFF, the RAM Address Is updated.

2.I/D=Increment / Decrement Bit

-I/D="1":Increment

-I/D="0":Decrement

3.S=Shift Entire Display Control Bit. When S=”0”, shift function disable.

4. BF=Busy Flag

-BF="1":Internal Operating in Progress

-BF="0":No Internal Operation is being executed, next instruction can be accepted.

5.R/L=Shift Right/Left

-R/L="1":Shift to the Right

-R/L="0":Shift to the Left

6.S/C=Display Shift / Cursor Move

-S/C="1":Display Shift

-S/C="0":Cursor Move

7. PWR=Internal DCDC on/of control. PWR=”1”, DCDC on. PWR=”0”, DCDC off.

8.DDRAM=Display Data RAM

9.CGRAM=Character Generator RAM

10.ACG=CGRAM Address

11.ADD=Address Counter Address(corresponds to cursor address)

12.AC=Address Counter (used for DDRAM and CGRAM Addresses)

13.F=Character Pattern Mode

-F="1":5x10 dots

-F="0":5x8 dots

14.N=Number of Lines Displayed

- N="1": 2 -Line Display

- N="0": 1 -Line Display

INSTRUCTION DESCRIPTION

CLEAR DISPLAY INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction is used to clear the Display Write Space 20H in all DDRAM Addresses. That is, the character pattern for the Character Code 20H must be a BLANK pattern.

RETURN HOME INSTRUCTION

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	*

Note:*=Not Relevant

This instruction is used to set the DDRAM Address 0 into the Address Counter and revert the display to its original status(if the display has been shifted).The DDRAM contents do not change.
The cursor or blinking will go to the left edge of the display .If there are 2 lines displayed, the cursor or blinking will go to the first line's left edge of the display.

ENTRYMODE SET INSTRUCTION

The Entry Mode Set Instruction has two controlling bits :I / D and S. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

I/D IS THEINCREMENT/DECREMENT BIT.

When I/D is set to"1",the DDRAM Address is incremented by "1"when a character code is written into or read from the DDRAM .An increment of 1 will move the cursor or blinking one step to the right.

When I/D is set to"0",the DDRAM is decremented by1when a character code is written into or read from the DDRAM.A decrement of 1will move the cursor or blinking one step to the left.

S:SHIFT ENTIRE DISPLAY CONTROL BIT

This bit is used to shift the entire display .When S is set to"1",the entire display is shifted to the right (when I/D="0")or left(when I/D="1").When S is set to"0",the display is not shifted.

Ex1 : I/D=1, S=1

		1	2	3	4	_	Initial display
	1	2	3	4	A	_	Input new character "A"
1	2	3	4	A	B	_	Input new character "B"
2	3	4	A	B	C	_	Input new character "C"
3	4	A	B	C	D	_	Input new character "D"

Ex2 : I/D=0, S=1

1	2	3	4	_			Initial display
	1	2	3	4	A		Input new character "A"
		1	2	3	B	A	Input new character "B"
			1	2	C	B	Input new character "C"
				1	D	C	Input new character "D"

DISPLAY ON/OFF CONTROL INSTRUCTION

The Display On/OFF Instruction is used to turn the display ON or OFF. The controlling bits are D,C and B.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

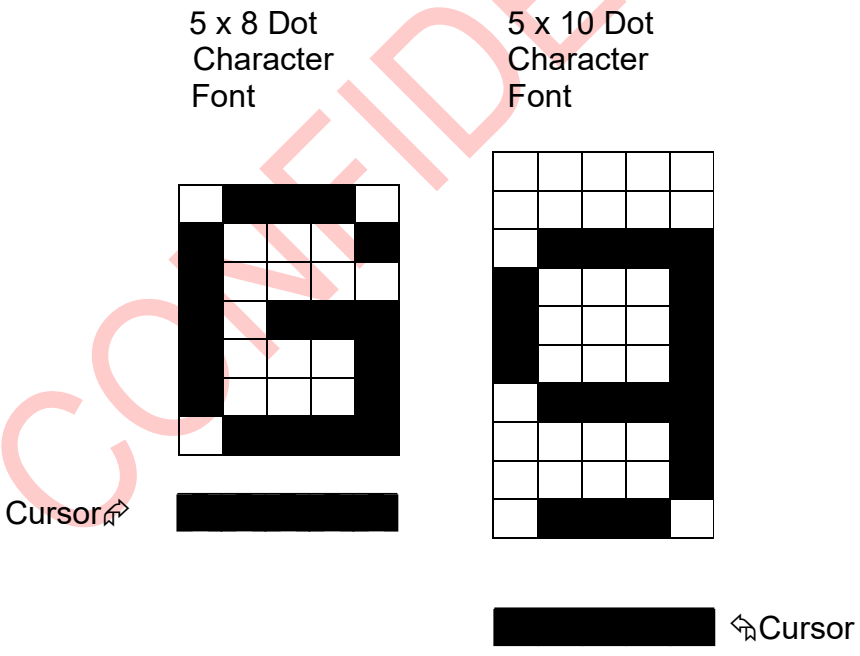
D:DISPLAY ON/OFF BIT

When D is set to"1",the display is turned ON. When D is set to"0",the display is turned OFF and the display data is stored in the DDRAM. The display data can be instantly displayed by setting D to"1".

C:CURSOR DISPLAYCONTROL BIT

When C is set to"1",the cursor is displayed. In a5x8 dot character font , the cursor is displayed via the 5 dots in the 8th line. In a 5 x 10 dot character font, it is displayed via 5 dots in the 11th line.

When C is set to"0",the cursor display is disabled.
During a Display Data Write, the function of the I/D and others will not be altered even if the cursor is not present. Please refer to the figure below.



B:BLINKING CONTROL BIT

When B is set to'1",the character specified by the cursor blinks. The blinking feature is displayed by switching between the blank dots and the displayed character at a speed of 409.6ms intervals when the fcp or fosc is 250kHz.Please refer to the figure below.

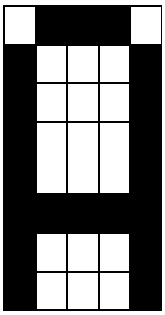
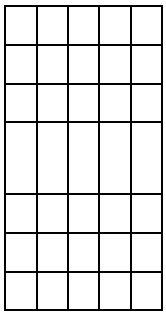


Figure 1



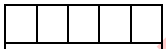


Figure 2

Note: Figures 1 and 2 are alternately displayed
The cursor and the blinking can be set to display at the same time. The blinking frequency depends on the fosc or the reciprocal of fcp.
To illustrate, when fosc=250K Hz, then ,the blinking frequency=409.6 x 250/270=379.2ms

CURSOR/DISPLAY SHIFT INSTRUCTION

This instruction is used to shift the cursor or display position to the left or right without writing or reading the Display Data. This function is used to correct or search the display. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	0	0
0	0	0	0	0	1	INT	PWR	1	1

S/C	R/L	Shift Function
0	0	Shifts the cursor position to the left.(AC is decremented by1).
0	1	Shifts cursor position to the right.(AC incremented by1).
1	0	Shifts entire display to the left .The cursor follows the display shift.
1	1	Shifts the entire display to the right .The cursor follows the display shift.

In a 2-line Display, the cursor moves to the second line when it passes the 40th digit of the first line. The first and second line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The second line display does not shift into the first line position.

The Address Counter (AC) contents will not change if the only action performed is a Display Shift.

PWR: ENABLE/DISABLE INTERNAL POWER

This bit is used to turn ON or turn OFF the internal power.
When PWR = 1, the internal power is turned ON.
When PWR = 0, the internal power is turned OFF.

INT: ENABLE/DISABLE INTERNAL SHLi

This bit is used to turn ON or turn OFF the internal display control function.
When INT = 1, display follow the internal SHLi set.
When INT = 0, display follow external SHL set.

FUNCTION SET INSTRUCTION

The Function Set Instruction has three controlling 3 bits, namely :DL, N and F. Please refer to the table below.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	FT1	FT0

DL: INTERFACE DATA LENGTH CONTROL BIT

This is used to set the interface data length. When DL is set to"1",the data is sent or received in 8-bit length via the DB0 to DB7(for an 8-Bit Data Transfer). When DL is set to"0",the data is sent or received in 4-bit length via DB4 to DB7 (for a 4-Bit Data Transfer).When the 4-bit data length is selected, the data must be sent or received twice.
The default data length is 8-bit, if chip want to operation in 4-Bit interface, the first instruction after power on, set to DL is “0” use function set command and data length is changed from 8-Bit to 4-Bit, secondly, it requires two times (4-Bit twice) to accomplish complete function set command to set DL(4-bit data length), N(display line), F(character font) and FT(font table). 4-Bit operation setting flow please refer to page 28.

N: NUMBER OF DISPLAY LINE

This is used to set the number of display lines. When N="1", the 2-line display is selected. When N is set to"0",the1-line display is selected.

F:CHARACTER FONT SET

This is used to set the character font set. When F is set to "0", the 5 x 8 dot character font is selected. When F is set to"1",the 5x10 dot character font is selected.

It must be noted that the character font setting must be performed at the head of the program before executing any instructions other than the Busy Flag and Address Instruction. Otherwise, the Function Set Instruction cannot be executed unless the interface data length is changed.

FT1, FT0:FONT TABLE SELECTION

These two bits are used to select one font table out of the three for further process.
When (FT1, FT0) = (0, 0), the *ENGLISH_JAPANESE CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (0, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE-I* will be selected.
(FT1, FT0) = (1, 0), the *ENGLISH_RUSSIAN CHARACTER FONT TABLE* will be selected.
(FT1, FT0) = (1, 1), the *WESTERN EUROPEAN CHARACTER FONT TABLE-II* will be selected.
Note: The default setting for FT1 and FT0 is 0 and 0 respectively which means the default Font Table is *ENGLISH_JAPANESE CHARACTER FONT TABLE.*

It must be noted that Function Set instruction be executed on display off status.

SET CGRAM ADDRESS INSTRUCTION

This instruction is used to set the CGRAM Address binary AAAAAA into the Address Counter. Data is then written to or read from the MPU for CGRAM.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	ACG	ACG	ACG	ACG	ACG	ACG

Note: ACG is the CGRAM Address

SET DDRAM ADDRESS INSTRUCTION

This instruction is used to set the DDRAM Address binary AAAAAAA into the Address Counter. The data is written to or read from the MPU for the DDRAM.If1-line display is selected(N="0"),then AAAAAAA can be 00H to 4FH.When the2-line display is selected, then AAAAAAA can be 00H to 27H for the first line and 40H to 67H for the second line.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	ADD	ADD	ADD	ADD	ADD	ADD	ADD

Note: ADD = DDRAM Address

READ BUSY FLAG AND ADDRESS INSTRUCTION

This instruction is used to read the Busy Flag (BF) to indicate if IST1305CA1-B is internally operating on a previously received instruction. If BF is set to"1",then the internal operation is in progress and the next instruction will not be accepted. If the BF is set to"0",then the previously received instruction has been executed and the next instruction can be accepted and processed. It is important to check the BF status before proceeding to the next write operation. The value of the Address Counter in binary AAAAAAA is simultaneously read out. This Address Counter is used by both the CGRAM and the DDRAM and its value is determined by the previous instruction. The contents of the address are the same as for the instructions—Set CGRAM Address and Set DDRAM Address.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC	AC	AC	AC	AC	AC	AC

Notes:
1. BF=Busy Flag
2.AC=Address Counter

WRITE DATA TO CGRAM / DDRAM INSTRUCTION

This instruction writes 8-bit binary data-- DDDDDDDD to the CGRAM or the DDRAM. The previous CGRAM or DDRAM Address setting determines whether a data is to be written into the CGRAM or the DDRAM .After the write process is completed, the address is automatically incremented or decremented by 1 in accordance with the Entry Mode instruction .It must be noted that the Entry Mode instruction also determines the Display Shift.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D	D	D	D	D	D	D	D

READ DATA FROM THE CGRAM OR DDRAM INSTRUCTION

This instruction reads the 8-bit binary data –DDDDDDDD from the CGRAM or the DDRAM. The Set CGRAM Address or Set DDRAM Address Set Instruction must be executed before this instruction can be performed, otherwise, the first Read Data will not be valid.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D	D	D	D	D	D	D	D

When the Read Instruction is executed in series, the next address data is normally read from the Second Read. There is no need for the Address Set Instruction to be performed before this Read instruction when using the Cursor Shift Instruction to shift the cursor(Reading the DDRAM).The Cursor Shift Instruction has the same operation as that of the Set the DDRAM Address Instruction.

After a Read instruction has been executed ,the Entry Mode is automatically incremented or decrementedby1.It must be noted that regardless of the Entry Mode, the Display Shift is not executed.

After the Write instruction to either the CGRAM or DDRAM has been performed, the Address Counter Is automatically increased or decreased by 1. The RAM data selected by the Address Counter cannot be read out at this time even if the Read Instructions are executed. Therefore, in order to correctly read the data, the following procedure has suggested:

1. Execute the Address Set or Cursor Shift(only with DDRAM)Instruction
2. Just before reading the desired data, execute the Read Instruction from the second time the Read Instruction has been sent.

TEST COMMAND INSTRUCTION

This instruction enter test mode.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	1

This instruction exits test mode.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0

This instruction selects internal display control set.

SHL= 0 / 1,display writing direction select.
When INT = 1, display follows the internal “display control command” setting.
When INT = 0, display follows the external SHL/CMS/SGS pins setting.

Normal Mode

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	1	0	1
0	0	0	0	0	0	0	SHLi	0	0

Normal mode, have two combinations.
(INT=1, DB5=0, SHLi=0, DB1=0, DB0=0 or INT=1, DB5=0, SHLi=1, DB1=0, DB0=0)
Please Refer to 「Normal Mode Application Description」.

180 Degrees Mode

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	1	0	1
0	0	0	0	1	0	0	SHLi	1	1

180 degrees mode, have two combinations.
(INT=1, DB5=1, SHLi=0, DB1=1, DB0=1 or INT=1, DB5=1, SHLi=1, DB1=1, DB0=1)
Please Refer to 「180 Degrees Mode Application Description」.

Normal Mode Application Description

INT	Ex-SHL	DB5	SHLi	DB1	DB0	Display Control Command	DDRAM Start Address	Original Position
0	H	X	X	X	X	X	Line-1=0x80h Line-2=0xC0h	Refer Figure-3
0	L	X	X	X	X	X	Line-1=0x94h Line-2=0xD4h	
1	Don't care	0	1	0	0	0x15h,0x04h	Line-1=0x80h Line-2=0xC0h	Refer Figure-4
1		0	0	0	0	0x15h,0x00h	Line-1=0x94h Line-2=0xD4h	

NOTE:
X = Don't use

When the panel layout is designed based on SGS=L, and CMS=L, which means the IC is bund on the left side of the panel (illustrated below) have four combinations.

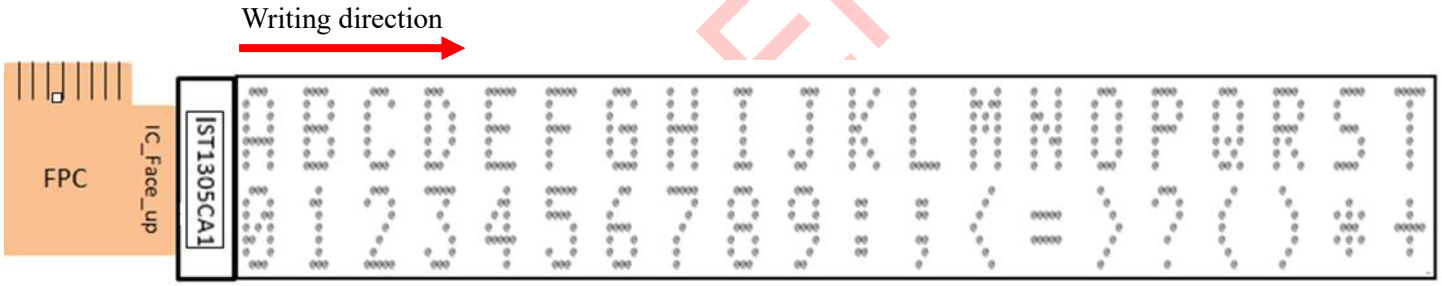


Figure-3

(1)External setting SHL=H, SGS=L ,CMS=L and INT=0
(2)Internal display control command setting INT=1, DB5 =0,SHLi=1, DB1=0 ,DB0=0)

NOTE:
*1)Display write DDRAM Line-1 start address set=0x80.
Display write DDRAM Line-2 start address set=0xC0.

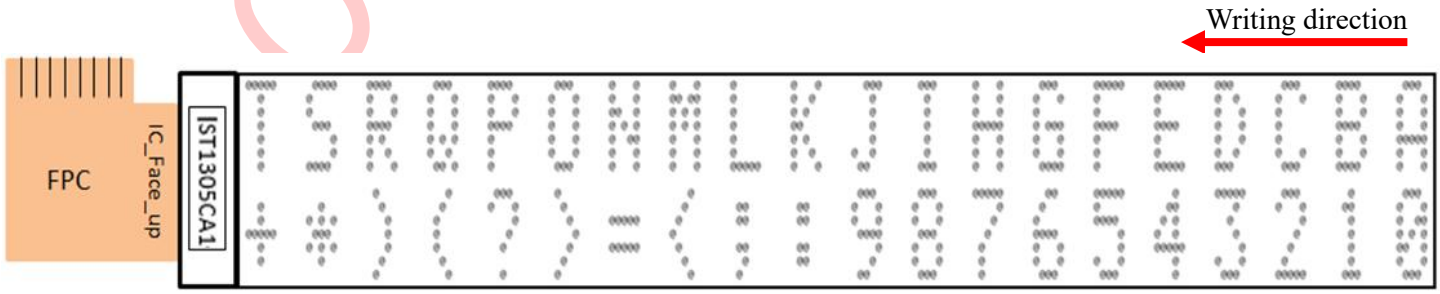


Figure-4

(3)External setting SHL=L, SGS=L ,CMS=L and INT=0
(4)Internal display control command setting INT=1, DB5 =0, SHLi=0, DB1=0 ,DB0=0)

NOTE:
*1)Display write DDRAM Line-1 start address set=0x94.
Display write DDRAM Line-2 start address set=0xD4.

180 Degrees Mode Application Description

INT	DB5	SHLi	DB1	DB0	Display Control Command	DDRAM Start Address	180' Rotate
1	1	1	1	1	0x15h,0x27h	Line-1=0x94h Line-2=0xD4h	Refer Figure-5
1	1	0	1	1	0x15h,0x23h	Line-1=0x80h Line-2=0xC0h	Refer Figure-6

And then, If the same panel has to be physically rotated 180 degrees and still keep the font character to be displayed correctly, it can be fulfilled by setting two combinations(illustrated below).

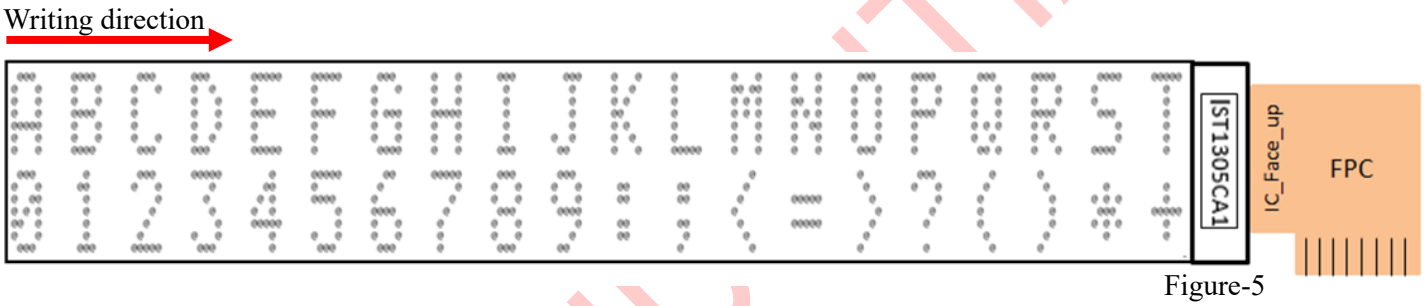


Figure-5

(1)INT=1, DB5 =1,SHLi=1, DB1=1, DB0=1.

NOTE:
*1)Display write DDRAM Line-1 start address set=0x94.
Display write DDRAM Line-2 start address set=0xD4.

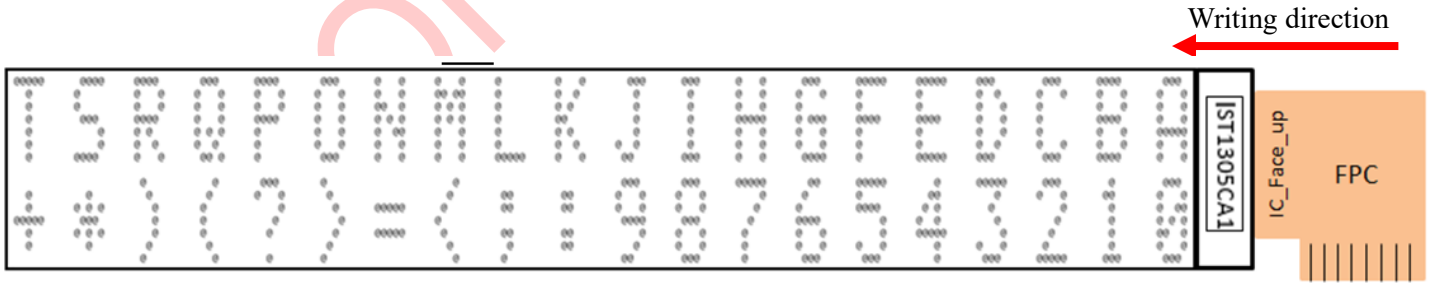


Figure-6

(2)INT=1, DB5 =1,SHLi=0, DB1=1, DB0=1

NOTE:
*1)Display write DDRAM Line-1 start address set=0x80.
Display write DDRAM Line-2 start address set=0xC0.

This instruction select internal or external DVR,BVR.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	0	PHSLC	IFENON

PHSLC=0 : External DVR. The precharge time is determined by external DVR resistor.
PHSLC=1 : Internal DVR. The precharge time is determined by internal PNUM setting.
IFENON=0 : External BVR. The I_{SEG} is determined by external BVR resistor.
IFENON=1 : Internal BVR. The I_{SEG} is determined by internal CT setting.

This instruction decided internal BVR current.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	0	1	0
0	0	CT	CT	CT	CT	CT	CT	CT	CT

CT setting range 0x01~0xFF.
Each CT step increases I_{SEG} driving current about 1.25uA.

CT	I_{SEG}（uA）
N/A	N/A
1	1.25
2	2.5
3	3.75
4	5.0
|	|
255	~300

This instruction decided internal DVR precharge timing.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	1	0	1	1
0	0	PNUM	PNUM	PNUM	PNUM	PNUM	PNUM	PNUM	PNUM

PNUM setting range 0x01~0xB3.

PNUM (decimal)	Precharge time(1/16Duty)	REMARK
N/A	N/A	● For 1/8 duty, $T_{DCK}=T_{OSC}$ x 4 ● For 1/11 duty, $T_{DCK}=T_{OSC}$ x 4 ● For 1/16 duty, $T_{DCK}=T_{OSC}$ x 2 (T_{OSC} = Oscillator clock cycle time)
1	2.5* T_{DCK}	
2	3.5* T_{DCK}	
3	4.5* T_{DCK}	
4	5.5* T_{DCK}	
5	6.5* T_{DCK}	

6	7.5* T_{DCK}	
:	:	
:	:	
174	175.5* T_{DCK}	
175	176.5* T_{DCK}	
176	177.5* T_{DCK}	
177	178.5* T_{DCK}	
178	179.5* T_{DCK}	
179	180.5* T_{DCK}	
>179	Don't use	

This instruction enable spi4/IIC interface read data.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	1	0	0

This instruction enable spi4/IIC interface read command.

RS	R/WB	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	1	1	0	1

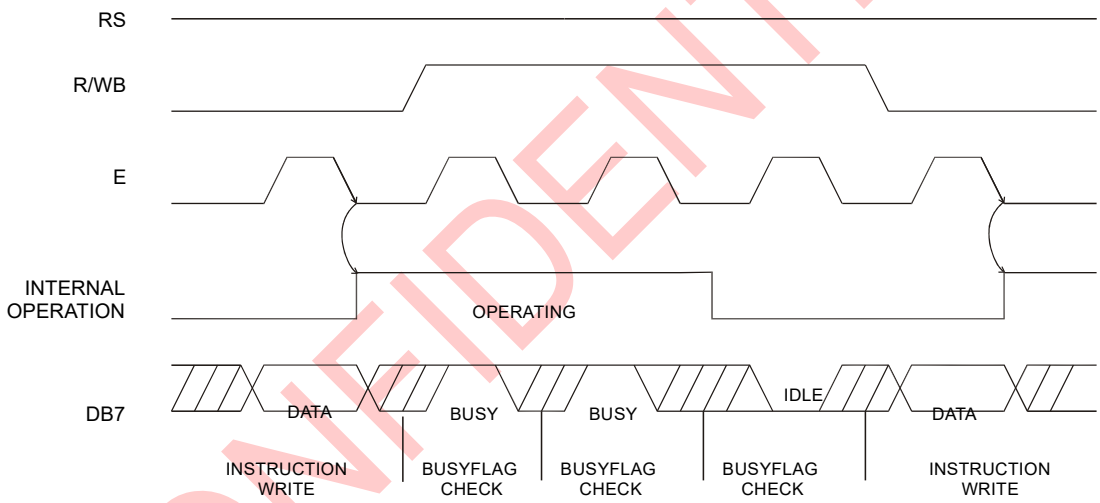
MPU INTERFACE

IST1305CA1-B provides High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-serier and serial interface. User can choice by signal “PS” and “C68”.

68-series interface

(a) 8-BIT mode (Not available for serial mode)

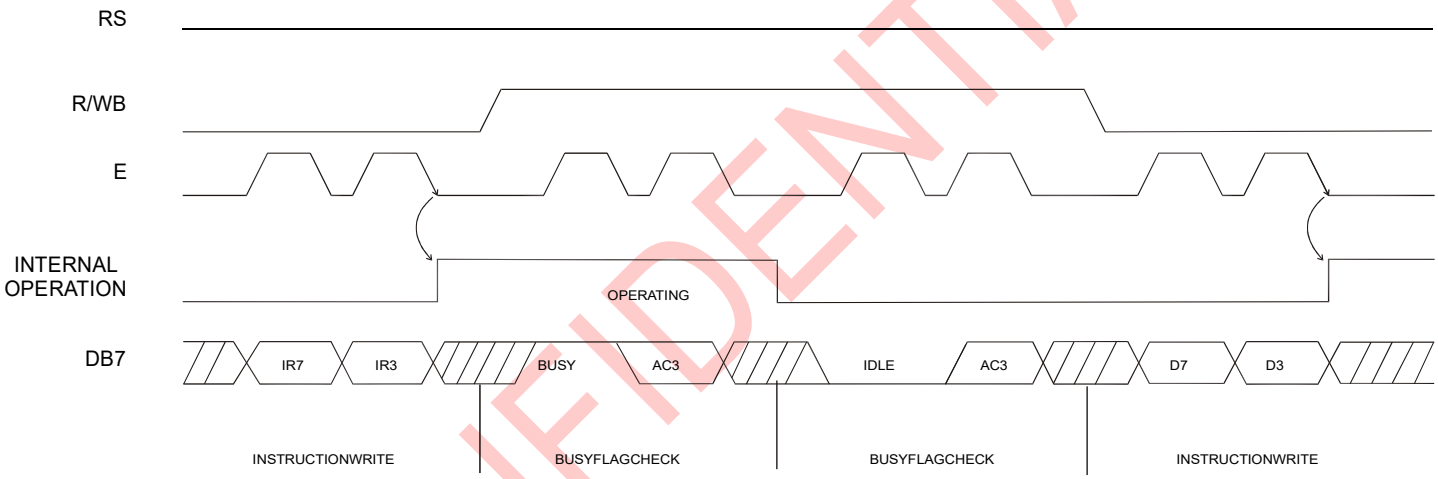
When IST1305CA1-B interfaces with an 8-bit MPU,DB0 to DB7 are used. The 8-bit data transfer starts from the four high order bits--DB4 to DB7 followed by the four low order bits--DB0 to DB3. An example of a Busy Flag Check Timing in an 8-Bit MPU Interface is given in the diagram below.



(b) 4-BITmode (Not available for serial mode)

IST1305CA1-B can be configured to interface with a 4-bit MPU and is selected via a program. If the I/O port of the 4-Bit MPU from which IST1305CA1-B is connected to, is capable of transferring 8bits, then an 8-bit data transfer operation is executed. Otherwise , two 4-bit data transfer operations are needed to satisfy one complete data transfer.

Under the 4-bit data transfer ,DB4 to DB7 are used as bus lines. DB0 to DB3 are disabled. The data transfer between IST1305CA1-B and MPU is completed after two 4-bit data have been transferred .The Busy Flag must be checked (one instruction)after completion of the data transfer (that is,4-bit data has been transferred twice.).The Busy Flag must be checked after two 4-bits data transfer has been completed. Please refer to the diagram below for a 4-bit data transfer timing sequence.

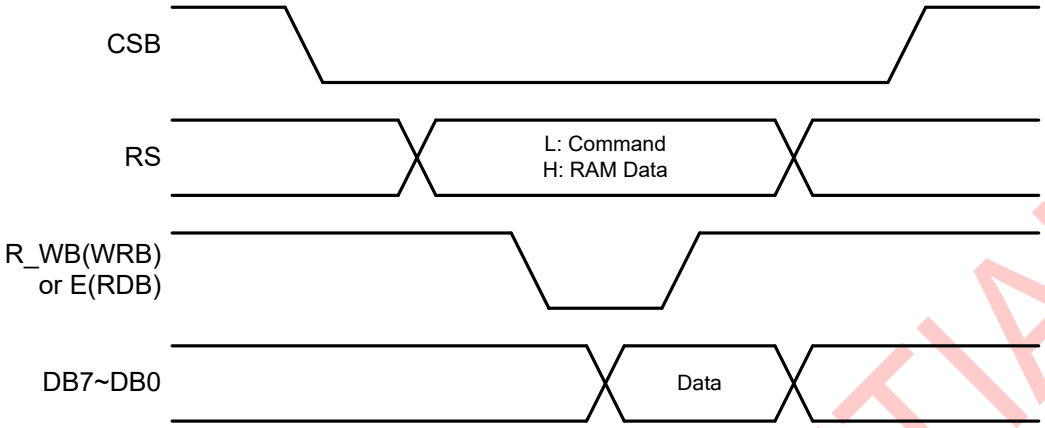


where:
1.IR7=Instruction Bit 7
2.IR3=Instruction Bit 3
3.AC3=Address Counter 3

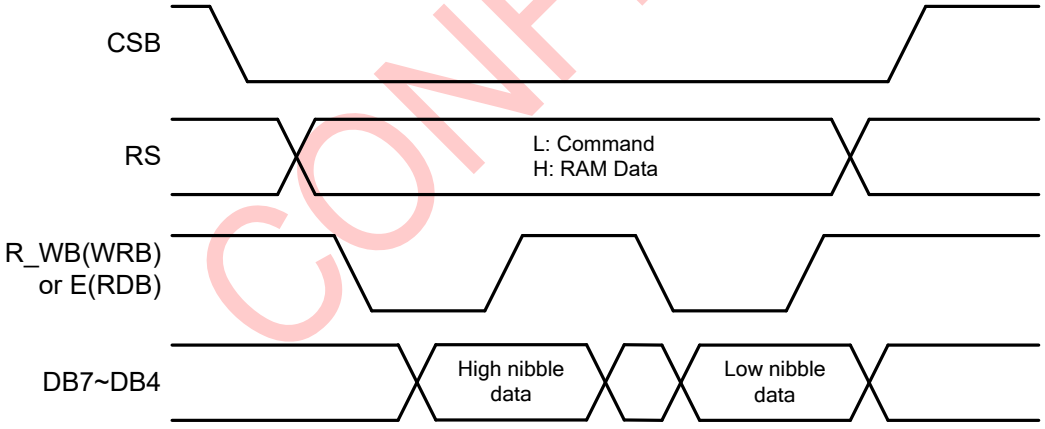
From the above timing diagram, it is important to note that the Busy Flag Check and the data transfer are both executed twice.

80-series interface

(a) 8-BIT mode



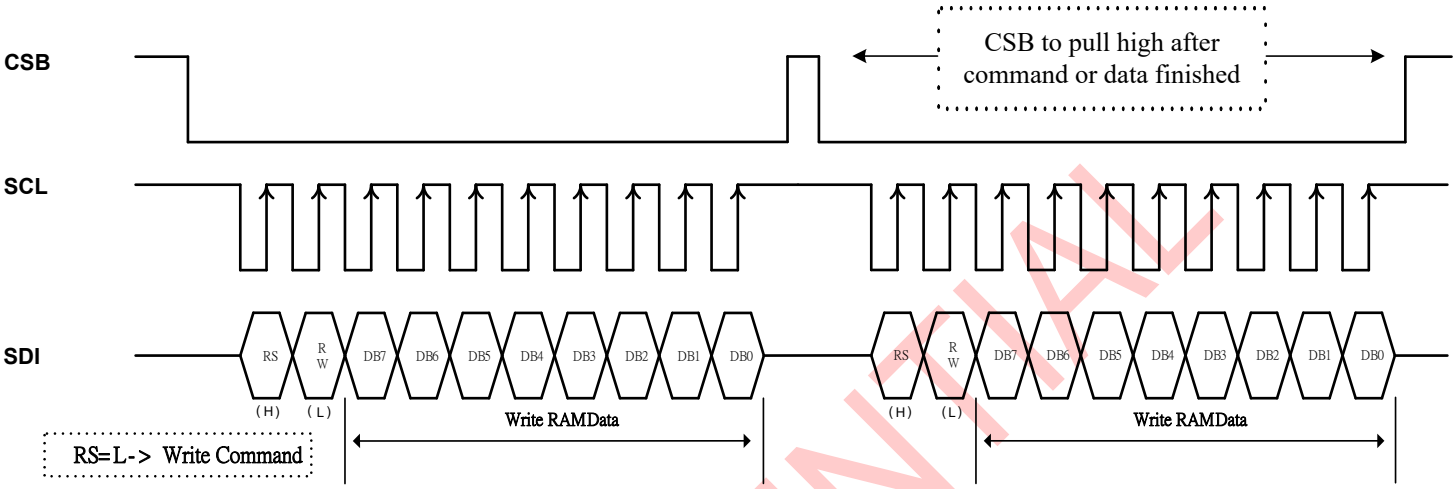
(b) 4-BIT mode



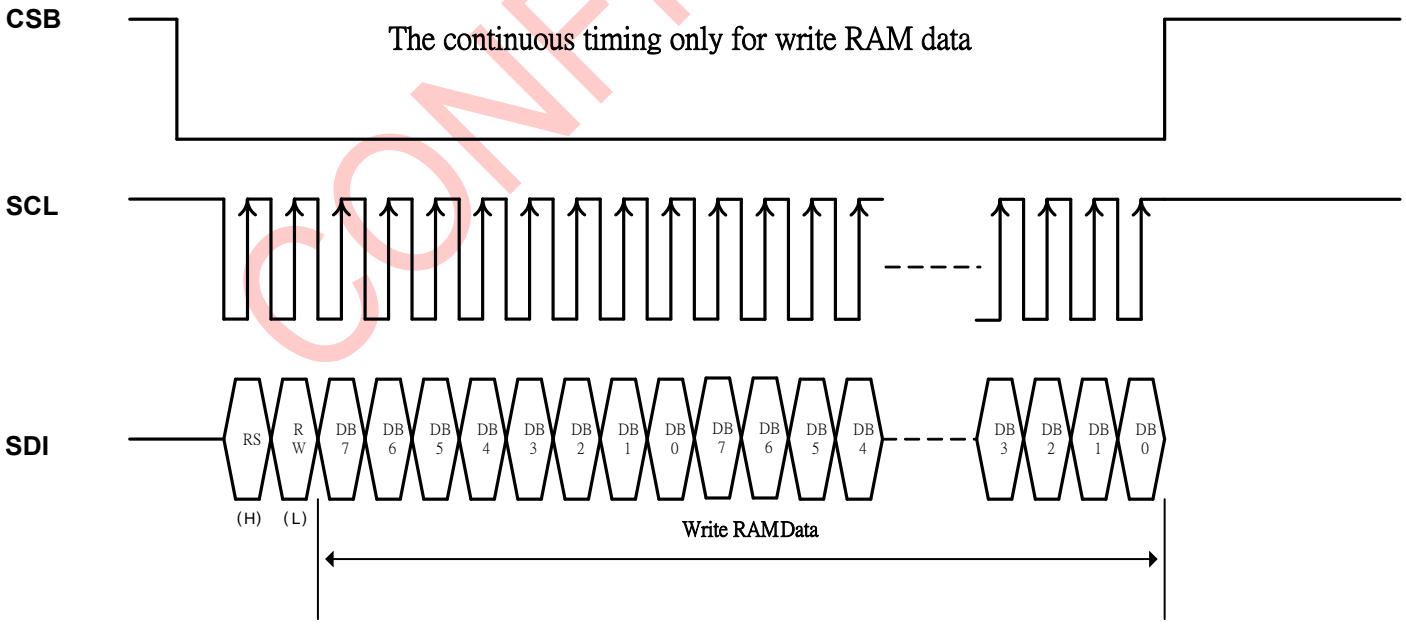
Serial interface

3-line serial write cycle

(a) Command write / RAM data single write

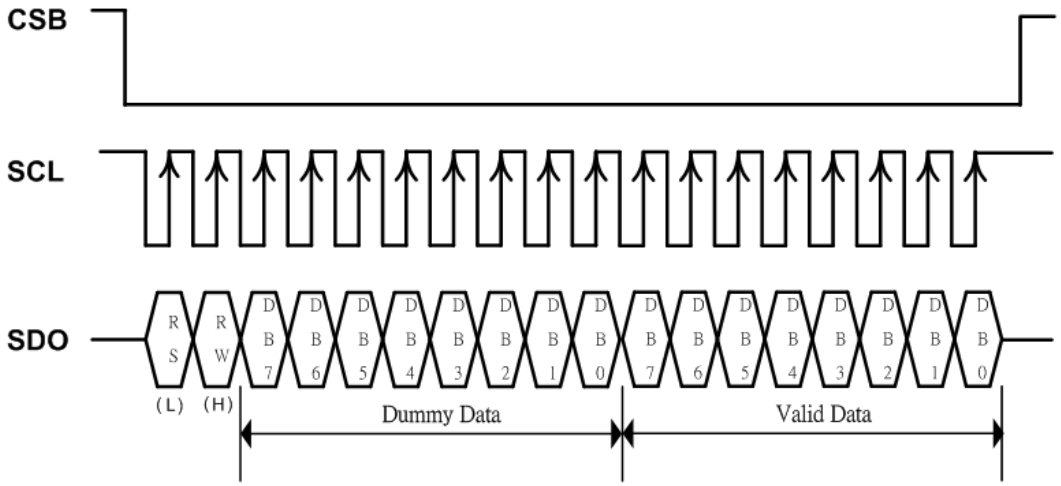


(b) RAM data continuous write

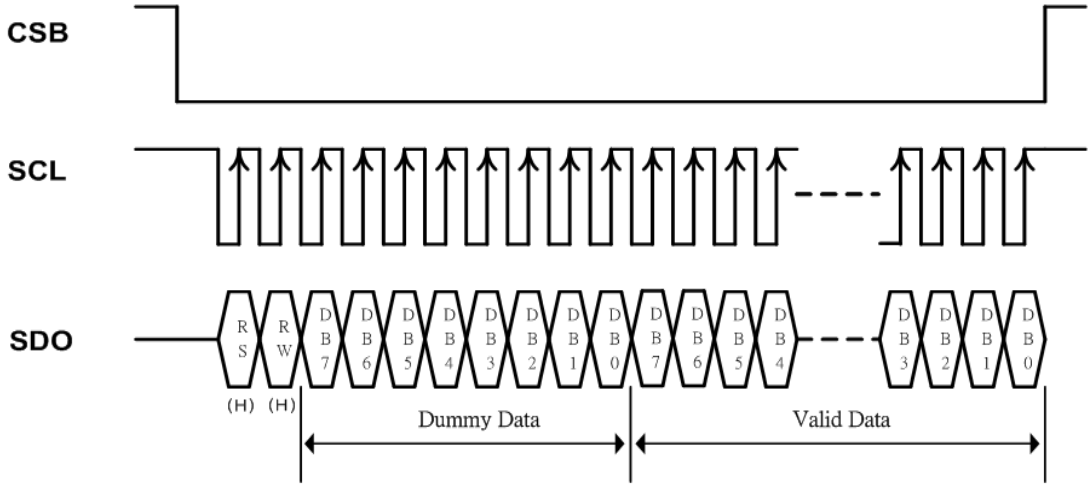


3-line serial read cycle

(a) Command Read

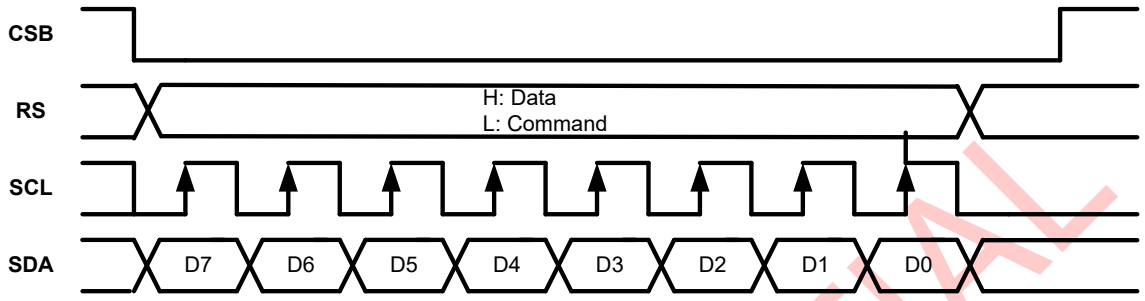


(b) RAM Read

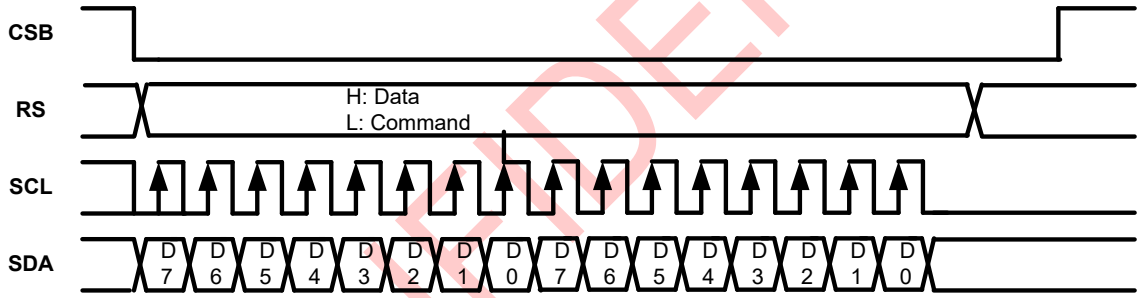


4-line serial write cycle

(a) Command write / RAM data single write

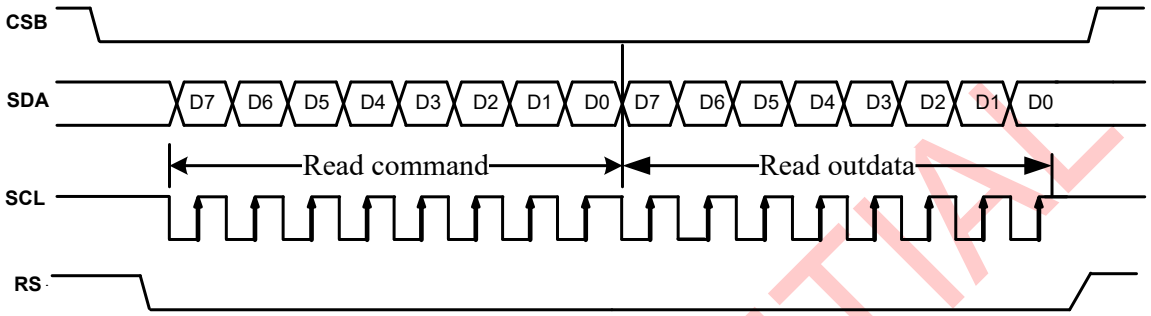


(b) RAM data continuous write

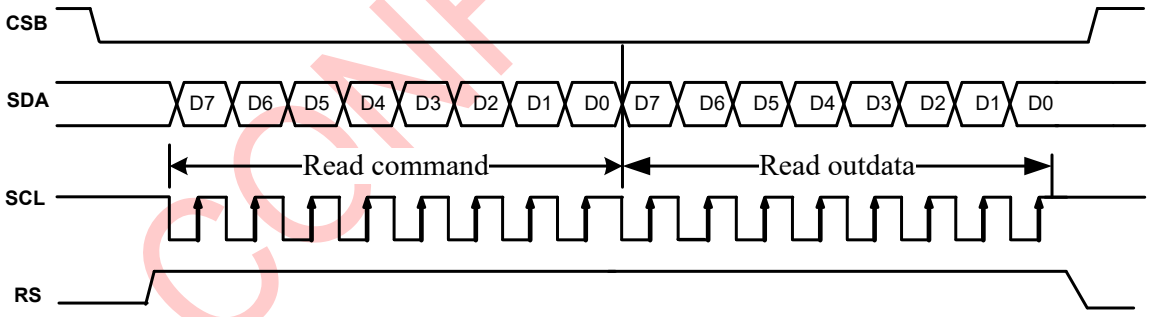


4-line serial read cycle

(a) Command Read

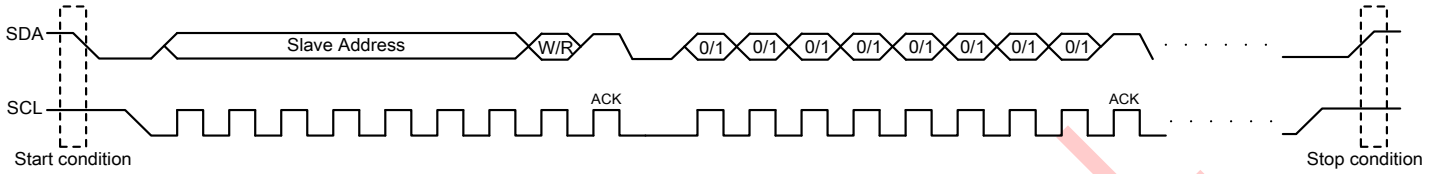


(b) RAM Read



IIC interface

The IIC interface is a bi-directional, two-line serial interface, the two lines are a Serial Data line(SDA) and a Serial Clock line(SCL), if MCU I/O is open-drain mode, both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.



START and STOP Conditions

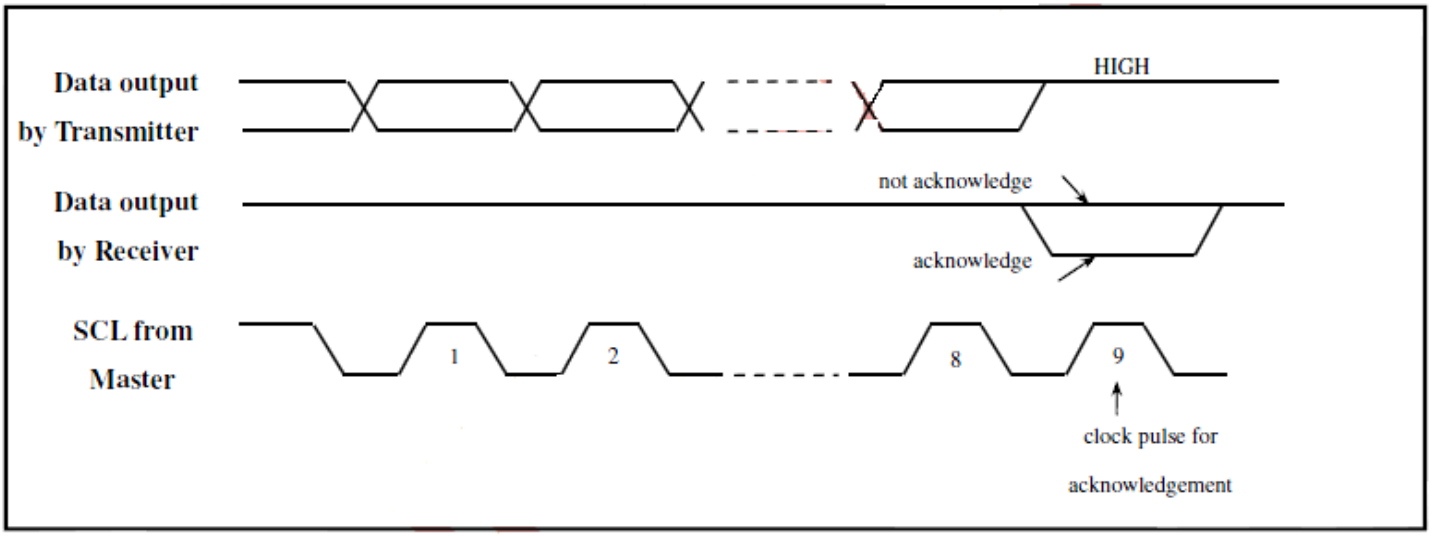
Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledgment bit. The acknowledgment bit is a HIGH signal put on the bus by the transmitter (to release the SDA control and waiting for receiver's acknowledgement), during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledgment after the reception of each byte. A master receiver must also generate an acknowledgment after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge must pull-down the SDA line during the acknowledgment clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledgment related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal and end-of-data to the transmitter by not generating an acknowledgment on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

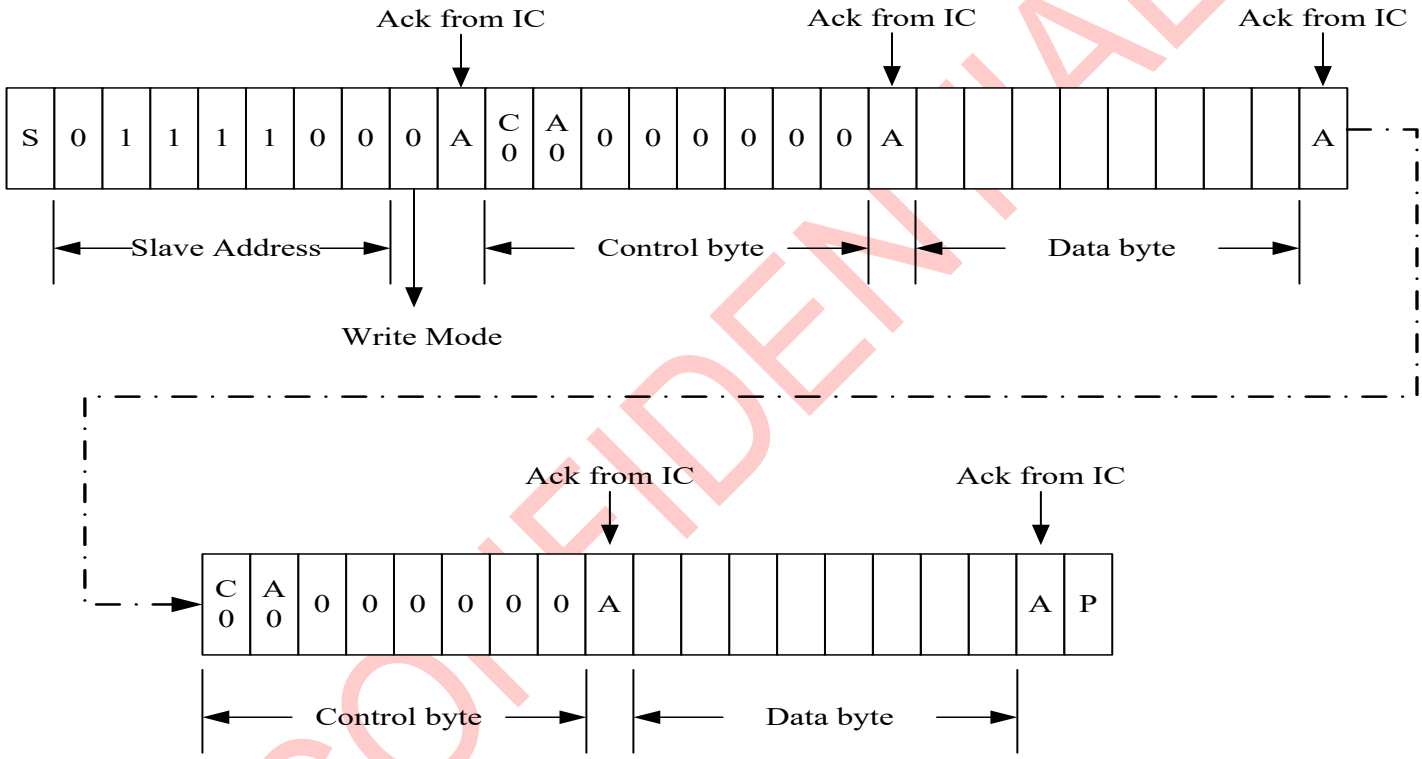


WRITE Mode (Master transmits data to Slave, R/W=0)

Write mode includes Slave address byte, control byte & data byte. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines C0 and A0, and a data byte. The control and data bytes are also acknowledged by all addressed slaves on the bus.

The C0 bit indicates the continuation of the command, please just set C0=1 during the whole Write transmitting period. The A0 bit decides the interpretation of the data byte. If A0 bit is 0, the data byte will be interpreted as command index, if A0 bit is 1, the data byte will be interpreted as command data.

A data transfer is always terminated by a STOP condition (P) generated by the master. However, if master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

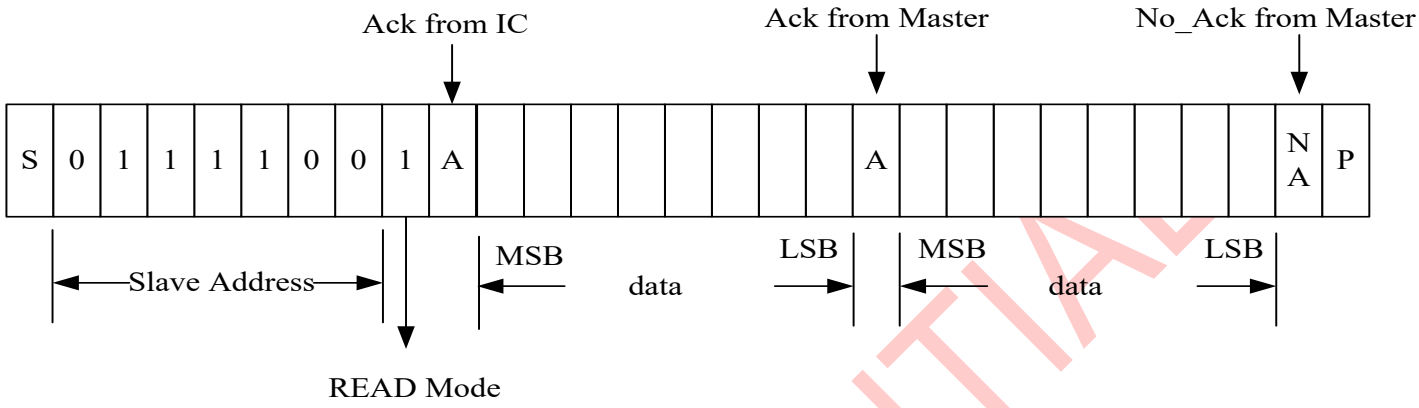


IIC Interface Protocol

The IIC transmitting is initiated with a START condition (S) from the IIC–bus Master and followed by a slave address. Four 7-bit slave addresses (0111100, 0111101, 0111110, and 0111111) are reserved for the IST1305CA1-B. The least significant bit of the slave address (ID) is configured by PS and C68 pin to decide is the slave address is 0111100 (PS=0/C68=0) or 0111101 (PS=0/C68=1) or 0111110(PS=1/C68=0) or 0111111(PS=1/C68=1). The 8th bit follows the previous 7-bit address is the data direction bit (R/W) -- '0' indicates Master data transmission (WRITE), '1' indicates Master data request (READ).

READ Mode (Master requests data from Slave, R/W=1)

At the moment of the first acknowledge, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave transmitter. The first acknowledge is still generated by the slave, but the following data bytes' acknowledgement are generated by Master. The STOP and Re-START conditions are generated by Master. If Master wants to stop the data request, after the last data byte has been received, send a Non-Acknowledge condition (keep SDA at HIGH) and trigger a STOP condition.



OLED INTERFACE

IST1305CA1-B supports two display types, namely :5x8 dots and 5x10 dots character fonts. Each of these types includes a cursor display. Up to 2 lines may be displayed in a 5x 8 dot character font type and 1 line for a 5x10 dots character font type. The number of lines that can bed is played as well as the type of font can be selected by using the software program. Please refer to the table below

Number of Display Line	Character Font Type	Number of Common Signals	Duty Factor
1	5 x 8 dots + cursor	8	1/8
1	5 x 10 dots + cursor	11	1/11
2	5 x 8 dots + cursor	16	1/16

SEG/COM OUTPUT MAPPING

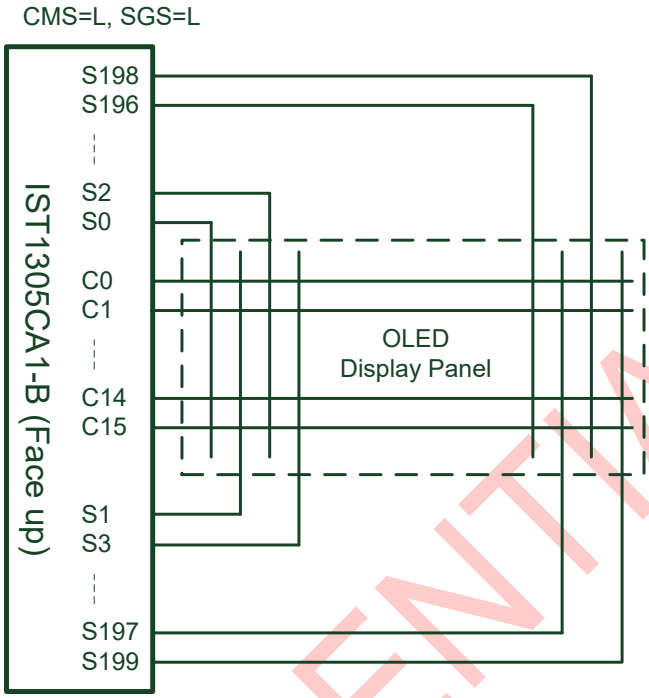
IST1305CA1-B COM outputs mapping can be configured by CMS pin. IST1305CA1-B SEG outputs mapping can be configured by SGS pin.

Pad No.	SGS=L
73	SEG<199>
74	SEG<197>
75	SEG<195>
76	SEG<193>
77	SEG<191>
78	SEG<189>
79	SEG<187>
80	SEG<185>
81	SEG<183>
82	SEG<181>
|	|
|	|
163	SEG<19>
164	SEG<17>
165	SEG<15>
166	SEG<13>
167	SEG<11>
168	SEG<9>
169	SEG<7>
170	SEG<5>
171	SEG<3>
172	SEG<1>

Pad No.	SGS=L
195	SEG<0>
196	SEG<2>
197	SEG<4>
198	SEG<6>
199	SEG<8>
200	SEG<10>
201	SEG<12>
202	SEG<14>
203	SEG<16>
204	SEG<18>
|	|
|	|
285	SEG<180>
286	SEG<182>
287	SEG<184>
288	SEG<186>
289	SEG<188>
290	SEG<190>
291	SEG<192>
292	SEG<194>
293	SEG<196>
294	SEG<198>

Pad No.	CMS=L	CMS=H
176	COM<15>	COM<0>
177	COM<14>	COM<1>
178	COM<13>	COM<2>
179	COM<12>	COM<3>
180	COM<11>	COM<4>
181	COM<10>	COM<5>
182	COM<9>	COM<6>
183	COM<8>	COM<7>
184	COM<7>	COM<8>
185	COM<6>	COM<9>
186	COM<5>	COM<10>
187	COM<4>	COM<11>
188	COM<3>	COM<12>
189	COM<2>	COM<13>
190	COM<1>	COM<14>
191	COM<0>	COM<15>

Examples are illustrated below.



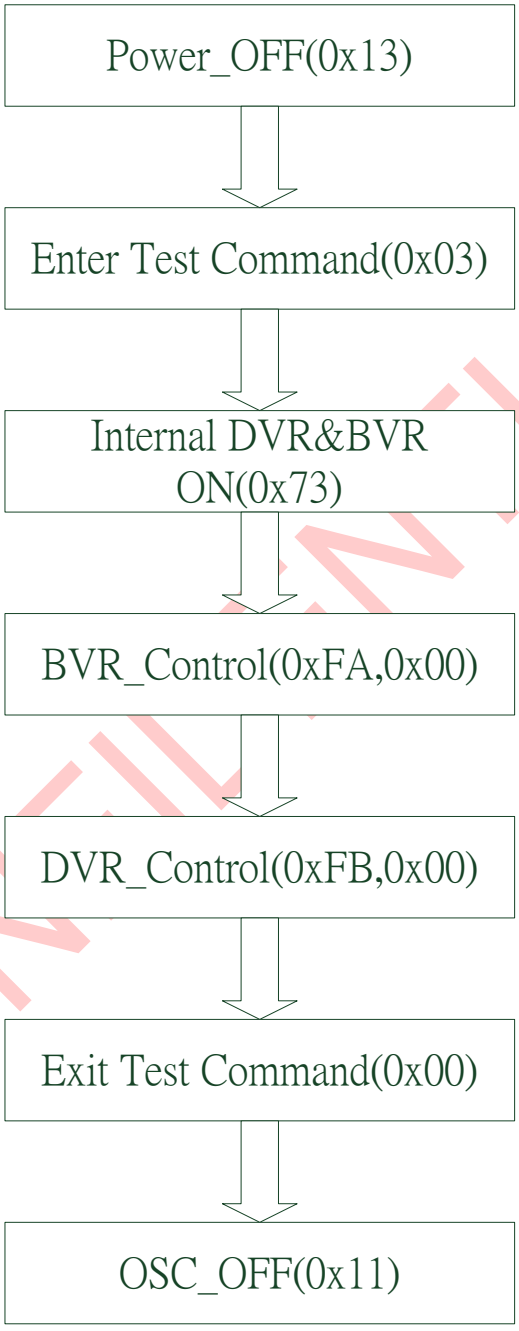
ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage range	VCC1/VCC2	- 0.3 to +6.5	V
	V16	-0.3 to +19.0	V
Input voltage range	VIN	-0.3 to VCC + 0.3	V
Operating temperature range	TOPR	-40 to +85	℃
Storage temperature range	TSTR	-55 to +150	℃

NOTES:

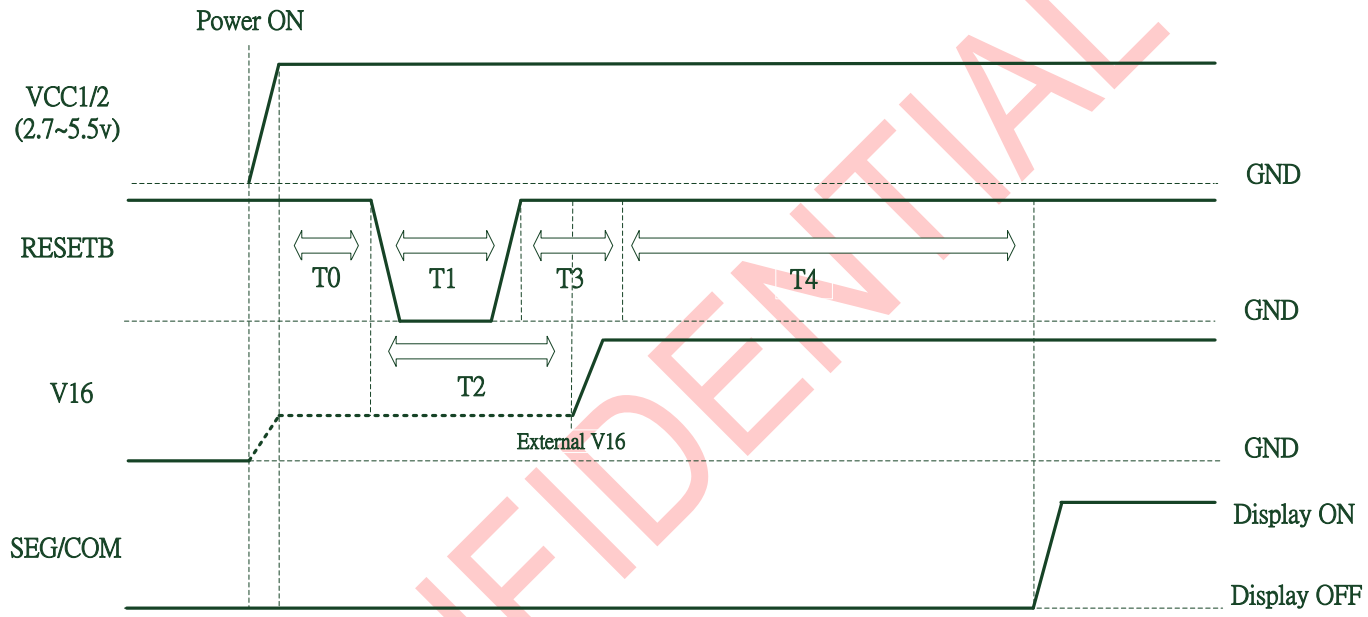
1. VCC1/VCC2 and V16 are based on GND/VSS2 = 0V
2. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

Standby mode



Power ON sequence(External V16)

1.Power ON VCC1/2, after VCC1/2 stable wait for at least 5ms(T0)(VDD stable delay time).
2.After VDD become stable, set RESETB pin LOW(logic low)for at least 5ms(T1)and then High(logic high).
3.After set RESETB pin LOW(logic low),wait for at least 15ms(T2).Then Power ON V16.
4.After set RESETB pin High(logic high),OTP reload wait for at least 10ms(T3).
5.After V16 become stable, send fundamental command 0Ch for display ON.SEG/COM will be ON after 100ms(T4).

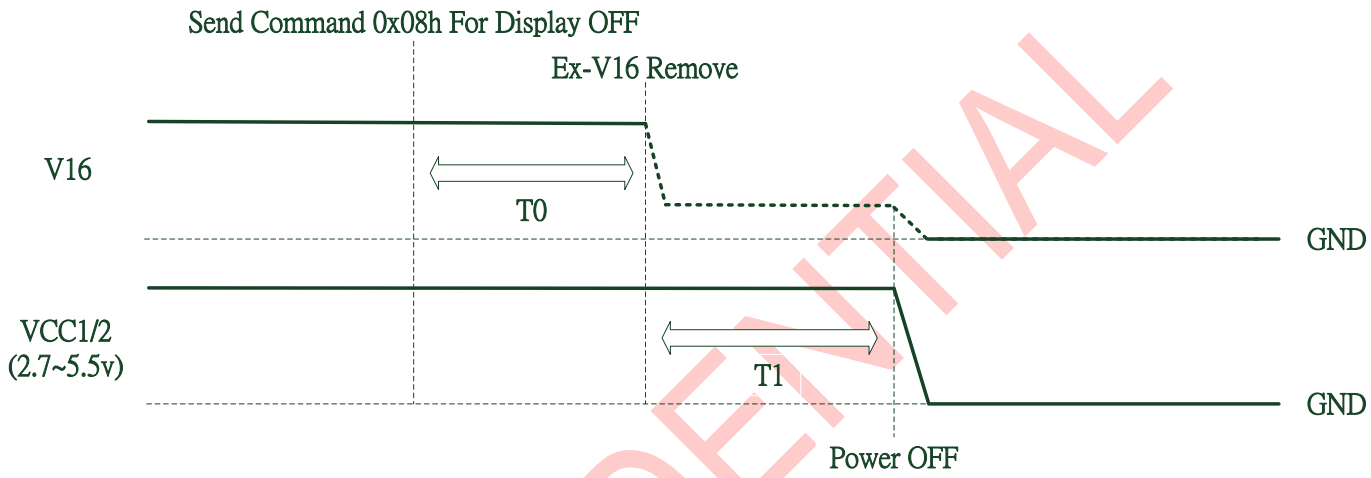


T0>=5ms(Internal VDD stabilization delay time)
T1>=5ms(Reset delay time)
T2>=15ms(Contact external V16 delay time)
T3>=10ms(OTP reloading delay time)
T4>=100ms(External V16 stabilization delay time)

Note:
*1) Since an ESD protection circuit is connected between VCC1/2 and V16, V16 becomes lower than VCC1/2,VCC1/2 is ON and V16 is OFF as shown in the dotted line(illustrated above).
*2)The register values are reset after T1.
*3)Power pins(VCC1,VCC2,V16)can never be pulled to ground under any circumstance.

Power OFF sequence(External V16)

1. Send fundamental command 08h for display OFF.
2. After send fundamental command 08h for display OFF, for at least 15ms(T0),can be remove external V16.
3. Remove external V16 for at least 20ms(T1),can be shut down VCC1/2.

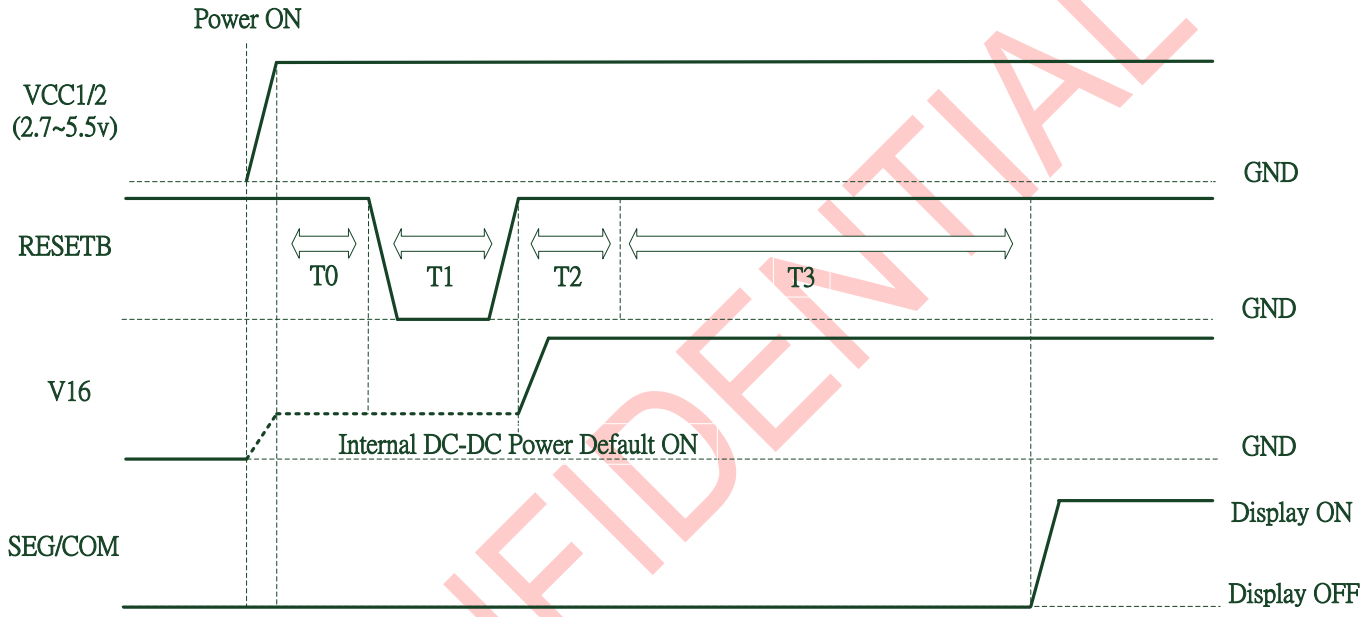


T0>=15ms, T1>=20ms

Note:
*1) Since an ESD protection circuit is connected between VCC1/2 and V16, V16 becomes lower than VCC1/2,VCC1/2 is ON and V16 is OFF as shown in the dotted line(illustrated above).
*2) VCC1/2 should not be Power OFF before V16 Power OFF.
*3) Power pins(VCC1,VCC2,V16)can never be pulled to ground under any circumstance.

Power ON sequence(Internal V16)

1.Power ON VCC1/2, after VCC1/2 stable wait for at least 5ms(T0)(VDD stable delay time).
2.After VDD become stable, set RESETB pin LOW(logic low)for at least 5ms(T1)and then High(logic high).
3.After set RESETB pin High(logic high),OTP reload wait for at least 10ms(T2).
4.After V16 become stable, send fundamental command 0Ch for display ON.SEG/COM will be ON after 100ms(T3).

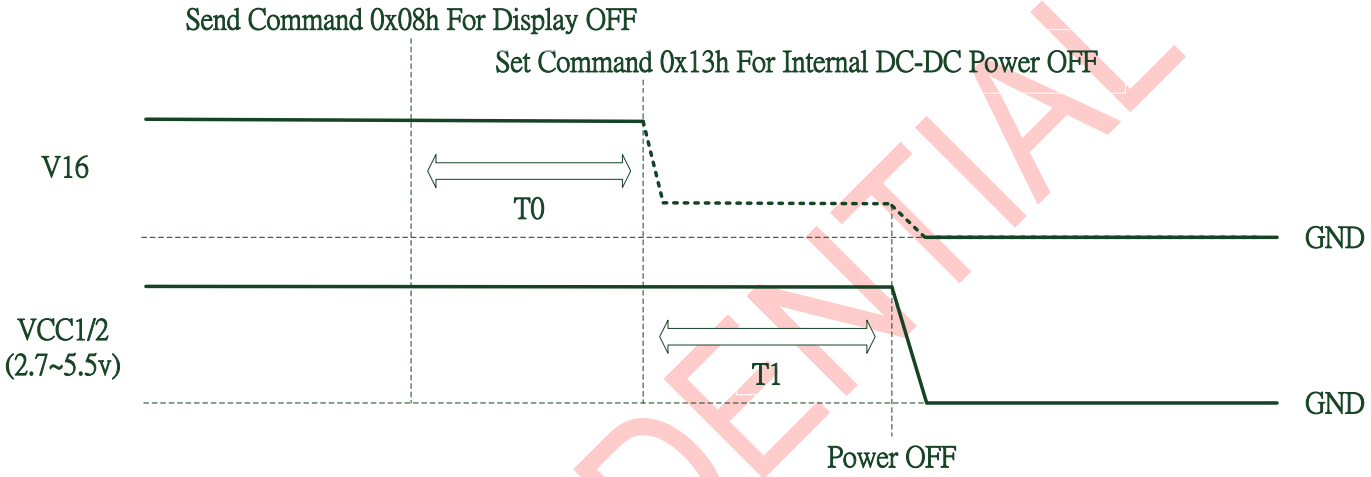


T0>=5ms(Internal VDD stabilization delay time)
T1>=5ms(Reset delay time)
T2>=10ms(OTP reloading delay time)
T3>=100ms(DC-DC V16 stabilization delay time)

Note:
*1) Since an ESD protection circuit is connected between VCC1/2 and V16, V16 becomes lower than VCC1/2,VCC1/2 is ON and V16 is OFF as shown in the dotted line(illustrated above).
*2)The register values are reset after T1.
*3)Power pins(VCC1,VCC2,V16)can never be pulled to ground under any circumstance.

Power OFF sequence(Internal V16)

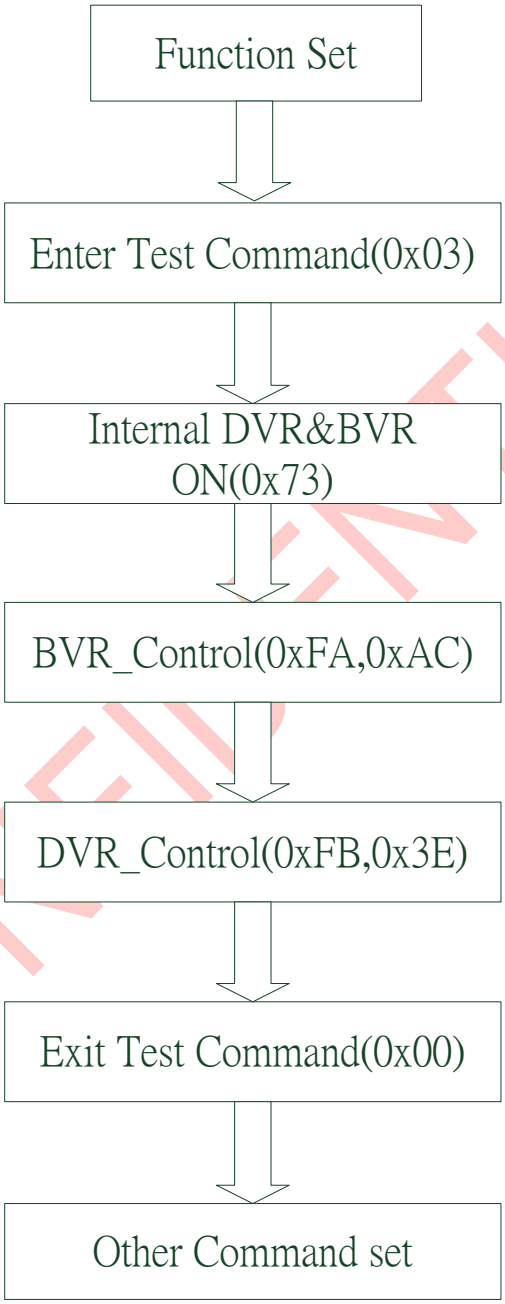
1. Send fundamental command 08h for display OFF.
2. After send fundamental command 08h for display OFF, for at least 15ms(T0),can be Send fundamental command 13h for DC-DC power OFF.
3. Send fundamental command 13h for DC-DC power OFF at least 20ms(T1),can be shut down VCC1/2.



T0>=15ms, T1>=20ms

Note:
*1) Since an ESD protection circuit is connected between VCC1/2 and V16, V16 becomes lower than VCC1/2,VCC1/2 is ON and V16 is OFF as shown in the dotted line(illustrated above).
*2) VCC1/2 should not be Power OFF before DC-DC Power OFF.
*3) Power pins(VCC1,VCC2,V16)can never be pulled to ground under any circumstance.

Internal DVR/BVR mode initial by instruction



DC CHARACTERISTICS

(GND = 0V, VCC = 2.7 to 5.5V, Ta = 25℃)

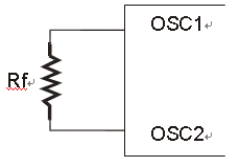
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating Voltage		VCC		2.7	-	5.5	V	VCC
Operating Voltage		V16		-	-	16	V	V16
Input voltage	High	V_{IH}		0.8VCC	-	VCC	V	*1
	Low	V_{IL}		-	-	0.2VCC		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8 VCC	-	VCC	V	*2
	Low	V_{OL}	I_{OL} = 0.5mA	-	-	0.2 VCC		
Input leakage current		IIL\IIH	V_{IN} = VCC or GND	-1	-	1	μA	*1
Oscillator frequency		fOSC	External OSC(Rf=75K)	460	620	780	KHz	OSC2
			External OSC(Rf=43K)	580	780	980		
High level segment output current		ISEGOH	VSEGOH=14V	-30	-	-300	μA	SEG0~199
High level segment output current tolerance		ITOL	VSEGOH=14V	-	-	±6	%	SEG0~199
Low level common sink current		ICOMOL	VCOMOL=0.4V	15	-	-	mA	COM0~15
DC-DC converter output voltage		V16	-	-	-	16	V	V16

Notes:

*1: SHL,CSB,DB7~DB0,RESETB,RS,R_WB,E,PS,C86,IIC,IERSEL,SGS,CMS

*2: DB7~DB0

*3:



External DVR/BVR Mode （DVR=4.7MOhm, BVR=10KOhm）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Standby current	Istd	Istd1=IVCC1+IVCC2 VCC1=VCC2=3.3v, Ex-OSC(75K/43K) 25C,With Panel(*4)			100	uA	VCC1,VCC2
Standby current (External V16)	Istd2	Istd2=IV16 V16=16v Ex-OSC(75K/43K) VCC1=VCC2=3.3v 25C,With Panel(*4)			75	uA	V16
Operating current	Iop	VCC1=3.3V Ex-BVR,DVR(10K,4.7M) Ex-OSC(75K/43K), 25C, No loading	-	-	330	uA	VCC1

Internal DVR/BVR Mode (*5)（DVR=0x3E, BVR=0xAC）

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Standby current	Istd1	Istd1=IVCC1+IVCC2 VCC1=VCC2=3.3v Ex-OSC(43K) 25C,With Panel(*4)			100	uA	VCC1,VCC2
Standby current (External V16)	Istd2	Istd2=IV16 V16=16v VCC1=VCC2=3.3v 25C,With Panel(*4)			75	uA	V16
Operating current	Iop	VCC1=3.3V Ex-OSC(43K) 25C, No loading	-	-	330	uA	VCC1

Notes:

*4: Standby mode setting refers to “Standby mode” page.

*5: Internal DVR/BVR mode setting refers to “Internal DVR/BVR mode initial by instruction“ page.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

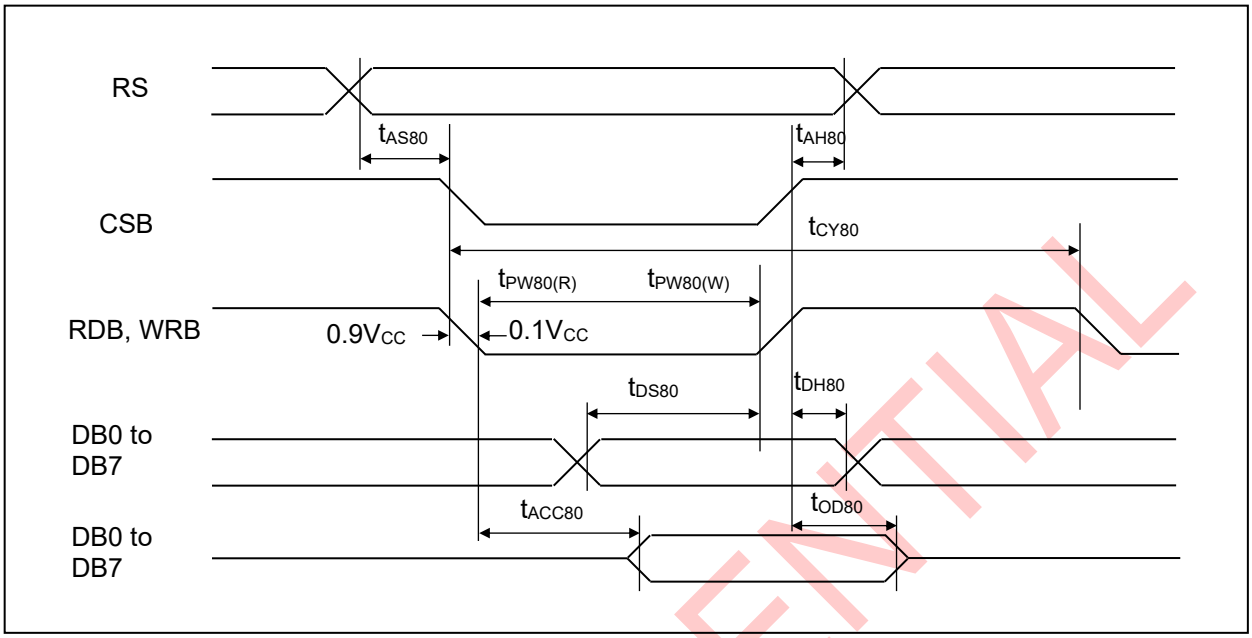


Figure 1. Read / Write Characteristics (8080-series MPU)

Vcc = 2.7 to 5.5V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	**tAS80** **tAH80**	20 0	-	-	ns	
System cycle time		**tCY80**	500	-	-	ns	
Pulse width (WRB)	RW_WRB	**tPW80**(W)	250	-	-	ns	
Pulse width (RDB)	E_RDB	**tPW80**(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	**tDS80** **tDH80**	40 20	-	-	ns	
Read access time Output disable time		**tACC80** **tOD80**	- 10	-	180 -	ns	CL = 100pF

Read / Write Characteristics (6800-series Microprocessor)

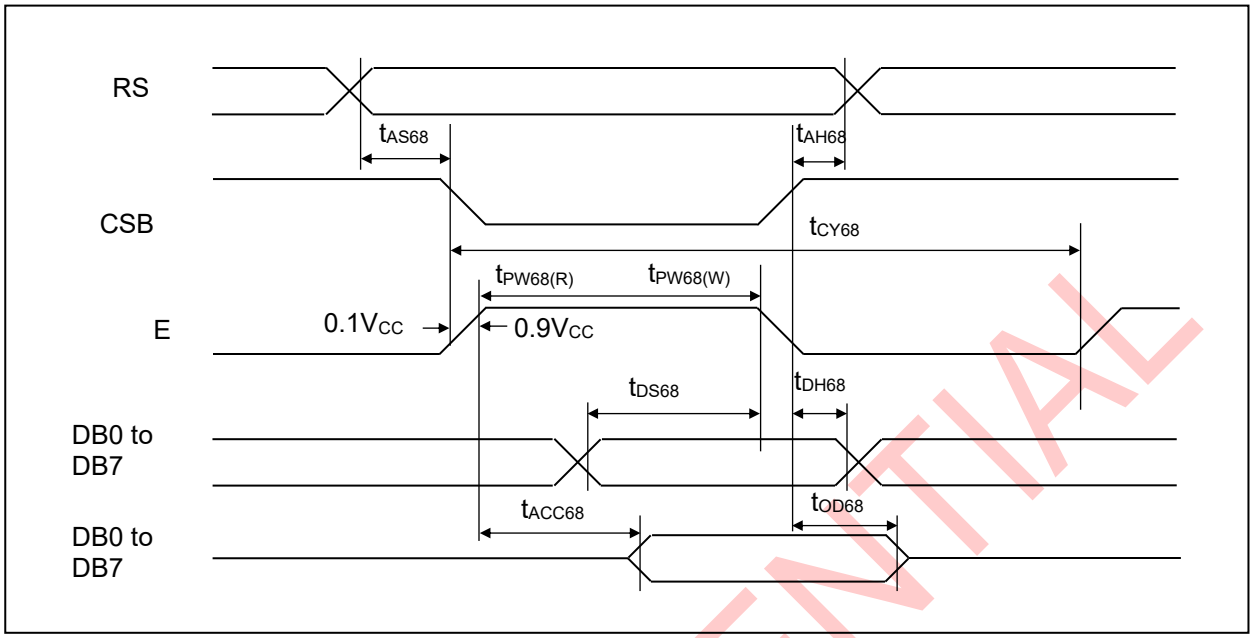


Figure 2. Read / Write Characteristics (6800-series MPU)

(Vcc = 2.7 to 5.5V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	tAS68 tAH68	20 0	-	-	ns	
System cycle time		tCY68	500	-	-	ns	
Pulse width (E)	E_RDB	tPW68(W)	250	-	-	ns	
Pulse width (E)	E_RDB	tPW68(R)	250	-	-	ns	
Data setup time Data hold time	DB7 to DB0	tDS68 tDH68	40 20	-	-	ns	
Read access time Output disable time		tACC68 tOD68	- 10	-	180 -	ns	CL = 100pF

Serial Interface Characteristics

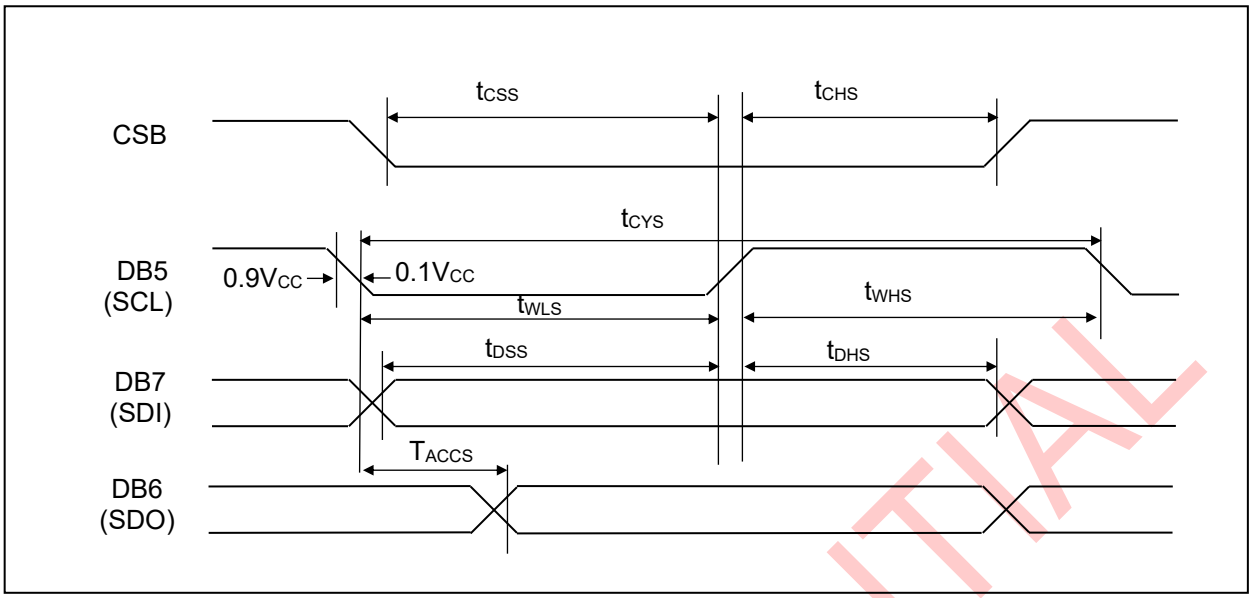
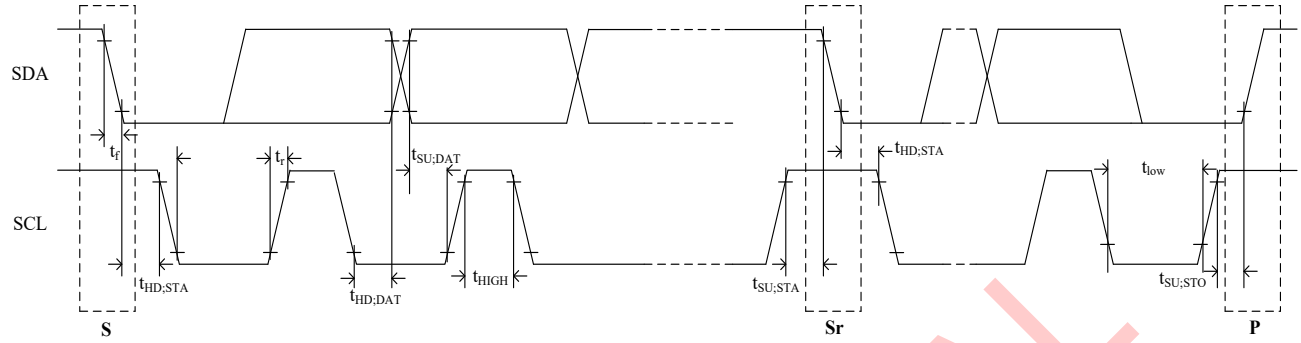


Figure 3. Serial Interface Characteristics

(Vcc = 2.7 to 5.5V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCL high pulse width SCL low pulse width	DB5 (SCL)	tCYS tWHS tWLS	300 100 100	- - -	- - -	ns	
CSB setup time CSB hold time	CSB	tCSS tCHS	150 150	- -	- -	ns	
Data setup time Data hold time	DB7 (SDI)	tDSS tDHS	100 100	- -	- -	ns	
Read access time	DB6 (SDO)	tACCS	-	-	80	ns	

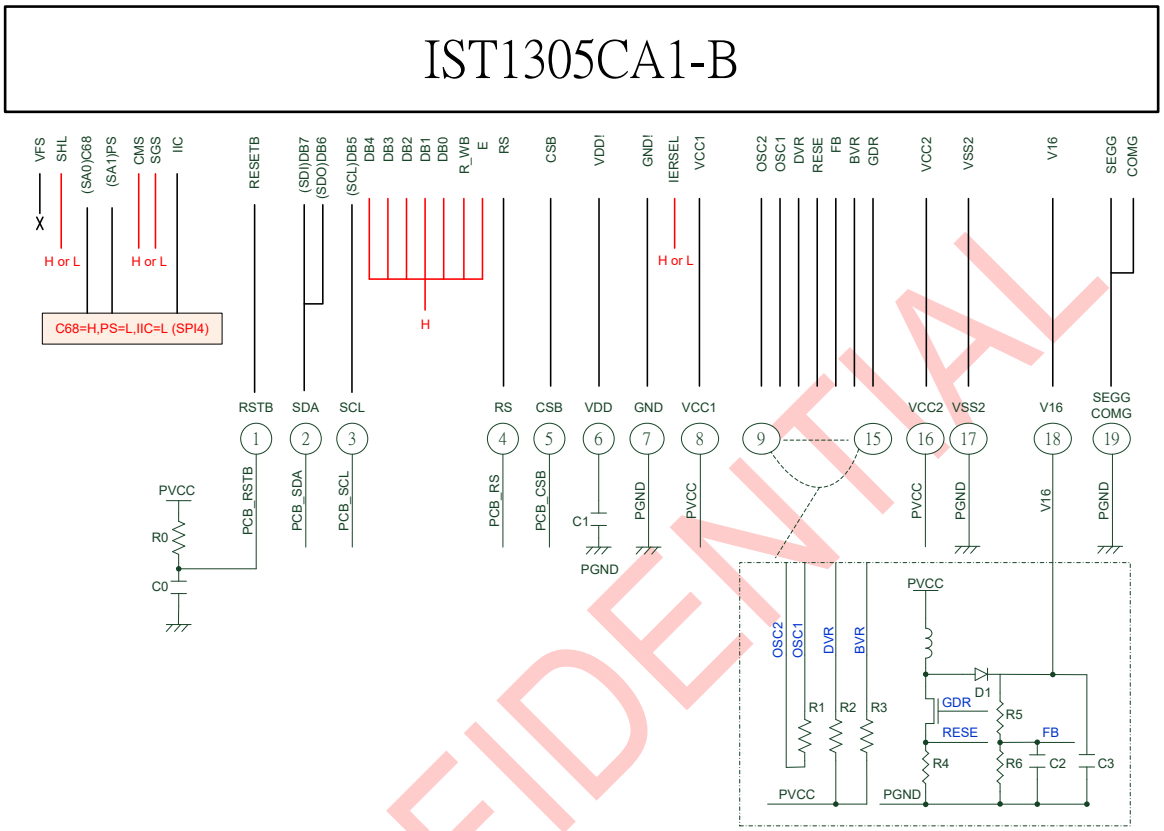
IIC interface Timing Characteristics



(Vcc = 2.7 to 5.5V, Ta = 25℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
SCL clock frequency		fSCL	0	-	400	kHz	
Set-up time for START condition		tSU/STA	600	-	-	ns	
Hold time for START condition		tHD/STA	600	-	-	ns	
Low period of the SCL clock		tLow	1300	-	-	ns	
High period of the SCL clock		tHIGH	600	-	-	ns	
Data set-up time		tSU/DAT	100	-	-	ns	
Data hold time		tHD/DAT	-	-	900	ns	
Rise time of both SDA and SCL signals		tr	-	-	30	ns	
Fall time of both SDA and SCL signals		tf	-	-	30	ns	
Set-up time for STOP condition		tSU/STO	600	-	-	ns	

APPLICATION EXAMPLE (SPI 4)



I/O Configuration			
IIC	PS	C68	I/O
L	L	L	SPI3
L	L	H	SPI4
L	H	L	P80
L	H	H	P68
H	H/L	H/L	IIC

IERSEL :
H: Internal Oscillator R
L: External Oscillator R

Peripheral Components			
Item	Value (Ohm)	Item	Value
R0	10K~15K	C0	0.1uF~1uF
R1	39K~75K (IERSEL=L)	C1	1uF~2uF
R2	4.7M~10M	C2	10nF~0.1uF
R3	4.3K~20K	C3	10uF~20uF
R4	1	L0	330uH
R5	510K	D1	4148
R6	51K	N1	N-channel MOSFET

CAUTIONS:

1. This Specification will be subjected to modify without notice.
2. Precautions on Light:
   Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

2.1 Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation.

2.2 Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3 The IC must be shielded from light in the front, back and side faces.

3. ESD control and prevention:
   3.1 Humidity Control: 30~70% relative humidity is recommended.
   3.2 To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed.(Example: Station ionizers).
   3.3 Grounding all personnel who come in contact with parts will eliminate a possible source of ESD.
   (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4. Storage Conditions:

Before open package	After open package
Temp.=25±10℃ Humidity:35~75% Less than 1 Years	Temp.=25±10℃ Humidity:35~75% Less than 3 Months