ST72568C

1200CH System-On-Chip Driver for 800RGBx480 TFT LCD

Datasheet

V1.0
2026/03

Hazardous Substance Free
RoHS/ REACH Compliant

Sitronix Technology Corporation

LIST OF CONTENT

1. GENERAL DESCRIPTION

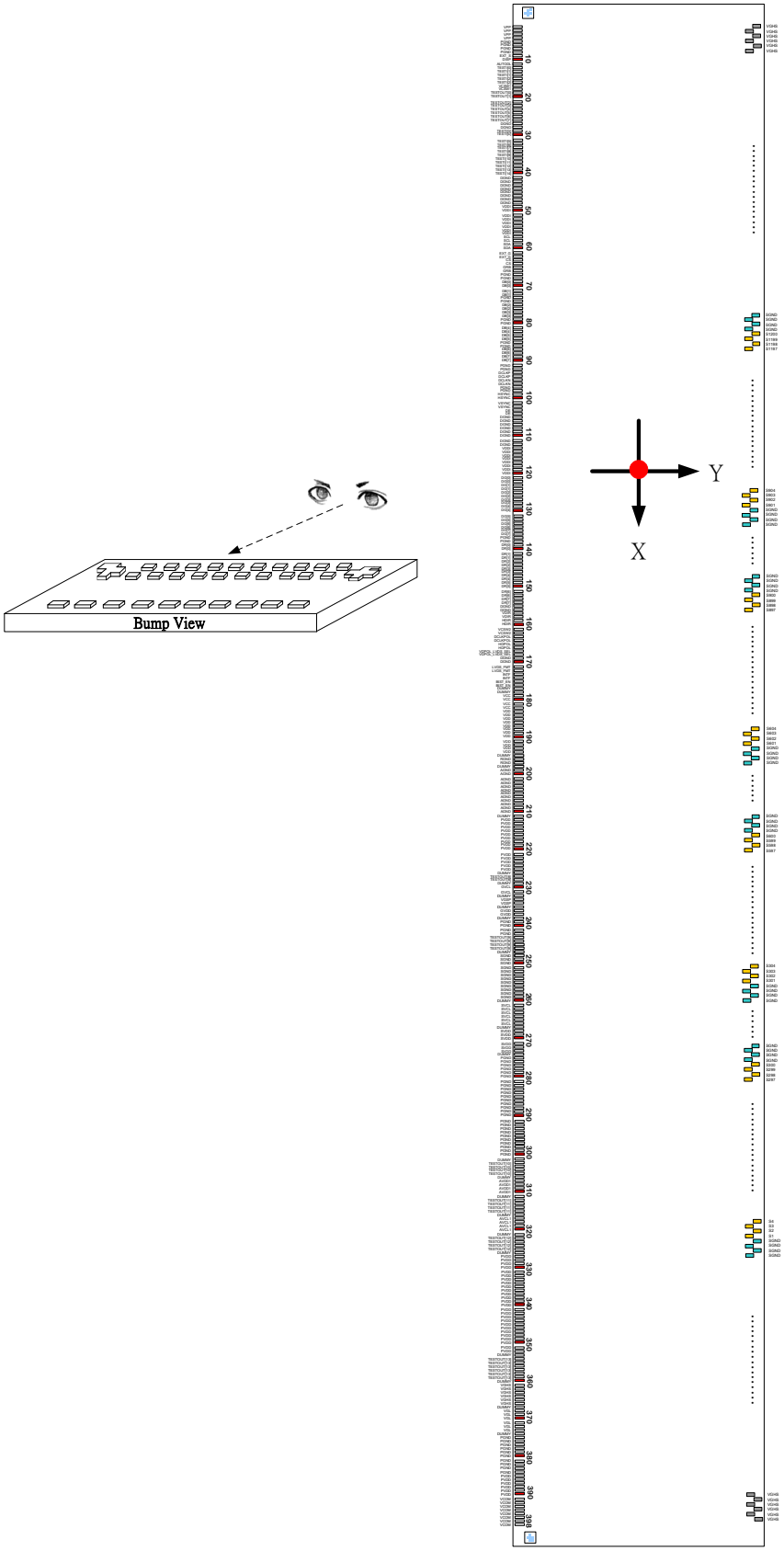
IC offers all-in-one chip solution of 800RGBx480 for color dual gate TFT-LCD panel. The driver IC output ports consists of 1200 source channels and 24 gate control channels for panel application. This chip incorporated with digital timing generator, source and gate driver, power supply circuit and embedded 3-wire SPI interfaces for function setting. The display data bits sent from MCU via LVDS interface or RGB interface directly related to the pixels of LCD panel. The source output supports 256 gray scale with real 8-bit DAC to get a small output deviation for high color resolution. The power supply circuit incorporated with step-up circuit, regulators and operational amplifiers to generate power supply voltages to drive TFT LCD.

2. FEATURES

- Display Resolution: 800RGB (H) * 480(V) , supports arbitrary resolution 200RGB+4*N (H)
  -256 Gray Scale with True 8-bit DAC
  -full color mode: 16.7M colors (25-bit 8(R):8(G):8(B))
- LCD Driver Output Circuits
  - source outputs: 1200channels
  - gate outputs: 24 GIP control signals
  - common electrode output
- Display Data Interface
  - 3 lane and 4 lane LVDS interface
  - 24-bit RGB interface support: SYNC, SYNC-DE and DE mode
- Register Setting Interface
  - 3-wire SPI interface
- On Chip Build-In Circuits
  - DC/DC converter
  - Multi-OTP circuit
  - Timing controller
- Wide Supply Voltage Range
  - I/O voltage (VDDI to DGND): 3.1V~3.6V
  - analog voltage (VDD to AGND): 3.1V ~3.6V
  - charge pump voltage (PVDD to PGND): 3.1V ~3.6V
- On-Chip Power System
  - GVDD: 4.6125V ~ 6.0V
  - GVCL: -3.0125V ~ -4.40V
  - VCOM: GND (Including built-in circuit for compensating feed-through voltage)
  - Maximum Vop : Vop(Max.) ≤ GVDD-VCOM” = VCOM”-GVCL
- Optimized Layout for COG Assembly
- Support 1 Power Mode and 3 Power Mode
- Built-in Multi-OTP Programming Circuit
  - Internal VPP power supply
- Multi-OTP Adjustable Parameters
  - 7-bit for VCOM offset adjustment
  - 7-bit ID1/ID2/ID3 OTP for end user use
- Temperature Range: −30°C ~ 85°C
- GAS function for preventing image sticking when abnormal power off
- Design for industrial applications; this product is not designed for use in military equipment, marine equipment, aircraft equipment and other applications in extreme environment

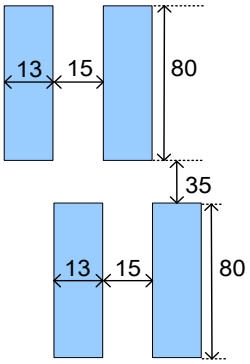
3. PAD ARRANGEMENT

3.1 Output Bump Dimension

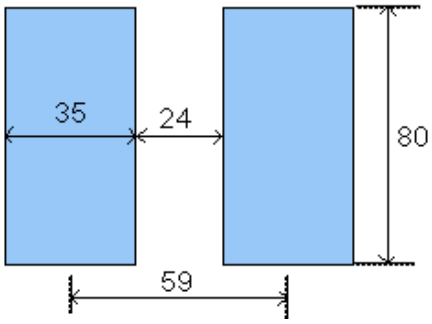


3.2 Bump Dimension

(Pad NO. 399~1990)

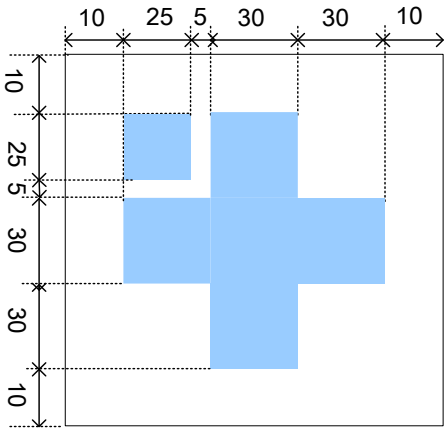


(Pad NO. 1~398)

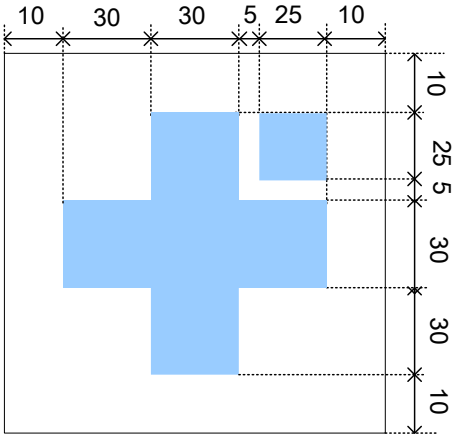


3.3 Alignment Mark Dimension

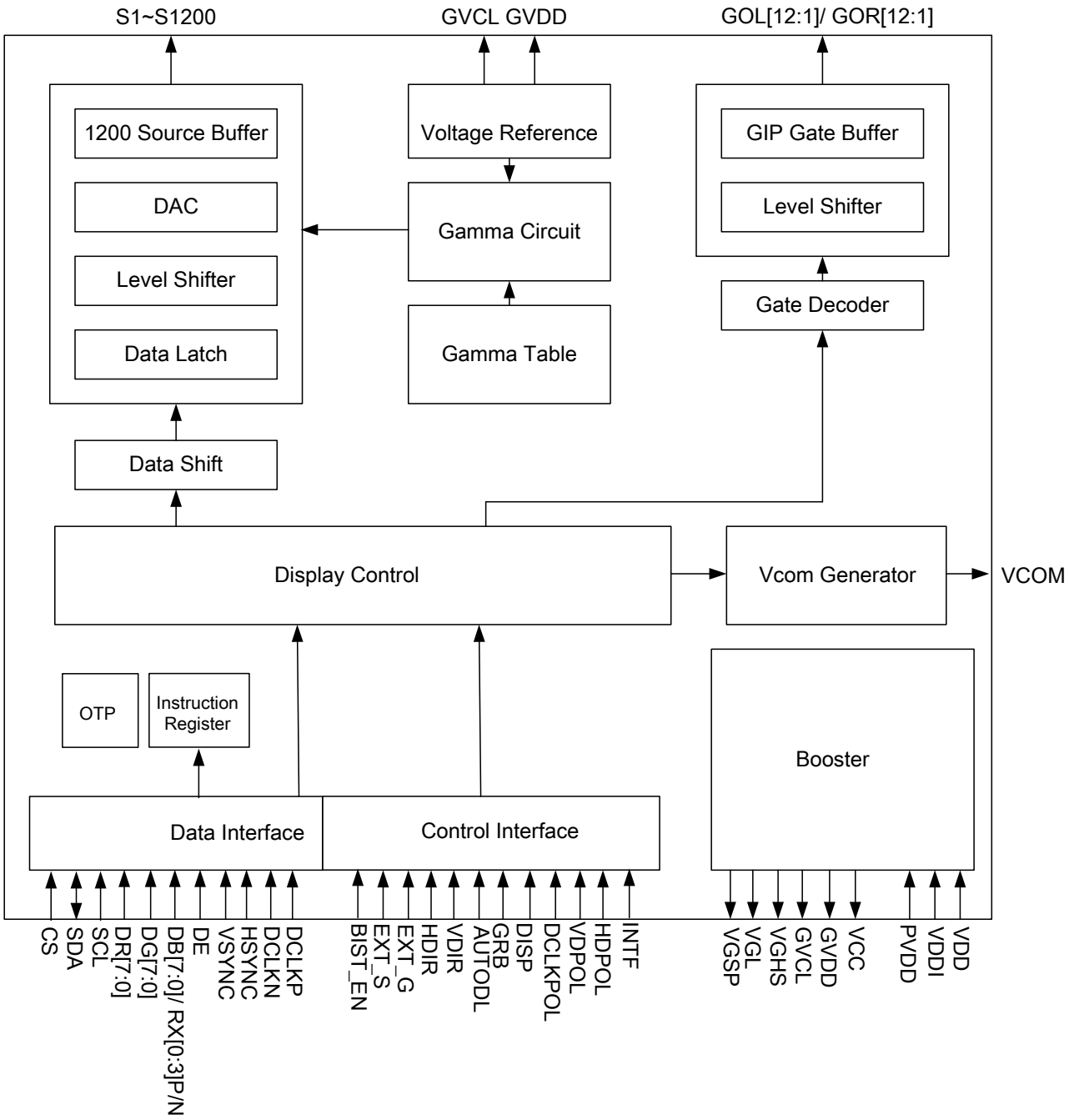
Alignment Mark: A1(X,Y)=(-11812,-337)



Alignment Mark: A2(X,Y)=(11812,-337)



4.BLOCK DIAGRAM



5. PIN DESCRIPTION

5.1 Pin Function

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="3">3-Wire SPI Interface Pins</td></tr>
<tr><td>CS</td><td>I</td><td>Serial communication chip selection.</td></tr>
<tr><td>SDA</td><td>I/O</td><td>Serial communication data input and output.</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial communication clock input.</td></tr>
<tr><td colspan="3">Control Pins</td></tr>
<tr><td>EXT_S</td><td>I</td><td>Power mode setting
<table>
<tr><th>EXT_S</th><th>Function Description</th></tr>
<tr><td>L</td><td>1 power mode (Internal pump mode)</td></tr>
<tr><td>H</td><td>3 Power Mode (Charge pump controller)
3 Power Mode (External power supply)</td></tr>
</table></td></tr>
<tr><td>VCSW[2:1]</td><td>O</td><td>PFM and Power IC control output for DC/DC converter.</td></tr>
<tr><td>GRB</td><td>I</td><td>Global reset pin. When GRB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>DISP</td><td>I</td><td>DISP sets the display mode.
<table>
<tr><th>DISP</th><th>Function Description</th></tr>
<tr><td>L</td><td>Standby mode(Default)</td></tr>
<tr><td>H</td><td>Normal display mode</td></tr>
</table></td></tr>
<tr><td>HDIR</td><td>I</td><td>Horizontal scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>HDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From right to left</td></tr>
<tr><td>H</td><td>From left to right(Default)</td></tr>
</table></td></tr>
<tr><td>VDIR</td><td>I</td><td>Vertical scan direction control pin. This pin must be connected to “H” or “L” according to system application.
<table>
<tr><th>VDIR</th><th>Function Description</th></tr>
<tr><td>L</td><td>From down to up</td></tr>
<tr><td>H</td><td>From up to down(Default)</td></tr>
</table></td></tr>
<tr><td>AUTODL</td><td>I</td><td>OTP trim function control pin. When normal display, AUTODL should be set to “H” and the value in the OTP will be downloaded automatically.
<table>
<tr><th>AUTODL</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable auto-refresh function</td></tr>
<tr><td>H</td><td>Enable auto-refresh function(Default)</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BIST_EN</td><td>I</td><td>BIST function control pin.
<table>
<tr><th>BIST_EN</th><th>Function Description</th></tr>
<tr><td>L</td><td>Disable BIST function(Default)</td></tr>
<tr><td>H</td><td>Enable BIST function</td></tr>
</table></td></tr>
<tr><td>INTF</td><td>I</td><td>Set RGB interface or LVDS interface.
<table>
<tr><th>INTF</th><th>Function Description</th></tr>
<tr><td>L</td><td>RGB interface mode(Default)</td></tr>
<tr><td>H</td><td>LVDS interface mode</td></tr>
</table></td></tr>
<tr><td colspan="3">Interface Control Pins</td></tr>
<tr><td>VDPOL_LVDS_SEL</td><td>I</td><td>VDPOL_LVDS_SEL sets VSYNC polarity in RGB interface and data format 3, 4 lane in LVDS interface.
<table>
<tr><th>MCU Type</th><th>VDPOL_LVDS_SEL</th><th>Function Description</th></tr>
<tr><td rowspan="2">RGB interface</td><td>L</td><td>VSYNC polarity: positive</td></tr>
<tr><td>H</td><td>VSYNC polarity: negative(Default)</td></tr>
<tr><td rowspan="2">LVDS interface</td><td>L</td><td>LVDS 3 lane</td></tr>
<tr><td>H</td><td>LVDS 4 lane(Default)</td></tr>
</table></td></tr>
<tr><td>HDPOL</td><td>I</td><td>HDPOL sets HSYNC polarity in RGB interface.
<table>
<tr><th>HDPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>HSYNC polarity: positive</td></tr>
<tr><td>H</td><td>HSYNC polarity: negative(Default)</td></tr>
</table>
HDPOL pin should be connected to “H” when it is used in LVDS interface.</td></tr>
<tr><td>DCLKPOL</td><td>I</td><td>DCLKPOL sets DCLK polarity in RGB interface.
<table>
<tr><th>DCLKPOL</th><th>Function Description</th></tr>
<tr><td>L</td><td>DCLK polarity: positive</td></tr>
<tr><td>H</td><td>DCLK polarity: negative(Default)</td></tr>
</table>
DCLKPOL pin should be connected to “H” when it is used in LVDS interface.</td></tr>
<tr><td>LVDS_FMT</td><td>I</td><td>LVDS_FMT sets LVDS data format.
<table>
<tr><th>LVDS_FMT</th><th>Function Description</th></tr>
<tr><td>L</td><td>VESA Mode</td></tr>
<tr><td>H</td><td>JEIDA Mode(Default)</td></tr>
</table>
LVDS_FMT pin should be connected to “L” when it is used in RGB interface.</td></tr>
</table>

<table>
<tr><th colspan="3">Input Interface Pins</th></tr>
<tr><td>DR[7:0]
DG[7:0]
DB[7:0]</td><td>I</td><td>RGB interface and LVDS interface data input pins.
LVDS pin definition. Please refer to LVDS Input Pin Mapping Table.
<table>
<tr><th>MCU Type</th><th colspan="2">Function Description</th></tr>
<tr><td rowspan="3">RGB interface</td><td>DR[7:0]</td><td>8 bit data bus display red data.</td></tr>
<tr><td>DG[7:0]</td><td>8 bit data bus display green data.</td></tr>
<tr><td>DB[7:0]</td><td>8 bit data bus display blue data.</td></tr>
<tr><td rowspan="6">LVDS interface</td><td>DR[7:0]</td><td>DR[7:0] are not used in LVDS mode and should be connected to “L”.</td></tr>
<tr><td>DG[7:0]</td><td>DG[7:0] are not used in LVDS mode and should be connected to “L”.</td></tr>
<tr><td>DB[1:0]</td><td>LVDS input lane: RX0N/ RX0P</td></tr>
<tr><td>DB[3:2]</td><td>LVDS input lane: RX1N/ RX1P</td></tr>
<tr><td>DB[5:4]</td><td>LVDS input lane: RX2N/ RX2P</td></tr>
<tr><td>DB[7:6]</td><td>LVDS input lane: RX3N/ RX3P</td></tr>
</table></td></tr>
<tr><td>DCLKP</td><td>I</td><td>Pixel clock/ RXCLKP control pin, this pin function is selected by INTF.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>Pixel clock input pin</td></tr>
<tr><td>LVDS interface</td><td>RXCLKP control pin. This is LVDS clock input pin, detail pin define please refer to LVDS Input Pin Mapping Table</td></tr>
</table></td></tr>
<tr><td>DCLKN</td><td>I</td><td>RXCLKN control pin, this pin function is selected by INTF.
<table>
<tr><th>MCU Type</th><th>Function Description</th></tr>
<tr><td>RGB interface</td><td>DCLKN is not used in RGB interface and should be connected to “L”.</td></tr>
<tr><td>LVDS interface</td><td>LVDS clock input pin, detail pin define please refer to LVDS Input Pin Mapping Table.</td></tr>
</table></td></tr>
<tr><td>HSYNC</td><td>I</td><td>Horizontal sync signal applied to the RGB interface.
HSYNC pin should be connected to “L” when it is used in LVDS interface.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Vertical sync signal applied to the RGB interface.
VSYNC pin should be connected to “L” when it is used in LVDS interface.</td></tr>
<tr><td>DE</td><td>I</td><td>Data input enable applied to the RGB interface.
DE pin should be connected to “L” when it is used in LVDS interface.</td></tr>
<tr><th colspan="3">Source / Gate Driver Pins</th></tr>
<tr><td>S[1200:1]</td><td>O</td><td>Source driver output signals.</td></tr>
<tr><td>GOR[12:1]
GOL[12:1]</td><td>O</td><td>GIP control signals</td></tr>
</table>

VCOM Generator Pin		
VCOM	C	Power supply for the TFT-LCD common electrode.
Power Supply Pins		
VDD	P	Power supply for analog circuit.
VDDI	P	Power supply for digital I/O pins.
PVDD	P	Power supply for charge pump circuit.
DGND	P	Ground pin for digital circuit.
AGND	P	Ground pin for analog circuit.
RGND	P	Ground pin for reference circuit.
SGND	P	Ground pin for source circuit.
PGND	P	Ground pin for charge pump circuit.
Power Circuit Pins		
SVDD	C	DC/DC converter for positive source OP-AMP driver.
AVDD1	C	DC/DC converter for positive gamma voltage.
SVCL	C	DC/DC converter for negative source OP-AMP driver.
AVCL1	C	DC/DC converter for negative gamma voltage.
VCC	C	Internal digital power.
VGHS	C	Positive power supply for gate driver.
VGL	C	Negative power supply for gate driver.
Test Pins		
GVDD	T	Monitor pin of internal positive grayscale power.
GVCL	T	Monitor pin of internal negative grayscale power.
VGSP	T	Monitor pin of internal VCOM offset.
VPP	T	Reserved for test only, please leave it open.
EXT_G	T	Reserved for test only, please connect to “L”.
TESTI[14:0]	T	Reserved for test only, please leave those pins open.
TESTOUT[13:0]	T	Reserved for test only, please leave those pins open.
DUMMY	D	Dummy pin, please leave those pins open.

Note: 1. I: input, O: output, I/O: input/output, P: power input, PO: power out, D: dummy, T: test pin, C: capacitor pin

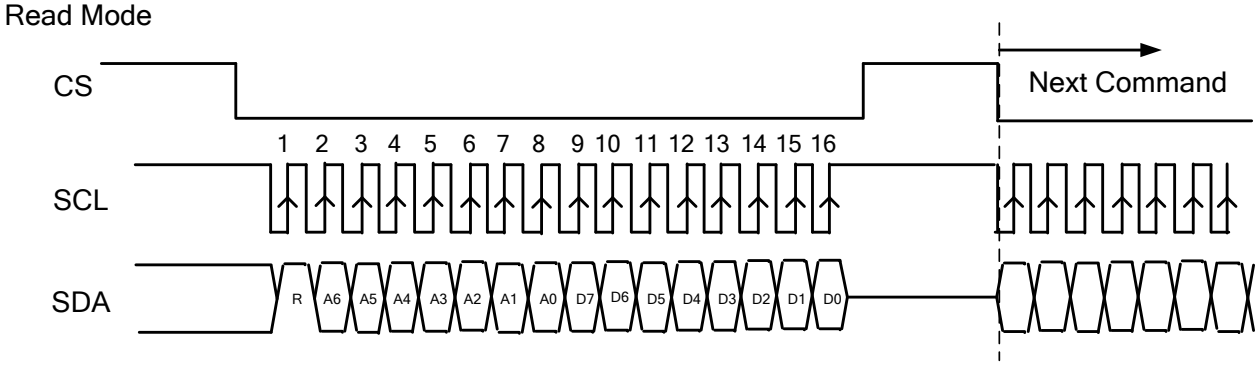
2. If hardware pin is not used, please fix to “H” by VDDI or “L” by DGND

6. COMMUNICATION INTERFACE

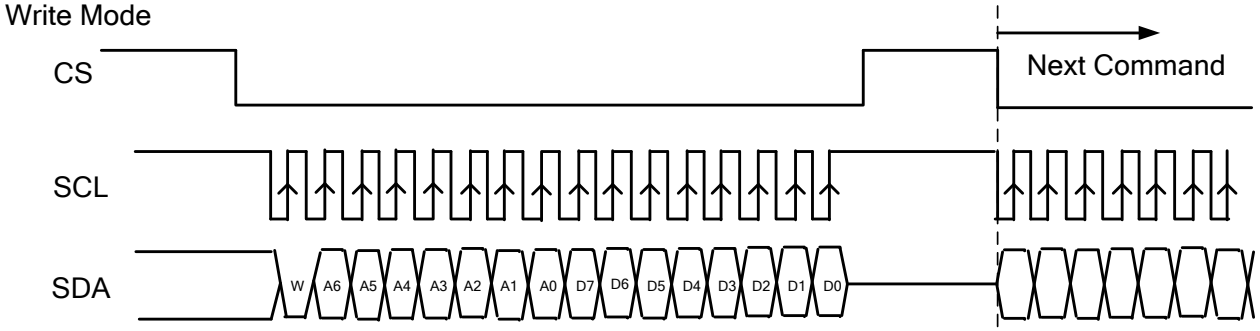
6.1 3-wire Serial Interface

R/W: Read/Write mode control bit.
R/W=1: Read mode
R/W=0: Write mode

Read Mode



Write Mode



a. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.

b. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.

c. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.

d. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.

e. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data before then rising edge of CS pulse are valid data.

f. Serial block operates with the SCL clock

g. Serial data can be accepted in the power save mode.

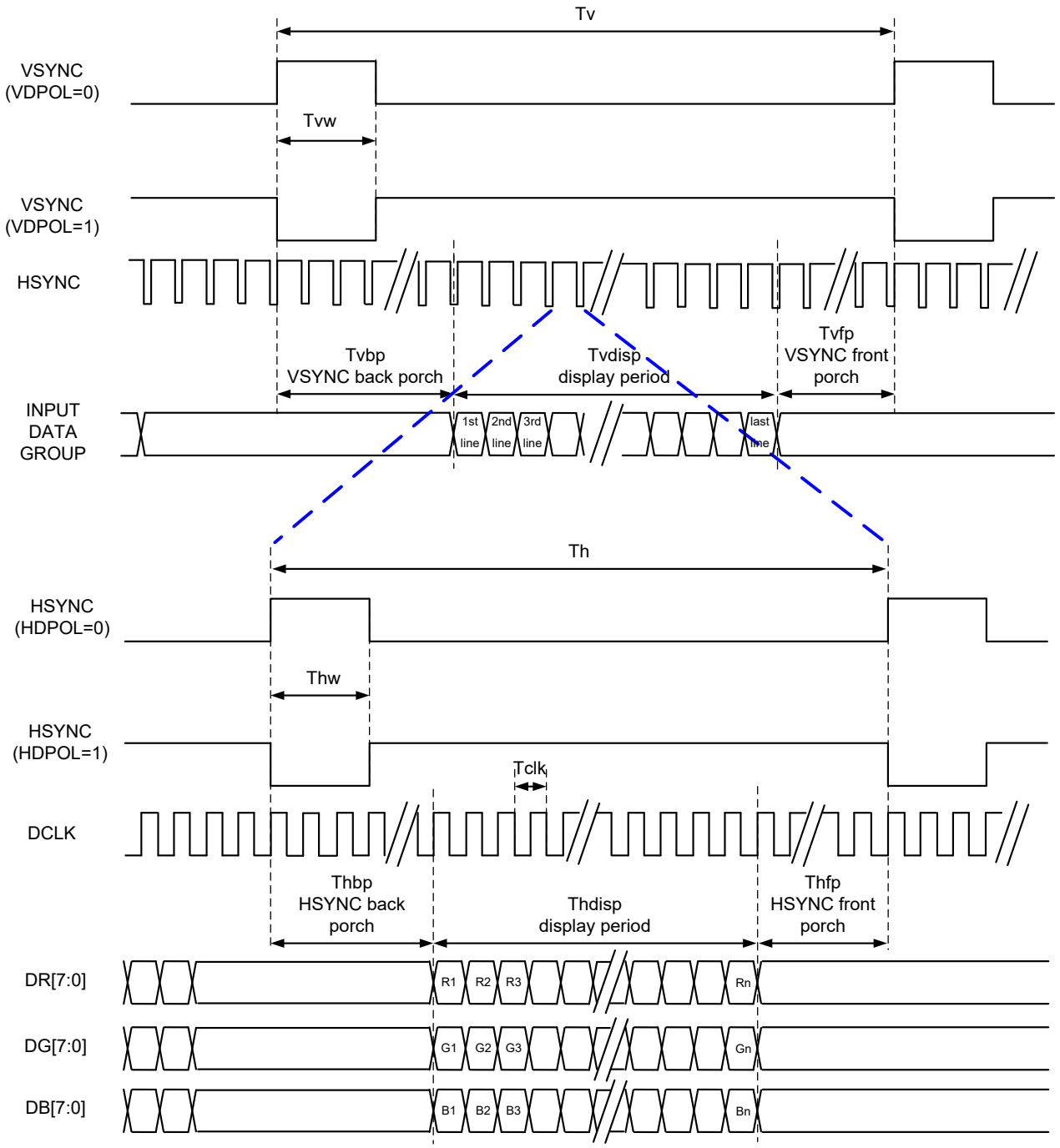
h. After power on reset or GRB reset, it is required 100ms delay to begin SPI communication.

6.2 RGB Interface

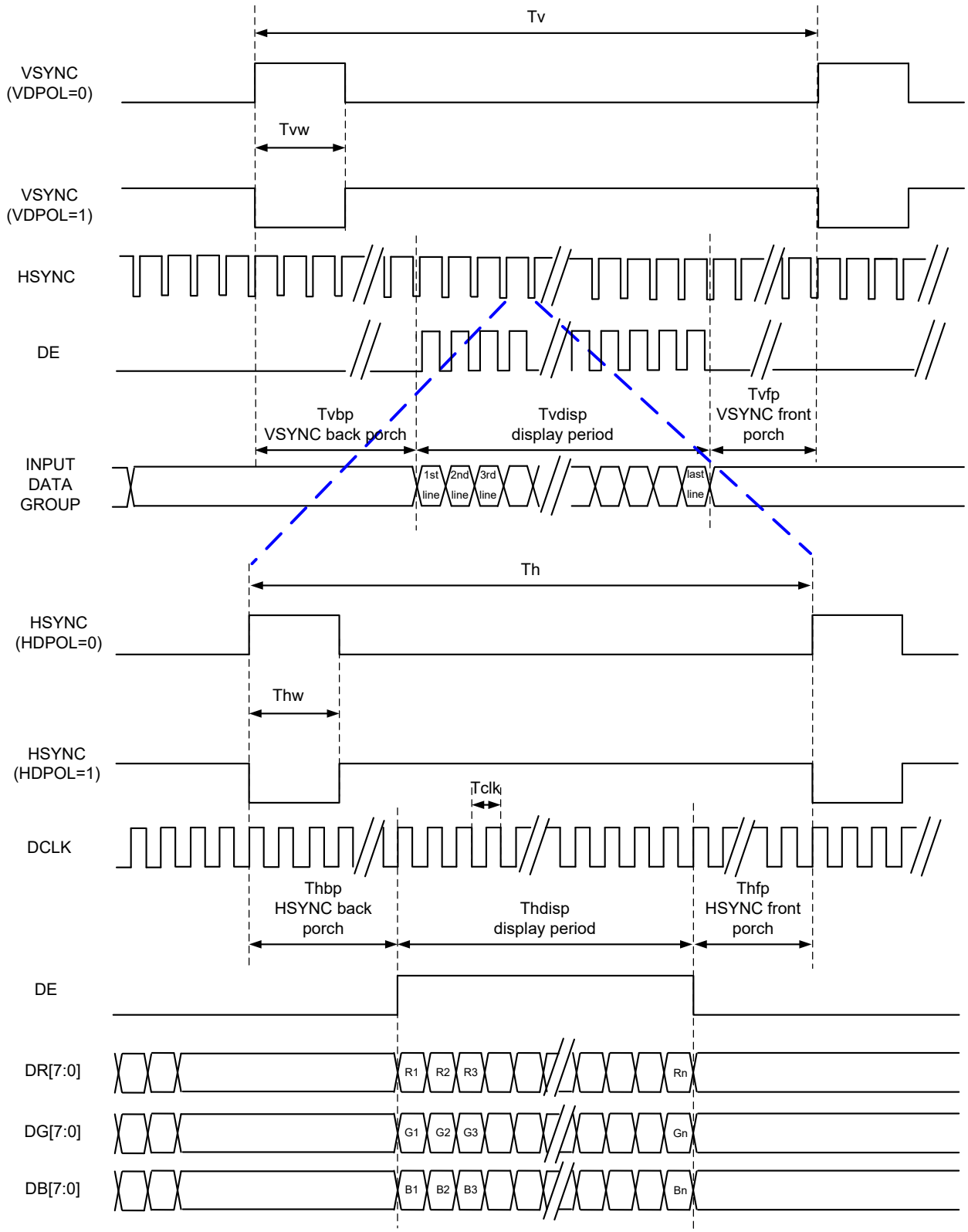
RGB Mode Selection Table	DCLK	HSYNC	VSYNC	DE
SYNC - DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

Note: "Input" means these signals are driven by host side

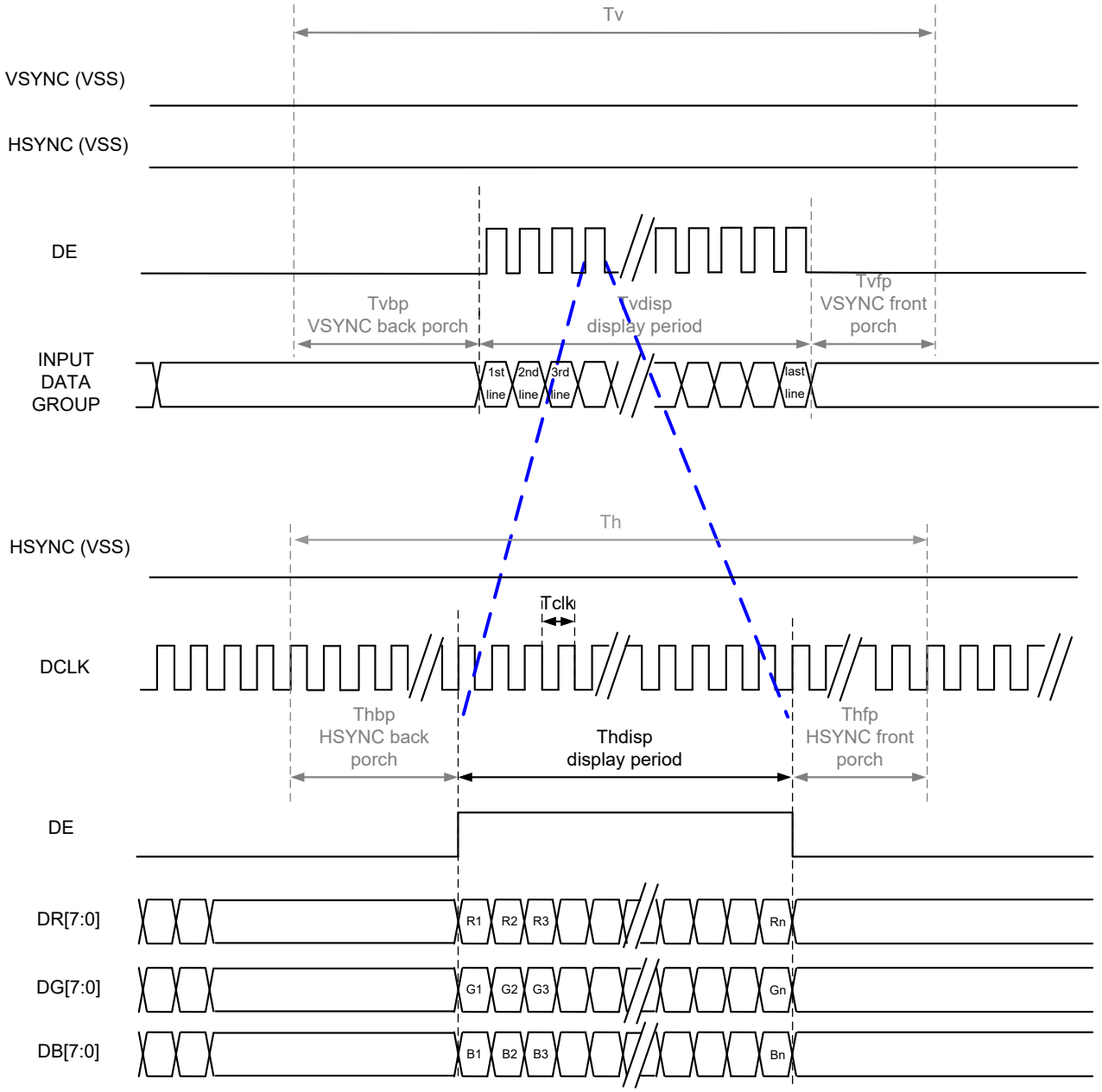
6.2.1 SYNC Mode



6.2.2 SYNC-DE Mode



6.2.3 DE Mode


Tv
VSYNC (VSS)
HSYNC (VSS)
DE
Tvbp
VSYNC back porch
Tvdisp
display period
Tvfp
VSYNC front
porch
INPUT
DATA
GROUP
1st
line
2nd
line
3rd
line
last
line
Th
HSYNC (VSS)
Tclk
DCLK
Thbp
HSYNC back
porch
Thdisp
display period
Thfp
HSYNC front
porch
DE
DR[7:0]
R1
R2
R3
Rn
DG[7:0]
G1
G2
G3
Gn
DB[7:0]
B1
B2
B3
Bn

6.2.4 Parallel 24-bit RGB Input Timing Table

Parallel 24-bit RGB Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Parallel 24-bit RGB Interface Timing Table							
Item		**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Remark**
DCLK Frequency		Fclk	23	25	27	MHz	.
HSYNC	Period Time	Th	808	816	848	DCLK	
	Display Period	Thdisp		800		DCLK	
	Back Porch	Thbp	4	8	24	DCLK	
	Front Porch	Thfp	4	8	24	DCLK	
	Pulse Width	Thw	2	4	8	DCLK	
VSYNC	Period Time	Tv	496	512	528	HSYNC	
	Display Period	Tvdisp		480		HSYNC	
	Back Porch	Tvbp	8	16	24	HSYNC	
	Front Porch	Tvfp	8	16	24	HSYNC	
	Pulse Width	Tvw	2	4	8	HSYNC	

Note: 1. The minimum blanking time depends on the GIP timing of the panel specification

2. To ensure the compatibility of different panels, it is recommended to use the typical setting.

3. It is necessary to keep Tvbp =16 and Thbp =8 in sync mode. DE mode is unnecessary to keep it.

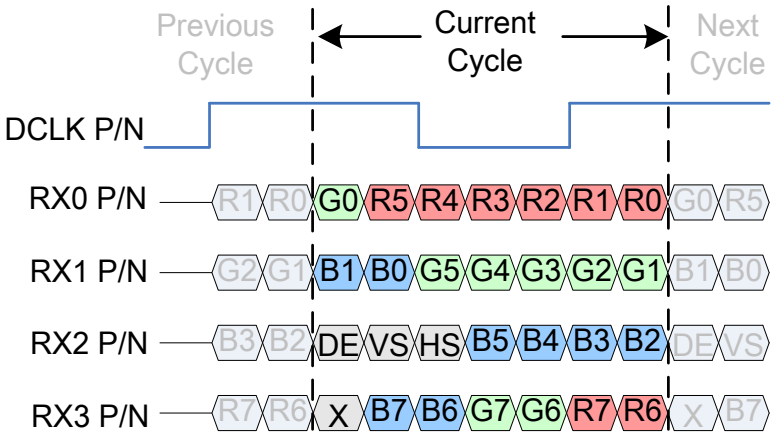
6.3 LVDS Interface

6.3.1 LVDS Input Pin Mapping Table

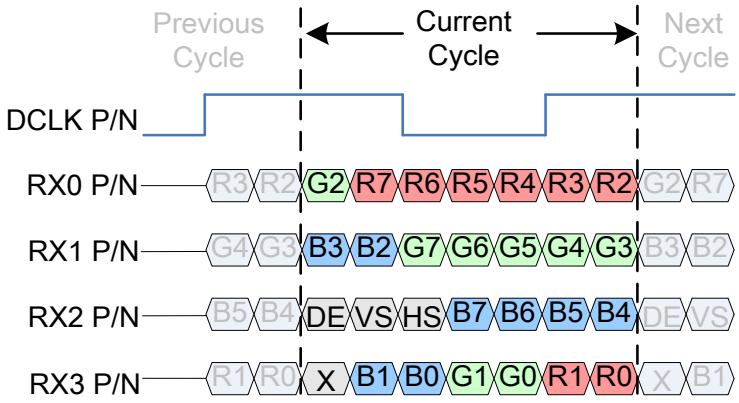
Pin Name RGB (LVDS)	LVDS 3 lane	LVDS 4 Lane
DCLKN	RXCLKN	RXCLKN
DCLKP	RXCLKP	RXCLKP
DB0	RX0P	RX0P
DB1	RX0N	RX0N
DB2	RX1P	RX1P
DB3	RX1N	RX1N
DB4	RX2P	RX2P
DB5	RX2N	RX2N
DB6	-	RX3P
DB7	-	RX3N

Note: Symbol "-" means reserve pin and should fix to "L" by DGND.

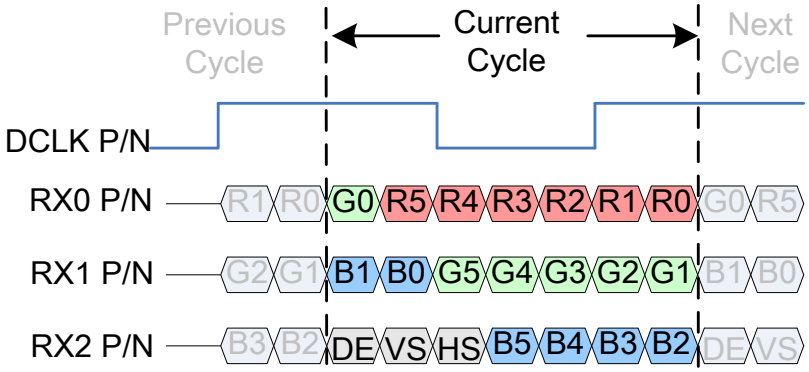
6.3.2 4 Lane VESA Data Format Color Bit Map



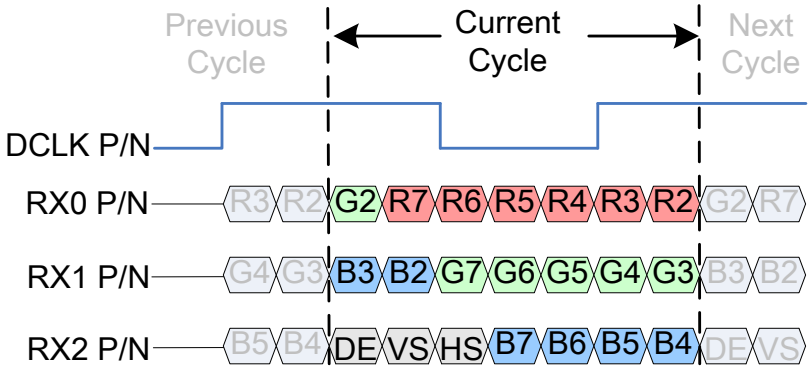
6.3.3 4 Lane JEIDA Data Format Color Bit Map



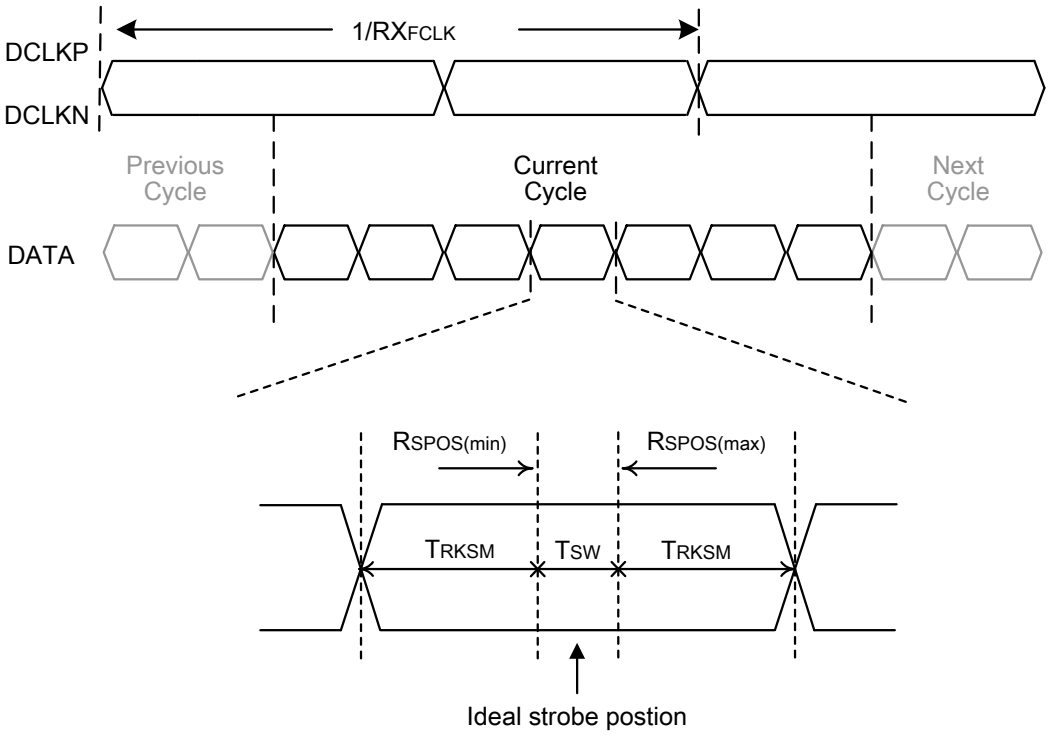
6.3.4 3 Lane VESA Mode Color Bit Map



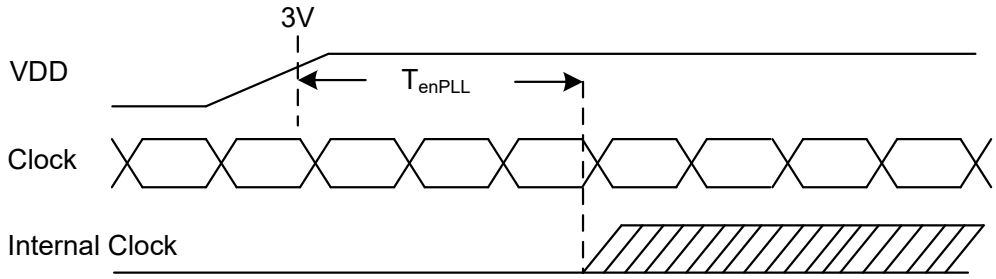
6.3.5 3 Lane JEIDA Mode Color Bit Map



6.3.6 LVDS Input Timing Table



RRKSM : Receiver strobe margin
RSPOS : Receiver strobe position
TSW : Strobe width (internal DATA sampling window)



LVDS Input Timing (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	RX_{FCLK}	23	25	30	MHz	
Input Data Skew Margin	T_{RKSM}	400	-	-	ps	
Clock High Time	T_{LVCH}	4/(7 x RX_{FCLK})			ns	
Clock Low Time	T_{LVCL}	3/(7 x RX_{FCLK})			ns	
PLL Wake-up Time	T_{enPLL}	-	-	150	us	
LVDS Spread Spectrum Clocking (SSC) Tolerance of LVDS Receiver						
Modulation Frequency	SSC_{MF}	-	-	100	KHz	
Modulation Rate	SSC_{MR}	-	-	+/-3	%	

7. REGISTER LIST

7.1 Register Summary

COMMAND TABLE1										
Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	W	0	0	0	0	GRB	0	0	DISP	08h
11h	W	CONTRAST[7:0]								40h
12h	W	0	SUB_CONTRAST_R[6:0]							40h
13h	W	0	SUB_CONTRAST_B[6:0]							40h
14h	W	BRIGHTNESS[7:0]								40h
15h	W	0	SUB_BRIGHTNESS_R[6:0]							40h
16h	W	0	SUB_BRIGHTNESS_B[6:0]							40h
17h	W	H_BLANKING[7:0]								08h
18h	W	V_BLANKING[7:0]								10h
1Ch	W	0	0	0	0	0	AUTODL	0	0	--
COMMAND TABLE2										
Address	Type	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	VRHP[6:0]							--
41h	R/W	0	VRHN[6:0]							--
45h	R/W	VGL[2:0]			1	VGHS[2:0]			1	--

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

GAMMA COMMAND TABLE										
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	R/W	0	RATIO1[1:0]		VRF0P[4:0]					--
21h	R/W	0	PFP6[3]	PFP0[3]	VOS0P[4:0]					--
22h	R/W	PFP0[2:0]			PKP0[4:0]					--
23h	R/W	PFP1[2:0]			PKP1[4:0]					--
24h	R/W	PFP2[2:0]			PKP2[4:0]					--
25h	R/W	PFP3[2:0]			PKP3[4:0]					--
26h	R/W	PFP4[2:0]			PKP4[4:0]					--
27h	R/W	PFP5[2:0]			PKP5[4:0]					--
28h	R/W	PFP6[2:0]			PKP6[4:0]					--
29h	R/W	0	0	0	PKP7[4:0]					--
30h	R/W	0	RATIO2[1:0]		VRF0N[4:0]					--
31h	R/W	0	PFN6[3]	PFN0[3]	VOS0N[4:0]					--
32h	R/W	PFN0[2:0]			PKN0[4:0]					--
33h	R/W	PFN1[2:0]			PKN1[4:0]					--
34h	R/W	PFN2[2:0]			PKN2[4:0]					--
35h	R/W	PFN3[2:0]			PKN3[4:0]					--
36h	R/W	PFN4[2:0]			PKN4[4:0]					--
37h	R/W	PFN5[2:0]			PKN5[4:0]					--
38h	R/W	PFN6[2:0]			PKN6[4:0]					--
39h	R/W	0	0	0	PKN7[4:0]					--

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

OTP COMMAND TABLE										
Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--
02h	R/W	0	ID2[6:0]							--
03h	R/W	0	ID3[6:0]							--
05h	R/W	0	VMF[6:0]							40h
60h	W	0	1	0	0	0	1	OTPEN	0	44h
65h	W	OTPACK[7:0]								00h
68h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			--
69h	R	0	0	0	0	0	ID2 OTP TIME[2:0]			--
6Ah	R	0	0	0	0	0	ID3 OTP TIME[2:0]			--
6Ch	R	0	0	0	0	0	VMF OTP TIME[2:0]			--

Note: 1. When GRB is "Low", all registers reset to default values.

2. Symbol "--" means this value is OTP setting according to parameters of system application, panel loading and display quality.

3. Do not use instructions not listed in these tables.

7.2 Command Table1 Register Description

7.2.1 GRB、DISP CONTROL (10h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	W	0	0	0	0	GRB	0	0	DISP	08h

Designation	Description
GRB	Reset register setting GRB=0: reset all registers to default value GRB=1: normal operation
DISP	Display on/off control DISP=0: standby mode DISP=1: normal mode

7.2.2 CONTRAST (11h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
11h	W	CONTRAST[7:0]								40h

Designation	Description
CONTRAST[7:0]	Set RGB contrast level, the range of gain is 0~3.984 CONTRAST=00h: contrast gain=0 CONTRAST=40h: contrast gain=1 CONTRAST=FFh: contrast gain=3.984

7.2.3 SUB_CONTRAST_R (12h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	W	0	SUB_CONTRAST_R[6:0]							40h

Designation	Description
SUB_CONTRAST_R[6:0]	Set red color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_R=00h: contrast gain=0.75 SUB_CONTRAST_R=40h: contrast gain=1 SUB_CONTRAST_R=7Fh: contrast gain=1.246

7.2.4 SUB_CONTRAST_B (13h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
13h	W	0	SUB_CONTRAST_B[6:0]							40h

Designation	Description
SUB_CONTRAST_B[6:0]	Set blue color sub-contrast level, the range of gain is 0.75~1.246 SUB_CONTRAST_B=00h: contrast gain=0.75 SUB_CONTRAST_B=40h: contrast gain=1 SUB_CONTRAST_B=7Fh: contrast gain=1.246

7.2.5 BRIGHTNESS (14h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	W	BRIGHTNESS[7:0]								40h

Designation	Description
BRIGHTNESS[7:0]	Set RGB brightness level, the range of brightness is -64~+191 BRIGHTNESS=00h: -64 BRIGHTNESS=40h: 0 BRIGHTNESS=FFh: +191

7.2.6 SUB-BRIGHTNESS_R (15h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
15h	W	0	SUB_BRIGHTNESS_R[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_R [6:0]	Set red color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_R=00h: -64 SUB_BRIGHTNESS_R=40h: 0 SUB_BRIGHTNESS_R=7Fh: +63

7.2.7 SUB-BRIGHTNESS_B (16h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	W	0	SUB_BRIGHTNESS_B[6:0]							40h

Designation	Description
SUB_BRIGHTNESS_B [6:0]	Set blue color sub-brightness level, the range of brightness is -64~+63 SUB_BRIGHTNESS_B=00h: -64 SUB_BRIGHTNESS_B=40h: 0 SUB_BRIGHTNESS_B=7Fh: +63

7.2.8 H_BLANKING (17h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
17h	W	H_BLANKING[7:0]								08h

Designation	Description
H_BLANKING[7:0]	The HSYNC back porch setting of RGB interface

7.2.9 V_BLANKING (18h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	W	V_BLANKING[7:0]								10h

Designation	Description
V_BLANKING[7:0]	The VSYNC back porch setting of RGB interface

7.2.10 OTP AUTO DOWNLOAD CONTROL (1Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	W	0	0	0	0	0	AUTODL	0	0	--

Designation	Description
AUTODL	OTP auto-refresh function control AUTODL= 0: disable auto-refresh function AUTODL= 1: enable auto-refresh function

7.3 Command Table2 Register Description

7.3.1 GVDD SETTING (40h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	R/W	0	VRHP[6:0]							--

Designation	Description
VRHP[6:0]	GVDD level setting

VRHP[6:0]	GVDD	VRHP[6:0]	GVDD	VRHP[6:0]	GVDD	VRHP[6:0]	GVDD
10h	6.0000	2Ch	5.6500	48h	5.3000	64h	4.9500
11h	5.9875	2Dh	5.6375	49h	5.2875	65h	4.9375
12h	5.9750	2Eh	5.6250	4Ah	5.2750	66h	4.9250
13h	5.9625	2Fh	5.6125	4Bh	5.2625	67h	4.9125
14h	5.9500	30h	5.6000	4Ch	5.2500	68h	4.9000
15h	5.9375	31h	5.5875	4Dh	5.2375	69h	4.8875
16h	5.9250	32h	5.5750	4Eh	5.2250	6Ah	4.8750
17h	5.9125	33h	5.5625	4Fh	5.2125	6Bh	4.8625
18h	5.9000	34h	5.5500	50h	5.2000	6Ch	4.8500
19h	5.8875	35h	5.5375	51h	5.1875	6Dh	4.8375
1Ah	5.8750	36h	5.5250	52h	5.1750	6Eh	4.8250
1Bh	5.8625	37h	5.5125	53h	5.1625	6Fh	4.8125
1Ch	5.8500	38h	5.5000	54h	5.1500	70h	4.8000
1Dh	5.8375	39h	5.4875	55h	5.1375	71h	4.7875
1Eh	5.8250	3Ah	5.4750	56h	5.1250	72h	4.7750
1Fh	5.8125	3Bh	5.4625	57h	5.1125	73h	4.7625
20h	5.8000	3Ch	5.4500	58h	5.1000	74h	4.7500
21h	5.7875	3Dh	5.4375	59h	5.0875	75h	4.7375
22h	5.7750	3Eh	5.4250	5Ah	5.0750	76h	4.7250
23h	5.7625	3Fh	5.4125	5Bh	5.0625	77h	4.7125
24h	5.7500	40h	5.4000	5Ch	5.0500	78h	4.7000
25h	5.7375	41h	5.3875	5Dh	5.0375	79h	4.6875
26h	5.7250	42h	5.3750	5Eh	5.0250	7Ah	4.6750
27h	5.7125	43h	5.3625	5Fh	5.0125	7Bh	4.6625
28h	5.7000	44h	5.3500	60h	5.0000	7Ch	4.6500
29h	5.6875	45h	5.3375	61h	4.9875	7Dh	4.6375
2Ah	5.6750	46h	5.3250	62h	4.9750	7Eh	4.6250
2Bh	5.6625	47h	5.3125	63h	4.9625	7Fh	4.6125

Note. Do not use register values not listed in the table

7.3.2 GVCL SETTING (41h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
41h	R/W	0	VRHN[6:0]							--

Designation	Description
VRHN[6:0]	GVCL level setting

VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL	VRHN[6:0]	GVCL
10h	-4.4000	2Ch	-4.0500	48h	-3.7000	64h	-3.3500
11h	-4.3875	2Dh	-4.0375	49h	-3.6875	65h	-3.3375
12h	-4.3750	2Eh	-4.0250	4Ah	-3.6750	66h	-3.3250
13h	-4.3625	2Fh	-4.0125	4Bh	-3.6625	67h	-3.3125
14h	-4.3500	30h	-4.0000	4Ch	-3.6500	68h	-3.3000
15h	-4.3375	31h	-3.9875	4Dh	-3.6375	69h	-3.2875
16h	-4.3250	32h	-3.9750	4Eh	-3.6250	6Ah	-3.2750
17h	-4.3125	33h	-3.9625	4Fh	-3.6125	6Bh	-3.2625
18h	-4.3000	34h	-3.9500	50h	-3.6000	6Ch	-3.2500
19h	-4.2875	35h	-3.9375	51h	-3.5875	6Dh	-3.2375
1Ah	-4.2750	36h	-3.9250	52h	-3.5750	6Eh	-3.2250
1Bh	-4.2625	37h	-3.9125	53h	-3.5625	6Fh	-3.2125
1Ch	-4.2500	38h	-3.9000	54h	-3.5500	70h	-3.2000
1Dh	-4.2375	39h	-3.8875	55h	-3.5375	71h	-3.1875
1Eh	-4.2250	3Ah	-3.8750	56h	-3.5250	72h	-3.1750
1Fh	-4.2125	3Bh	-3.8625	57h	-3.5125	73h	-3.1625
20h	-4.2000	3Ch	-3.8500	58h	-3.5000	74h	-3.1500
21h	-4.1875	3Dh	-3.8375	59h	-3.4875	75h	-3.1375
22h	-4.1750	3Eh	-3.8250	5Ah	-3.4750	76h	-3.1250
23h	-4.1625	3Fh	-3.8125	5Bh	-3.4625	77h	-3.1125
24h	-4.1500	40h	-3.8000	5Ch	-3.4500	78h	-3.1000
25h	-4.1375	41h	-3.7875	5Dh	-3.4375	79h	-3.0875
26h	-4.1250	42h	-3.7750	5Eh	-3.4250	7Ah	-3.0750
27h	-4.1125	43h	-3.7625	5Fh	-3.4125	7Bh	-3.0625
28h	-4.1000	44h	-3.7500	60h	-3.4000	7Ch	-3.0500
29h	-4.0875	45h	-3.7375	61h	-3.3875	7Dh	-3.0375
2Ah	-4.0750	46h	-3.7250	62h	-3.3750	7Eh	-3.0250
2Bh	-4.0625	47h	-3.7125	63h	-3.3625	7Fh	-3.0125

Note. Do not use register values not listed in the table

7.3.3 VGHS, VGL SETTING (45h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
45h	R/W	VGL[2:0]			1	VGHS[2:0]			1	--

Designation	Description
VGL[2:0]	VGL level setting VGL[2:0] / VGL (V) 000 / -7.5 001 / -8.5 010 / -9.5 011 / -10.5 100 / -11 101 / -11.5
VGHS[2:0]	VGHS level setting VGHS[2:0] / VGHS (V) 000 / 9 001 / 11 010 / 13 011 / 15 100 / 17

7.4 Gamma Table Register Description

7.4.1 GAMMA SETTING (20h~29h, 30h~39h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	R/W	0	RATIO1[1:0]		VRFP0P[4:0]					--
21h	R/W	0	PFP6[3]	PFP0[3]	VOS0P[4:0]					--
22h	R/W	PFP0[2:0]			PKP0[4:0]					--
23h	R/W	PFP1[2:0]			PKP1[4:0]					--
24h	R/W	PFP2[2:0]			PKP2[4:0]					--
25h	R/W	PFP3[2:0]			PKP3[4:0]					--
26h	R/W	PFP4[2:0]			PKP4[4:0]					--
27h	R/W	PFP5[2:0]			PKP5[4:0]					--
28h	R/W	PFP6[2:0]			PKP6[4:0]					--
29h	R/W	0	0	0	PKP7[4:0]					--
30h	R/W	0	RATIO2[1:0]		VRFP0N[4:0]					--
31h	R/W	0	PFN6[3]	PFN0[3]	VOS0N[4:0]					--
32h	R/W	PFN0[2:0]			PKN0[4:0]					--
33h	R/W	PFN1[2:0]			PKN1[4:0]					--
34h	R/W	PFN2[2:0]			PKN2[4:0]					--
35h	R/W	PFN3[2:0]			PKN3[4:0]					--
36h	R/W	PFN4[2:0]			PKN4[4:0]					--
37h	R/W	PFN5[2:0]			PKN5[4:0]					--
38h	R/W	PFN6[2:0]			PKN6[4:0]					--
39h	R/W	0	0	0	PKN7[4:0]					--

Designation	Description
PKP0[4:0]	V16 gamma selection
PKN0[4:0]	
PKP1[4:0]	V32 gamma selection
PKN1[4:0]	
PKP2[4:0]	V48 gamma selection
PKN2[4:0]	
PKP3[4:0]	V80 gamma selection
PKN3[4:0]	
PKP4[4:0]	V176 gamma selection
PKN4[4:0]	
PKP5[4:0]	V208 gamma selection
PKN5[4:0]	
PKP6[4:0]	V224 gamma selection
PKN6[4:0]	

PKP7[4:0]	V240 gamma selection
PKN7[4:0]	
VRF0P[4:0]	V8 gamma selection
VRF0N[4:0]	
VOS0P[4:0]	V248 gamma selection
VOS0N[4:0]	
PFP0[3:0]	V12 gamma selection
PFN0[3:0]	
PFP1[2:0]	V64 gamma selection
PFN1[2:0]	
PFP2[2:0]	V104 gamma selection
PFN2[2:0]	
PFP3[2:0]	V128 gamma selection
PFN3[2:0]	
PFP4[2:0]	V152 gamma selection
PFN4[2:0]	
PFP5[2:0]	V192 gamma selection
PFN5[2:0]	
PFP6[3:0]	V244 gamma selection
PFN6[3:0]	
RATIO1[1:0]	V0-V8 gamma ratio selection
RATIO2[1:0]	V248-V255 gamma ratio selection

7.5 OTP Table Register Description

7.5.1 ID1 SETTING (01h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	R/W	0	ID1[6:0]							--

Designation	Description
ID1[6:0]	Built-in OTP for ID1 setting.

7.5.2 ID2 SETTING (02h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	R/W	0	ID2[6:0]							--

Designation	Description
ID2[6:0]	Built-in OTP for ID2 setting.

7.5.3 ID3 SETTING (03h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
03h	R/W	0	ID3[6:0]							--

Designation	Description
ID3[6:0]	Built-in OTP for ID3 setting.

7.5.4 VCOM OFFSET SETTING (05h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
05h	R/W	0	VMF[6:0]							40h

Designation	Description
VMF[6:0]	VCOM offset setting

VMF[6]	VMF[5:0]	VCOM”	GVDD	GVCL
0	000000	VCOM+64d	VRHP[6:0]+64d	VRHN[6:0]+64d
0	000001	VCOM+63d	VRHP[6:0]+63d	VRHN[6:0]+63d
0	000010	VCOM+62d	VRHP[6:0]+62d	VRHN[6:0]+62d
0	|	|	|	|
0	111110	VCOM+2d	VRHP[6:0]+2d	VRHN[6:0]+2d
0	111111	VCOM+1d	VRHP[6:0]+1d	VRHN[6:0]+1d
1	000000	VCOM+0d	VRHP[6:0]	VRHN[6:0]
1	000001	VCOM-1d	VRHP[6:0]-1d	VRHN[6:0]-1d
1	000010	VCOM-2d	VRHP[6:0]-2d	VRHN[6:0]-2d
1	|	|	|	|

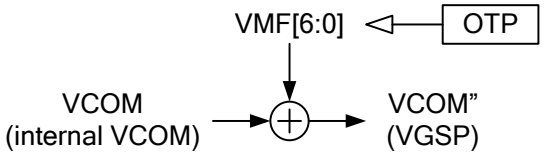
1	111110	VCOM-62d	VRHP[6:0]-62d	VRHN[6:0]-62d
1	111111	VCOM-63d	VRHP[6:0]-63d	VRHN[6:0]-63d

Note: 1.d=12.5mV

2. Adjustable VCOM offset (OTP) can be used to compensate feedthrough tolerance and its limitation couldn't exceed the maximum voltage range of GVDD and GVCL.

3. VCOM" ≤ GVDD-Vop = GVCL+Vop

Vop is the operation voltage of liquid crystal.



7.5.5 OTP FUNCTION CONTROL (60h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	W	0	1	0	0	0	1	OTPEN	0	44h

Designation	Description
OTPEN	OTP programming function control OTPEN = 0: disable OTP programming function OTPEN = 1: enable OTP programming function

7.5.6 OTP ACKNOWLEDGEMENT CONTROL (65h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
65h	W	OTPACK[7:0]								00h

Designation	Description
OTPACK[7:0]	OTP active selection

OTPACK[7:0]	Description
31h	ID1 program
32h	ID2 program
33h	ID3 program
3Ah	VCOM offset program

7.5.7 ID1 PROGRAM TIMES (68h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	R	0	0	0	0	0	ID1 OTP TIME[2:0]			--

Designation	Description
ID1 OTP TIME[2:0]	Read ID1 remaining programmable times

7.5.8 ID2 PROGRAM TIMES (69h)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
69h	R	0	0	0	0	0	ID2 OTP TIME[2:0]			--

Designation	Description
ID2 OTP TIME[2:0]	Read ID2 remaining programmable times

7.5.9 ID3 PROGRAM TIMES (6Ah)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ah	R	0	0	0	0	0	ID3 OTP TIME[2:0]			--

Designation	Description
ID3 OTP TIME[2:0]	Read ID3 remaining programmable times

7.5.10 VCOM OFFEST PROGRAM TIMES (6Ch)

Address	TYPE	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	R	0	0	0	0	0	VMF OTP TIME[2:0]			--

Designation	Description
VMF OTP TIME[2:0]	Read VMF remaining programmable times

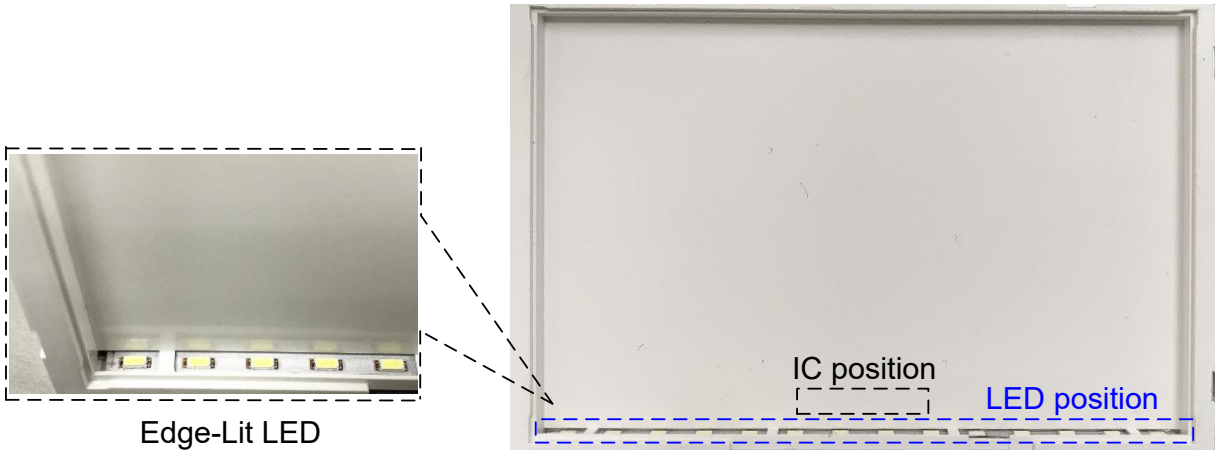
8. ELECTRICAL SPECIFICATIONS

8.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage	VDD	- 0.3 ~ +4.0	V
IO Supply Voltage	VDDI	- 0.3 ~ +4.0	V
Charge Pump Supply Voltage	PVDD	- 0.3 ~ +4.0	V
Logic Input Voltage Range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output Voltage Range	VOUT	-0.3 ~ VDDI + 0.3	V
Driver Supply Voltage	VGHS-VGL	- 0.3 ~ +30.0	V
Operating Temperature Range	TOPR	-30 ~ +85	℃
Storage Temperature Range	TSTG	-40 ~ +125	℃

Note:

1. *That the stress exceeds the Limiting Value listed above it may cause the driver IC permanent damage. These values are for stress only. IC should be operated under the DC/AC Characteristic conditions for normal operation. If these conditions are not met, IC operation may be error and the reliability may be deteriorated.*
2. *Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.*
3. *Insure the voltage levels of VDDI, VDD, PVDD always matches the correct relation:*
   3.1V ≦ VDDI ≦ VDD = PVDD ≦ 3.6V
4. *VIN should be less than or equal to 3.6V. (VIN ≤ 3.6V)*
5. *Panel display quality depends on panel loading, and it may have the different performance at low/high temperature.*
6. *When the backlight LED is turned on which is the heat generation leads to the increasing temperature of the LCD module.*
   In order to protect the LCD driver IC against thermal effect, we advise that the positon of backlight LED should not be close to the driver IC. The edge-lit type LED is recommended.



8.2 DC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

8.2.1 Recommended Operating Range

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
IO Supply Voltage	VDDI	3.1	3.3	3.6	V	
Analog Supply Voltage	VDD	3.1	3.3	3.6	V	
Charge Pump Supply Voltage	PVDD	3.1	3.3	3.6	V	

8.2.2 DC Characteristics for Digital Circuit

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic-High Input Voltage	Vih	0.7VDDI	-	VDDI	V	
Logic-Low Input Voltage	Vil	DGND	-	0.3VDDI	V	
Logic-High Output Voltage	Voh	VDDI-0.4	-	VDDI	V	
Logic-Low Output Voltage	Vol	DGND	-	DGND+0.4	V	

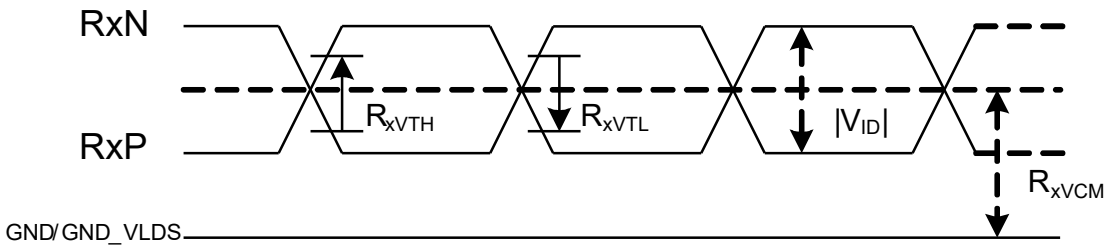
8.2.3 DC Characteristics for Analog Circuit

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

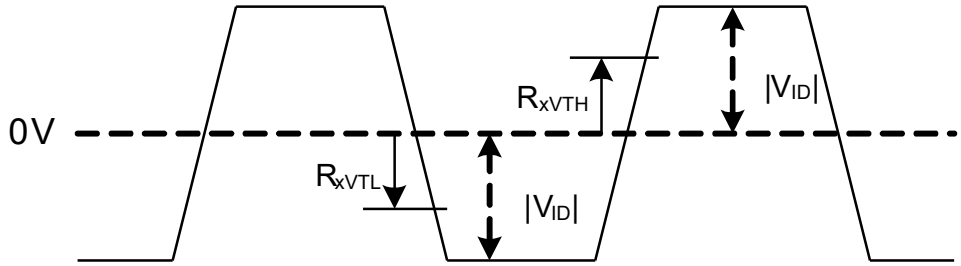
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Positive High-Voltage Power	VGHS	9	15	17	V	No Load@ FR=60Hz
Negative High-Voltage Power	VGL	-11.5	-10.5	-7.5	V	
Output Voltage Deviation	Vod	-	±40	±50	mV	
Standby Current	Isc	-	-	50	uA	
Operation Current	Ioc	-	40	-	mA	

8.2.4 DC Characteristics for LVDS Receiver Circuit

Single End Signals



Differential Signals



DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold Voltage	R_{xVTH}	-	-	0.1	V	R_{xVCM} = 1.2V
Differential Input Low Threshold Voltage	R_{xVTL}	-0.1	-	-	V	
Input Voltage Range (Singled-End)	R_{xVIN}	0	-	VDD-1.0	V	
Differential Input Common Mode Voltage	R_{xVCM}	$\lvert V_{ID} \rvert /2$	-	$2.4-\lvert V_{ID} \rvert /2$	V	
Differential Input Voltage	$\lvert V_{ID} \rvert$	0.2	-	0.6	V	
Differential Input Leakage Current	RV_{xliz}	-10	-	10	uA	
LVDS Digital Operating Current	I_{VDD_LVDS}	-	10	15	mA	
LVDS Digital Stand-by Current	I_{STBD_LVDS}	-	10	50	uA	
Differential Input Termination Resistance	R_{ID}	-	100	-	Ω	

8.3 AC Characteristics

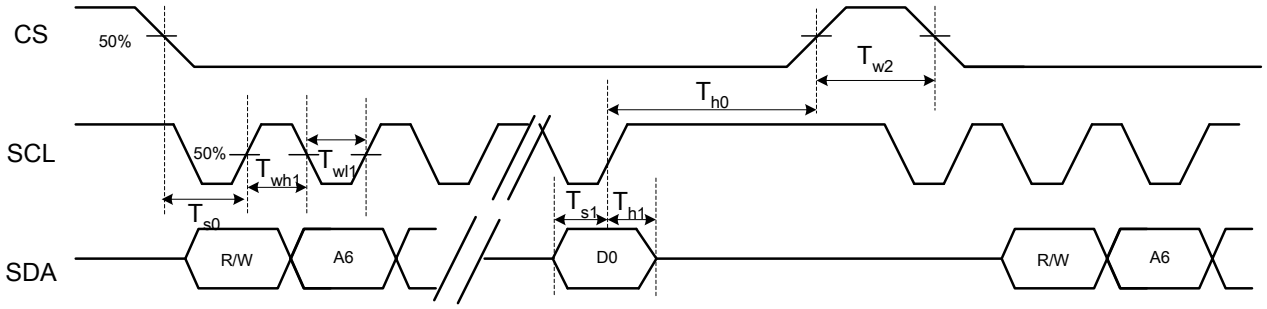
AC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

8.3.1 System Operation AC Characteristics

DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
VDD Power Source Slew Time	TPOR	-	-	20	ms	From 0V to 99% VDD
GRB Pulse Width	tRSTW	10	50	-	us	R=10Kohm, C=1uF
SD Output Stable Time	Tst	-	-	12	us	Output settled within +20mV Loading = 6.8k+28.2pF.
GD Output Rise and Fall Time	Tgst	-	-	6	us	Output settled (5%~95%), Loading = 4.7k+29.8pF

8.3.2 System Bus Timing for 3-Wire SPI Interface

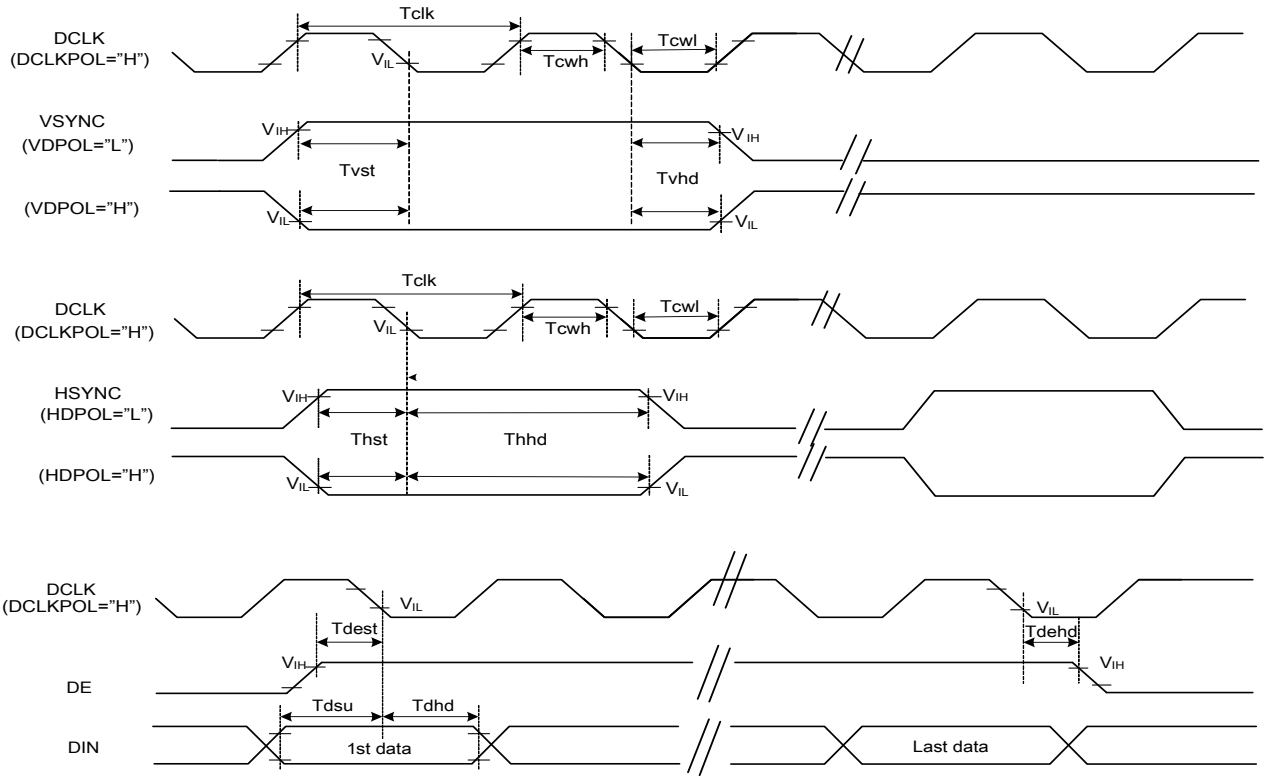


DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

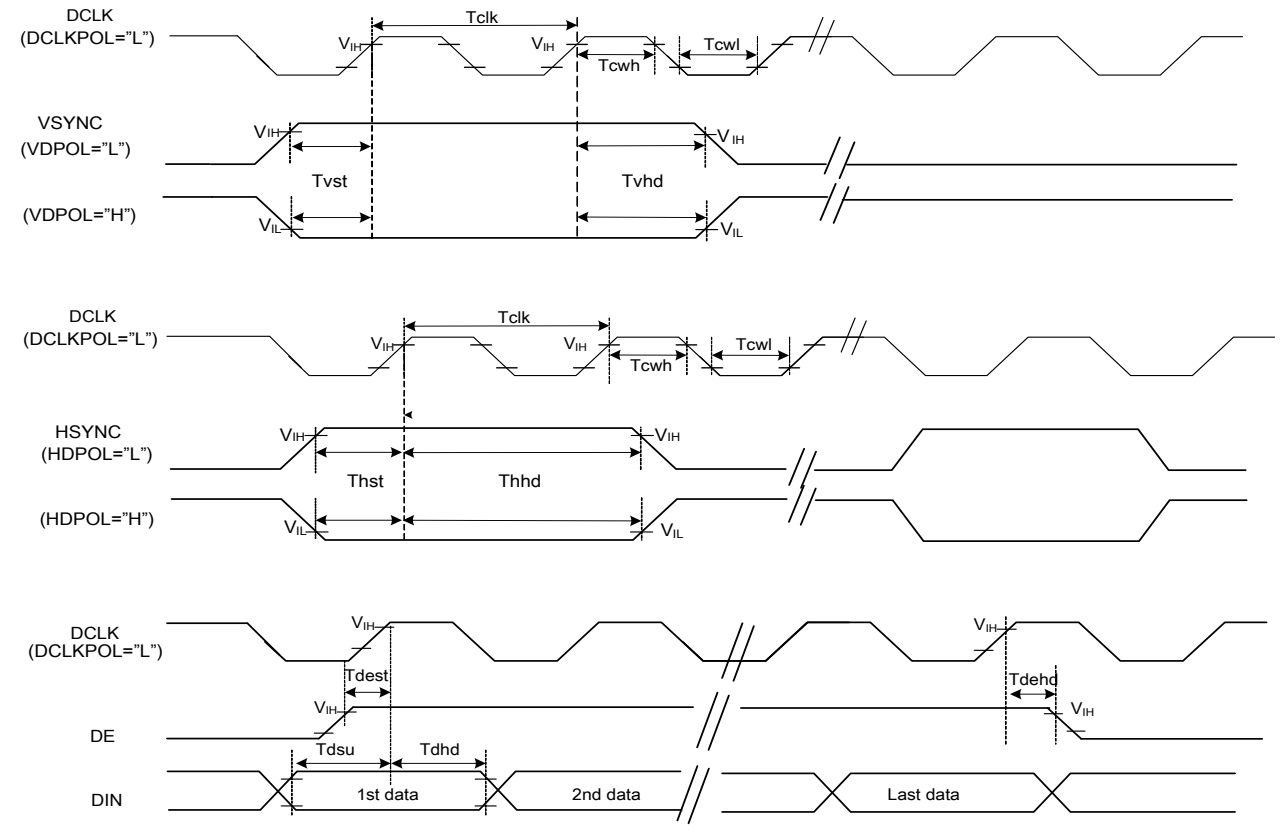
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CS Input Setup Time	T_{s0}	50	-	-	ns	
Serial Data Input Setup Time	T_{s1}	50	-	-	ns	
CS Input Hold Time	T_{h0}	50	-	-	ns	
Serial Data Input Hold Time	T_{h1}	50	-	-	ns	
SCL Write Pulse High Width	T_{wh1}	50	-	2000	ns	
SCL Write Pulse Low Width	T_{wl1}	50	-	2000	ns	
SCL Read Pulse High Width	T_{rh1}	300	-	2000	ns	
SCL Read Pulse Low Width	T_{rl1}	300	-	2000	ns	
CS Pulse High Width	T_{w2}	400	-	-	ns	

8.3.3 System Bus Timing for RGB Interface

DCLK Neagtive Polarity (DCLPOL="H")



DCLK Positive Polarity (DCLPOL="L")



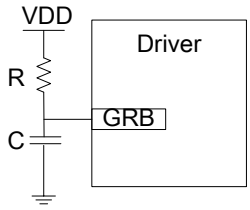
DC Electrical Characteristics (PVDD=VDD=VDDI= 3.3V, AGND= 0V, TA=25°C, Bare Chip)

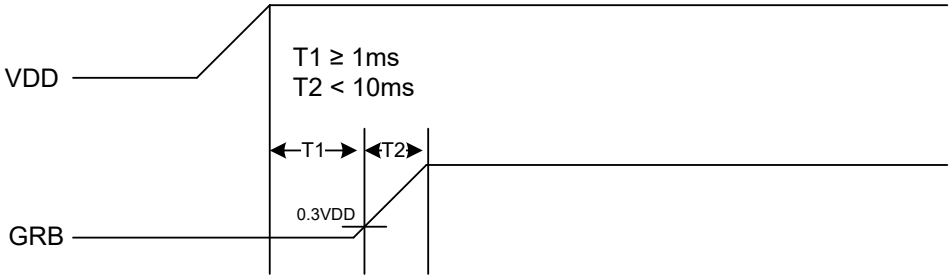
Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK Pulse Duty	Tcw	40	50	60	%	
VSYNC Setup Time	Tvst	10	-	-	ns	
VSYNC Hold Time	Tvhd	10	-	-	ns	
HSYNC Setup Time	Thst	10	-	-	ns	
HSYNC Hold Time	Thhd	10	-	-	ns	
Data Setup Time	Tdsu	10	-	-	ns	
Data Hold Time	Tdhd	10	-	-	ns	
DE Setup Time	Tdest	10	-	-	ns	
DE Hold Time	Tdehd	10	-	-	ns	

8.3.4 Reset timing

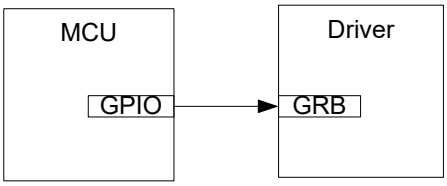
Setting GRB pin to “L” (hardware reset) can initialize internal function. Initialized by GRB pin is essential before operating. There are two suggestions for hardware reset connection.

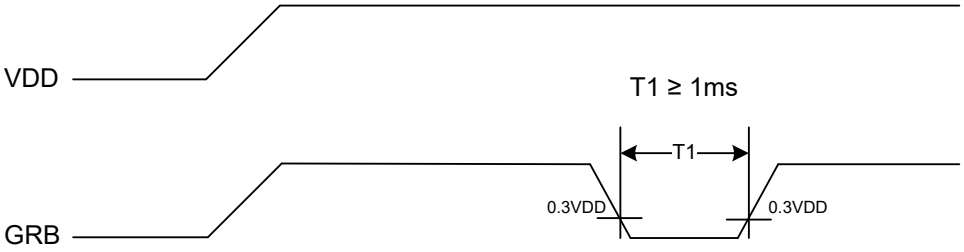
(1) The GRB pin with external RC circuit.





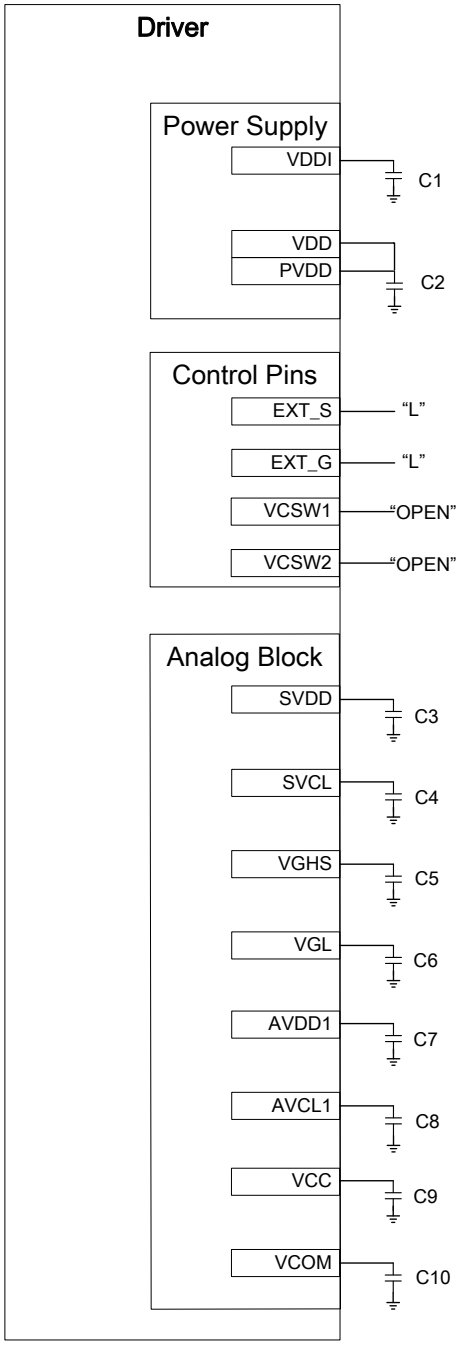
(2) The GRB pin controlled by MCU.





9. APPLICATION CIRCUIT

9.1 1 Power Mode



9.1.1 Input Voltage

Pin Name	Voltage range	Note
VDDI	3.1~3.6V	
VDD	3.1~3.6V	
PVDD	3.1~3.6V	

9.1.2 External component

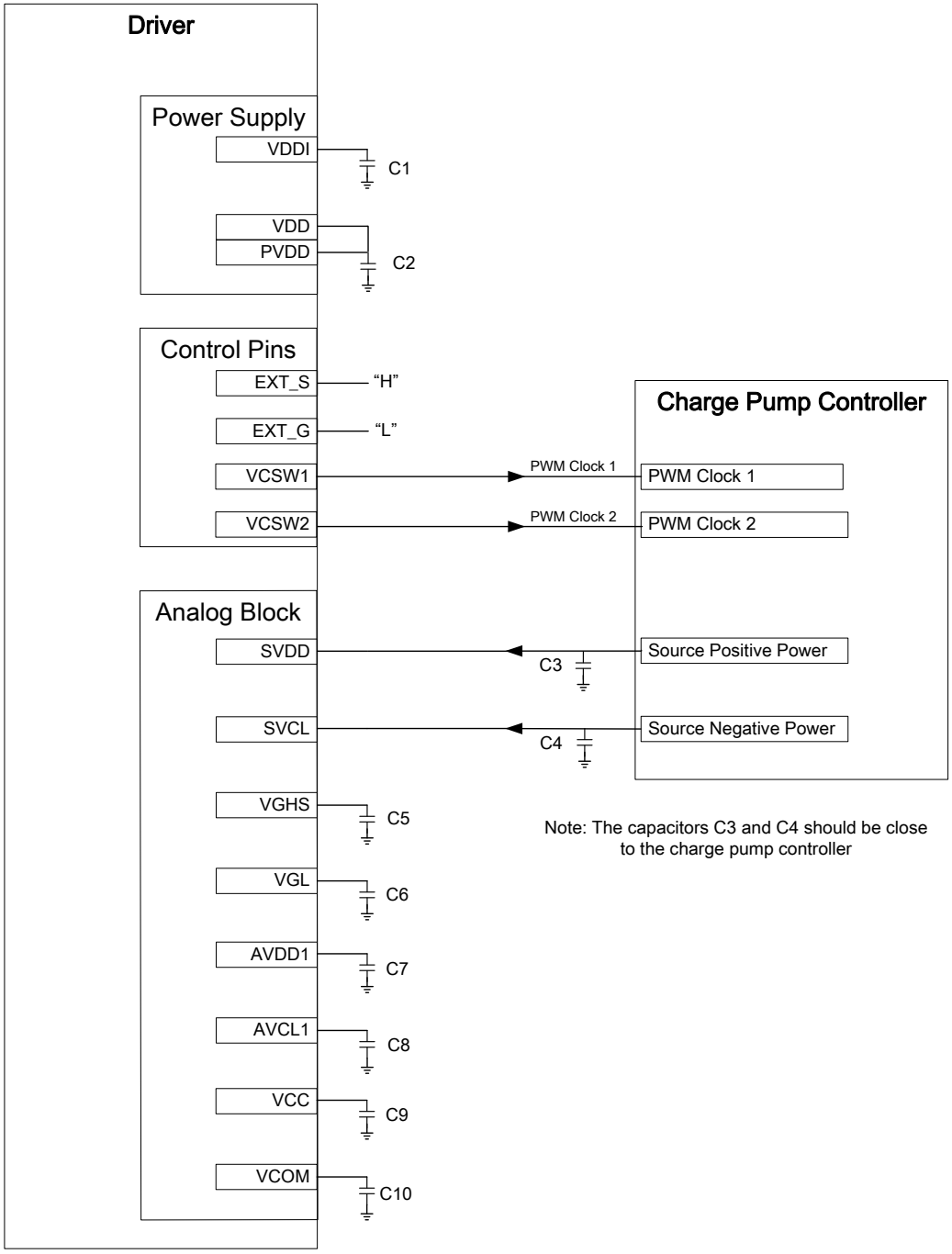
Pin Name	Symbol	Capacitance (uF)	Voltage Proof (V)	Note
VDDI	C1	2.2~4.7	6	
VDD/ PVDD	C2	2.2~4.7	6	
SVDD	C3	2.2~4.7	10	
SVCL	C4	2.2~4.7	10	
VGHS	C5	2.2~4.7	25	
VGL	C6	2.2~4.7	25	
AVDD1	C7	2.2~4.7	10	
AVCL1	C8	2.2~4.7	10	
VCC	C9	2.2~4.7	6	
VCOM	C10	2.2~4.7	6	

Note: 1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C10 is used when feedthrough voltage > 1.2V.

3. Capacitance value depends on panel loading. The recommended default value is 2.2uF.

9.2 3 Power Mode with Charge Pump Controller



9.2.1 Input Voltage

Pin Name	Voltage range(V)	Note
VDDI	3.1~3.6	
VDD	3.1~3.6	
PVDD	3.1~3.6	
SVDD	6.2~6.6	External power supply by Charge Pump Controller
SVCL	-6.2~-6.6	External power supply by Charge Pump Controller

9.2.2 External component

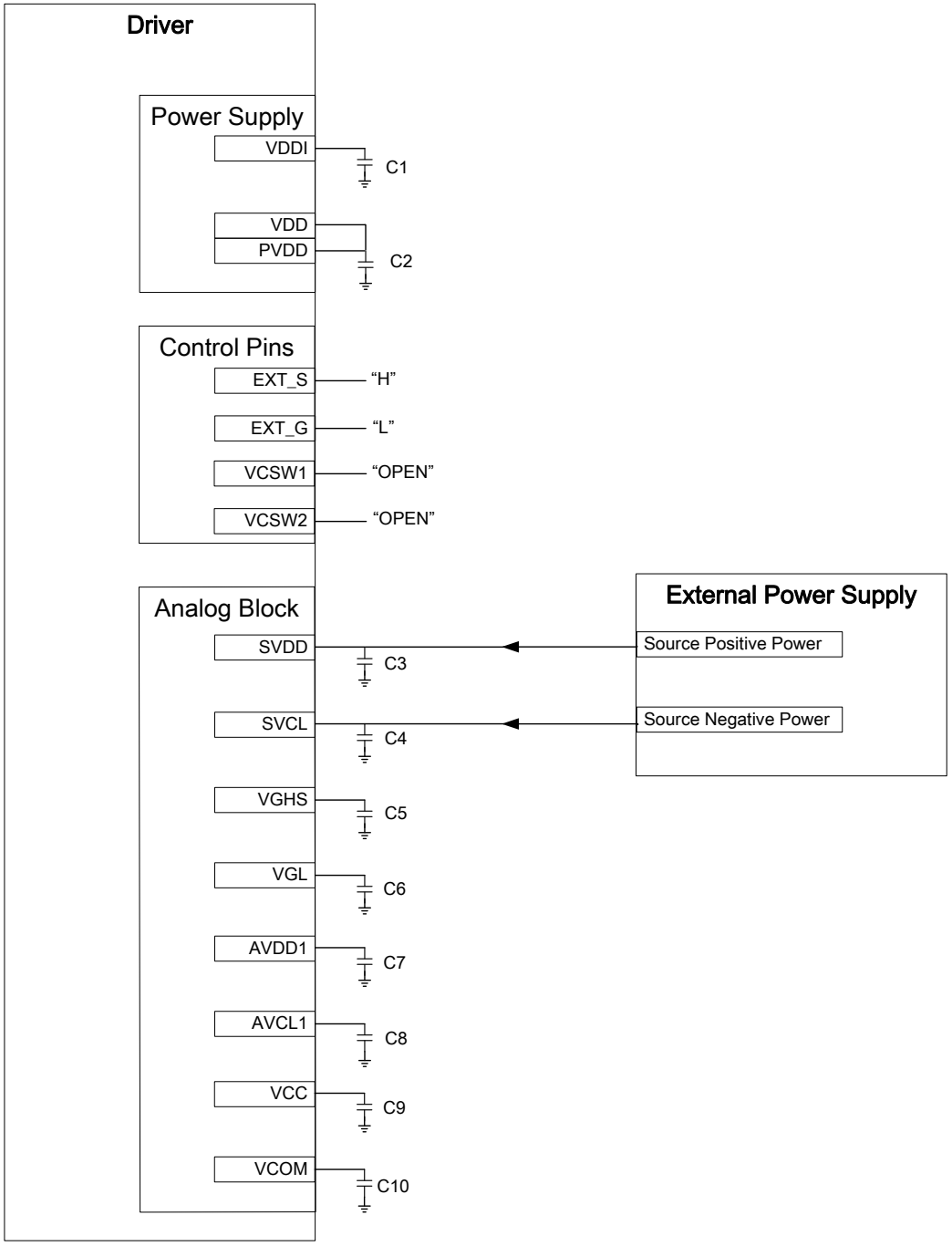
Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2~4.7	6	
C2	2.2~4.7	6	
C3	2.2~4.7	10	
C4	2.2~4.7	10	
C5	2.2~4.7	25	
C6	2.2~4.7	25	
C7	2.2~4.7	10	
C8	2.2~4.7	10	
C9	2.2~4.7	6	
C10	2.2~4.7	6	

Note: 1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C10 is used when feedthrough voltage > 1.2V.

3. Capacitance value depends on panel loading. The recommended default value is 2.2uF.

9.3 3 Power Mode with External Power Supply



9.3.1 Input Voltage

Pin Name	Voltage range(V)	Note
VDDI	3.1~3.6	
VDD	3.1~3.6	
PVDD	3.1~3.6	
SVDD	6.2~6.6	External power supply
SVCL	-6.2~-6.6	External power supply

9.3.2 External component

Symbol	Capacitance (uF)	Voltage Proof (V)	Note
C1	2.2~4.7	6	
C2	2.2~4.7	6	
C3	2.2~4.7	10	
C4	2.2~4.7	10	
C5	2.2~4.7	25	
C6	2.2~4.7	25	
C7	2.2~4.7	10	
C8	2.2~4.7	10	
C9	2.2~4.7	6	
C10	2.2~4.7	6	

Note: 1. Capacitor C1 must be added to VDDI when using LVDS interface.

2. Capacitor C10 is used when feedthrough voltage > 1.2V.

3. Capacitance value depends on panel loading. The recommended default value is 2.2uF.

9.4 Input Color Format Application Circuit

9.4.1 Pin Assignment for RGB Interface

Pin		Parallel RGB		
		888	666	565
VSYNC	SYNC Mode	VSYNC	VSYNC	VSYNC
	DE Mode	x	x	x
	SYNC DE Mode	VSYNC	VSYNC	VSYNC
HSYNC	SYNC Mode	HSYNC	HSYNC	HSYNC
	DE Mode	x	x	x
	SYNC DE Mode	HSYNC	HSYNC	HSYNC
DE	SYNC Mode	x	x	x
	DE Mode	DE	DE	DE
	SYNC DE Mode	DE	DE	DE
DCLK		DCLK	DCLK	DCLK
DR0		R0	x	x
DR1		R1	x	x
DR2		R2	R2	x
DR3		R3	R3	R3
DR4		R4	R4	R4
DR5		R5	R5	R5
DR6		R6	R6	R6
DR7		R7	R7	R7
DG0		G0	x	x
DG1		G1	x	x
DG2		G2	G2	G2
DG3		G3	G3	G3
DG4		G4	G4	G4
DG5		G5	G5	G5
DG6		G6	G6	G6
DG7		G7	G7	G7
DB0		B0	x	x
DB1		B1	x	x
DB2		B2	B2	x
DB3		B3	B3	B3
DB4		B4	B4	B4
DB5		B5	B5	B5
DB6		B6	B6	B6
DB7		B7	B7	B7

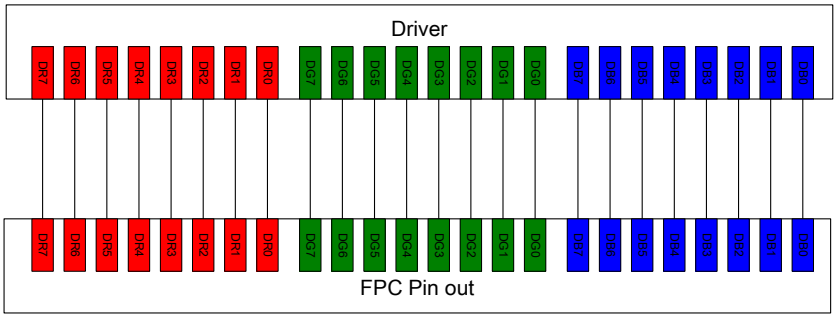
9.4.2 Data Format

Parallel RGB888					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	1'R0	2'R0	3'R0	…	N'R0
DR1	1'R1	2'R1	3'R1	…	N'R1
DR2	1'R2	2'R2	3'R2	…	N'R2
DR3	1'R3	2'R3	3'R3	…	N'R3
DR4	1'R4	2'R4	3'R4	…	N'R4
DR5	1'R5	2'R5	3'R5	…	N'R5
DR6	1'R6	2'R6	3'R6	…	N'R6
DR7	1'R7	2'R7	3'R7	…	N'R7
DG0	1'G0	2'G0	3'G0	…	N'G0
DG1	1'G1	2'G1	3'G1	…	N'G1
DG2	1'G2	2'G2	3'G2	…	N'G2
DG3	1'G3	2'G3	3'G3	…	N'G3
DG4	1'G4	2'G4	3'G4	…	N'G4
DG5	1'G5	2'G5	3'G5	…	N'G5
DG6	1'G6	2'G6	3'G6	…	N'G6
DG7	1'G7	2'G7	3'G7	…	N'G7
DB0	1'B0	2'B0	3'B0	…	N'B0
DB1	1'B1	2'B1	3'B1	…	N'B1
DB2	1'B2	2'B2	3'B2	…	N'B2
DB3	1'B3	2'B3	3'B3	…	N'B3
DB4	1'B4	2'B4	3'B4	…	N'B4
DB5	1'B5	2'B5	3'B5	…	N'B5
DB6	1'B6	2'B6	3'B6	…	N'B6
DB7	1'B7	2'B7	3'B7	…	N'B7

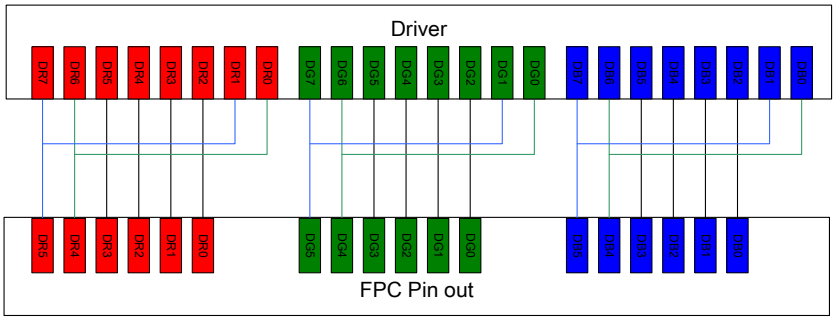
Parallel RGB666					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	x	x	x	…	x
DR1	x	x	x	…	x
DR2	1'R0	2'R0	3'R0	…	N'R0
DR3	1'R1	2'R1	3'R1	…	N'R1
DR4	1'R2	2'R2	3'R2	…	N'R2
DR5	1'R3	2'R3	3'R3	…	N'R3
DR6	1'R4	2'R4	3'R4	…	N'R4
DR7	1'R5	2'R5	3'R5	…	N'R5
DG0	x	x	x	…	x
DG1	x	x	x	…	x
DG2	1'G0	2'G0	3'G0	…	N'G0
DG3	1'G1	2'G1	3'G1	…	N'G1
DG4	1'G2	2'G2	3'G2	…	N'G2
DG5	1'G3	2'G3	3'G3	…	N'G3
DG6	1'G4	2'G4	3'G4	…	N'G4
DG7	1'G5	2'G5	3'G5	…	N'G5
DB0	x	x	x	…	x
DB1	x	x	x	…	x
DB2	1'B0	2'B0	3'B0	…	N'B0
DB3	1'B1	2'B1	3'B1	…	N'B1
DB4	1'B2	2'B2	3'B2	…	N'B2
DB5	1'B3	2'B3	3'B3	…	N'B3
DB6	1'B4	2'B4	3'B4	…	N'B4
DB7	1'B5	2'B5	3'B5	…	N'B5

Parallel RGB565					
Pin	1st Data	2nd Data	3rd Data	…	Nth Data
DR0	x	x	x	…	x
DR1	x	x	x	…	x
DR2	x	x	x	…	x
DR3	1’R0	2’R0	3’R0	…	N’R0
DR4	1’R1	2’R1	3’R1	…	N’R1
DR5	1’R2	2’R2	3’R2	…	N’R2
DR6	1’R3	2’R3	3’R3	…	N’R3
DR7	1’R4	2’R4	3’R4	…	N’R4
DG0	x	x	x	…	x
DG1	x	x	x	…	x
DG2	1’G0	2’G0	3’G0	…	N’G0
DG3	1’G1	2’G1	3’G1	…	N’G1
DG4	1’G2	2’G2	3’G2	…	N’G2
DG5	1’G3	2’G3	3’G3	…	N’G3
DG6	1’G4	2’G4	3’G4	…	N’G4
DG7	1’G5	2’G5	3’G5	…	N’G5
DB0	x	x	x	…	x
DB1	x	x	x	…	x
DB2	x	x	x	…	x
DB3	1’B0	2’B0	3’B0	…	N’B0
DB4	1’B1	2’B1	3’B1	…	N’B1
DB5	1’B2	2’B2	3’B2	…	N’B2
DB6	1’B3	2’B3	3’B3	…	N’B3
DB7	1’B4	2’B4	3’B4	…	N’B4

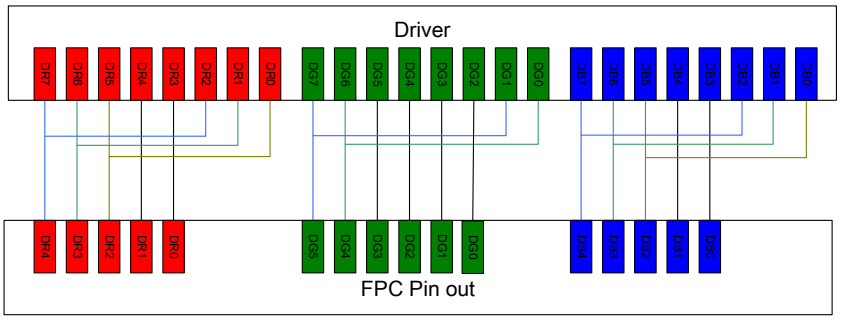
9.4.3 16.7M (R G B, 8 8 8) INPUT COLOR FORMAT



9.4.4 262K (R G B, 6 6 6) INPUT COLOR FORMAT



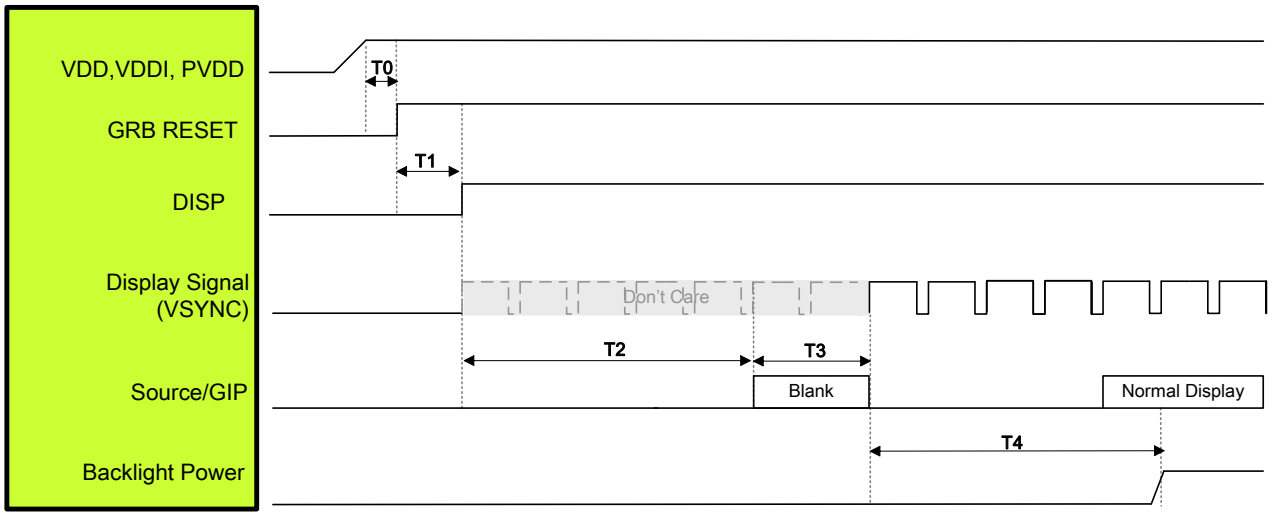
9.4.5 65K (R G B, 5 6 5) INPUT COLOR FORMAT



10. POWER ON/OFF SEQUENCE

10.1 Power On Sequence

10.1.1 1 Power Mode



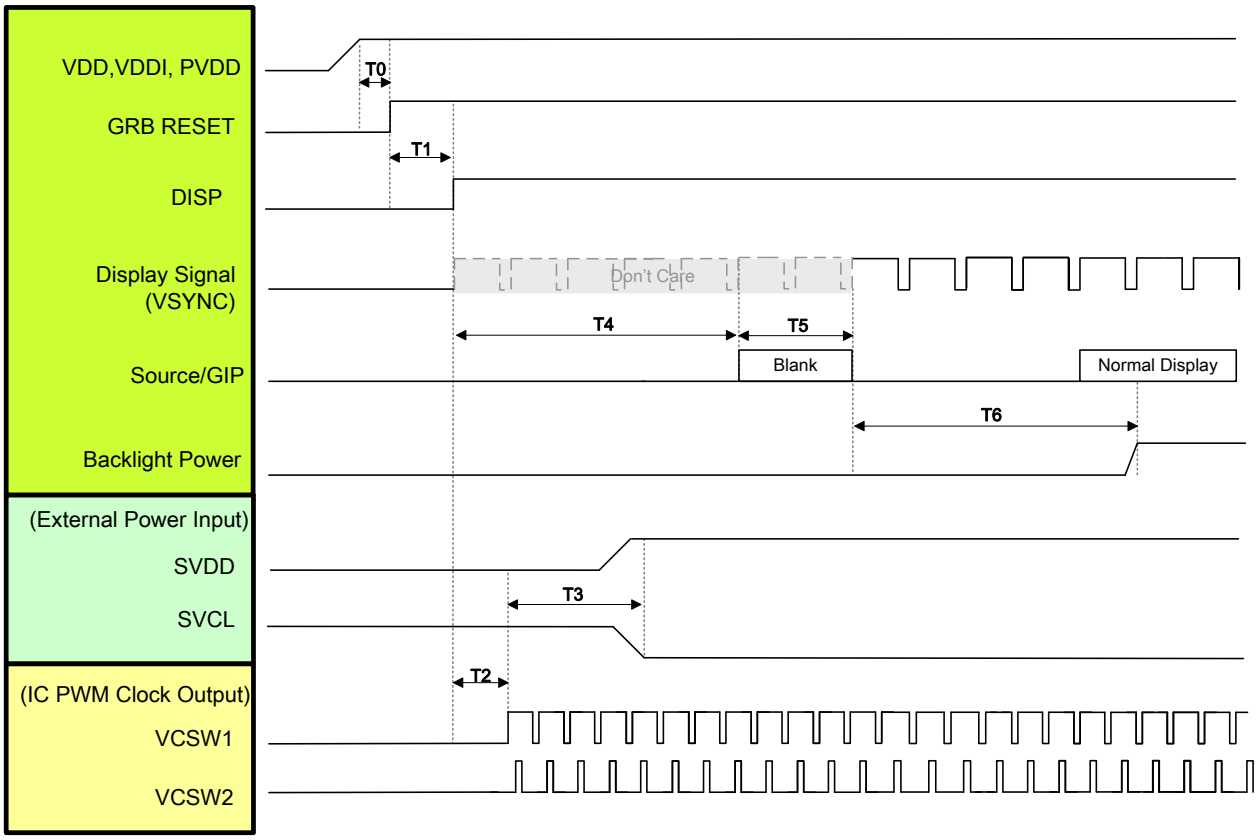
Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to DISP=“High”	≥10	ms
T2	DISP=“High” to Source/GIP scan blank	85	ms
T3	IC scan blanking signal	≥33	ms
T4	Display signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N

10.1.2 3 Power Mode with Charge Pump Controller



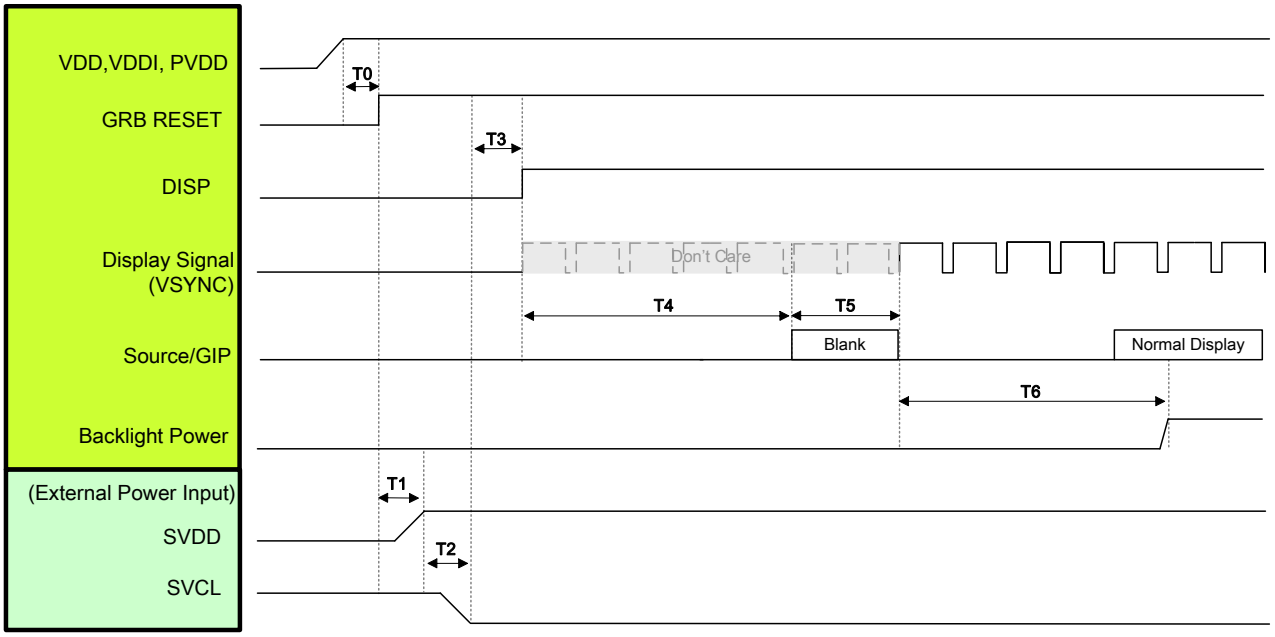
Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to DISP= “High”	≥10	ms
T2	DISP=“High” to IC output PWM clock	1	ms
T3	PWM clock input to SVDD/SVCL stability	≤50	ms
T4	DISP=“High” to Source/GIP scan blank	85	ms
T5	IC scan blanking signal	≥33	ms
T6	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

10.1.3 3 Power Mode with External Power Supply



Symbol	Description	Time	Unit
T0	System power stability to GRB RESET signal	≥1	ms
T1	GRB RESET= “High” to SVDD input	≥10	ms
T2	SVDD input to SVCL input	≥1	ms
T3	SVCL input to DISP=“High”	≥1	ms
T4	DISP=“High” to Source/GIP scan blank	85	ms
T5	IC scan blanking signal	≥33	ms
T6	Display Signal input to Backlight power on (base on Display Signal Frame Rate 60Hz)	≥100	ms

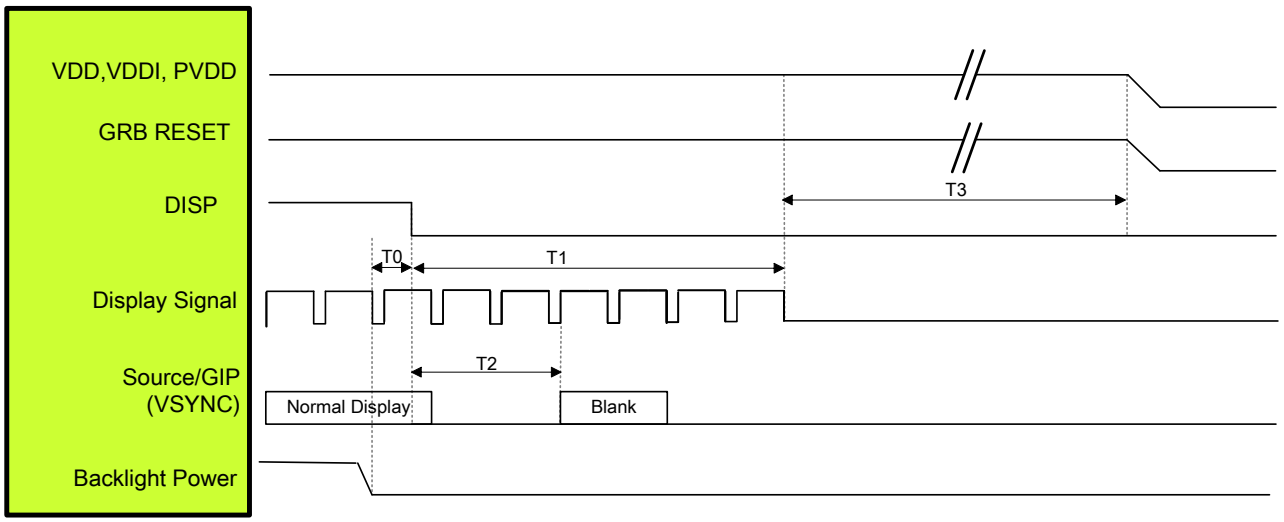
Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

10.2 Power Off Sequence

10.2.1 1 Power Mode



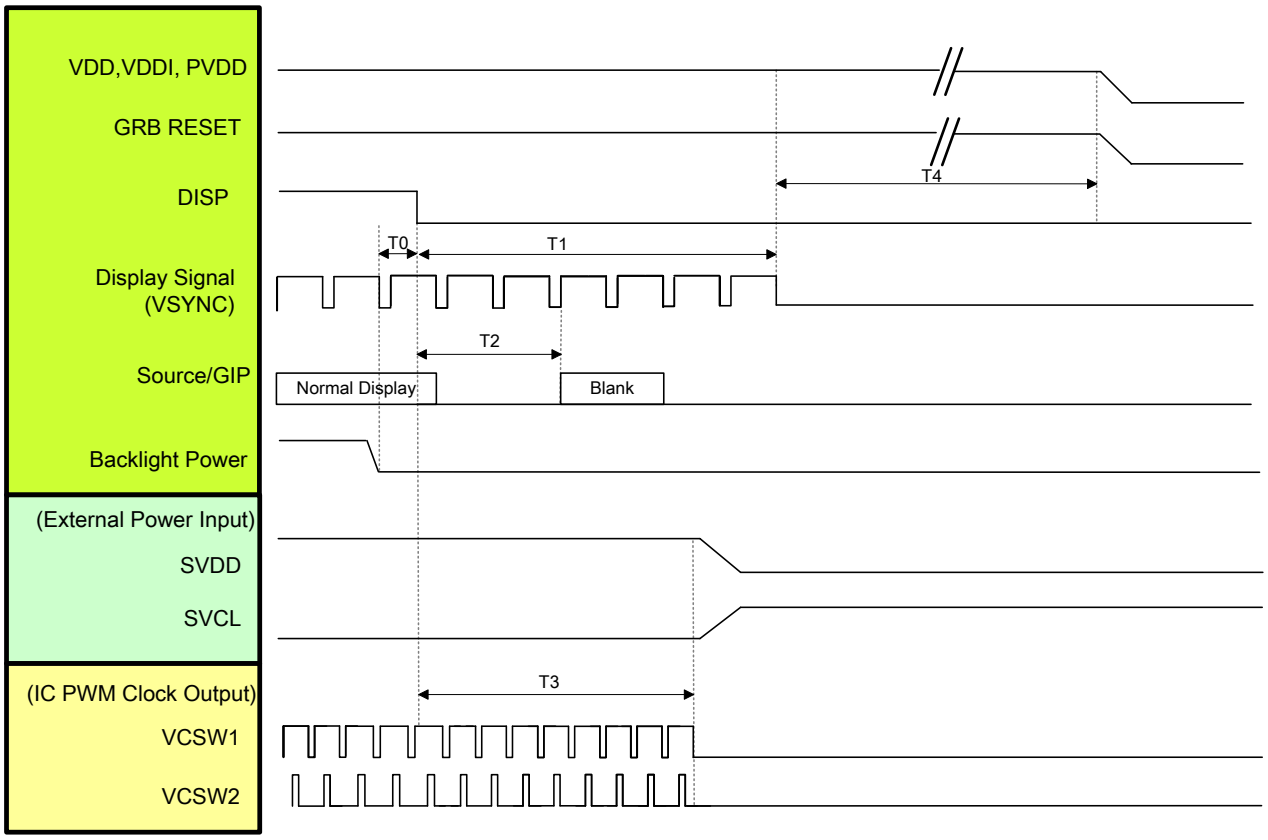
Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

10.2.2 3 Power Mode with Charge Pump Controller



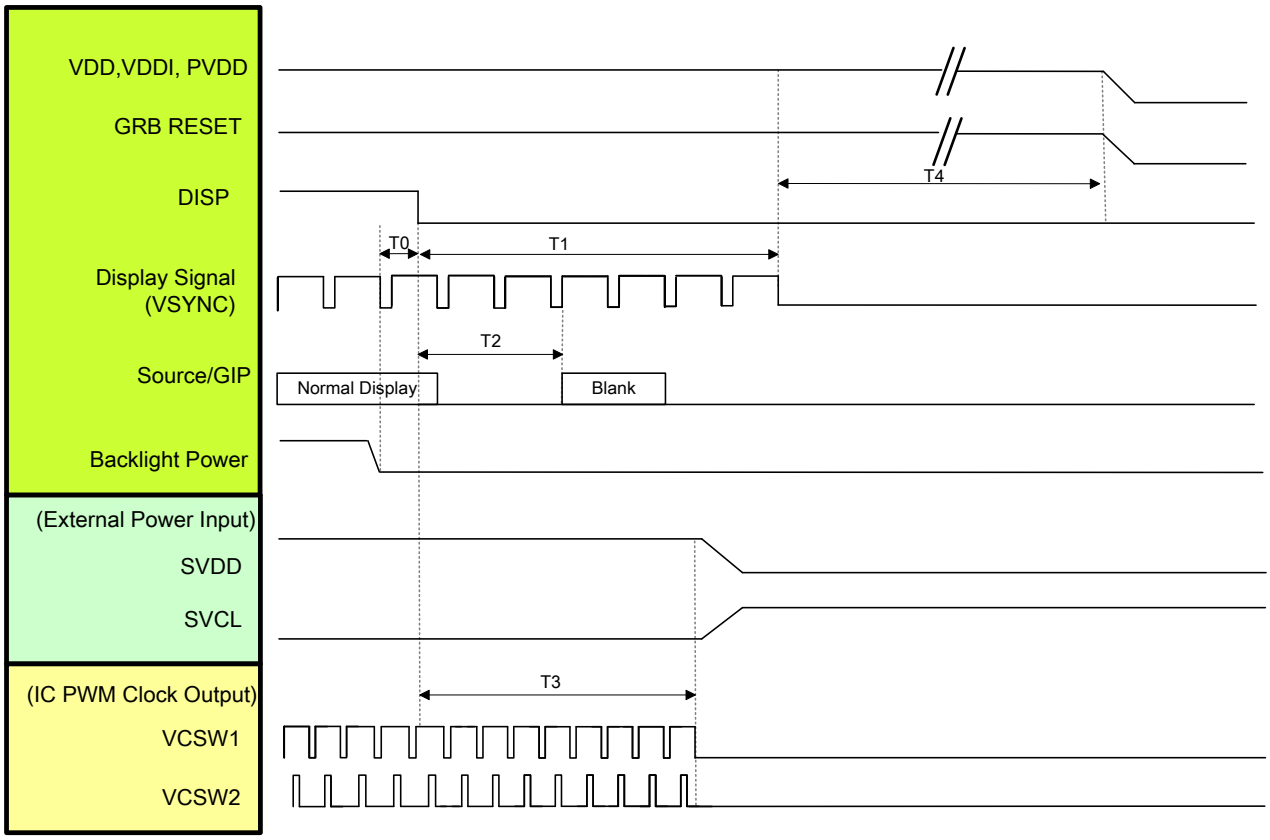
Symbol	Description	Time	Unit
T0	Backlight Power off to DISP="Low"	≥1	ms
T1	DISP="Low" to IC internal voltage discharge complete	≥100	ms
T2	DISP="Low" to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP="Low" to PWM clock stop (base on Display Signal Frame Rate 60Hz)	85	ms
T4	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull "H" or "L", IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

10.2.3 3 Power Mode with External Power Supply



Symbol	Description	Time	Unit
T0	Backlight Power off to DISP=”Low”	≥1	ms
T1	DISP=”Low” to IC internal voltage discharge complete	100	ms
T2	DISP=”Low” to Source/GIP scan blank (base on Display Signal Frame Rate 60Hz)	≤50	ms
T3	DISP=”Low” to SVDD /SVCL Power off	85	ms
T4	IC internal voltage discharge is completed to VDD/VDDI/PVDD off	≥0	ms

Note: 1. When DISP pull “H” or “L”, IC will execute the internal power on or power off procedures .Please be careful about the timing of DISP and do not interrupt it during power on or power off procedure, otherwise unexpected errors will occur.

2. RGB interface Display signal: DCLK; VSYNC; HSYNC; DE; DR[7:0]; DG[7:0]; DB[7:0].

3. LVDS interface Display signal: DCLK P/N; RX[3:0] P/N.

11. RECOMMENDED PANEL ROUTING RESISTANCE

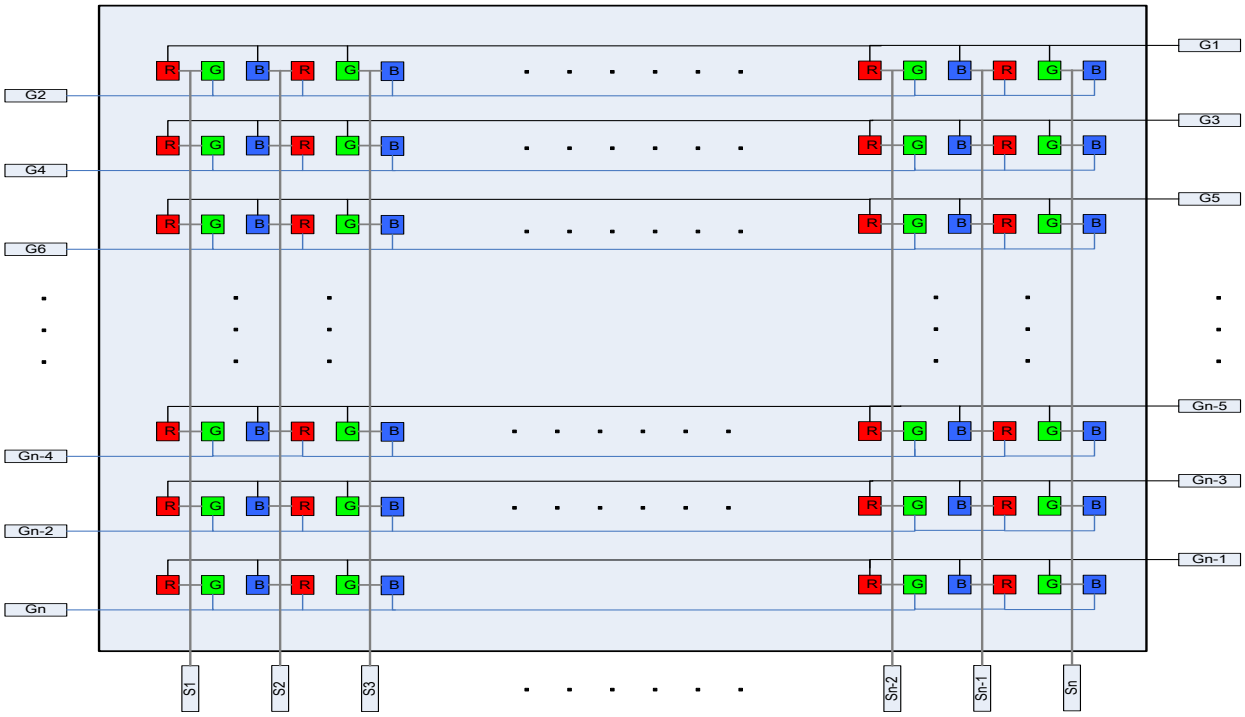
The recommended wiring resistance values are given below. The wiring resistance values affect the current capability of the power supply blocks and thus must be designed within the given range.

Pin Number	Pin Name	Unit: ohm
1	VDDI	<1
2	VDD	<1
3	PVDD	<1
4	DGND	<1
5	AGND	<1
6	SGND	<1
7	PGND	<1
8	SVCL	<3
9	SVDD	<3
10	VCOM	<3
11	VGHS	<3
12	VGL	<3
13	GVDD	<50
14	GVCL	<50
15	VGSP	<50
16	VCC	<50
17	RGND	<50
18	AVCL1	<50
19	AVDD1	<50
20	CS	<50
21	SDA	<50
22	SCL	<50
23	DISP	<50
24	GRB	<50
25	DCLKN	<50
26	DCLKP	<50
27	DR[7:0]	<50
28	DG[7:0]	<50
29	DB[7:0]	<50
30	DE	<50
31	VSYNC	<50

Pin Number	Pin Name	Unit: ohm
32	HSYNC	<50
33	AUTODL	<50
34	HDIR	<50
35	VDIR	<50
36	INTF	<50
37	VDPOL_LVDS_SEL	<50
38	HDPOL	<50
39	DCLKPOL	<50
40	VPP	<50
41	BIST_EN	<50
42	LVDS_FMT	<50
43	EXT_S	<50
44	EXT_G	<50
45	VCSW1	<50
46	VCSW2	<50
47	TESTI[14:0]	<50
48	TESTOUT[13:0]	<50
49	DUMMY	<50

12. COLOR FILTER ARRANGEMENT

The IC supports the stripe color filter of dual-gate application. The color filter arrangement on panel is shown below.



13. REVISION HISTORY

Revision	Description	Date
V1.0	Official Release	2026/03