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ILI9342C

a-Si TFT LCD Single Chip Driver 320RGBx240 Resolution and 262K color

Datasheet

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Table of Contents

1. Introduction

ILI9342C is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 320RGBx240 dots, comprising a 960-channel source driver, a 240-channel gate driver, 172,800 bytes GRAM for graphic display data of 320RGBx240 dots, and power supply circuit.

ILI9342C supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9342C supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9342C an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

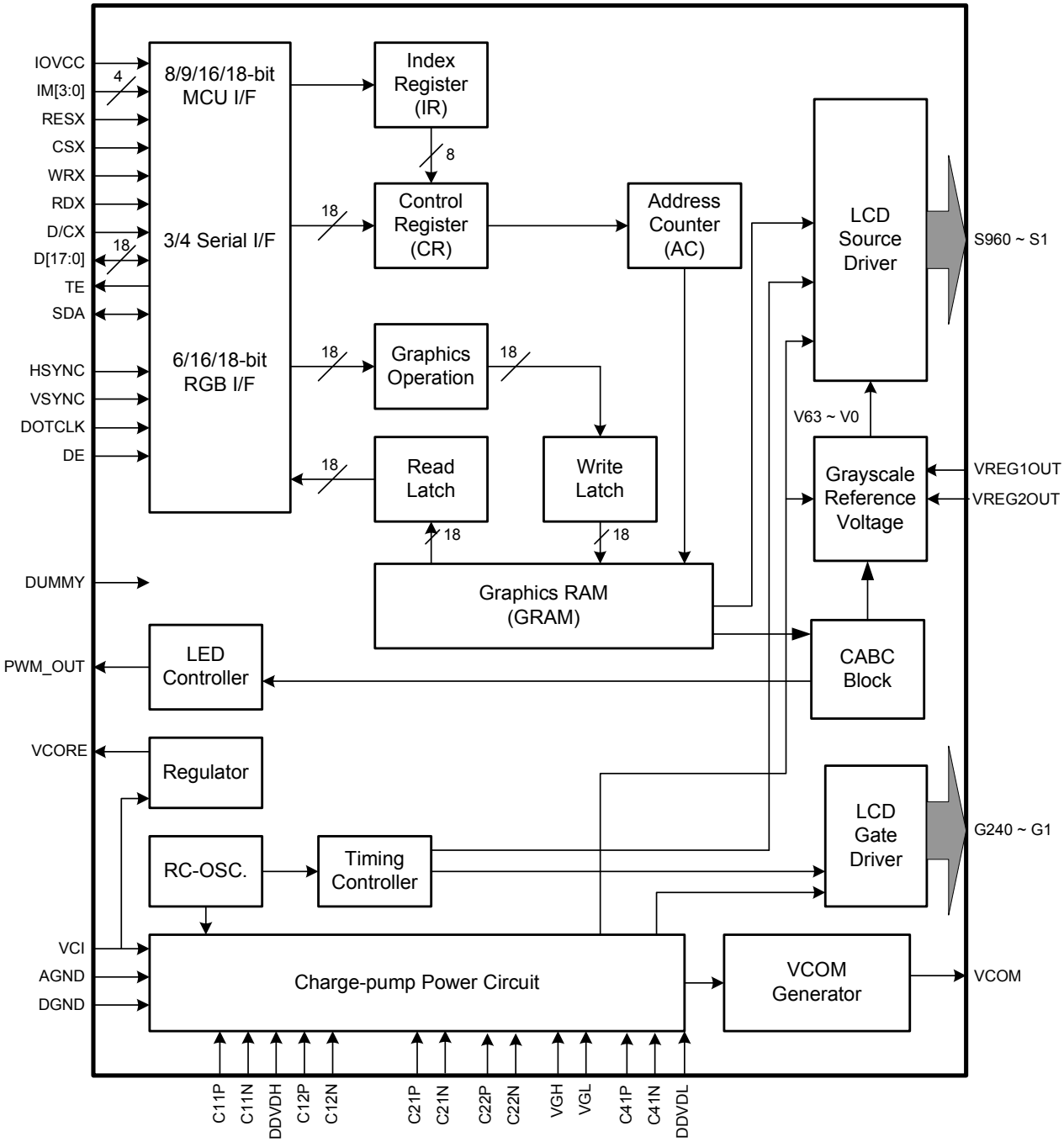
2. Features

- Display resolution: [320xRGB](H) x 240(V)
- Output:
  - 960 source outputs
  - 240 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-Ⅰ/8080-Ⅱ series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/Column inversion
  - 4 preset Gamma curves with separate RGB Gamma correction
- Dynamic backlight control
- MTP :
  - 8-bits for ID1, ID2, ID3
  - MADCTL (MX/MY/MV/RGB/REV)
  - 7-bits for VCOM adjustment
- Low -power consumption architecture
  - Low operating power supplies:

- IOVCC = 1.65V ~ 3.3V (logic)
- VCI = 2.6V ~ 3.3V (analog)

- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - DDVDH - GND = 4.5V ~ 6.0V
    - DDVDL - GND = -4.5V ~ -6.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL ≦ 32.0V
  - VCOM driver output voltage
    - VCOM = -0.4 ~ -2.0 V
- Operate temperature range: -30℃ to 70℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

Power Supply Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
IOVCC	I	P	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.6 ~ 3.3 V)
VCORE	O	Digital Power	Regulated Low voltage level for interface circuits
DGND	P	Power supply	- DGND for the digital side: DGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
AGND	P	Power supply	- AGND for the analog side: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.

Test Pads			
Pin Name	I/O	Type	Descriptions
TEST_EN TEST_OSC	I	DGND	TEST pin input
TESTO1~O2	I/O	Open	TEST pin
TEST0~8	I	DGND	TEST pin
DUMMYR1 DUMMYR2 DUMMYR3 DUMMYR4	-	Open	Contact resistance measurement pad. In normal operation, leave this unconnected. These pads are at DGND level. When measuring an ohm resistance of the contact, do not apply any power.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
GPIO0~7	I/O	-	Standard input/output pin As for GPIO0~7 to terminal, setting of an input and output direction is possible

<table>
<tr><th colspan="3">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/GND)</td><td>- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>80 MCU 16-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>80 MCU 9-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>4-wire 8-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10]
D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10],</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
* : Fix this pin at IOVCC or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low. RESX1 is equal to RESX.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>Chip select input pin (“Low” enable).
This pin can be permanently fixed “Low” in MPU interface mode only.
CSX1 is equal to CSX.
* note1,2</td></tr>
<tr><td>D/CX (SCL)</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>(D/CX)This pin is used to select “Data or Command” in the parallel interface.
When D/CX = ’1’, data is selected.
When D/CX = ’0’, command is selected.
(SCL)This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
If not used, this pin should be connected to IOVCC or GND.
DCX_SCL1 is equal to D/CX(SCL).</td></tr>
<tr><td>RDX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>8080-Ⅰ/8080-Ⅱ system (RDX): Serves as a read signal and MCU read data at the rising edge.
Fix to IOVCC or GND level when not in use.</td></tr>
<tr><td>WRX
(D/CX)</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>8080-Ⅰ/8080-Ⅱ system (WRX): Serves as a write signal and writes data at the rising edge.
4-line system (D/CX): Serves as command or parameter select.</td></tr>
</table>

			Fix to IOVCC or GND level when not in use.
D[17:0]	I/O	MCU (IOVCC/GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode *Fix to GND level when not in use*
SDA	I/O	MCU (IOVCC/GND)	When IM[3] : High, Serial in/out signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.
TE	O	MCU (IOVCC/GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin. TE1 is equal to TE.
DOTCLK	I	MCU (IOVCC/GND)	Dot clock signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*
VSYNC	I	MCU (IOVCC/GND)	Frame synchronizing signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*
HSYNC	I	MCU (IOVCC/GND)	Line synchronizing signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*
DE	I	MCU (IOVCC/GND)	Data enable signal for RGB interface operation. *Fix to IOVCC or GND level when not in use.*

Note.

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins			
Pin Name	**I/O**	**Type**	**Descriptions**
S960~S1	O	Source	Source output signals.. *Leave the pin to open when not in use.*
G240~G1	O	Gate	Gate output signals. *Leave the pin to open when not in use.*
DDVDH	O	Stabilizing capacitor	Power supply for the source driver and VCOM driver
DDVDL	O	Stabilizing capacitor	Power supply for the source driver and VCOM driver
VGH	O	Power	Power supply for the gate driver. Adjust the VGH level with the BT[3:0] bits. Connect this pad with a stabilizing capacitor.
VGL	O	Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[3:0] bits. Connect this pad with a stabilizing capacitor.
C11P, C11N	P	Step-up capacitor	Connect the charge-pumping capacitor on C11P/C11N for generating DDVDH level.
C12P, C12N	P	Step-up capacitor -	Connect the charge-pumping capacitor on C12P/C12N for generating DDVDH level.
C21P, C21N	P	Step-up capacitor	Connect the charge-pumping capacitor on C21P/C21N for generating VGH, VGL level.
C22P, C22N	P	Step-up capacitor	Connect the charge-pumping capacitor on C22P/C22N for generating –VCI1 3X level.
C41P, C41N	P	Step-up capacitor	Connect the charge-pumping capacitor for generating DDVDL level.
VREG1OUT	O	Power	- Internal generated stable power for source driver unit. - The voltage level can be set by VRH1[4:0]. - VREG1OUT is a positive grayscale reference voltage of source driver. - VREG1OUT =3.6~(DDVDH-0.3V)
VREG2OUT	O	Power	- Internal generated stable power for source driver unit. - The voltage level can be set by VRH2[4:0]. - VREG2OUT is a negative grayscale reference voltage of source driver. - VREG2OUT =(DDVDL-0.3)~-3.6V
VGS	I	Power	Low reference voltage for grayscale voltage generator. Connect an external resistor or to system ground.
VCOM	O	Power	- The power supply of common voltage in DC VCOM driving. - The voltage range is set between -0.4V to -2.0V.

PWM_OUT	O		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad. Pwm_OUT1 is equal to PWM_OUT.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		960 pins (320 x RGB)
2	TFT Gate Driver		240 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S960	V0 ~ V63 grayscales
		G1 ~ G240	VGH - VGL
		VCOM	-0.4~-2.0V
5	Input Voltage	IOVCC	1.65V ~3.3V
		VCI	2.60V ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH	4.5V ~ 6.0V
		DDVDL	-6.0V ~ -4.5V
		VGH	10.0V ~ 20.0V
		VGL	-5.0V ~ -15.0V
		VGH - VGL	Max. 32.0V
7	Internal Step-up Circuits	DDVDH	VCI1 x2
		DDVDL	-(VCI1-VCL)
		VGH	VCI1 x4, x5, x6
		VGL	VCI1 x-3, x-4, x-5

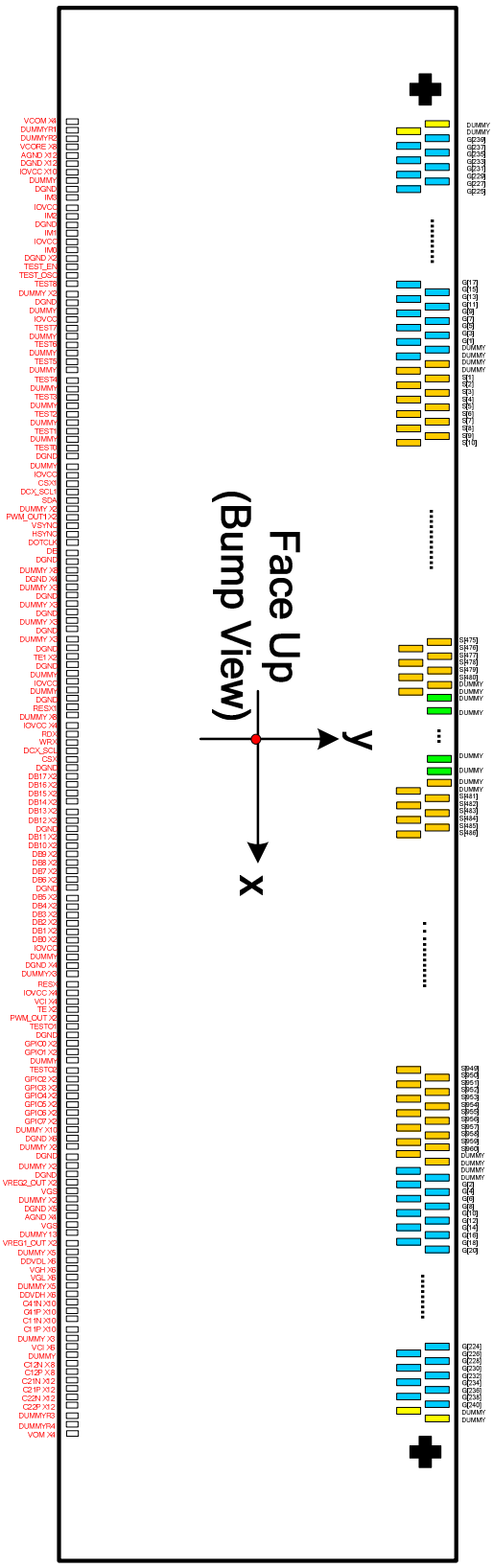
Note: VCI1 is an internal reference voltage for the step-up circuit1.

5. Pad Arrangement and Coordination

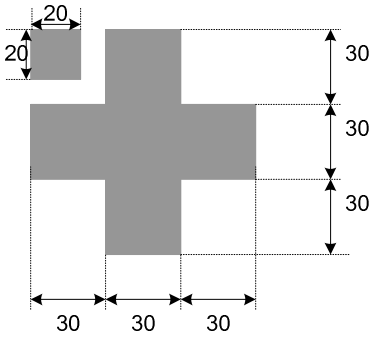
Chip Size: 18620um x 690um
Chip thickness : 280 um (typ.)
Pad Location: Pad Center.
Coordinate Origin: Chip center: (0.-3.5)
Leftest & down coordinate : (-9310,-348.5)
Rightest & up coordinate : (9310, 341.5)
Au bump height: 9 um (typ.)
Au Bump Size:

1. 24um x 69um
   input side :
   No. 1 ~ 436

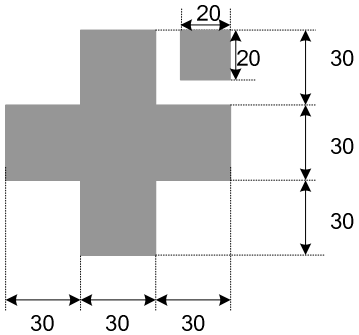
2. 14um x 90um
   Staggered LCD output side :
   No. 437 ~ 1672



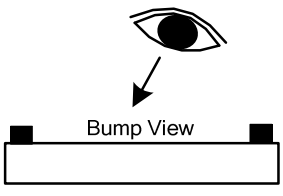
Alignment Marks



Alignment Mark: A1
(-9200, 225)



Alignment Mark: A2
(9200,225)



No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	VCOM	-8989	-245.5	51	IM3	-6989	-245.5	101	DUMMY	-4989	-245.5	151	DB17	-2989	-245.5
2	VCOM	-8949	-245.5	52	IOVCC	-6949	-245.5	102	DUMMY	-4949	-245.5	152	DB17	-2949	-245.5
3	VCOM	-8909	-245.5	53	IM2	-6909	-245.5	103	DUMMY	-4909	-245.5	153	DB16	-2909	-245.5
4	VCOM	-8869	-245.5	54	DGND	-6869	-245.5	104	DUMMY	-4869	-245.5	154	DB16	-2869	-245.5
5	DUMMYR1	-8829	-245.5	55	IM1	-6829	-245.5	105	DUMMY	-4829	-245.5	155	DB15	-2829	-245.5
6	DUMMYR2	-8789	-245.5	56	IOVCC	-6789	-245.5	106	DGND	-4789	-245.5	156	DB15	-2789	-245.5
7	VCORE	-8749	-245.5	57	IM0	-6749	-245.5	107	DGND	-4749	-245.5	157	DB14	-2749	-245.5
8	VCORE	-8709	-245.5	58	DGND	-6709	-245.5	108	DGND	-4709	-245.5	158	DB14	-2709	-245.5
9	VCORE	-8669	-245.5	59	DGND	-6669	-245.5	109	DGND	-4669	-245.5	159	DB13	-2669	-245.5
10	VCORE	-8629	-245.5	60	TEST_EN	-6629	-245.5	110	DUMMY	-4629	-245.5	160	DB13	-2629	-245.5
11	VCORE	-8589	-245.5	61	TESTOSC	-6589	-245.5	111	DUMMY	-4589	-245.5	161	DB12	-2589	-245.5
12	VCORE	-8549	-245.5	62	TEST8	-6549	-245.5	112	DUMMY	-4549	-245.5	162	DB12	-2549	-245.5
13	VCORE	-8509	-245.5	63	DUMMY	-6509	-245.5	113	DGND	-4509	-245.5	163	DGND	-2509	-245.5
14	VCORE	-8469	-245.5	64	DUMMY	-6469	-245.5	114	DUMMY	-4469	-245.5	164	DB11	-2469	-245.5
15	AGND	-8429	-245.5	65	DGND	-6429	-245.5	115	DUMMY	-4429	-245.5	165	DB11	-2429	-245.5
16	AGND	-8389	-245.5	66	DUMMY	-6389	-245.5	116	DUMMY	-4389	-245.5	166	DB10	-2389	-245.5
17	AGND	-8349	-245.5	67	IOVCC	-6349	-245.5	117	DGND	-4349	-245.5	167	DB10	-2349	-245.5
18	AGND	-8309	-245.5	68	TEST7	-6309	-245.5	118	DUMMY	-4309	-245.5	168	DB9	-2309	-245.5
19	AGND	-8269	-245.5	69	DUMMY	-6269	-245.5	119	DUMMY	-4269	-245.5	169	DB9	-2269	-245.5
20	AGND	-8229	-245.5	70	TEST6	-6229	-245.5	120	DUMMY	-4229	-245.5	170	DB8	-2229	-245.5
21	AGND	-8189	-245.5	71	DUMMY	-6189	-245.5	121	DGND	-4189	-245.5	171	DB8	-2189	-245.5
22	AGND	-8149	-245.5	72	TEST5	-6149	-245.5	122	DUMMY	-4149	-245.5	172	DB7	-2149	-245.5
23	AGND	-8109	-245.5	73	DUMMY	-6109	-245.5	123	DUMMY	-4109	-245.5	173	DB7	-2109	-245.5
24	AGND	-8069	-245.5	74	TEST4	-6069	-245.5	124	DUMMY	-4069	-245.5	174	DB6	-2069	-245.5
25	AGND	-8029	-245.5	75	DUMMY	-6029	-245.5	125	DGND	-4029	-245.5	175	DB6	-2029	-245.5
26	AGND	-7989	-245.5	76	TEST3	-5989	-245.5	126	TE1	-3989	-245.5	176	DGND	-1989	-245.5
27	DGND	-7949	-245.5	77	DUMMY	-5949	-245.5	127	TE1	-3949	-245.5	177	DB5	-1949	-245.5
28	DGND	-7909	-245.5	78	TEST2	-5909	-245.5	128	DGND	-3909	-245.5	178	DB5	-1909	-245.5
29	DGND	-7869	-245.5	79	DUMMY	-5869	-245.5	129	DUMMY	-3869	-245.5	179	DB4	-1869	-245.5
30	DGND	-7829	-245.5	80	TEST1	-5829	-245.5	130	IOVCC	-3829	-245.5	180	DB4	-1829	-245.5
31	DGND	-7789	-245.5	81	DUMMY	-5789	-245.5	131	DUMMY	-3789	-245.5	181	DB3	-1789	-245.5
32	DGND	-7749	-245.5	82	TEST0	-5749	-245.5	132	DGND	-3749	-245.5	182	DB3	-1749	-245.5
33	DGND	-7709	-245.5	83	DGND	-5709	-245.5	133	RESX1	-3709	-245.5	183	DB2	-1709	-245.5
34	DGND	-7669	-245.5	84	DUMMY	-5669	-245.5	134	DUMMY	-3669	-245.5	184	DB2	-1669	-245.5
35	DGND	-7629	-245.5	85	IOVCC	-5629	-245.5	135	DUMMY	-3629	-245.5	185	DB1	-1629	-245.5
36	DGND	-7589	-245.5	86	CSX1	-5589	-245.5	136	DUMMY	-3589	-245.5	186	DB1	-1589	-245.5
37	DGND	-7549	-245.5	87	DCX_SCL1	-5549	-245.5	137	DUMMY	-3549	-245.5	187	DB0	-1549	-245.5
38	DGND	-7509	-245.5	88	SDA	-5509	-245.5	138	DUMMY	-3509	-245.5	188	DB0	-1509	-245.5
39	IOVCC	-7469	-245.5	89	DUMMY	-5469	-245.5	139	DUMMY	-3469	-245.5	189	IOVCC	-1469	-245.5
40	IOVCC	-7429	-245.5	90	DUMMY	-5429	-245.5	140	DUMMY	-3429	-245.5	190	DUMMY	-1429	-245.5
41	IOVCC	-7389	-245.5	91	PWM_OUT1	-5389	-245.5	141	DUMMY	-3389	-245.5	191	DGND	-1389	-245.5
42	IOVCC	-7349	-245.5	92	PWM_OUT1	-5349	-245.5	142	IOVCC	-3349	-245.5	192	DGND	-1349	-245.5
43	IOVCC	-7309	-245.5	93	VSYNC	-5309	-245.5	143	IOVCC	-3309	-245.5	193	DGND	-1309	-245.5
44	IOVCC	-7269	-245.5	94	HSYNC	-5269	-245.5	144	IOVCC	-3269	-245.5	194	DGND	-1269	-245.5
45	IOVCC	-7229	-245.5	95	DOTCLK	-5229	-245.5	145	IOVCC	-3229	-245.5	195	DUMMY	-1229	-245.5
46	IOVCC	-7189	-245.5	96	DE	-5189	-245.5	146	RDX	-3189	-245.5	196	DUMMY	-1189	-245.5
47	IOVCC	-7149	-245.5	97	DGND	-5149	-245.5	147	WRX	-3149	-245.5	197	DUMMY	-1149	-245.5
48	IOVCC	-7109	-245.5	98	DUMMY	-5109	-245.5	148	DCX_SCL	-3109	-245.5	198	RESX	-1109	-245.5
49	DUMMY	-7069	-245.5	99	DUMMY	-5069	-245.5	149	CSX	-3069	-245.5	199	IOVCC	-1069	-245.5
50	DGND	-7029	-245.5	100	DUMMY	-5029	-245.5	150	DGND	-3029	-245.5	200	IOVCC	-1029	-245.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
201	IOVCC	-989	-245.5	251	DUMMY	1589	-245.5	301	VGL	3589	-245.5	351	C11P	5589	-245.5
202	IOVCC	-949	-245.5	252	DGND	1629	-245.5	302	VGL	3629	-245.5	352	C11P	5629	-245.5
203	VCI	-909	-245.5	253	VREG2_OUT	1669	-245.5	303	VGL	3669	-245.5	353	C11P	5669	-245.5
204	VCI	-869	-245.5	254	VREG2_OUT	1709	-245.5	304	VGL	3709	-245.5	354	C11P	5709	-245.5
205	VCI	-829	-245.5	255	VGS	1749	-245.5	305	VGL	3749	-245.5	355	C11P	5749	-245.5
206	VCI	-789	-245.5	256	DUMMY	1789	-245.5	306	DUMMY	3789	-245.5	356	C11P	5789	-245.5
207	TE	-749	-245.5	257	DUMMY	1829	-245.5	307	DUMMY	3829	-245.5	357	DUMMY	5829	-245.5
208	TE	-709	-245.5	258	DGND	1869	-245.5	308	DUMMY	3869	-245.5	358	DUMMY	5869	-245.5
209	PWM_OUT	-669	-245.5	259	DGND	1909	-245.5	309	DUMMY	3909	-245.5	359	DUMMY	5909	-245.5
210	PWM_OUT	-629	-245.5	260	DGND	1949	-245.5	310	DUMMY	3949	-245.5	360	VCI	5949	-245.5
211	TESTO1	-589	-245.5	261	DGND	1989	-245.5	311	DDVDH	3989	-245.5	361	VCI	5989	-245.5
212	DGND	-549	-245.5	262	DGND	2029	-245.5	312	DDVDH	4029	-245.5	362	VCI	6029	-245.5
213	GPIO0	-509	-245.5	263	AGND	2069	-245.5	313	DDVDH	4069	-245.5	363	VCI	6069	-245.5
214	GPIO0	-469	-245.5	264	AGND	2109	-245.5	314	DDVDH	4109	-245.5	364	VCI	6109	-245.5
215	GPIO1	-429	-245.5	265	AGND	2149	-245.5	315	DDVDH	4149	-245.5	365	VCI	6149	-245.5
216	GPIO1	-389	-245.5	266	AGND	2189	-245.5	316	DDVDH	4189	-245.5	366	DUMMY	6189	-245.5
217	DUMMY	-349	-245.5	267	VGS	2229	-245.5	317	C41N	4229	-245.5	367	C12N	6229	-245.5
218	TESTO2	-309	-245.5	268	DUMMY	2269	-245.5	318	C41N	4269	-245.5	368	C12N	6269	-245.5
219	GPIO2	309	-245.5	269	DUMMY	2309	-245.5	319	C41N	4309	-245.5	369	C12N	6309	-245.5
220	GPIO2	349	-245.5	270	DUMMY	2349	-245.5	320	C41N	4349	-245.5	370	C12N	6349	-245.5
221	GPIO3	389	-245.5	271	DUMMY	2389	-245.5	321	C41N	4389	-245.5	371	C12N	6389	-245.5
222	GPIO3	429	-245.5	272	DUMMY	2429	-245.5	322	C41N	4429	-245.5	372	C12N	6429	-245.5
223	GPIO4	469	-245.5	273	DUMMY	2469	-245.5	323	C41N	4469	-245.5	373	C12N	6469	-245.5
224	GPIO4	509	-245.5	274	DUMMY	2509	-245.5	324	C41N	4509	-245.5	374	C12N	6509	-245.5
225	GPIO5	549	-245.5	275	DUMMY	2549	-245.5	325	C41N	4549	-245.5	375	C12P	6549	-245.5
226	GPIO5	589	-245.5	276	DUMMY	2589	-245.5	326	C41N	4589	-245.5	376	C12P	6589	-245.5
227	GPIO6	629	-245.5	277	DUMMY	2629	-245.5	327	C41P	4629	-245.5	377	C12P	6629	-245.5
228	GPIO6	669	-245.5	278	DUMMY	2669	-245.5	328	C41P	4669	-245.5	378	C12P	6669	-245.5
229	GPIO7	709	-245.5	279	DUMMY	2709	-245.5	329	C41P	4709	-245.5	379	C12P	6709	-245.5
230	GPIO7	749	-245.5	280	DUMMY	2749	-245.5	330	C41P	4749	-245.5	380	C12P	6749	-245.5
231	DUMMY	789	-245.5	281	VREG1_OUT	2789	-245.5	331	C41P	4789	-245.5	381	C12P	6789	-245.5
232	DUMMY	829	-245.5	282	VREG1_OUT	2829	-245.5	332	C41P	4829	-245.5	382	C12P	6829	-245.5
233	DUMMY	869	-245.5	283	DUMMY	2869	-245.5	333	C41P	4869	-245.5	383	C21N	6869	-245.5
234	DUMMY	909	-245.5	284	DUMMY	2909	-245.5	334	C41P	4909	-245.5	384	C21N	6909	-245.5
235	DUMMY	949	-245.5	285	DUMMY	2949	-245.5	335	C41P	4949	-245.5	385	C21N	6949	-245.5
236	DUMMY	989	-245.5	286	DUMMY	2989	-245.5	336	C41P	4989	-245.5	386	C21N	6989	-245.5
237	DUMMY	1029	-245.5	287	DUMMY	3029	-245.5	337	C11N	5029	-245.5	387	C21N	7029	-245.5
238	DUMMY	1069	-245.5	288	DDVDL	3069	-245.5	338	C11N	5069	-245.5	388	C21N	7069	-245.5
239	DUMMY	1109	-245.5	289	DDVDL	3109	-245.5	339	C11N	5109	-245.5	389	C21N	7109	-245.5
240	DUMMY	1149	-245.5	290	DDVDL	3149	-245.5	340	C11N	5149	-245.5	390	C21N	7149	-245.5
241	DGND	1189	-245.5	291	DDVDL	3189	-245.5	341	C11N	5189	-245.5	391	C21N	7189	-245.5
242	DGND	1229	-245.5	292	DDVDL	3229	-245.5	342	C11N	5229	-245.5	392	C21N	7229	-245.5
243	DGND	1269	-245.5	293	DDVDL	3269	-245.5	343	C11N	5269	-245.5	393	C21N	7269	-245.5
244	DGND	1309	-245.5	294	VGH	3309	-245.5	344	C11N	5309	-245.5	394	C21N	7309	-245.5
245	DGND	1349	-245.5	295	VGH	3349	-245.5	345	C11N	5349	-245.5	395	C21P	7349	-245.5
246	DGND	1389	-245.5	296	VGH	3389	-245.5	346	C11N	5389	-245.5	396	C21P	7389	-245.5
247	DUMMY	1429	-245.5	297	VGH	3429	-245.5	347	C11P	5429	-245.5	397	C21P	7429	-245.5
248	DUMMY	1469	-245.5	298	VGH	3469	-245.5	348	C11P	5469	-245.5	398	C21P	7469	-245.5
249	DGND	1509	-245.5	299	VGH	3509	-245.5	349	C11P	5509	-245.5	399	C21P	7509	-245.5
250	DUMMY	1549	-245.5	300	VGL	3549	-245.5	350	C11P	5549	-245.5	400	C21P	7549	-245.5

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
401	C21P	7589	-245.5	451	G216	8811	233	501	G116	8011	233	551	G16	7211	233
402	C21P	7629	-245.5	452	G214	8795	107	502	G114	7995	107	552	G14	7195	107
403	C21P	7669	-245.5	453	G212	8779	233	503	G112	7979	233	553	G12	7179	233
404	C21P	7709	-245.5	454	G210	8763	107	504	G110	7963	107	554	G10	7163	107
405	C21P	7749	-245.5	455	G208	8747	233	505	G108	7947	233	555	G8	7147	233
406	C21P	7789	-245.5	456	G206	8731	107	506	G106	7931	107	556	G6	7131	107
407	C22N	7829	-245.5	457	G204	8715	233	507	G104	7915	233	557	G4	7115	233
408	C22N	7869	-245.5	458	G202	8699	107	508	G102	7899	107	558	G2	7099	107
409	C22N	7909	-245.5	459	G200	8683	233	509	G100	7883	233	559	DUMMY	7083	233
410	C22N	7949	-245.5	460	G198	8667	107	510	G98	7867	107	560	DUMMY	7067	107
411	C22N	7989	-245.5	461	G196	8651	233	511	G96	7851	233	561	DUMMY	7051	233
412	C22N	8029	-245.5	462	G194	8635	107	512	G94	7835	107	562	DUMMY	7037	107
413	C22N	8069	-245.5	463	G192	8619	233	513	G92	7819	233	563	S960	7023	233
414	C22N	8109	-245.5	464	G190	8603	107	514	G90	7803	107	564	S959	7009	107
415	C22N	8149	-245.5	465	G188	8587	233	515	G88	7787	233	565	S958	6995	233
416	C22N	8189	-245.5	466	G186	8571	107	516	G86	7771	107	566	S957	6981	107
417	C22N	8229	-245.5	467	G184	8555	233	517	G84	7755	233	567	S956	6967	233
418	C22N	8269	-245.5	468	G182	8539	107	518	G82	7739	107	568	S955	6953	107
419	C22P	8309	-245.5	469	G180	8523	233	519	G80	7723	233	569	S954	6939	233
420	C22P	8349	-245.5	470	G178	8507	107	520	G78	7707	107	570	S953	6925	107
421	C22P	8389	-245.5	471	G176	8491	233	521	G76	7691	233	571	S952	6911	233
422	C22P	8429	-245.5	472	G174	8475	107	522	G74	7675	107	572	S951	6897	107
423	C22P	8469	-245.5	473	G172	8459	233	523	G72	7659	233	573	S950	6883	233
424	C22P	8509	-245.5	474	G170	8443	107	524	G70	7643	107	574	S949	6869	107
425	C22P	8549	-245.5	475	G168	8427	233	525	G68	7627	233	575	S948	6855	233
426	C22P	8589	-245.5	476	G166	8411	107	526	G66	7611	107	576	S947	6841	107
427	C22P	8629	-245.5	477	G164	8395	233	527	G64	7595	233	577	S946	6827	233
428	C22P	8669	-245.5	478	G162	8379	107	528	G62	7579	107	578	S945	6813	107
429	C22P	8709	-245.5	479	G160	8363	233	529	G60	7563	233	579	S944	6799	233
430	C22P	8749	-245.5	480	G158	8347	107	530	G58	7547	107	580	S943	6785	107
431	DUMMYR3	8789	-245.5	481	G156	8331	233	531	G56	7531	233	581	S942	6771	233
432	DUMMYR4	8829	-245.5	482	G154	8315	107	532	G54	7515	107	582	S941	6757	107
433	VCOM	8869	-245.5	483	G152	8299	233	533	G52	7499	233	583	S940	6743	233
434	VCOM	8909	-245.5	484	G150	8283	107	534	G50	7483	107	584	S939	6729	107
435	VCOM	8949	-245.5	485	G148	8267	233	535	G48	7467	233	585	S938	6715	233
436	VCOM	8989	-245.5	486	G146	8251	107	536	G46	7451	107	586	S937	6701	107
437	DUMMY	9035	233	487	G144	8235	233	537	G44	7435	233	587	S936	6687	233
438	DUMMY	9019	107	488	G142	8219	107	538	G42	7419	107	588	S935	6673	107
439	G240	9003	233	489	G140	8203	233	539	G40	7403	233	589	S934	6659	233
440	G238	8987	107	490	G138	8187	107	540	G38	7387	107	590	S933	6645	107
441	G236	8971	233	491	G136	8171	233	541	G36	7371	233	591	S932	6631	233
442	G234	8955	107	492	G134	8155	107	542	G34	7355	107	592	S931	6617	107
443	G232	8939	233	493	G132	8139	233	543	G32	7339	233	593	S930	6603	233
444	G230	8923	107	494	G130	8123	107	544	G30	7323	107	594	S929	6589	107
445	G228	8907	233	495	G128	8107	233	545	G28	7307	233	595	S928	6575	233
446	G226	8891	107	496	G126	8091	107	546	G26	7291	107	596	S927	6561	107
447	G224	8875	233	497	G124	8075	233	547	G24	7275	233	597	S926	6547	233
448	G222	8859	107	498	G122	8059	107	548	G22	7259	107	598	S925	6533	107
449	G220	8843	233	499	G120	8043	233	549	G20	7243	233	599	S924	6519	233
450	G218	8827	107	500	G118	8027	107	550	G18	7227	107	600	S923	6505	107

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	S922	6491	233	651	S872	5791	233	701	S822	5091	233	751	S772	4391	233
602	S921	6477	107	652	S871	5777	107	702	S821	5077	107	752	S771	4377	107
603	S920	6463	233	653	S870	5763	233	703	S820	5063	233	753	S770	4363	233
604	S919	6449	107	654	S869	5749	107	704	S819	5049	107	754	S769	4349	107
605	S918	6435	233	655	S868	5735	233	705	S818	5035	233	755	S768	4335	233
606	S917	6421	107	656	S867	5721	107	706	S817	5021	107	756	S767	4321	107
607	S916	6407	233	657	S866	5707	233	707	S816	5007	233	757	S766	4307	233
608	S915	6393	107	658	S865	5693	107	708	S815	4993	107	758	S765	4293	107
609	S914	6379	233	659	S864	5679	233	709	S814	4979	233	759	S764	4279	233
610	S913	6365	107	660	S863	5665	107	710	S813	4965	107	760	S763	4265	107
611	S912	6351	233	661	S862	5651	233	711	S812	4951	233	761	S762	4251	233
612	S911	6337	107	662	S861	5637	107	712	S811	4937	107	762	S761	4237	107
613	S910	6323	233	663	S860	5623	233	713	S810	4923	233	763	S760	4223	233
614	S909	6309	107	664	S859	5609	107	714	S809	4909	107	764	S759	4209	107
615	S908	6295	233	665	S858	5595	233	715	S808	4895	233	765	S758	4195	233
616	S907	6281	107	666	S857	5581	107	716	S807	4881	107	766	S757	4181	107
617	S906	6267	233	667	S856	5567	233	717	S806	4867	233	767	S756	4167	233
618	S905	6253	107	668	S855	5553	107	718	S805	4853	107	768	S755	4153	107
619	S904	6239	233	669	S854	5539	233	719	S804	4839	233	769	S754	4139	233
620	S903	6225	107	670	S853	5525	107	720	S803	4825	107	770	S753	4125	107
621	S902	6211	233	671	S852	5511	233	721	S802	4811	233	771	S752	4111	233
622	S901	6197	107	672	S851	5497	107	722	S801	4797	107	772	S751	4097	107
623	S900	6183	233	673	S850	5483	233	723	S800	4783	233	773	S750	4083	233
624	S899	6169	107	674	S849	5469	107	724	S799	4769	107	774	S749	4069	107
625	S898	6155	233	675	S848	5455	233	725	S798	4755	233	775	S748	4055	233
626	S897	6141	107	676	S847	5441	107	726	S797	4741	107	776	S747	4041	107
627	S896	6127	233	677	S846	5427	233	727	S796	4727	233	777	S746	4027	233
628	S895	6113	107	678	S845	5413	107	728	S795	4713	107	778	S745	4013	107
629	S894	6099	233	679	S844	5399	233	729	S794	4699	233	779	S744	3999	233
630	S893	6085	107	680	S843	5385	107	730	S793	4685	107	780	S743	3985	107
631	S892	6071	233	681	S842	5371	233	731	S792	4671	233	781	S742	3971	233
632	S891	6057	107	682	S841	5357	107	732	S791	4657	107	782	S741	3957	107
633	S890	6043	233	683	S840	5343	233	733	S790	4643	233	783	S740	3943	233
634	S889	6029	107	684	S839	5329	107	734	S789	4629	107	784	S739	3929	107
635	S888	6015	233	685	S838	5315	233	735	S788	4615	233	785	S738	3915	233
636	S887	6001	107	686	S837	5301	107	736	S787	4601	107	786	S737	3901	107
637	S886	5987	233	687	S836	5287	233	737	S786	4587	233	787	S736	3887	233
638	S885	5973	107	688	S835	5273	107	738	S785	4573	107	788	S735	3873	107
639	S884	5959	233	689	S834	5259	233	739	S784	4559	233	789	S734	3859	233
640	S883	5945	107	690	S833	5245	107	740	S783	4545	107	790	S733	3845	107
641	S882	5931	233	691	S832	5231	233	741	S782	4531	233	791	S732	3831	233
642	S881	5917	107	692	S831	5217	107	742	S781	4517	107	792	S731	3817	107
643	S880	5903	233	693	S830	5203	233	743	S780	4503	233	793	S730	3803	233
644	S879	5889	107	694	S829	5189	107	744	S779	4489	107	794	S729	3789	107
645	S878	5875	233	695	S828	5175	233	745	S778	4475	233	795	S728	3775	233
646	S877	5861	107	696	S827	5161	107	746	S777	4461	107	796	S727	3761	107
647	S876	5847	233	697	S826	5147	233	747	S776	4447	233	797	S726	3747	233
648	S875	5833	107	698	S825	5133	107	748	S775	4433	107	798	S725	3733	107
649	S874	5819	233	699	S824	5119	233	749	S774	4419	233	799	S724	3719	233
650	S873	5805	107	700	S823	5105	107	750	S773	4405	107	800	S723	3705	107

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
801	S722	3691	233	851	S672	2991	233	901	S622	2291	233	951	S572	1591	233
802	S721	3677	107	852	S671	2977	107	902	S621	2277	107	952	S571	1577	107
803	S720	3663	233	853	S670	2963	233	903	S620	2263	233	953	S570	1563	233
804	S719	3649	107	854	S669	2949	107	904	S619	2249	107	954	S569	1549	107
805	S718	3635	233	855	S668	2935	233	905	S618	2235	233	955	S568	1535	233
806	S717	3621	107	856	S667	2921	107	906	S617	2221	107	956	S567	1521	107
807	S716	3607	233	857	S666	2907	233	907	S616	2207	233	957	S566	1507	233
808	S715	3593	107	858	S665	2893	107	908	S615	2193	107	958	S565	1493	107
809	S714	3579	233	859	S664	2879	233	909	S614	2179	233	959	S564	1479	233
810	S713	3565	107	860	S663	2865	107	910	S613	2165	107	960	S563	1465	107
811	S712	3551	233	861	S662	2851	233	911	S612	2151	233	961	S562	1451	233
812	S711	3537	107	862	S661	2837	107	912	S611	2137	107	962	S561	1437	107
813	S710	3523	233	863	S660	2823	233	913	S610	2123	233	963	S560	1423	233
814	S709	3509	107	864	S659	2809	107	914	S609	2109	107	964	S559	1409	107
815	S708	3495	233	865	S658	2795	233	915	S608	2095	233	965	S558	1395	233
816	S707	3481	107	866	S657	2781	107	916	S607	2081	107	966	S557	1381	107
817	S706	3467	233	867	S656	2767	233	917	S606	2067	233	967	S556	1367	233
818	S705	3453	107	868	S655	2753	107	918	S605	2053	107	968	S555	1353	107
819	S704	3439	233	869	S654	2739	233	919	S604	2039	233	969	S554	1339	233
820	S703	3425	107	870	S653	2725	107	920	S603	2025	107	970	S553	1325	107
821	S702	3411	233	871	S652	2711	233	921	S602	2011	233	971	S552	1311	233
822	S701	3397	107	872	S651	2697	107	922	S601	1997	107	972	S551	1297	107
823	S700	3383	233	873	S650	2683	233	923	S600	1983	233	973	S550	1283	233
824	S699	3369	107	874	S649	2669	107	924	S599	1969	107	974	S549	1269	107
825	S698	3355	233	875	S648	2655	233	925	S598	1955	233	975	S548	1255	233
826	S697	3341	107	876	S647	2641	107	926	S597	1941	107	976	S547	1241	107
827	S696	3327	233	877	S646	2627	233	927	S596	1927	233	977	S546	1227	233
828	S695	3313	107	878	S645	2613	107	928	S595	1913	107	978	S545	1213	107
829	S694	3299	233	879	S644	2599	233	929	S594	1899	233	979	S544	1199	233
830	S693	3285	107	880	S643	2585	107	930	S593	1885	107	980	S543	1185	107
831	S692	3271	233	881	S642	2571	233	931	S592	1871	233	981	S542	1171	233
832	S691	3257	107	882	S641	2557	107	932	S591	1857	107	982	S541	1157	107
833	S690	3243	233	883	S640	2543	233	933	S590	1843	233	983	S540	1143	233
834	S689	3229	107	884	S639	2529	107	934	S589	1829	107	984	S539	1129	107
835	S688	3215	233	885	S638	2515	233	935	S588	1815	233	985	S538	1115	233
836	S687	3201	107	886	S637	2501	107	936	S587	1801	107	986	S537	1101	107
837	S686	3187	233	887	S636	2487	233	937	S586	1787	233	987	S536	1087	233
838	S685	3173	107	888	S635	2473	107	938	S585	1773	107	988	S535	1073	107
839	S684	3159	233	889	S634	2459	233	939	S584	1759	233	989	S534	1059	233
840	S683	3145	107	890	S633	2445	107	940	S583	1745	107	990	S533	1045	107
841	S682	3131	233	891	S632	2431	233	941	S582	1731	233	991	S532	1031	233
842	S681	3117	107	892	S631	2417	107	942	S581	1717	107	992	S531	1017	107
843	S680	3103	233	893	S630	2403	233	943	S580	1703	233	993	S530	1003	233
844	S679	3089	107	894	S629	2389	107	944	S579	1689	107	994	S529	989	107
845	S678	3075	233	895	S628	2375	233	945	S578	1675	233	995	S528	975	233
846	S677	3061	107	896	S627	2361	107	946	S577	1661	107	996	S527	961	107
847	S676	3047	233	897	S626	2347	233	947	S576	1647	233	997	S526	947	233
848	S675	3033	107	898	S625	2333	107	948	S575	1633	107	998	S525	933	107
849	S674	3019	233	899	S624	2319	233	949	S574	1619	233	999	S524	919	233
850	S673	3005	107	900	S623	2305	107	950	S573	1605	107	1000	S523	905	107

No.	Pad name	X	Y
1001	S522	891	233
1002	S521	877	107
1003	S520	863	233
1004	S519	849	107
1005	S518	835	233
1006	S517	821	107
1007	S516	807	233
1008	S515	793	107
1009	S514	779	233
1010	S513	765	107
1011	S512	751	233
1012	S511	737	107
1013	S510	723	233
1014	S509	709	107
1015	S508	695	233
1016	S507	681	107
1017	S506	667	233
1018	S505	653	107
1019	S504	639	233
1020	S503	625	107
1021	S502	611	233
1022	S501	597	107
1023	S500	583	233
1024	S499	569	107
1025	S498	555	233
1026	S497	541	107
1027	S496	527	233
1028	S495	513	107
1029	S494	499	233
1030	S493	485	107
1031	S492	471	233
1032	S491	457	107
1033	S490	443	233
1034	S489	429	107
1035	S488	415	233
1036	S487	401	107
1037	S486	387	233
1038	S485	373	107
1039	S484	359	233
1040	S483	345	107
1041	S482	331	233
1042	S481	317	107
1043	DUMMY	303	233
1044	DUMMY	289	107
1045	DUMMY	275	233
1046	DUMMY	247	233
1047	DUMMY	219	233
1048	DUMMY	191	233
1049	DUMMY	163	233
1050	DUMMY	135	233

No.	Pad name	X	Y
1051	DUMMY	107	233
1052	DUMMY	79	233
1053	DUMMY	51	233
1054	DUMMY	23	233
1055	DUMMY	-23	233
1056	DUMMY	-51	233
1057	DUMMY	-79	233
1058	DUMMY	-107	233
1059	DUMMY	-135	233
1060	DUMMY	-163	233
1061	DUMMY	-191	233
1062	DUMMY	-219	233
1063	DUMMY	-247	233
1064	DUMMY	-275	233
1065	DUMMY	-289	107
1066	DUMMY	-303	233
1067	S480	-317	107
1068	S479	-331	233
1069	S478	-345	107
1070	S477	-359	233
1071	S476	-373	107
1072	S475	-387	233
1073	S474	-401	107
1074	S473	-415	233
1075	S472	-429	107
1076	S471	-443	233
1077	S470	-457	107
1078	S469	-471	233
1079	S468	-485	107
1080	S467	-499	233
1081	S466	-513	107
1082	S465	-527	233
1083	S464	-541	107
1084	S463	-555	233
1085	S462	-569	107
1086	S461	-583	233
1087	S460	-597	107
1088	S459	-611	233
1089	S458	-625	107
1090	S457	-639	233
1091	S456	-653	107
1092	S455	-667	233
1093	S454	-681	107
1094	S453	-695	233
1095	S452	-709	107
1096	S451	-723	233
1097	S450	-737	107
1098	S449	-751	233
1099	S448	-765	107
1100	S447	-779	233

No.	Pad name	X	Y
1101	S446	-793	107
1102	S445	-807	233
1103	S444	-821	107
1104	S443	-835	233
1105	S442	-849	107
1106	S441	-863	233
1107	S440	-877	107
1108	S439	-891	233
1109	S438	-905	107
1110	S437	-919	233
1111	S436	-933	107
1112	S435	-947	233
1113	S434	-961	107
1114	S433	-975	233
1115	S432	-989	107
1116	S431	-1003	233
1117	S430	-1017	107
1118	S429	-1031	233
1119	S428	-1045	107
1120	S427	-1059	233
1121	S426	-1073	107
1122	S425	-1087	233
1123	S424	-1101	107
1124	S423	-1115	233
1125	S422	-1129	107
1126	S421	-1143	233
1127	S420	-1157	107
1128	S419	-1171	233
1129	S418	-1185	107
1130	S417	-1199	233
1131	S416	-1213	107
1132	S415	-1227	233
1133	S414	-1241	107
1134	S413	-1255	233
1135	S412	-1269	107
1136	S411	-1283	233
1137	S410	-1297	107
1138	S409	-1311	233
1139	S408	-1325	107
1140	S407	-1339	233
1141	S406	-1353	107
1142	S405	-1367	233
1143	S404	-1381	107
1144	S403	-1395	233
1145	S402	-1409	107
1146	S401	-1423	233
1147	S400	-1437	107
1148	S399	-1451	233
1149	S398	-1465	107
1150	S397	-1479	233

No.	Pad name	X	Y
1151	S396	-1493	107
1152	S395	-1507	233
1153	S394	-1521	107
1154	S393	-1535	233
1155	S392	-1549	107
1156	S391	-1563	233
1157	S390	-1577	107
1158	S389	-1591	233
1159	S388	-1605	107
1160	S387	-1619	233
1161	S386	-1633	107
1162	S385	-1647	233
1163	S384	-1661	107
1164	S383	-1675	233
1165	S382	-1689	107
1166	S381	-1703	233
1167	S380	-1717	107
1168	S379	-1731	233
1169	S378	-1745	107
1170	S377	-1759	233
1171	S376	-1773	107
1172	S375	-1787	233
1173	S374	-1801	107
1174	S373	-1815	233
1175	S372	-1829	107
1176	S371	-1843	233
1177	S370	-1857	107
1178	S369	-1871	233
1179	S368	-1885	107
1180	S367	-1899	233
1181	S366	-1913	107
1182	S365	-1927	233
1183	S364	-1941	107
1184	S363	-1955	233
1185	S362	-1969	107
1186	S361	-1983	233
1187	S360	-1997	107
1188	S359	-2011	233
1189	S358	-2025	107
1190	S357	-2039	233
1191	S356	-2053	107
1192	S355	-2067	233
1193	S354	-2081	107
1194	S353	-2095	233
1195	S352	-2109	107
1196	S351	-2123	233
1197	S350	-2137	107
1198	S349	-2151	233
1199	S348	-2165	107
1200	S347	-2179	233

No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1201	S346	-2193	107	1251	S296	-2893	107	1301	S246	-3593	107	1351	S196	-4293	107
1202	S345	-2207	233	1252	S295	-2907	233	1302	S245	-3607	233	1352	S195	-4307	233
1203	S344	-2221	107	1253	S294	-2921	107	1303	S244	-3621	107	1353	S194	-4321	107
1204	S343	-2235	233	1254	S293	-2935	233	1304	S243	-3635	233	1354	S193	-4335	233
1205	S342	-2249	107	1255	S292	-2949	107	1305	S242	-3649	107	1355	S192	-4349	107
1206	S341	-2263	233	1256	S291	-2963	233	1306	S241	-3663	233	1356	S191	-4363	233
1207	S340	-2277	107	1257	S290	-2977	107	1307	S240	-3677	107	1357	S190	-4377	107
1208	S339	-2291	233	1258	S289	-2991	233	1308	S239	-3691	233	1358	S189	-4391	233
1209	S338	-2305	107	1259	S288	-3005	107	1309	S238	-3705	107	1359	S188	-4405	107
1210	S337	-2319	233	1260	S287	-3019	233	1310	S237	-3719	233	1360	S187	-4419	233
1211	S336	-2333	107	1261	S286	-3033	107	1311	S236	-3733	107	1361	S186	-4433	107
1212	S335	-2347	233	1262	S285	-3047	233	1312	S235	-3747	233	1362	S185	-4447	233
1213	S334	-2361	107	1263	S284	-3061	107	1313	S234	-3761	107	1363	S184	-4461	107
1214	S333	-2375	233	1264	S283	-3075	233	1314	S233	-3775	233	1364	S183	-4475	233
1215	S332	-2389	107	1265	S282	-3089	107	1315	S232	-3789	107	1365	S182	-4489	107
1216	S331	-2403	233	1266	S281	-3103	233	1316	S231	-3803	233	1366	S181	-4503	233
1217	S330	-2417	107	1267	S280	-3117	107	1317	S230	-3817	107	1367	S180	-4517	107
1218	S329	-2431	233	1268	S279	-3131	233	1318	S229	-3831	233	1368	S179	-4531	233
1219	S328	-2445	107	1269	S278	-3145	107	1319	S228	-3845	107	1369	S178	-4545	107
1220	S327	-2459	233	1270	S277	-3159	233	1320	S233	-3859	233	1370	S177	-4559	233
1221	S326	-2473	107	1271	S276	-3173	107	1321	S226	-3873	107	1371	S176	-4573	107
1222	S325	-2487	233	1272	S275	-3187	233	1322	S225	-3887	233	1372	S175	-4587	233
1223	S324	-2501	107	1273	S274	-3201	107	1323	S224	-3901	107	1373	S174	-4601	107
1224	S323	-2515	233	1274	S273	-3215	233	1324	S223	-3915	233	1374	S173	-4615	233
1225	S322	-2529	107	1275	S272	-3229	107	1325	S222	-3929	107	1375	S172	-4629	107
1226	S321	-2543	233	1276	S271	-3243	233	1326	S221	-3943	233	1376	S171	-4643	233
1227	S320	-2557	107	1277	S270	-3257	107	1327	S220	-3957	107	1377	S170	-4657	107
1228	S319	-2571	233	1278	S269	-3271	233	1328	S219	-3971	233	1378	S169	-4671	233
1229	S318	-2585	107	1279	S268	-3285	107	1329	S218	-3985	107	1379	S168	-4685	107
1230	S317	-2599	233	1280	S267	-3299	233	1330	S217	-3999	233	1380	S167	-4699	233
1231	S316	-2613	107	1281	S266	-3313	107	1331	S216	-4013	107	1381	S166	-4713	107
1232	S315	-2627	233	1282	S265	-3327	233	1332	S215	-4027	233	1382	S165	-4727	233
1233	S314	-2641	107	1283	S264	-3341	107	1333	S214	-4041	107	1383	S164	-4741	107
1234	S313	-2655	233	1284	S263	-3355	233	1334	S213	-4055	233	1384	S163	-4755	233
1235	S312	-2669	107	1285	S262	-3369	107	1335	S212	-4069	107	1385	S162	-4769	107
1236	S311	-2683	233	1286	S261	-3383	233	1336	S211	-4083	233	1386	S161	-4783	233
1237	S310	-2697	107	1287	S260	-3397	107	1337	S210	-4097	107	1387	S160	-4797	107
1238	S309	-2711	233	1288	S259	-3411	233	1338	S209	-4111	233	1388	S159	-4811	233
1239	S308	-2725	107	1289	S258	-3425	107	1339	S208	-4125	107	1389	S158	-4825	107
1240	S307	-2739	233	1290	S257	-3439	233	1340	S207	-4139	233	1390	S157	-4839	233
1241	S306	-2753	107	1291	S256	-3453	107	1341	S206	-4153	107	1391	S156	-4853	107
1242	S305	-2767	233	1292	S255	-3467	233	1342	S205	-4167	233	1392	S155	-4867	233
1243	S304	-2781	107	1293	S254	-3481	107	1343	S204	-4181	107	1393	S154	-4881	107
1244	S303	-2795	233	1294	S253	-3495	233	1344	S203	-4195	233	1394	S153	-4895	233
1245	S302	-2809	107	1295	S252	-3509	107	1345	S202	-4209	107	1395	S152	-4909	107
1246	S301	-2823	233	1296	S251	-3523	233	1346	S201	-4223	233	1396	S151	-4923	233
1247	S300	-2837	107	1297	S250	-3537	107	1347	S200	-4237	107	1397	S150	-4937	107
1248	S299	-2851	233	1298	S249	-3551	233	1348	S199	-4251	233	1398	S149	-4951	233
1249	S298	-2865	107	1299	S248	-3565	107	1349	S198	-4265	107	1399	S148	-4965	107
1250	S297	-2879	233	1300	S247	-3579	233	1350	S197	-4279	233	1400	S147	-4979	233

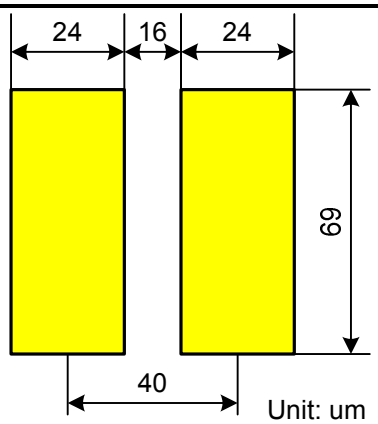
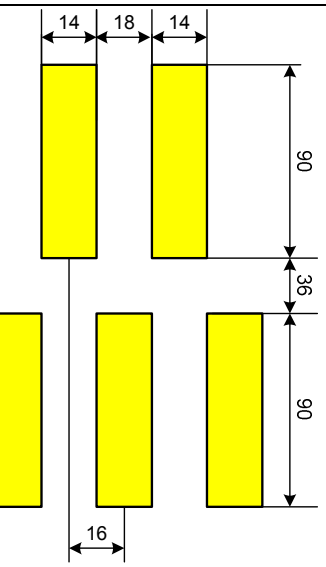
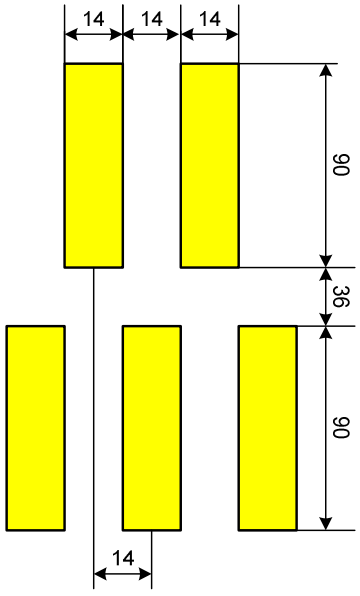
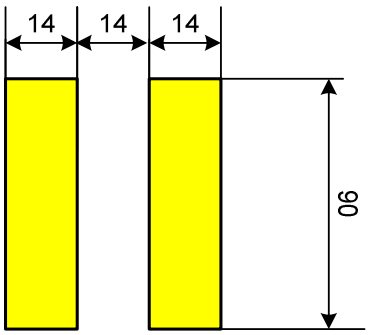
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1401	S146	-4993	107	1451	S96	-5693	107	1501	S46	-6393	107	1551	G1	-7099	107
1402	S145	-5007	233	1452	S95	-5707	233	1502	S45	-6407	233	1552	G3	-7115	233
1403	S144	-5021	107	1453	S94	-5721	107	1503	S44	-6421	107	1553	G5	-7131	107
1404	S143	-5035	233	1454	S93	-5735	233	1504	S43	-6435	233	1554	G7	-7147	233
1405	S142	-5049	107	1455	S92	-5749	107	1505	S42	-6449	107	1555	G9	-7163	107
1406	S141	-5063	233	1456	S91	-5763	233	1506	S41	-6463	233	1556	G11	-7179	233
1407	S140	-5077	107	1457	S90	-5777	107	1507	S40	-6477	107	1557	G13	-7195	107
1408	S139	-5091	233	1458	S89	-5791	233	1508	S39	-6491	233	1558	G15	-7211	233
1409	S138	-5105	107	1459	S88	-5805	107	1509	S38	-6505	107	1559	G17	-7227	107
1410	S137	-5119	233	1460	S87	-5819	233	1510	S37	-6519	233	1560	G19	-7243	233
1411	S136	-5133	107	1461	S86	-5833	107	1511	S36	-6533	107	1561	G21	-7259	107
1412	S135	-5147	233	1462	S85	-5847	233	1512	S35	-6547	233	1562	G23	-7275	233
1413	S134	-5161	107	1463	S84	-5861	107	1513	S34	-6561	107	1563	G25	-7291	107
1414	S133	-5175	233	1464	S83	-5875	233	1514	S33	-6575	233	1564	G27	-7307	233
1415	S132	-5189	107	1465	S82	-5889	107	1515	S32	-6589	107	1565	G29	-7323	107
1416	S131	-5203	233	1466	S81	-5903	233	1516	S31	-6603	233	1566	G31	-7339	233
1417	S130	-5217	107	1467	S80	-5917	107	1517	S30	-6617	107	1567	G33	-7355	107
1418	S129	-5231	233	1468	S79	-5931	233	1518	S29	-6631	233	1568	G35	-7371	233
1419	S128	-5245	107	1469	S78	-5945	107	1519	S28	-6645	107	1569	G37	-7387	107
1420	S127	-5259	233	1470	S77	-5959	233	1520	S27	-6659	233	1570	G39	-7403	233
1421	S126	-5273	107	1471	S76	-5973	107	1521	S26	-6673	107	1571	G41	-7419	107
1422	S125	-5287	233	1472	S75	-5987	233	1522	S25	-6687	233	1572	G43	-7435	233
1423	S124	-5301	107	1473	S74	-6001	107	1523	S24	-6701	107	1573	G45	-7451	107
1424	S123	-5315	233	1474	S73	-6015	233	1524	S23	-6715	233	1574	G47	-7467	233
1425	S122	-5329	107	1475	S72	-6029	107	1525	S22	-6729	107	1575	G49	-7483	107
1426	S121	-5343	233	1476	S71	-6043	233	1526	S21	-6743	233	1576	G51	-7499	233
1427	S120	-5357	107	1477	S70	-6057	107	1527	S20	-6757	107	1577	G53	-7515	107
1428	S119	-5371	233	1478	S69	-6071	233	1528	S19	-6771	233	1578	G55	-7531	233
1429	S118	-5385	107	1479	S68	-6085	107	1529	S18	-6785	107	1579	G57	-7547	107
1430	S117	-5399	233	1480	S67	-6099	233	1530	S17	-6799	233	1580	G59	-7563	233
1431	S116	-5413	107	1481	S66	-6113	107	1531	S16	-6813	107	1581	G61	-7579	107
1432	S115	-5427	233	1482	S65	-6127	233	1532	S15	-6827	233	1582	G63	-7595	233
1433	S114	-5441	107	1483	S64	-6141	107	1533	S14	-6841	107	1583	G65	-7611	107
1434	S113	-5455	233	1484	S63	-6155	233	1534	S13	-6855	233	1584	G67	-7627	233
1435	S112	-5469	107	1485	S62	-6169	107	1535	S12	-6869	107	1585	G69	-7643	107
1436	S107	-5483	233	1486	S61	-6183	233	1536	S11	-6883	233	1586	G71	-7659	233
1437	S110	-5497	107	1487	S60	-6197	107	1537	S10	-6897	107	1587	G73	-7675	107
1438	S109	-5511	233	1488	S59	-6211	233	1538	S9	-6911	233	1588	G75	-7691	233
1439	S108	-5525	107	1489	S58	-6225	107	1539	S8	-6925	107	1589	G77	-7707	107
1440	S107	-5539	233	1490	S57	-6239	233	1540	S7	-6939	233	1590	G79	-7723	233
1441	S106	-5553	107	1491	S56	-6253	107	1541	S6	-6953	107	1591	G81	-7739	107
1442	S105	-5567	233	1492	S55	-6267	233	1542	S5	-6967	233	1592	G83	-7755	233
1443	S104	-5581	107	1493	S54	-6281	107	1543	S4	-6981	107	1593	G85	-7771	107
1444	S103	-5595	233	1494	S53	-6295	233	1544	S3	-6995	233	1594	G87	-7787	233
1445	S102	-5609	107	1495	S52	-6309	107	1545	S2	-7009	107	1595	G89	-7803	107
1446	S101	-5623	233	1496	S51	-6323	233	1546	S1	-7023	233	1596	G91	-7819	233
1447	S100	-5637	107	1497	S50	-6337	107	1547	DUMMY	-7037	107	1597	G93	-7835	107
1448	S99	-5651	233	1498	S49	-6351	233	1548	DUMMY	-7051	233	1598	G95	-7851	233
1449	S98	-5665	107	1499	S48	-6365	107	1549	DUMMY	-7067	107	1599	G97	-7867	107
1450	S97	-5679	233	1500	S47	-6379	233	1550	DUMMY	-7083	233	1600	G99	-7883	233

No.	Pad name	X	Y
1601	G101	-7899	107
1602	G103	-7915	233
1603	G105	-7931	107
1604	G107	-7947	233
1605	G109	-7963	107
1606	G107	-7979	233
1607	G113	-7995	107
1608	G115	-8011	233
1609	G117	-8027	107
1610	G119	-8043	233
1611	G121	-8059	107
1612	G123	-8075	233
1613	G125	-8091	107
1614	G127	-8107	233
1615	G129	-8123	107
1616	G131	-8139	233
1617	G133	-8155	107
1618	G135	-8171	233
1619	G137	-8187	107
1620	G139	-8203	233
1621	G141	-8219	107
1622	G143	-8235	233
1623	G145	-8251	107
1624	G147	-8267	233
1625	G149	-8283	107
1626	G151	-8299	233
1627	G153	-8315	107
1628	G155	-8331	233
1629	G157	-8347	107
1630	G159	-8363	233
1631	G161	-8379	107
1632	G163	-8395	233
1633	G165	-8411	107
1634	G167	-8427	233
1635	G169	-8443	107
1636	G171	-8459	233
1637	G173	-8475	107
1638	G175	-8491	233
1639	G177	-8507	107
1640	G179	-8523	233
1641	G181	-8539	107
1642	G183	-8555	233
1643	G185	-8571	107
1644	G187	-8587	233
1645	G189	-8603	107
1646	G191	-8619	233
1647	G193	-8635	107
1648	G195	-8651	233
1649	G197	-8667	107
1650	G199	-8683	233

No.	Pad name	X	Y
1651	G201	-8699	107
1652	G203	-8715	233
1653	G205	-8731	107
1654	G207	-8747	233
1655	G209	-8763	107
1656	G211	-8779	233
1657	G213	-8795	107
1658	G215	-8811	233
1659	G217	-8827	107
1660	G219	-8843	233
1661	G221	-8859	107
1662	G223	-8875	233
1663	G225	-8891	107
1664	G233	-8907	233
1665	G229	-8923	107
1666	G231	-8939	233
1667	G233	-8955	107
1668	G235	-8971	233
1669	G237	-8987	107
1670	G239	-9003	233
1671	DUMMY	-9019	107
1672	DUMMY	-9035	233

Alignment mark	X	Y
A1	-9200	225
A2	9200	225

BUMP Size

Input Pad (NO.1 ~ NO.436)	
Output Pad (NO.437 ~ NO.1672)	 No. 437 ~ No. 561 No.1549 ~ No.1672 Unit: um  No. 562 ~ No.1045 No.1065 ~ No.1548  No.1046 ~ No.1054 No.1055 ~ No.1064 Unit: um

6. Block Function Description

MCU System Interface

ILI9342C provides four kinds of MCU system interface with 8080-Ⅰ/8080-Ⅱ series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	1	0	0	80 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0]
0	1	1	0	80 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0]
0	1	0	1	80 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0]
0	1	1	1	80 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0]
1	1	0	1	3-wire 9-bit data serial interface Ⅰ	SDA: In/OUT	
1	1	1	1	4-wire 8-bit data serial interface Ⅰ	SDA: In/OUT	
0	0	1	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10] D[8:1]
0	0	0	0	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10],
0	0	1	1	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
0	0	0	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]

In 8080-Ⅰ/8080-Ⅱ series parallel interface, the registers are accessed by the D[17:0] data pins.

8080-Ⅰ Series				8080-Ⅱ Series				Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"	⎍	"L"	"L"	"H"	⎍	Write command
"L"	"H"	⎍	"H"	"L"	"H"	⎍	"H"	Read parameter
"L"	"H"	"H"	⎍	"L"	"H"	"H"	⎍	Write parameter

Parallel RGB Interface

ILI9342C also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 320(RGB) x240 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9342C can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as DDVDH, DDVDL, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9342C incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 960-output source driver (S1~S960), 240-output gate driver (G1~G240), and VCOM signal.

7. Function Description

7.1. MCU interfaces

ILI9342C provides the 8-/9-/16-/18-bit parallel system interface for 8080-Ⅰ/8080-Ⅱ series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use	
					Register/Content	GRAM
0	1	0	0	80 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0]
0	1	1	0	80 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0]
0	1	0	1	80 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0]
0	1	1	1	80 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0]
1	1	0	1	3-wire 9-bit data serial interface Ⅰ	SDA: In/OUT	
1	1	1	1	4-wire 8-bit data serial interface Ⅰ	SDA: In/OUT	
0	0	1	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10] D[8:1]
0	0	0	0	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10],
0	0	1	1	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
0	0	0	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]

7.1.2. 8080-Ⅰ Series Parallel Interface

ILI9342C can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅰ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9342C chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9342C latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅰ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. Interface bus width can be selected by IM [3:0] bits.

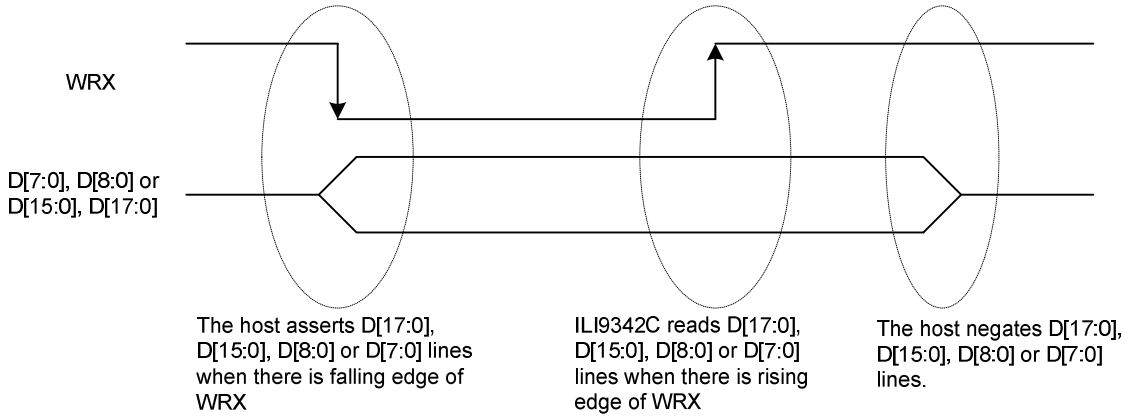
The selection of 8080-Ⅰ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8080 MCU 8-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	0	8080 MCU 16-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	0	1	8080 MCU 9-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	1	8080 MCU 18-bit bus interface Ⅰ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

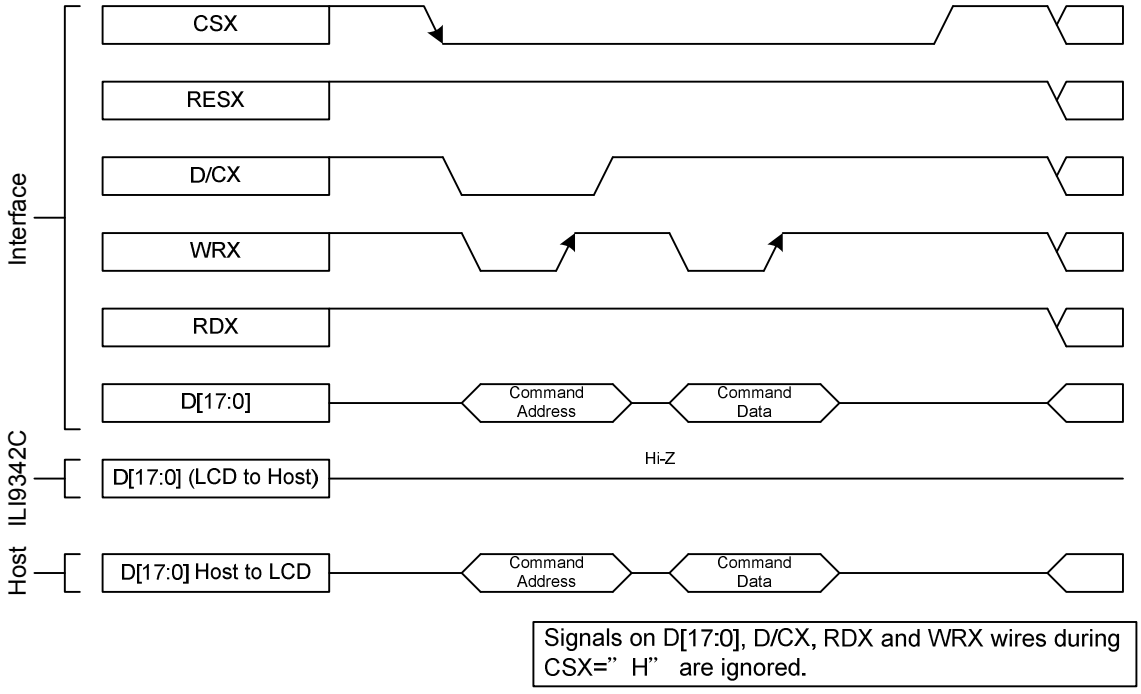
7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅰ MCU interface.



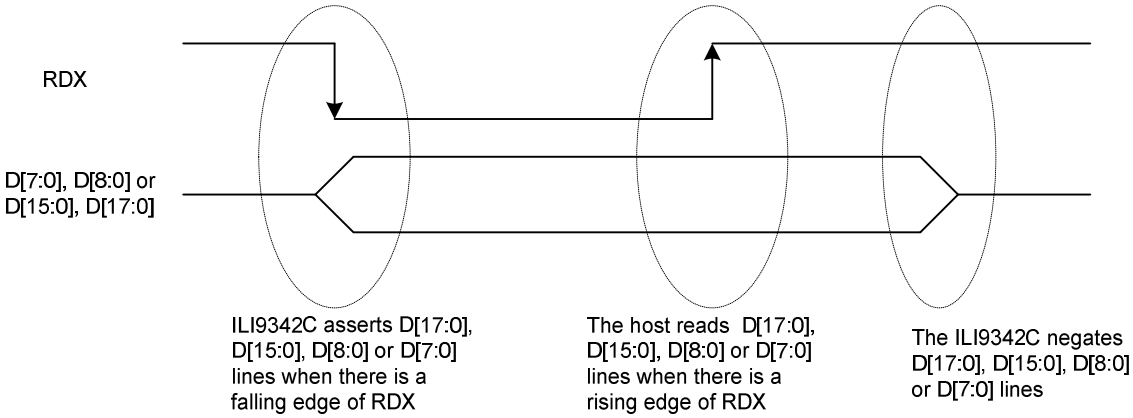
Note: WRX is an unsynchronized signal (It can be stopped)



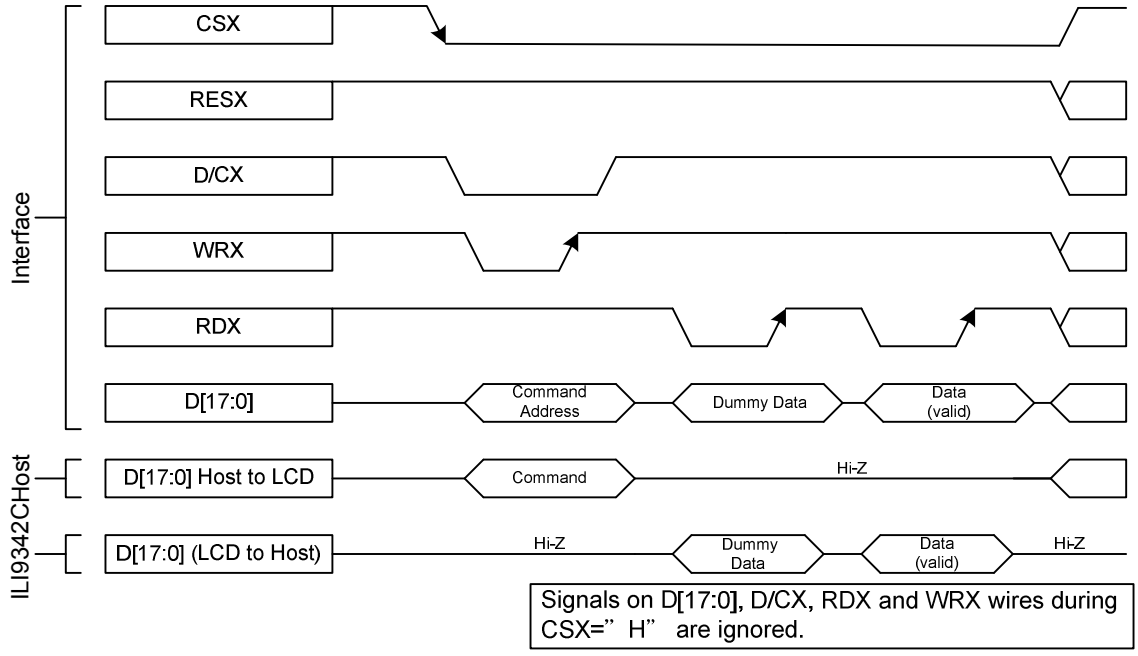
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- Ⅰ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.5. 8080-Ⅱ Parallel Interface

ILI9342C can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9342C chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9342C latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅱ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. Interface bus width can be selected by IM [3:0] bits.

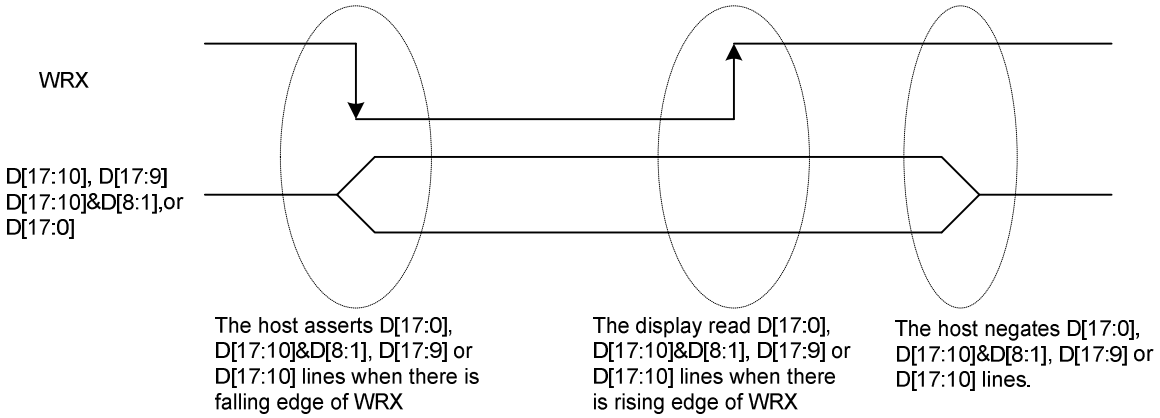
The selection of 8080-Ⅱ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	0	1	0	8080 MCU 16-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	0	8080 MCU 8-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 9-bit bus interface Ⅱ	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

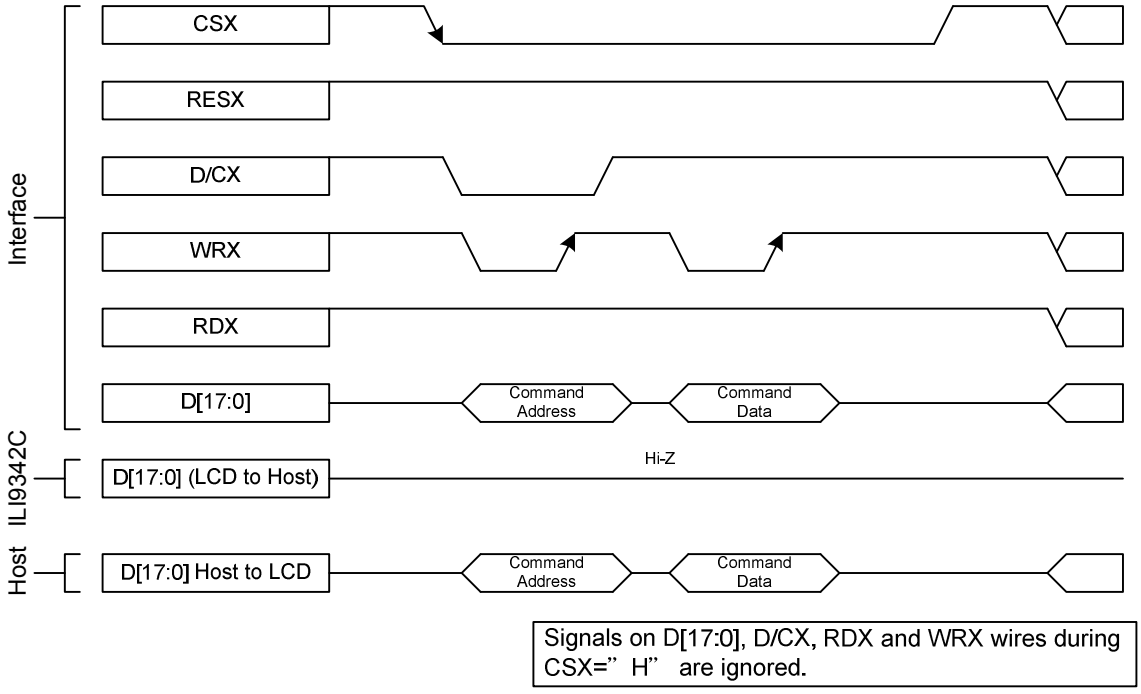
7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅱ MCU interface.



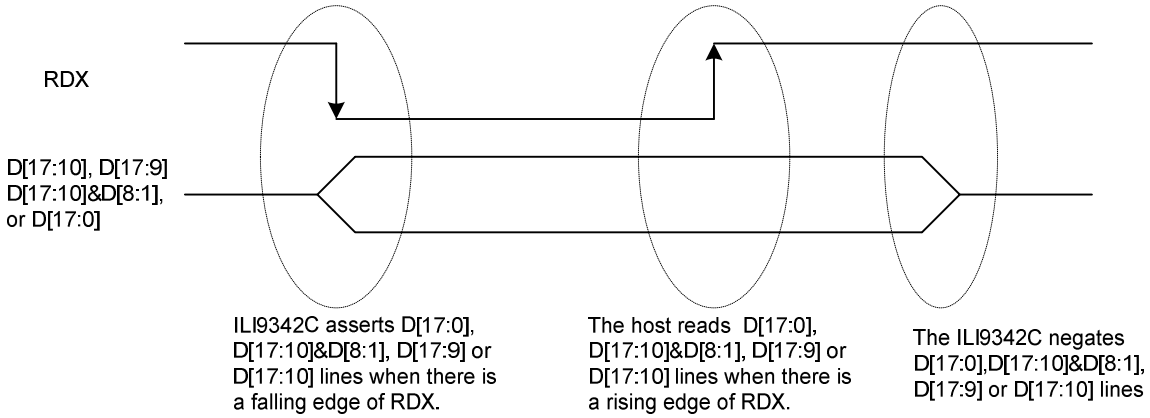
Note: WRX is an unsynchronized signal (It can be stopped)



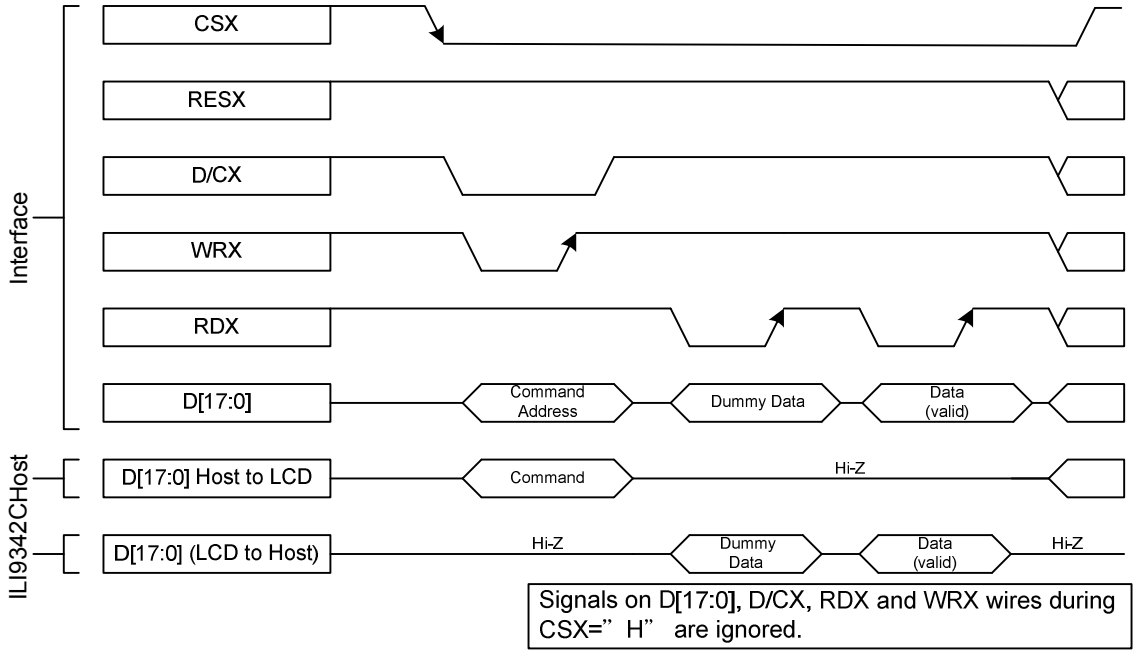
7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅱ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

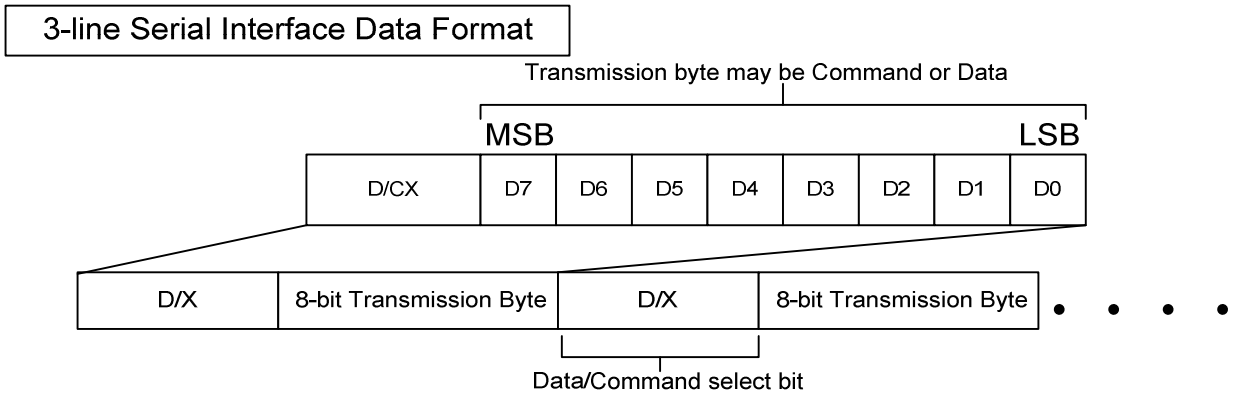
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
1	1	0	1	3-line serial interface	"L"	-	⎍	Read/Write command, parameter or display data.
1	1	1	1	4-line serial interface	"L"	'H/L"	⎍	Read/Write command, parameter or display data.

ILI9342C supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9342C. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

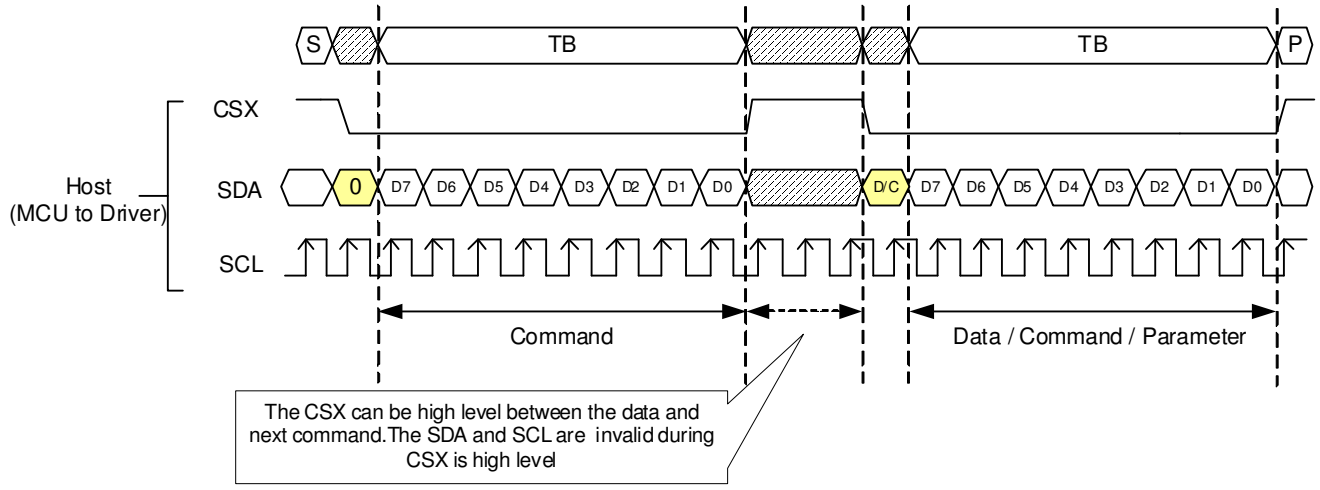
The write mode of the interface means that host writes commands or data to ILI9342C. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9342C and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

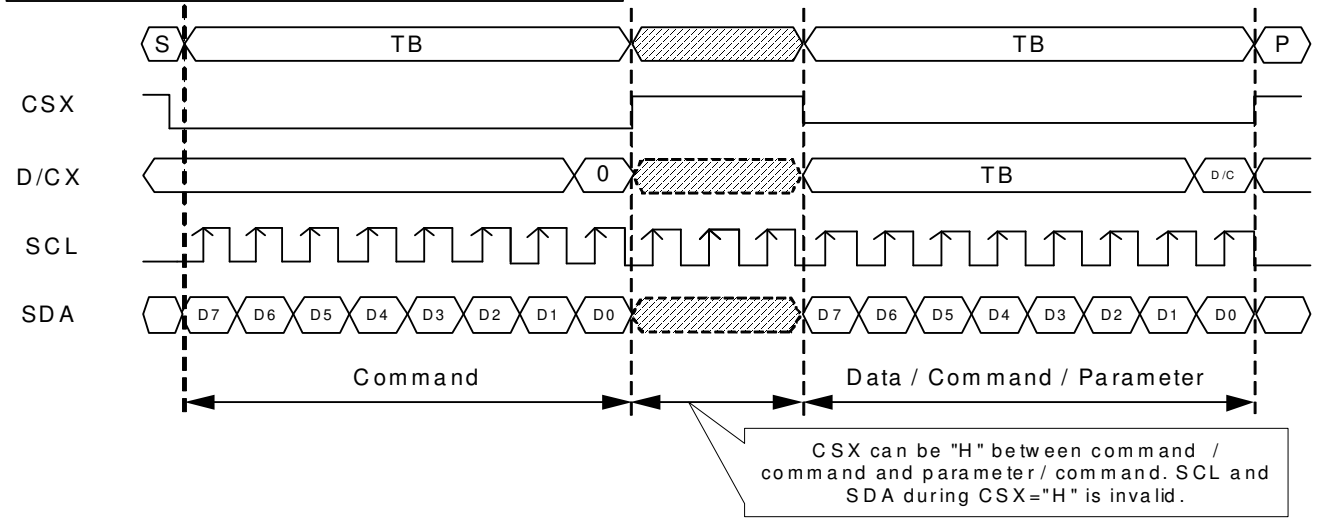


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9342C on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

3-line Serial Interface Protocol



4-line Serial Interface Protocol



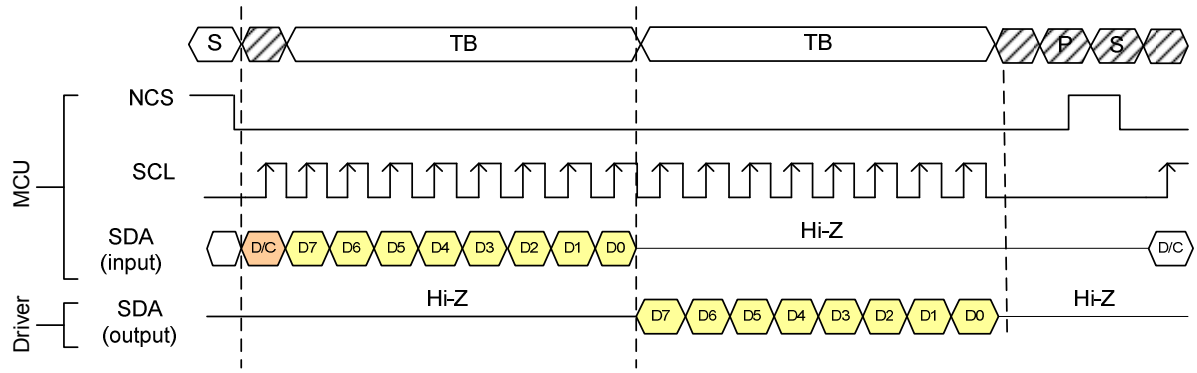
7.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9342C. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9342C latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

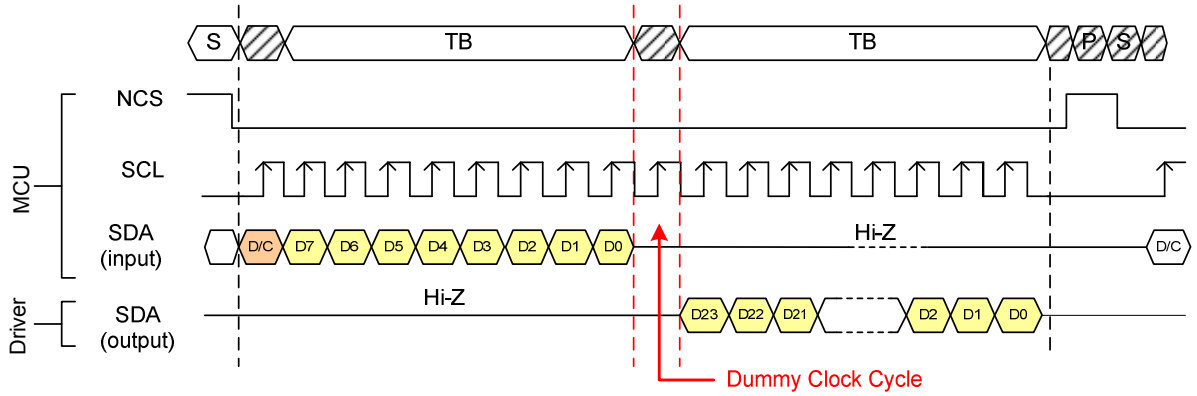
The host read the n-th parameter of the level 2 command by SPI interface need set additional command RD9h at first. Only the first 8-bit parameter will be read out by the serial interface protocol at a time and it will be necessary set RD9h command again for another ordinal number parameter.

3-wire Serial Interface Protocol

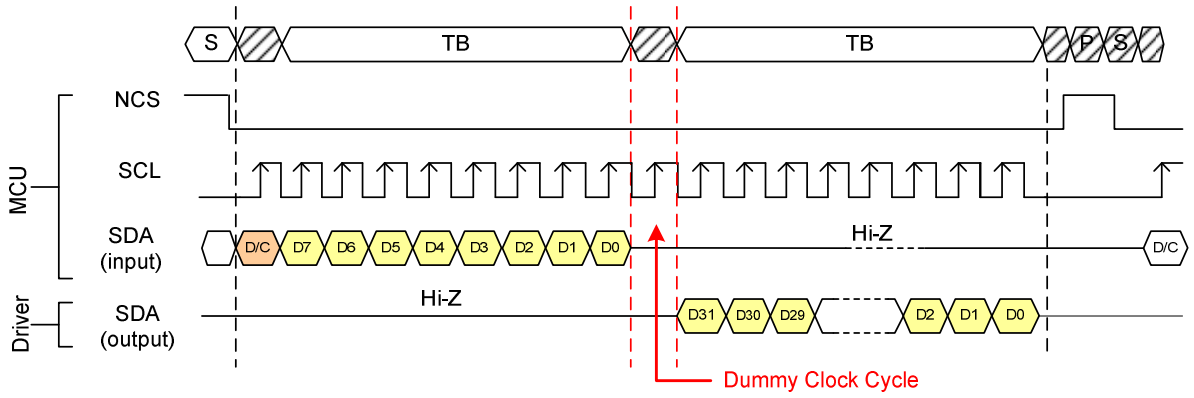
3-line Serial Protocol (for RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



3-line Serial Protocol (for RDDID command: 24-bit read)

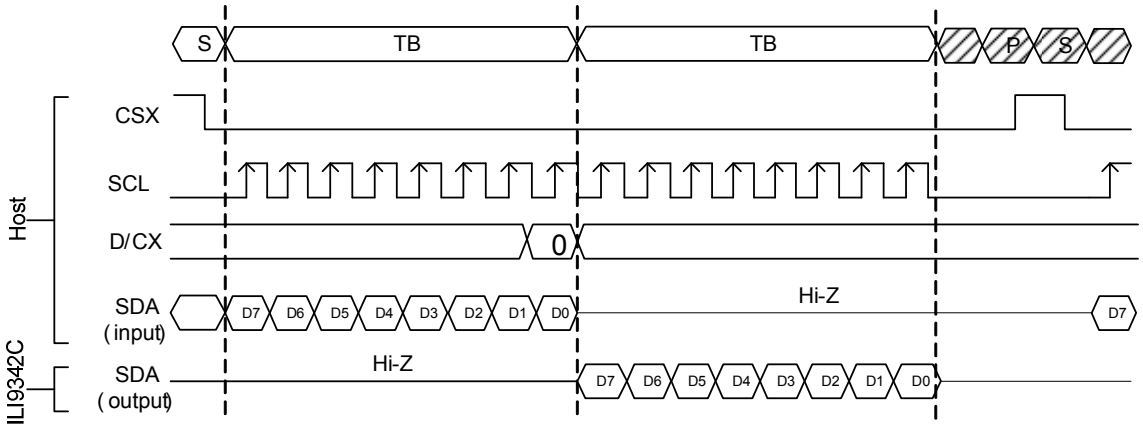


3-line Serial Protocol (for RDDST command: 32-bit read)

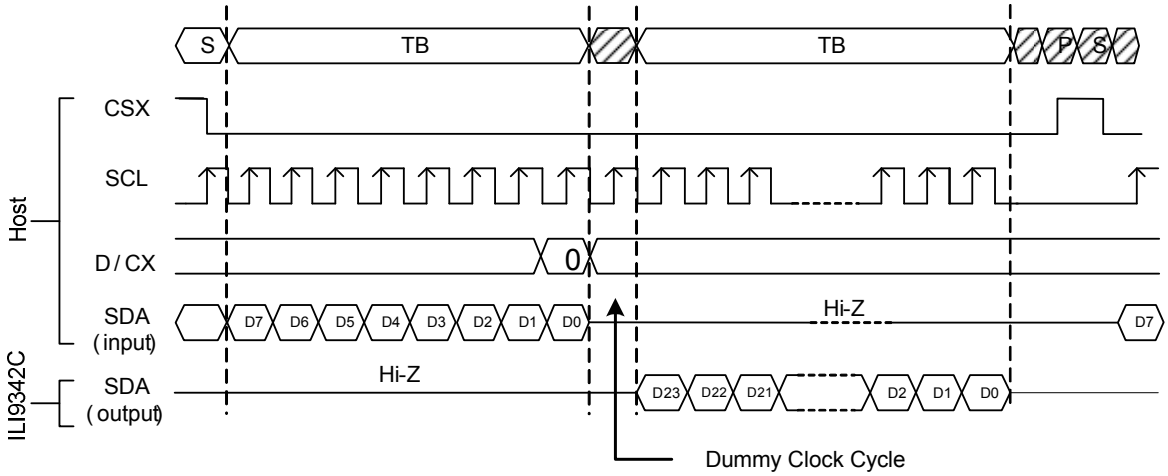


4-wire Serial Interface Protocol

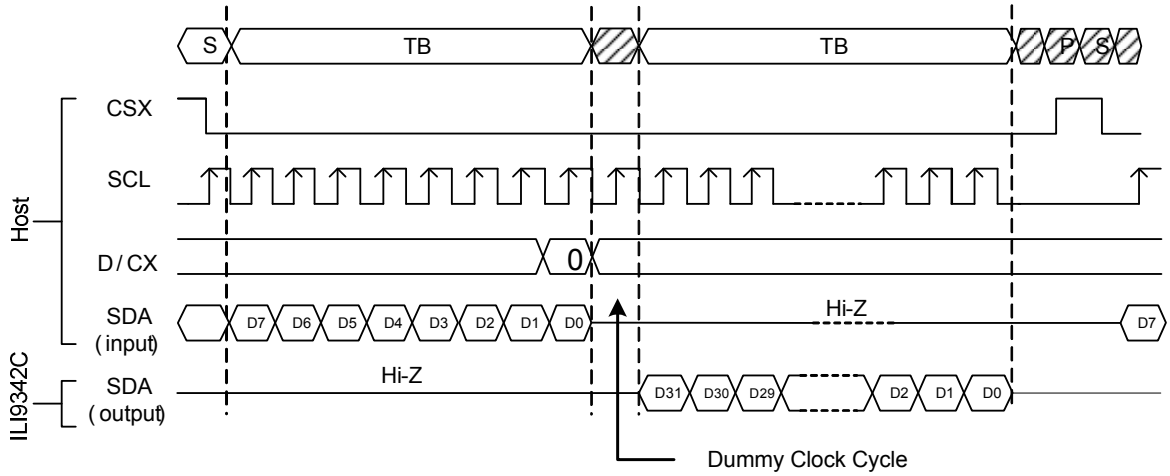
4-line Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



4-line Serial Protocol (for RDDID command 24-bit read)

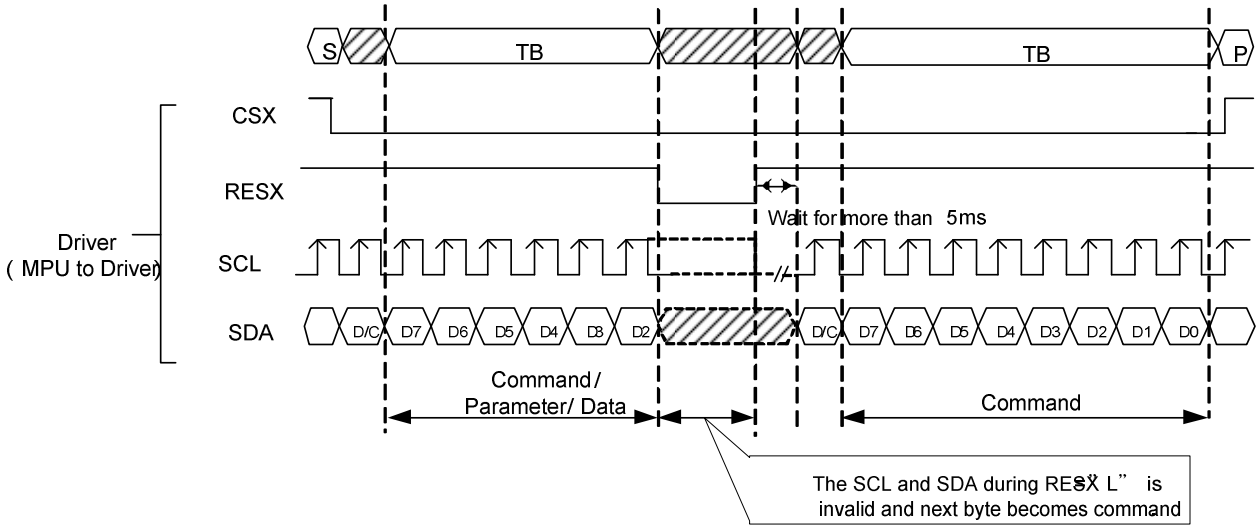


4-line Serial Protocol(for RDDST command 32-bit read)

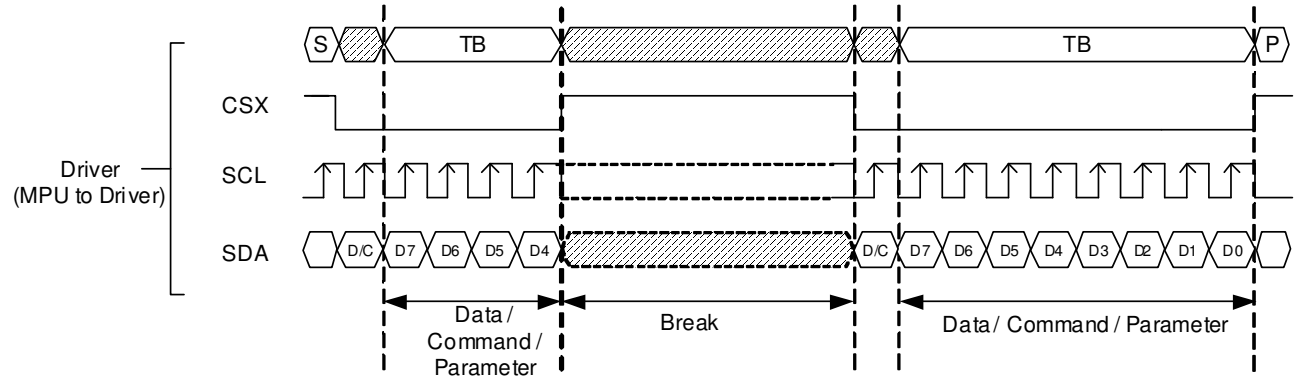


Data Transfer Break and Recovery

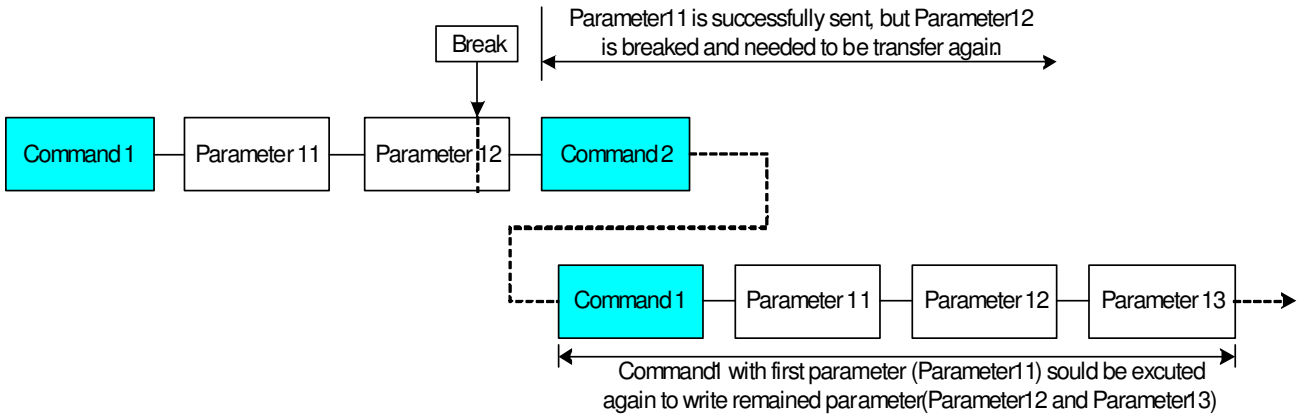
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



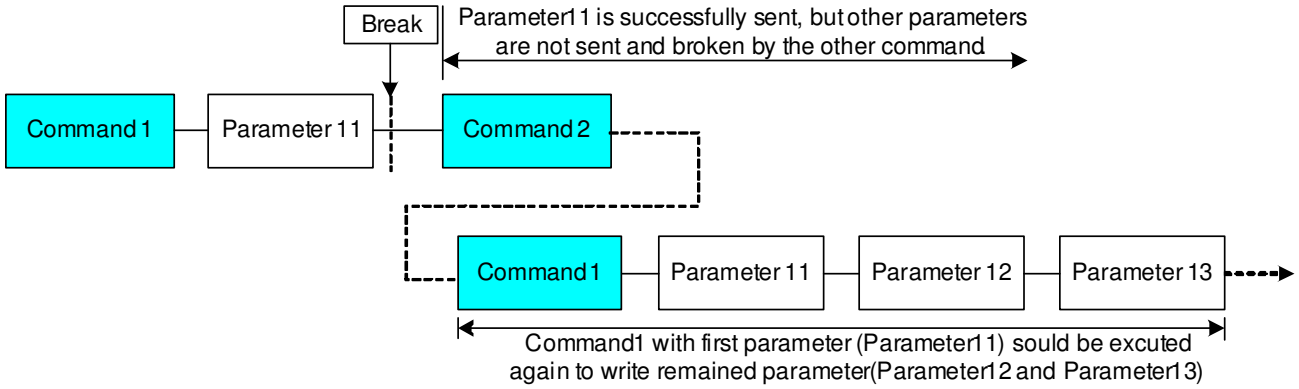
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



7.1.11. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9342C will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

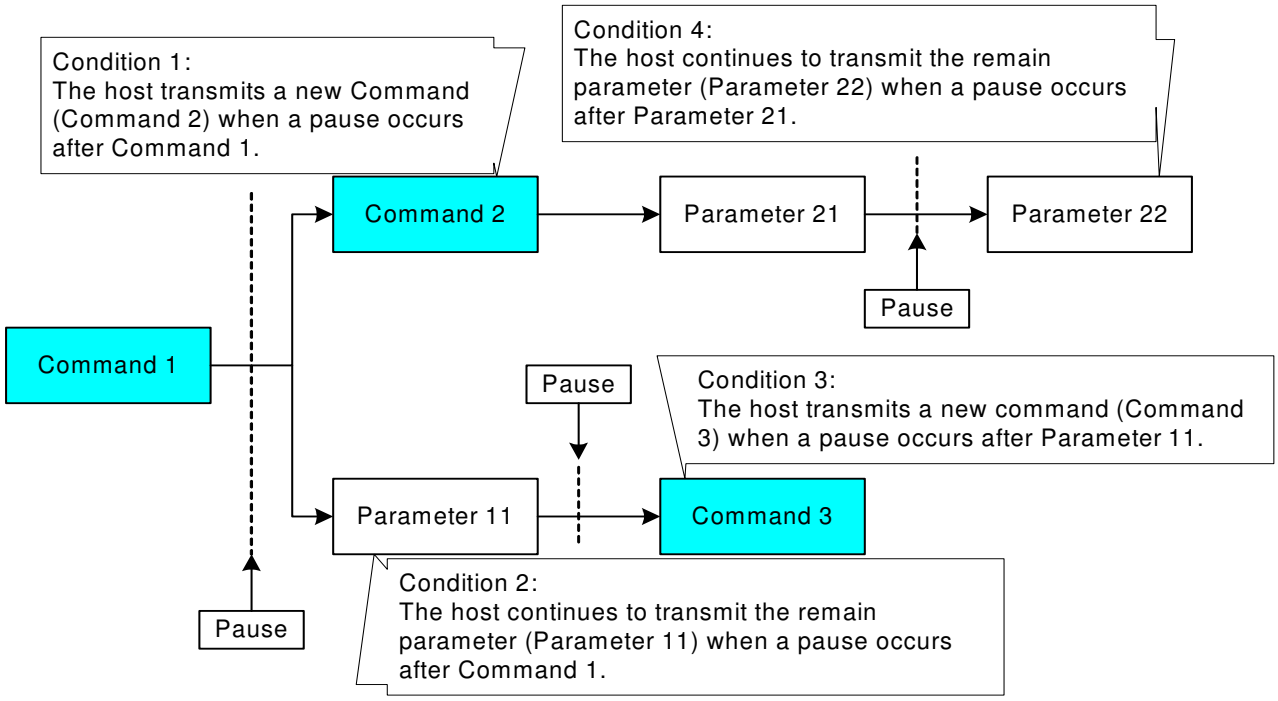
This applies to the following 4 conditions:

1) Command-Pause-Command

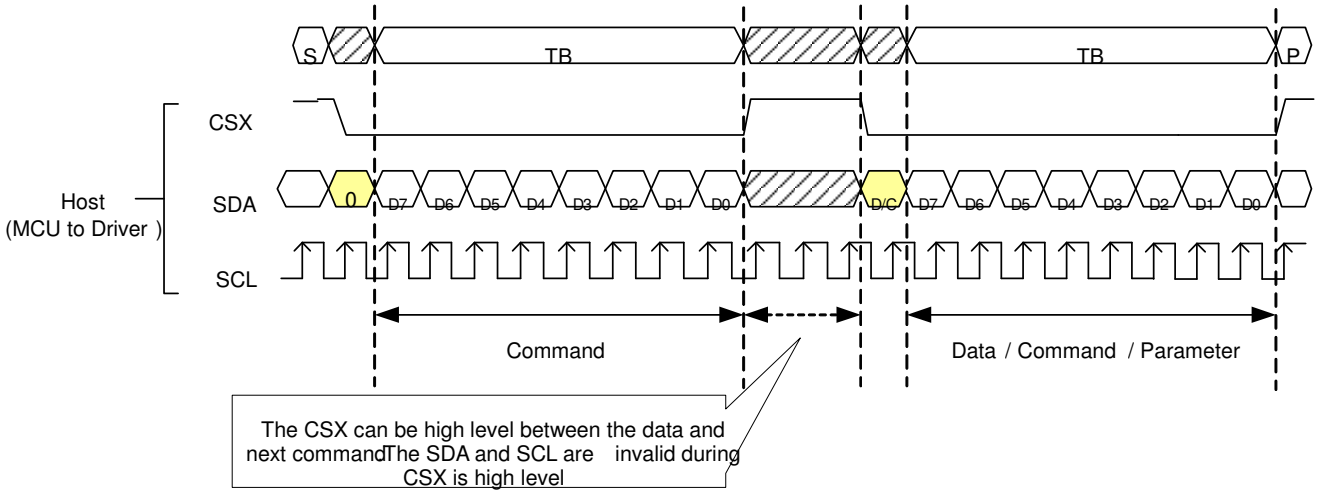
2) Command-Pause-Parameter

3) Parameter-Pause-Command

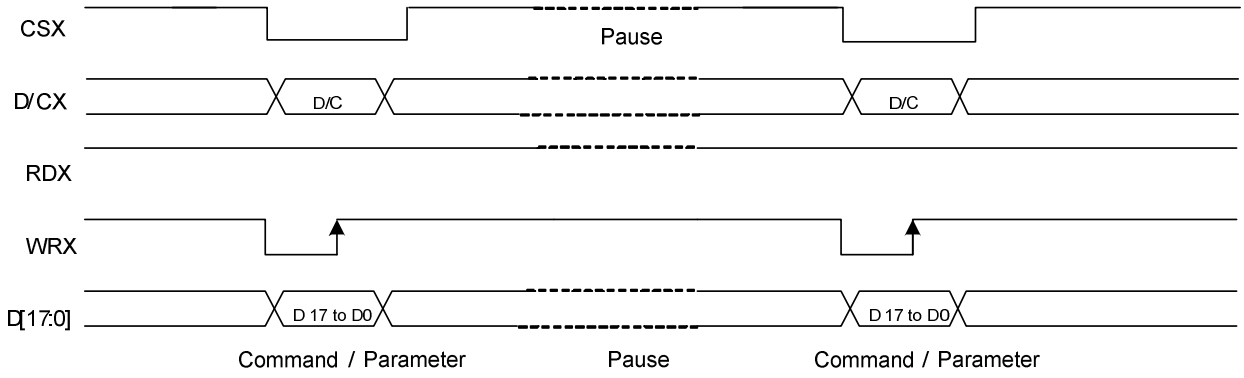
4) Parameter-Pause-Parameter



7.1.12. Serial Interface Pause (3_wire)



7.1.13. Parallel Interface Pause

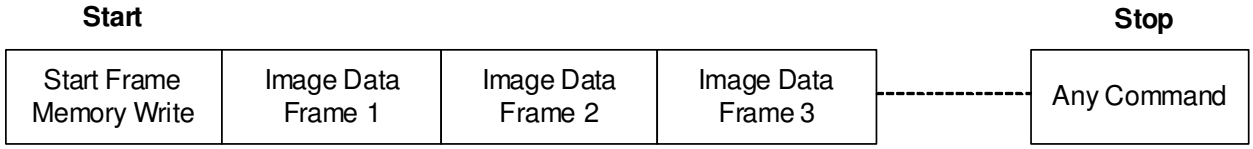


7.1.14. Data Transfer Mode

ILI9342C can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

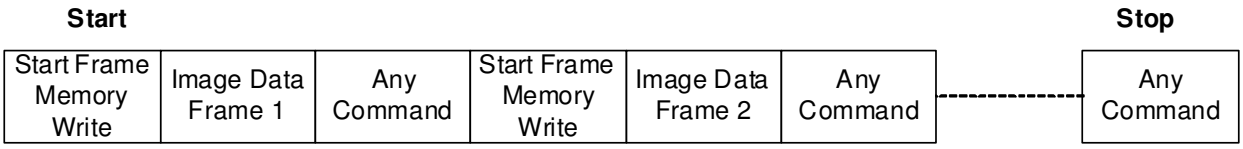
7.1.15. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.16. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9342C has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9342C supports several pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]		RIM	DPI[2:0]			RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	**DE Mode** Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, DB[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[15:0]
1	0	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, DB[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	**SYNC Mode** In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, DB[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[15:0]
1	1	1	1	1	0	6-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, DB[5:0]

18-bit data bus interface (D[17:0] is used), DPI[2:0] = 110, and RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[15:0] is used), DPI[2:0] = 101, and RIM=0

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red / blue color depends on the EPF[1:0] setting

6-bit data bus interface (D[5:0] is used), DPI[2:0] = 110, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[5:0] is used), DPI[2:0] = 101, and RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]	

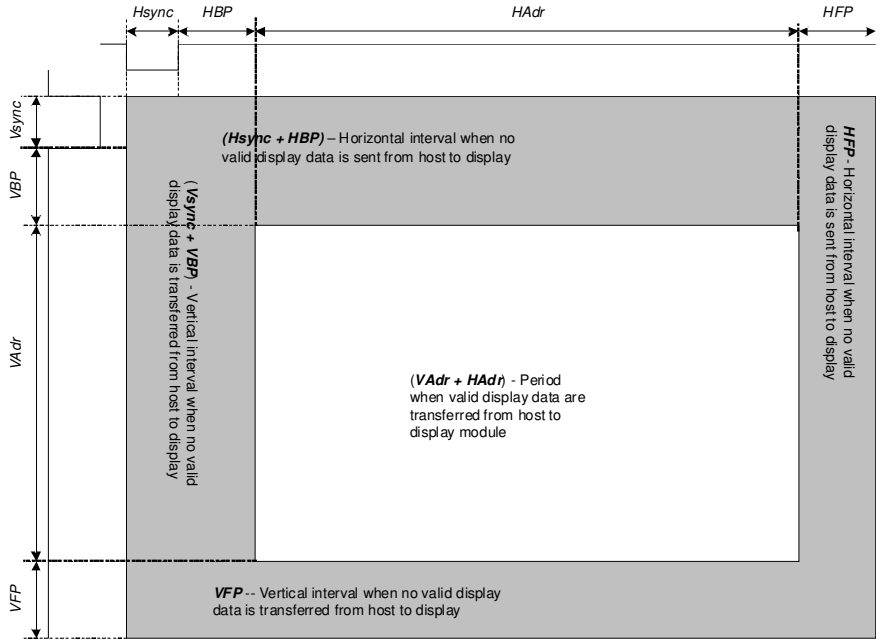
The LSB data of red/blue color depends on the EPF[1:0] setting

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. The DOTCLK cannot be used as continues internal

clock for other functions of the display module. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(By pass mode)*	HBP(BP)		58	68	200	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Note1: HBP setting need to 3 times in RGB 6/6/6 by pass mode. It can set HBP[0:6] in RB5h.

Typical values are setting example when used with panel resolution 320 x 240 (LQVGA), clock frequency 6.35MHz and frame frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction

(Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'h0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h1D (240 lines)

Frame Rate → 70.30Hz

DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 240 + 2) lines x (10 + 20 + 320 + 10) clocks = 6.35MHz

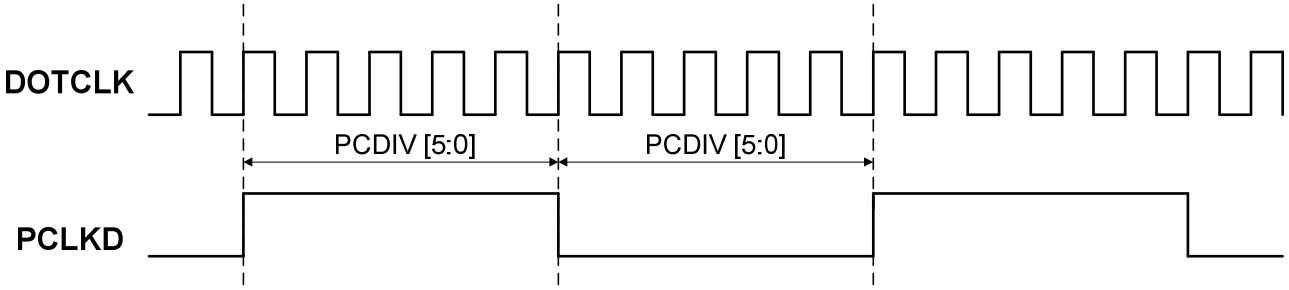
DOTCLK frequency = 6.15MHz

6.35 MHz / 615KHz = 10.32 ☐ Set PCDIV so that PCLK is divided by 10.

external fosc = 6.35 MHz / 10 = 635KHz

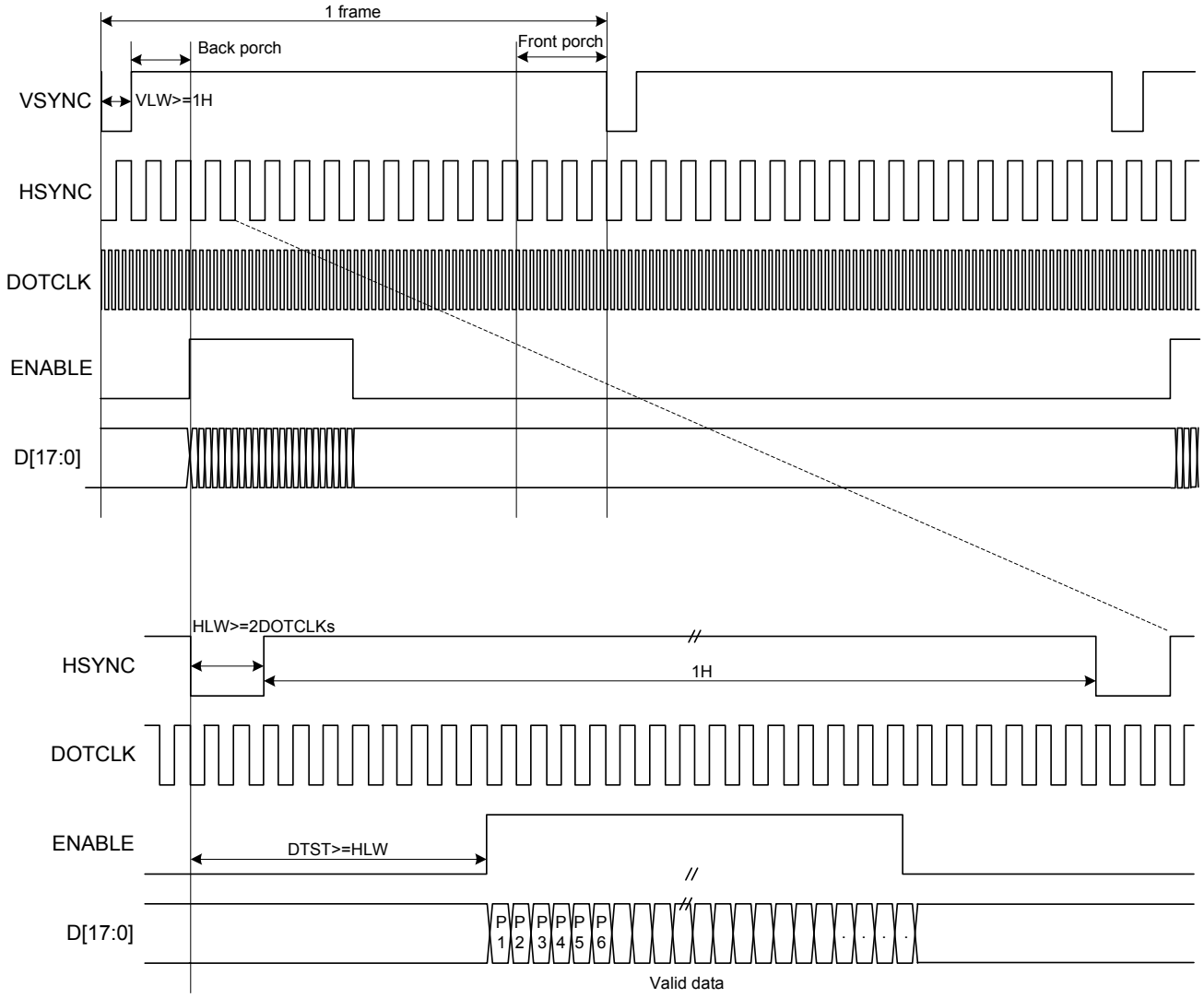
PCDIV = [6.35MHz / 635KHz) / 2] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)

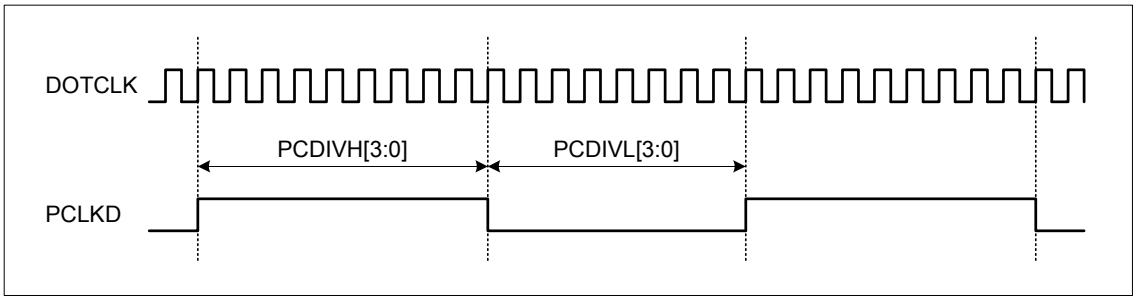


7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



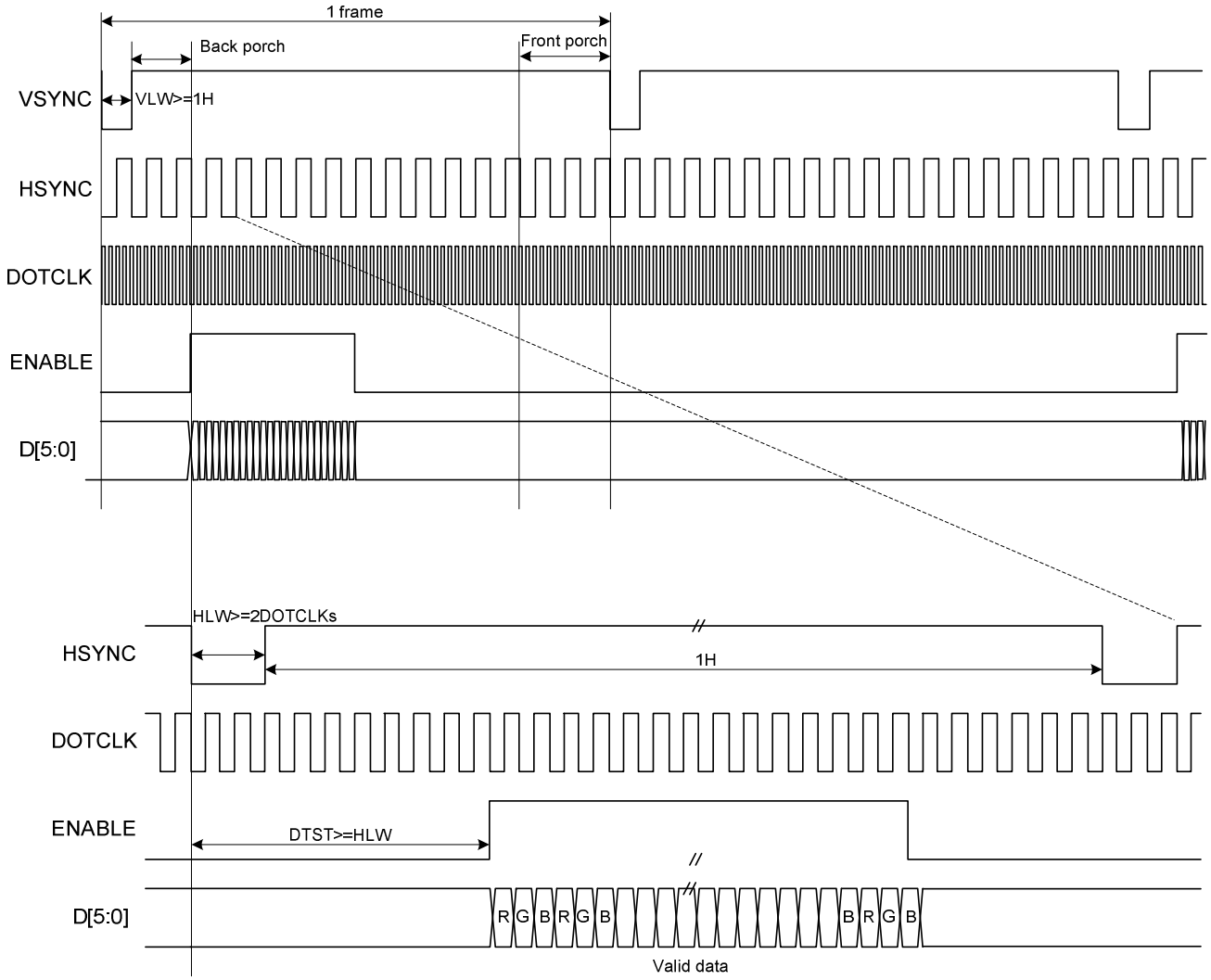
VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time



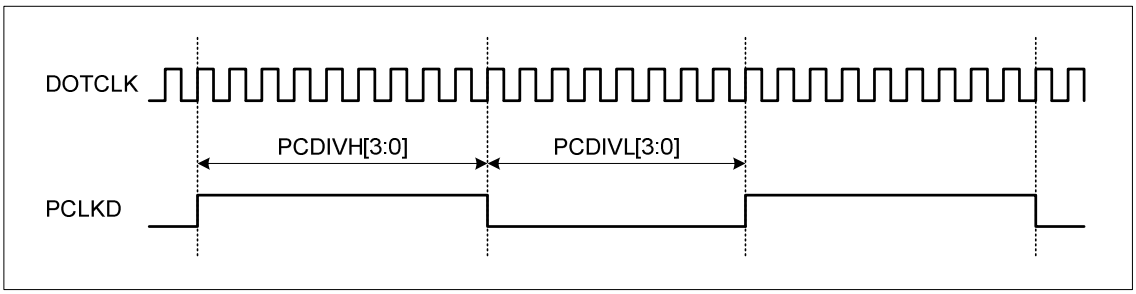
Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

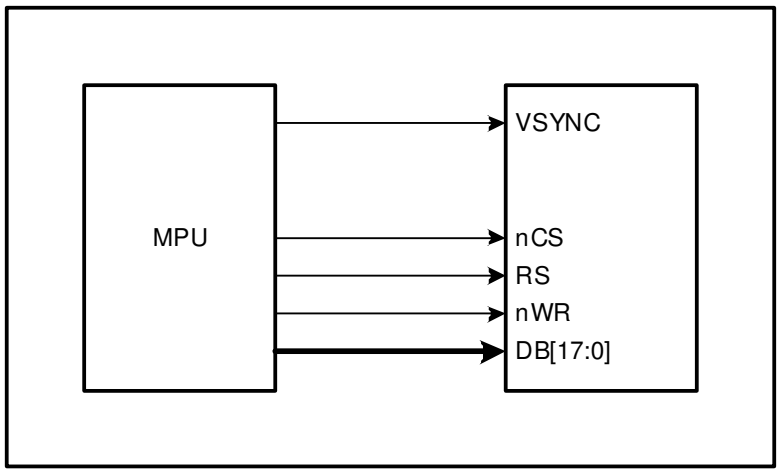
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

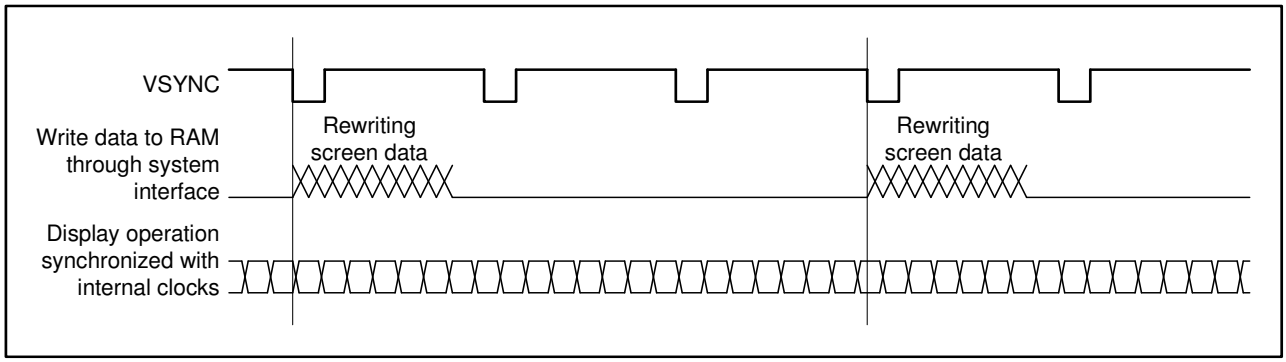
Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

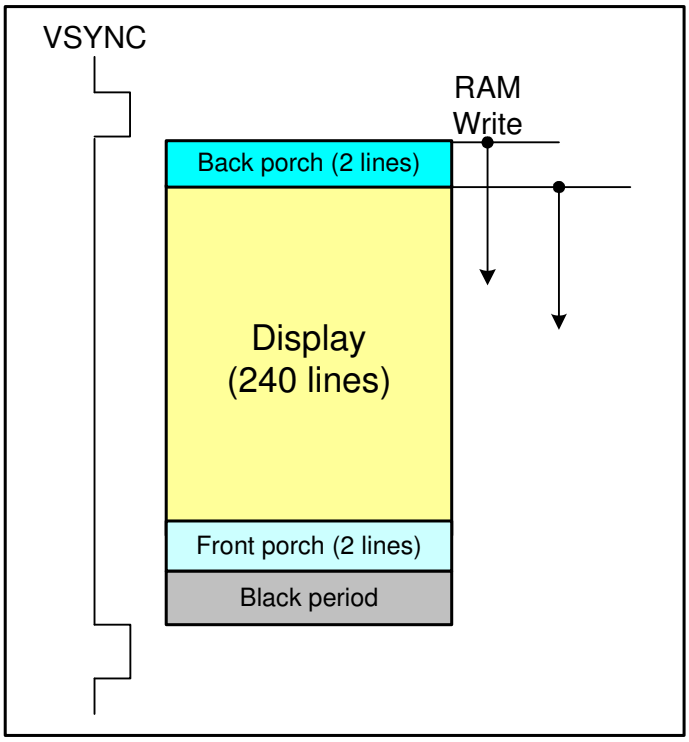
VSYNC Interface

ILI9342C supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{320 \times \text{DisplayLines(NL)}}{[\text{BackPorch(VBP)} + \text{DisplayLines(NL)} - \text{margins}] \times \text{Clocks per line} \times (1/\text{fosc})}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 320 RGB × 240 lines

Lines: 240 lines (NL = 111101)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = 70 x [240+ 2 + 2] x 27 clocks x (1.1/0.9) ≒ 748KHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

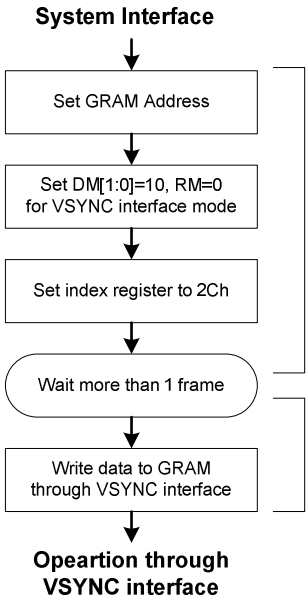
Minimum speed for RAM writing [Hz] > 320 x 240 x 748K / [(2 + 240 – 2)lines x 27clocks] ≒ 6.65 MHz

The above theoretical value is calculated based on the premise that the ILI9342C starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9342C starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

System Interface Mode to VSYNC interface mode

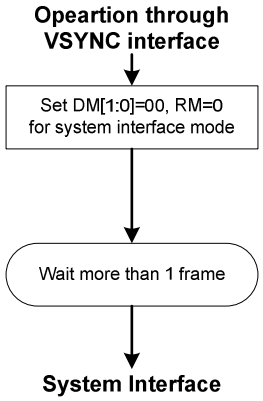


Display operation in synchronization with internal clocks

DM[1:0], RM become enable after completion of displaying 1 frame

Display operation in synchronization with VSYNC

VSYNC interface mode to System Interface Mode



Display operation in synchronization with VSYNC

DM[1:0], RM become enable after completion of displaying 1 frame

Display operation in synchronization with internal clocks

Note: input VSYNC for more than 1 frame period after setting the DM, RM register.

7.3. Color Depth Conversion Look Up Table

When ILI9342C operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R_{005} R_{004} R_{003} R_{002} R_{001} R_{000}	1
00001	R_{015} R_{014} R_{013} R_{012} R_{011} R_{010}	2
00010	R_{025} R_{024} R_{023} R_{022} R_{021} R_{020}	3
00011	R_{035} R_{034} R_{033} R_{032} R_{031} R_{030}	4
00100	R_{045} R_{044} R_{043} R_{042} R_{041} R_{040}	5
00101	R_{055} R_{054} R_{053} R_{052} R_{051} R_{050}	6
00110	R_{065} R_{064} R_{063} R_{062} R_{061} R_{060}	7
00111	R_{075} R_{074} R_{073} R_{072} R_{071} R_{070}	8
01000	R_{085} R_{084} R_{083} R_{082} R_{081} R_{080}	9
01001	R_{095} R_{094} R_{093} R_{092} R_{091} R_{090}	10
01010	R_{105} R_{104} R_{103} R_{102} R_{101} R_{100}	11
01011	R_{115} R_{114} R_{113} R_{112} R_{111} R_{110}	12
01100	R_{125} R_{124} R_{123} R_{122} R_{121} R_{120}	13
01101	R_{135} R_{134} R_{133} R_{132} R_{131} R_{130}	14
01110	R_{145} R_{144} R_{143} R_{142} R_{141} R_{140}	15
01111	R_{155} R_{154} R_{153} R_{152} R_{151} R_{150}	16
10000	R_{165} R_{164} R_{163} R_{162} R_{161} R_{160}	17
10001	R_{175} R_{174} R_{173} R_{172} R_{171} R_{170}	18
10010	R_{185} R_{184} R_{183} R_{182} R_{181} R_{180}	19
10011	R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}	20
10100	R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}	21
10101	R_{215} R_{214} R_{213} R_{212} R_{211} R_{210}	22
10110	R_{225} R_{224} R_{223} R_{222} R_{221} R_{220}	23
10111	R_{235} R_{234} R_{233} R_{232} R_{231} R_{230}	24
11000	R_{245} R_{244} R_{243} R_{242} R_{241} R_{240}	25
11001	R_{255} R_{254} R_{253} R_{252} R_{251} R_{250}	26
11010	R_{265} R_{264} R_{263} R_{262} R_{261} R_{260}	27
11011	R_{275} R_{274} R_{273} R_{272} R_{271} R_{270}	28
11100	R_{285} R_{284} R_{283} R_{282} R_{281} R_{280}	29
11101	R_{295} R_{294} R_{293} R_{292} R_{291} R_{290}	30
11110	R_{305} R_{304} R_{303} R_{302} R_{301} R_{300}	31
11111	R_{315} R_{314} R_{313} R_{312} R_{311} R_{310}	32

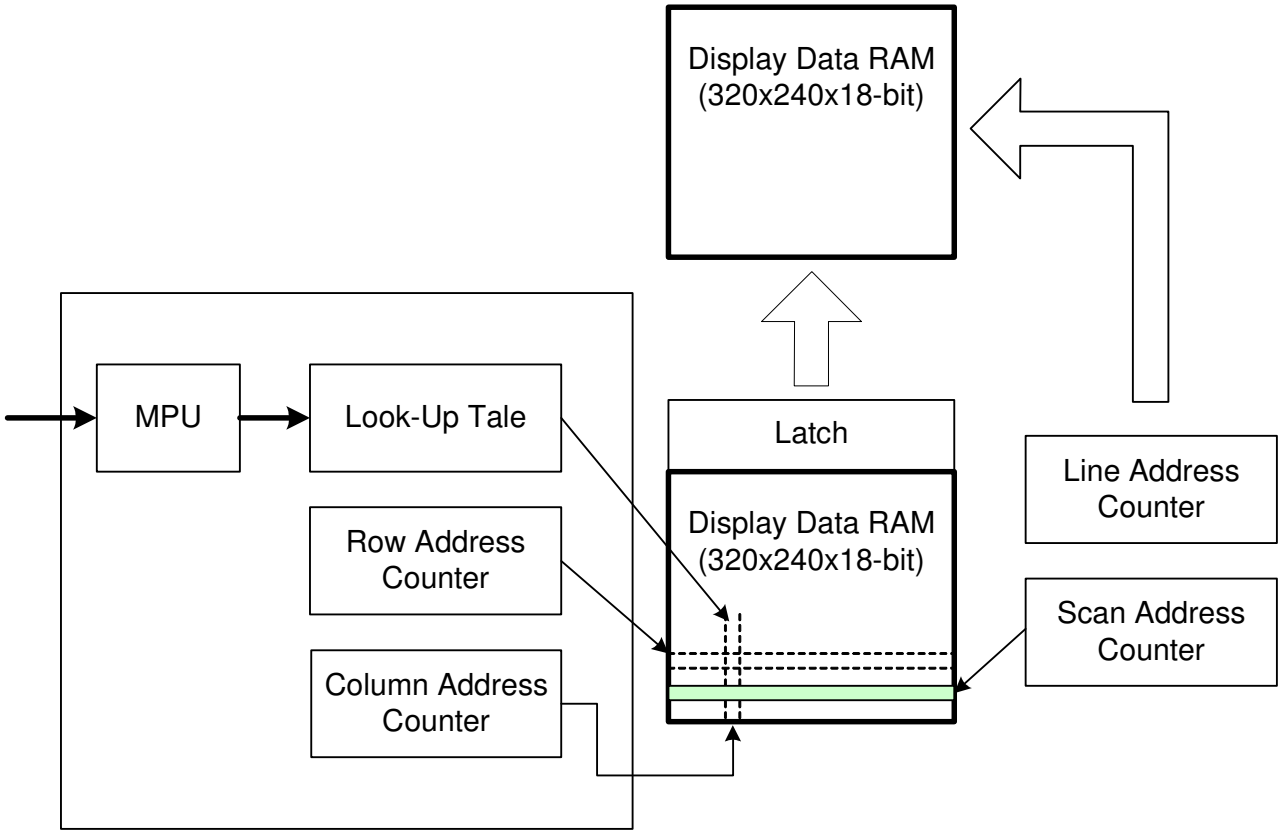
G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G_{005} G_{004} G_{003} G_{002} G_{001} G_{000}	33
000001	G_{015} G_{014} G_{013} G_{012} G_{011} G_{010}	34
000010	G_{025} G_{024} G_{023} G_{022} G_{021} G_{020}	35
000011	G_{035} G_{034} G_{033} G_{032} G_{031} G_{030}	36
000100	G_{045} G_{044} G_{043} G_{042} G_{041} G_{040}	37
000101	G_{055} G_{054} G_{053} G_{052} G_{051} G_{050}	38
000110	G_{065} G_{064} G_{063} G_{062} G_{061} G_{060}	39
000111	G_{075} G_{074} G_{073} G_{072} G_{071} G_{070}	40
001000	G_{085} G_{084} G_{083} G_{082} G_{081} G_{080}	41
001001	G_{095} G_{094} G_{093} G_{092} G_{091} G_{090}	42
001010	G_{105} G_{104} G_{103} G_{102} G_{101} G_{100}	43
001011	G_{115} G_{114} G_{113} G_{112} G_{111} G_{110}	44
001100	G_{125} G_{124} G_{123} G_{122} G_{121} G_{120}	45
001101	G_{135} G_{134} G_{133} G_{132} G_{131} G_{130}	46
001110	G_{145} G_{144} G_{143} G_{142} G_{141} G_{140}	47
001111	G_{155} G_{154} G_{153} G_{152} G_{151} G_{150}	48
010000	G_{165} G_{164} G_{163} G_{162} G_{161} G_{160}	49
010001	G_{175} G_{174} G_{173} G_{172} G_{171} G_{170}	50
010010	G_{185} G_{184} G_{183} G_{182} G_{181} G_{180}	51
010011	G_{195} G_{194} G_{193} G_{192} G_{191} G_{190}	52
010100	G_{205} G_{204} G_{203} G_{202} G_{201} G_{200}	53
010101	G_{215} G_{214} G_{213} G_{212} G_{211} G_{210}	54
010110	G_{225} G_{224} G_{223} G_{222} G_{221} G_{220}	55
010111	G_{235} G_{234} G_{233} G_{232} G_{231} G_{230}	56
011000	G_{245} G_{244} G_{243} G_{242} G_{241} G_{240}	57
011001	G_{255} G_{254} G_{253} G_{252} G_{251} G_{250}	58
011010	G_{265} G_{264} G_{263} G_{262} G_{261} G_{260}	59
011011	G_{275} G_{274} G_{273} G_{272} G_{271} G_{270}	60
011100	G_{285} G_{284} G_{283} G_{282} G_{281} G_{280}	61
011101	G_{295} G_{294} G_{293} G_{292} G_{291} G_{290}	62
011110	G_{305} G_{304} G_{303} G_{302} G_{301} G_{300}	63
011111	G_{315} G_{314} G_{313} G_{312} G_{311} G_{310}	64
100000	G_{325} G_{324} G_{323} G_{322} G_{321} G_{320}	65
100001	G_{335} G_{334} G_{333} G_{332} G_{331} G_{330}	66

G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G_{345} G_{344} G_{343} G_{342} G_{341} G_{340}	67
100011	G_{355} G_{354} G_{353} G_{352} G_{351} G_{350}	68
100100	G_{365} G_{364} G_{363} G_{362} G_{361} G_{360}	69
100101	G_{375} G_{374} G_{373} G_{372} G_{371} G_{370}	70
100110	G_{385} G_{384} G_{383} G_{382} G_{381} G_{380}	71
100111	G_{395} G_{394} G_{393} G_{392} G_{391} G_{390}	72
101000	G_{405} G_{404} G_{403} G_{402} G_{401} G_{400}	73
101001	G_{415} G_{414} G_{413} G_{412} G_{411} G_{410}	74
101010	G_{425} G_{424} G_{423} G_{422} G_{421} G_{420}	75
101011	G_{435} G_{434} G_{433} G_{432} G_{431} G_{430}	76
101100	G_{445} G_{444} G_{443} G_{442} G_{441} G_{440}	77
101101	G_{455} G_{454} G_{453} G_{452} G_{451} G_{450}	78
101110	G_{465} G_{464} G_{463} G_{462} G_{461} G_{460}	79
101111	G_{475} G_{474} G_{473} G_{472} G_{471} G_{470}	80
110000	G_{485} G_{484} G_{483} G_{482} G_{481} G_{480}	81
110001	G_{495} G_{494} G_{493} G_{492} G_{491} G_{490}	82
110010	G_{505} G_{504} G_{503} G_{502} G_{501} G_{500}	83
110011	G_{515} G_{514} G_{513} G_{512} G_{511} G_{510}	84
110100	G_{525} G_{524} G_{523} G_{522} G_{521} G_{520}	85
110101	G_{535} G_{534} G_{533} G_{532} G_{531} G_{530}	86
110110	G_{545} G_{544} G_{543} G_{542} G_{541} G_{540}	87
110111	G_{555} G_{554} G_{553} G_{552} G_{551} G_{550}	88
111000	G_{565} G_{564} G_{563} G_{562} G_{561} G_{560}	89
111001	G_{575} G_{574} G_{573} G_{572} G_{571} G_{570}	90
111010	G_{585} G_{584} G_{583} G_{582} G_{581} G_{580}	91
111011	G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}	92
111100	G_{605} G_{604} G_{603} G_{602} G_{601} G_{600}	93
111101	G_{615} G_{614} G_{613} G_{612} G_{611} G_{610}	94
111110	G_{625} G_{624} G_{623} G_{622} G_{621} G_{620}	95
111111	G_{635} G_{634} G_{633} G_{632} G_{631} G_{630}	96

B input (5-bit) 16-bit/pixel –mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B_{005} B_{004} B_{003} B_{002} B_{001} B_{000}	97
00001	B_{015} B_{014} B_{013} B_{012} B_{011} B_{010}	98
00010	B_{025} B_{024} B_{023} B_{022} B_{021} B_{020}	99
00011	B_{035} B_{034} B_{033} B_{032} B_{031} B_{030}	100
00100	B_{045} B_{044} B_{043} B_{042} B_{041} B_{040}	101
00101	B_{055} B_{054} B_{053} B_{052} B_{051} B_{050}	102
00110	B_{065} B_{064} B_{063} B_{062} B_{061} B_{060}	103
00111	B_{075} B_{074} B_{073} B_{072} B_{071} B_{070}	104
01000	B_{085} B_{084} B_{083} B_{082} B_{081} B_{080}	105
01001	B_{095} B_{094} B_{093} B_{092} B_{091} B_{090}	106
01010	B_{105} B_{104} B_{103} B_{102} B_{101} B_{100}	107
01011	B_{115} B_{114} B_{113} B_{112} B_{111} B_{110}	108
01100	B_{125} B_{124} B_{123} B_{122} B_{121} B_{120}	109
01101	B_{135} B_{134} B_{133} B_{132} B_{131} B_{130}	110
01110	B_{145} B_{144} B_{143} B_{142} B_{141} B_{140}	111
01111	B_{155} B_{154} B_{153} B_{152} B_{151} B_{150}	112
10000	B_{165} B_{164} B_{163} B_{162} B_{161} B_{160}	113
10001	B_{175} B_{174} B_{173} B_{172} B_{171} B_{170}	114
10010	B_{185} B_{184} B_{183} B_{182} B_{181} B_{180}	115
10011	B_{195} B_{194} B_{193} B_{192} B_{191} B_{190}	116
10100	B_{205} B_{204} B_{203} B_{202} B_{201} B_{200}	117
10101	B_{215} B_{214} B_{213} B_{212} B_{211} B_{210}	118
10110	B_{225} B_{224} B_{223} B_{222} B_{221} B_{220}	119
10111	B_{235} B_{234} B_{233} B_{232} B_{231} B_{230}	120
11000	B_{245} B_{244} B_{243} B_{242} B_{241} B_{240}	121
11001	B_{255} B_{254} B_{253} B_{252} B_{251} B_{250}	122
11010	B_{265} B_{264} B_{263} B_{262} B_{261} B_{260}	123
11011	B_{275} B_{274} B_{273} B_{272} B_{271} B_{270}	124
11100	B_{285} B_{284} B_{283} B_{282} B_{281} B_{280}	125
11101	B_{295} B_{294} B_{293} B_{292} B_{291} B_{290}	126
11110	B_{305} B_{304} B_{303} B_{302} B_{301} B_{300}	127
11111	B_{315} B_{314} B_{313} B_{312} B_{311} B_{310}	128

7.4. Display Data RAM (DDRAM)

ILI9342C has an integrated 320x240x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 320xRGBx240 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

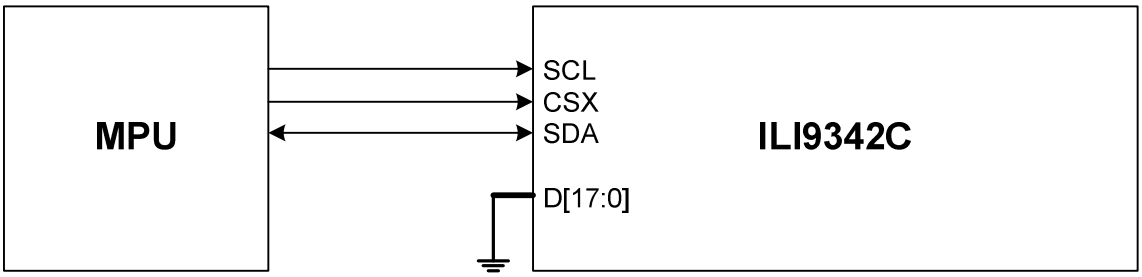


7.5. Display Data Format

ILI9342C supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.5.1. 3-line Serial Interface

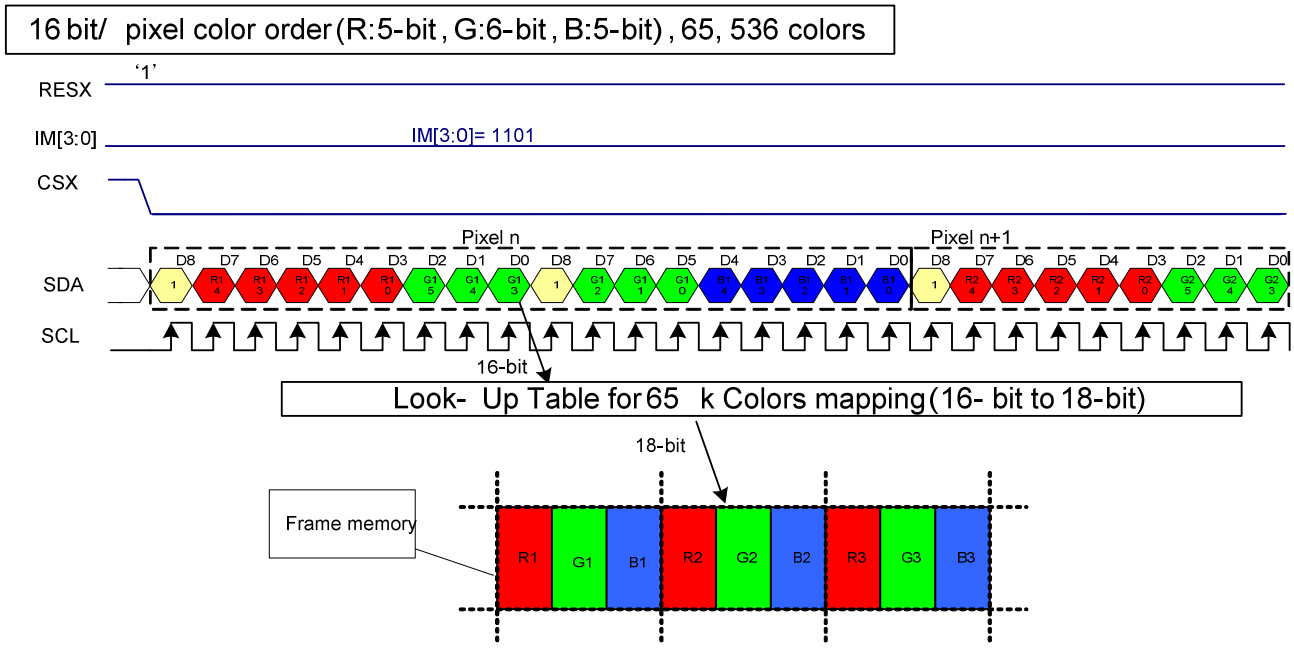
The 3-line/9-bit serial bus interface of ILI9342C can be used by setting external pin as IM [3:0] to "1101" for serial interface. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.



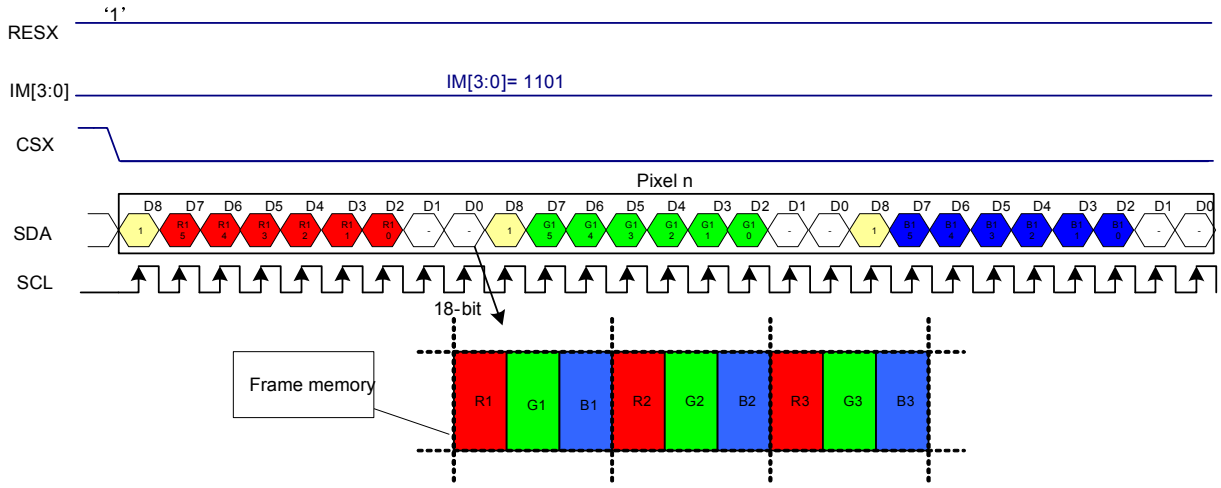
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/ pixel color order (R:6-bit , G:6-bit , B:6-bit) , 262, 144 colors



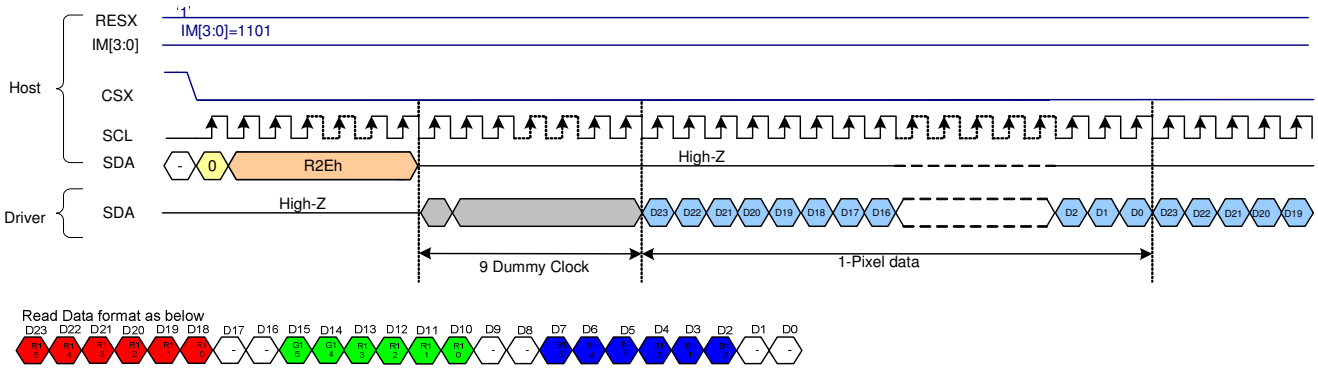
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

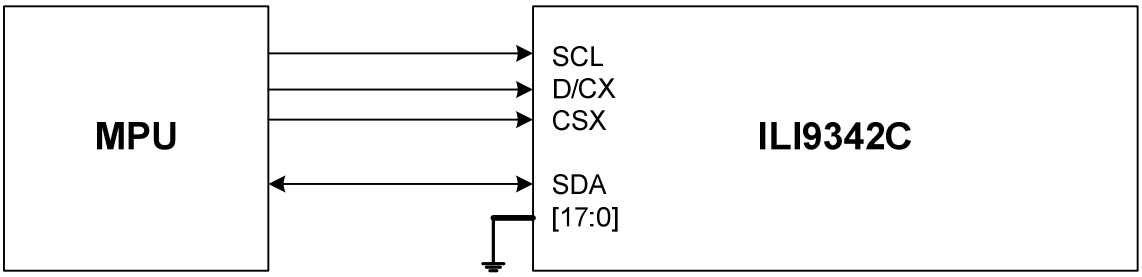
Read data through 3-line SPI mode



Note 1: '-'= Don't care –Can be set "0" or "1".

7.5.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9342C can be used by setting external pin as IM [3:0] to "1111" for serial interface. The shown figure is the example of 4-line SPI interface.

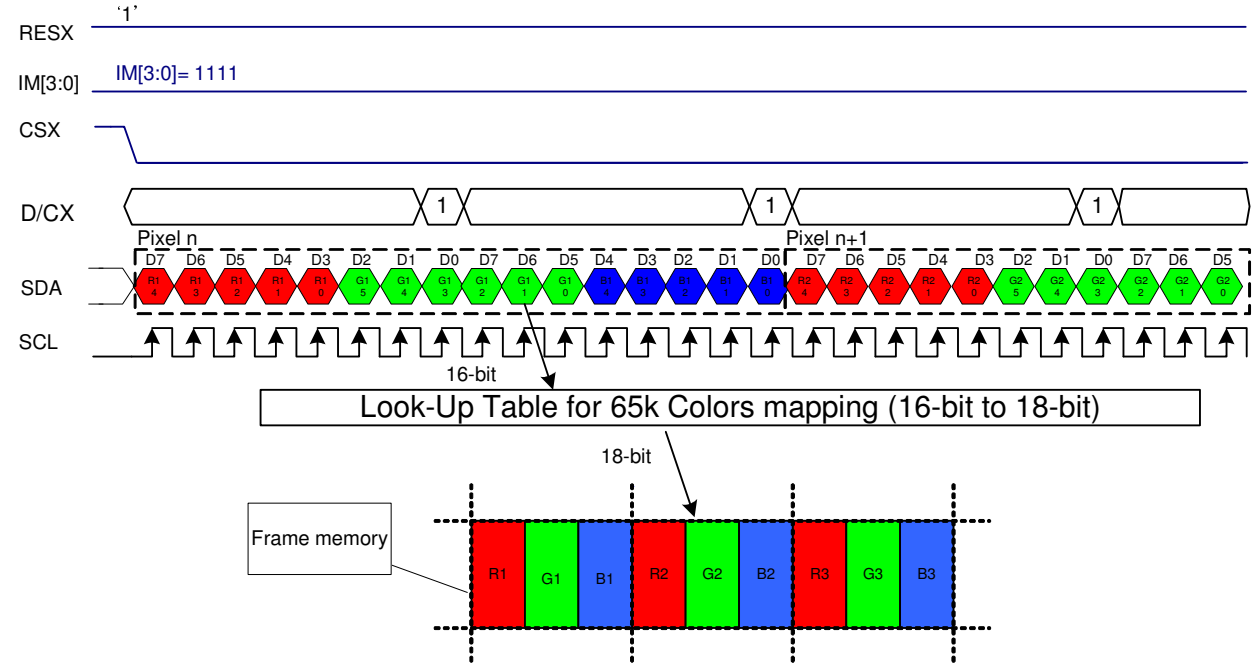


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



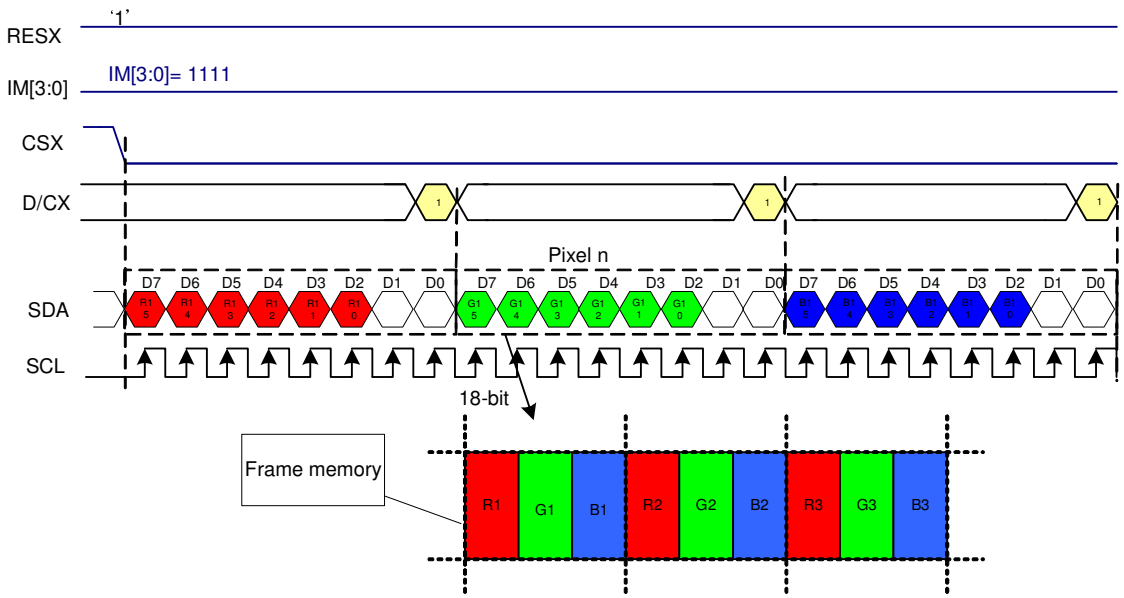
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



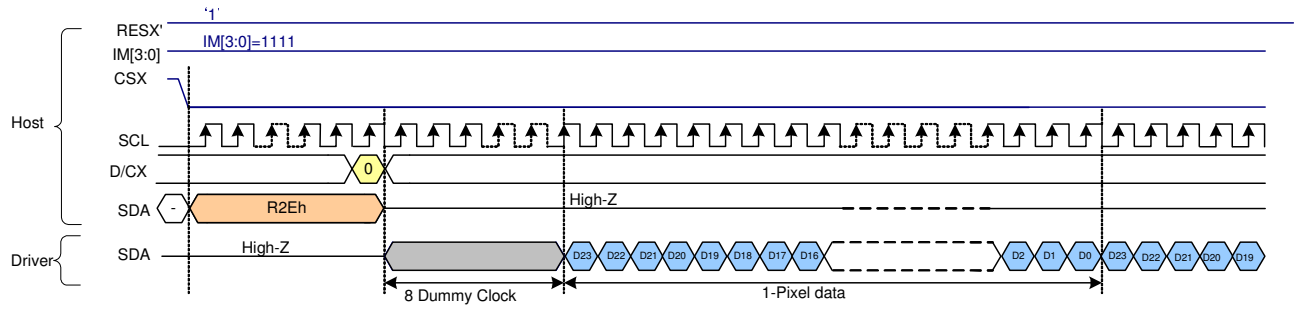
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

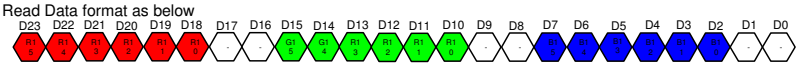
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Read data through 4-line SPI mode



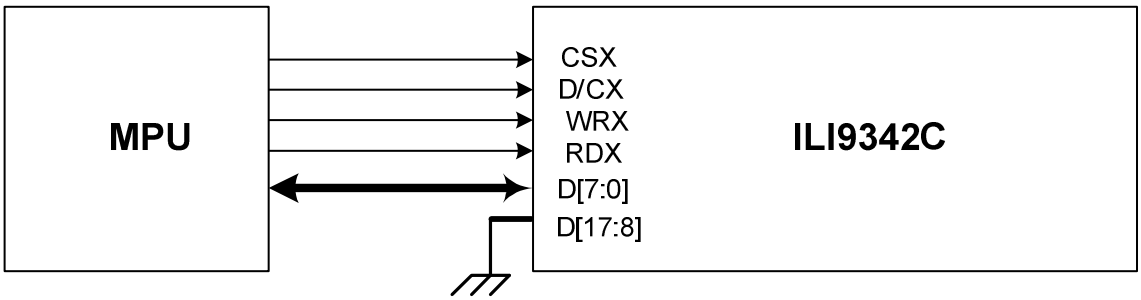
Read Data format as below



Note 1: '-'= Don't care – Can be set "0" or "1".

7.5.3. 8-bit Parallel MCU Interface

The 8080-Ⅰ system 8-bit parallel bus interface of ILI9342C can be used by setting external pin as IM [3:0] to "0100".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

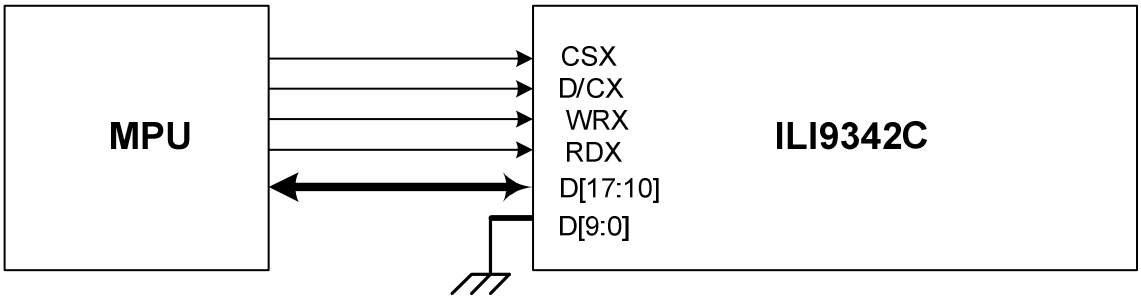
Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 8-bit parallel bus interface of ILI9342C can be used by settings as IM [3:0] ="0000". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

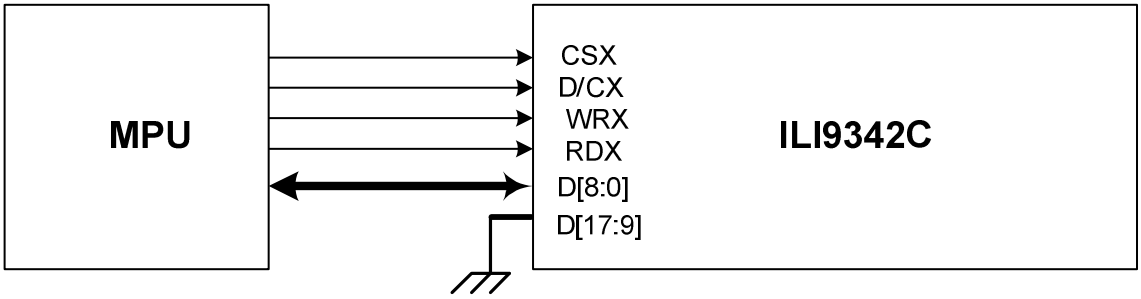
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

7.5.4. 9-bit Parallel MCU Interface

The 8080-Ⅰ system 9-bit parallel bus interface of ILI9342C can be selected by setting hardware pin IM [3:0] to "0101". The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8										
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

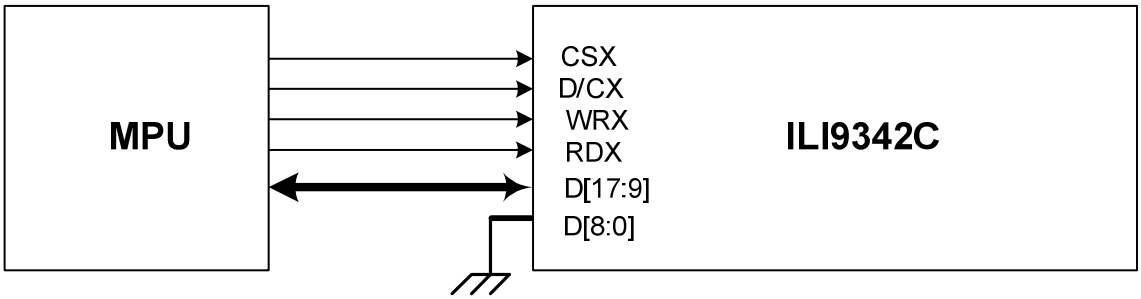
MDT[1:0]="00"

Count	0	1	2	3	4	…	478	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

MDT[1:0]="01"

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D8								
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 9-bit parallel bus interface of ILI9342C can be selected by setting hardware pin IM [3:0] to "0001". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7									
D16	C6	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

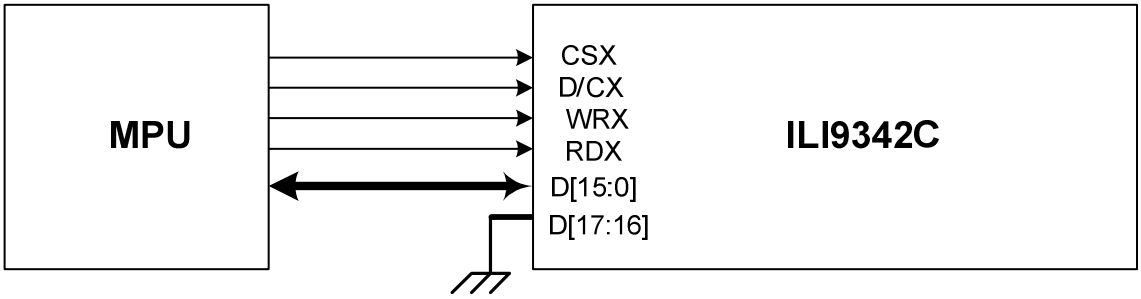
Count	0	1	2	3	4	…	478	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2		238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

MDT[1:0]="01"

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7							
D16	C6	0R5	0G5	0B5	…	239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	…	239R4	239G4	239B4
D14	C4	0R3	0G3	0B3	…	239R3	239G3	239B3
D13	C3	0R2	0G2	0B2	…	239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	…	239R1	239G1	239B1
D11	C1	0R0	0G0	0B0	…	239R0	239G0	239B0
D10	C0				…			
D9					…			

7.5.5. 16-bit Parallel MCU Interface

The 8080-Ⅰ system 16-bit parallel bus interface of ILI9342C can be selected by setting hardware pin IM[3:0] to "0110".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

MDT[1:0]=”00”

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9					…			
D8					…			
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1				…			
D0	C0				…			

MDT[1:0]=”01”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

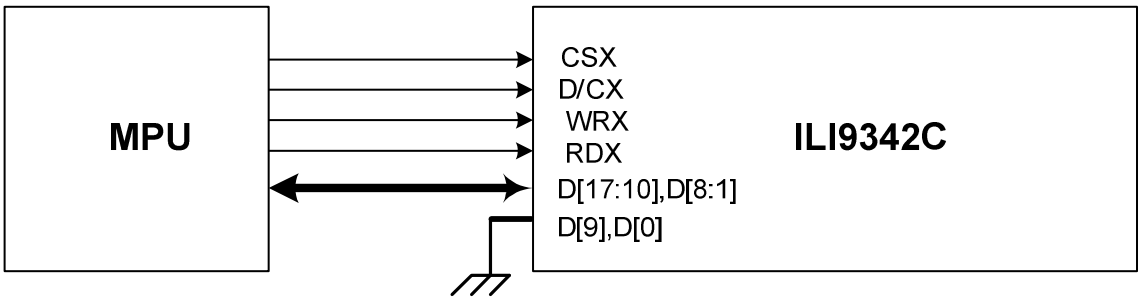
MDT[1:0]=”10”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-Ⅱ system 16-bit parallel bus interface of ILI9342C can be selected by settings IM [3:0] ="0010". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

MDT[1:0]=”00”

Count	0	1	2	3	…	358	359	360
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	238R5	238B5	239G5
D16		0R4	0B4	1G4	…	238R4	238B4	239G4
D15		0R3	0B3	1G3	…	238R3	238B3	239G3
D14		0R2	0B2	1G2	…	238R2	238B2	239G2
D13		0R1	0B1	1G1	…	238R1	238B1	239G1
D12		0R0	0B0	1G0	…	238R0	238B0	239G0
D11					…			
D10					…			
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D2	C1				…			
D1	C0				…			

MDT[1:0]=”01”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

MDT[1:0]=”10”

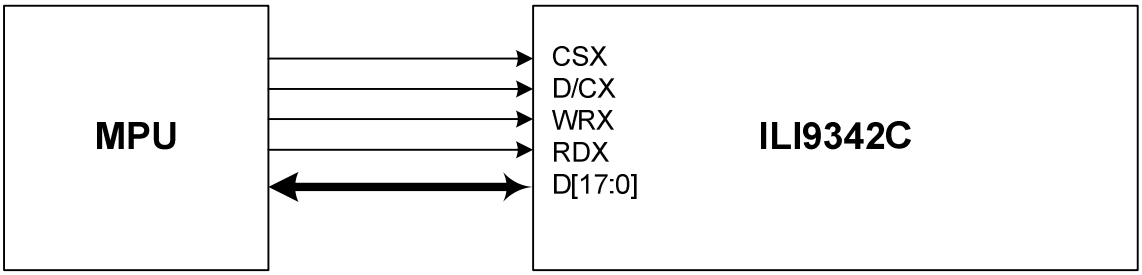
Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=”11”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…		1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

7.5.6. 18-bit Parallel MCU Interface

The 8080-Ⅰ system 18-bit parallel bus interface of ILI9342C can be selected by setting hardware pin IM[3:0] to "0111".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

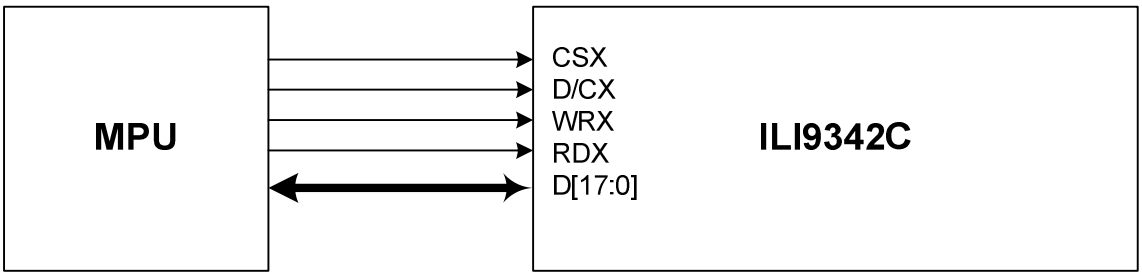
Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-Ⅱ system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="0011". The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

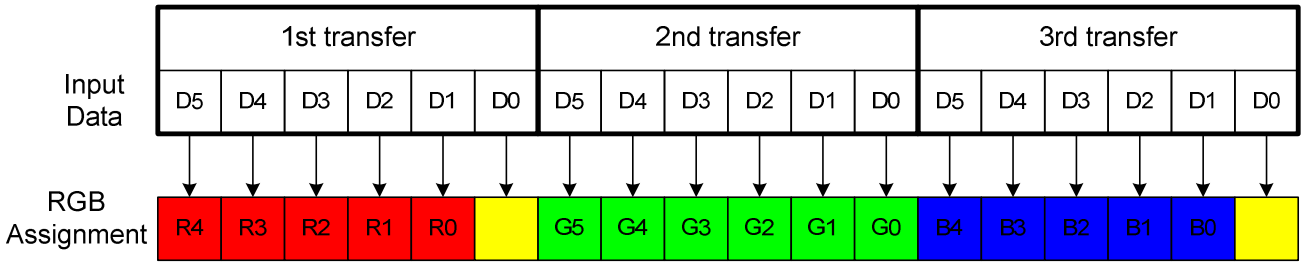
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

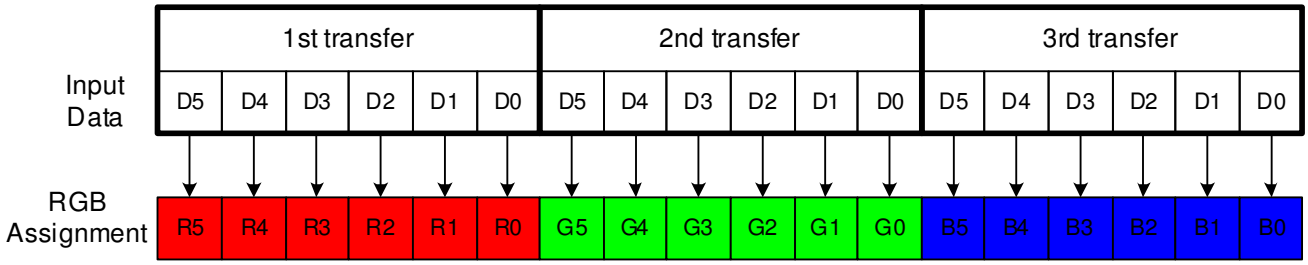
7.5.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



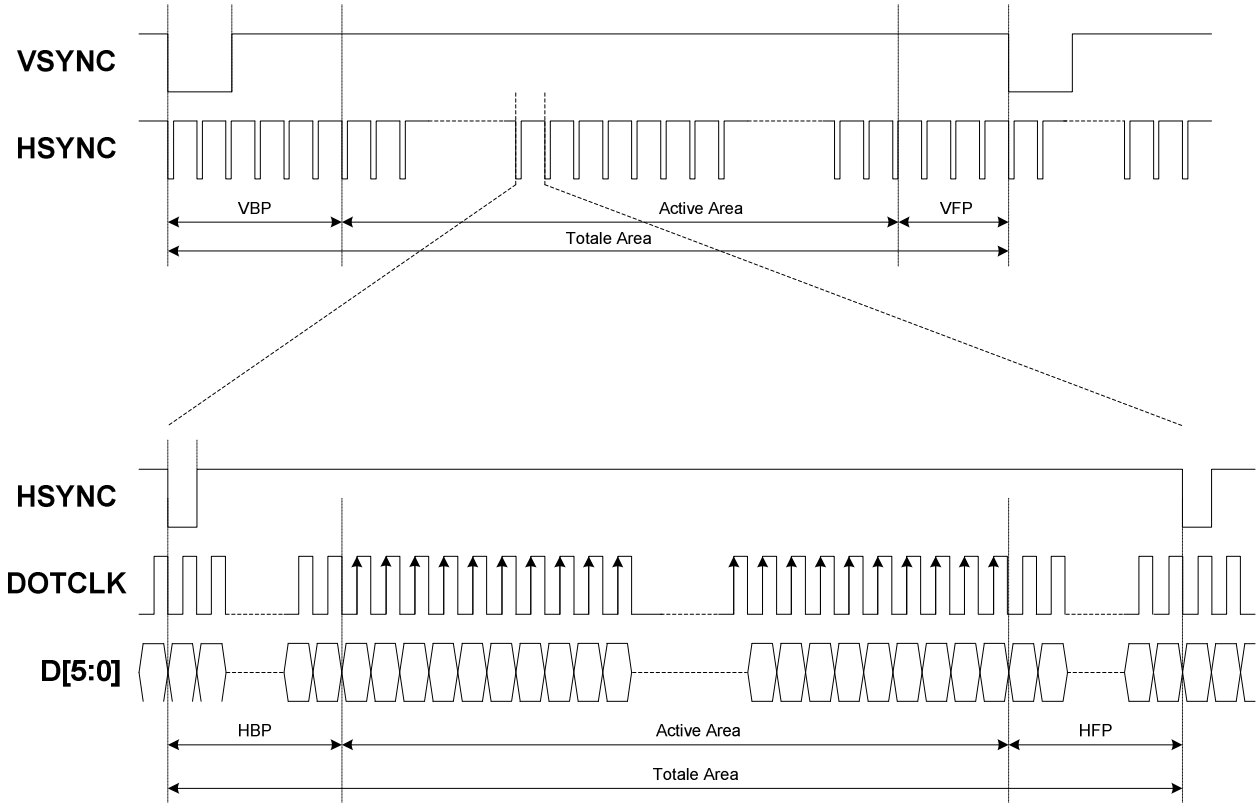
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



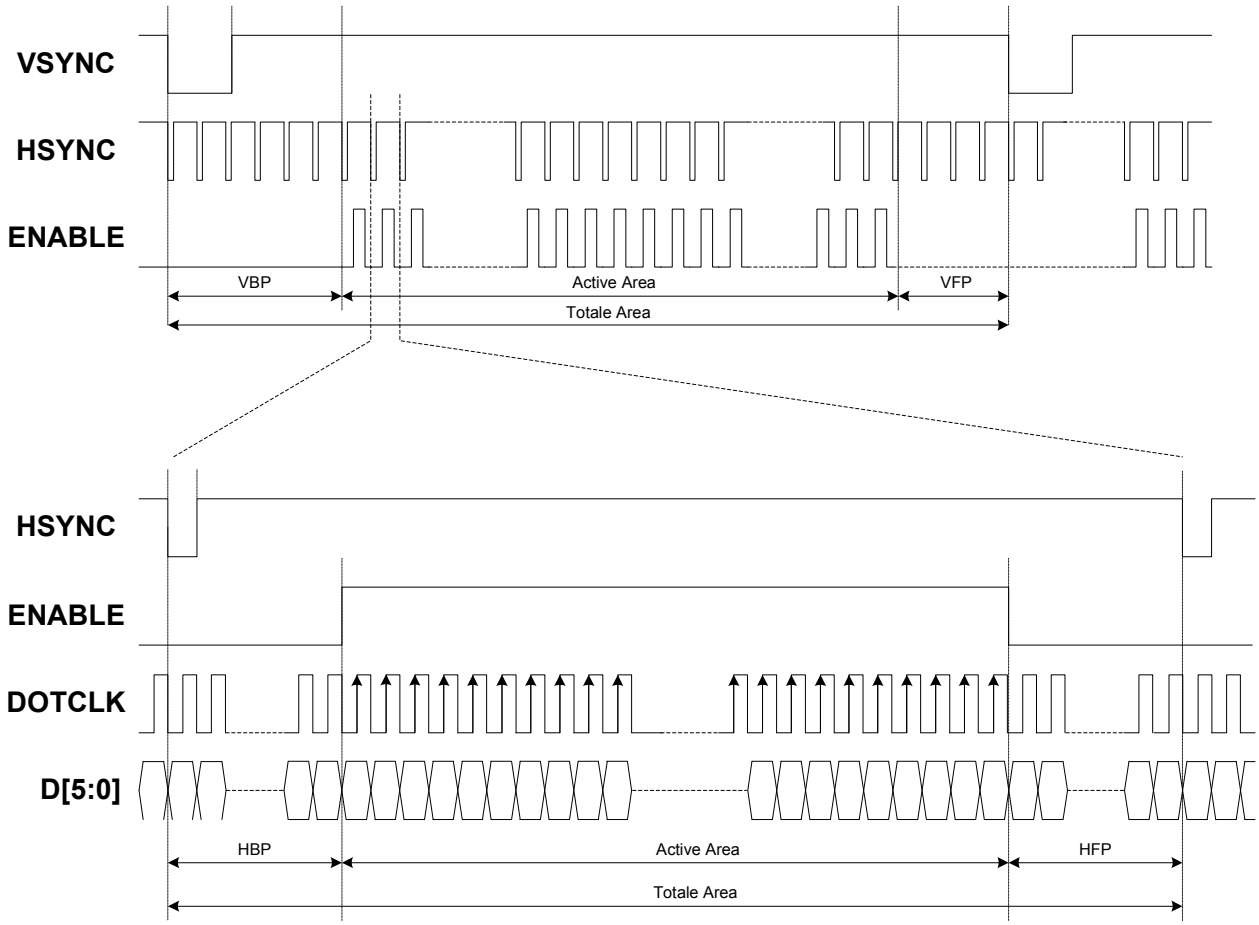
ILI9342C has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0]="11"

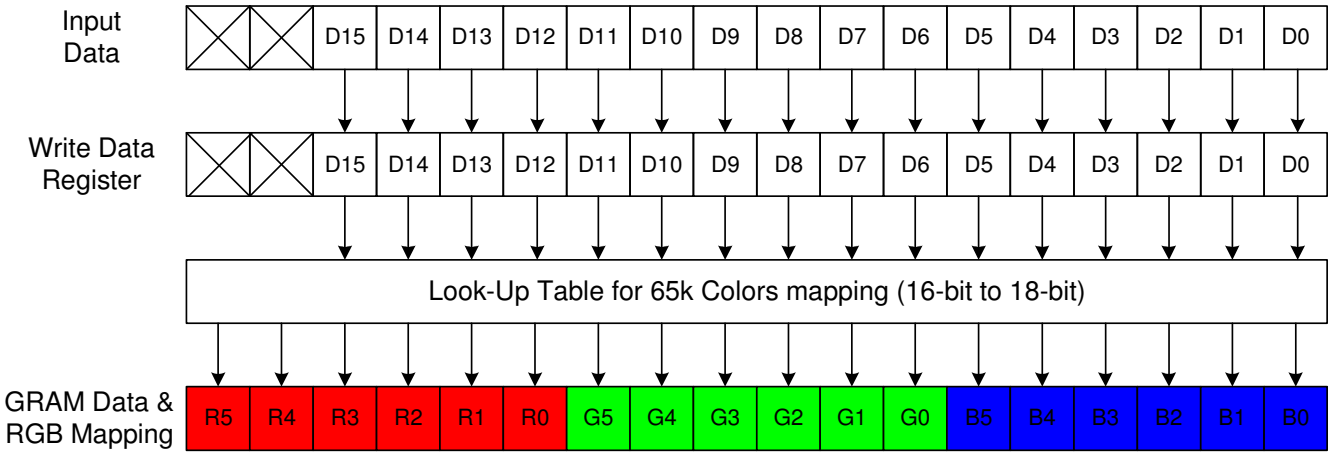


DE Mode, RCM[1:0]="10"



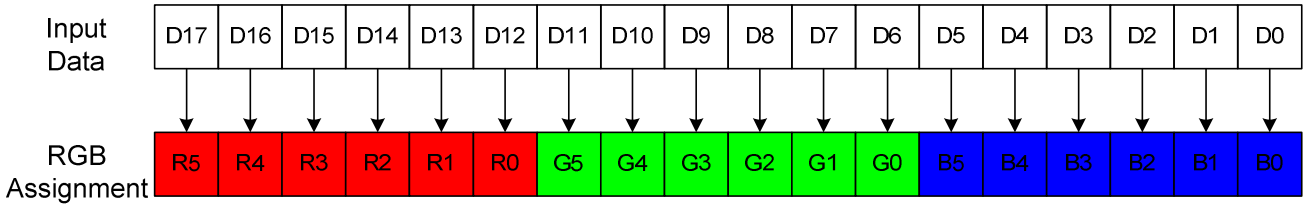
7.5.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [15:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via (D [15:0]) according to the VFP/VBP and HFP/HBP settings. The unused D17 and D16 pins must be connected to DGND for ensure normally operation. Registers can be set by the SPI system interface.



7.5.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1 [7:0]								E3
	1	↑	1	XX	ID2 [7:0]								00
	1	↑	1	XX	ID3 [7:0]								00
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [31:25]							X	00
	1	↑	1	XX	X	D [22:20]			D [19:16]				61
	1	↑	1	XX	X	X	X	X	X	D [10:8]			00
	1	↑	1	XX	D [7:5]			X	X	X	X	X	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	DPI [2:0]			X	DBI [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	D [2:0]			00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:2]						0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D [7:6]		X	X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
	1	1	↑	XX	GC [7:0]								01
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]								XX
	1	1	↑	XX	SC [7:0]								XX
	1	1	↑	XX	EC [15:8]								XX
	1	1	↑	XX	EC [7:0]								XX
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP [15:8]								XX
	1	1	↑	XX	SP [7:0]								XX
	1	1	↑	XX	EP [15:8]								XX
	1	1	↑	XX	EP [7:0]								XX

Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D [17:0]									XX
Color SET	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
	1	1	↑	XX	R00 [5:0]								XX
	1	1	↑	XX	Rnn [5:0]								XX
	1	1	↑	XX	R31 [5:0]								XX
	1	1	↑	XX	G00 [5:0]								XX
	1	1	↑	XX	Gnn [5:0]								XX
	1	1	↑	XX	G63 [5:0]								XX
	1	1	↑	XX	B00 [5:0]								XX
	1	1	↑	XX	Bnn [5:0]								XX
	1	1	↑	XX	B31 [5:0]								XX
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR [15:8]								00
	1	1	↑	XX	SR [7:0]								00
	1	1	↑	XX	ER [15:8]								00
	1	1	↑	XX	ER [7:0]								EF
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA [15:8]								00
	1	1	↑	XX	TFA [7:0]								00
	1	1	↑	XX	VSA [15:8]								00
	1	1	↑	XX	VSA [7:0]								F0
	1	1	↑	XX	BFA [15:8]								00
	1	1	↑	XX	BFA [7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP [15:8]								00
	1	1	↑	XX	VSP [7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI [2:0]			X	DBI [2:0]			66
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00
	1	1	↑	XX	STS [7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	GTS [9]	GTS [8]	00
	1	↑	1	XX	GTS [7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	1	↑	XX	DBV [7:0]								00

Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV [7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	00
Write Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	X	X	X	X	X	X	C [1:0]		00
Read Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	C [1:0]		00
Write CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XX	CMB [7:0]								00
Read CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CMB [7:0]								00
Read Automatic Brightness Control Self-Diagnostic Result	0	1	↑	XX	0	1	1	0	1	0	0	0	68H
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	X	X	X	X	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Module's Manufacture [7:0]								E3
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver Version [7:0]								XX
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	ByPass_MODE	RCM [1:0]		X	VSPL	HSPL	DPL	EPL	40
Frame Control (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
	1	1	↑	XX	X	X	X	X	X	X	DIVA [1:0]		00
	1	1	↑	XX	X	X	X	RTNA [4:0]					1C
Frame Control (In Idle Mode)	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
	1	1	↑	XX	X	X	X	X	X	X	DIVB [1:0]		00
	1	1	↑	XX	X	X	X	RTNB [4:0]					1C
Frame Control (In Partial Mode)	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
	1	1	↑	XX	X	X	X	X	X	X	DIVC [1:0]		00
	1	1	↑	XX	X	X	X	RTNC [4:0]					1C
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	X	X	X	X	X	X	DINV[1:0]		00
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	VFP [6:0]							02
	1	1	↑	XX	0	VBP [6:0]							02
	1	1	↑	XX	0	HFP [6:0]							0A
	1	1	↑	XX	0	HBP [6:0]							14

Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h

	1	1	↑	XX	X	X	X	X	PTG [1:0]		PT [1:0]			0A
	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]					80
	1	1	↑	XX	X	X	NL [5:0]							1D
	1	1	↑	XX	X	X	PCDIV [5:0]							04
Entry Mode Set	0	1	↑	XX	1	0	1	1	0	1	1	1		B7h
	1	1	↑	XX	X	X	X	X	X	GON	DTE	GAS		07
Backlight Control 1	0	1	↑	XX	1	0	1	1	1	0	0	0		B8h
	1	1	↑	XX	X	X	X	X	X	X	X	X		XX
	1	1	↑	XX	X	X	X	X	TH_UI [3:0]					0B
Backlight Control 2	0	1	↑	XX	1	0	1	1	1	0	0	1		B9h
	1	1	↑	XX	X	X	X	X	X	X	X	X		XX
	1	1	↑	XX	TH_MV [3:0]				TH_ST [3:0]					BB
Backlight Control 3	0	1	↑	XX	1	0	1	1	1	0	1	0		BAh
	1	1	↑	XX	X	X	X	X	X	X	X	X		XX
	1	1	↑	XX	X	X	X	X	DTH_UI [3:0]					04
Backlight Control 4	0	1	↑	XX	1	0	1	1	1	0	1	1		BBh
	1	1	↑	XX	X	X	X	X	X	X	X	X		XX
	1	1	↑	XX	DTH_MV [3:0]				DTH_ST [3:0]					A8
Backlight Control 5	0	1	↑	XX	1	0	1	1	1	1	0	0		BCh
	1	1	↑	XX	X	X	X	X	X	X	X	X		XX
	1	1	↑	XX	DIM2 [3:0]				X	DIM1 [2:0]				43
Backlight Control 6	0	1	↑	XX	1	0	1	1	1	1	0	1		BDh
	1	1	↑	XX						LEDONR	LEDONPOL	LEDPW MOPL		00
Backlight Control 7	0	1	↑	XX	1	0	1	1	1	1	1	0		BEh
	1	1	↑	XX	PWM_DIV[7:0]									D0
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0		C0h
	1	1	↑	XX	X	X	X	VRH1 [4:0]						09
	1	1	↑	XX	X	X	X	VRH2 [4:0]						09
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1		C1h
	1	1	↑	XX	0	VC[2:0]			0	BT [2:0]				00
Power Control 3	0	1	↑	XX	1	1	0	0	0	0	1	0		C2h
(For Normal Mode)	1	1	↑	XX	1	DCA1 [2:0]			0	DCA0 [2:0]				B2
Power Control 4	0	1	↑	XX	1	1	0	0	0	0	1	1		C3h
(For Idle Mode)	1	1	↑	XX	1	DCB1 [2:0]			0	DCB0 [2:0]				B2
Power Control 5	0	1	↑	XX	1	1	0	0	0	1	0	0		C4h
(For Partial Mode)	1	1	↑	XX	1	DCC1 [2:0]			0	DCC0 [2:0]				B2
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1		C5h
	1	1	↑	XX	nVM	VCM[6:0]								F2
Get GPIO0~7 Status	0	1	↑	XX	1	1	0	0	0	1	1	0		C6h
	1	↑	1	XX	X	X	X	X	X	X	X	X		XX
	1	↑	1	XX	GPI [7:0]									00
Set GPIO0~7 Status	0	1	↑	XX	1	1	0	0	0	1	1	1		C7h
	1	1	↑	XX	GPO[7:0]									00
	1	1	↑	XX	X	X	X	X	X	X	IE	OE B		02
Set EXTC	0	1	↑	XX	1	1	0	0	1	0	0	0		C8h
	1	1	↑	XX	EXTC1[7:0]									FF
	1	1	↑	XX	EXTC2[7:0]									93
	1	1	↑	XX	EXTC3[7:0]									42
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0		D0h
	1	1	↑	XX	X	X	X	X	PGM_ADR [3:0]					00
	1	1	↑	XX	PGM_DATA [7:0]									XX
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	1		D1h
	1	1	↑	XX	KEY [23:16]									55
	1	1	↑	XX	KEY [15:8]									AA
	1	1	↑	XX	KEY [7:0]									66

NV Memory Status Read	0	↓	↑	XX	1		1	0	1	0	0	1	0	D2h
	1	↑	↓	XX	X		X	X	X	X	X	X	X	XX
	1	↑	↓	XX	MADCTL_CNT [1:0]			ID3_CNT [1:0]		ID2_CNT [1:0]		ID1_CNT [1:0]		XX
	1	↑	↓	XX	BUSY		X	X	X	VMF_CNT [2:0]				XX
Read ID4	0	↓	↑	XX	1	1	0	1	0	0	1	1		D3h
	1	↑	↓	XX	X	X	X	X	X	X	X	X		XX
	1	↑	↓	XX	0	0	0	0	0	0	0	0		00
	1	↑	↓	XX	1	0	0	1	0	0	1	1		93
	1	↑	↓	XX	0	1	0	0	0	0	1	0		42
Get External Register by SPI	0	1	↑	XX	1	1	0	1	1	0	0	1		D9h
	1	1	↑	XX	X	X	X	ENSPI	SPI_EXT_ORD [3:0]					00
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0		E0h
	1	1	↑	XX	X	X	X	X	VP0 [3:0]					00
	1	1	↑	XX	X	X	VP1 [5:0]							05
	1	1	↑	XX	X	X	VP2 [5:0]							08
	1	1	↑	XX	X	X	X	X	VP4 [3:0]					04
	1	1	↑	XX	X	X	X	VP6 [4:0]						13
	1	1	↑	XX	X	X	X	X	VP13 [3:0]					0A
	1	1	↑	XX	X	VP20 [6:0]								34
	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]					8A
	1	1	↑	XX	X	VP43 [6:0]								46
	1	1	↑	XX	X	X	X	X	VP50 [3:0]					07
	1	1	↑	XX	X	X	X	VP57 [4:0]						0E
	1	1	↑	XX	X	X	X	X	VP59 [3:0]					0A
	1	1	↑	XX	X	X	VP61 [5:0]							1B
	1	1	↑	XX	X	X	VP62 [5:0]							1D
	1	1	↑	XX	X	X	X	X	VP63 [3:0]					0F
Negative Gamma CorrectionE	0	1	↑	XX	1	1	1	0	0	0	0	1		E1h
	1	1	↑	XX	X	X	X	X	VN0 [4:0]					00
	1	1	↑	XX	X	X	VN1 [5:0]							22
	1	1	↑	XX	X	X	VN2 [5:0]							25
	1	1	↑	XX	X	X	X	X	VN4 [3:0]					04
	1	1	↑	XX	X	X	X	VN6 [4:0]						0F
	1	1	↑	XX	X	X	X	X	VN13 [3:0]					06
	1	1	↑	XX	X	VN20 [6:0]								38
	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]					56
	1	1	↑	XX	X	VN43 [6:0]								4B
	1	1	↑	XX	X	X	X	X	VN50 [3:0]					05
	1	1	↑	XX	X	X	X	VN57 [4:0]						0C
	1	1	↑	XX	X	X	X	X	VN59 [3:0]					0A
	1	1	↑	XX	X	X	VN61 [5:0]							37
	1	1	↑	XX	X	X	VN62 [5:0]							3A
	1	1	↑	XX	X	X	X	X	VN63 [4:0					0F
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0		E2h
1st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]					XX
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]					XX
16th Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]					XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1		E3h
1st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]					XX
:	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]					XX
64th Parameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]					XX
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0		F6h
	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	X	BGR_EOR	X	X	WEMODE		01
	1	1	↑	XX	X	X	EPF [1:0]		X	X	MDT [1:0]			00
	1	1	↑	XX	X	X	ENDIAN	X	DM [1:0]		RM	RIM		00

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP (00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9342C is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

8.2. Description of Level 1 Command

8.2.1. NOP (00h)

00h	NOP (No Operation)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Parameter	No Parameter.												
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.												
Restriction	None												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A

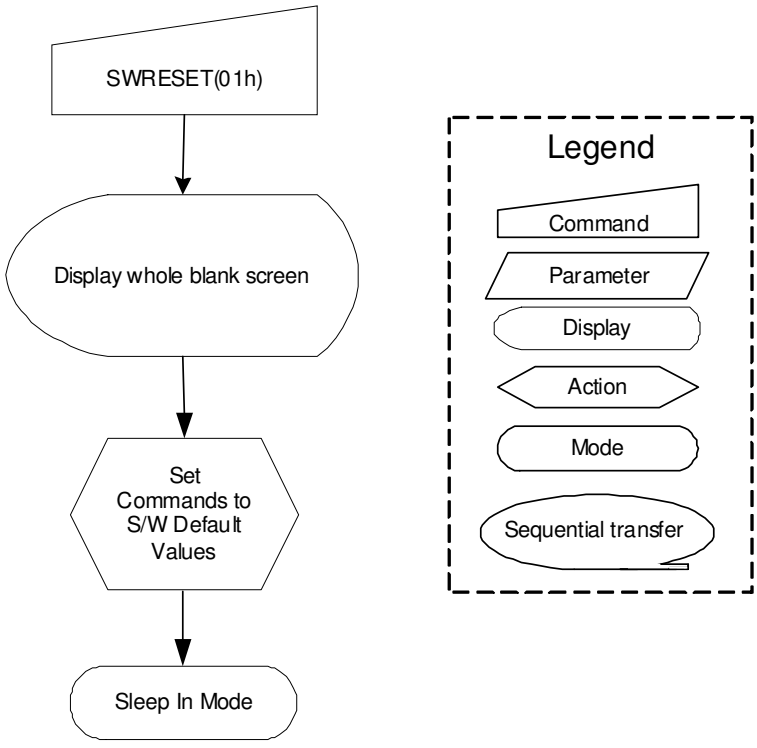
Flow Chart	None

8.2.2. Software Reset (01h)

01h	SWRESET												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Parameter	No Parameter.												
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command X = Don't care.												
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.												
Register Availability													
Default													
Flow Chart													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
SW Reset	N/A
HW Reset	N/A



8.2.3. Read display identification information (04h)

04h	RDDIDIF (Read Display Identification Information)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	ID1 [7:0]								E3
3rd Parameter	1	↑	1	XX	ID2 [7:0]								00
4th Parameter	1	↑	1	XX	ID3 [7:0]								00
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2 [7:0]): LCD module/driver version ID. The 4th parameter (ID3 [7:0]): LCD module/driver ID.												
Restriction													

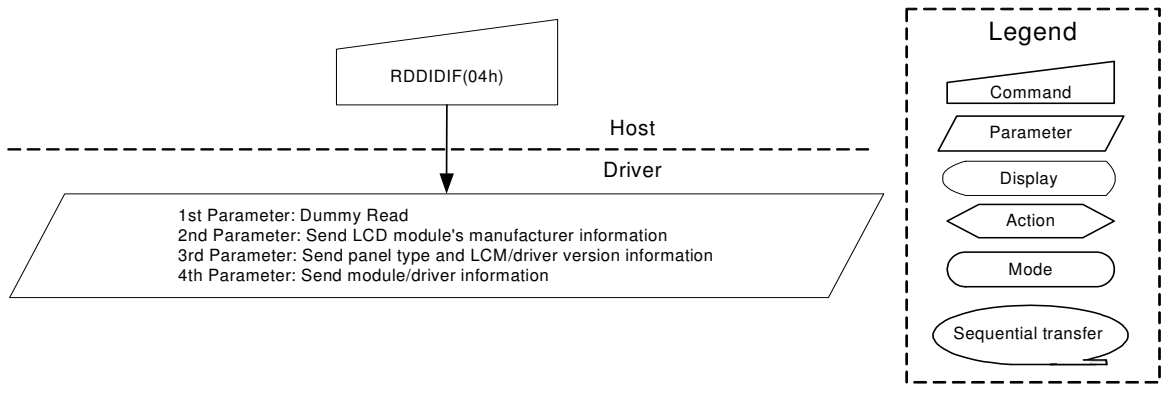
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



8.2.4. Read Display Status (09h)

09h	RDDST (Read Display Status)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D [31:25]							0	00
3rd Parameter	1	↑	1	XX	0	D [22:20]			D [19:16]				61
4th Parameter	1	↑	1	XX	0	0	0	0	0	D [10:8]			00
5th Parameter	1	↑	1	XX	D [7:5]			0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
31	booster oltage status	0	Booster OFF
		1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL D7='0')
		1	Bottom to Top (When MADCTL D7='1')
D29	Column address order	0	Left to Right (When MADCTL D6='0').
		1	Right to Left (When MADCTL D6='1').
D28	Row/column exchange	0	Normal Mode (When MADCTL D5='0').
		1	Reverse Mode (When MADCTL D5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL D4='0')
		1	LCD Refresh Bottom to Top (When MADCTL D4='1').
D26	RGB/BGR order	0	RGB (When MADCTL D3='0')
		1	BGR (When MADCTL D3='1')
D25	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL D2='0')
		1	LCD Refresh Right to Left (When MADCTL D2='1')
D24	Not used	0	---
D23	Not used	0	---
D22	Interface color pixel format definition	101	16-bit/pixel
D21			
D20		110	18-bit/pixel
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Scroll OFF
D14	Not used	0	---
D13	Inversion status	0	Not defined
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
		1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
D[8:6]	Gamma curve selection	000	GC0
		001	GC1
		010	GC2
		011	GC3
		other	Not defined

	D5	Tearing effect line mode	0	Mode 1, V-Blanking only
			1	Mode 2, both H-Blanking and V-Blanking.
	D4	Not used	0	---
	D3	Not used	0	---
	D2	Not used	0	---
	D1	Not used	0	---
	D0	Not used	0	---

X = Don't care

Restriction

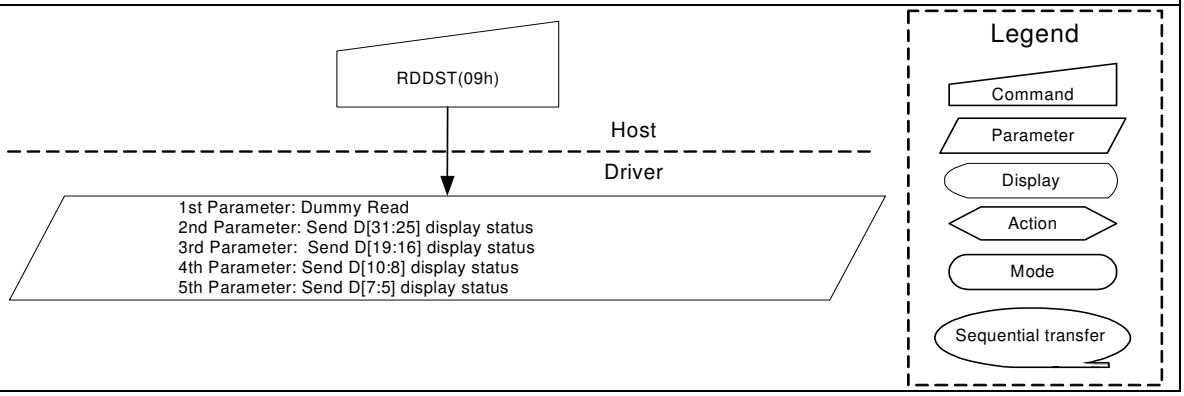
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000h
SW Reset	32'h00610000h
HW Reset	32'h00610000h

Flow Chart



8.2.5. Read Display Power Mode (0Ah)

0Ah	RDDPM (Read Display Power Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	08

Description

This command indicates the current status of the display as described in the table below::

Bit	Value	Description	Comment
D7	0	Booster Off or has a fault.	---
	1	Booster On and working OK	---
D6	0	Idle Mode Off.	---
	1	Idle Mode On.	---
D5	0	Partial Mode Off.	---
	1	Partial Mode On.	---
D4	0	Sleep In Mode	---
	1	Sleep Out Mode	---
D3	0	Display Normal Mode Off.	---
	1	Display Normal Mode On	---
D2	0	Display is Off.	---
	1	Display is On	---
D1	--	Not Defined	Set to '0'
D0	--	Not Defined	Set to '0'

X = Don't care

Restriction

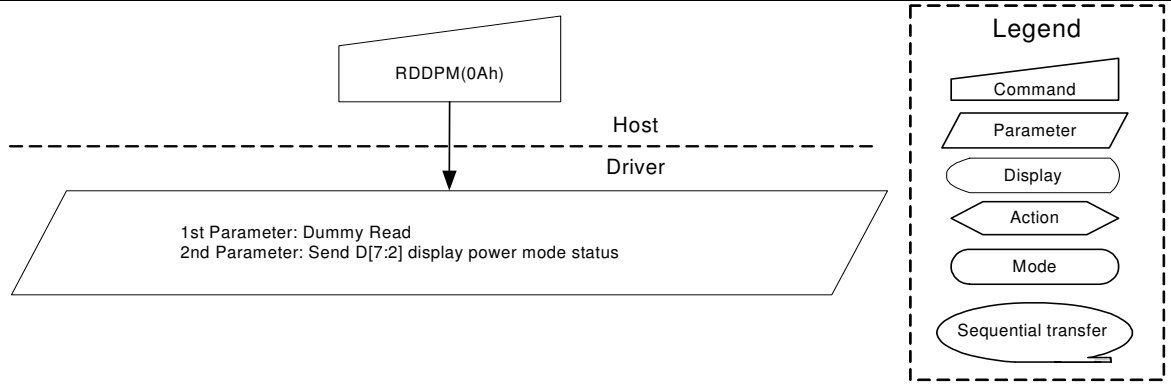
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h08h
SW Reset	8'h08h
HW Reset	8'h08h

Flow Chart



8.2.6. Read Display MADCTL (0Bh)

0Bh	RDDMADCTL (Read Display MADCTL)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	0	0	00

Description

This command indicates the current status of the display as described in the table below:

it	Valu	Description	Comment
D7	0	Top to Bottom (When MADCTL D7='0').	---
	1	Bottom to Top (When MADCTL D7='1').	---
D6	0	Left to Right (When MADCTL D6='0')	---
	1	Right to Left (When MADCTL D6='1')	---
D5	0	Normal Mode (When MADCTL D5='0').	---
	1	Reverse Mode (When MADCTL D5='1')	---
D4	0	LCD Refresh Top to Bottom (When MADCTL D4='0')	---
	1	LCD Refresh Bottom to Top (When MADCTL D4='1').	---
D3	0	RGB (When MADCTL D3='0')	---
	1	BGR (When MADCTL D3='1').	---
D2	0	LCD Refresh Left to Right (When MADCTL D2='0').	---
	1	LCD Refresh Right to Left (When MADCTL D2='1').	---
D1	--	Switching between Segment outputs and RAM	Set to '0'
D0	--	Switching between Segment outputs and RAM	Set to '0'

X = Don't care

Restriction

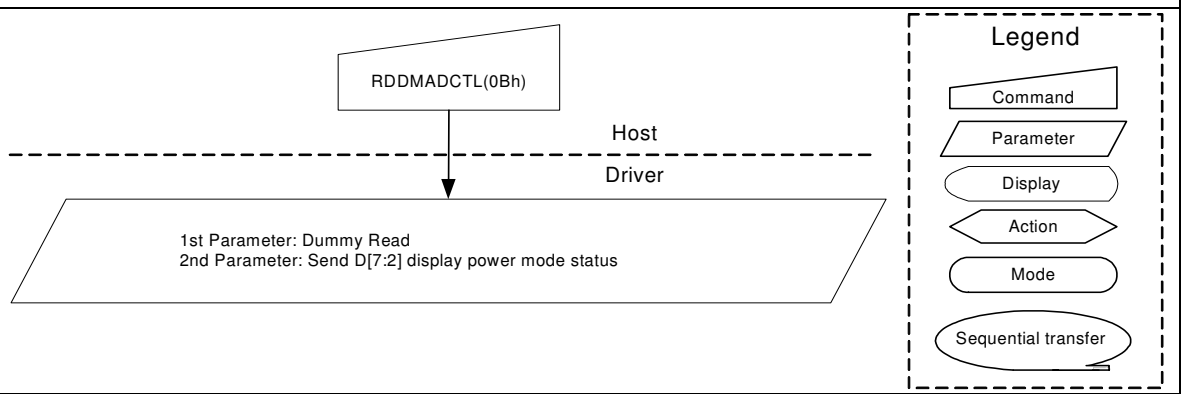
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No Change
HW Reset	8'h00h

Flow Chart



8.2.7. Read Display Pixel Format (0Ch)

0Ch	RDDCOLMOD (Read Display Pixel Format)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	X	DPI [2:0]			0	DBI [2:0]			06

Description

This command indicates the current status of the display as described in the table below:

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved
1	0	1	16 bits / pixel (6-bit 3 times data transfer)
1	1	0	18 bits / pixel (6-bit 3 times data transfer)

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

X = Don't care

Restriction

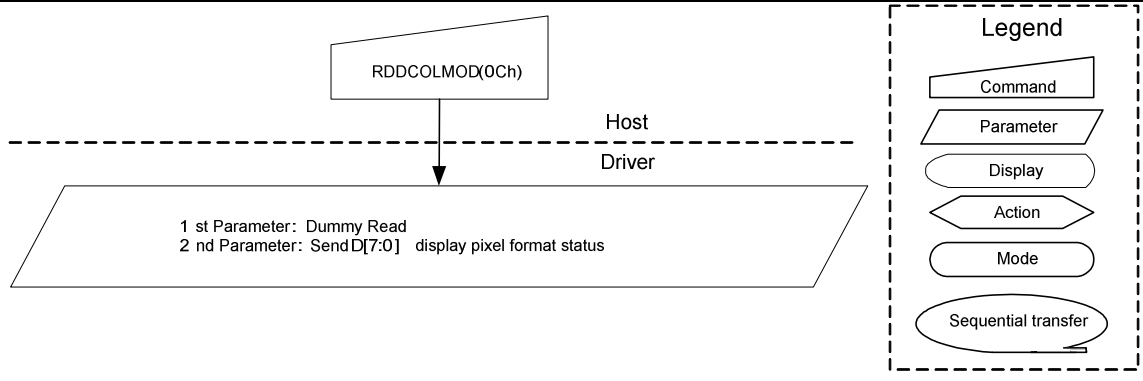
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

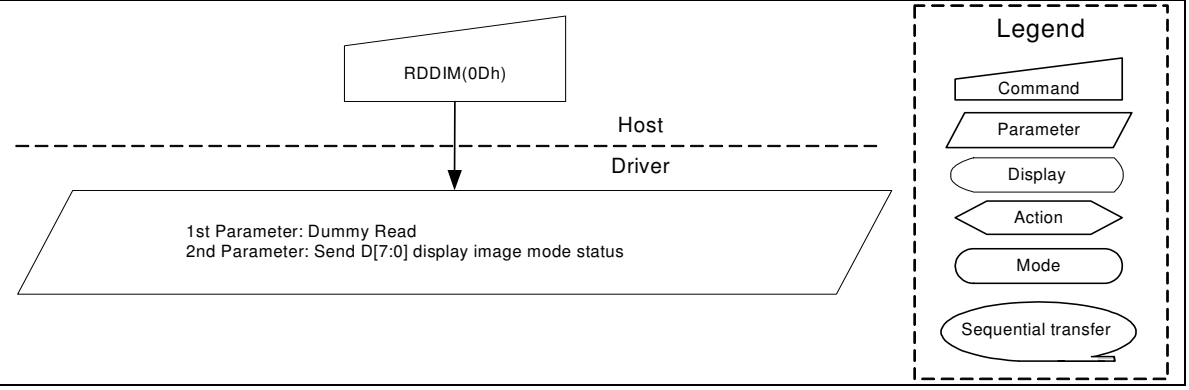
Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b000	3'b110
SW Reset	No Chang	No Chang
HW Reset	3'b000	3'b110

Flow Chart



8.2.8. Read Display Image Format (0Dh)

0Dh	RDDIM (Read Display Image Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	D [2:0]			00
Description	This command indicates the current status of the display as described in the table below: D [2:0] / Description 000 / Gamma curve 1 (G2.2) 001 / Gamma curve 2 (G1.8) 010 / Gamma curve 3 (G2.5) 011 / Gamma curve 4 (G1.0) Other / Not defined X = Don't care												
Restriction													
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Partial Mode On, Idle Mode Off, Sleep Out / Yes Partial Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes												
Default	Status / Default Value Power On Sequence / 3'b000 SW Reset / 3'b000 HW Reset / 3'b000												
Flow Chart													

8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Value	Description
D7	0	Tearing effect line OFF
	1	Tearing effect line ON
D6	0	Tearing effect line mode 1
	1	Tearing effect line mode 2
D5	0	Horizontal sync. (RGB interface) OFF
	1	Horizontal sync. (RGB interface) ON
D4	0	Vertical sync. (RGB interface) OFF
	1	Vertical sync. (RGB interface) ON
D3	0	Pixel clock (DOTCLK, RGB interface) OFF
	1	Pixel clock (DOTCLK, RGB interface) ON
D2	0	Data enable (DE, RGB interface) OFF
	1	Data enable (DE, RGB interface) ON
D1	0	Reserved
D0	0	Reserved

X = Don't care

Restriction

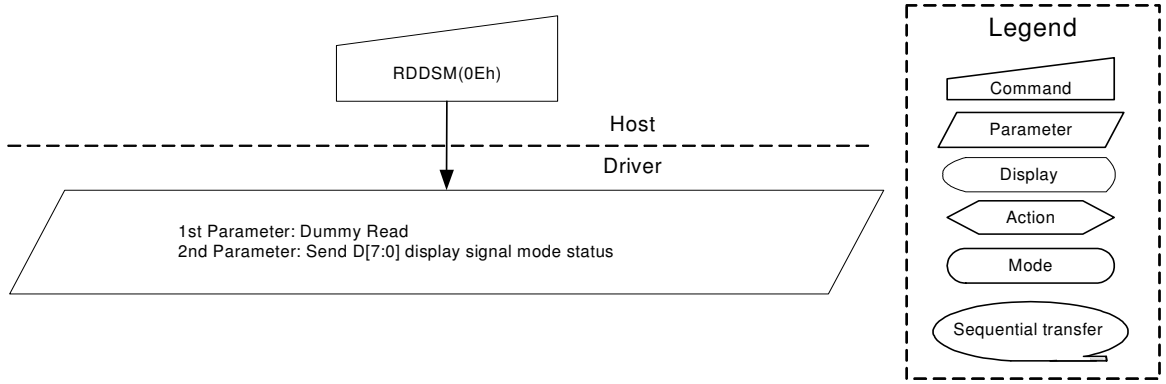
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	RDDSDR (Read Display Self-Diagnostic Result)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detect on	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

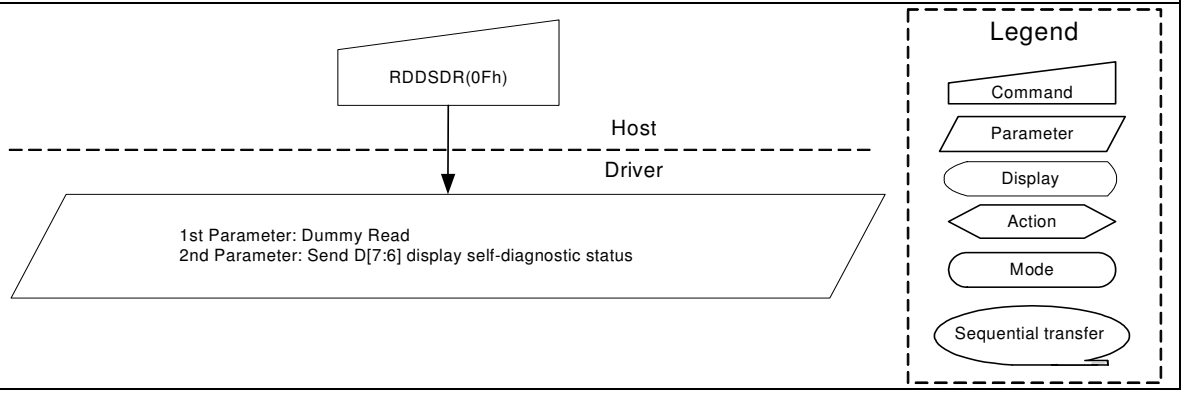
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.11. Enter Sleep Mode (10h)

10h	SPLIN (Enter Sleep Mode)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Parameter	No Parameter												
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. Out → Blank → STOP MCU interface and memory are still working and the memory keeps its contents. X = Don't care												
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.												

Register Availability

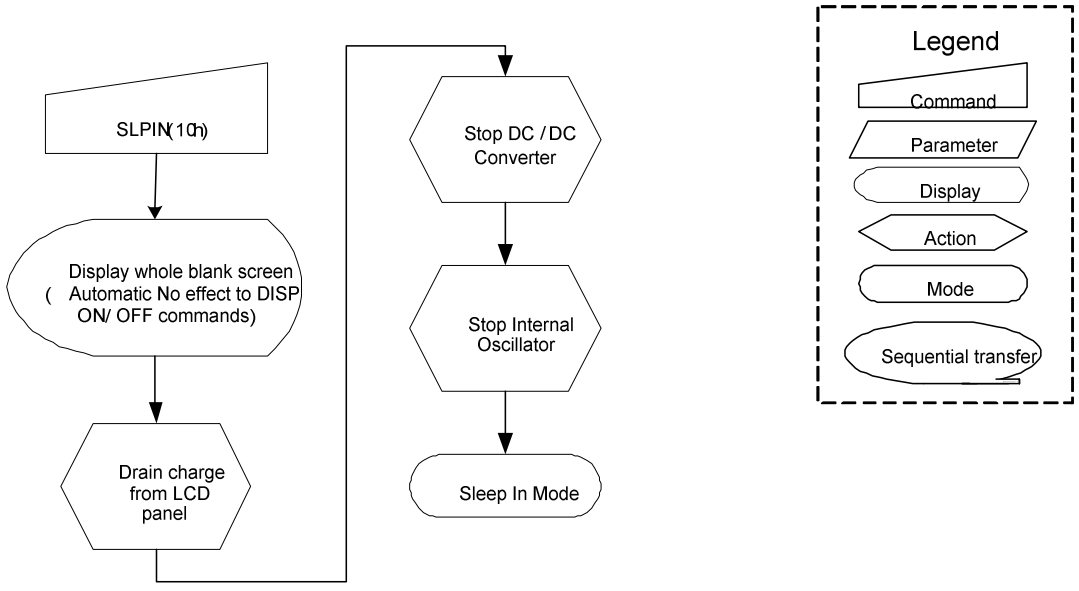
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

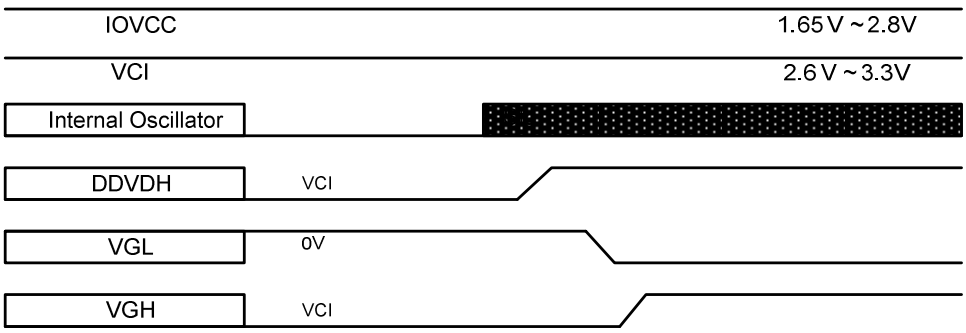
Status	Default Value
Power On Sequence	Sleep IN Mode
SW Reset	Sleep IN Mode
HW Reset	Sleep IN Mode

Flow Chart

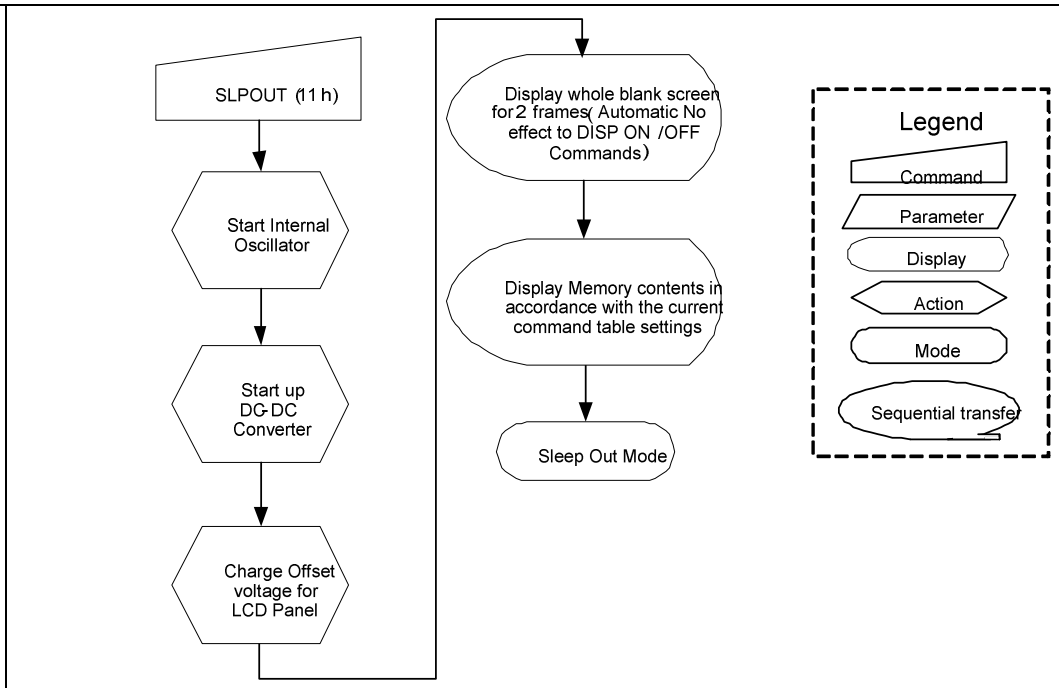
It takes 120msec to get into Sleep In mode after SLPIN command issued.



8.2.12. Sleep Out (11h)

<table>
<tr><th>11h</th><th colspan="13">SLPOUT (Sleep Out)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 120msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">It takes 120msec to become Sleep Out mode after SLPOUT command issued.</td></tr>
</table>



8.2.13. Partial Mode ON (12h)

12h	PTLON (Partial Mode On)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Parameter	No Parameter												
Description	This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. X = Don't care												
Restriction	This command has no effect when Partial mode is active.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Display Mode ON
SW Reset	Normal Display Mode ON
HW Reset	Normal Display Mode ON

Flow Chart	See Partial Area (30h)

8.2.14. Normal Display Mode ON (13h)

<table>
<tr><th>13h</th><th colspan="12">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

8.2.15. Display Inversion OFF (20h)

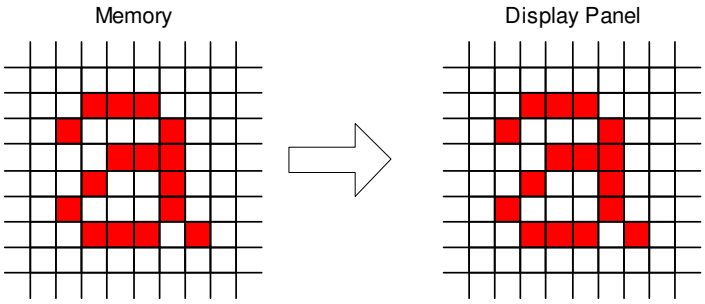
20h	DINVOFF (Display Inversion OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												

Description

This command is used to recover from display inversion mode.

This command makes no change of the content of frame memory.

This command doesn't change any other status.



X = Don't care

Restriction

This command has no effect when module already is inversion OFF mode.

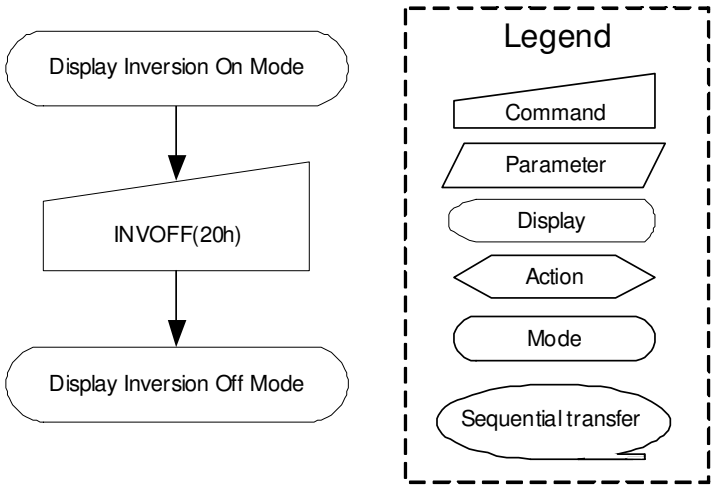
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.16. Display Inversion ON (21h)

21h	DINVON (Display Inversion ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												

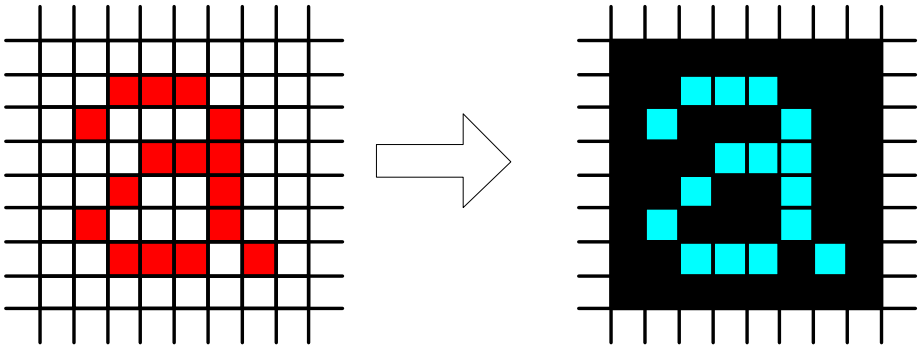
Description

This command is used to enter into display inversion mode.

This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.

This command doesn't change any other status.

To exit Display inversion mode, the Display inversion OFF command (20h) should be written.



X = Don't care

Restriction

This command has no effect when module already is inversion ON mode.

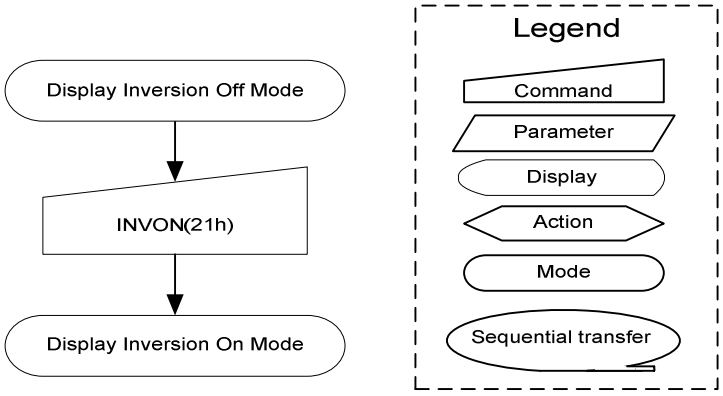
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



8.2.17. Gamma Set (26h)

26h	GAMSET (Gamma Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	↑	XX	GC [7:0]								01

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:

GC [7:0]	Curve Selected
01h	Gamma curve 1 (G2.2)
02h	Gamma curve 2 (G1.8)
04h	Gamma curve 3 (G2.5)
08h	Gamma curve 4 (G1.0)

Note: All other values are undefined.

X = Don't care

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.

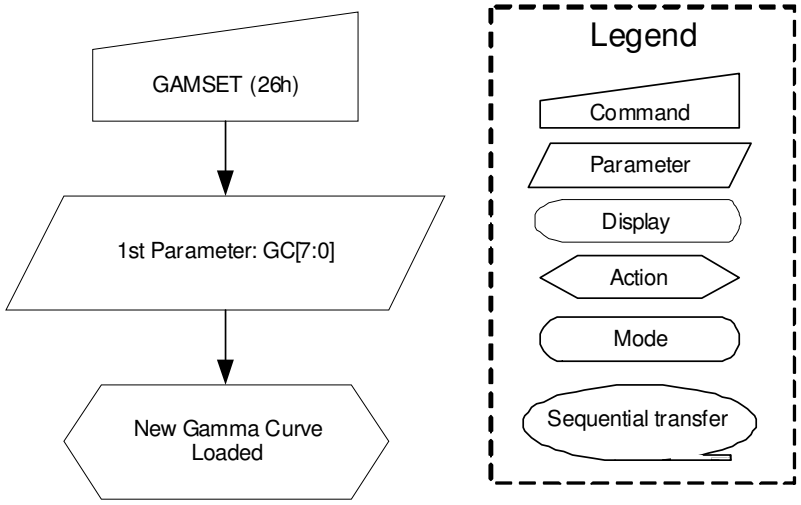
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

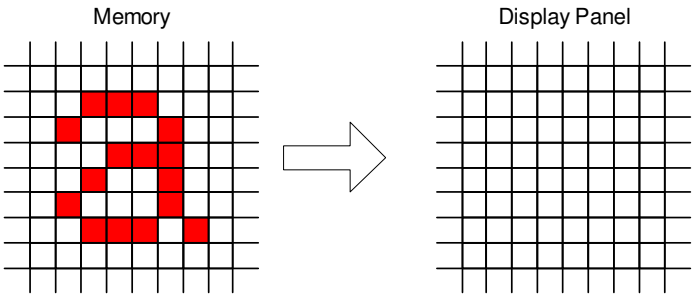
Default

Status	Default Value
Power On Sequence	8'h01h
SW Reset	8'h01h
HW Reset	8'h01h

Flow Chart



8.2.18. Display OFF (28h)

28h	DISPOFF (Display OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care.												
Restriction	This command has no effect when module is already in display off mode.												

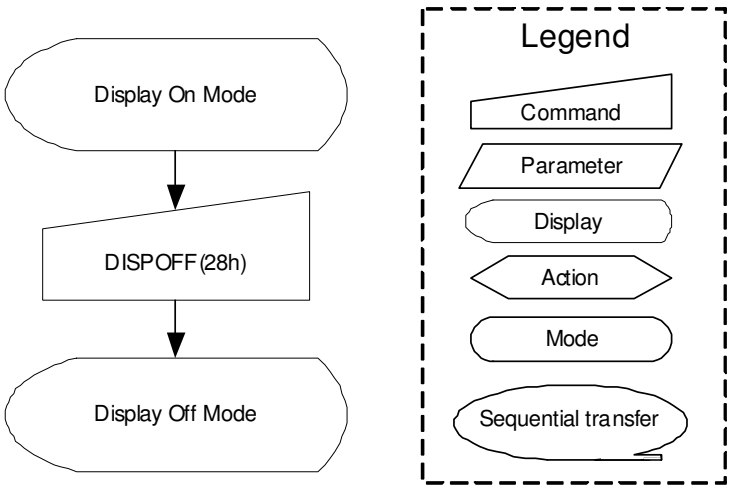
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



8.2.19. Display ON (29h)

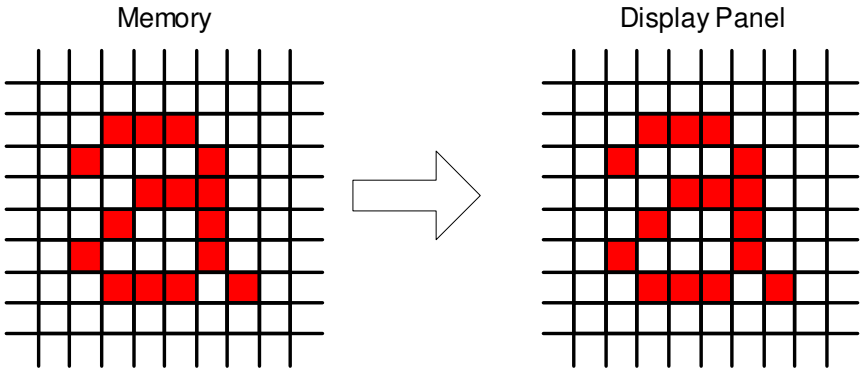
29h	DISPON (Display ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Parameter	No Parameter												

Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.

This command makes no change of contents of frame memory.

This command does not change any other status



X = Don't care.

Restriction

This command has no effect when module is already in display on mode.

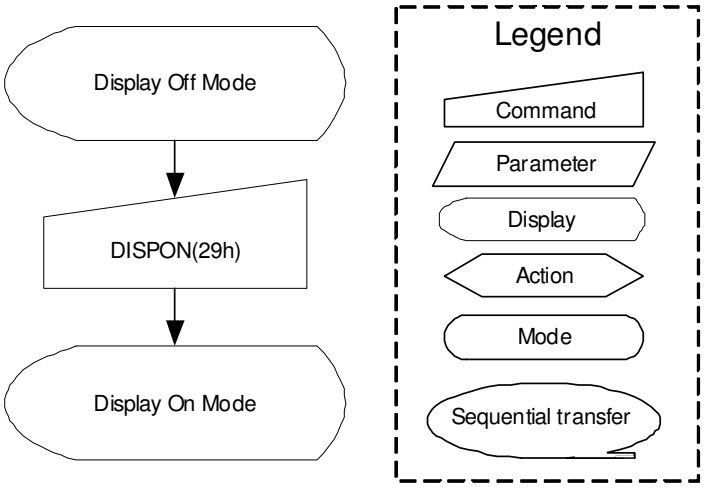
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

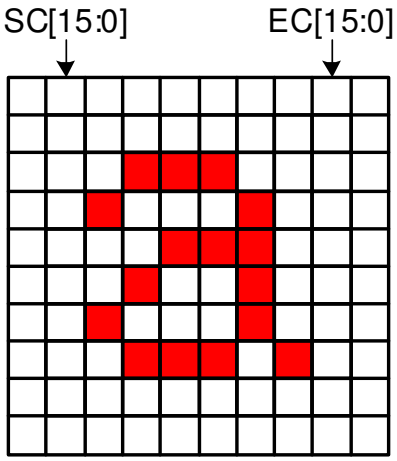


8.2.20. Column Address Set (2Ah)

2Ah	CASET (Column Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2ndParameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's D5 = 0) or 013Fh (When MADCTL's D5 = 1), data of out of range will be ignored

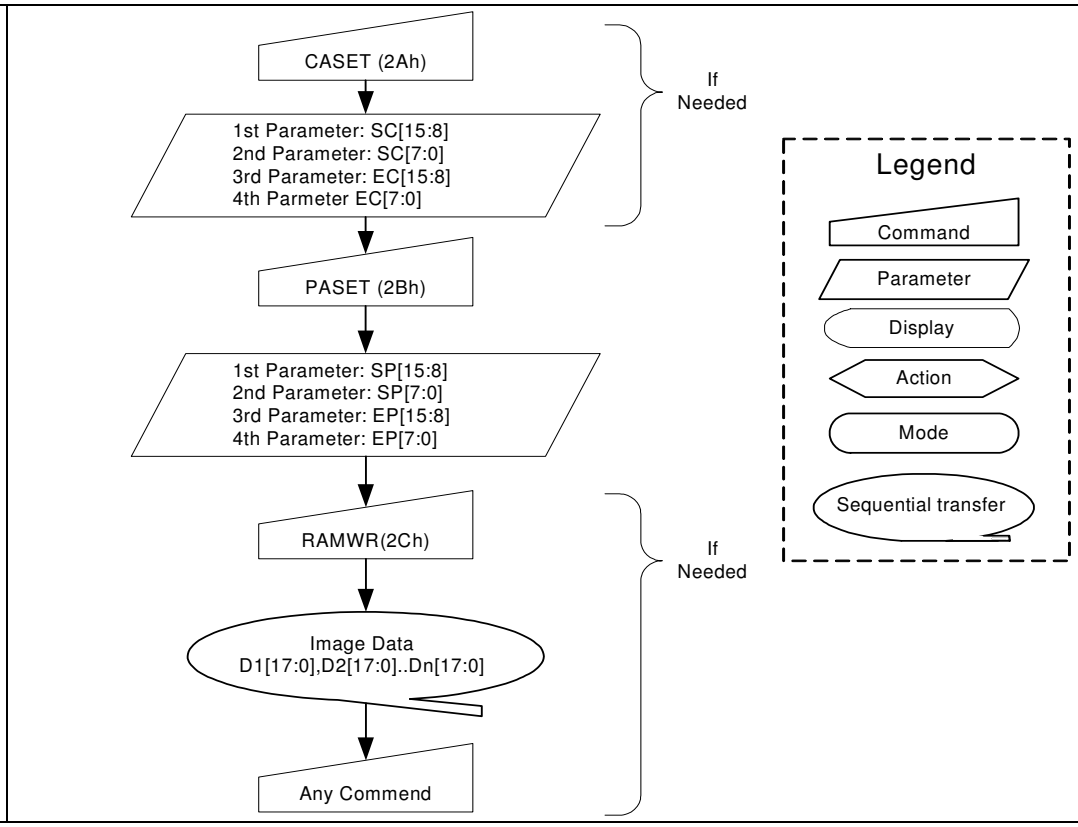
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=013Fh
SW Reset	SC [15:0]=0000h	If MADCTL's D5 = 0: EC [15:0]=013Fh If MADCTL's D5 = 1: EC [15:0]=00EFh
HW Reset	SC [15:0]=0000h	EC [15:0]=013Fh

Flow Chart

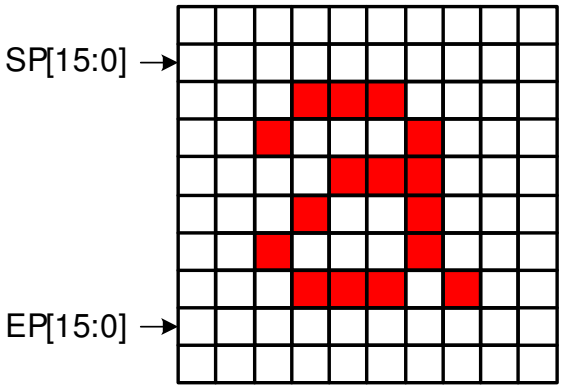


8.2.21. Page Address Set (2Bh)

2Bh	PASET (Page Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2ndParameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rdParameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP [15:0] always must be equal to or less than EP [15:0]

Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's D5 = 0) or 00EFh (When MADCTL's D5 = 1), data of out of range will be ignored.

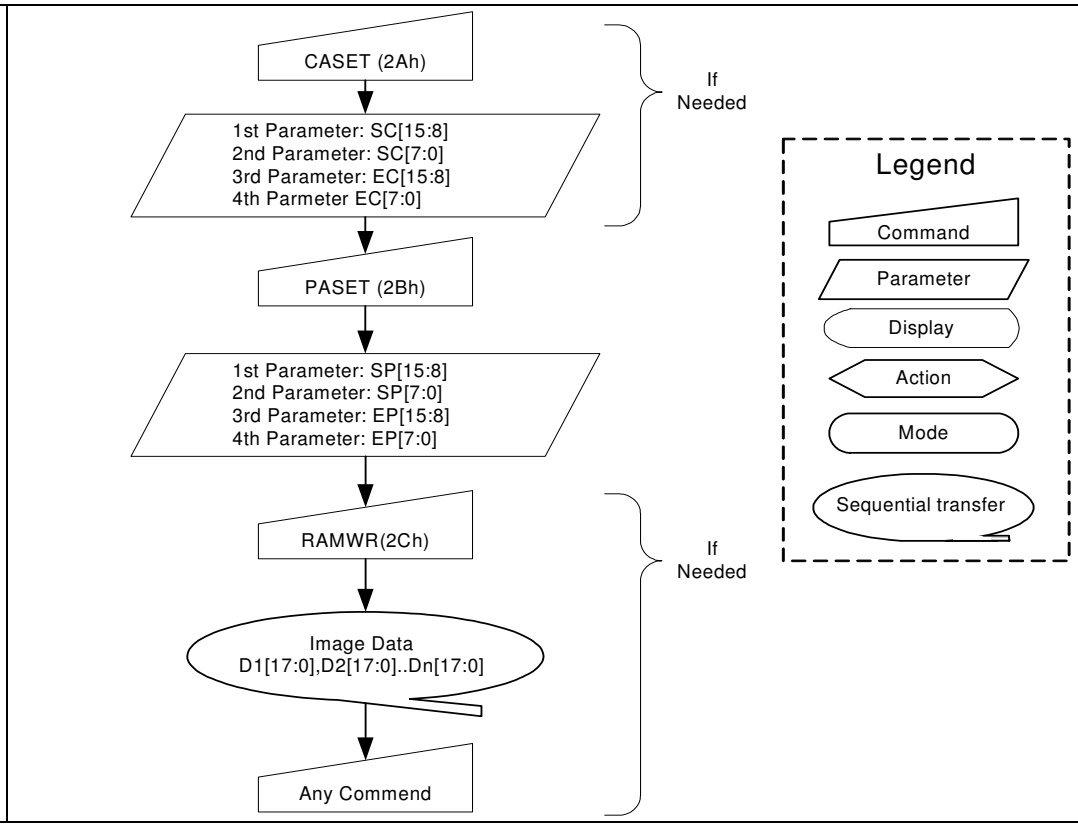
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=00EFh
SW Reset	SP [15:0]=0000h	If MADCTL's D5 = 0: EP [15:0]=00EFh If MADCTL's D5 = 1: EP [15:0]=013Fh
HW Reset	SP [15:0]=0000h	EP [15:0]=00EFh

Flow Chart



8.2.22. Memory Write (2Ch)

2Ch	RAMWR (Memory Write)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.												
Restriction	In all color modes, there is no restriction on length of parameters.												

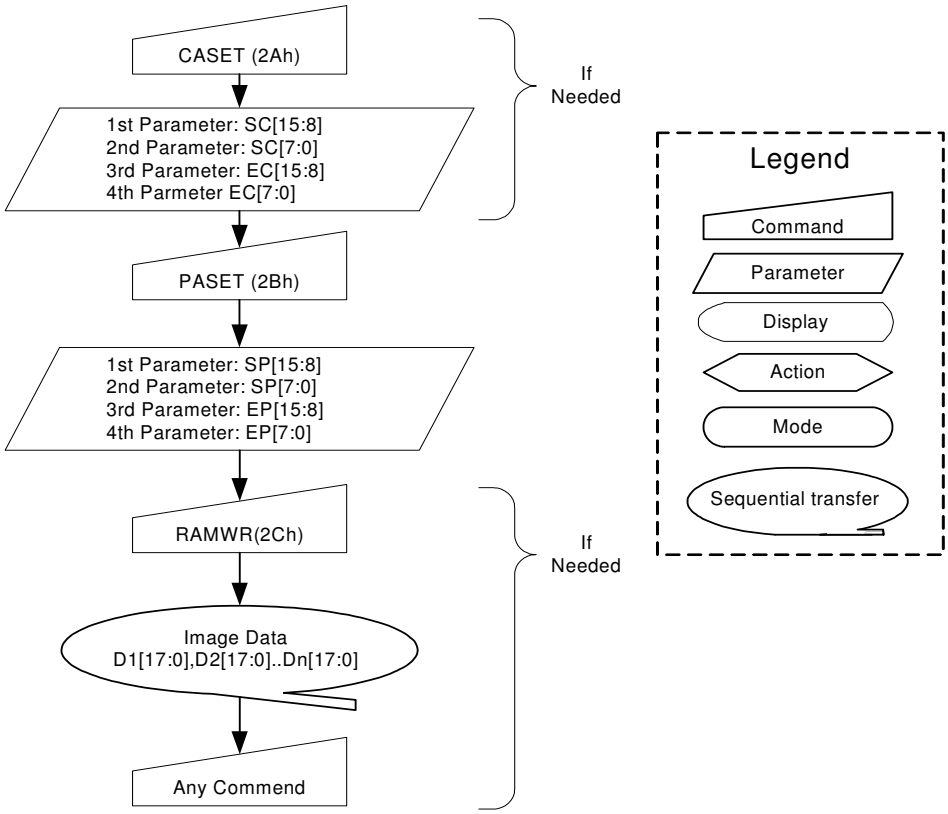
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



8.2.23. Color Set (2Dh)

2Dh	RGBSET (Color Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh
1st Parameter	1	1	↑	XX	R00 [5:0]								XX
nth Parameter	1	1	↑	XX	Rnn [5:0]								XX
32ndParameter	1	1	↑	XX	R31 [5:0]								XX
33rdParameter	1	1	↑	XX	G00 [5:0]								XX
nth Parameter	1	1	↑	XX	Gnn [5:0]								XX
96thParameter	1	1	↑	XX	G64 [5:0]								XX
97thParameter	1	1	↑	XX	B00 [5:0]								XX
nth Parameter	1	1	↑	XX	Bnn [5:0]								XX
128thParameter	1	1	↑	XX	B31 [5:0]								XX
Description	This command is used to define the LUT for 16-bit to 18-bit color depth conversion. 128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.4 are referred. This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.												
Restriction													

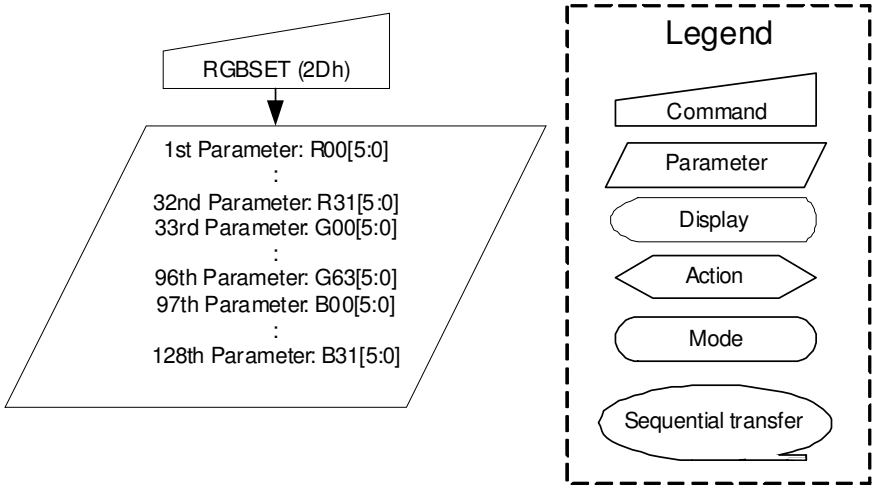
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Random values
SW Reset	Contents of LUT protected
HW Reset	Random values

Flow Chart



8.2.24. Memory Read (2Eh)

2Eh	RAMRD (Memory Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
(N+1)th Parameter	1	1	↑	Dn [17:0]									XX

Description

This command transfers image data from ILI9342C's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.

If Memory Access control D5 = 0:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.

If Memory Access Control D5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.

Restriction

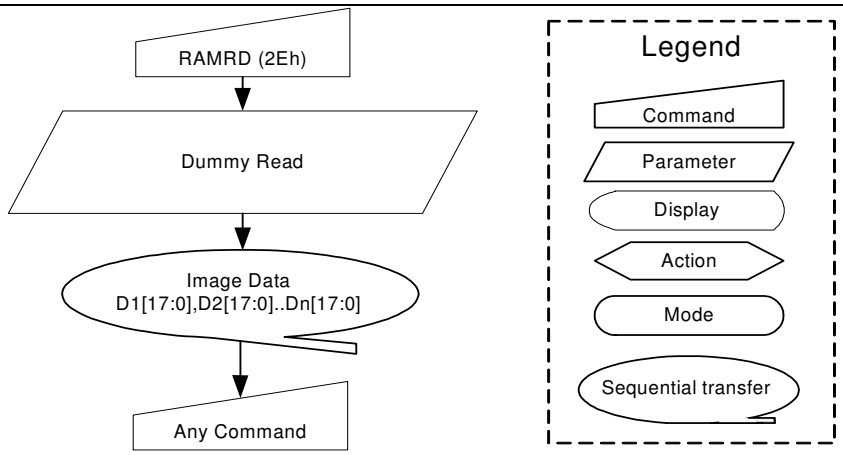
There is no restriction on length of parameters.

Register Availability

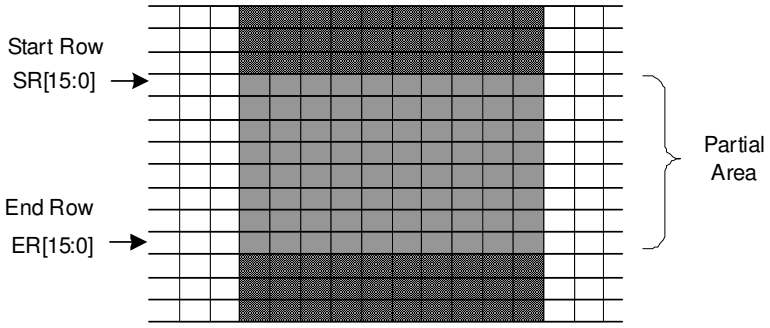
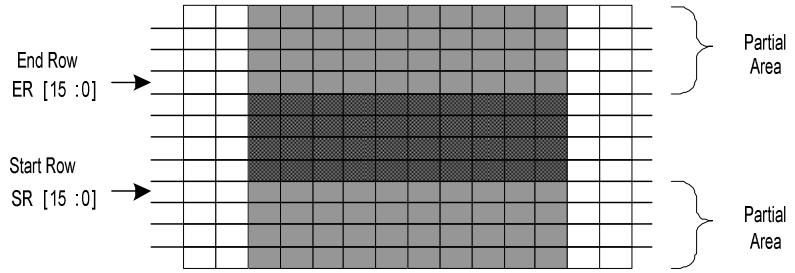
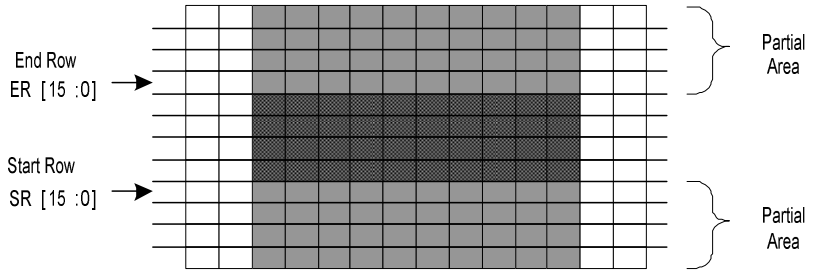
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

8.2.25. Partial Area (30h)

30h	PLTAR (Partial Area)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2ndParameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rdParameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	00
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	EF
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL D4=0:-  If End Row>Start Row when MADCTL D4=1:-  If End Row<Start Row when MADCTL D4=0:-  If End Row = Start Row then the Partial Area will be one row deep. X = Don't care.												
Restriction	SR [15…0] and ER [15…0] cannot be 0000h nor exceed 00EFh.												

Register Availability

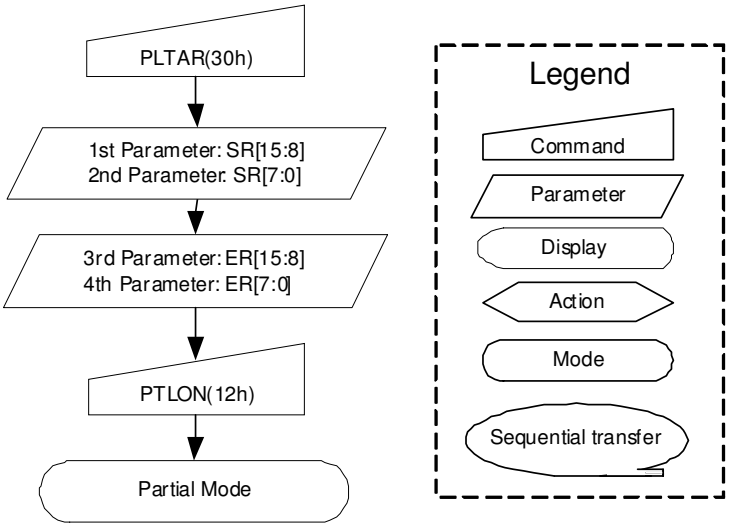
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

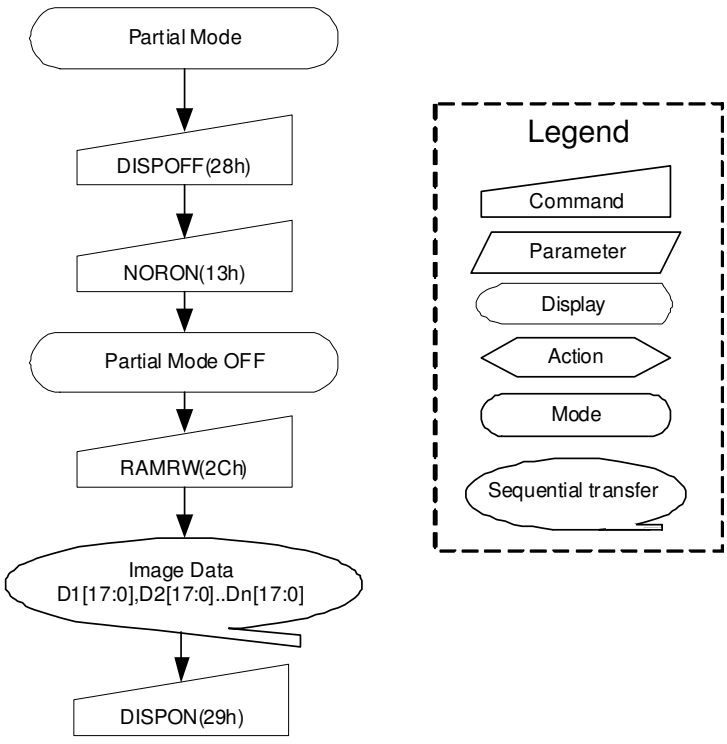
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h00EFh
SW Reset	16'h 0000h	16'h00EFh
HW Reset	16'h 0000h	16'h00EFh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



8.2.26. Vertical Scrolling Definition (33h)

33h	VSCRDEF (Vertical Scrolling Definition)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								00
4th Parameter	1	1	↑	XX	VSA [7:0]								F0
5th Parameter	1	1	↑	XX	BFA [15:8]								00
6th Parameter	1	1	↑	XX	BFA [7:0]								00

Description

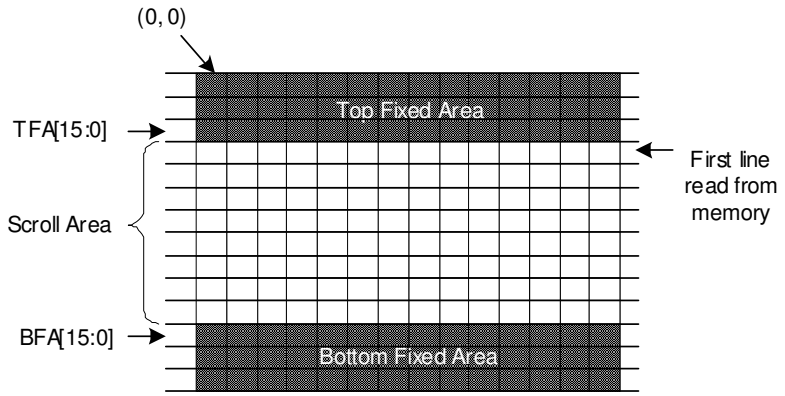
This command defines the Vertical Scrolling Area of the display.

When MADCTL D4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

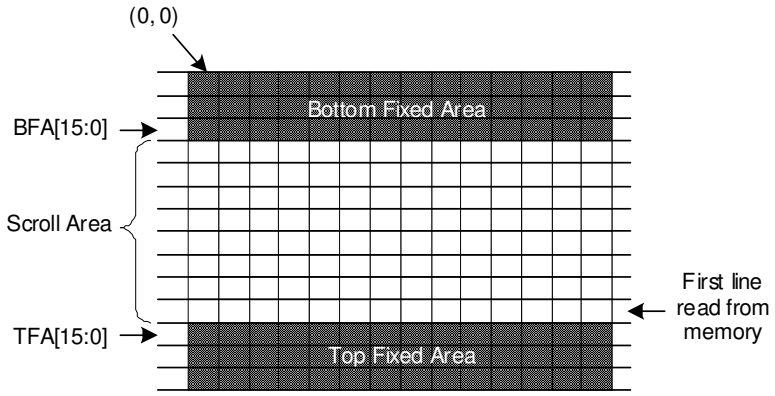


When MADCTL D4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



X = Don't care

Restriction

Register Availability

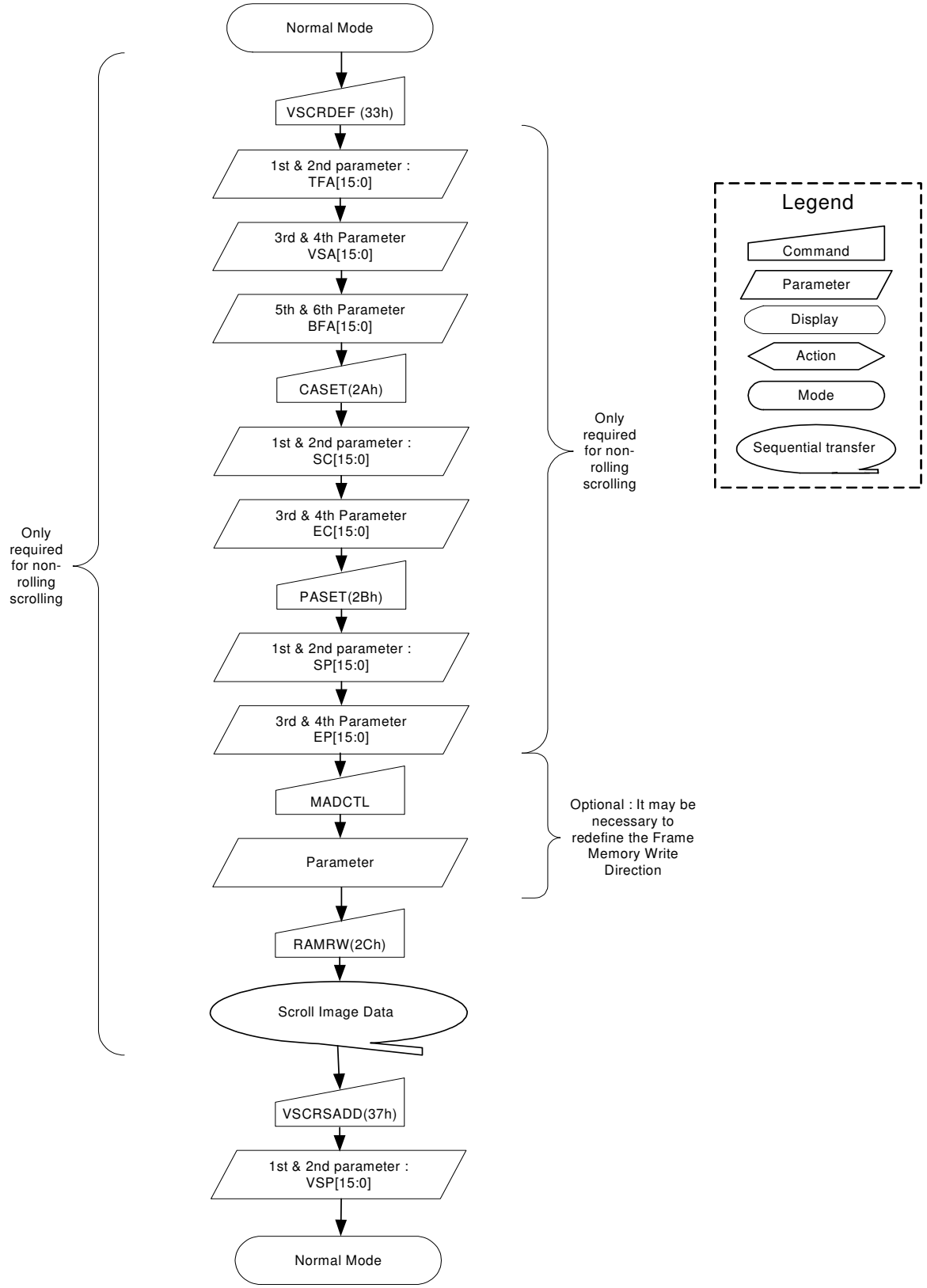
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	TFA [15:0]	VSA [15:0]	BFA [15:0]
Power On Sequence	16'h0000h	16'h00F0h	16'h0000h
SW Reset	16'h0000h	16'h00F0h	16'h0000h
HW Reset	16'h0000h	16'h00F0h	16'h0000h

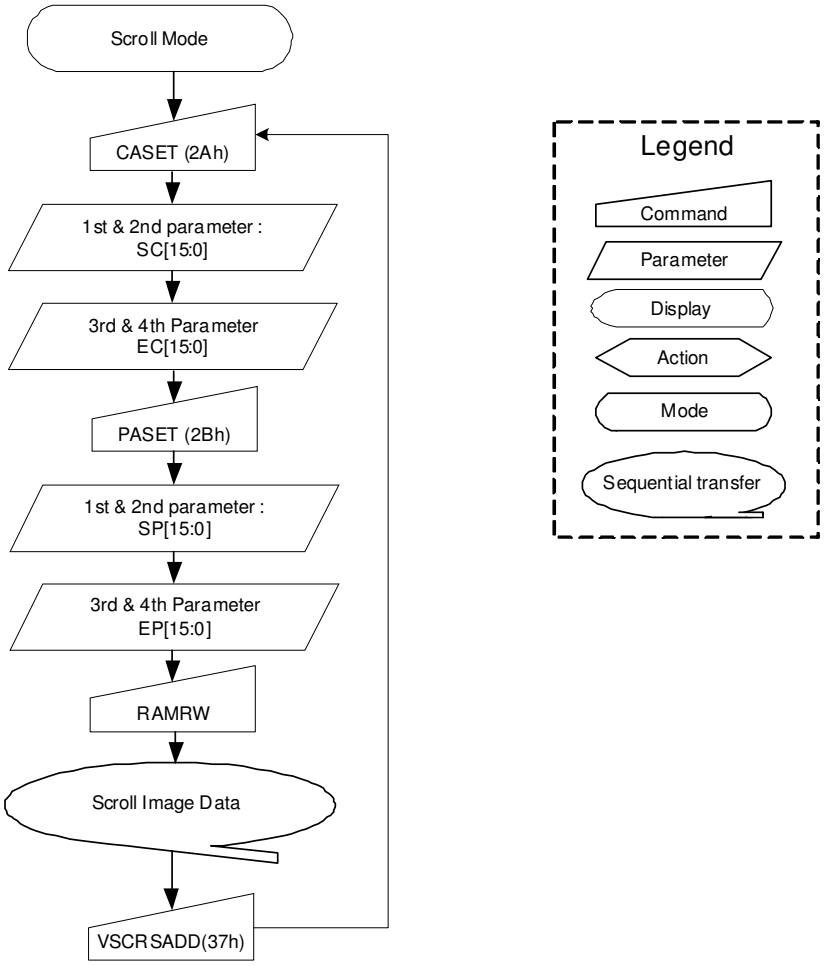
Flow Chart

1. To enter Vertical Scroll Mode :

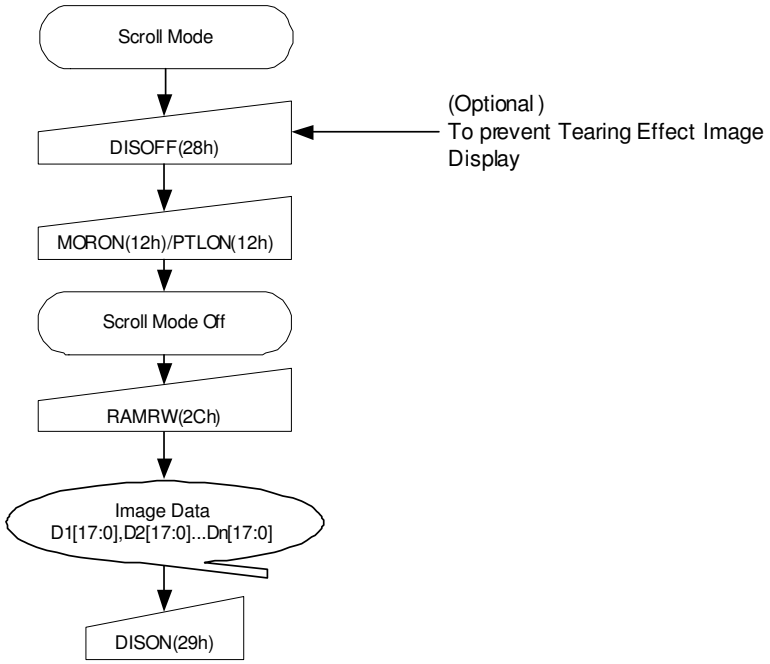


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2. Continuous Scroll :



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

8.2.27. Tearing Effect Line OFF (34h)

34h	TEOFF (Tearing Effect Line OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Parameter	No Parameter												
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.												
Restriction	This command has no effect when Tearing Effect output is already OFF.												

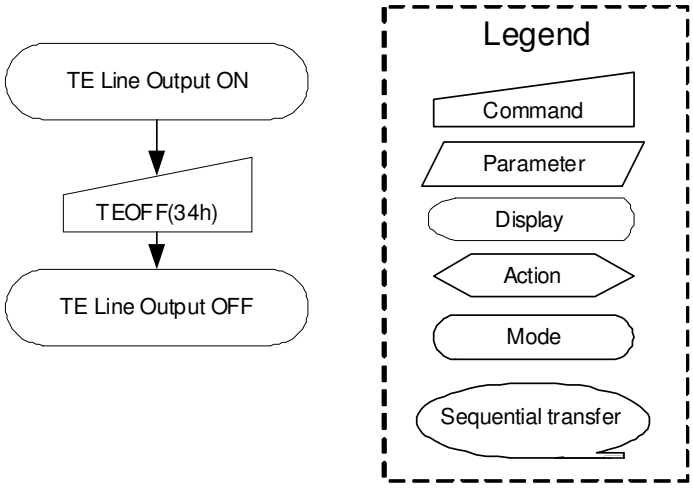
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart



8.2.28. Tearing Effect Line ON (35h)

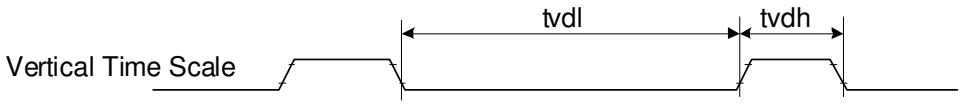
35h	TEON (Tearing Effect Line ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
Parameter	1	1	↑	XX	X	X	X	X	X	X	X	M	00

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit D4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:

The Tearing Effect Output line consists of V-Blanking information only:



When **M=1**:

The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.

X = Don't care.

Restriction

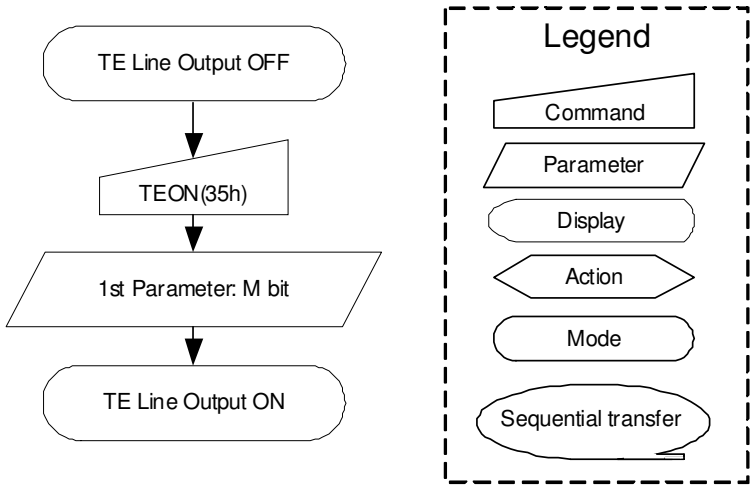
This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

Flow Chart	

8.2.29. Memory Access Control (36h)

36h	MADCTL (Memory Access Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

This command defines read/write scanning direction of frame memory.

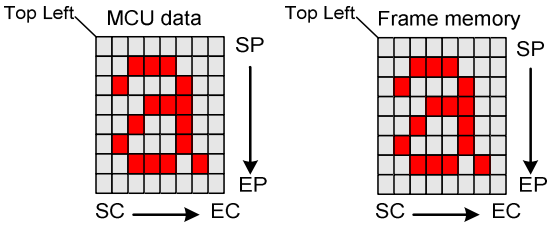
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

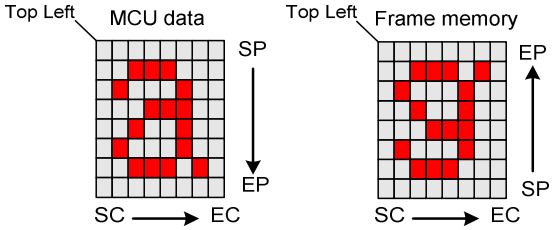
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.

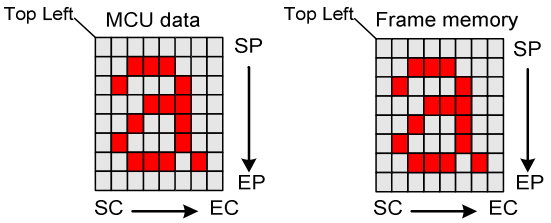
MY (Page Address Order)="0"



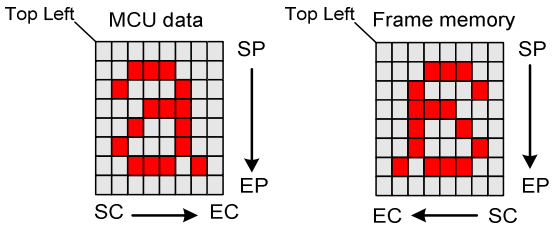
MY (Page Address Order)="1"



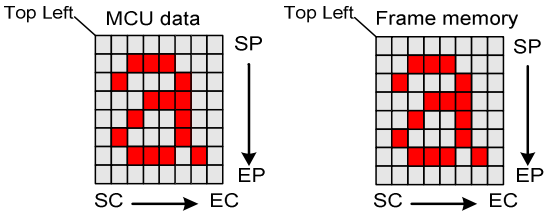
MX (Column Address Order)="0"



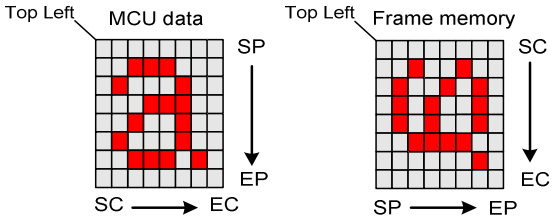
MX (Column Address Order)="1"



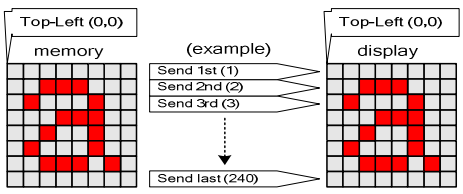
MV (Vertical Refresh Order bit)="0"



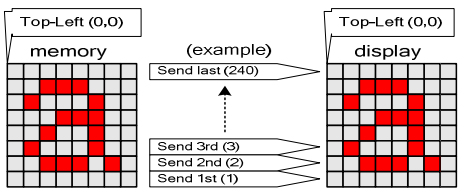
MV (Vertical Refresh Order bit)="1"

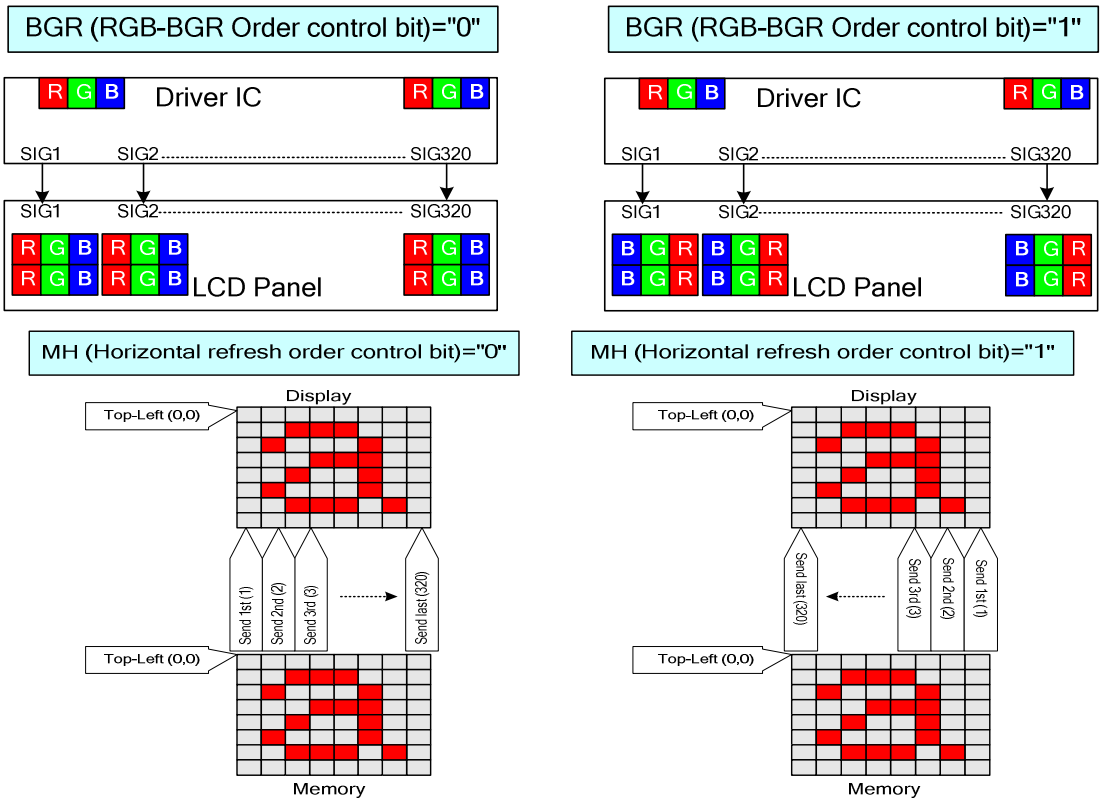


ML (Vertical refresh order bit)="0"



ML (Vertical refresh order bit)="1"





Note: Top-Left (0,0) means a physical memory location.

Restriction

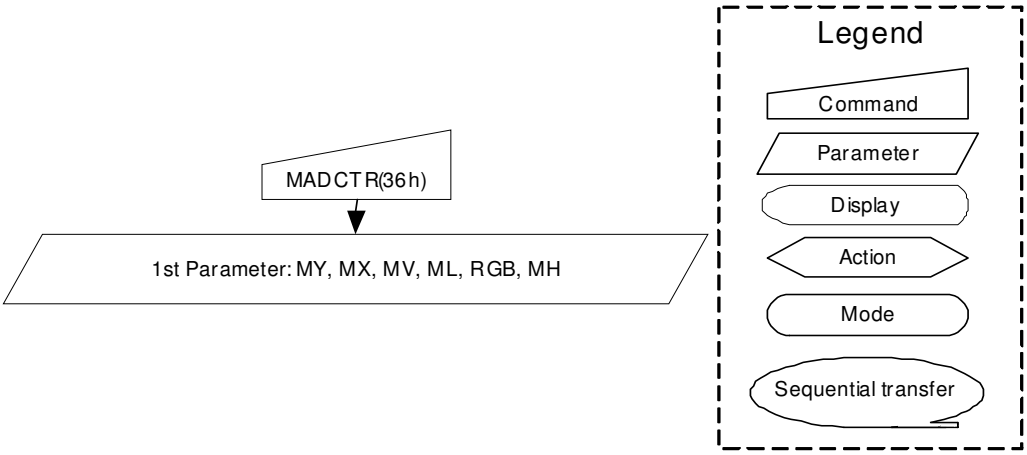
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart



8.2.30. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	↑	1	XX	VSP [15:8]								00
2nd Parameter	1	↑	1	XX	VSP [7:0]								00

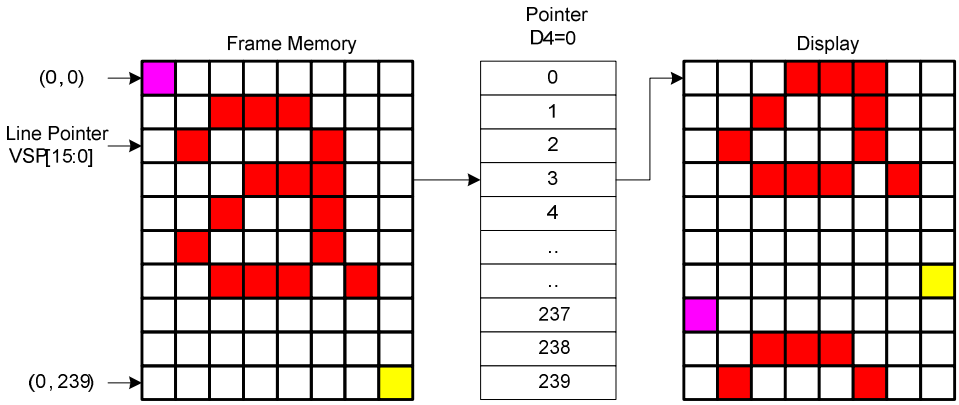
Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL D4=0

Example:

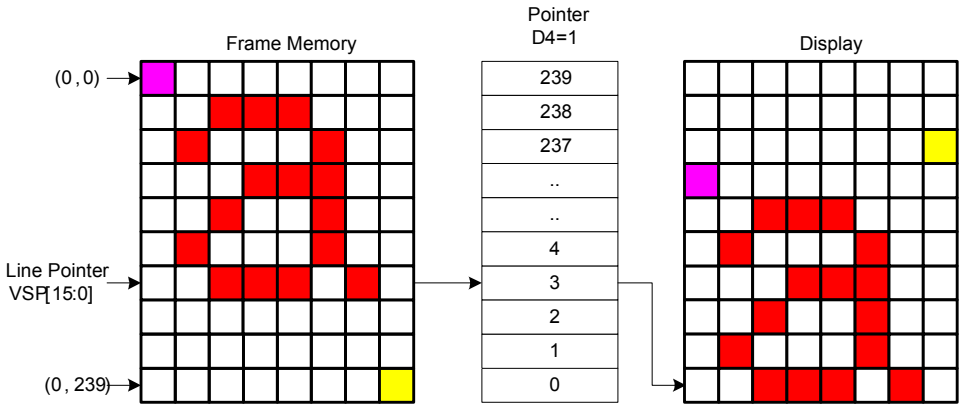
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP='3'.



When MADCTL D4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 240 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9342C enters Partial mode.

X = Don't care

Restriction

<table>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

8.2.31. Idle Mode OFF (38h)

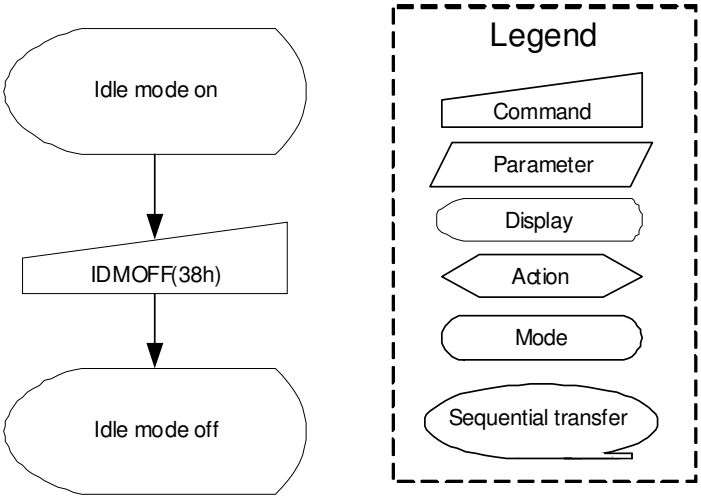
38h	IDMOFF (Idle Mode OFF)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Parameter	No Parameter												
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. X = Don't care.												
Restriction	This command has no effect when module is already in idle off mode.												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



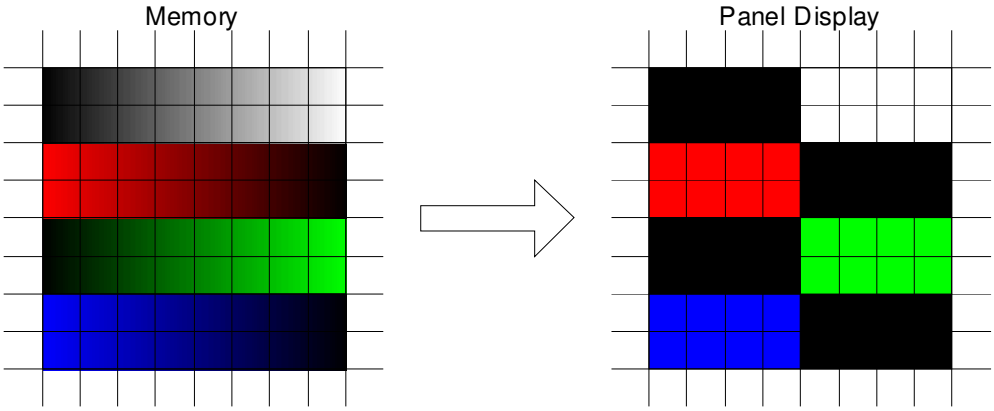
8.2.32. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Parameter	No Parameter												

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory Contents vs. Display Color			
	$R_5\ R_4\ R_3\ R_2\ R_1\ R_0$	$G_5\ G_4\ G_3\ G_2\ G_1\ G_0$	$B_5\ B_4\ B_3\ B_2\ B_1\ B_0$
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don't care.

Restriction

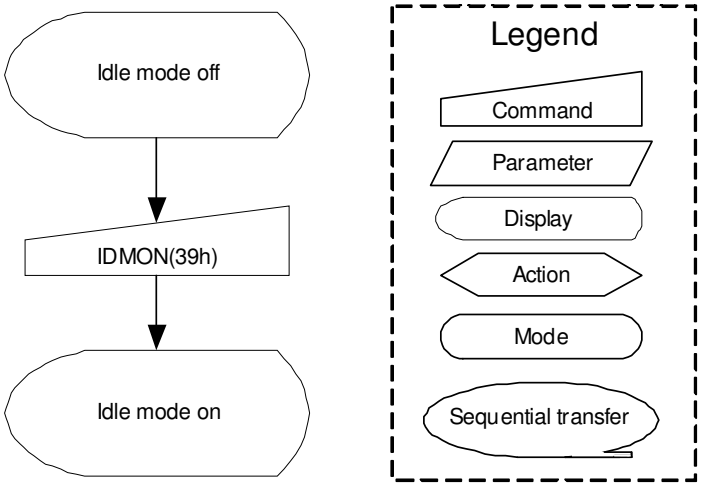
This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart	

8.2.33. COLMOD: Pixel Format Set (3Ah)

3Ah	PIXSET (Pixel Format Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
Parameter	1	1	↑	XX	0	DPI [2:0]			0	DBI [2:0]			66

Description

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

DPI [2:0]			RGB Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

DBI [2:0]			MCU Interface Format
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	16 bits / pixel
1	1	0	18 bits / pixel
1	1	1	Reserved

If using RGB Interface must selection serial interface.

X = Don't care

Restriction

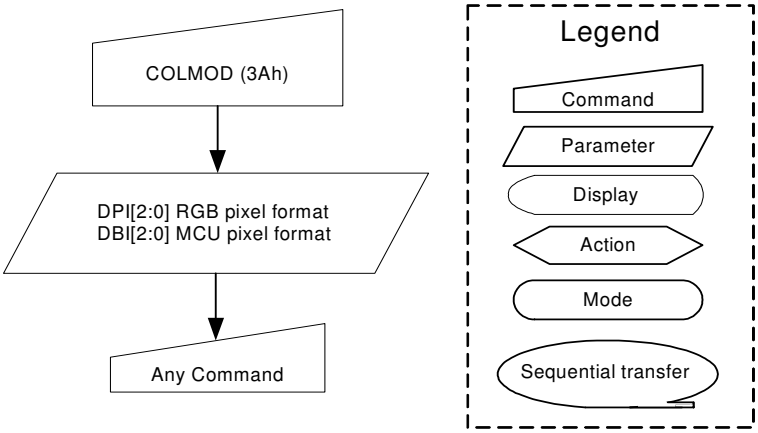
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DPI [2:0]	DBI [2:0]
Power On Sequence	3'b110	3'b110
SW Reset	No Change	No Change
HW Reset	3'b110	3'b110

Flow Chart

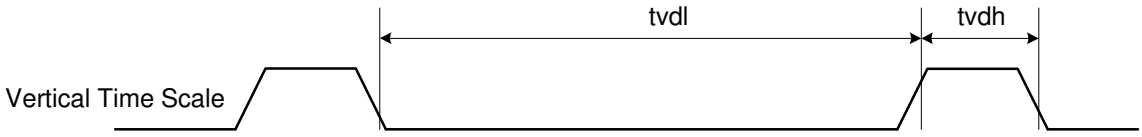


8.2.34. Set_Tear_Scanline (44h)

44h	Set_Tear_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00
2nd Parameter	1	1	↑	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00

Description

This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.



Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.

The Tearing Effect Output line shall be active low when the display module is in Sleep mode.

Restriction

-

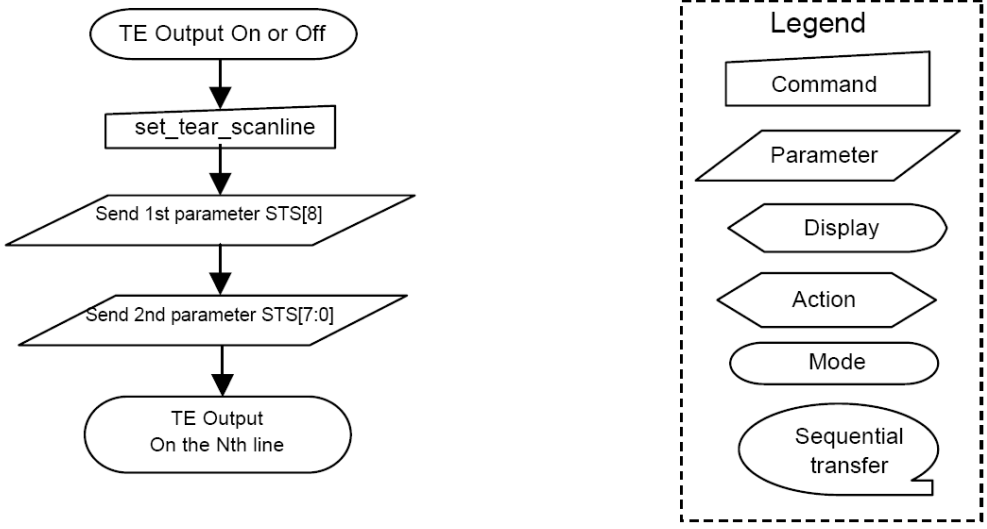
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	STS [8:0]=0000h
SW Reset	STS [8:0]=0000h
HW Reset	STS [8:0]=0000h

Flow Chart



8.2.35. Get_Scanline (45h)

45h	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00
3rd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00

Description

The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.

When in Sleep Mode, the value returned by get_scanline is undefined.

Restriction

-

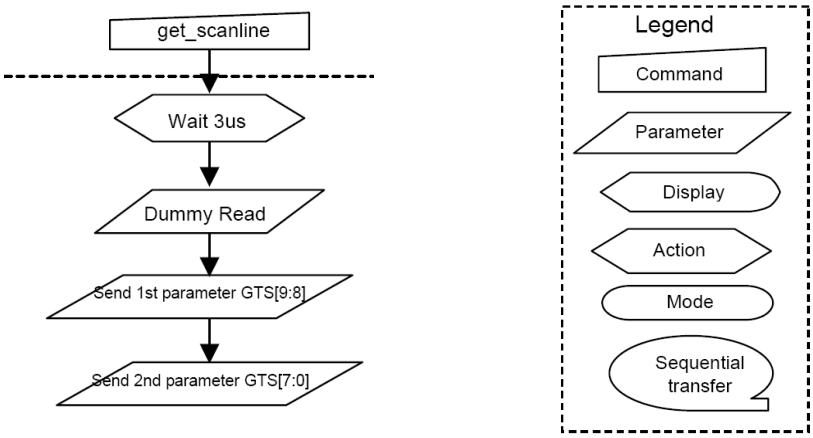
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	GTS [9:0]
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart



8.2.36. Write Display Brightness (51h)

51h	WRDISBV (Write Display Brightness)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
Parameter	1	1	↑	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												

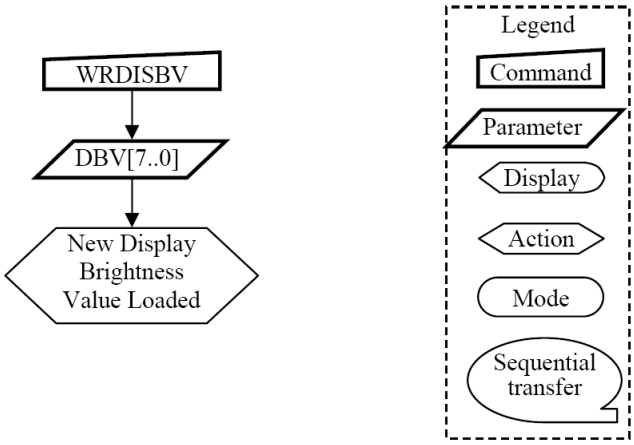
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DBV [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.37. Read Display Brightness (52h)

52h	RDDISBV (Read Display Brightness Value)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00

Description

This command returns the brightness value of the display.

It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

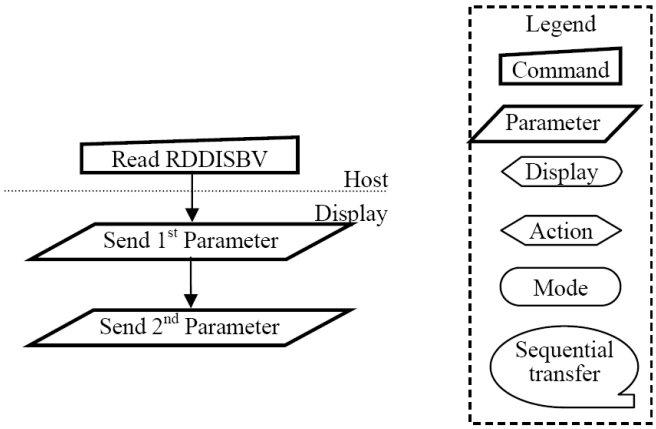
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DBV [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.38. Write CTRL Display (53h)

53h	WRCTRLD (Write Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.

0 = Off (Brightness registers are 00h, DBV[7..0])

1 = On (Brightness registers are active, according to the other parameters.)

DD: Display Dimming, only for manual brightness setting

DD = 0: Display Dimming is off

DD = 1: Display Dimming is on

BL: Backlight Control On/Off

0 = Off (Completely turn off backlight circuit. Control lines must be low.)

1 = On

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1→ 0.

When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.

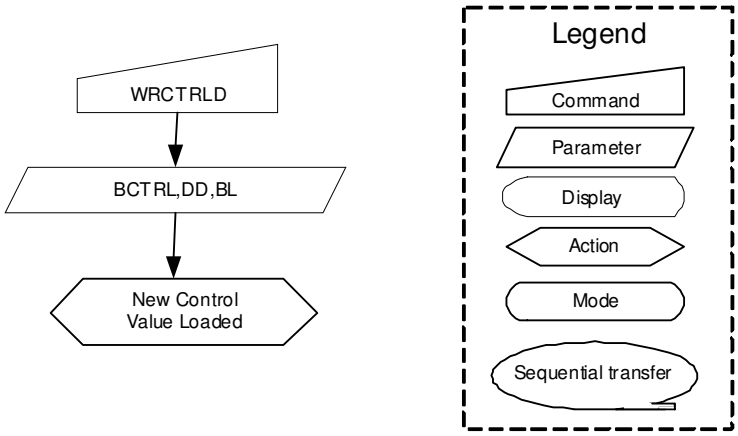
Restriction: None

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

8.2.39. Read CTRL Display (54h)

54h	RDCTRLD (Read Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00

Description

This command is used to return brightness setting.

BCTRL: Brightness Control Block On/Off,

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)

DD: Display Dimming

'0' = Display Dimming is off

'1' = Display Dimming is on

BL: Backlight On/Off

'0' = Off (Completely turn off backlight circuit. Control lines must be low.)

'1' = On

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

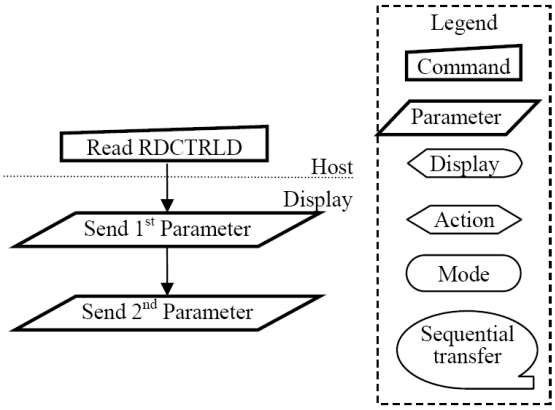
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	

8.2.40. Write Content Adaptive Brightness Control (55h)

55h	WRCABC (Write Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
Parameter	1	1	↑	XX	0	0	0	0	0	0	C [1]	C [0]	00

Description

This command is used to set parameters for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C [1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

None

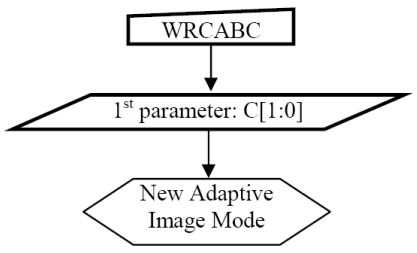
Register Availability

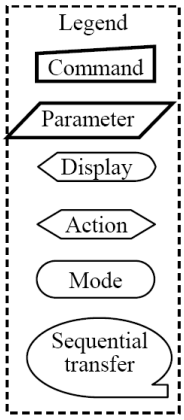
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C [1:0]=00h
SW Reset	C [1:0]=00h
HW Reset	C [1:0]=00h

Flow Chart





8.2.41. Read Content Adaptive Brightness Control (56h)

56h	RDCABC (Read Content Adaptive Brightness Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	C [1]	C [0]	00

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C [1:0]	Default Value
2'b00	Off
2'b01	User Interface Image
2'b10	Still Picture
2'b11	Moving Image

Restriction

The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.

Only 2nd parameter is sent on DSI (The 1st parameter is not sent).

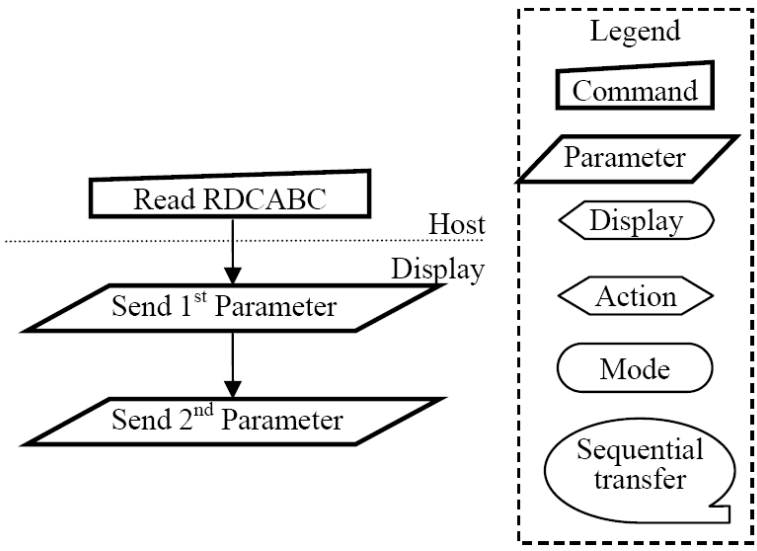
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	C [1:0]=00h
SW Reset	C [1:0]=00h
HW Reset	C [1:0]=00h

Flow Chart



8.2.42. Write CABC Minimum Brightness (5Eh)

5Eh	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
Parameter	1	1	↑	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00
Description	This command is used to set the minimum brightness value of the display for CABC function. CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction. When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal. When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)"), CABC minimum brightness setting is ignored. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CMB [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

8.2.43. Read CABC Minimum Brightness (5Fh)

5Fh	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	5Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00

Description

This command returns the minimum brightness value of CABC function.

In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

CMB[7:0] is CABC minimum brightness specified with "Write CABC minimum brightness (5Eh)" command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	CMB [7:0]
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

8.2.44. Read Automatic Brightness Control Self-Diagnostic Result (68h)

68h	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	1	0	1	0	0	0	68h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality
D5	Not Used	'0'
D4	Not Used	'0'
D3	Not Used	'0'
D2	Not Used	'0'
D1	Not Used	'0'
D0	Not Used	'0'

Restriction

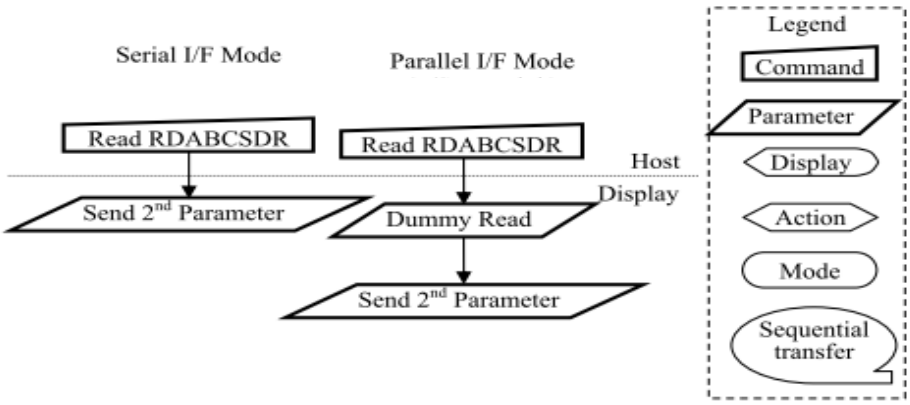
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	8'h00h
HW Reset	8'h00h

Flow Chart



8.2.45. Read ID1 (DAh)

DAh	RDID1 (Read ID1)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1 [7:0]								E3
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction													

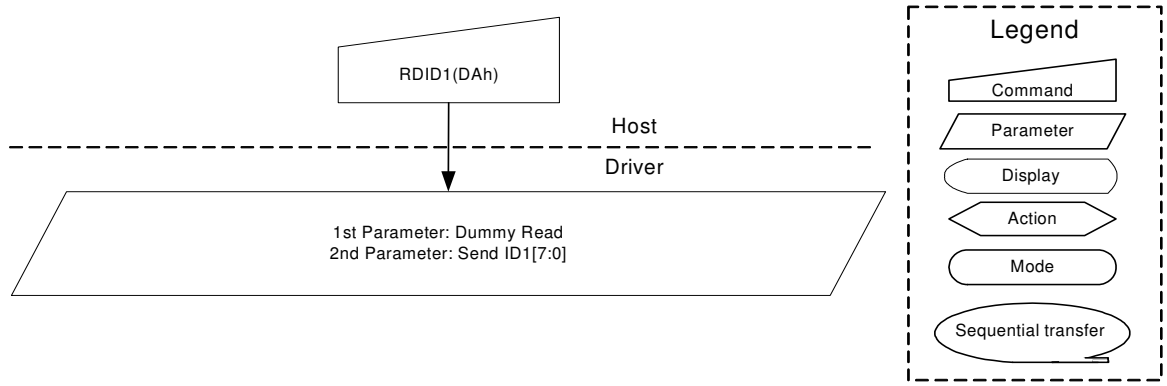
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



8.2.46. Read ID2 (DBh)

DBh	RDID2 (Read ID2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2ndParameter	1	↑	1	XX	1	ID2 [6:0]							00
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction													

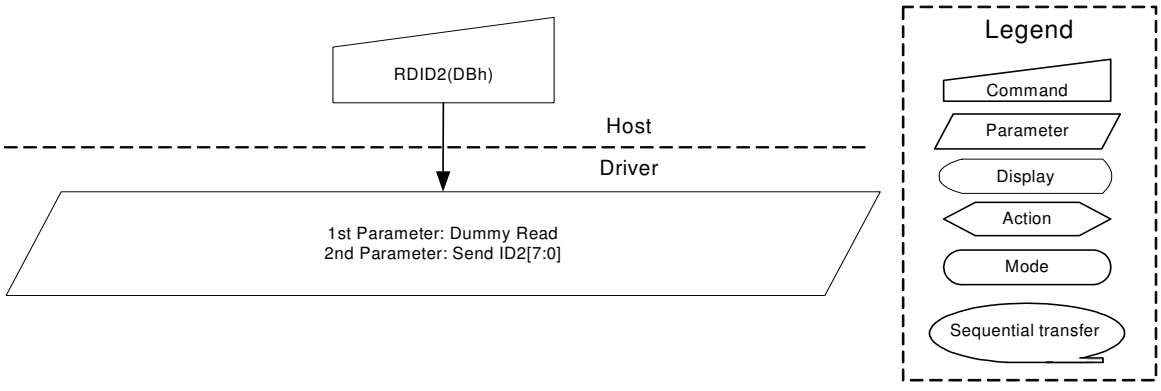
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h80h	MTP value
SW Reset	8'h80h	MTP value
HW Reset	8'h80h	MTP value

Flow Chart



8.2.47. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								00
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver ID. The ID3 can be programmed by MTP function. X = Don't care												
Restriction													

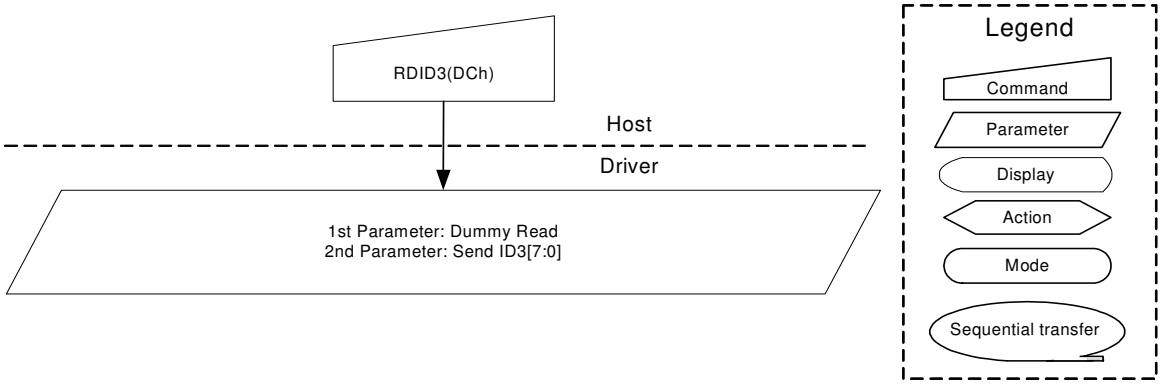
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

B0h	IFMODE (Interface Mode Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
Parameter	1	1	↑	XX	ByPass_MODE	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40

Description

Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.

EPL: DE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface)

DPL: DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time)

HSPL: HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

VSPL: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)

RCM [1:0]: RGB interface selection (refer to the RGB interface section).

ByPass_MODE: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.

ByPass_MODE	Display Data Path
0	Direct to Shift Register (**default**)
1	Memory

Restriction

Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value					
	ByPass_MODE	RCM [1:0]	VSPL	HSPL	DPL	EPL
Power ON Sequence	1'b0	2'b10	1'b0	1'b0	1'b0	1'b0
SW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b0
HW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b0

8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVA [1:0]		00
2nd Parameter	1	1	↑	XX	0	0	0	RTNA [4:0]					1C

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNA setting

Division ratio : DIVA setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNA [4:0]					Frame Rate (Hz)
1	0	0	0	0	Setting prohibited
1	0	0	0	1	Setting prohibited
1	0	0	1	0	Setting prohibited
1	0	0	1	1	Setting prohibited
1	0	1	0	0	Setting prohibited
1	0	1	0	1	Setting prohibited
1	0	1	1	0	Setting prohibited
1	0	1	1	1	Setting prohibited

RTNA [4:0]					Frame Rate (Hz)
1	1	0	0	0	70
1	1	0	0	1	68
1	1	0	1	0	65
1	1	0	1	1	63
1	1	1	0	0	61
1	1	1	0	1	Setting prohibited
1	1	1	1	0	Setting prohibited
1	1	1	1	1	Setting prohibited

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA [1:0]		Division Ratio
0	0	fosc

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

RTNA [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNA [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNA [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction	Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVA [1:0]	RTNA [4:0]
Power ON Sequence	2'b00	5'h1Ch
SW Reset	2'b00	5'h1Ch
HW Reset	2'b00	5'h1Ch

8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8l colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVB [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNB [4:0]					1C

Description

Formula to calculate frame frequency

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Idle mode at MCU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNB setting

Division ratio : DIVB setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNB [4:0]					Frame Rate (Hz)
1	0	0	0	0	Setting prohibited
1	0	0	0	1	Setting prohibited
1	0	0	1	0	Setting prohibited
1	0	0	1	1	Setting prohibited
1	0	1	0	0	Setting prohibited
1	0	1	0	1	Setting prohibited
1	0	1	1	0	Setting prohibited
1	0	1	1	1	Setting prohibited

RTNB [4:0]					Frame Rate (Hz)
1	1	0	0	0	70
1	1	0	0	1	68
1	1	0	1	0	65
1	1	0	1	1	63
1	1	1	0	0	61
1	1	1	0	1	Setting prohibited
1	1	1	1	0	Setting prohibited
1	1	1	1	1	Setting prohibited

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVB [1:0]		Division Ratio
0	0	fosc

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

RTNB [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNB [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNB [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DIVB [1:0]	RTNB [4:0]
Power ON Sequence	2'b00	5'h1Ch
SW Reset	2'b00	5'h1Ch
HW Reset	2'b00	5'h1Ch

8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC [1:0]		00
2ndParameter	1	1	↑	XX	0	0	0	RTNC [4:0]					1C

Description

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line x Division ratio x (Lines + VBP + VFP)}}$$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

fosc : internal oscillator frequency(Oscillator/26)

Clocks per line : RTNC setting

Division ratio : DIVC setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNC [4:0]					Frame Rate (Hz)
1	0	0	0	0	Setting prohibited
1	0	0	0	1	Setting prohibited
1	0	0	1	0	Setting prohibited
1	0	0	1	1	Setting prohibited
1	0	1	0	0	Setting prohibited
1	0	1	0	1	Setting prohibited
1	0	1	1	0	Setting prohibited
1	0	1	1	1	Setting prohibited

RTNC [4:0]					Frame Rate (Hz)
1	1	0	0	0	70
1	1	0	0	1	68
1	1	0	1	0	65
1	1	0	1	1	63
1	1	1	0	0	61
1	1	1	0	1	Setting prohibited
1	1	1	1	0	Setting prohibited
1	1	1	1	1	Setting prohibited

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC [1:0]		Division Ratio
0	0	fosc

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

RTNC [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

RTNC [4:0]					Clock per Line
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

RTNC [4:0]					Clock per Line
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks

Restriction	Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

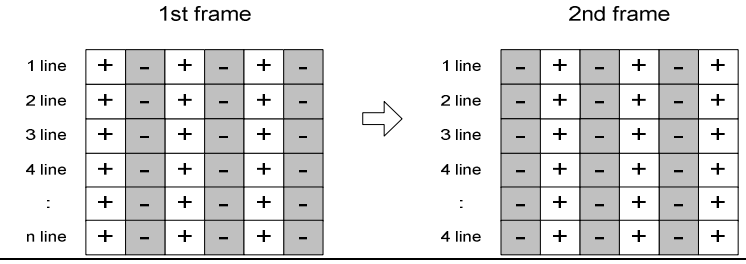
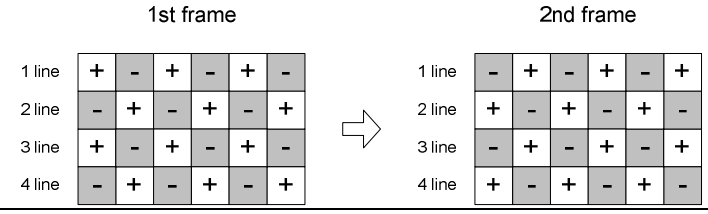
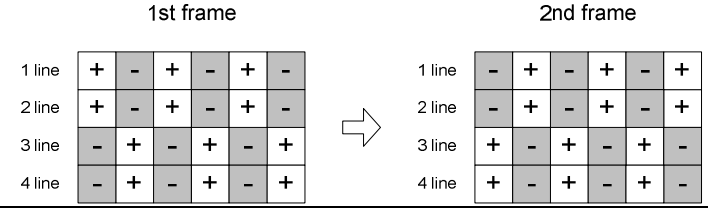
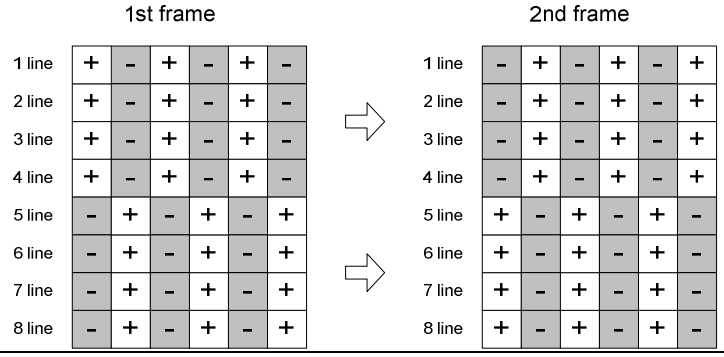
Status	Default Value	
	DIVC [1:0]	RTNC [4:0]
Power ON Sequence	2'b00	5'h1Ch
SW Reset	2'b00	5'h1Ch
HW Reset	2'b00	5'h1Ch

8.3.5. Display Inversion Control (B4h)

B4h	INVTR (Display Inversion Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	0	0	0	0	0	0	DINV[1:0]		00

Description

DINV[1:0] : Set the inversion mode

DINV [1:0]	Dot inversion mode	
2'b00	Column inversion	
2'b01	1-dot inversion	
2'b10	2-dot inversion	
2'b11	4-dot inversion	

Restriction	Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
	DINV[1:0]
Power ON Sequence	2'h00h
SW Reset	2'h00h
H/W Reset	2'h00h

8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	VFP [6:0]							02
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							02
3rd Parameter	1	1	↑	XX	0	HFP [6:0]							0A
4th Parameter	1	1	↑	XX	0	HBP [6:0]							14

Description

VFP [6:0] / **VBP [6:0]:** The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting prohibited	1000000	64
0000001	Setting prohibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HFP [4:0] / **HBP [6:0]:** The HFP [4:0] and HBP [6:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [6:0] HBP [6:0]	Number of DOTCLK of the front/back porch
0000000	Setting prohibited
0000001	Setting prohibited
0000010	2
0000011	3
0000100	4
0000101	5
0000110	6
0000111	7
0001000	8
0001001	9
0001010	10
0001011	11
0001100	12
0001101	13
0001110	14
0001111	15

HFP [6:0] HBP [6:0]	Number of DOTCLK of front/back porch
0010000	16
0010001	17
0010010	18
0010011	19
0010100	20
0010101	21
0010110	22
0010111	23
0011000	24
0011001	25
0011010	26
0011011	27
0011100	28
0011101	29
:	:
1111111	127

**HBP need to setting more than 58 clock and less than 200 clocks in By-pass mode. There is 8 bit setting in HBP register.*

<table>
<tr><td>Restriction</td><td>Set EXTC(C8h)=FF,93,42 to enable this command.</td></tr>
<tr><td>Register
Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HFP [4:0]</th><th>HBP 6:0]</th></tr>
<tr><td>Power ON Sequence</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>7’h14h</td></tr>
<tr><td>SW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>7’h14h</td></tr>
<tr><td>HW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>7’h14h</td></tr>
</table>
</td></tr>
</table>

8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	0	0	0	0	PTG [1:0]		PT [1:0]		0A
2nd Parameter	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				80
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						1D
4th Parameter	1	1	↑	XX	0	0	PCDIV [5:0]						04

Description

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area
0	0	Normal scan	Set with the PT [2:0] bits
0	1	Setting prohibited	---
1	0	Interval scan	Set with the PT [2:0] bits
1	1	Setting prohibited	---

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

PT [1:0]		Source output on non-display area
0	0	V63
0	1	V0
1	0	AGND
1	1	Hi-Z

SS: This bit controls MPU to memory write/read direction by column address order.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

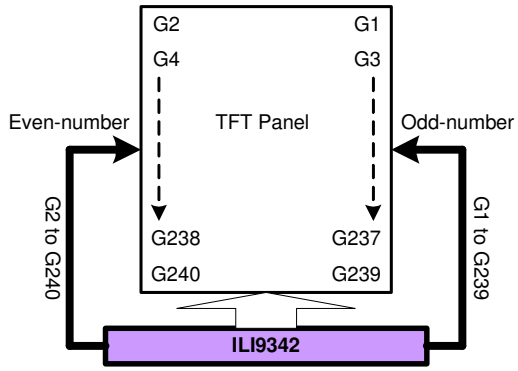
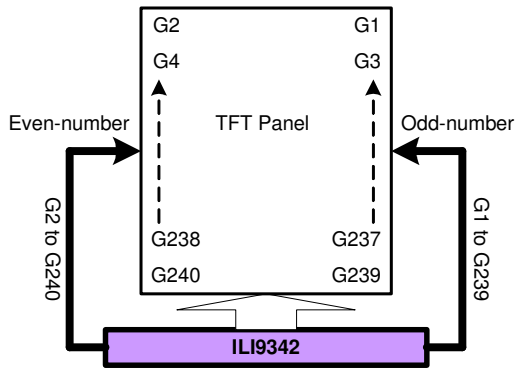
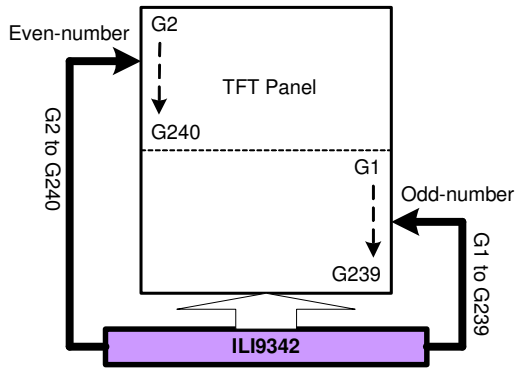
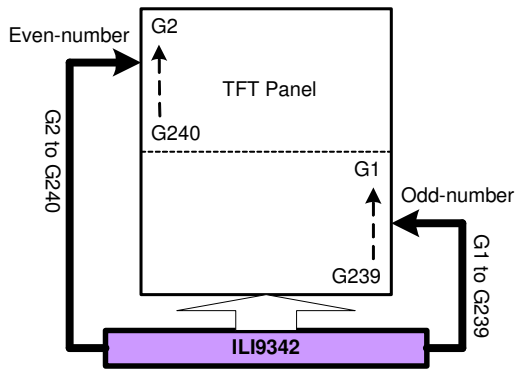
Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1 → G240
1	G240 → G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1→G2→G3→G4→ …… ….→G237→G238→G239→G240
0	1		G240→G239->G238→G237→…… …. →G4→G3→G2→G1
1	0		G1→G3→……...→G237→G239→ G2→G4→……→G238→G240
1	1		G240→G238→……...→G4→G2→ G239→G237→……→G3→G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

NL [5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
Others						Setting prohibited

PCDIV [5:0]:

$$\text{external fosc} = \frac{\text{DOTCLK}}{2 \times (\text{PCDIV} + 1)}$$

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value								
	PTG [1:0]	PT [1:0]	REV	GS	SS	SM	ISC [3:0]	NL [5:0]	PCDIV [5:0]
Power ON Sequence	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0000	6'b1Dh	6'b04h
SW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0000	6'b1Dh	6'b04h
HW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0000	6'b1Dh	6'b04h

8.3.8. Entry Mode Set (B7h)

B7h	ETMOD (Entry Mode Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
Parameter	1	1	↑	XX	0	0	0	0	0	GON	DTE	GAS	07

Description

GAS: Low voltage detection control.

GAS	Low voltage detection
0	Enable
1	Disable

GON/DTE: Set the output level of gate driver G1 ~ G320 as follows

GON	DTE	G1~G320 Gate utput
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	GON	DTE	GAS
Power ON Sequence	1'b1	1'b1	1'b1
SW Reset	1'b1	1'b1	1'b1
HW Reset	1'b1	1'b1	1'b1

8.3.9. Backlight Control 1 (B8h)

B8h	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
Parameter	1	1	↑	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	0B

Description

TH_UI [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_UI [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_UI [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	TH_UI [3:0]
Power On Sequence	4'b1011
SW Reset	4'b1011
HW Reset	4'b1011

8.3.10. Backlight Control 2 (B9h)

B9h	Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
Parameter	1	1	↑	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	BB

Description

TH_ST [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

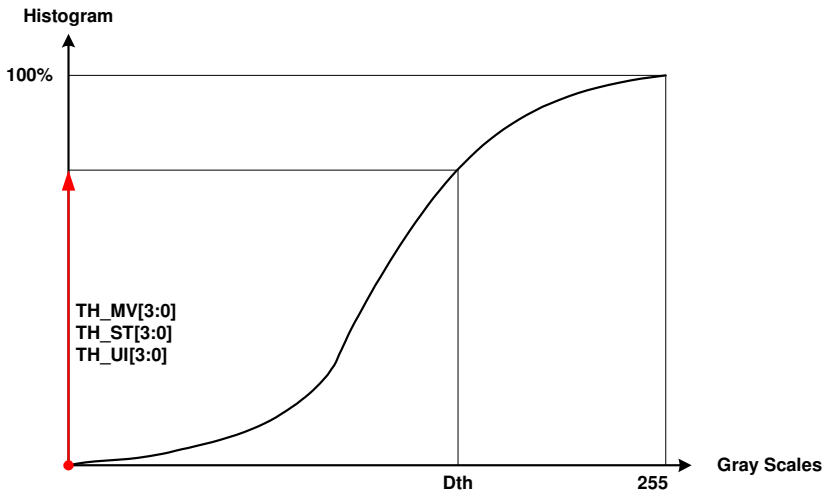
TH_ST [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_ST [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

TH_MV [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_MV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%



<table>
<tr><td>Restriction</td><td>Set EXTC(C8h)=FF,93,42 to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>TH_MV [3:0]</th><th>TH_ST [3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’b1011</td><td>4’b1011</td></tr>
<tr><td>SW Reset</td><td>No change</td><td>4’b1011</td></tr>
<tr><td>HW Reset</td><td>4’b1011</td><td>4’b1011</td></tr>
</table>
</td></tr>
</table>

8.3.11. Backlight Control 3 (BAh)

BAh	Backlight Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
Parameter	1	1	↑	XX	0	0	0	0	DTH_UI [3]	DTH_UI [2]	DTH_UI [1]	DTH_UI [0]	04

Description

DTH_UI [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_UI [3:0]	Description
4'0h	252
4'1h	248
4'2h	244
4'3h	240
4'4h	236
4'5h	232
4'6h	228
4'7h	224

DTH_UI [3:0]	Description
4'8h	220
4'9h	216
4'Ah	212
4'Bh	208
4'Ch	204
4'Dh	200
4'Eh	196
4'Fh	192

Restriction: Set EXTC (C8h)=FF,93,42 to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	DTH_UI [3:0]
Power On Sequence	4'b0100
SW Reset	4'b0100
HW Reset	4'b0100

8.3.12. Backlight Control 4 (BBh)

BBh	Backlight Control 4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
Parameter	1	1	↑	XX	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	A8

Description

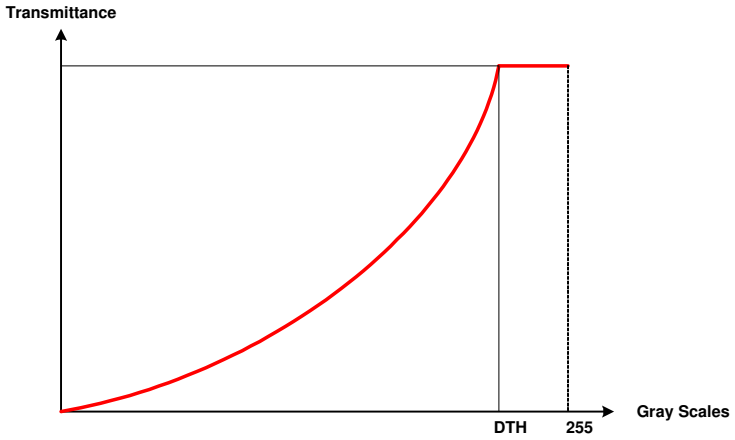
DTH_ST [3:0]/DTH_MV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_ST [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_ST [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_MV [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_MV [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164



Restriction: Set EXTC (C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DTH_MV [3:0]	DTH_ST [3:0]
Power On Sequence	4'b1010	4'b1000
SW Reset	No change	4'b1000
HW Reset	4'b1010	4'b1000

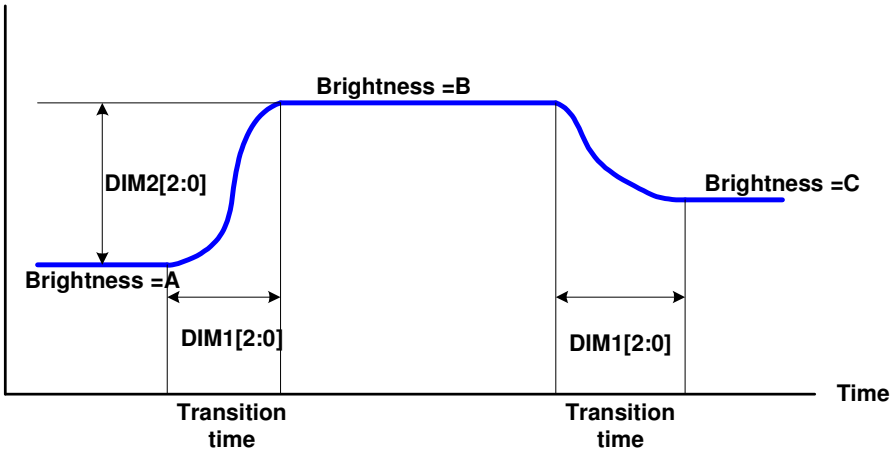
8.3.13. Backlight Control 5 (BCh)

BCh	Backlight Control 5												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh
Parameter	1	1	↑	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	43

Description

DIM1 [2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM1 [2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	8 frames
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames



DIM2 [3:0]: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.

For example:

If | brightness B – brightness A| < DIM2 [2:0], the brightness transition will be ignored and keep the brightness A.

Restriction

Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	DIM2 [3:0]	DIM1 [2:0]
Power On Sequence	4'b0100	4'b0011
SW Reset	No change	4'b0011
HW Reset	4'b0100	4'b0011

8.3.14. Backlight Control 6 (BDh)

<table>
<tr><th>BDh</th><th colspan="12">Backlight Control 2</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>BDh</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>LEDONR</td><td>LEDONPOL</td><td>LEDPWMPOL</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
LEDPWMPOL: The bit is used to define polarity of LEDPWM signal.
<table>
<tr><th>BL</th><th>LEDPWMPOL</th><th>LEDPWM pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>Original polarity of PWM signal</td></tr>
<tr><td>1</td><td>1</td><td>Inversed polarity of PWM signal</td></tr>
</table>
LEDONPOL: This bit is used to control LEDON pin.
<table>
<tr><th>BL</th><th>LEDONPOL</th><th>LEDON pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>LEDONR</td></tr>
<tr><td>1</td><td>1</td><td>Inversed LEDONR</td></tr>
</table>
LEDONR: This bit is used to control LEDON pin.
<table>
<tr><th>LEDONR</th><th>Description</th></tr>
<tr><td>0</td><td>Low</td></tr>
<tr><td>1</td><td>High</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">Set EXTC(C8h)=FF,93,42 to enable this command.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>LEDONR</th><th>LEDONPOL</th><th>LEDPWMPOL</th></tr>
<tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr>
</table>
</td></tr>
</table>

8.3.15. Backlight Control 7 (BEh)

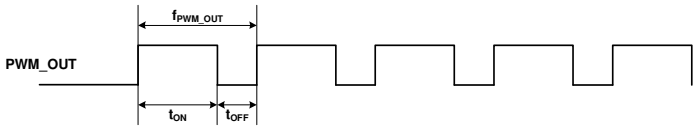
BEh	Backlight Control 7												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
Parameter	1	1	↑	XX	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	D0

Description

PWM_DIV [7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM\_OUT} = \frac{16MHz}{(PWM\_DIV[7:0]+1)\times 255}$$

PWM_DIV [7:0]	f_{PWM_OUT}
8'h0	62.74 KHz
8'h1	31.38 KHz
8'h2	20.915KHz
8'h3	15.686KHz
8'h4	12.549 KHz
…	…
8'hFB	249Hz
8'hFC	248Hz
8'hFD	247Hz
8'hFE	246Hz
8'hFF	245Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%

Restriction

Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	PWM_DIV [7:0]=D0h
SW Reset	PWM_DIV [7:0]=D0h
HW Reset	PWM_DIV [7:0]=D0h

8.3.16. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
1st Parameter	1	1	↑	XX	0	0	0	VRH1 [4:0]					09
2nd Parameter	1	1	↑	XX	0	0	0	VRH2 [4:0]					09

Description

VRH1[4:0]: Sets the VREG1OUT voltage for positive gamma

VRH1[4:0]	VREG1OUT	VRH1[4:0]	VREG1OUT
5'h00	Halt (Vreg1out =Hiz)	5'h10	1.209 x 3.80 = 4.594
5'h01	1.209 x 3.05 = 3.687	5'h11	1.209 x 3.85 = 4.655
5'h02	1.209 x 3.10 = 3.748	5'h12	1.209 x 3.90 = 4.715
5'h03	1.209 x 3.15 = 3.808	5'h13	1.209 x 3.95 = 4.776
5'h04	1.209 x 3.20 = 3.869	5'h14	1.209 x 4.00 = 4.836
5'h05	1.209 x 3.25 = 3.929	5'h15	1.209 x 4.05 = 4.896
5'h06	1.209 x 3.30 = 3.990	5'h16	1.209 x 4.10 = 4.957
5'h07	1.209 x 3.35 = 4.050	5'h17	1.209 x 4.15 = 5.017
5'h08	1.209 x 3.40 = 4.111	5'h18	1.209 x 4.20 = 5.078
5'h09	1.209 x 3.45 = 4.171	5'h19	1.209 x 4.25 = 5.138
5'h0A	1.209 x 3.50 = 4.232	5'h1A	1.209 x 4.30 = 5.199
5'h0B	1.209 x 3.55 = 4.292	5'h1B	1.209 x 4.35 = 5.259
5'h0C	1.209 x 3.60 = 4.352	5'h1C	1.209 x 4.40 = 5.320
5'h0D	1.209 x 3.65 = 4.413	5'h1D	1.209 x 4.45 = 5.380
5'h0E	1.209 x 3.70 = 4.473	5'h1E	1.209 x 4.50 = 5.441
5'h0F	1.209 x 3.75 = 4.534	5'h1F	1.209 x 4.55 = 5.501

VRH2[4:0]: Sets the VREG2OUT voltage for negative gamma

VRH2[4:0]	VREG2OUT	VRH2[4:0]	VREG2OUT
5'h00	Halt (Vreg2out =Hiz)	5'h10	1.209 x 3.80 = -4.594
5'h01	1.209 x 3.05 = -3.687	5'h11	1.209 x 3.85 = -4.655
5'h02	1.209 x 3.10 = -3.748	5'h12	1.209 x 3.90 = -4.715
5'h03	1.209 x 3.15 = -3.808	5'h13	1.209 x 3.95 = -4.776
5'h04	1.209 x 3.20 = -3.869	5'h14	1.209 x 4.00 = -4.836
5'h05	1.209 x 3.25 = -3.929	5'h15	1.209 x 4.05 = -4.896
5'h06	1.209 x 3.30 = -3.990	5'h16	1.209 x 4.10 = -4.957
5'h07	1.209 x 3.35 = -4.050	5'h17	1.209 x 4.15 = -5.017
5'h08	1.209 x 3.40 = -4.111	5'h18	1.209 x 4.20 = -5.078
5'h09	1.209 x 3.45 = -4.171	5'h19	1.209 x 4.25 = -5.138
5'h0A	1.209 x 3.50 = -4.232	5'h1A	1.209 x 4.30 = -5.199
5'h0B	1.209 x 3.55 = -4.292	5'h1B	1.209 x 4.35 = -5.259
5'h0C	1.209 x 3.60 = -4.352	5'h1C	1.209 x 4.40 = -5.320
5'h0D	1.209 x 3.65 = -4.413	5'h1D	1.209 x 4.45 = -5.380
5'h0E	1.209 x 3.70 = -4.473	5'h1E	1.209 x 4.50 = -5.441
5'h0F	1.209 x 3.75 = -4.534	5'h1F	1.209 x 4.55 = -5.501

<table>
<tr><td>Restriction</td><td>Set EXTC(C8h)=FF,93,42 to enable this command.</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr>
<tr><td>Sleep IN</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>VRH1 [4:0]</th><th>VRH2 [4:0]</th></tr>
<tr><td>Power ON Sequence</td><td>5’b01001</td><td>5’b01001</td></tr>
<tr><td>SW Reset</td><td>5’b01001</td><td>5’b01001</td></tr>
<tr><td>HW Reset</td><td>5’b01001</td><td>5’b01001</td></tr>
</table>
</td></tr>
</table>

8.3.17. Power Control 2 (C1h)

C1h	PWCTRL 2 (Power Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
Parameter	1	1	↑	XX	0	VC[2:0]			0	BT [2:0]			00

Description

BT [3:0]: Sets the factor used in the step-up circuits.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT [2 0]			DDVDH	DDVDL	VCL	VGH	VGL
0	0	0	VCI1 x 2	-(VCI1-VCL)	-VCI1	VCI1 x 6	-VCI1 x 5
0	0	1					-VCI1 x 4
0	1	0					-VCI1 x 3
0	1	1				VCI1 x 5	-VCI1 x 5
1	0	0					-VCI1 x 4
1	0	1					-VCI1 x 3
1	1	0				VCI1 x 4	-VCI1 x 4
1	1	1					-VCI1 x 3

Note1: Make sure that DDVDH setting restriction: DDVDH ≦ 6.0 V.

2: Make sure that VGH and VGL setting restriction: VGH -VGL≦ 32 V.

VC [3:0]: Sets VCI1 regulator voltage.

VC [3:0]			VCI1 Voltage
0	0	0	External VCI
0	0	1	2.6V
0	1	0	2.5V
0	1	1	2.4V
1	0	0	2.3V
1	0	1	2.2V
1	1	0	2.1V
1	1	1	2.0V

Note: Do not set any higher VCI1 level than VCI - 0.2V.

Restriction

Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	VC[2:0]	BT [2:0]
Power ON Sequence	3'b000	3'b000
SW Reset	3'b000	3'b000
HW Reset	3'b000	3'b000

8.3.18. Power Control 3 (For Normal Mode) (C2h)

C2h	PWCTRL 3 (Power Control 3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	0	C2h
Parameter	1	1	↑	XX	1	DCA1 [2:0]			0	DCA0 [2:0]			B2

Description

DCA0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Normal mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCA0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	Prohibit
0	0	1	1/8 H
0	1	0	1/4 H
0	1	1	1/2 H
1	0	0	1 H
1	0	1	2 H
1	1	0	4 H
1	1	1	8 H

DCA1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	Prohibit
0	0	1	1/8 H
0	1	0	1/4 H
0	1	1	1/2 H
1	0	0	1 H
1	0	1	Prohibit
1	1	0	Prohibit
1	1	1	Prohibit

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCA0 [2:0]	DCA1 [2:0]
Power ON Sequence	3'b010	3'b011
SW Reset	3'b010	3'b011
HW Reset	3'b010	3'b011

8.3.19. Power Control 4 (For Idle Mode) (C3h)

C3h	PWCTRL 4 (Power Control 4)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	0	1	1	C3h
Parameter	1	1	↑	XX	1	DCB1 [2:0]			0	DCB0 [2:0]			B2

Description

DCB0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Idle mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCB0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	Prohibit
0	0	1	1/8 H
0	1	0	1/4 H
0	1	1	1/2 H
1	0	0	1 H
1	0	1	2 H
1	1	0	4 H
1	1	1	8 H

DCB1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	Prohibit
0	0	1	1/8 H
0	1	0	1/4 H
0	1	1	1/2 H
1	0	0	1 H
1	0	1	Prohibit
1	1	0	Prohibit
1	1	1	Prohibit

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCB0 [2:0]	DCB1 [2:0]
Power ON Sequence	3'b010	3'b011
SW Reset	3'b010	3'b011
H/W Reset	3'b010	3'b011

8.3.20. Power Control 5 (For Partial Mode) (C4h)

C4h	PWCTRL 5 (Power Control 5)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	0	C4h
Parameter	1	1	↑	XX	1	DCC1 [2:0]			0	DCC0 [2:0]			B2

Description

DCC0 [2:0]: Selects the operating frequency of the step-up circuit 1 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC1 [2:0]: Selects the operating frequency of the step-up circuit 2/3/4 for Partial mode. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DCC0 [2:0]			Step-up cycle for step-up circuit 1
0	0	0	Prohibit
0	0	1	1/8 H
0	1	0	1/4 H
0	1	1	1/2 H
1	0	0	1 H
1	0	1	2 H
1	1	0	4 H
1	1	1	8 H

DCC1 [2:0]			Step-up cycle for step-up circuit 2/3/4
0	0	0	Prohibit
0	0	1	1/8 H
0	1	0	1/4 H
0	1	1	1/2 H
1	0	0	1 H
1	0	1	Prohibit
1	1	0	Prohibit
1	1	1	Prohibit

Restriction: Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	DCC0 [2:0]	DCC1 [2:0]
Power ON Sequence	3'b010	3'b011
SW Reset	3'b010	3'b011
HW Reset	3'b010	3'b011

8.3.21. VCOM Control 1(C5h)

C5h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
1st Parameter	1	1	↑	XX	nVM	VCM[6:0]							F2

Description

nVM : Selection the VCM setting.
0 : NV Memory selected for VCM setting
1 : Register C5h for VCM setting, when NV memory is already programmed, nVM=1 will be valid when VCM[6:0] is set

VCM [6:0] is used to set factor to generate VCOM voltage from the reference voltage VREG2OUT.

VCM[6:0]	VCOM	VCM[6:0]	VCOM	VCM[6:0]	VCOM	VCM[6:0]	VCOM
00h	Prohibit	20h	VREG2OUT*0.439	40h	VREG2OUT*0.325	60h	VREG2OUT*0.211
01h	VREG2OUT*0.550	21h	VREG2OUT*0.436	41h	VREG2OUT*0.322	61h	VREG2OUT*0.208
02h	VREG2OUT*0.546	22h	VREG2OUT*0.432	42h	VREG2OUT*0.318	62h	VREG2OUT*0.204
03h	VREG2OUT*0.543	23h	VREG2OUT*0.429	43h	VREG2OUT*0.315	63h	VREG2OUT*0.201
04h	VREG2OUT*0.539	24h	VREG2OUT*0.425	44h	VREG2OUT*0.311	64h	VREG2OUT*0.197
05h	VREG2OUT*0.536	25h	VREG2OUT*0.421	45h	VREG2OUT*0.307	65h	VREG2OUT*0.193
06h	VREG2OUT*0.532	26h	VREG2OUT*0.418	46h	VREG2OUT*0.304	66h	VREG2OUT*0.190
07h	VREG2OUT*0.528	27h	VREG2OUT*0.414	47h	VREG2OUT*0.300	67h	VREG2OUT*0.186
08h	VREG2OUT*0.525	28h	VREG2OUT*0.411	48h	VREG2OUT*0.297	68h	VREG2OUT*0.183
09h	VREG2OUT*0.521	29h	VREG2OUT*0.407	49h	VREG2OUT*0.293	69h	VREG2OUT*0.179
0Ah	VREG2OUT*0.518	2Ah	VREG2OUT*0.404	4Ah	VREG2OUT*0.290	6Ah	VREG2OUT*0.176
0Bh	VREG2OUT*0.514	2Bh	VREG2OUT*0.400	4Bh	VREG2OUT*0.286	6Bh	VREG2OUT*0.172
0Ch	VREG2OUT*0.511	2Ch	VREG2OUT*0.397	4Ch	VREG2OUT*0.282	6Ch	VREG2OUT*0.168
0Dh	VREG2OUT*0.507	2Dh	VREG2OUT*0.393	4Dh	VREG2OUT*0.279	6Dh	VREG2OUT*0.165
0Eh	VREG2OUT*0.504	2Eh	VREG2OUT*0.389	4Eh	VREG2OUT*0.275	6Eh	VREG2OUT*0.161
0Fh	VREG2OUT*0.500	2Fh	VREG2OUT*0.386	4Fh	VREG2OUT*0.272	6Fh	VREG2OUT*0.158
10h	VREG2OUT*0.496	30h	VREG2OUT*0.382	50h	VREG2OUT*0.268	70h	VREG2OUT*0.154
11h	VREG2OUT*0.493	31h	VREG2OUT*0.379	51h	VREG2OUT*0.265	71h	VREG2OUT*0.151
12h	VREG2OUT*0.489	32h	VREG2OUT*0.375	52h	VREG2OUT*0.261	72h	VREG2OUT*0.147
13h	VREG2OUT*0.486	33h	VREG2OUT*0.372	53h	VREG2OUT*0.258	73h	VREG2OUT*0.143
14h	VREG2OUT*0.482	34h	VREG2OUT*0.368	54h	VREG2OUT*0.254	74h	VREG2OUT*0.140
15h	VREG2OUT*0.479	35h	VREG2OUT*0.364	55h	VREG2OUT*0.250	75h	VREG2OUT*0.136
16h	VREG2OUT*0.475	36h	VREG2OUT*0.361	56h	VREG2OUT*0.247	76h	VREG2OUT*0.133
17h	VREG2OUT*0.471	37h	VREG2OUT*0.357	57h	VREG2OUT*0.243	77h	VREG2OUT*0.129
18h	VREG2OUT*0.468	38h	VREG2OUT*0.354	58h	VREG2OUT*0.240	78h	VREG2OUT*0.126
19h	VREG2OUT*0.464	39h	VREG2OUT*0.350	59h	VREG2OUT*0.236	79h	VREG2OUT*0.122
1Ah	VREG2OUT*0.461	3Ah	VREG2OUT*0.347	5Ah	VREG2OUT*0.233	7Ah	VREG2OUT*0.119
1Bh	VREG2OUT*0.457	3Bh	VREG2OUT*0.343	5Bh	VREG2OUT*0.229	7Bh	VREG2OUT*0.115
1Ch	VREG2OUT*0.454	3Ch	VREG2OUT*0.340	5Ch	VREG2OUT*0.225	7Ch	VREG2OUT*0.111
1Dh	VREG2OUT*0.450	3Dh	VREG2OUT*0.336	5Dh	VREG2OUT*0.222	7Dh	VREG2OUT*0.108
1Eh	VREG2OUT*0.446	3Eh	VREG2OUT*0.332	5Eh	VREG2OUT*0.218	7Eh	VREG2OUT*0.104
1Fh	VREG2OUT*0.443	3Fh	VREG2OUT*0.329	5Fh	VREG2OUT*0.215	7Fh	Prohibit

Restriction

Set EXTC(C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	VCM[6:0]	nVM
Power ON Sequence	7'b1110010	1'b1
S/W Reset	7'b1110010	1'b1

8.3.22. Get GPIO0~7 Status (C6h)

C6h	Get GPIO0~7 Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	0	C6h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	GPI[7:0]								00
Description	**GPI[7:0]:** get the GPIO0~7 input configuration correspondent with register GPI bit 0 ~ 7. 0 : logic low input 1 : logic High input												
Restriction	Set EXTC(C8h)=FF,93,42 to enable this command.												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
	GPI[7:0]
Power ON Sequence	7'h00h
SW Reset	7'h00h
HW Reset	7'h00h

8.3.23. Set GPIO0~7 Status (C7h)

C7h	Set GPIO0~7 Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
1st Parameter	1	1	↑	XX	GPO[7:0]								00
2ndParameter	1	1	↑	XX	X	X	X	X	X	X	IE	OEB	02

Description

GPO[7:0] : Setting the GPIO output configuration

0 : GPIO output is logic low

1 : GPIO output is logic High

IE/OEB : Control the GPO output direction

IE	OEB	GPO output control
0	0	Enable GPIO output
1	1	Disable GPIO output

Restriction

SET EXTC (C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	GPO[7:0]	IE	OEB
Power ON Sequence	7'h00h	1'b0	1'b0
SW Reset	7'h00h	1'b0	1'b0
HW Reset	7'h00h	1'b0	1'b0

8.3.24. Set EXTC (C8h)

C8h	SETEXTC (Set EXTC)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	1	0	0	0	C8h
1st Parameter	1	1	↑	XX	EXTC1[7:0]								00
2nd Parameter	1	1	↑	XX	EXTC2[7:0]								00
3rd Parameter	1	1	↑	XX	EXTC3[7:0]								00
Description	Turn on the external command if setting EXTC1[7:0] = 0xFF, EXTC2[7:0] = 0x93, and EXTC3[7:0] = 0x42												
Restriction													

Register Availability

Status	Availability
Normal Mo e ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mo e ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value		
	EXTC1[7:0]	EXTC2[7:0]	EXTC3[7:0]
Power ON Sequence	00h	00h	00h
SW Reset	00h	00h	00h
HW Reset	00h	00h	00h

8.3.25. NV Memory Write (D0h)

D0h	NVMWR (NV Memory Write)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
1st Parameter	1	1	↑	XX	0	0	0	0	PGM_ADR [3:0]				00
2ndParameter	1	1	↑	XX	PGM_DATA [7:0]								XX

Description

This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will programmed to NV memory.

PGM_ADR [3:0]: The select bits of ID1, ID2, ID3 ,VMF [6:0] and MADCTL programming.

PGM_ADR [3:0]				Programmed NV Memory Selection
0	0	0	0	ID1 programming
0	0	0	1	ID2 programming
0	0	1	0	ID3 programming
0	1	0	0	VMF [6:0] programming
1	0	0	0	MADCTL programming
Others				Reserved

PGM_DATA [7:0]: The programmed data.

Restriction

Set EXTC (C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	PGM_ADR [3:0]	PGM_DATA [7:0]
Power ON Sequence	4'b0000	MTP value
SW Reset	4'b0000	MTP value
HW Reset	4'b0000	MTP value

8.3.26. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
1st Parameter	1	1	↑	XX	KEY [23:16]								55h
2nd Parameter	1	1	↑	XX	KEY [15:8]								AAh
3rd Parameter	1	1	↑	XX	KEY [7:0]								66h
Description	**KEY [23:0]:** NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.												
Restriction	Set EXTC (C8h)=FF,93,42 to enable this command.												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	KEY [23:0]=55AA66h
SW Reset	KEY [23:0]=55AA66h
HW Reset	KEY [23:0]=55AA66h

8.3.27. NV Memory Status Read (D2h)

D2h	RDNVM (NV Memory Status Read)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	MADCTL_CNT [1:0]		ID3_CNT [1:0]		ID2_CNT [1:0]		ID1_CNT [1:0]		XX
3rdParameter	1	↑	1	XX	BUSY	0	0	0	0	VMF_CNT [2:0]			XX

Description

ID1_CNT [1:0] / **ID2_CNT [1:0]** / **ID3_CNT [1:0]** /**MADCTL_CNT [1:0]:** NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

ID1_CNT [1:0] / ID2_CNT [1:0] ID3_CNT [1:0] / MADCTL_CNT [1:0]		Description
Status		Availability
0	0	No Programmed
0	1	Programmed 1 time
1	1	Programmed 2 times

VMF_CNT [2:0]: NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.

VMF_CNT [2:0]			Description
Status			Availability
0	0	0	No Programmed
0	0	1	Programmed 1 time
0	1	1	Programmed 2 times
1	1	1	Programmed 3 times

BUSY: The status bit of NV memory programming.

BUSY	The Status of NV Memory
0	Idle
1	Busy

Restriction: Set EXTC (C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value					
	MADCTL_CNT	ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY
Power ON Sequence	X	X	X	X	X	X
SW Reset	X	X	X	X	X	X
HW Reset	X	X	X	X	X	X

8.3.28. Read ID4 (D3h)

D3h	RDID4 (Read ID4)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2ndParameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h
3rdParameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93h
4th Parameter	1	↑	1	XX	0	1	0	0	0	0	1	0	42h
Description	Read IC device code. The 1st parameter is dummy read period. The 4th parameter mean the IC model name.												
Restriction	Set EXTC (C8h)=FF,93,42 to enable this command.												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value
Power ON Sequence	24'h009342h
SW Reset	24'h009342h
HW Reset	24'h009342h

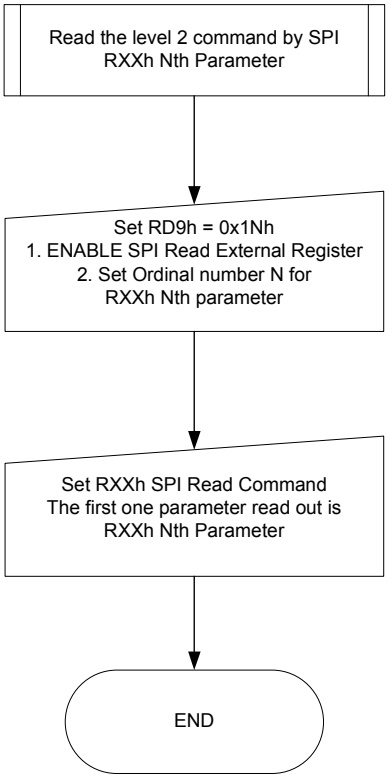
8.3.29. Get External Register for SPI (D9h)

D9h	XREG (Get External Register)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	0	1	D9h
1st Parameter	1	1	↑	XX	0	0	0	ENSPI	SPI_EXT_ORD [3:0]				00

Description

ENSPI : This command is used to enable the SPI interface to access the level 2 commands.

SPI_EXT_ORD [3:0]: Th SPI will get the one desired parameter of the external register by setting this ordinal number.



Restriction: Set EXTC (C8h)=FF,93,42 to enable this command.

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	ENSPI	SPI_EXT_ORD [3:0]
Power ON Sequence	1'b0	4'b0000
SW Reset	1'b0	4'b0000
HW Reset	1'b0	4'b0000

8.3.30. Positive Gamma Correction (E0h)

E0h	PGAMCTRL (Positive Gamma Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
1st Parameter	1	1	↑	XX	X	X	X	X	VP0 [3:0]				00
2ndParameter	1	1	↑	XX	X	X	VP1 [5:0]						05
3rdParameter	1	1	↑	XX	X	X	VP2 [5:0]						08
4th Parameter	1	1	↑	XX	X	X	X	X	VP4 [3:0]				04
5th Parameter	1	1	↑	XX	X	X	X	VP6 [4:0]					13
6th Parameter	1	1	↑	XX	X	X	X	X	VP13 [3:0]				0A
7th Parameter	1	1	↑	XX	X	VP20 [6:0]							34
8th Parameter	1	1	↑	XX	VP36 [3:0]				VP27 [3:0]				8A
9th Parameter	1	1	↑	XX	X	VP43 [6:0]							46
10thParameter	1	1	↑	XX	X	X	X	X	VP50 [3:0]				07
11thParameter	1	1	↑	XX	X	X	X	VP57 [4:0]					0E
12thParameter	1	1	↑	XX	X	X	X	X	VP59 [3:0]				0A
13thParameter	1	1	↑	XX	X	X	VP61 [5:0]						1B
14thParameter	1	1	↑	XX	X	XX	VP62 [5:0]						1D
15thParameter	1	1	↑	XX	X	X	X	X	VP63 [3:0]				0F
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Set EXTC (C8h)=FF,93,42 to enable this command.												
Register Availability													

Status	Availability
Normal Mode N, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default	

8.3.31. Negative Gamma Correction (E1h)

E1h	NGAMCTRL (Negative Gamma Correction)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
1st Parameter	1	1	↑	XX	X	X	X	X	VN0 [3:0]				00
2ndParameter	1	1	↑	XX	X	X	VN1 [5:0]						22
3rdParameter	1	1	↑	XX	X	X	VN2 [5:0]						25
4th Parameter	1	1	↑	XX	X	X	X	X	VN4 [3:0]				04
5th Parameter	1	1	↑	XX	X	X	X	VN6 [4:0]					0F
6th Parameter	1	1	↑	XX	X	X	X	X	VN13 [3:0]				06
7th Parameter	1	1	↑	XX	X	VN20 [6:0]							38
8th Parameter	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]				56
9th Parameter	1	1	↑	XX	X	VN43 [6:0]							4B
10thParameter	1	1	↑	XX	X	X	X	X	VN50 [3:0]				05
11thParameter	1	1	↑	XX	X	X	X	VN57 [4:0]					0C
12thParameter	1	1	↑	XX	X	X	X	X	VN59 [3:0]				0A
13thParameter	1	1	↑	XX	X	X	VN61 [5:0]						37
14thParameter	1	1	↑	XX	X	X	VN62 [5:0]						3A
15thParameter	1	1	↑	XX	X	X	X	X	VN63 [3:0]				0F
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.												
Restriction	Set EXTC (C8h)=FF,93,42 to enable this command.												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default	

8.3.32. Digital Gamma Control 1 (E2h)

E2h	DGAMCTRL (Digital Gamma Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX
16th Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX
Description	**RCAx [3:0]:** Gamma Macro-adjustment registers for red gamma curve. **BCAx [3:0]:** Gamma Macro-adjustment registers for blue gamma curve.												
Restriction	Set EXTC (C8h)=FF,93,42 to enable this command.												
Register Availability													

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RCAx [3:0]	BCAx [3:0]
Power ON Sequence	TBD	TBD
SW Reset	TBD	TBD
HW Reset	TBD	TBD

8.3.33. Digital Gamma Control 2(E3h)

E3h	DGAMCTRL (Digital Gamma Control 2)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX
:	1	1	↑	XX	RFAx [3:0]				BFAx [3:0]				XX
64rdParameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX
Description	**RFAx [3:0]:** Gamma Micro-adjustment register for red gamma curve. **BFAx [3:0]:** Gamma Micro-adjustment register for blue gamma curve.												
Restriction	Set EXTC (C8h)=FF,93,42 to enable this command.												

Register Availability

Status	Availability
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

Default

Status	Default Value	
	RFAx [3:0]	BFAx [3:0]
Power ON Sequence	TBD	TBD
SW Reset	TBD	TBD
HW Reset	TBD	TBD

8.3.34. Interface Control (F6h)

F6h	IFCTL (16bits Data Format Selection)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
1st Parameter	1	1	↑	XX	MY_ EOR	MX_ EOR	MV_ EOR	0	BGR_ EOR	0	0	WE MODE	01
2nd Parameter	1	1	↑	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00
3rd Parameter	1	1	↑	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00

Description

MY_EOR / MX_EOR / MV_EOR / BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

MDT [1:0]: Select the method of display data transferring.

WEMODE: Memory write control

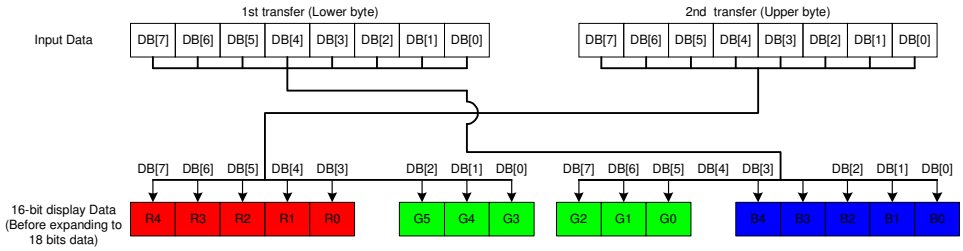
WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode
0	Normal (MSB first, default)
1	Little Endian (LSB first)

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.



DM [1:0]: Select the display operation mode.

DM [1]	DM [0]	Display Operation Mode
0	0	Internal clock operation
0	1	RGB Interface Mode
1	0	VSYNC interface mode
1	1	Setting disabled

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

RM: Select the interface to access the GRAM.

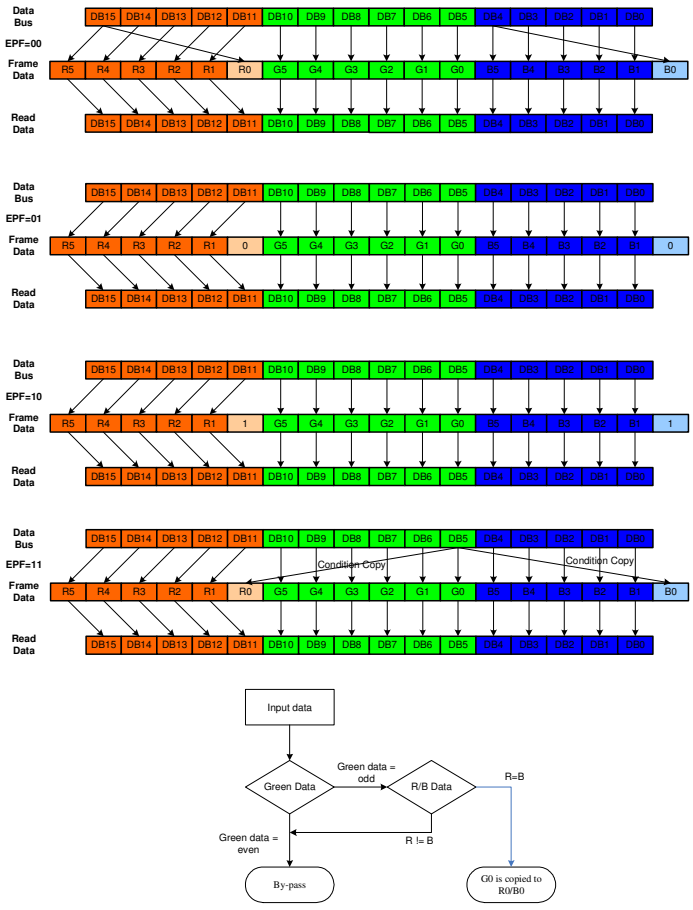
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.



EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)
00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}

	01	"0" is inputted to LSB r [5:0] = {R [4:0], 0} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 0} Exception: R [4:0], B[4:0] = 5'h1F → r [5:0], b[5:0] = 6'h3F
	10	"1" is inputted to LSB r [5:0] = {R [4:0], 1} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], 1} Exception: R [4:0], B[4:0] = 5'h00 → r [5:0], b[5:0] = 6'h00
	11	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B≠G → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G≠B → r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G≠R → r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}

Restriction: Set "EXTC" turn on to enable this command

Register Availability

Status	Ava lability
Nor al Mode ON, Idle Mode OFF, Sleep OUT	Yes
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes
Sleep IN	Yes

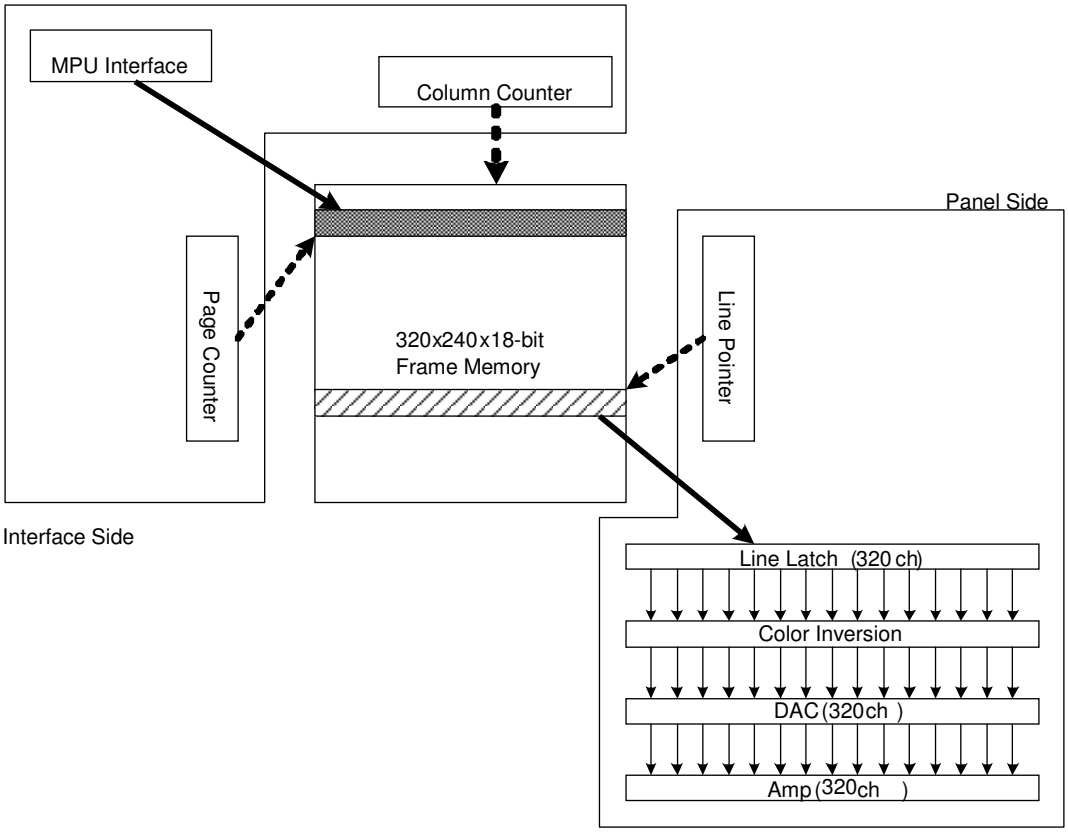
Default

Status	Default Value						
	EPF [1:0]	MDT [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM
Power ON Sequence	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
SW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0
HW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (320x18x240 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

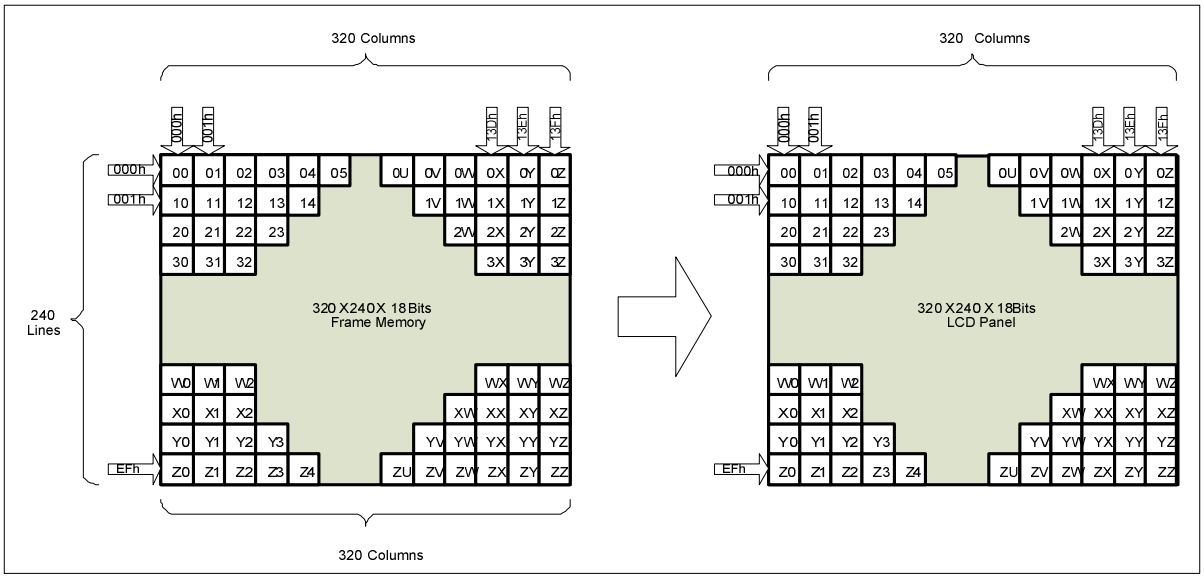


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 013Fh and page pointer is 0000h to 00EFh is displayed.

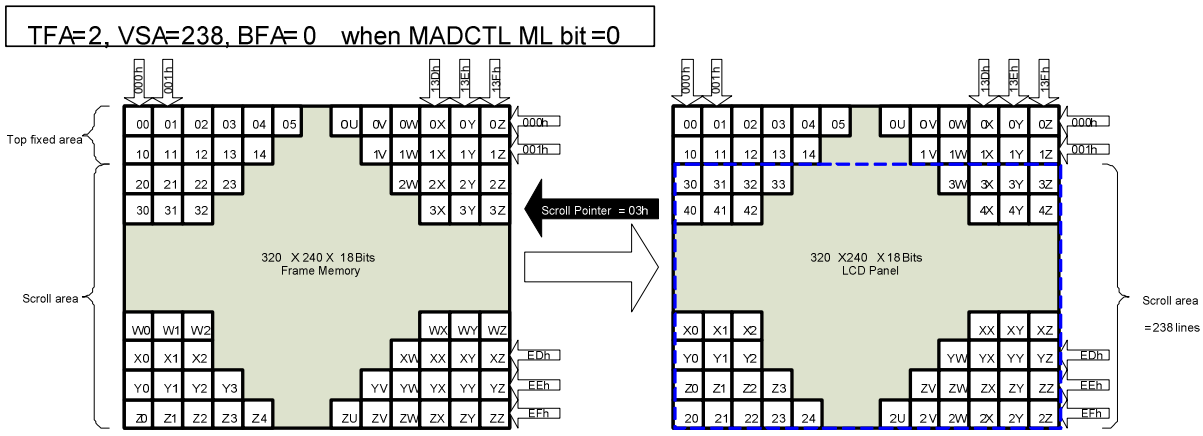
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

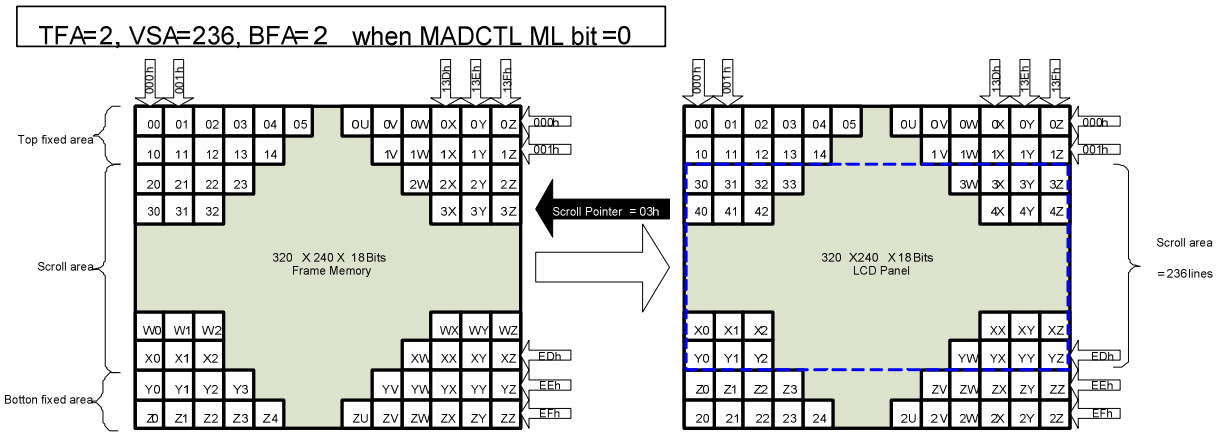


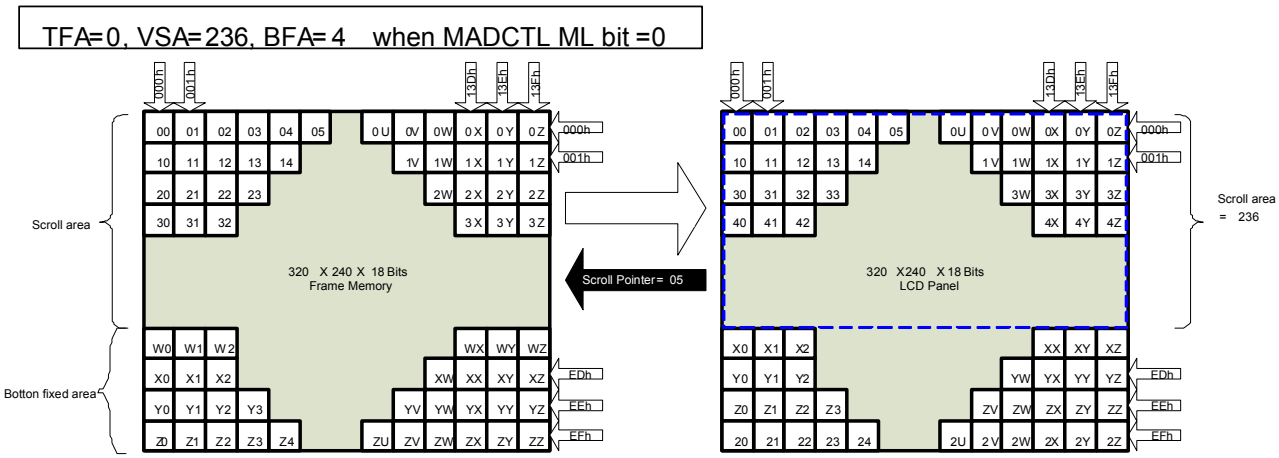
9.2.2. Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.







Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 240, Scrolling Mode is undefined.

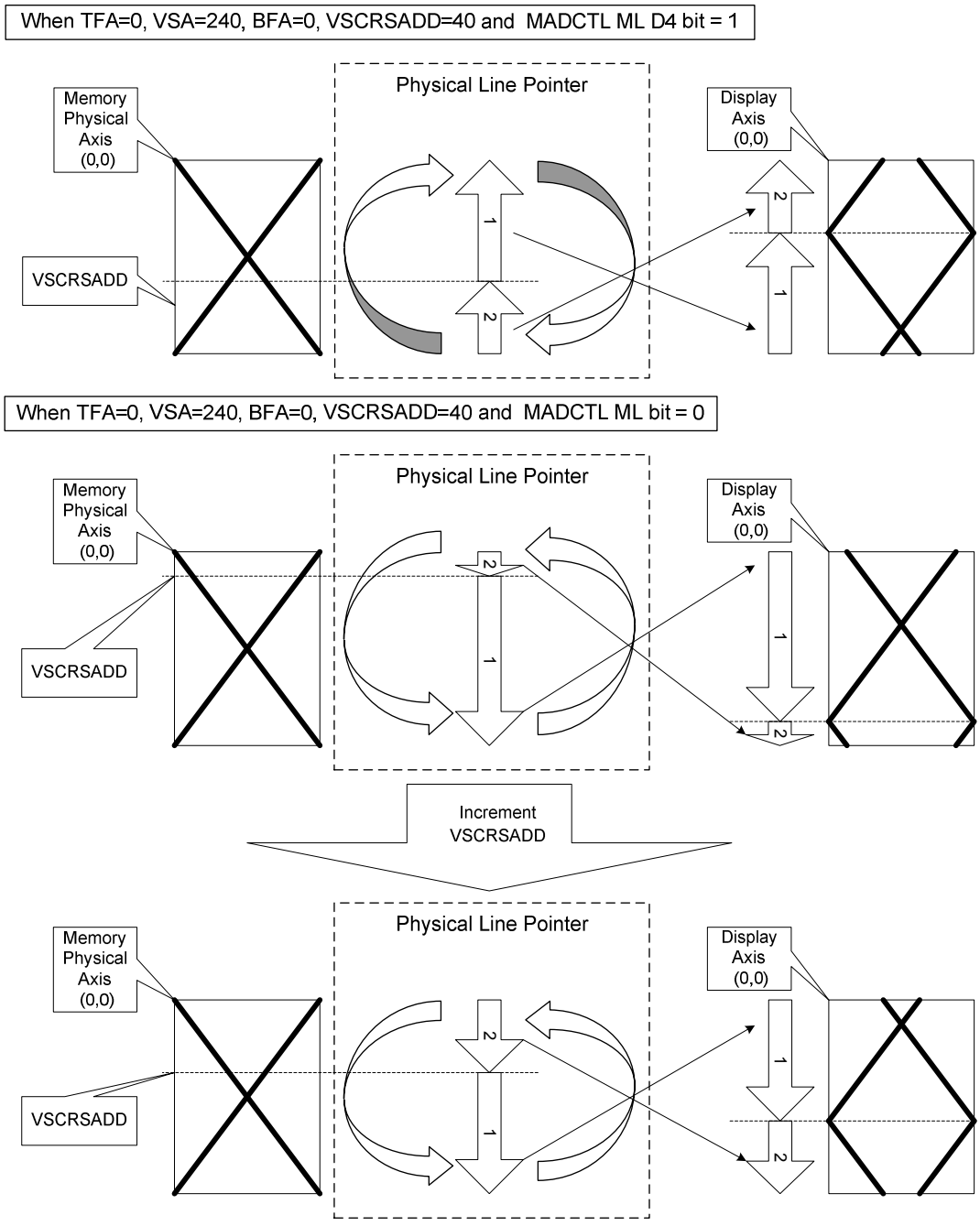
9.2.3. Vertical Scroll Example

9.2.4. Case1: TFA+VSA+BFA < 240

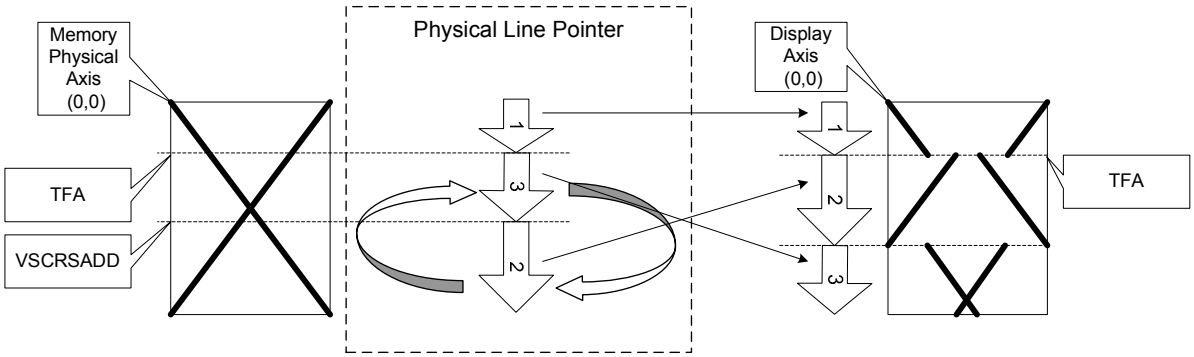
This setting is prohibited, unless unexpected picture will be shown.

9.2.5. Case2: TFA+VSA+BFA = 240 (Rolling Scrolling)

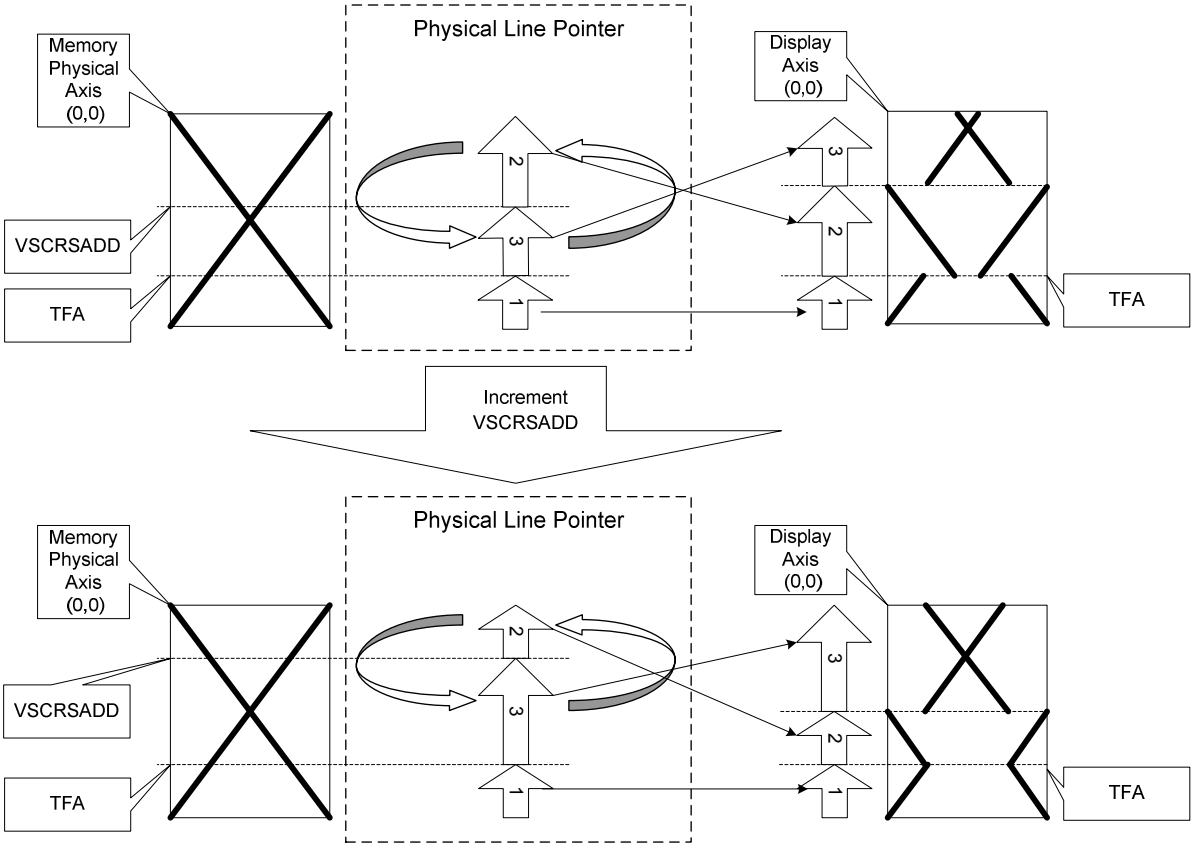
The operation of Rolling Scrolling is explained by these examples in the following.



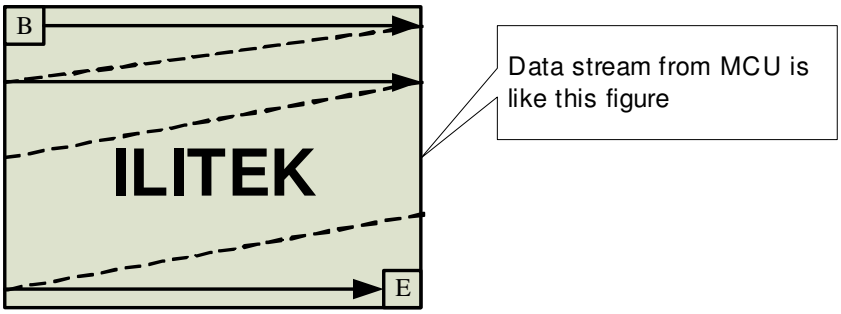
When TFA=30, VSA=210, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



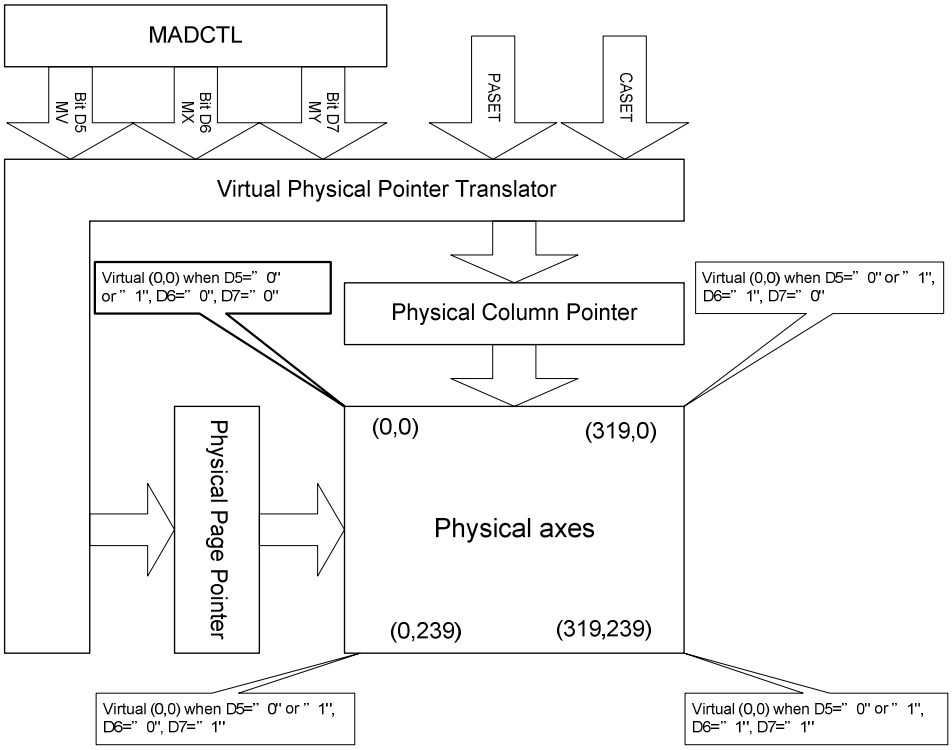
When TFA=30, VSA=210, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits D5, D6, and D7 as described below.



D5	D6	D7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (239-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (239-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (239-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (239-Physical Page Pointer)	Direct to (319-Physical Column Pointer)

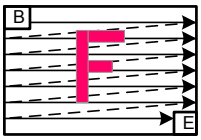
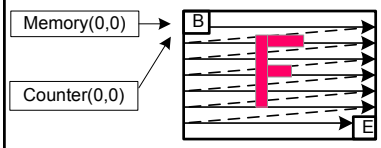
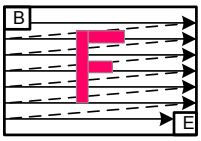
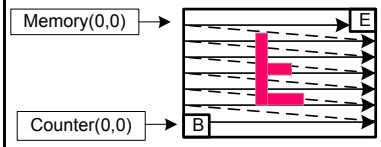
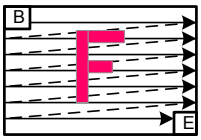
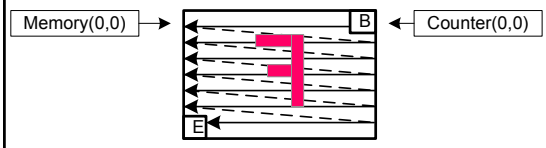
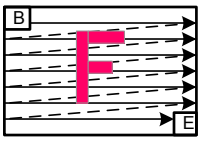
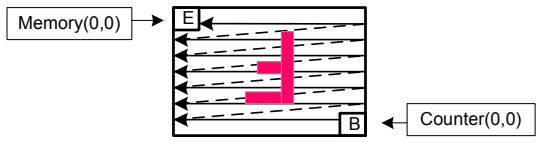
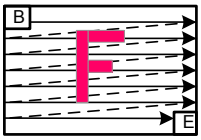
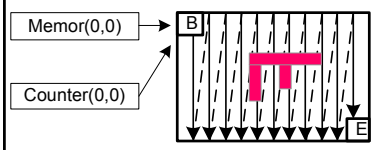
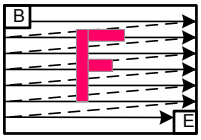
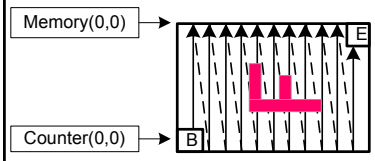
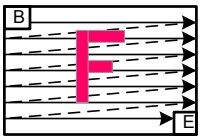
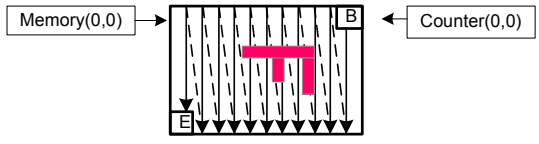
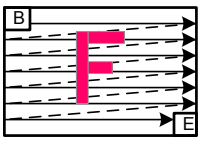
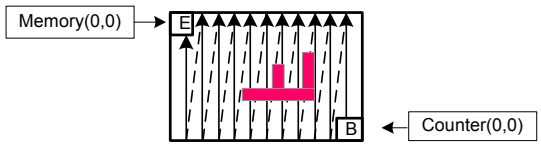
Condition	Column Counter	Page counter
When RAMWR/RAMRD command is accepted	Return to “Start column”	Return to “Start Page”
Complete Pixel Read/Write action	Increment by 1	No change
The Column values is large than “End Column”	Return to “Start column”	Increment by 1
The Page counter is large than “End Page”	Return to “Start column”	Return to “Start Page”

Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits D7, D6 and D5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data Direction	MADCTR Parameter			Image in the Memory (MCU)	Image in the Driver (Frame Memory)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

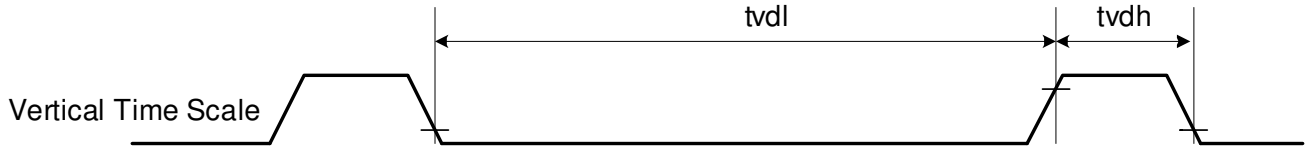
10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

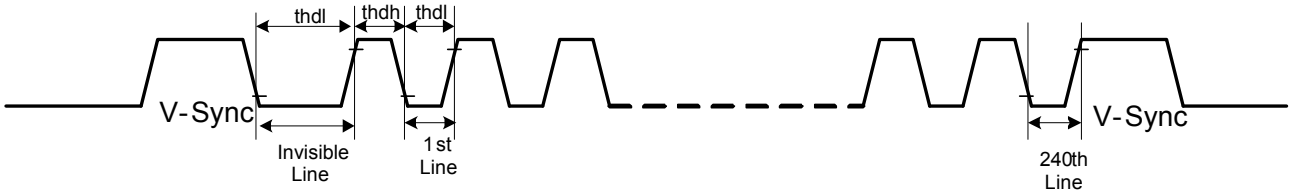
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

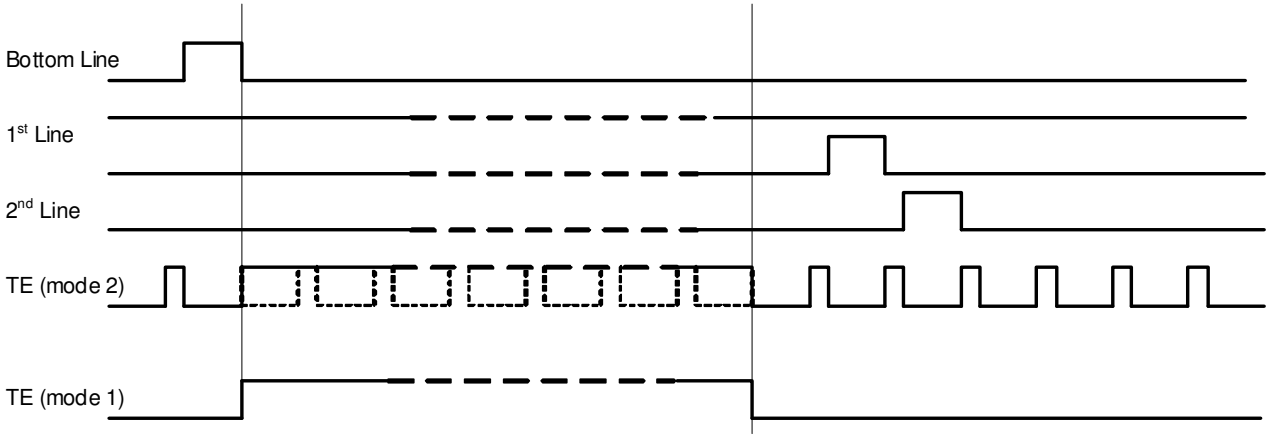
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 240 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

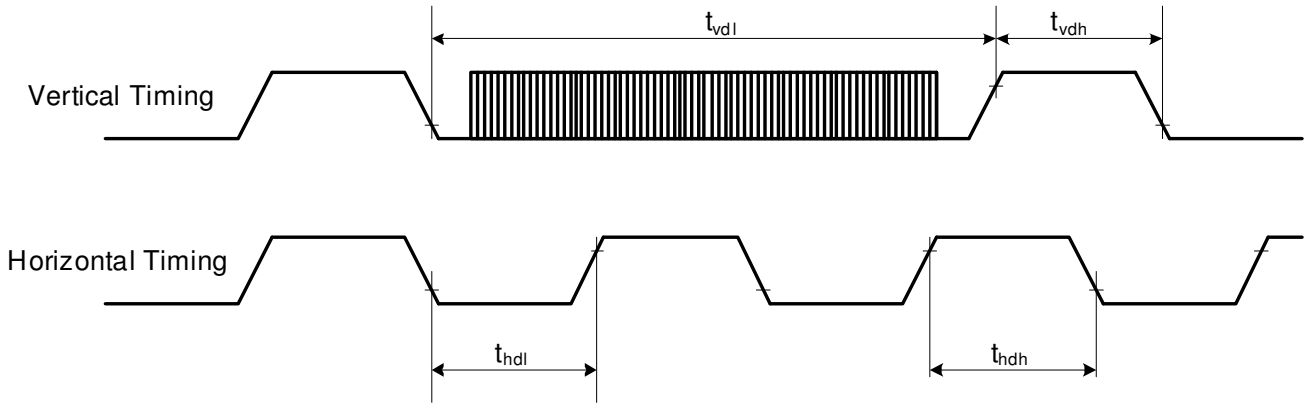
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

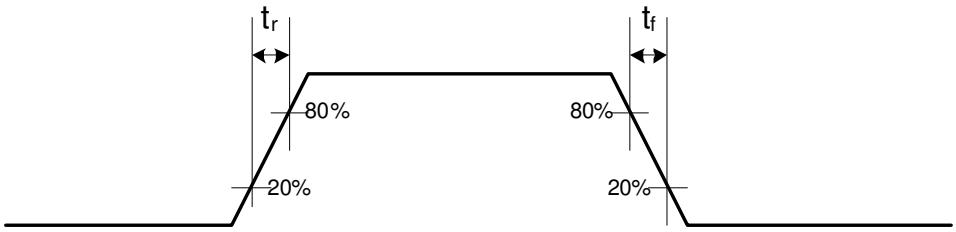


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL D4=0 and D4=1
2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

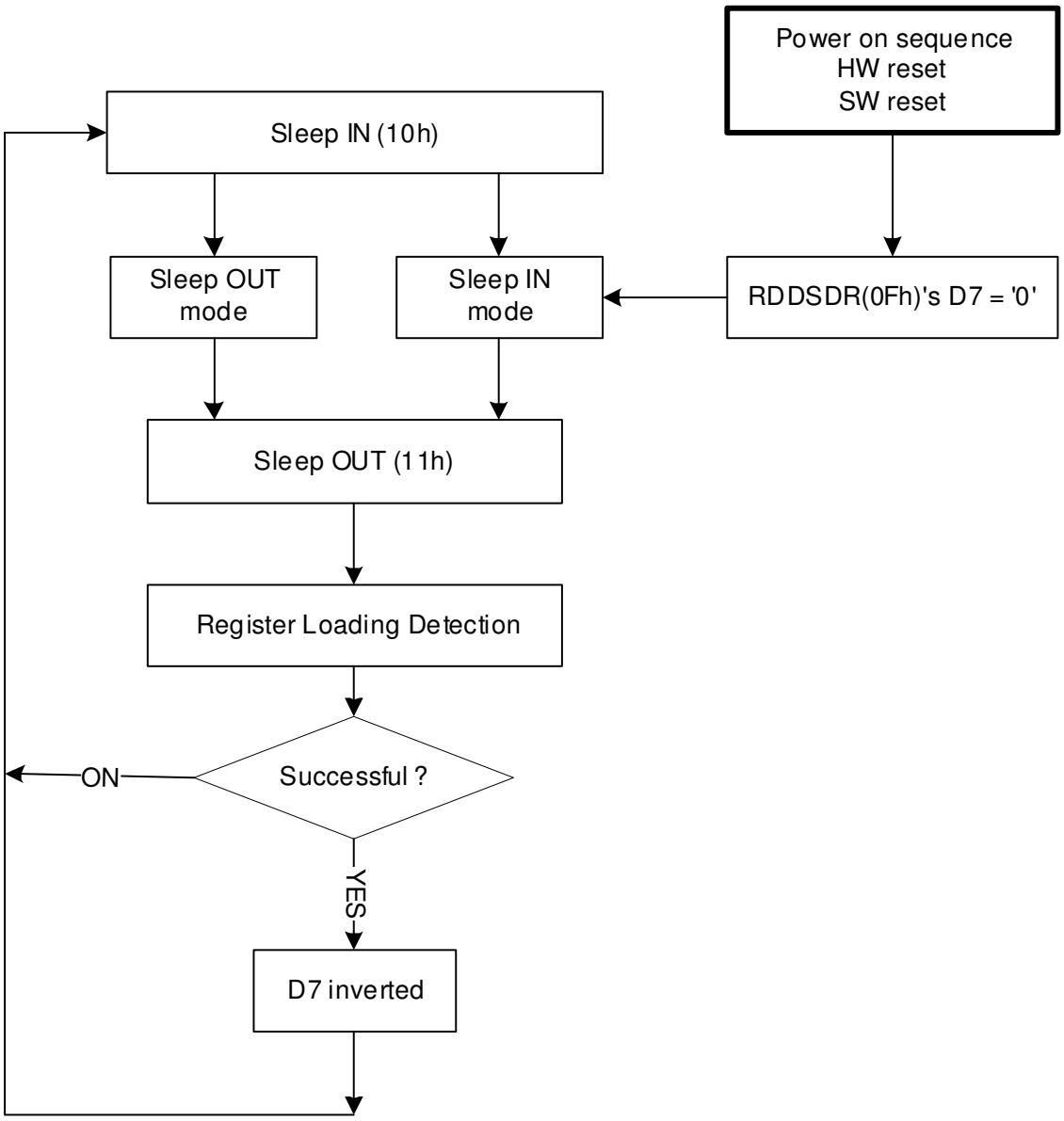
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

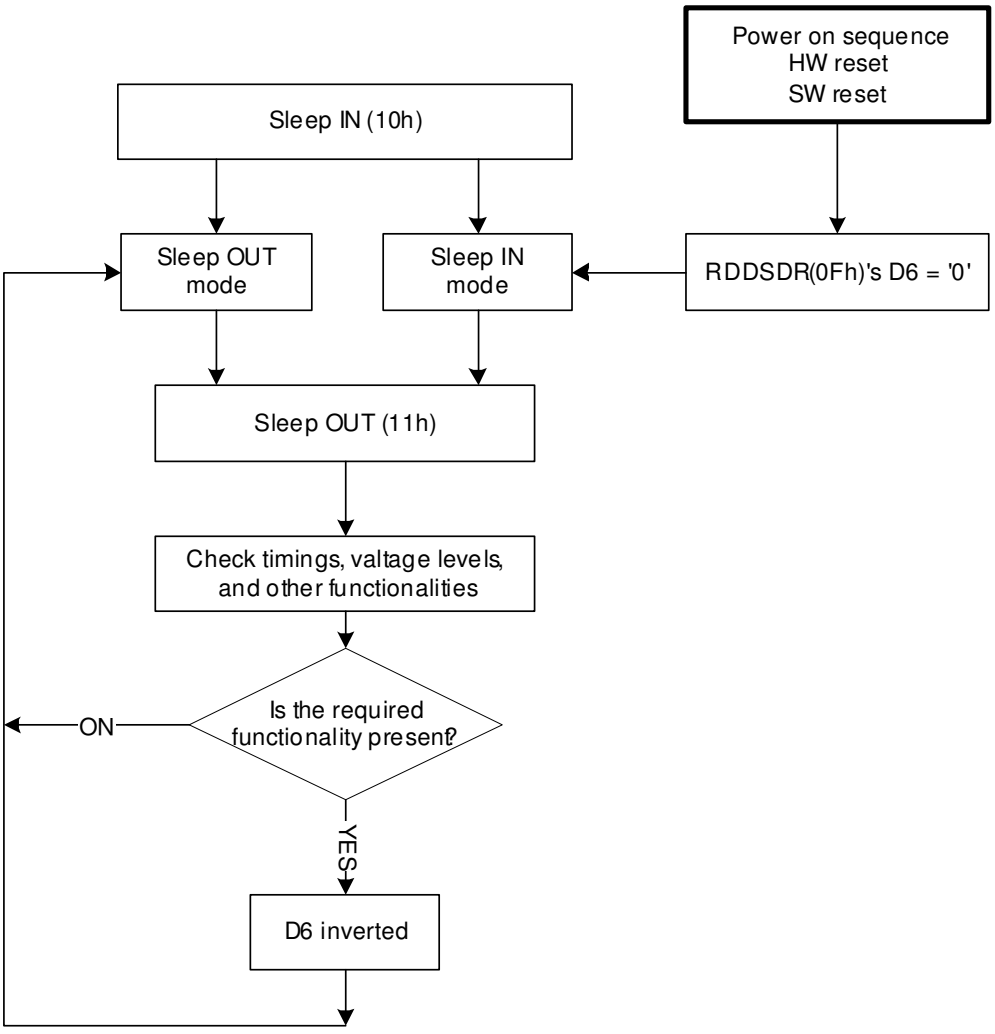


11.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self- Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out –command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order.

VCI and IOVCC can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

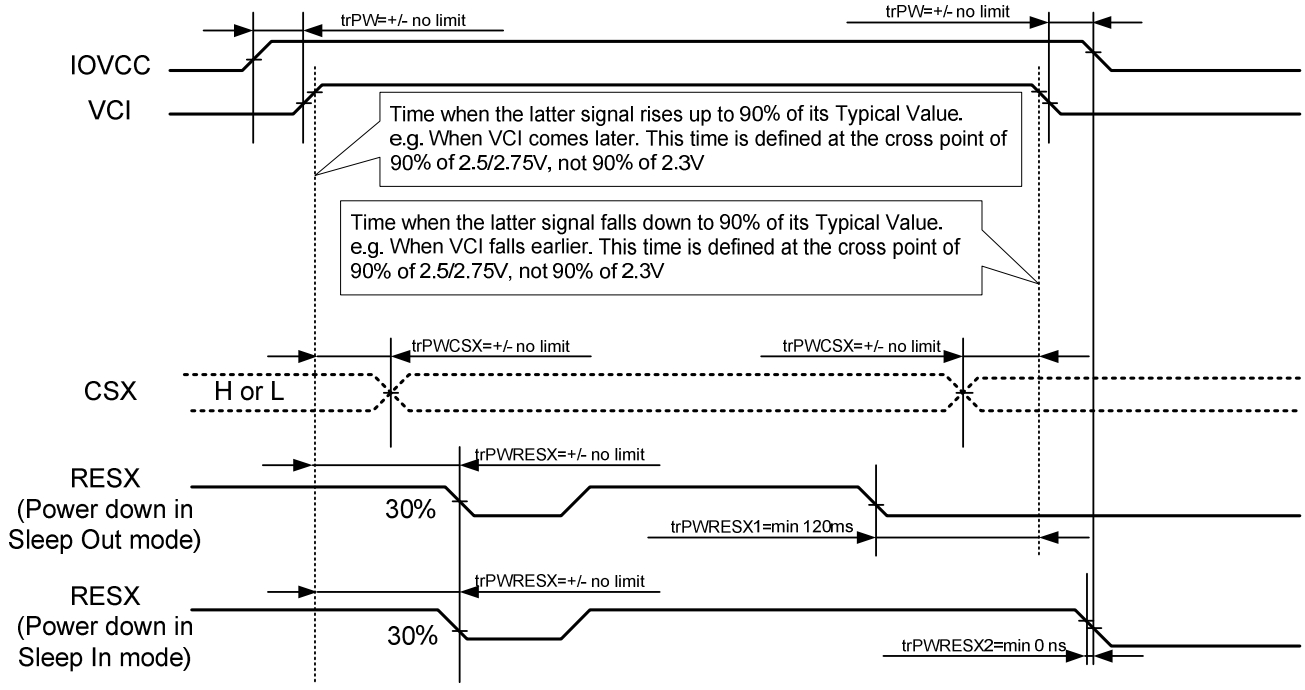
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

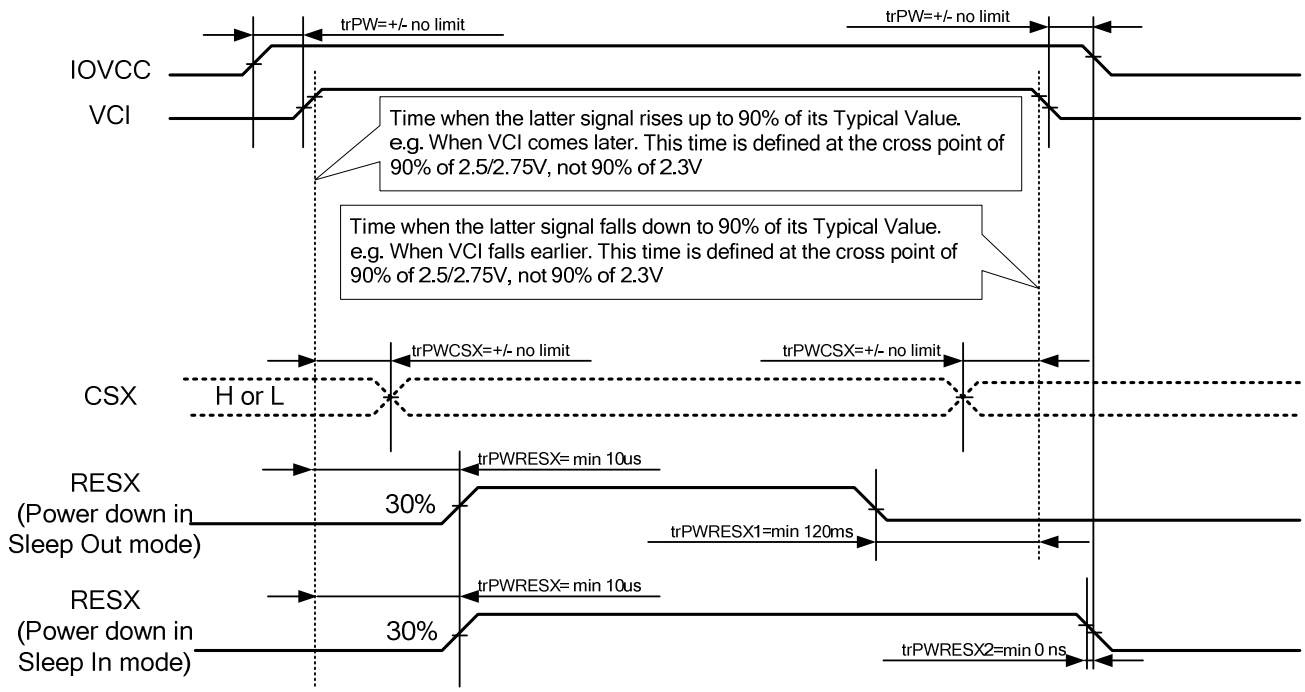


trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9342C will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” actives.

13. Power Level Definition

13.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

   In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

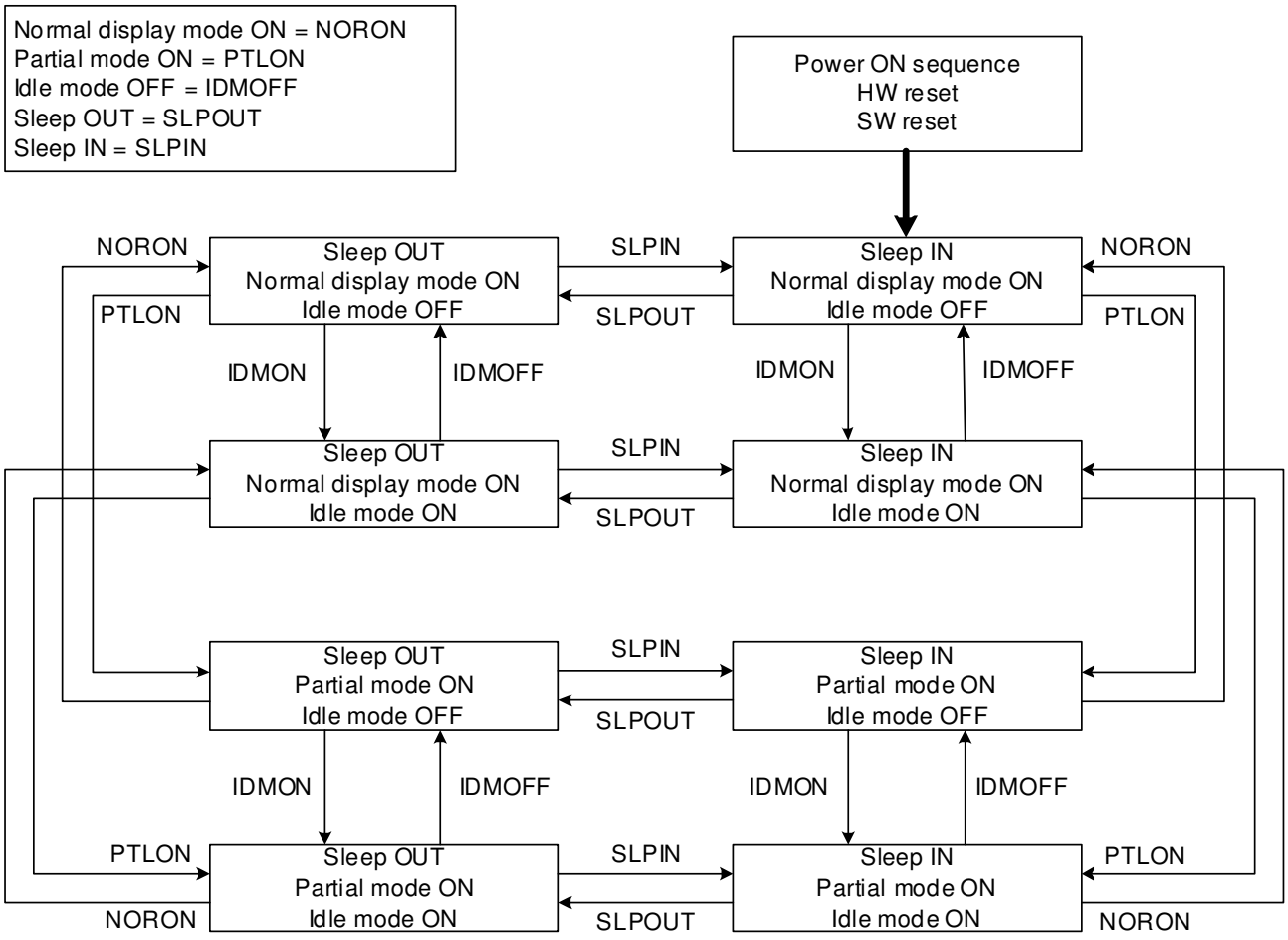
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.

6. Power Off Mode.

   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

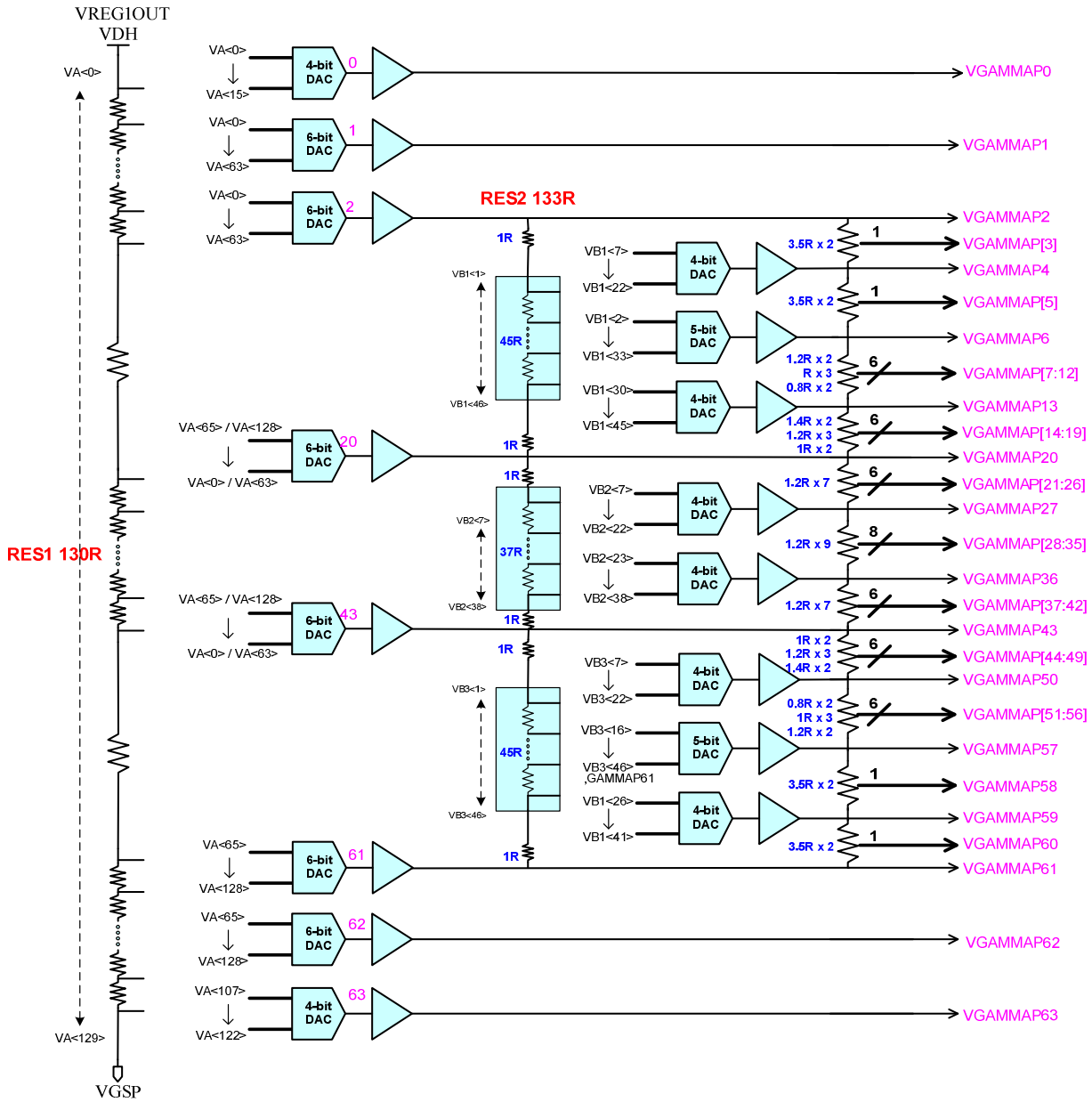
Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

14. Gamma Curves Selection

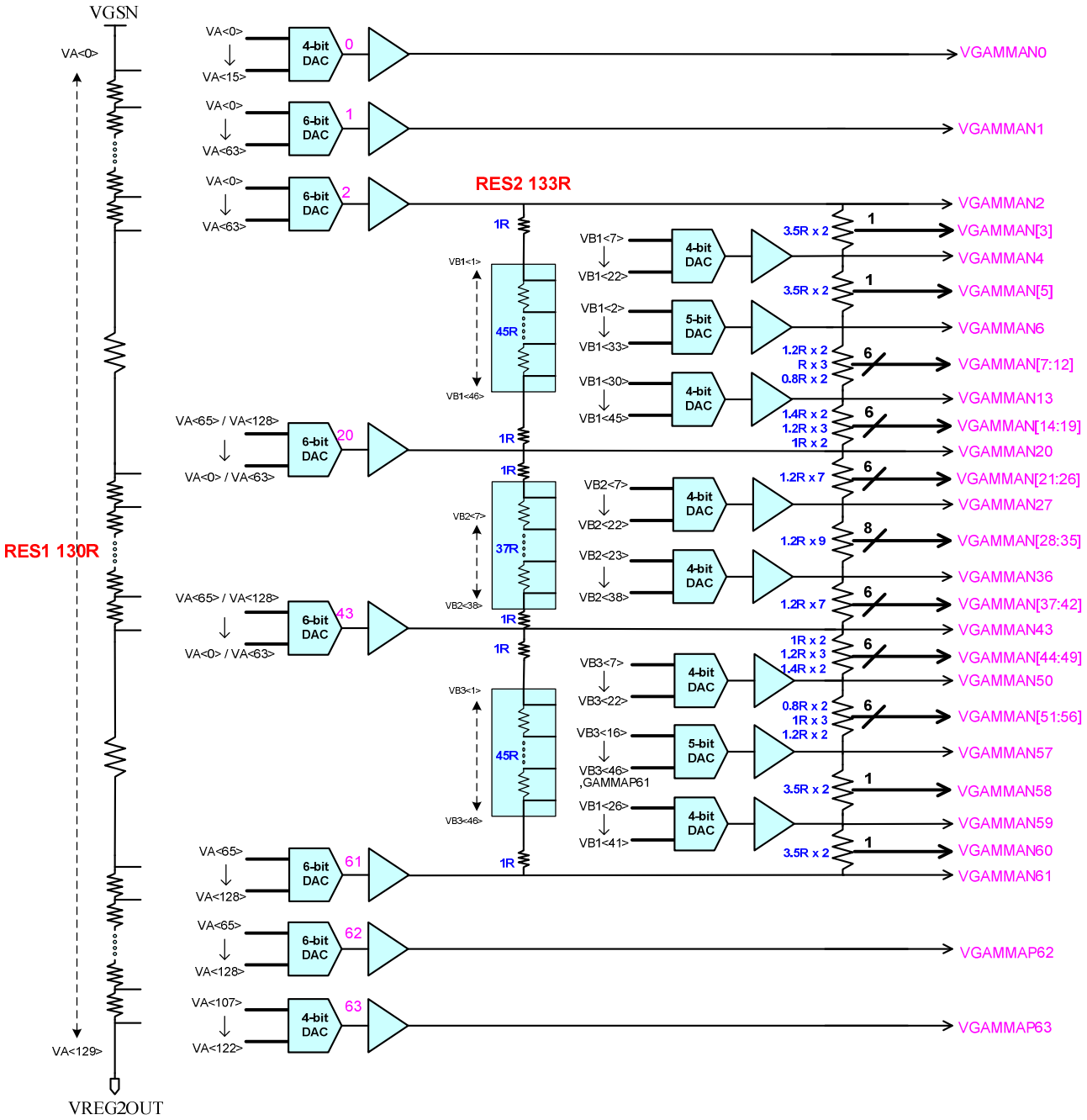
ILI9342C provide four gamma curves (Gamma1.0, Gamma1.8, Gamma2.2 and Gamma2.5). The gamma curve can be selected by the GC0 to GC3 settings. determined

14.1. Gamma Default Values

Positive Gamma Control (E0h)



Negative Gamma Control (E1h)



Positive polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGMMAP0		VGSP＋ΔVDHP(130R-1R*VP0[3:0])/130R
VGMMAP1		VGSP＋ΔVDHP(130R-1R*VP0[5:0])/130R
VGMMAP2	3.5R	VGSP＋ΔVDHP(130R-1R*VP0[5:0])/130R
VGMMAP3	3.5R	VGAMMAP4+(VGAMMP2-VGAMMAP4)*(3.5R)/(7R)
VGMMAP4	3.5R	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((40R-1R*VP4[3:0])/47R)
VGMMAP5	3.5R	VGAMMAP6+(VGAMMP4-VGAMMAP6)*(3.5R)/(7R)
VGMMAP6	1.2R	VGAMMAP13+(VGAMMP6-VGAMMAP13)*(5.8R)/(7R)
VGMMAP7	1.2R	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((45R-1R*VP6[4:0])/47R)
VGMMAP8	1R	VGAMMAP13+(VGAMMP6-VGAMMAP13)*(4.6R)/(7R)
VGMMAP9	1R	VGAMMAP13+(VGAMMP6-VGAMMAP13)*(3.6R)/(7R)
VGMMAP10	1R	VGAMMAP13+(VGAMMP6-VGAMMAP13)*(2.6R)/(7R)
VGMMAP11	0.8R	VGAMMAP13+(VGAMMP6-VGAMMAP13)*(1.6R)/(7R)
VGMMAP12	0.8R	VGAMMAP13+(VGAMMP6-VGAMMAP13)*(0.8R)/(7R)
VGMMAP13	1.4R	VGAMMAP20+(VGAMMAP2-VGAMMAP20)*((17R-1R*VP13[3:0])/47R)
VGMMAP14	1.4R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(7R)/(8.4R)
VGMMAP15	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(5.6R)/(8.4R)
VGMMAP16	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(4.4R)/(8.4R)
VGMMAP17	1.2R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(3.2R)/(8.4R)
VGMMAP18	1R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(2R)/(8.4R)
VGMMAP19	1R	VGAMMAP20+(VGAMMP13-VGAMMAP20)*(1R)/(8.4R)
VGMMAP20	1.2R	VGSP+ΔVDHP(130R-1R*VP20[5:0])/130R : VP20[5:0]=0~63 VGSP+ΔVDHP(129R-1R*VP20[5:0])/130R : VP20[5:0]=64~127
VGMMAP21	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(7.2R)/(8.4R)
VGMMAP22	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(6R)/(8.4R)
VGMMAP23	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(4.8R)/(8.4R)
VGMMAP24	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(3.6R)/(8.4R)
VGMMAP25	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(2.4R)/(8.4R)
VGMMAP26	1.2R	VGAMMAP27+(VGAMMP20-VGAMMAP27)*(1.2R)/(8.4R)
VGMMAP27	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((32R-1R*VP27[3:0])/39R)
VGMMAP28	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(9.6R)/(10.8R)
VGMMAP29	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(8.4R)/(10.8R)
VGMMAP30	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(7.2R)/(10.8R)
VGMMAP31	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(6R)/(10.8R)
VGMMAP32	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(4.8R)/(10.8R)
VGMMAP33	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(3.6R)/(10.8R)
VGMMAP34	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(2.4R)/(10.8R)

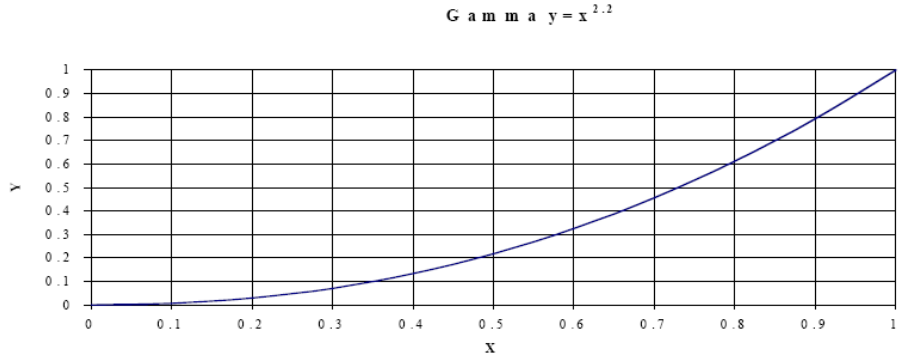
VGMMAP35	1.2R	VGAMMAP36+(VGAMMP27-VGAMMAP36)*(1.2R)/(10.8R)
VGMMAP36	1.2R	VGAMMAP43+(VGAMMAP20-VGAMMAP43)*((16R-1R*VP36[3:0])/39R)
VGMMAP37	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(7.2R)/(8.4R)
VGMMAP38	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(6R)/(8.4R)
VGMMAP39	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(4.8R)/(8.4R)
VGMMAP40	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(3.6R)/(8.4R)
VGMMAP41	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(2.4R)/(8.4R)
VGMMAP42	1.2R	VGAMMAP43+(VGAMMP36-VGAMMAP43)*(1.2R)/(8.4R)
VGMMAP43	1R	VGSP+ΔVDHP(130R-1R*VP43[5:0])/130R : VP43[5:0]=0~63 VGSP+ΔVDHP(129R-1R*VP43[5:0])/130R : VP43[5:0]=64~127
VGMMAP44	1R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(7.4R)/(8.4R)
VGMMAP45	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(6.4R)/(8.4R)
VGMMAP46	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(5.2R)/(8.4R)
VGMMAP47	1.2R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(4R)/(8.4R)
VGMMAP48	1.4R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(2.8R)/(8.4R)
VGMMAP49	1.4R	VGAMMAP50+(VGAMMP43-VGAMMAP50)*(1.4R)/(8.4R)
VGMMAP50	0.8R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((40R-1R*VP50[3:0])/47R)
VGMMAP51	0.8R	VGAMMAP57+(VGAMMP50-VGAMMAP57)*(6.2R)/(7R)
VGMMAP52	1R	VGAMMAP57+(VGAMMP50-VGAMMAP57)*(5.4R)/(7R)
VGMMAP53	1R	VGAMMAP57+(VGAMMP50-VGAMMAP57)*(4.4R)/(7R)
VGMMAP54	1R	VGAMMAP57+(VGAMMP50-VGAMMAP57)*(3.4R)/(7R)
VGMMAP55	1.2R	VGAMMAP57+(VGAMMP50-VGAMMAP57)*(2.4R)/(7R)
VGMMAP56	1.2R	VGAMMAP57+(VGAMMP50-VGAMMAP57)*(1.2R)/(7R)
VGMMAP57	3.5R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((31R-1R*VP57[3:0])/47R)
VGMMAP58	3.5R	VGAMMAP59+(VGAMMP57-VGAMMAP59)*(3.5R)/(7R)
VGMMAP59	3.5R	VGAMMAP61+(VGAMMAP43-VGAMMAP61)*((21R-1R*VP59[3:0])/47R)
VGMMAP60	3.5R	VGAMMAP61+(VGAMMP59-VGAMMAP61)*(3.5R)/(7R)
VGMMAP61		VGSP+ΔVDHP(65R-1R*VP61[5:0])/130R
VGMMAP62		VGSP+ΔVDHP(65R-1R*VP62[5:0])/130R
VGMMAP63		VGSP+ΔVDHP(23R-1R*VP63[3:0])/130R

Negative polarity	Resister stream	Gamma 64 grayscale voltage calculation formula
VGMMAP63		VREG2OUT+ΔVDHN(23R-1R*VN63[3:0])/130R
VGMMAP62		VREG2OUT+ΔVDHN(65R-1R*VN62[5:0])/130R
VGMMAP61		VREG2OUT+ΔVDHN(65R-1R*VN61[5:0])/130R
VGMMAP60	3.5R	VGAMMAN61+(VGAMMP59-VGAMMAN61)*(3.5R)/(7R)
VGMMAP59	3.5R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((21R-1R*VN59[3:0])/47R)
VGMMAP58	3.5R	VGAMMAN59+(VGAMMP57-VGAMMAN59)*(3.5R)/(7R)
VGMMAP57	3.5R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((31R-1R*VN57[3:0])/47R)
VGMMAP56	1.2R	VGAMMAN57+(VGAMMP50-VGAMMAN57)*(1.2R)/(7R)
VGMMAP55	1.2R	VGAMMAN57+(VGAMMP50-VGAMMAN57)*(2.4R)/(7R)
VGMMAP54	1R	VGAMMAN57+(VGAMMP50-VGAMMAN57)*(3.4R)/(7R)
VGMMAP53	1R	VGAMMAN57+(VGAMMP50-VGAMMAN57)*(4.4R)/(7R)
VGMMAP52	1R	VGAMMAN57+(VGAMMP50-VGAMMAN57)*(5.4R)/(7R)
VGMMAP51	0.8R	VGAMMAN57+(VGAMMP50-VGAMMAN57)*(6.2R)/(7R)
VGMMAP50	0.8R	VGAMMAN61+(VGAMMAN43-VGAMMAN61)*((40R-1R*VN50[3:0])/47R)
VGMMAP49	1.4R	VGAMMAN50+(VGAMMP43-VGAMMAN50)*(1.4R)/(8.4R)
VGMMAP48	1.4R	VGAMMAN50+(VGAMMP43-VGAMMAN50)*(2.8R)/(8.4R)
VGMMAP47	1.2R	VGAMMAN50+(VGAMMP43-VGAMMAN50)*(4R)/(8.4R)
VGMMAP46	1.2R	VGAMMAN50+(VGAMMP43-VGAMMAN50)*(5.2R)/(8.4R)
VGMMAP45	1.2R	VGAMMAN50+(VGAMMP43-VGAMMAN50)*(6.4R)/(8.4R)
VGMMAP44	1R	VGAMMAN50+(VGAMMP43-VGAMMAN50)*(7.4R)/(8.4R)
VGMMAP43	1R	VREG2OUT+ΔVDHN(130R-1R*VN43[5:0])/130R : VN43[5:0]=0~63 VREG2OUT+ΔVDHN(129R-1R*VN43[5:0])/130R : VN43[5:0]=64~127
VGMMAP42	1.2R	VGAMMAN43+(VGAMMP36-VGAMMAN43)*(1.2R)/(8.4R)
VGMMAP41	1.2R	VGAMMAN43+(VGAMMP36-VGAMMAN43)*(2.4R)/(8.4R)
VGMMAP40	1.2R	VGAMMAN43+(VGAMMP36-VGAMMAN43)*(3.6R)/(8.4R)
VGMMAP39	1.2R	VGAMMAN43+(VGAMMP36-VGAMMAN43)*(4.8R)/(8.4R)
VGMMAP38	1.2R	VGAMMAN43+(VGAMMP36-VGAMMAN43)*(6R)/(8.4R)
VGMMAP37	1.2R	VGAMMAN43+(VGAMMP36-VGAMMAN43)*(7.2R)/(8.4R)
VGMMAP36	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((16R-1R*VN36[3:0])/39R)
VGMMAP35	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(1.2R)/(10.8R)
VGMMAP34	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(2.4R)/(10.8R)
VGMMAP33	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(3.6R)/(10.8R)
VGMMAP32	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(4.8R)/(10.8R)
VGMMAP31	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(6R)/(10.8R)
VGMMAP30	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(7.2R)/(10.8R)
VGMMAP29	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(8.4R)/(10.8R)

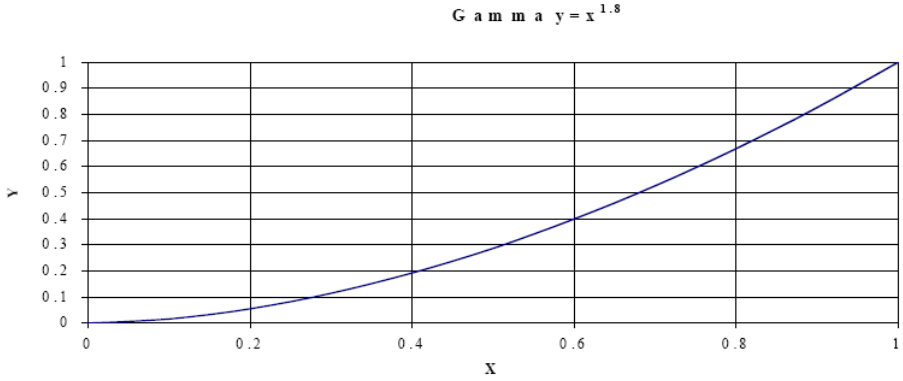
VGMMAP28	1.2R	VGAMMAN36+(VGAMMP27-VGAMMAN36)*(9.6R)/(10.8R)
VGMMAP27	1.2R	VGAMMAN43+(VGAMMAN20-VGAMMAN43)*((32R-1R*VN27[3:0])/39R)
VGMMAP26	1.2R	VGAMMAN27+(VGAMMP20-VGAMMAN27)*(1.2R)/(8.4R)
VGMMAP25	1.2R	VGAMMAN27+(VGAMMP20-VGAMMAN27)*(2.4R)/(8.4R)
VGMMAP24	1.2R	VGAMMAN27+(VGAMMP20-VGAMMAN27)*(3.6R)/(8.4R)
VGMMAP23	1.2R	VGAMMAN27+(VGAMMP20-VGAMMAN27)*(4.8R)/(8.4R)
VGMMAP22	1.2R	VGAMMAN27+(VGAMMP20-VGAMMAN27)*(6R)/(8.4R)
VGMMAP21	1.2R	VGAMMAN27+(VGAMMP20-VGAMMAN27)*(7.2R)/(8.4R)
VGMMAP20	1.2R	VREG2OUT+△VDHN(130R-1R*VN20[5:0])/130R : VN20[5:0]=0~63 VREG2OUT+△VDHN(129R-1R*VN20[5:0])/130R : VN20[5:0]=64~127
VGMMAP19	1R	VGAMMAN20+(VGAMMP13-VGAMMAN20)*(1R)/(8.4R)
VGMMAP18	1R	VGAMMAN20+(VGAMMP13-VGAMMAN20)*(2R)/(8.4R)
VGMMAP17	1.2R	VGAMMAN20+(VGAMMP13-VGAMMAN20)*(3.2R)/(8.4R)
VGMMAP16	1.2R	VGAMMAN20+(VGAMMP13-VGAMMAN20)*(4.4R)/(8.4R)
VGMMAP15	1.2R	VGAMMAN20+(VGAMMP13-VGAMMAN20)*(5.6R)/(8.4R)
VGMMAP14	1.4R	VGAMMAN20+(VGAMMP13-VGAMMAN20)*(7R)/(8.4R)
VGMMAP13	1.4R	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((17R-1R*VN13[3:0])/47R)
VGMMAP12	0.8R	VGAMMAN13+(VGAMMP6-VGAMMAN13)*(0.8R)/(7R)
VGMMAP11	0.8R	VGAMMAN13+(VGAMMP6-VGAMMAN13)*(1.6R)/(7R)
VGMMAP10	1R	VGAMMAN13+(VGAMMP6-VGAMMAN13)*(2.6R)/(7R)
VGMMAP9	1R	VGAMMAN13+(VGAMMP6-VGAMMAN13)*(3.6R)/(7R)
VGMMAP8	1R	VGAMMAN13+(VGAMMP6-VGAMMAN13)*(4.6R)/(7R)
VGMMAP7	1.2R	VGAMMAN13+(VGAMMP6-VGAMMAN13)*(5.8R)/(7R)
VGMMAP6	1.2R	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((45R-1R*VN6[4:0])/47R)
VGMMAP5	3.5R	VGAMMAN6+(VGAMMP4-VGAMMAN6)*(3.5R)/(7R)
VGMMAP4	3.5R	VGAMMAN20+(VGAMMAN2-VGAMMAN20)*((40R-1R*VN4[3:0])/47R)
VGMMAP3	3.5R	VGAMMAN4+(VGAMMP2-VGAMMAN4)*(3.5R)/(7R)
VGMMAP2	3.5R	VREG2OUT+ΔVDHN(130R-1R*VN2[5:0])/130R
VGMMAP1		VREG2OUT+ΔVDHN(130R-1R*VN1[5:0])/130R
VGMMAP0		VREG2OUT+ΔVDHN(130R-1R*VN0[3:0])/130R

14.2. Gamma Curves

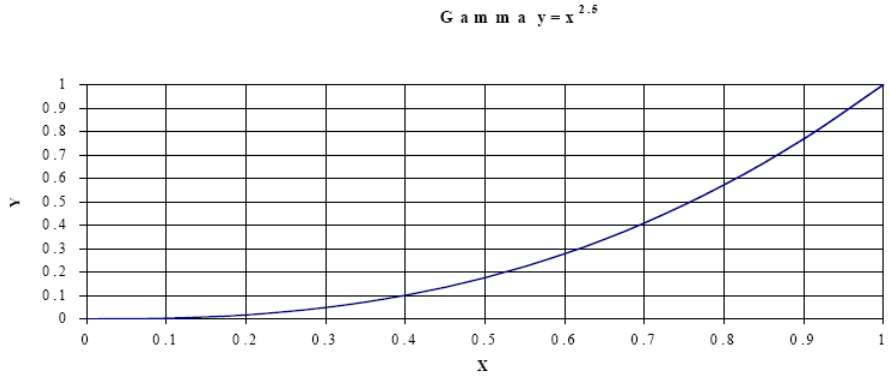
14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



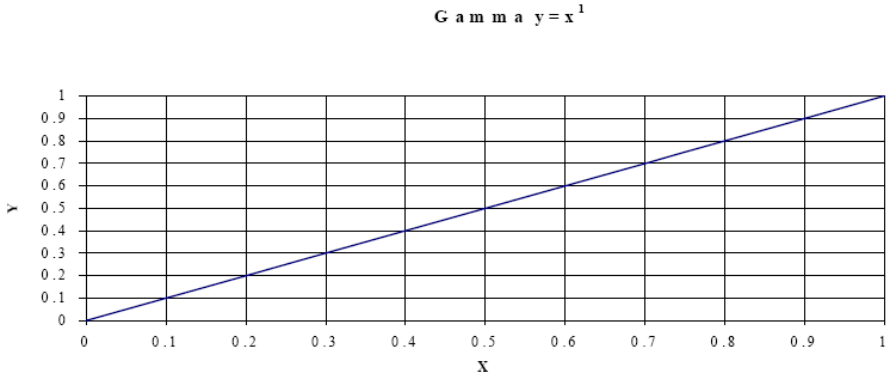
14.2.2. Gamma Curve 2 (GC1), applies the function $y=x^{1.8}$



14.2.3. Gamma Curve 3 (GC2), applies the function $y=x^{2.5}$



14.2.4. Gamma Curve 4 (GC3), applies the function $y=x^{1.0}$



15. Reset

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's D5=0:00EF h If MADCTL's D5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's D5 = 0:013F h If MADCTL's D5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	00EF h	00EF h	00EF h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10µs after both VCI *& IOVCC are applied.*

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

15.2. Output Pins, I/O Pins

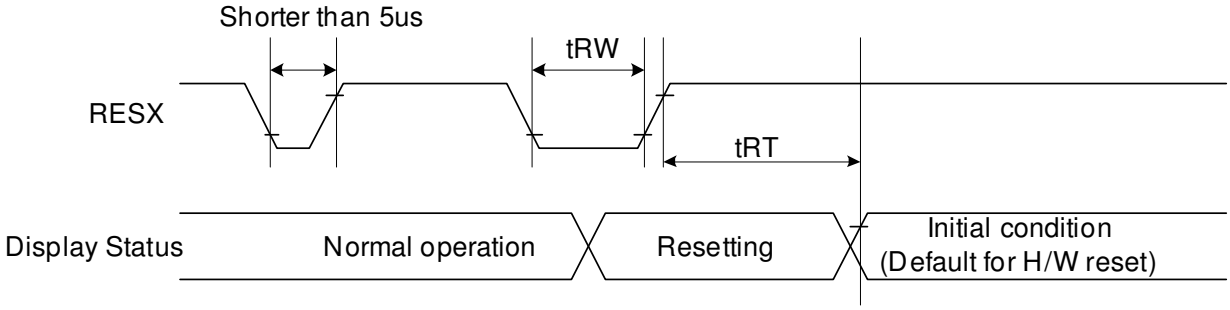
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

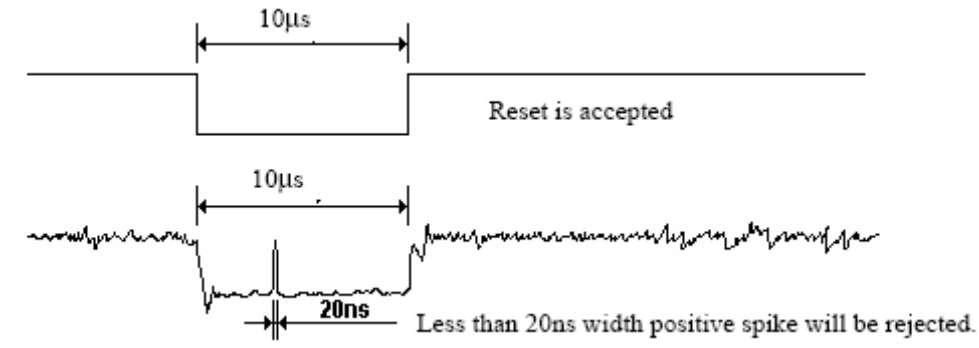
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

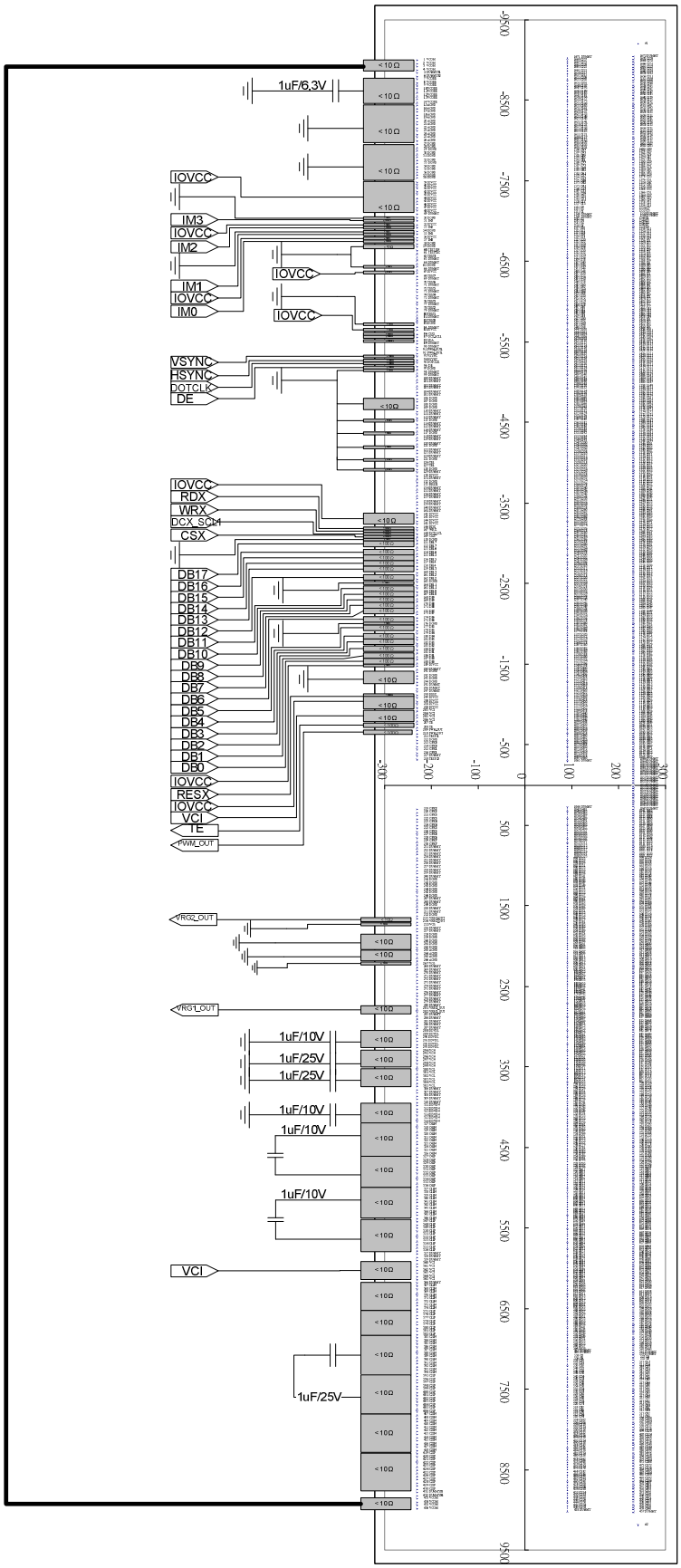


Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

16. Configuration of Power Supply Circuit



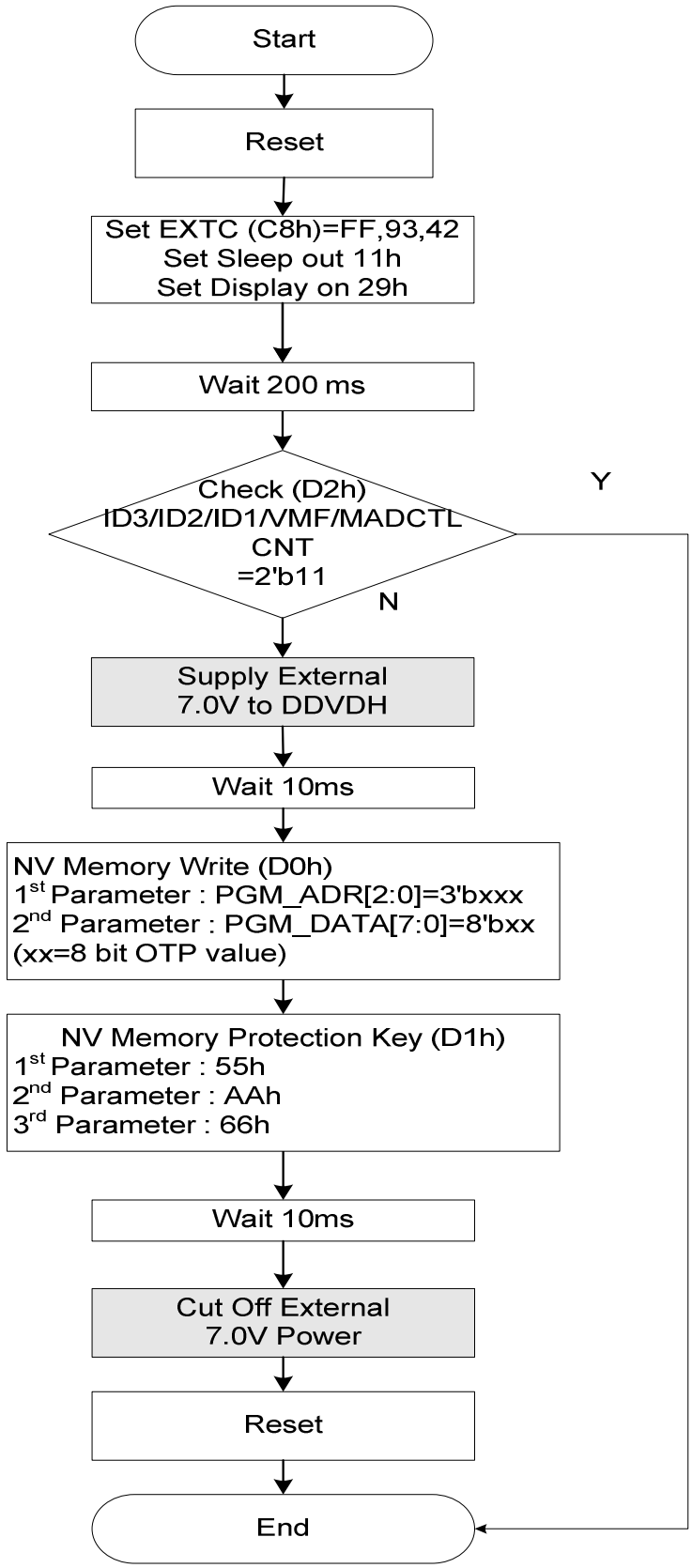
The Following tables shows specifications of external elements connected to the ILI9342C's power supply

circuit.

Only 8 capacitors are needed in ILI9342C and other capacitors are Panel dependent.Please check the recommended 8 capacitors specification as below.

Items	Recommended Specification	Pin connection
Capacity 1uF (B characteristics)	6.3V	Vcore
	10V	DDVDH,DDVDL,C11N/P,C41N/P,
	16V	VGL, C21N/P
	25V	VGH

17. NV Memory Programming Flow



NOTE: For using "Internal voltage for OTP flow", the gray block steps can be skipped.

18. Electrical Characteristics

18.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9342C is used out of the absolute maximum ratings, ILI9342C may be permanently damaged. To use ILI9342C within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9342C will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.2
Supply voltage (Logic)	IOVCC	V	-0.3 ~ +4.2
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.4
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ IOVCC + 0.5
Logic output voltage range	VO	V	-0.3 ~ IOVCC + 0.5
Operating temperature	Topr	℃	-30 ~ +70
Storage temperature	Tstg	℃	-55 ~ +110
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

18.2. DC Characteristics

18.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.6	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	1.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	GND	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	GND	-	0.2*IOVCC	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or GND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM Amplitude	VCOMA	V		-2.0	-	-0.4	Note3
Source Driver							
Source Output Range	Vsout	V	-	DDVDH +0.1	-	DDVDH-0.1	Note4
Positive Gamma Reference Voltage	VREG1OUT	V	-	3.6	-	DDVDH-0.3	Note3
Negative Gamma Reference Voltage	VREG2OUT	V	-	DDVDL-0.3	-	-3.6	Note3

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, AGND=GND=0V, Ta=-30 to 70 (to +80 no damage) ℃.

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

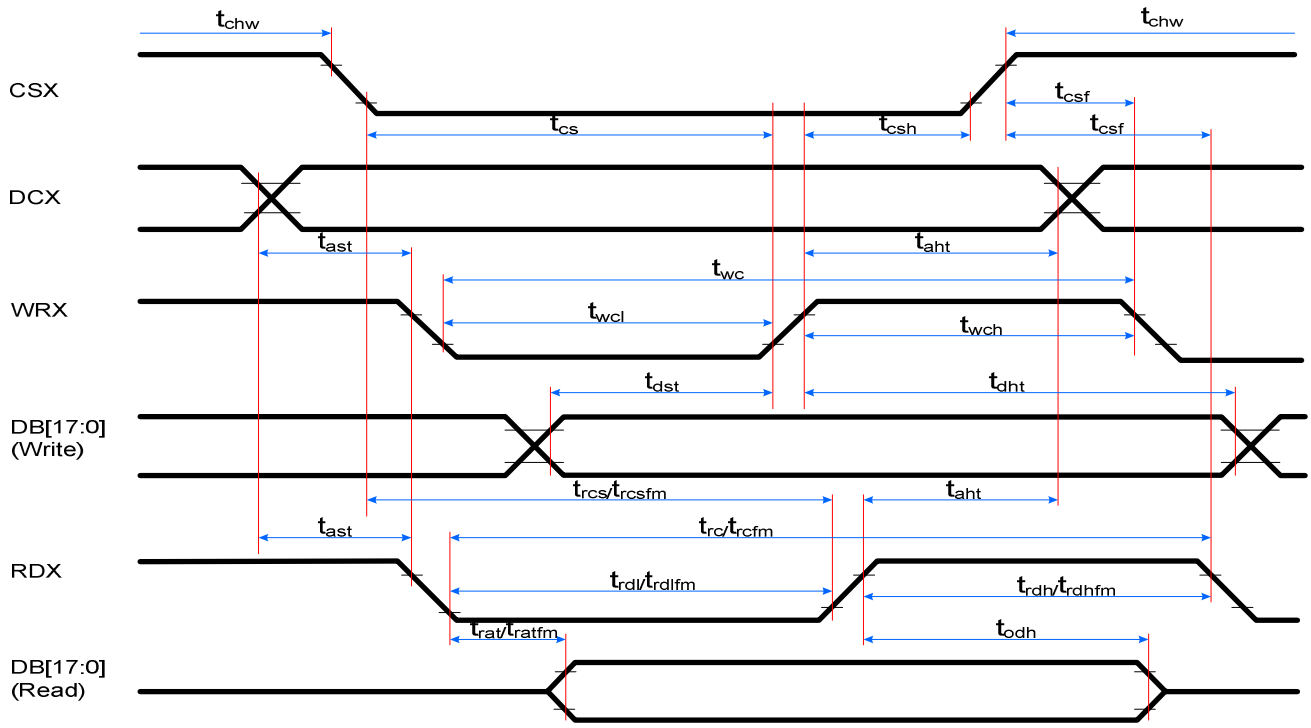
Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

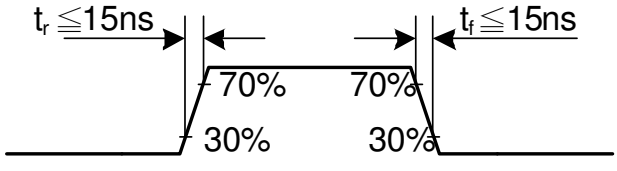
18.3. AC Characteristics

18.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

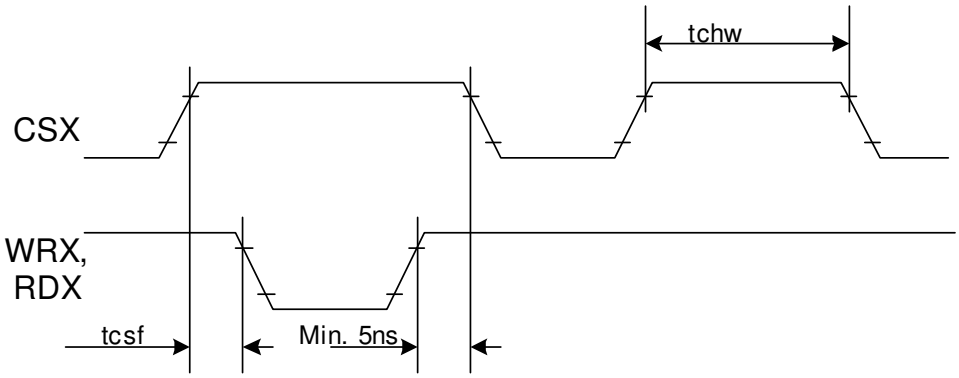


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX “H” pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.3V, VCI=2.6V to 3.3V, GND=0V

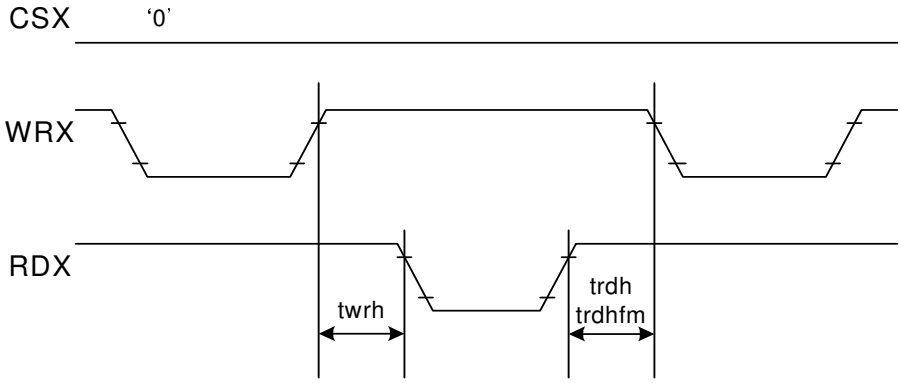


CSX timings :



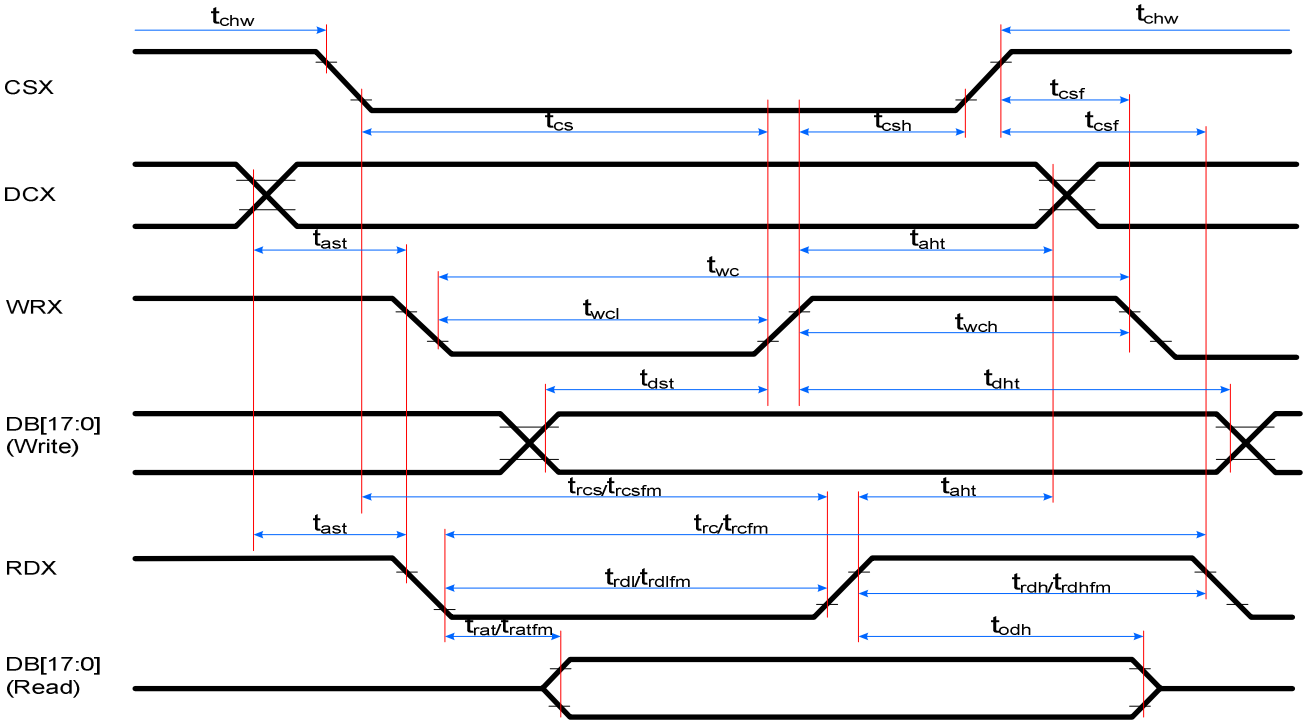
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



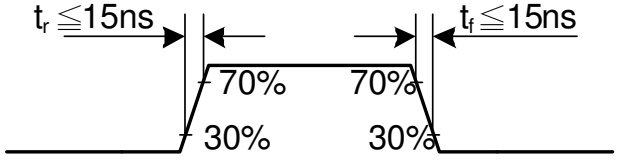
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

18.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)

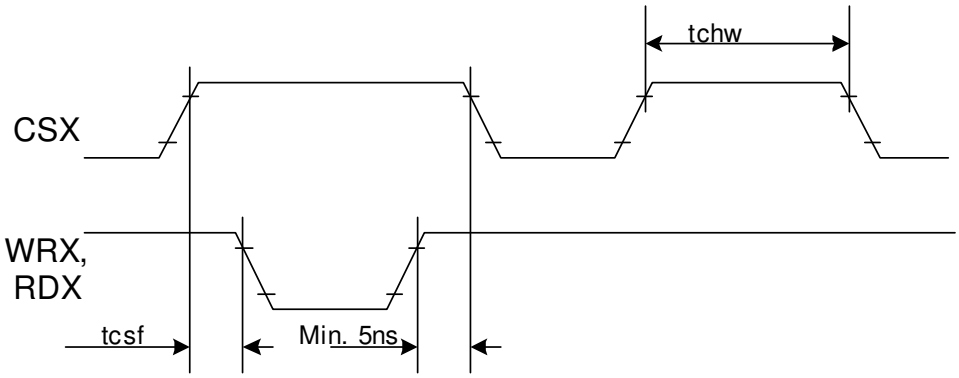


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.3V, VCI=2.6V to 3.3V, GND=0V.

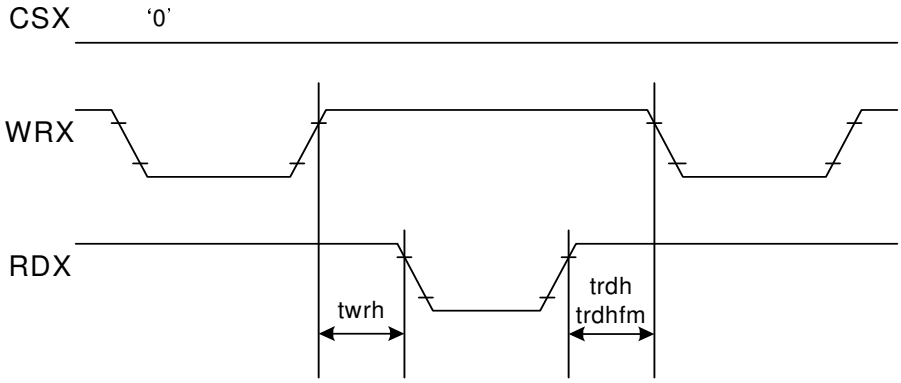


CSX timins :



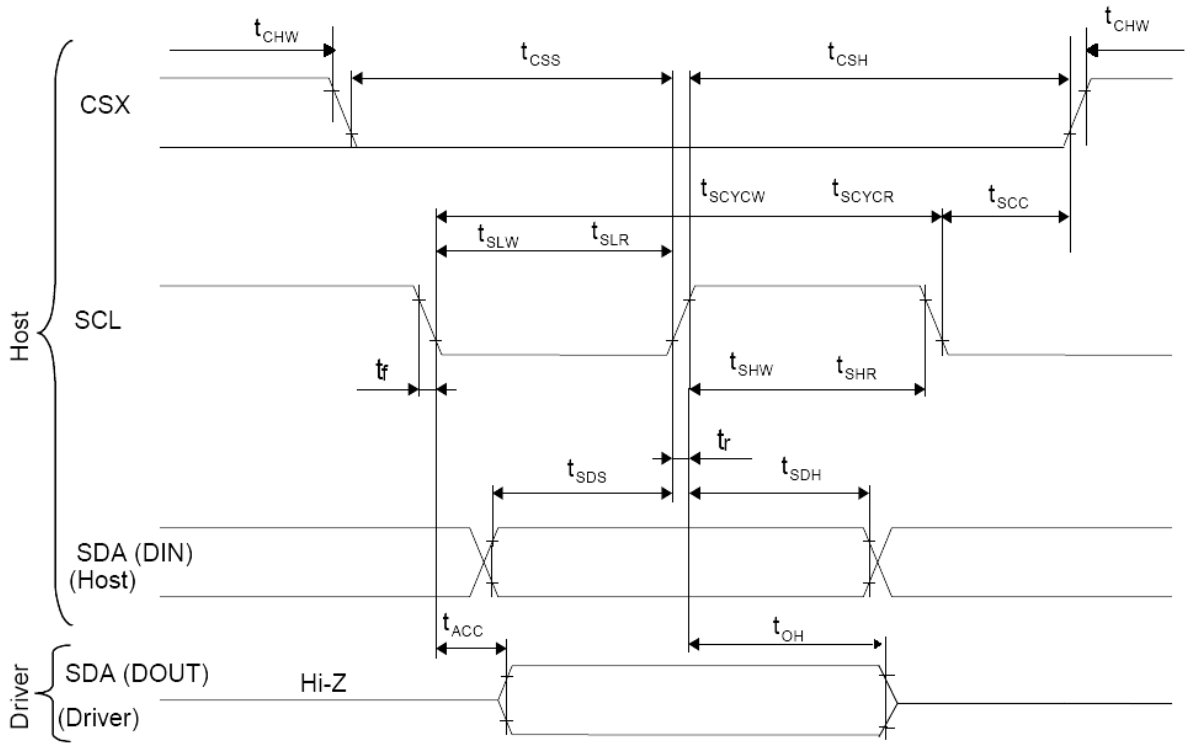
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



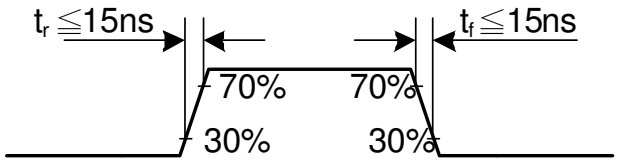
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

18.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

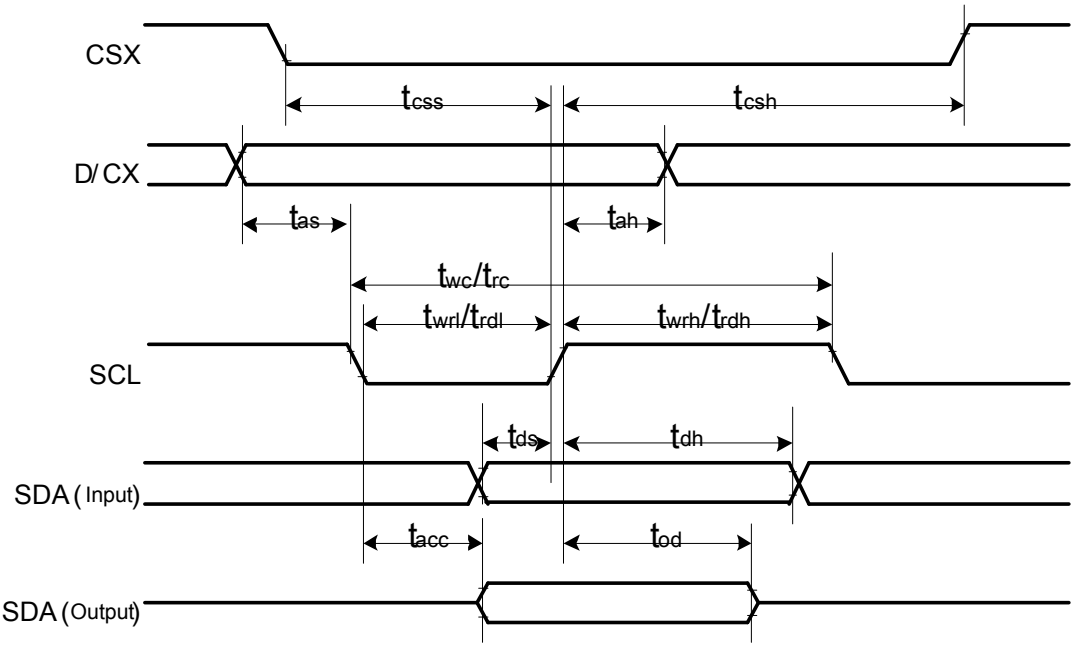


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL “H” Pulse Width (Write)	35	-	ns	
	tslw	SCL “L” Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL “H” Pulse Width (Read)	60	-	ns	
	tslr	SCL “L” Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX “H” Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	30	-	ns	
	tcsh		30	-	ns	

Note: Ta = 25 ℃, IOVCC=1.65V to 3.3V, VCI=2.6V to 3.3V, AGND=GND=0V

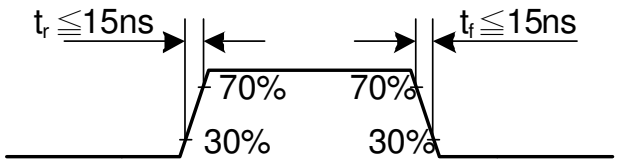


18.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

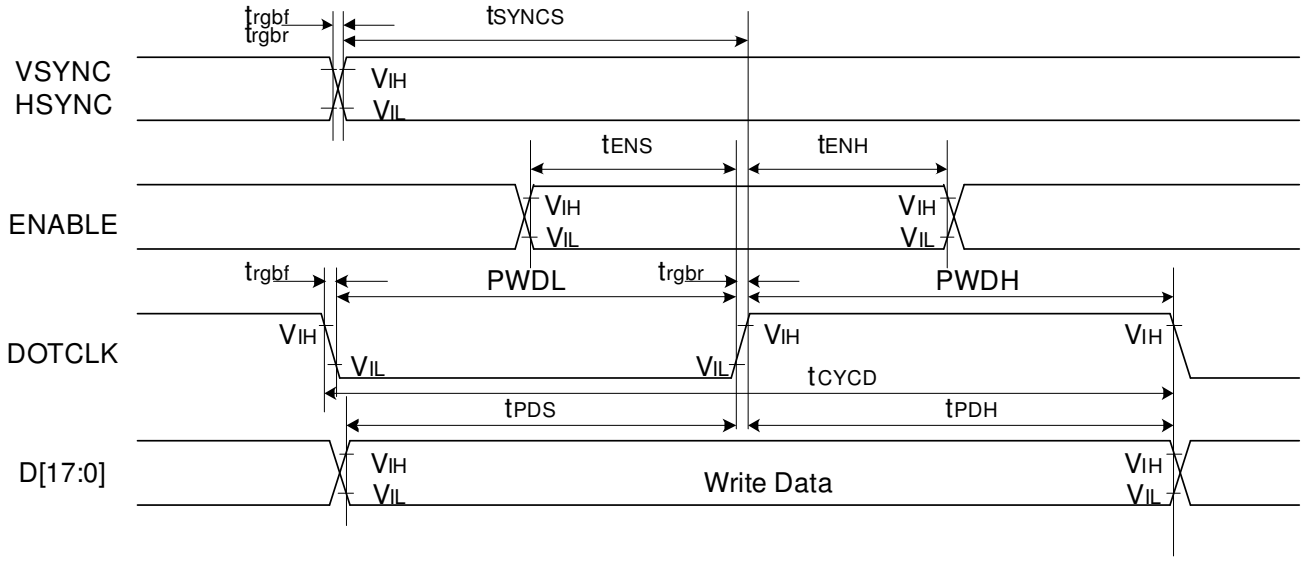


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	30	-	ns	
	tcsh	Chip select hold time (write)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL “H” pulse width (Write)	35	-	ns	
	twrl	SCL “L” pulse width (Write)	35	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL “H” pulse width (Read)	60	-	ns	
	trdl	SCL “L” pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	-	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = 25 ℃, IOVCC=1.65V to 3.3V, VCI=2.6V to 3.3V, AGND=GND=0V

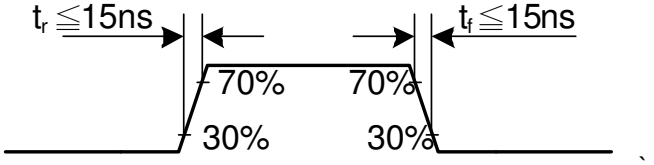


18.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 3.3V, VCI=2.6V to 3.3V, AGND=GND=0V



19. Revision History

Version No.	Date	Page	Description
V0.01	2010/11/01	All	New Created
V0.02	2011/04/18	All	1. Modify model name. 2. Update Pad location 367~382 (C12P/N)
V0.03	2011/05/02	All	1. Remove command R3Ch,R3Eh,R44h,R45h 2. Modify NV Memory Programming Flow Supply External 7.0V to VPP 3. Remove RC2h,RC3h,RC4h selects the operating frequency 1/16H 4. Update RC0h default 5. Update RB1h default 6. Modify DOTCLK cycle time min. is 100 ns 7. Command RBFh change to RBEh Addr. 8. Frame Rate Control removed DIVA function(RB1h,RB2h,RB3h)
V0.04	2011/5/11	15	Update chip size
V0.05	2011/6/13	149~154	Update I RTNA 60~70Hz
V006	2011/8/16	All 13,18 All All 146 150~159 220~221 224 225~229	1. Modify IOVCC & VCI 2. Vreg2out add to pin descriptions and pad 253,254 3. AVDD modify another noun.(DDVDH) 4. VCL modify another noun.(DDVDL) 5. Add R68h command 6. Update RTNA level 7. Modify configuration of power supply circuit 8. Modify VIH,VIL. 9. Update twrl, twrh, trat, tscycw, tshw, tslw, tshr, tslr, toh.
V100	2011/8/30 ~ 2011/9/6 2011/10/24	All 11~14	1. Revise IOVCC spec to 1.65~2.8V 2. Revise VCI spec to 2.6~3.3V 3. Revise operational temperature to -30 ~ +70 ℃ 4. Trim redundant descriptions 5. Revise typo and wrong description 6. update Command & parameter default value 7. Add description for R68h register 8. Revise all the description for the diagram and figure that doesn't match spec 9. Revise AC timing value to match Nokia spec 10. Add description (CSX1=CSX,RESX1=RESX,DCX_SCL1 = DCX_SCL,TE1 = TE PWM_OUT1 = PWM_OUT)
		14 16 135~136	11. Add description for VPP 12. Revise alignment mark. 13. Add description for R44h, R45h registers.
V101	2011/12/14 2011/12/26 2012/01/05	225 17 16 223 13	1. Modify NV Memory Programming Flow. 2. Remove VPP pad.(195,196,197) 3. Modify chip thickness:250um 4. Modify Configuration of Power Supply Circuit that only 8 capacitors are needed. 5. Modify C12P/N and C22P/N descriptions.
V102	2012/3/28 2012/3/29	224 16	1. Modify Configuration of Power Supply Circuit. 2. Revise chip center.
V103	2012/12/18	All 224	1. Modify IOVCC voltage values. 2. Modify the maximum capacitor voltage values of VGL and C21N/P.