Specification

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
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Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P001	-	New release	E02160001	Plato	2016/02/03
P002	Page 2	Boost ratio of voltage converter is X5/X6/X8	E06160010	Michael	2016/06/29
	Page 27~28	Updated ICON RAM mapping table	E06160010		
	Page 30~32	Updated frame rate command, Delete effuse entry command, Add DIV control command, Add AC return zero command	E06160010		
	Page 37	Updated duty calculation table	E06160010		
	Page 42	Add DIV control command, Updated entry IST test command flow	E06160010		
	Page 57	Updated IIC interface	E06160010		
P003	Page 31,42,43	Add “frame rate adjusting enable” command Add “OSC clock select” command Updated IST test command write flow	E09160008	Michael	2016/09/26
P004	Page 30,36	Updated “follow control” command	E08170001	Michael	2017/08/03
001	Page 47	Updated Power Supply Current Removed “Preilimlnary”	E06180002	Michael	2018/06/06
002	Page 37	Add “Note for Cursor"	E07180005	Plato	2018/07/19
003	Page 29,31,34,35,37	1. Instruction table modify, remove S function of Entry Mode 2. Set Entry Mode function description modify (remove display shift direction function) 3. Curser/Display shift function description correction and	E08180004	Plato	2018/08/17

		annotation. 4. SLEEP mode annotation. Using SLEEP command to turned off or resume display. 5. Set Display pattern typo correction			
004	Page 8	Modify serial clock define from "SDI(DB6)" to "SCL(DB6)"	E10180003	Plato	2018/10/24
005	Page 42	Modify OSC Divide Select	E12180010	Plato	2018/12/14
006	Page10,11,51	Add Serial interface selection instructions	E05200009	Sky	2020/05/29
	Page52	Refine Reset Input Timing			
007	Page 45	Modify ABSOLUTE MAXIMUN RATING (TOPR) from -30C to -40C	E07200002	Plato	2020/07/08
008	Page 51	I2C AC information	E02210001	David	2021/02/04
009	Page 26	ICON and SEG Mapping	E03210001	Plato	2021/03/08
	Page 41	Duty6~0 change to DUTY			
	Page 42	Command 10110011 change to 11100011			
010	P29/P30	Add Instruction time	E08210003	Plato	2021/08/05
011	P24	Modify 4-line Display mode	E10220002	Sky	2022/10/25
012	P21	Modify 2-line Display mode	E12240002	Sean	2024/12/13
013	P16/P44	Modify IIC Interface Protocol Modify Booster Circuits	E04250005	Zico	2025/04/23

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

IST3602

24 Character x 4 Lines with 120 Icons

Character-type (5x8) LCD Controller/Driver

INTRODUCTION

IST3602 is a character display controller and driver LSI for dot-matrix liquid crystal display. It's especially designed for VA & EBN LCD Display Module, It can display alphanumeric, Japanese kana and symbols, which are store in the internal Character Generator ROM. It can be configured by a microprocessor with 8-bit parallel interface (6800/8080 series MPU), 3-Line/4-Line serial interface or I2C interface.

IST3602 is designed for low voltage supplied applications especially for portable products, and especially for the battery-driven applications. IST3602 integrates with DDRAM (Display Data RAM), CGROM/CGRAM (Character Generator ROM/RAM), Icon RAM, LCD drivers (SEG, COM) and LCD power circuits.

The internal CGROM has 256 fonts, every font defined by 5x8 dots, and 8 fonts in CGRAM, every fonts defined by 5X8bit RAM cells. Fonts in CGRAM can use to replace part (all) of the first column of CGROM by configured through MPU.

The LCD module can be set as 1-line/2-line/3-line/4-line x 24 characters with 120 ICON. The LCD scan direction is controlled by instruction. One LCD module can be used in different view directions without hardware modification.

FEATURES

Power Supply

-Logic Power VDD1 –GROUND = 1.8V ~ 3.6V
-Analog Power VDD2 –GROUND = 2.4V ~ 3.6V
-Analog Power VDD3 –GROUND = 2.4V ~ 3.6V
-LCD Driving V0 – GROUND = 18V (Max)

Display Driver Output Circuits

- 33 common outputs / 120 segment outputs
- Display Duty = 1/9,1/17,1/25 1/33 select by command HLINE and NLINE
- Applicable Bias: 1/4 ~ 1/7

On-chip Display CGRAM(Character Generator RAM)

-RAM size : 24x4 =96bytes
-

On-chip Display ICON RAM

-RAM size : 24x5 =120 bits

On-chip Display CGROM(Character Generator)

-ROM size : 256X8X5 =10,240 bits

Built-in Analog Circuit

- On-chip oscillator circuit for display clock (external clock can also be used)
- High performance voltage converter (with booster ratios X5/X6/X7/X8)
- High accuracy reference voltage generator
- Electronic contrast control (64 steps)
- Embedded V0 Voltage regulator
- High performance voltage follower (V1 ~ V4 voltage generator with output buffer inside)

Microprocessor Interface

- High-speed 8080/6800-series 8-bit parallel bi-directional interface
- Serial 3 line Write/Read interface
- Serial 4 line Write/Read interface
- IIC interface

Various Function Set

- Display On/Off control
- Set display starting line,
- Set row/column address
- Software reset
- Reverse display
- COM/SEG output direction control
- Display power control
- LCD Contrast (V0) control

Operating Temperatures

- Wide range of operating temperatures from -30℃ to 80℃

Package Type

- COG(Gold-bumped bared chip)

BLOCK DIAGRAM

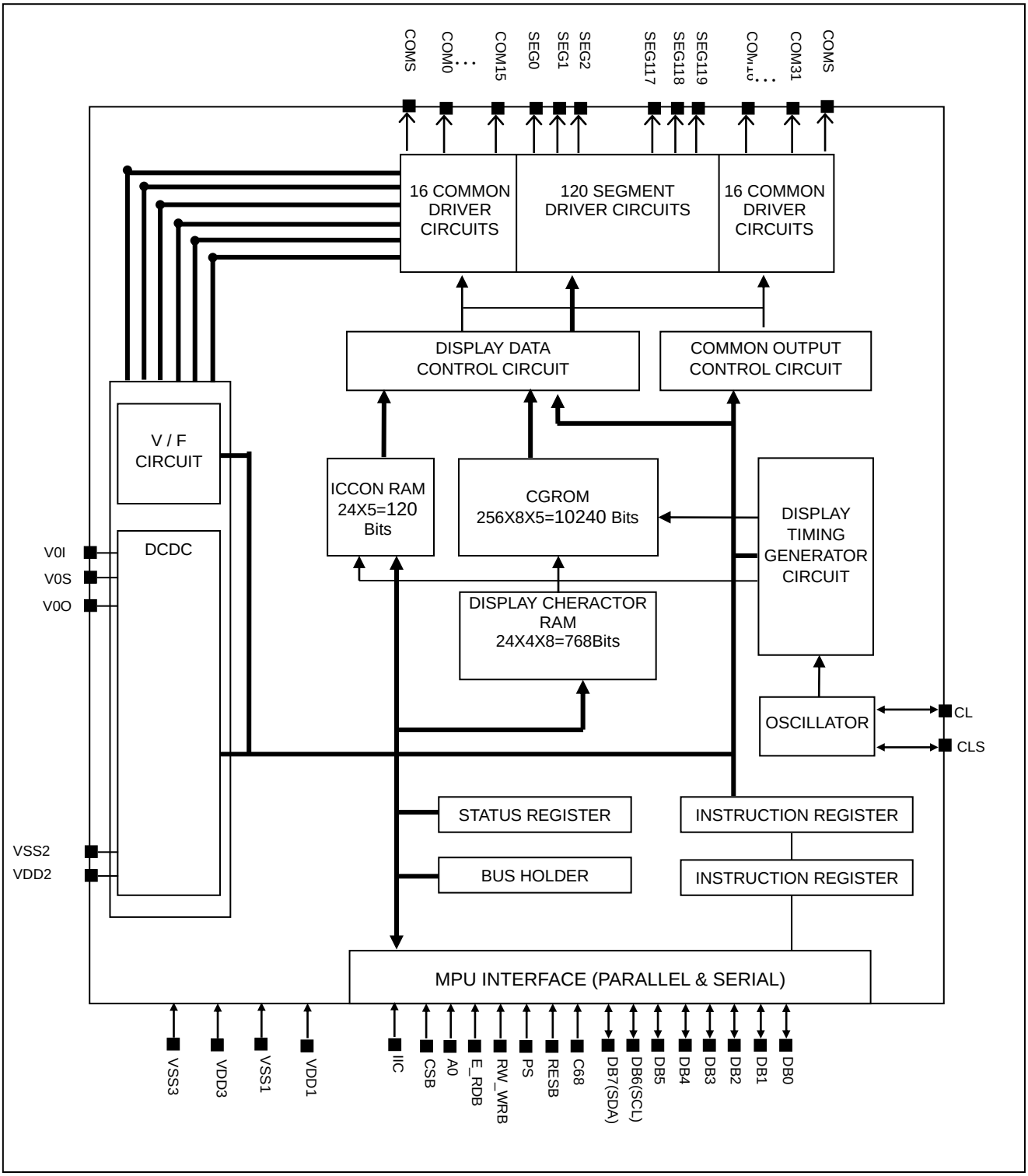
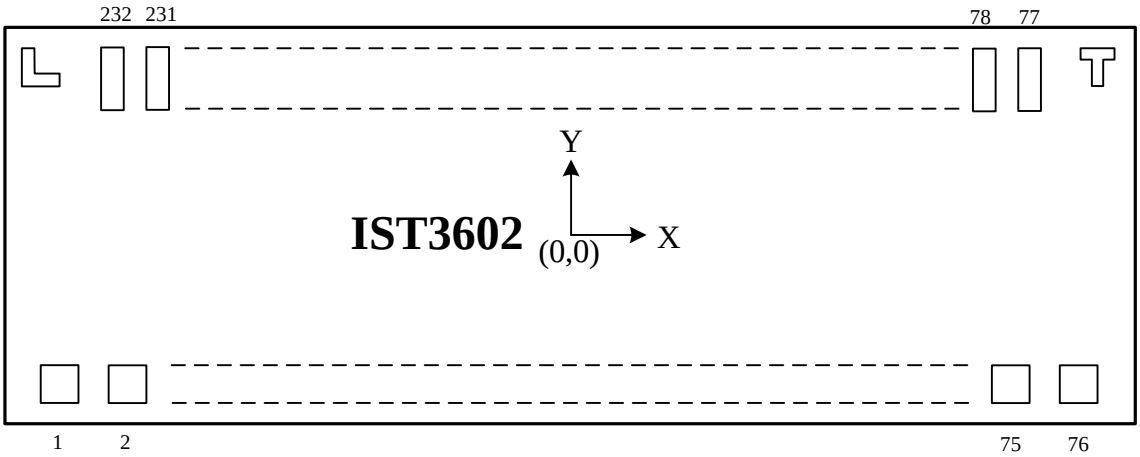
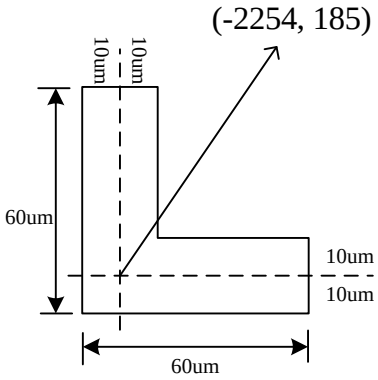
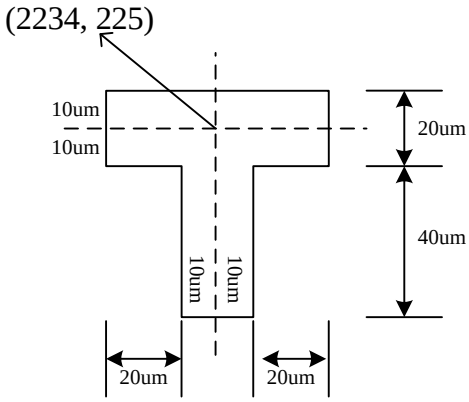


Figure 1 Block Diagram

PAD CONFIGURATION







Chip Size	4652 x 650 (Exclude Scribe Lane)	
Chip Thickness	300um(Typ)	
Bump Height	12um(Typ)	
Bump Pitch	27um(min)	
Bump Spacing	13um(min)	
Bump Size(X*Y)	30 x 40 um2	Pad No. = 1 ~ 76
	14 x 86 um2	Pad No. = 77 ~ 232

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	NC	-2250	-230	51	NC	750	-230	101	SEG<113>	1444.5	205
2	NC	-2190	-230	52	NC	810	-230	102	SEG<112>	1417.5	205
3	CSB	-2130	-230	53	NC	870	-230	103	SEG<111>	1390.5	205
4	RESB	-2070	-230	54	NC	930	-230	104	SEG<110>	1363.5	205
5	A0	-2010	-230	55	NC	990	-230	105	SEG<109>	1336.5	205
6	WRB	-1950	-230	56	NC	1050	-230	106	SEG<108>	1309.5	205
7	RDB	-1890	-230	57	NC	1110	-230	107	SEG<107>	1282.5	205
8	VDD1	-1830	-230	58	NC	1170	-230	108	SEG<106>	1255.5	205
9	VSS1	-1770	-230	59	NC	1230	-230	109	SEG<105>	1228.5	205
10	DB<0>	-1710	-230	60	NC	1290	-230	110	SEG<104>	1201.5	205
11	DB<1>	-1650	-230	61	NC	1350	-230	111	SEG<103>	1174.5	205
12	DB<2>	-1590	-230	62	NC	1410	-230	112	SEG<102>	1147.5	205
13	DB<3>	-1530	-230	63	NC	1470	-230	113	SEG<101>	1120.5	205
14	DB<4>	-1470	-230	64	NC	1530	-230	114	SEG<100>	1093.5	205
15	DB<5>	-1410	-230	65	NC	1590	-230	115	SEG<99>	1066.5	205
16	DB<6>	-1350	-230	66	NC	1650	-230	116	SEG<98>	1039.5	205
17	DB<7>	-1290	-230	67	NC	1710	-230	117	SEG<97>	1012.5	205
18	C68	-1230	-230	68	NC	1770	-230	118	SEG<96>	985.5	205
19	PS	-1170	-230	69	NC	1830	-230	119	SEG<95>	958.5	205
20	IIC	-1110	-230	70	NC	1890	-230	120	SEG<94>	931.5	205
21	VDD1	-1050	-230	71	NC	1950	-230	121	SEG<93>	904.5	205
22	VDD1	-990	-230	72	V0O	2010	-230	122	SEG<92>	877.5	205
23	VSS1	-930	-230	73	V0O	2070	-230	123	SEG<91>	850.5	205
24	VSS1	-870	-230	74	V0S	2130	-230	124	SEG<90>	823.5	205
25	VSS1	-810	-230	75	V0I	2190	-230	125	SEG<89>	796.5	205
26	VSS1	-750	-230	76	V0I	2250	-230	126	SEG<88>	769.5	205
27	CL	-690	-230	77	NC	2145.5	205	127	SEG<87>	742.5	205
28	CLS	-630	-230	78	COM<15>	2118.5	205	128	SEG<86>	715.5	205
29	VOP	-570	-230	79	COM<14>	2091.5	205	129	SEG<85>	688.5	205
30	TEST1	-510	-230	80	COM<13>	2064.5	205	130	SEG<84>	661.5	205
31	TEST2	-450	-230	81	COM<12>	2037.5	205	131	SEG<83>	634.5	205
32	VDD2	-390	-230	82	COM<11>	2010.5	205	132	SEG<82>	607.5	205
33	VDD2	-330	-230	83	COM<10>	1983.5	205	133	SEG<81>	580.5	205
34	VDD2	-270	-230	84	COM<9>	1956.5	205	134	SEG<80>	553.5	205
35	VDD2	-210	-230	85	COM<8>	1929.5	205	135	SEG<79>	526.5	205
36	VDD2	-150	-230	86	COM<7>	1902.5	205	136	SEG<78>	499.5	205
37	VDD2	-90	-230	87	COM<6>	1875.5	205	137	SEG<77>	472.5	205
38	VDD3	-30	-230	88	COM<5>	1848.5	205	138	SEG<76>	445.5	205
39	VDD3	30	-230	89	COM<4>	1821.5	205	139	SEG<75>	418.5	205
40	VSS3	90	-230	90	COM<3>	1794.5	205	140	SEG<74>	391.5	205
41	VSS3	150	-230	91	COM<2>	1767.5	205	141	SEG<73>	364.5	205
42	VSS2	210	-230	92	COM<1>	1740.5	205	142	SEG<72>	337.5	205
43	VSS2	270	-230	93	COM<0>	1713.5	205	143	SEG<71>	310.5	205
44	VSS2	330	-230	94	COMS	1686.5	205	144	SEG<70>	283.5	205
45	VSS2	390	-230	95	SEG<119>	1606.5	205	145	SEG<69>	256.5	205
46	VSS2	450	-230	96	SEG<118>	1579.5	205	146	SEG<68>	229.5	205
47	VSS2	510	-230	97	SEG<117>	1552.5	205	147	SEG<67>	202.5	205
48	NC	570	-230	98	SEG<116>	1525.5	205	148	SEG<66>	175.5	205
49	NC	630	-230	99	SEG<115>	1498.5	205	149	SEG<65>	148.5	205
50	NC	690	-230	100	SEG<114>	1471.5	205	150	SEG<64>	121.5	205

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	SEG<63>	94.5	205	201	SEG<13>	-1255.5	205				
152	SEG<62>	67.5	205	202	SEG<12>	-1282.5	205				
153	SEG<61>	40.5	205	203	SEG<11>	-1309.5	205				
154	SEG<60>	13.5	205	204	SEG<10>	-1336.5	205				
155	SEG<59>	-13.5	205	205	SEG<9>	-1363.5	205				
156	SEG<58>	-40.5	205	206	SEG<8>	-1390.5	205				
157	SEG<57>	-67.5	205	207	SEG<7>	-1417.5	205				
158	SEG<56>	-94.5	205	208	SEG<6>	-1444.5	205				
159	SEG<55>	-121.5	205	209	SEG<5>	-1471.5	205				
160	SEG<54>	-148.5	205	210	SEG<4>	-1498.5	205				
161	SEG<53>	-175.5	205	211	SEG<3>	-1525.5	205				
162	SEG<52>	-202.5	205	212	SEG<2>	-1552.5	205				
163	SEG<51>	-229.5	205	213	SEG<1>	-1579.5	205				
164	SEG<50>	-256.5	205	214	SEG<0>	-1606.5	205				
165	SEG<49>	-283.5	205	215	COM<16>	-1686.5	205				
166	SEG<48>	-310.5	205	216	COM<17>	-1713.5	205				
167	SEG<47>	-337.5	205	217	COM<18>	-1740.5	205				
168	SEG<46>	-364.5	205	218	COM<19>	-1767.5	205				
169	SEG<45>	-391.5	205	219	COM<20>	-1794.5	205				
170	SEG<44>	-418.5	205	220	COM<21>	-1821.5	205				
171	SEG<43>	-445.5	205	221	COM<22>	-1848.5	205				
172	SEG<42>	-472.5	205	222	COM<23>	-1875.5	205				
173	SEG<41>	-499.5	205	223	COM<24>	-1902.5	205				
174	SEG<40>	-526.5	205	224	COM<25>	-1929.5	205				
175	SEG<39>	-553.5	205	225	COM<26>	-1956.5	205				
176	SEG<38>	-580.5	205	226	COM<27>	-1983.5	205				
177	SEG<37>	-607.5	205	227	COM<28>	-2010.5	205				
178	SEG<36>	-634.5	205	228	COM<29>	-2037.5	205				
179	SEG<35>	-661.5	205	229	COM<30>	-2064.5	205				
180	SEG<34>	-688.5	205	230	COM<31>	-2091.5	205				
181	SEG<33>	-715.5	205	231	COMS	-2118.5	205				
182	SEG<32>	-742.5	205	232	NC	-2145.5	205				
183	SEG<31>	-769.5	205	（END）							
184	SEG<30>	-796.5	205								
185	SEG<29>	-823.5	205								
186	SEG<28>	-850.5	205								
187	SEG<27>	-877.5	205								
188	SEG<26>	-904.5	205								
189	SEG<25>	-931.5	205								
190	SEG<24>	-958.5	205								
191	SEG<23>	-985.5	205								
192	SEG<22>	-1012.5	205								
193	SEG<21>	-1039.5	205								
194	SEG<20>	-1066.5	205								
195	SEG<19>	-1093.5	205								
196	SEG<18>	-1120.5	205								
197	SEG<17>	-1147.5	205								
198	SEG<16>	-1174.5	205								
199	SEG<15>	-1201.5	205								
200	SEG<14>	-1228.5	205								

PIN DESCRIPTION

Power Supply

Name	I/O	Description
VDD1	Power Supply	IO power supply The input voltage range is 1.8V ≤ VDD1 ≤ 3.6V
VDD2 VDD3	Power Supply	Analog Power supply The input voltage range is 2.4V ≤ VDD2 ≤ 3.6V
VSS1	Power Supply	Logic Ground
VSS2	Power Supply	DCDC Ground
VSS3	Power Supply	Analog Ground
V0I V0O V0S	Power Supply	V0I is the power of COM and SEG driver V0S is the sensor of the V0 generator V0O is the output of V0 generator V0O, V0S & V0I should be separated in ITO layout. V0O, V0S & V0I should be connected together in FPC layout.

System Control

Name	I/O	Description
CLS	I	Built-in oscillator circuit enable / disable select pin - CLS = “H” : enable (this pin is used together with digital command) - CLS = “L” : disable (external display clock input through CL pin)
CL	I	External clock input pin, when use built-in oscillator, let it “H”

Micro-Controller Interface

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESB</td><td>I</td><td>Hardware Reset input pin
When RESB is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel / serial data input select input(IIC=H).
<table>
<tr><th>PS</th><th>C68</th><th>Interface mode</th><th>Chip select</th><th>Data / instruction</th><th>Data</th><th>Read / Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>-</td><td>Parallel</td><td>CSB</td><td>A0</td><td>DB0 to DB7</td><td>E_RDB
RW_WRB</td><td>--</td></tr>
<tr><td>L</td><td>H</td><td>SPi3</td><td>CSB</td><td>-</td><td>SDA (DB7)</td><td>Write/Read</td><td>SCL (DB6)</td></tr>
<tr><td>L</td><td>L</td><td>SPi4</td><td>CSB</td><td>A0</td><td>SDA (DB7)</td><td>Write/Read</td><td>SCL (DB6)</td></tr>
</table>
<NOTE> In serial mode, DB0 to DB5 and E_RDB and RW_WRB must be fixed to either “H” or “L”.</td></tr>
<tr><td>C68</td><td>I</td><td>Microprocessor Interface Select input pin in parallel mode(when PS=“H”, IIC=“H”)
- C68 = “H” : 6800-series MPU interface
- C68 = “L” : 8080-series MPU interface</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CSB is “L”.
When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin
- A0 = “H” : DB0 to DB7 are display data
- A0 = “L” : DB0 to DB7 are control data</td></tr>
<tr><td>RW_WRB</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>RW_WRB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read / Write control input pin
- RW = “H” : read
- RW = “L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WRB</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WRB signal.</td></tr>
</table></td></tr>
<tr><td>E_RDB</td><td>I</td><td>Read / Write execution control pin
<table>
<tr><th>C68</th><th>MPU Type</th><th>E_RDB</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
- RW = “H” : When E is “H”, DB0 to DB7 are in an output status.
- RW = “L”: The data on DB0 to DB7 are latched at the falling edge the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RDB</td><td>Read enable clock input pin
When / RDB is “L”, DB0 to DB7 are in an output status.</td></tr>
</table></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td>8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = “L”);
- DB0 to DB5 : high impedance
- DB6 : serial input clock (SCL)
- DB7 : serial input data (SDA)
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>VOP</td><td>I/O</td><td>Test pin, must keep them open</td></tr>
<tr><td>TEST1~2</td><td>I/O</td><td>Test pins, must keep them open</td></tr>
<tr><td>IIC</td><td>I</td><td>IIC mode selection pin. IIC mode is enabled when IIC is “L”, and it disabled when IIC is “H”</td></tr>
</table>

LCD Driver Outputs

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0 ~ SEG119</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>GROUND</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>GROUND</td></tr>
<tr><td colspan="2">Power save mode</td><td>GROUND</td><td>GROUND</td></tr>
<tr><td rowspan="7">COM0 ~ COM31</td><td rowspan="7">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and the FR signal control the output voltage of segment driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">GROUND</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">GROUND</td></tr>
<tr><td>COMS</td><td>O</td><td colspan="4">LCD common driver output for icons.
When icons feature are not used, these pins should be left open.</td></tr>
</table>

I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VDD1,VDD3,VSS1, VSS3,V0O,V0I	<200Ω
VDD2, VSS2	<100Ω
V0S	<300Ω
CSB,RW_WRB,E_RDB,A0,DB0~DB7	<1KΩ
DB6(SCL) and DB7(SDA) for IIC interface	< 500Ω
RESB	<10KΩ
CL,C68,PS,CLS,VOP,IIC	<10KΩ
TEST1, TEST2,VOP	Floating

FUNCTIONAL DESCRIPTION

Microprocessor Interface

Chip select control

There are CSB pins for chip selection. The IST3602 can interface with an MPU only when CSB is “L” . When these pins are set to any other combination, A0, E_RDB, and RW_WRB inputs are disabled and DB0 to DB7 are high impedance. In case of serial interface, the internal shift registers and the counter are reset.

MPU Interface types

IST3602 has five types of MPU interface, which are three serial and two parallel interfaces. This parallel or serial interface is determined by IIC , PS , C68 pin as shown below.

IIC	PS	C68	Type	Interface mode
H	H	H	Parallel	6800-series MPU mode
H	H	L	Parallel	8080-series MPU mod
H	L	H	Serial	3-Line SPI Serial-mode (*2)
H	L	L	Serial	4-Line SPI Serial-mode (*2)
L	ID1(*1)	ID0(*1)	Serial	IIC Serial-mode (*2)

NOTE:
*1) PS/C68 is use as ID1/ID0, IIC host can use ID1/ID0 to select difference IIC device.

*2) For serial Interface, If the serial data(SDA) and serial clock (SCL) pins will be shared with other devices, SPI3 or SPI4 is recommended. If IIC interface is required, there are some application notices that should be regarded. Please contact our FAE member for further information.

Parallel Interface (IIC=“H” PS = “H”)

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68. The type of data transfer is determined by signals at A0, E_RDB and RW_WRB as shown below.

C68	CSB	A0	E_RDB	RW_WRB	DB0 to DB7	MPU bus
H	CSB	A0	E	RW	DB0 to DB7	6800-series
L	CSB	A0	/RDB	/WRB	DB0 to DB7	8080-series

Common	6800-series		8080-series		Description
A0	E_RDB (E)	RW_WRB (RW)	E_RDB (/RDB)	RW_WRB (/WRB)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (IIC="H" PS = "L")

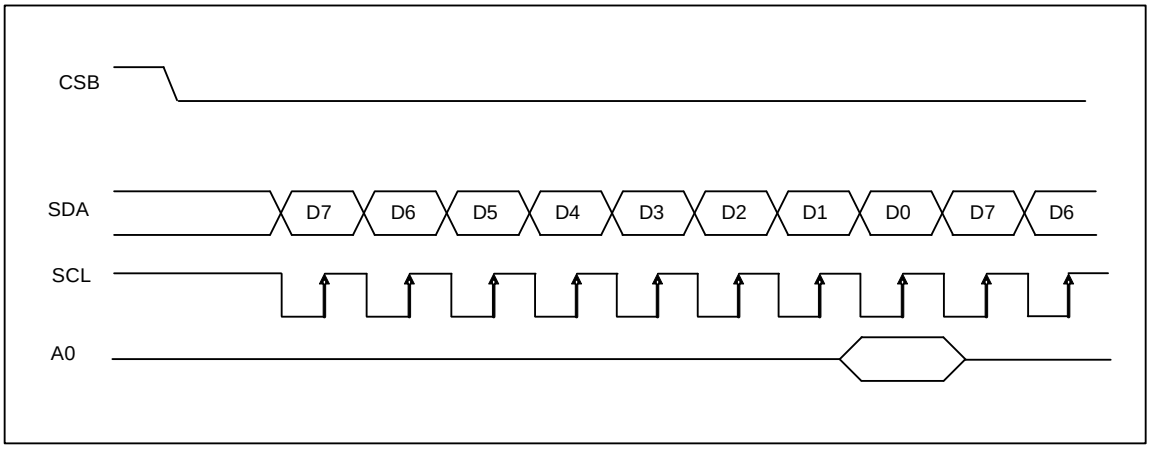
When IIC = "H" PS = "L", the IST3602 is configured as Serial interface(4-line or 3-line), the serial data can be input through DB7 (SDA) and serial clock can be input through DB6 (SCL).

When the chip is not selected, the shift register & serial data counter will be reset and SDA & SCL will also be disabled internally.

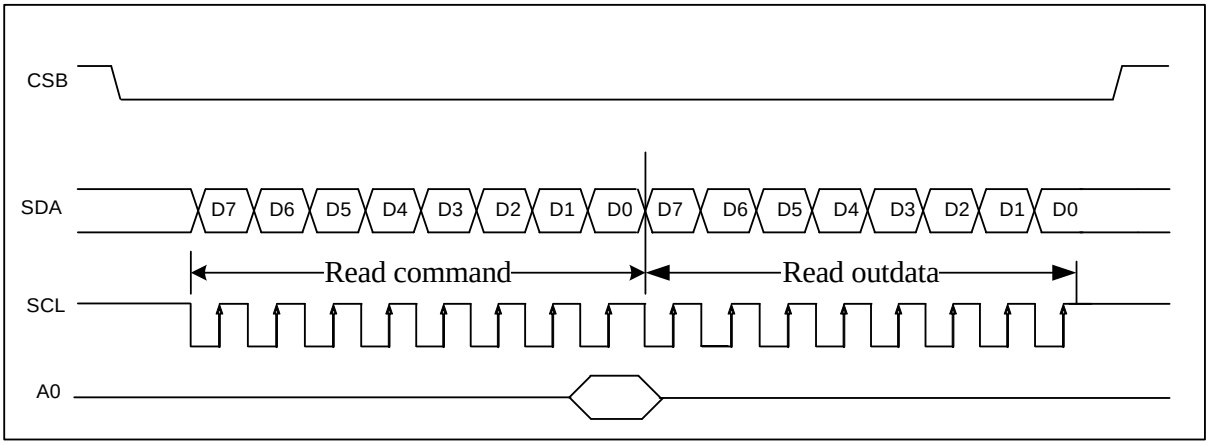
4-Line Serial Interface (IIC="H" PS = "L" C68="L")

When the chip is selected (CSB="L"), the serial data can be shifted in sequentially at the rising edge of SCL and transferred to 8-bit parallel data internally; at the eighth SCL rising edge, A0 will also be sampled to decide these 8-bit data is interpreted as command or display data.

4-Line Serial Interface Timing



Write operation of 4-Line SPI

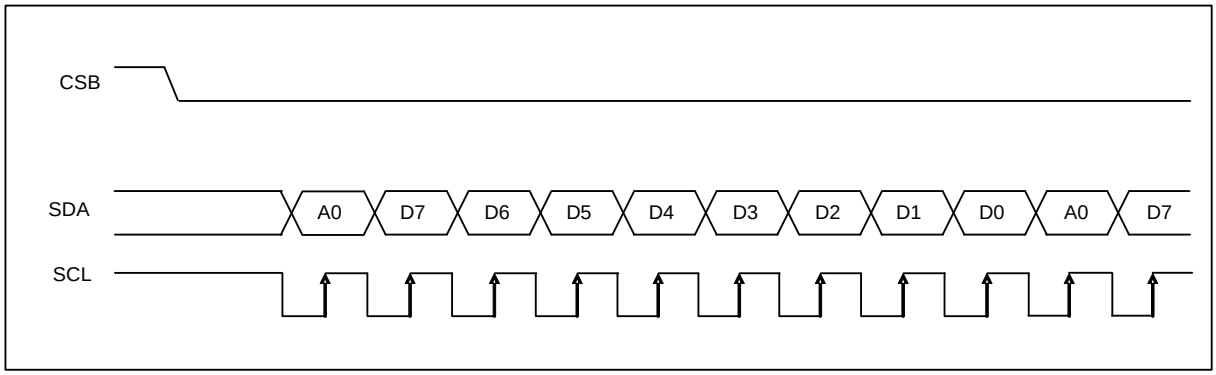


Read operation of 4-Line SPI

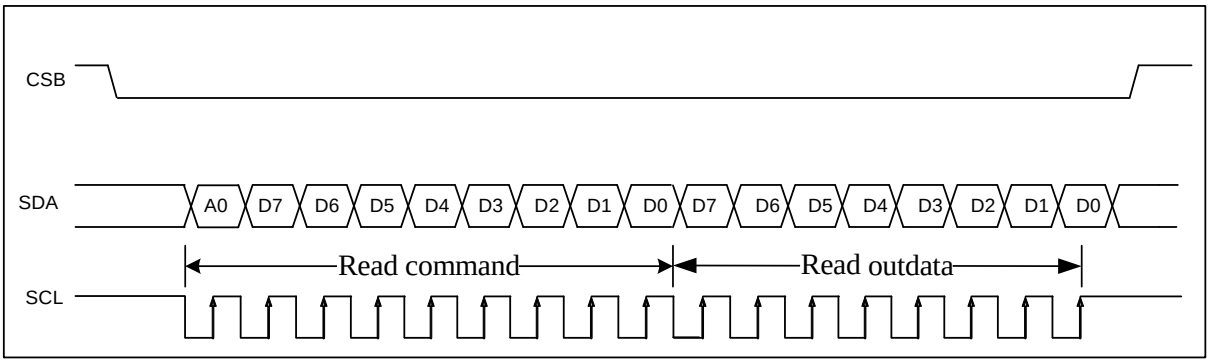
3-Line Serial Interface (IIC="H" PS = "L" C68="H")

In 3-Line interface, A0 signal is not available and the 1st output of SDA will be treated as A0 flag.

3-Line Serial Interface Timing



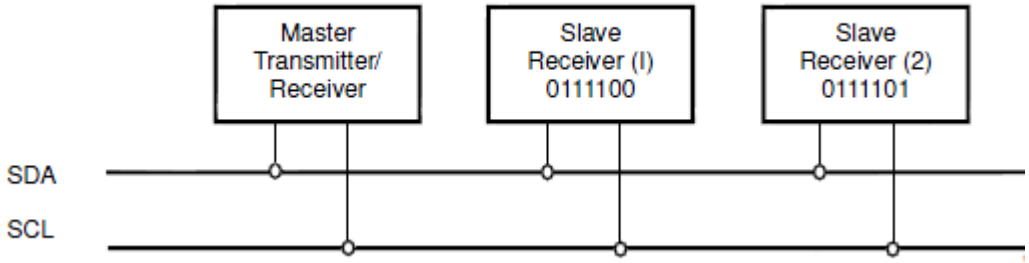
Write operation of 3-Line SPI



Read operation of 3-Line SPI

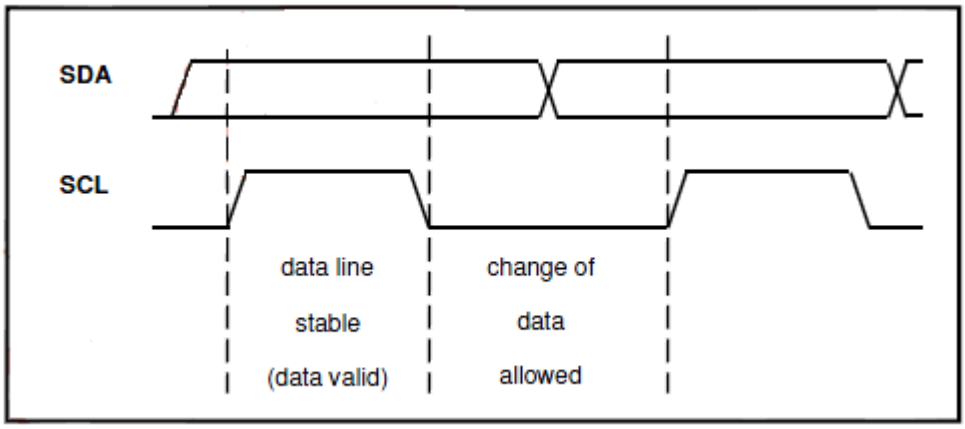
IIC Interface

As 80/68-sreies or 4-line serial interface, The IST3602 also supports standard IIC interface for command & display data communication. The IIC interface is a bi-directional, two-line serial interface, the two lines are a Serial Data line(SDA) and a Serial Clock line(SCL), both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.



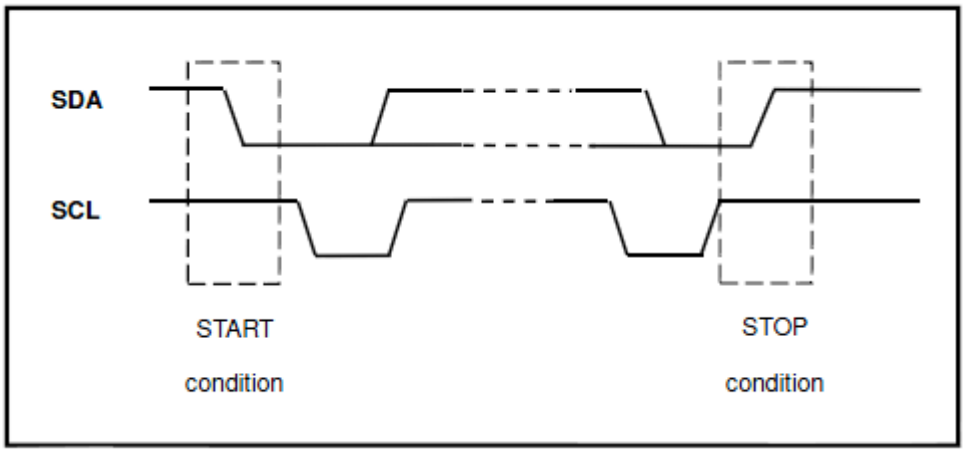
Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, because changes in the data line at this time will be interpreted as a control signal



START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

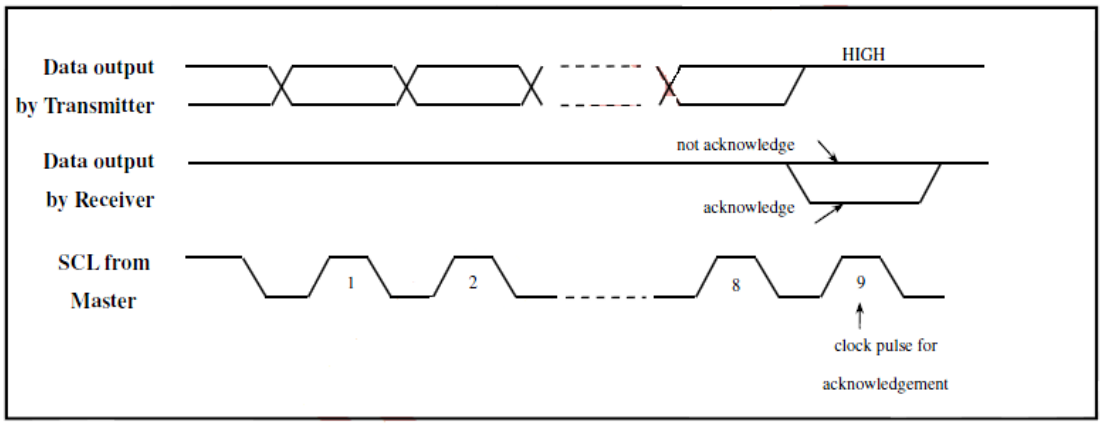


ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter (to release the SDA control and waiting for receiver's ACK), during which time the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an ACK after the reception of each byte. A master receiver must also generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the ACK related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal and end-of-data to the transmitter by not generating an ACK on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



IIC Interface Protocol

The IIC transmitting is initiated with a START condition (S) from the IIC–bus Master and followed by a slave address. Four 7-bit slave address (0111100, 0111101, 0111110, 0111111) are reserved for the IST3602. The least significant bit of the slave address (ID) is configured by C68 and PS pin to decide is the slave address is 0111100 (C68=0/PS=0) or 0111101 (C68=0/PS=1) or 0111110(C68=1/PS=0) or 0111111(C68=1/PS=1). The 8th bit follows the previous 7-bit address is the data direction bit (R/W) -- '0' indicates Master data transmission (WRITE), '1' indicates Master data request (READ).

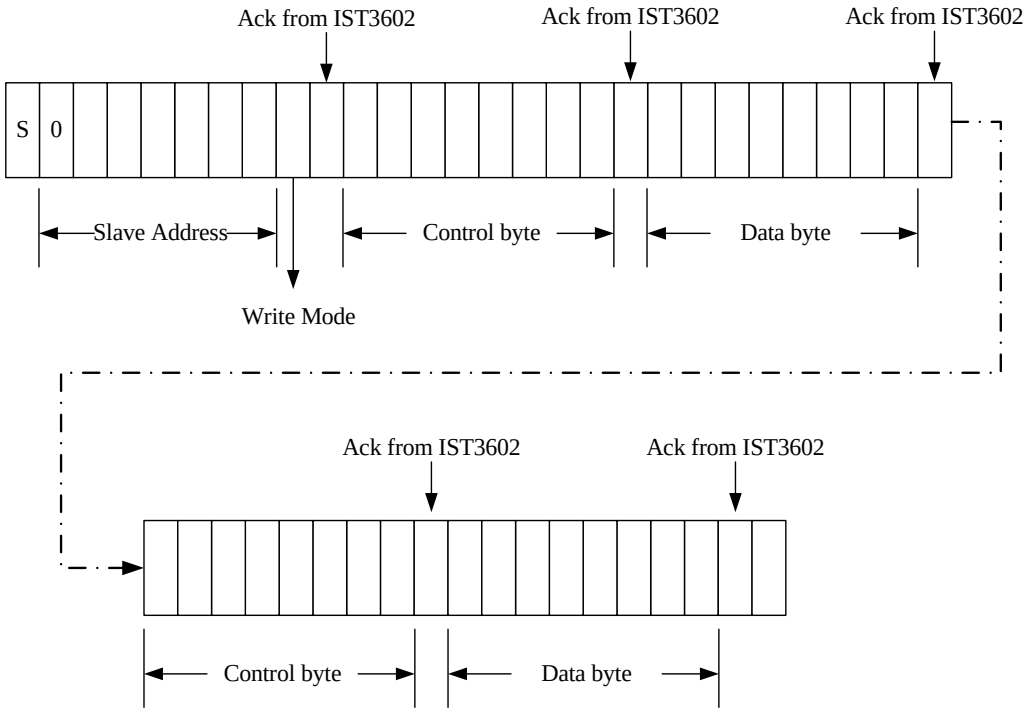
WRITE Mode (Master transmits data to Slave, R/W=0)

Write mode includes Slave address byte, control byte & data byte. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines C0 and A0, and a data byte. The control and data bytes are also acknowledged by all addressed slaves on the bus.

The C0 bit indicates the continuation of the command, please just set C0=1 during the whole Write transmitting period. The A0 bit decides the interpretation of the data byte. If A0 bit is 0, the data byte will be interpreted as command index, if A0 bit is 1, the data byte will be interpreted as command data.

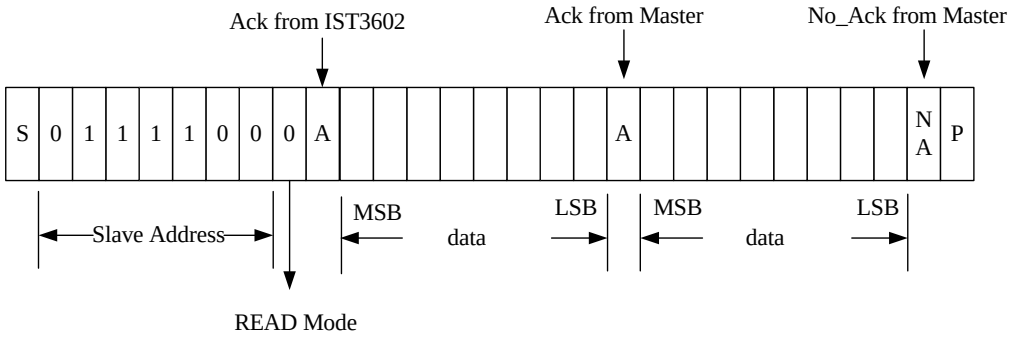
A data transfer is always terminated by a STOP condition (P)generated by the master. However, if master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

WRITE Mode



READ Mode (Master requests data from Slave, R/W=1)

At the moment of the first acknowledge, the Master-transmitter becomes a Master-receiver and the Slave-receiver becomes a Slave transmitter. The first acknowledge is still generated by the slave, but the following data bytes' acknowledge are generated by Master. The STOP and Re-START conditions are generated by Master. If Master wants to stop the data request, after the last data byte has been received, send a Non-Acknowledge condition (keep SDA at HIGH) and trigger a STOP condition.



Busy Flag

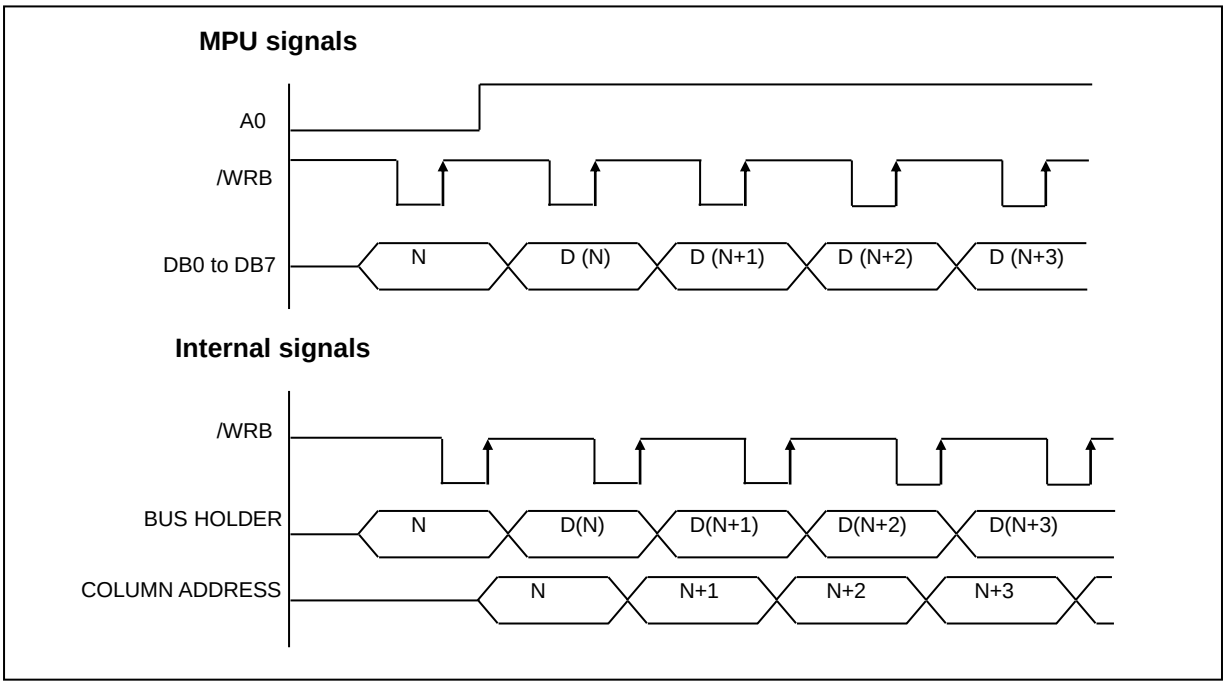
The Busy Flag indicates whether the IST3602 is still during operation or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the write cycle time is correct, the microprocessor needs not to check this flag before each instruction to improve the operation efficiency.

Data Transfer

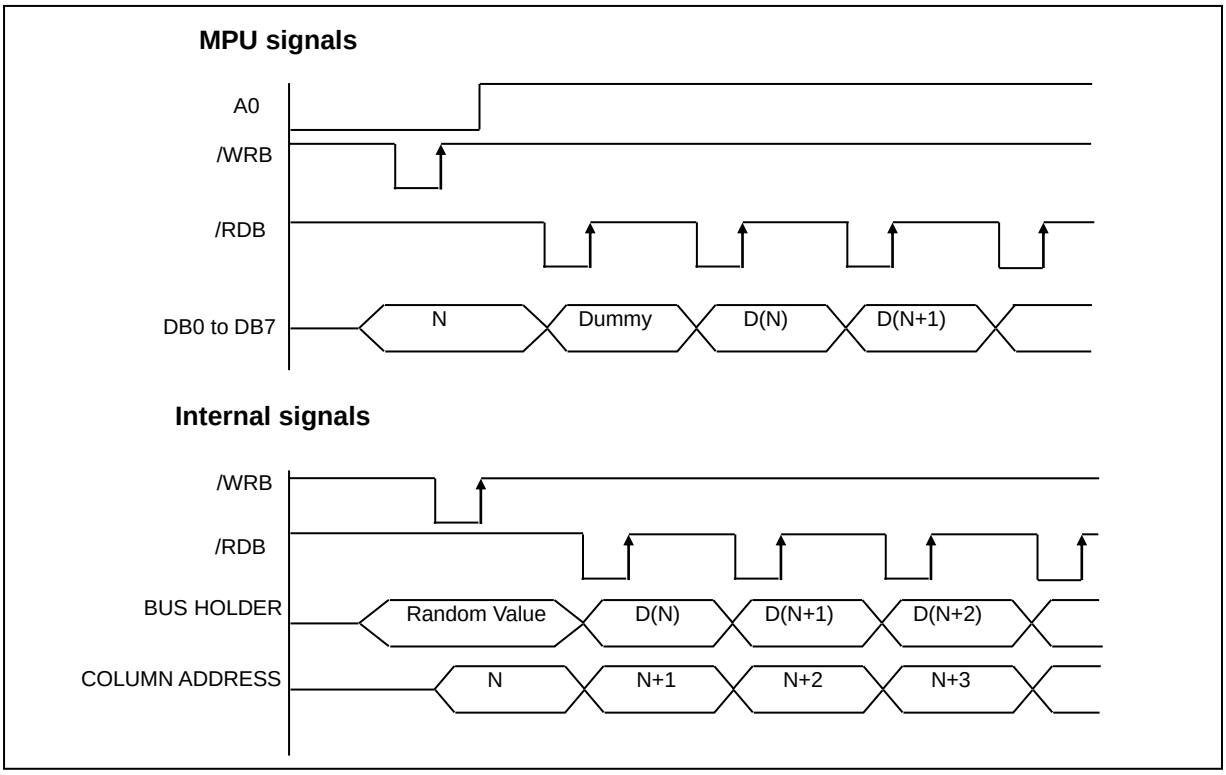
The IST3602 has an I/O bus holder stage to temporary storage the data received from MPU or on-chip RAM data requesting from MPU to read.

When user wants to read out the on-chip RAM data, after setting the address, a “dummy read” cycle must be inserted first to clean out the data stored in the output bus holder, so please just skip this dummy read data and the target RAM data can be read out from the second read cycle.

Write Timing



Read Timing


MPU signals
A0
/WRB
/RDB
DB0 to DB7
N
Dummy
D(N)
D(N+1)
Internal signals
/WRB
/RDB
BUS HOLDER
Random Value
D(N)
D(N+1)
D(N+2)
COLUMN ADDRESS
N
N+1
N+2
N+3

Address Counter(AC)

Address Counter (AC) stores DDRAM/CGRAM/ICON RAM address which is used as pointer. After each access (write/read) to internal RAM (DDRAM/CGRAM/ICON RAM), AC is automatically increased (decreased) by 1. The current AC can be read by command Read AC that descript at Command Table

Display Data RAM (DDRAM)

Display Data RAM (DDRAM) stores display data represented in 8-bit character codes. Each character code has a unique font stored in the Character Generator ROM (CGROM). The capacity of DDRAM is 96 bytes (i.e. 96 characters). IST3602 has 120 SEG outputs, and 24 characters (max.) can be displayed within each line.

The non-displayed area of DDRAM can be used as general data RAM. By using shifting-instruction (Set Entry Mode), the non-displayed area of DDRAM can be displayed. Please refer to the following sections for the relationships between DDRAM address and display position on the LCD module under different display mode. Please note that: In following demonstration, the DDRAM address is hexadecimal format while the character position is decimal format.

1-Line Display Mode

In this mode, one line can use 96 bytes of DDRAM to store the display data. The default mapping between DDRAM address and display position is on the top of Figure 13. The following figure illustrates the mapping on a 16-character LCD module. When the display shift operation is performed, all display contents are shifted and the new relation is shown in

Default DDRAM Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	……	22	23	24				
DDRAM ADDRESS	(Hex)	00	01	02	03	04	……	15	16	17	18	……	5E	5F

Shift Left Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	(Hex)	01	02	03	04	05	…	16	17	18	19	……	5F	00

Shift Right Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	(Hex)	5F	00	01	02	03	…	15	16	17	18	……	5D	5E

Figure DDRAM Address Mapping in 1-Line Display Mode

2-Line Display Mode

In this mode, each line can use 48 bytes of DDRAM to store the display data. The default relation between DDRAM Address and display position is illustrated on the top of Figure The following figure illustrates the mapping on a 2-Line LCD module with 24-character per line. When the display shift operation is performed, all display contents are shifted and the new relation is shown in Figure

Default DDRAM Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	1st line(Hex)	00	01	02	03	04	…	15	16	17	18	…	2E	2F
	2nd line(Hex)	30	31	32	33	34	…	45	46	47	48	…	5E	5F

Shift Left Mapping

		Display Area (Normal)									Hide Area
Display	(Dec)	1	2	3	4	5	…	22	23	24	

DDRAM ADDRESS	1st line(Hex)	01	02	03	04	05	…	16	17	18	19	…	2F	00
	2nd line(Hex)	31	32	33	34	35	…	46	47	48	49	…	5F	30

Shift Right Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	1st line(Hex)	2F	00	01	02	03	…	14	15	16	17	…	2D	2E
	2nd line(Hex)	5F	30	31	32	33	…	44	45	46	47	…	5D	5E

Figure DDRAM Address Mapping in 2-Line Display Mode

3-Line Display Mode

In this mode, each line can use 32 bytes of DDRAM to store the display data. The default relation between DDRAM Address and display position is illustrated on the top of **Figure** The following figure illustrates the mapping on a 3-Line LCD module with 24-character per line. When the display shift operation is performed, all display contents are shifted and the new relation is shown in **Figure**

Default DDRAM Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	1st line(Hex)	00	01	02	03	04	…	15	16	17	18	…	1E	1F
	2nd line(Hex)	20	21	22	23	24	…	35	36	37	38	…	3E	3F
	3RD line(Hex)	40	41	42	43	44	…	55	56	57	58		5E	5F

Shift Left Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	1st line(Hex)	01	02	03	04	05	…	16	17	18	19	…	1F	00
	2nd line(Hex)	21	22	23	24	25	…	36	37	38	39	…	3F	20
	3RD line(Hex)	41	42	43	44	45	…	56	57	58	59		5F	40

Shift Right Mapping

		Display Area (Normal)									Hide Area			
Display	(Dec)	1	2	3	4	5	…	22	23	24				
DDRAM ADDRESS	1st line(Hex)	1F	00	01	02	03	…	14	15	16	17	…	1D	1E
	2nd line(Hex)	3F	20	21	22	23	…	34	35	36	37	…	3D	3E
	3RD line(Hex)	5F	40	41	42	43	…	54	55	56	57		5D	5E

Figure DDRAM Address Mapping in 3-Line Display Mode

4-Line Display Mode

In this mode, each line can use 24 bytes of DDRAM to store the display data. The default relation between DDRAM Address and display position is illustrated on the top of **Figure** The following figure illustrates the mapping on a 4-Line LCD module with 24-character per line. When the display shift operation is set, all display contents are shifted and the new relation is shown in **Figure**

Default DDRAM Mapping

		Display Area (Normal)								
Display	(Dec)	1	2	3	4	5	…	22	23	24
DDRAM ADDRESS	1st line(Hex)	00	01	02	03	04	…	15	16	17
	2nd line(Hex)	18	19	1A	1B	1C	…	2D	2E	2F
	3RD line(Hex)	30	31	32	33	34	…	45	46	47
	4TH line(Hex)	48	49	4A	4B	4C	…	5D	5E	5F

Shift Left Mapping

		Display Area (Normal)								
Display	(Dec)	1	2	3	4	5	…	22	23	24
DDRAM ADDRESS	1st line(Hex)	01	02	03	04	05	…	16	17	00
	2nd line(Hex)	19	1A	1B	1C	1D	…	2E	2F	18
	3RD line(Hex)	31	32	33	34	35	…	46	47	30
	4TH line(Hex)	49	4A	4B	4C	4D	…	5E	5F	48

Shift Right Mapping

		Display Area (Normal)								
Display	(Dec)	1	2	3	4	5	…	22	23	24
DDRAM ADDRESS	1st line(Hex)	17	00	01	02	03	…	14	15	16
	2nd line(Hex)	2F	18	19	1A	1B	…	2C	2D	2E
	3RD line(Hex)	47	30	31	32	33	…	44	45	46
	4TH line(Hex)	5F	48	49	4A	4B	…	5C	5D	5E

Figure DDRAM Address Mapping in 4-Line Display Mode

Character Generator ROM (CGROM)

The Character Generator ROM (CGROM) stores 256 character patterns (5x8-dot) which can be addressed by 8-bit Character Codes. A ROM table illustrates the relationship between Character Codes and the character fonts. Each ROM table has an identical code : ROM Code, so that customer can specify the character fonts according to the ROM Code. Please refer to Appendix for the available ROM table(s) and its ROM code(s). Since the CGROM is a mask-programmed ROM, user-defined ROM table is also supported by changing the content in the mask-programmed ROM.

Note: The first column in the ROM table is also multiplexed with the Character Generator RAM (CGRAM). Up to 8 software-defined character patterns are available for replacing some of the CGROM character patterns (refer to Appendix).

Character Generator RAM (CGRAM)

The Character Generator RAM is used for customers to re-define some character patterns by software. Up to 8 character patterns (5x8 dots per character) can be stored in CGRAM. Each character pattern is consisted of 8 bytes CGRAM data and each byte in CGRAM are 5 bits only. Areas that are not displaying can be used as general data RAM (* only 5-bit per byte).

Creating CGRAM pattern

Before using the character patterns in CGRAM, the required character patterns should be written into CGRAM. Each byte data in CGRAM can be addressed by CGRAM Address: b[5:3] point to a CGRAM pattern; b[2:0] pointer to each CGRAM byte (row of a character pattern). After 8 bytes data of a character pattern is re-written, one CGRAM pattern is finished.

Setting CGRAM Select mode

The first column of ROM table (Character Code: 0x00~0x0F) is multiplexed with the CGRAM. Customer can set OPR[2:1] (by instruction) to control how many(0, 6, 8 or 16) character patterns in CGROM will be replaced by the CGRAM patterns.

Displaying CGRAM pattern

Customer select a Character Code (0x00~0x07 or 0x08~0x0F) and write it into DDRAM. This code will point to 1 of the 8 CGRAM patterns (8 bytes or 5x8 bits), and IST3602 displays the CGRAM pattern, whose address bits "b[5:3]" are specified by the bits "b[2:0]" of the Character Code in DDRAM (refer to the following 2 red blocks below).

DDRAM Address (Instruction)								**CGRAM Address (Instruction)**						CGRAM Address (Instruction)							
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	–	0	0	0	0	0	0	0	0	0	–	–	–	0	1	1	1	0
											0	0	1				1	0	0	0	1
											0	1	0				1	0	0	0	0
											0	1	1				1	0	0	0	0
											1	0	0				1	0	0	0	0
											1	0	1				1	0	0	0	1
											1	1	0				0	1	1	1	0
											1	1	1				0	0	0	0	0
0	0	0	0		0	0	1	0	0	1	0	0	0	–	–	–	0	1	1	1	0
											0	0	1				1	0	0	1	0
											0	1	0				1	0	0	0	0
											0	1	1				1	0	1	1	1
											1	0	0				1	0	0	1	0
											1	0	1				1	0	0	1	0
											1	1	0				0	1	1	1	0
											1	1	1								

Table Relation among CGRAM Address, Character Code (DDRAM Data) & Character Pattern (CGRAM Data)

Notes:

1. The data "1" corresponds to display selection, "0" to non-selection while "-" indicates no effect.
2. Character Code bits b[2:0] point to the CGRAM pattern, whose address bits (b[5:3]) are the same (the red blocks).These 3 bits indicate there are maximum 8 character patterns can be generated by CGRAM.
3. In CGRAM, the row position of a character pattern corresponds to CGRAM data bits 4 to 0 (bit 4 is on the left side).
4. CGRAM address bits b[2:0] point to a byte of the character pattern (row position). The 8th row is the cursor position and its display is formed by a logical OR with the cursor. Try to keep the 8th row data at 0. Otherwise, those pixels with 1 in the 8th row will be turned ON no matter the cursor is ON or OFF.
5. As shown in **Table 4**. character patterns in CGRAM are selected when character code bits 7 to 4 are all 0 (assume CGS1-0 setting are correct). However, since character code bit 3 is not used, the "R" pattern in **Table 4** can be selected by either character code 01H or 09H.
6. Setting CGS1-0 (by instruction) controls how many CGRAM character patterns will be used to replace the CGROM patterns

ICON RAM

ICON RAM Mapping when SHLS=1:

ICON Address	ICON RAM bits							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	-	-	-	ICON1	ICON2	ICON3	ICON4	ICON5
01H	-	-	-	ICON6	ICON7	ICON8	ICON9	ICON10
02H	-	-	-	ICON11	ICON12	ICON13	ICON14	ICON15
03H	-	-	-	ICON16	ICON17	ICON18	ICON19	ICON20
04H	-	-	-	ICON21	ICON22	ICON23	ICON24	ICON25
05H	-	-	-	ICON26	ICON27	ICON28	ICON29	ICON30
06H	-	-	-	ICON31	ICON32	ICON33	ICON34	ICON35
07H	-	-	-	ICON36	ICON37	ICON38	ICON39	ICON40
08H	-	-	-	ICON41	ICON42	ICON43	ICON44	ICON45
09H	-	-	-	ICON46	ICON47	ICON48	ICON49	ICON50
0AH	-	-	-	ICON51	ICON52	ICON53	ICON54	ICON55
0BH	-	-	-	ICON56	ICON57	ICON58	ICON59	ICON60
0CH	-	-	-	ICON61	ICON62	ICON63	ICON64	ICON65
0DH	-	-	-	ICON66	ICON67	ICON68	ICON69	ICON70
0EH	-	-	-	ICON71	ICON72	ICON73	ICON74	ICON75
0FH	-	-	-	ICON76	ICON77	ICON78	ICON79	ICON80
10H	-	-	-	ICON81	ICON82	ICON83	ICON84	ICON85
11H	-	-	-	ICON86	ICON87	ICON88	ICON89	ICON90
12H	-	-	-	ICON91	ICON92	ICON93	ICON94	ICON95
13H	-	-	-	ICON96	ICON97	ICON98	ICON99	ICON100
14H	-	-	-	ICON101	ICON102	ICON103	ICON104	ICON105
15H	-	-	-	ICON106	ICON107	ICON108	ICON109	ICON110
16H	-	-	-	ICON111	ICON112	ICON113	ICON114	ICON115
17H	-	-	-	ICON116	ICON117	ICON118	ICON119	ICON120

Note: SEG0 map with ICON1,
SEG1 map with ICON2,
...,
SEG119 map with ICON120

ICON RAM Mapping when SHLS=0:

ICON Address	ICON RAM bits							
	b7	b6	b5	b4	b3	b2	b1	b0
00H	-	-	-	ICON120	ICON119	ICON118	ICON117	ICON116
01H	-	-	-	ICON115	ICON114	ICON113	ICON112	ICON111
02H	-	-	-	ICON110	ICON109	ICON108	ICON107	ICON106
03H	-	-	-	ICON105	ICON104	ICON103	ICON102	ICON101
04H	-	-	-	ICON100	ICON99	ICON98	ICON97	ICON96
05H	-	-	-	ICON95	ICON94	ICON93	ICON92	ICON91
06H	-	-	-	ICON90	ICON89	ICON88	ICON87	ICON86
07H	-	-	-	ICON85	ICON84	ICON83	ICON82	ICON81
08H	-	-	-	ICON80	ICON79	ICON78	ICON77	ICON76
09H	-	-	-	ICON75	ICON74	ICON73	ICON72	ICON71
0AH	-	-	-	ICON70	ICON69	ICON68	ICON67	ICON66
0BH	-	-	-	ICON65	ICON64	ICON63	ICON62	ICON61
0CH	-	-	-	ICON60	ICON59	ICON58	ICON57	ICON56
0DH	-	-	-	ICON55	ICON54	ICON53	ICON52	ICON51
0EH	-	-	-	ICON50	ICON49	ICON48	ICON47	ICON46
0FH	-	-	-	ICON45	ICON44	ICON43	ICON42	ICON41
10H	-	-	-	ICON40	ICON39	ICON38	ICON37	ICON36
11H	-	-	-	ICON35	ICON34	ICON33	ICON32	ICON31
12H	-	-	-	ICON30	ICON29	ICON28	ICON27	ICON26
13H	-	-	-	ICON25	ICON24	ICON23	ICON22	ICON21
14H	-	-	-	ICON20	ICON19	ICON18	ICON17	ICON16
15H	-	-	-	ICON15	ICON14	ICON13	ICON12	ICON11
16H	-	-	-	ICON10	ICON9	ICON8	ICON7	ICON6
17H	-	-	-	ICON5	ICON4	ICON3	ICON2	ICON1

Table 5 ICON RAM Address and ICON Mapping

Note: SEG0 map with ICON1,
SEG1 map with ICON2,
...,
SEG119 map with ICON120

Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as: DDRAM, CGROM and CGRAM. RAM read timing for display and RAM access timing for MPU are generated separately so that the interfering with each other can be avoided. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in the whole display area.

Cursor and Blink Control Circuit

IST3602 can generate the cursor and blink effects with built-in cursor/blink control circuit. The cursor or blink effect will appear at the current DDRAM display position which is kept in the AC (Address Counter).

INSTRUCTION TABLE

Default Instruction Table
IS[1:0]=Don't Care

No	Instruction	A0	W/R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Instruction Time
1	Display Clear	0	0	0	0	0	0	0	0	0	1	Display clear and set AC to "00H". Set AC to "00H". It will return cursor	1ms
2	AC Return Zero	0	0	0	0	0	0	0	0	1	X	Return to the original position if shifted. The contents in DDRAM are not changed.	20us
3	Set Entry Mode	0	0	0	0	0	0	0	1	I/D	0	Set cursor move direction. The effects are performed after each data access (write or read).	20us
4	Display Control	0	0	0	0	0	0	1	D	C	B	D=1: Entire display on; C=1: Cursor on; B=1: Cursor position blinks.	20us
5	Function Set	0	0	0	0	1	0	0	0	IS1	IS0	DL: Interface data is 8/4 bits; IS[1:0]: select instruction table.	20us
6	Set DDRAM Address	0	0	1	0	0	1	0	0	0	0	Set DDRAM address into AC (address counter).	20us
		0	0	0	AC6	AC5	AC4	AC3	AC2	AC1	AC0		
7	Read Status	0	1	0	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Read the content of AC (address counter)	20us
8	Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/ CGRAM/ ICONRAM)	20us
9	Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/ CGRAM/ ICONRAM)	20us

IS[1:0]=(0,0)

No	Instruction	A0	W/R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Instruction Time
1	Cursor Shift or Display Shift	0	0	0	0	0	1	S/C	R/L	0	0	S/C and R/L: Immediately move cursor or shift display by 1.	20us
2	Set CGRAM Address	0	0	1	0	0	1	0	0	0	1	Set CGRAM address into AC (address counter)	20us
		0	0	0	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address into AC (address counter)	

IS[1:0]=(0,1)

No	Instruction	A0	W/R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Instruction Time
1	Follows Control	0	0	0	0	0	1	0	0	BS1	BS0	BS[1:0]: Bias select	20us
2	Set ICON RAM Address	0	0	0	1	0	AC4	AC3	AC2	AC1	AC0	Set ICON address into AC (address counter).	20us
3	Power Control 1	0	0	0	0	1	1	0	0	0	SLEEP	Enter sleep mode	20us
4	ICON/Power Control2	0	0	0	1	1	0	Icon	Bon	Ron	Fon	Ion: ICON display on/off Bon: Set booster circuit on/off Ron: Set regulator circuit on/off Fon: Set follower circuit on/off.	1ms
5	V0 Control 2	0	0	0	1	1	1	0	0	BT[1:0]		Set booster	20us

IS[1:0]=(1,0)

No	Instruction	A0	W/R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Instruction Time
1	Set Display Mode	0	0	0	0	0	1	DH1	DH0	N2	N1	DH[2:1]:Set n-Line height N[2:1]: Display line number	20us
2	Set Display pattern	0	0	0	1	1	0	0	0	INV	AP	INV: reverse display AP : Pixel all on	20us
3	Select CGRAM & COM/SEG direction	0	0	0	1	0	0	OPR 2	OPR 1	SHLS	SHL C	OPR[2:1]: Set CGRAM mapping SHLS: Set SEG scan direction SHLC: Set COM scan direction	20us

IS[1:0]=(1,1)

No	Instruction	A0	W/R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Instruction Time
1	Power Loss Detection	0	0	0	0	0	1	0	0	0	1	PLD: Set the function of power loss detection	20us
		0	0	0	0	1	0	0	VBO N	0	0		
2	Start line	0	0	1	0	0	0	0	0	1	0	start line setting	20us
		0	0	0	0	ST[5:0]							
3	Contrast	0	0	1	0	0	0	0	0	0	1	CT setting	20us
		0	0	CT[7:0]									
4	Rgain set	0	0	1	0	1	0	RGR[3:0]				Rgain set	20us
5	Soft reset	0	0	1	1	1	0	0	0	1	0	soft reset	20us
6	spi3&spi4 read ram command	0	0	0	0	1	1	0	1	1	1	spi read ram data command	20us
7	spi3&spi4 read status command	0	0	0	0	1	1	0	1	1	0	spi3&spi4&iic read status command	20us

IST Test Mode

No	Instruction	A0	W/R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Instruction Time
1	IST command entry	0	0	1	0	0	0	1	0	0	0	Test command entry	20us
2	Frame rate adjusting enable	0	0	0	0	1	0	FME N	0	0	0	Frame rate adjusting enable	20us
3	Frame rate control(3B)	0	0	1	0	1	1	0	0	1	0	Set frame rate control	20us
				LN7	LN6	LN5	LN4	LN3	LN2	LN1	LN0		
				LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8		
4	OSC clock select	0	0	1	0	0	1	0	0	VCK_SEL [1:0]		DCDC pump clock select	20us
5	OSC Divide Select	0	0	1	0	0	1	1	OSC_DIV[2:0]			Select 1,1/2,1/4,1/8 Oscillator frequency for display operation	20us
6	Exit entry	0	0	1	1	1	0	0	0	1		Exit test entry	`20us

INSTRUCTION DESCRIPTION (IS=0)

Normal Instruction table

Display Clear

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction will clear all DDRAM, CG and ICON RAM. DDRAM will be cleared by writing "20H" (space code) to all DDRAM address. Then set DDRAM address "00H" into AC (address counter). This (AC=00H) will return cursor to the original position, namely, bring the cursor to the left edge on first line of the display. CG and ICON RAM will be cleared by writing “00H” to all CG and ICON RAM address. Besides, this instruction also reset the entry mode to be “increment” (I/D = "1").

AC Return Zero

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

By setting DDRAM address "00H" into AC (address counter), this instruction returns the cursor back to 1ST LINE and 1st column position. This instruction not only returns cursor to its original position but also returns the display to its original setting, if it is shifted. Contents in DDRAM are not changed.

Set Entry Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	0

Set the moving direction of cursor. After each data access, the cursor will be moved or shifted according to I/D-bit.

I/D: Increment / decrement of DDRAM address (cursor/blink) after each byte data access.
I/D = "1", cursor/blink moves to right and DDRAM address is increased by 1.
I/D = "0", cursor/blink moves to left and DDRAM address is decreased by 1.
CGRAM operation is the same as DDRAM. CGRAM address is automatically adjusted according I/D bit after each byte access.

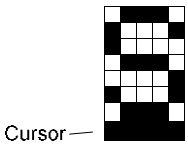
Display Control

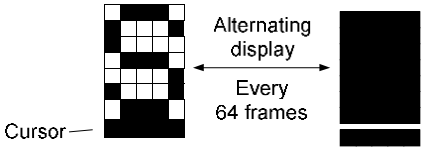
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Set Display and Cursor mode.
D: Display ON/OFF control bit.
D = "1", the display is turned on.
D = "0", the display is turned off, but display data is remained in DDRAM. C: Cursor ON/OFF control bit.

NOTICE: When the display is going to be turned off, to prevent the last COM scan line to be visualized before the LCD power to be fully discharged, please set SLEEP=1 to enter power save mode first, and then set D=0 to turned off the display.

C = "1", cursor is turned on.
C = "0", cursor is disappeared from current display, but I/D register remains its data. B: Cursor Blink ON/OFF control bit.
B = "1", cursor blink is on. The display on the cursor position will alternate between all-black and the character.
B = "0", blink is off.





Function Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	0	IS1	IS0

When IS[1:0]=(0,0): Normal instruction is selected(refer instruction table 0)
When IS[1:0]=(0,1): Extension instruction is selected(refer instruction table 1).
When IS[1:0]=(1,0): Extension instruction is selected(refer instruction table 2).
When IS[1:0]=(1,1): Extension instruction is selected(refer instruction table 3)

Set DDRAM Address

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	0
0	0	0	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction sets DDRAM address into AC. This instruction makes DDRAM data available for MPU access.

N2=0, N1=0: 1-Line display mode, the valid DDRAM address will be:
"00H" to "5FH" (96 bytes).

N2=0, N1=1: 2-Line display mode, the valid DDRAM address will be:
1st Line: "00H" to "2FH" (48 bytes);
2nd Lines: “30H" to "5FH" (48 bytes).

N2=1, N1=0: 3-Line display mode, the valid DDRAM address will be:
1st Line: “00H” to “1FH” (32 bytes);
2nd Line: “20H” to “3FH” (32 bytes);
3rd Line: “40H” to “5FH” (32 bytes).

N2=1, N1=1: 4-Line display mode, the valid DDRAM address will be:
1stLine: “00H” to “17H” (24 bytes);
2ndLine: “18H” to “2FH” (24 bytes);
3rdLine: “30H” to “47H” (24 bytes).
4thLine: “48H” to “5FH” (24 bytes).

Read Status

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	AC6	AC5	AC4	AC3	AC2	AC1	AC0

AC: Address Counter

In parallel interface modes the Address Counter (AC) can be read by MPU on DB6~DB0. The AC stores DDRAM/CGRAM pointer. After each byte access (read/write) with DDRAM/CGRAM, AC is adjusted by 1 automatically (increase or decrease is controlled by the setting of Entry Mode).

Write Data to CGRAM, DDRAM or ICON RAM

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

This operation writes binary 8-bit data to CGRAM, DDRAM or ICON RAM. The selection of RAM (DDRAM, CGRAM or ICON RAM) is controlled by the “Set xxxxx Address” instruction (Set DDRAM Address, Set CGRAM Address and Set ICON RAM Address). RAM set instruction can also determine the AC direction to RAM.
After write operation, the address is adjusted by 1 automatically (increase or decrease depends on the Entry Mode).

Read Data from DDRAM, CGRAM or ICON RAM

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

This operation reads binary 8-bit data from DDRAM, CGRAM or ICON RAM. The selection of RAM (DDRAM, CGRAM or ICON RAM) is controlled by the previous “Set xxxxx Address” instruction. Make sure the selected RAM (DDRAM, CGRAM or ICON RAM) is correct before read data operation.

Note: After writing instruction or Display Data, a Dummy Read is necessary before reading the required data.

Instruction Table 0: IS=00

Cursor or Display Shift

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	0	0	1	S/C	R/L	0	0

This instruction is different from the “Entry Mode Set” instruction. The shift is performed immediately right after receiving this instruction. The data search or data correction in applications can be easily achieved by using cursor shift.

S/C: Selects Cursor or Screen to perform the shift function.
S/C=1: The Screen (current display) is selected to shift. The direct is controlled by R/L bit.
S/C=0: The Cursor is selected to shift. The direction is controlled by R/L bit.
R/L: Selects the shift direction.

R/L=1: The shift direction is toward Right;

R/L=0: The shift direction is toward Left.

NOTICE: When S/C=1, the R/L bit can only be set to 0 (R/L=0). That means the screen shift direct can only toward left.

Cursor Shift

When display line mode is more than 1-Line, the cursor will move to the first position on the next line if AC reaches the last valid address. If the line address is at the last line, the cursor will shift to the first position on the first line.

Screen Shift

The screen shift is performed simultaneously on each line in all kinds o display line mode. Each line is shifted individually. The content kept in AC is not changed when performing Screen Shift operation.

S/C	R/L	Description	AC Value
0	0	Shift cursor left.	AC=AC-1
0	1	Shift cursor right.	AC=AC+1
1	0	Shift Screen (current display) left. Cursor follows the screen to shift left.	AC=AC
1	**1**	**(forbidden)**	----

Set CGRAM Address

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	0	1
0	0	0	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction sets CGRAM address into AC. This instruction makes CGRAM data available for MPU access.

Instruction Table 1:IS=01

Follow Control (IS=10)

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	BS1	BS0

SET Voltage follow Bias:

BS1	BS0	BIAS
0	0	1/4
0	1	1/5
1	0	1/6
1	1	1/7

ICON RAM

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	AC4	AC3	AC2	AC1	AC0

Set icon ram address

Power Save

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	0	SLEEP

SLEEP: Set IST3602 Into power save mode.

NOTICE: When the display is going to be turned off, to prevent the last COM scan line to be visualized before the LCD power to be fully discharged, please set SLEEP=1 to enter power save mode first, and then set D=0 to turned off the display.

ICON/Power Control

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	ION	BON	RON	FON

Setting	I_{ON}	B_{ON}	R_{ON}	F_{ON}
1	ICON display: ON	Built-in Booster: ON	Built -in Regulator: ON	Built -in Follower: ON
0	ICON display: OFF	Built -in Booster: OFF	Built -in Regulator: OFF	Built -in Follower: OFF

V0 Control 2

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	1	0	0	BT[1:0]	

BT: Set booster
00B： Booster will be 5X
01B： Booster will be 6X
10B： Booster will be 7X
11B： Booster will be 8X

Instruction Table 2: IS=10

Set Display Mode

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DH1	DH0	NL1	NL0

DH1-0: Define Display font height (5X8/5X16/5X24/5X32 dot-matrix).
DH1-0=00: Normal character fonts;
DH1-0=01: Double-Height character fonts.
DH1-0=10: Tribe-Height character fonts.
DH1-0=11: Fourth-Height character fonts.

NL1-0: Control the “Display Line Number”.
NL1-0=00: 1-Line Display mode
NL1-0=01: 2-Line Display mode
NL1-0=10: 3-Line Display mode
NL1-0=11: 4-Line Display mode

Duty calculation:

DH1-0	NL1-0	Duty	COM
00	00	1/9	COM0~7+coms
00	01	1/17	COM0~15+coms
00	10	1/25	COM0~23+coms
00	11	1/33	COM0~31+coms
01	00	1/17	COM0~15+coms
01	01	1/33	COM0~31+coms
01	1X	Don’t use	-
10	00	25	COM0~23+coms
10	01/10/11	Don’t use	-
11	00	33	COM0~31+coms
11	01/10/11	Don’t use	-

Set Display pattern

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	0	INV	AP

AP = H: All Pixels On
AP = L: All Pixels on Function not enable.

INV=H: Reverse Display, Font Cell Bit 1 → White, Font Cell Bit 0 → Black
INV=L: Normal Display, Font Cell Bit1 → Black, Font Cell Bit → White,

Select CGRAM & COM/SEG direction

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	CGS1	CGS0	SHLS	SHLC

CGS1, CGS0: Select CGROM size. The CGROM stores 256 characters. The first 16 characters can be replaced by CGRAM data (customized pattern). By setting CGS1 and CGS0, the CGROM pattern will be changed. The used character numbers are shown below:

CGS1	CGS0	Character Code Mapping vs. Available Characters			
		CGRAM	(Characters)	CGROM	(Characters)
1	1	Not Available	(0)	00h~FFh	(256)
1	0	00h~05h	(6)	06h~FFh	(250)
0	1	00h~07h	(8)	08h~FFh	(248)
0	0	00h~07h 08h~0Fh	(8)	10h~FFh	(240)

SHLS: (Pin definition is NOT changed when SHLS=0)
SHLS=1: SEG0~119 ← Column address 0~119 (Normal)
SHLS=0: SEG119~0 ← Column address 119~0 (Invert)

* Pin definition of SEG is NOT changed when SHLS=0

SHLC: (Pin definition is changed when SHLC=0)
SHLC=1: COM0~31 ← Row address 0~31 (Normal)
SHLC=0: COM31~0 ← Row address 31~0 (Invert)

Note:

1.Cursor line will display at 8*N(N=0,1,2,...)Row, When SHLC=0 and ST(start line)=0
2.Cursor line will display at 8*N+7(N=0,1,2,...)Row, When SHLC=1 and IST(start line)=0

Instruction Table 3:IS=11

Power Loss Detection

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	**0**	**0**	**0**	**1**	0	0	0	1
		0	0	1	0	0	VBON	0	0

VBON: This bit is used to set the function of power loss detection is turned ON or OFF.
VBON=1: Enable power loss detection;
VBON=0: Disable power loss detection.

Start Line

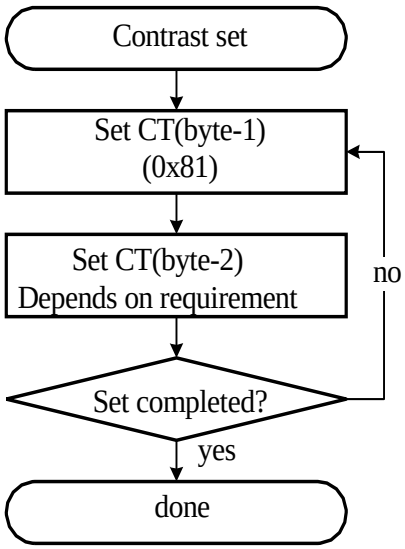
A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	1	0	0	0	0	0	1	0
0	**0**	0	0	ST[5:0]					

ST5-0: Define 1st line Display start at Panel Position

Contrast Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	1	0	0	0	0	0	0	1
0	**0**	CT[7:0]							

CT7-0: Define the V0 Voltage, the Instruction control the electronic volume to adjust a suitable V0 voltage for the LCD, and make the LCD display show figures with perfect performance Contrast.



The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 16 V0 voltage curves can be selected. It is recommended the CT should be close to the center (7FH) for easy contrast adjustment. Please refer to the “Selection of Application Voltage” section for detailed information

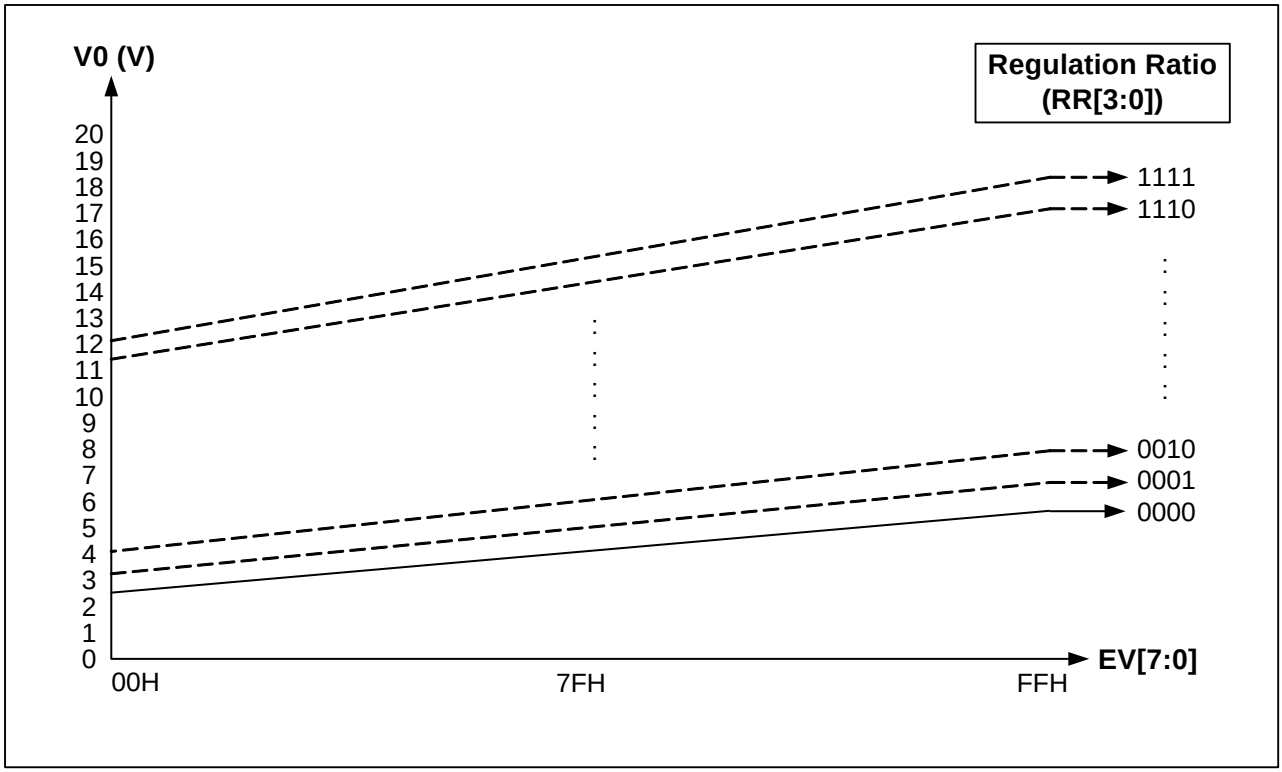
Regulator Set

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	RGR[3:0]			

RGR3	RGR2	RGR1	RGR0	Regulation Ratio (RGR)
0	0	0	0	2.0
0	0	0	1	2.5
0	0	1	0	3.0
0	0	1	1	3.5
0	1	0	0	4.0
0	1	0	1	4.5
0	1	1	0	5.0
0	1	1	1	5.5
1	0	0	0	6.0
1	0	0	1	6.5
1	0	1	0	7.0
1	0	1	1	7.5
1	1	0	0	8.0
1	1	0	1	8.5
1	1	1	0	9.0
1	1	1	1	9.5

The operation voltage (V0) calculation formula is shown below: (RGR comes from Regulation Gain Ratio, CT comes from CT[7:0])
V0 = RGR X [1 – (255 – CT) / 648] X 2.1, or V0 = RGR X [(393 + CT) / 648] X 2.1

SYMBOL	REGISTER	VALUE
RGR	RGR[3:0]	2, 2.5, 3, 3.5 …… and 9.5
CT	CT[7:0]	0 ~ 255



Soft reset

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

SPI3 & SPI4 read ram command

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	1	1	1

SPI3 & SPI4 read status command

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	1	1	0

Instruction Table 4: IST Test Mode

IST command entry:

A0	RW		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0		1	0	0	0	1	0	0	0

Set 88H 4 times to entry IST test command mode

Frame rate adjusting enable

A0	RW		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0		0	0	1	0	FMEN	0	0	0

Frame rate control

Frame rate control command

A0	RW		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0		1	0	1	1	0	0	1	0
0	0		LN7	LN6	LN5	LN4	LN3	LN2	LN1	LN0
0	0		LN15	LN14	LN13	LN12	LN11	LN10	LN9	LN8

The **Frame Control** consists by three commands. The 1st command sets **Frame Control** mode, the 2nd and 3rd command set the Frame frequency DIV number.

LN15~0: DIV number by inside display base clock (F_{dck})

Row frequency = F_{dck} / (LN15~0+1)

Frame frequency = **Row frequency / DUTY (at 25 ^{0}C)**

OSC Clock Select

DCDC pump clock select:

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	0	0	VCK_SEL[1:0]	

VCK_SEL[1:0]	VCK (F_{dck})
00B	Fosc/8
01B	Fosc/4
10B	Fosc/2
11B	Fosc/1

OSC Divide Select

Frame rate control must set OSC_DIV[2:0] firtst, OSC_DIV[2:0] default value is 001B

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	1	1	OSC_DIV[2:0]		

OSC_DIV[2:0]	Base display clock (F_{dck})	
000B	Fosc/2	1.5Mhz
001B	Fosc/4	750Khz
010B	Fosc/8	375Khz
011B~111B	Fosc/16	187Khz

Exit IST test command

A0	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

After set E3h IST test command will return to normal command access mode

IST test command write flow

The suggested IST test command write flow is listed as below:

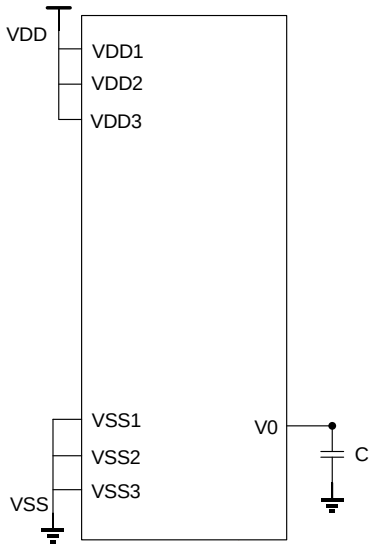
Step	A0	RW	Command	Description
1^{step1}	0	0	88h	■ Enter IST test command
1^{step2}	0	0	88h	■ Enter IST test command
1^{step3}	0	0	88h	■ Enter IST test command
1^{step4}	0	0	88h	■ Enter IST test command
2^{A1}	0	0	28h	■ Frame rate adjusting enable
2^{A2}	0	0	LN	■ Frame Rate Set
2^{A3}	0	0	VCK select SET	■ DCDC pump clock select
2^{A4}	0	0	OSC_DIV	■ OSC_DIV setting
3	0	0	E3h	■ Use NOP command to release IST test command

Power Supply Circuits

The operation voltage (V0) calculation formula is shown below: (RGR comes from Regulation Gain Ratio, CT comes from CT[7:0])
V0 = RGR X [1 – (255 – CT) / 648] X 2.1, or V0 = RGR X [(393 + CT) / 648] X 2.1

SYMBOL	REGISTER	VALUE
RGR	RGR[3:0]	2, 2.5, 3, 3.5 …… and 9.5
CT	CT[7:0]	0 ~ 255

Booster Circuits



Typical values are: C=1uF (the larger, the better display performance),

Power Supply Configurations

Power Configuration	Instruction (VB VR VF)	VB circuits	VR circuits	VF circuits	V0O V0I V0S
Internal power supply circuits are used	(1 1 1)	ON	ON	ON	Open*1
Only the voltage follower circuits are used	(0 1 1)	OFF	ON	ON	External input

<Note>

* 1 V0O, V0I and V0S are short together by ITO. When VB="1", connect external stabilizing capacitors to GROUND.

Voltage Follower Circuits

The Voltage Follower circuits resistively divide the liquid crystal operating voltage (V0) into four voltage levels (V1, V2, V3 and V4) and these voltage levels will be buffered output to serve as the LCD driving power sources.

Bias	V1	V2	V3	V4
1/4*	3/4 x V0*	2/4 x V0*	2/4 x V0*	1/4 x V0*
1/5	4/5 x V0	3/5 x V0	2/5 x V0	1/5 x V0
1/6	5/6 x V0	4/6 x V0	2/6 x V0	1/6 x V0
1/7	6/7 x V0	5/7 x V0	2/7 x V0	1/7 x V0

* Default Value

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD1	-0.3 ~ 4.0	V
Analog Power supply voltage	VDD2, VDD3	-0.3 ~ 4.0	V
LCD Operating Voltage	V0-VSS3	-0.3 ~ 18.0	V
MPU Interface Input Voltage	VIN	-0.3 ~ VDD1+0.3	V
Operating Temperature	TOPR	–40 to +85	℃
Storage Temperature	TSTR	–55 to +150	℃

Notes:

1. Stresses exceed the Absolute Limiting Values listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of V0, VDD2, VSS always match the correct relation: V0 ≥ VDD2/3 >VSS1/2/3 =0V

DC CHARACTERISTICS

V_{SS} (VSS1, VSS2 & VSS3) is 0V unless otherwise specified.

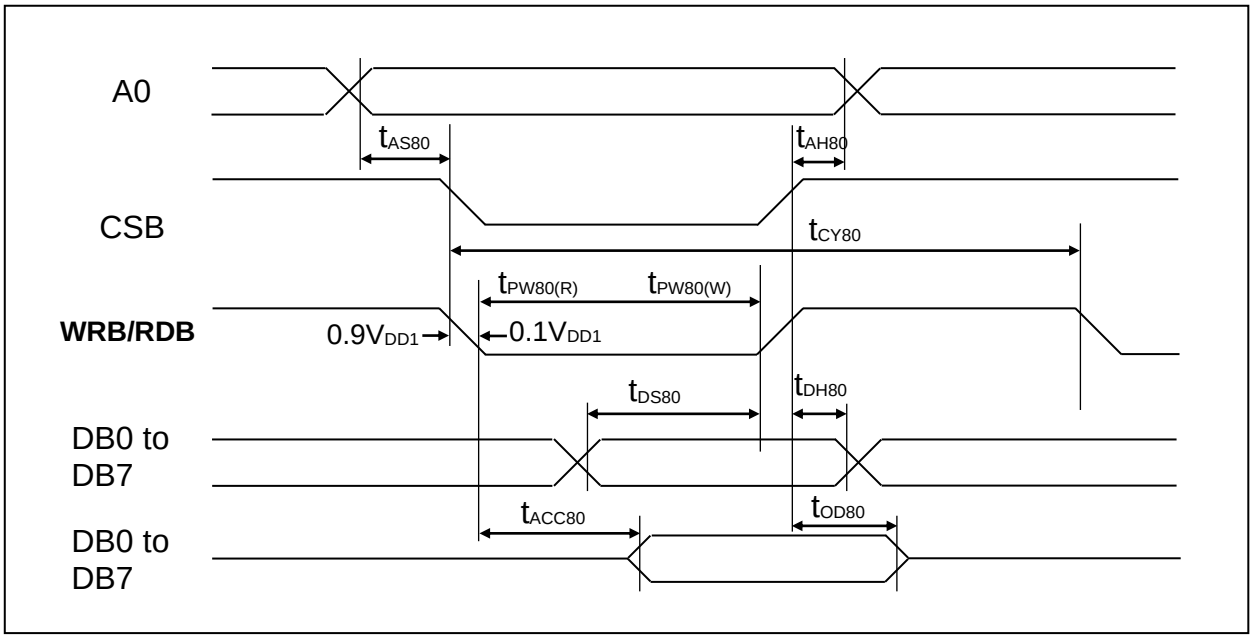
Characteristics	Symbol	Test Condition		Min.	Typ.	Max.	Unit	Pin
Operating Voltage: Digital	VDD1	(Relative to Vss)		1.8	-	3.6	V	VDD1
Operating Voltage: Analog	VDD2,VDD3	(Relative to Vss)		2.4	-	3.6	V	VDD2, VDD3
LCD Voltage	V0			4V	-	18	V	V0-XV0
Input High Voltage	V_{IH}	-		0.8 VDD1	-	VDD1	V	*1
Input Low Voltage	V_{IL}	-		VSS1	-	0.2 VDD1	V	
Output High Voltage	V_{OH1}	VDD1= 1.8~3.6V	I_{OH}:-1mA	0.8 VDD1	-	-	V	DB[7:0]
Output Low Voltage	V_{OL1}		I_{OL}: 1mA	-	-	0.2 VDD1	V	
Input Leakage Current	I_{LEAK}	V_{IN} = 0V ~ VDD1		-1	-	1	uA	*2
LCD Driver ON Resistance	R_{ON}	Ta=25℃ Bias=1/5	V0=6V ΔV=0.6V	-	1.5	-	KΩ	COMn
			VG=2.4V ΔV=0.24 V	-	1.5	-	KΩ	SEGn
Frame frequency	f_{FR}	V_{DD} = 3V, 1/33duty LN15-0=0513H, Ta=25°C		65	70	75	Hz	

The Bare-Chip power consumptions are:

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD}	VDD1=VDD2=VDD3=3.0V V0=8.2V, Bias=1/4 1/17 Display Duty (2-Line Display) Ta=25℃	-	240	-	uA
Sleep Mode	I_{DD}	VDD1=VDD2=VDD3=3.0V	-	3	-	uA

AC CHARATERISTIC

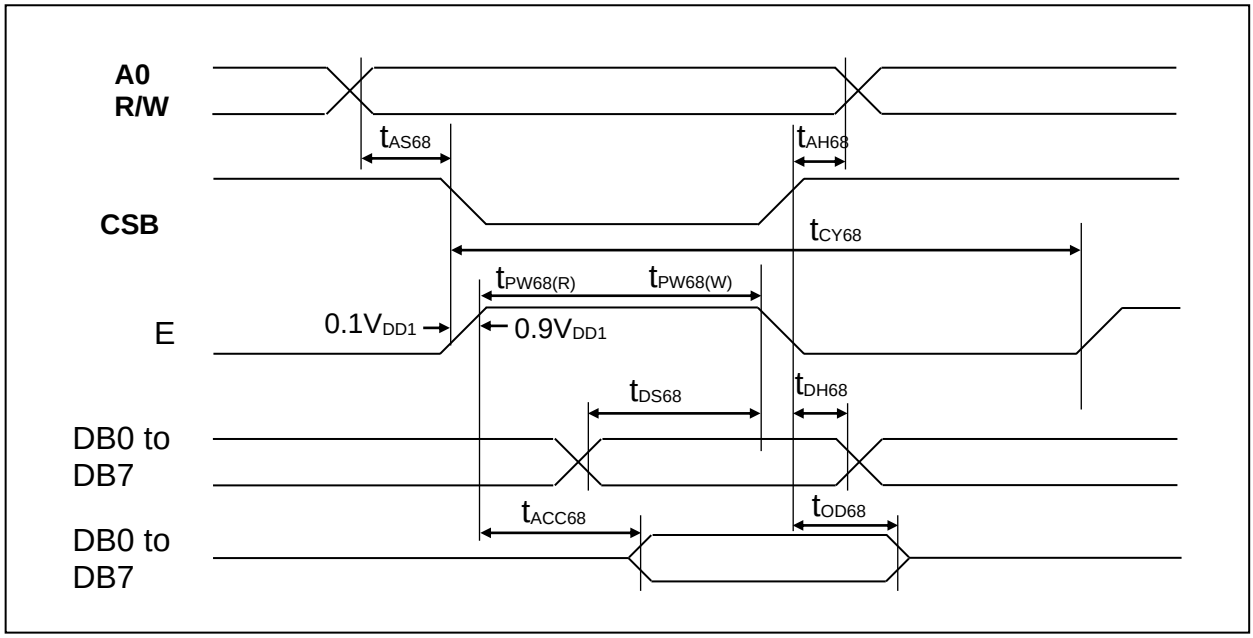
Read / Write Characteristics (8080-series MPU)



(V_{DD1} = 1.8V ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time		t_{CY80}	300	-	-	ns	
Pulse width (WRB)	RW_WRB	t_{PW80}(W)	150	-	-	ns	
Pulse width (RDB)	E_RDB	t_{PW80}(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	60 0	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	140 -	-	- 10	ns	(No load)

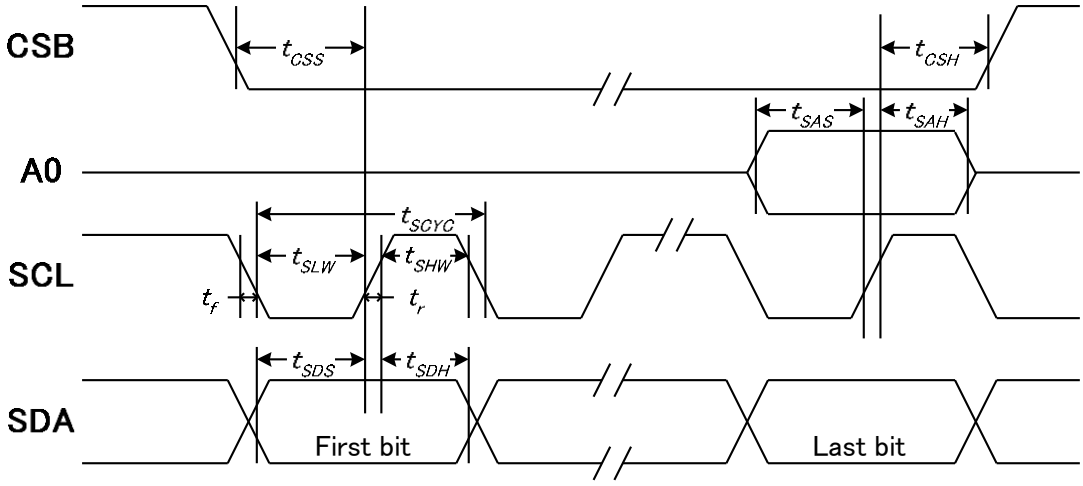
Read / Write Characteristics (6800-series Microprocessor)



(V**DD1** = 1.8V ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	A0	t**AS68** t**AH68**	0 0	-	-	ns	
System cycle time		t**CY68**	300	-	-	ns	
Pulse width (E)	RW_WRB	t**PW68**(W)	150	-	-	ns	
Pulse width (E)	E_RDB	t**PW68**(R)	150	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t**DS68** t**DH68**	60 0	-	-	ns	
Read access time Output disable time		t**ACC68** t**OD68**	140 -	-	- 10	ns	(No load)

Serial 4-Line Interface



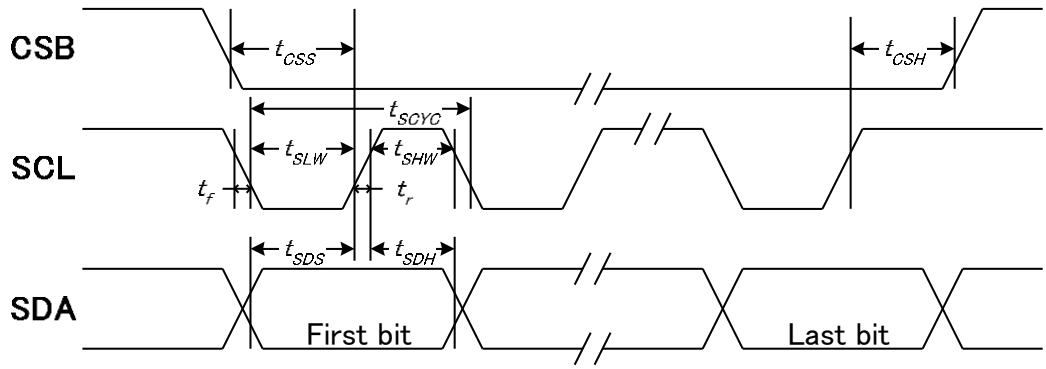
Ta = 25℃

Item	Signal	Symbol	VDD1=2.8V		VDD1=3.3V		Unit
			Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	tSCYC	200	-	200	-	ns
SCL “H” pulse width		tSHW	90	-	90	-	
SCL “L” pulse width		tSLW	90	-	90	-	
Address setup time	A0	tSAS	45	-	45	-	ns
Address hold time		tSAH	45	-	45	-	
Data setup time	SI	tSDS	45	-	45	-	ns
Data hold time		tSDH	45	-	45	-	
Chip select setup time	CSB	tCSS	90	-	90	-	ns
Chip select hold time		tCSH	90	-	90	-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Serial 3-Line Interface



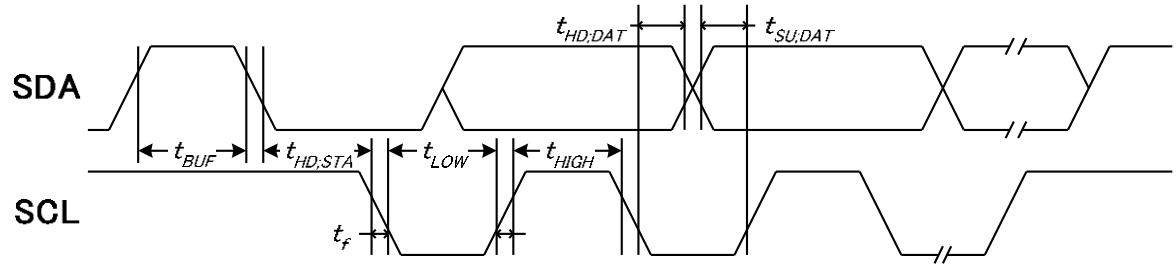
Ta = 25℃

Item	Signal	Symbol	VDD1=1.8V		VDD1=2.8V		VDD1=3.3V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Serial Clock Period	SCL	tSCYC	200	-	200	-	200	-	ns
SCL “H” pulse width		tSHW	90	-	90	-	90	-	
SCL “L” pulse width		tSLW	90	-	90	-	90	-	
Data setup time	SDA	tSDS	45	-	45	-	45	-	ns
Data hold time		tSDH	45	-	45	-	45	-	
Chip select setup time	CSB	tCSS	90	-	90	-	90	-	ns
Chip select hold time		tCSH	90	-	90	-	90	-	

Note:

1. All timing is specified using 20% and 80% of VDD1 as the reference.
2. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Serial I²C Interface

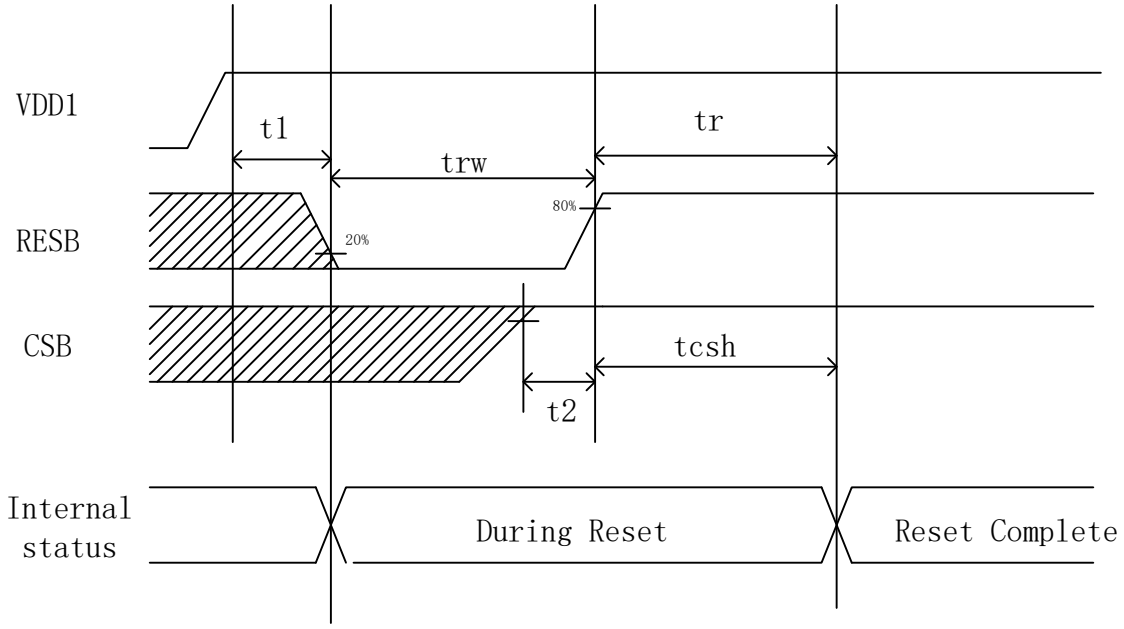


(VDD1 = 1.8 ~ 3.6V, Ta = -30 to +80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
SCL clock frequency		fSCL	0	-	400	kHz	
Set-up time for START condition		tSU/STA	600	-	-	ns	
Hold time for START condition		tHD/STA	600	-	-	ns	
Low period of the SCL clock		tLow	1300	-	-	ns	
High period of the SCL clock		tHIGH	600	-	-	ns	
Data set-up time		tSU/DAT	100	-	-	ns	
Data hold time		tHD/DAT	-	-	900	ns	
Rise time of both SDA and SCL signals		tr	-	-	30	ns	
Fall time of both SDA and SCL signals		tf	-	-	30	ns	
Set-up time for STOP condition		tSU/STO	600	-	-	ns	

Note:
It is recommended to use 4.7KΩ for the pull-up resistors of SCL and SDA. The actual resistance value should be adjusted according to the characteristics of the real system.

Reset Input Timing



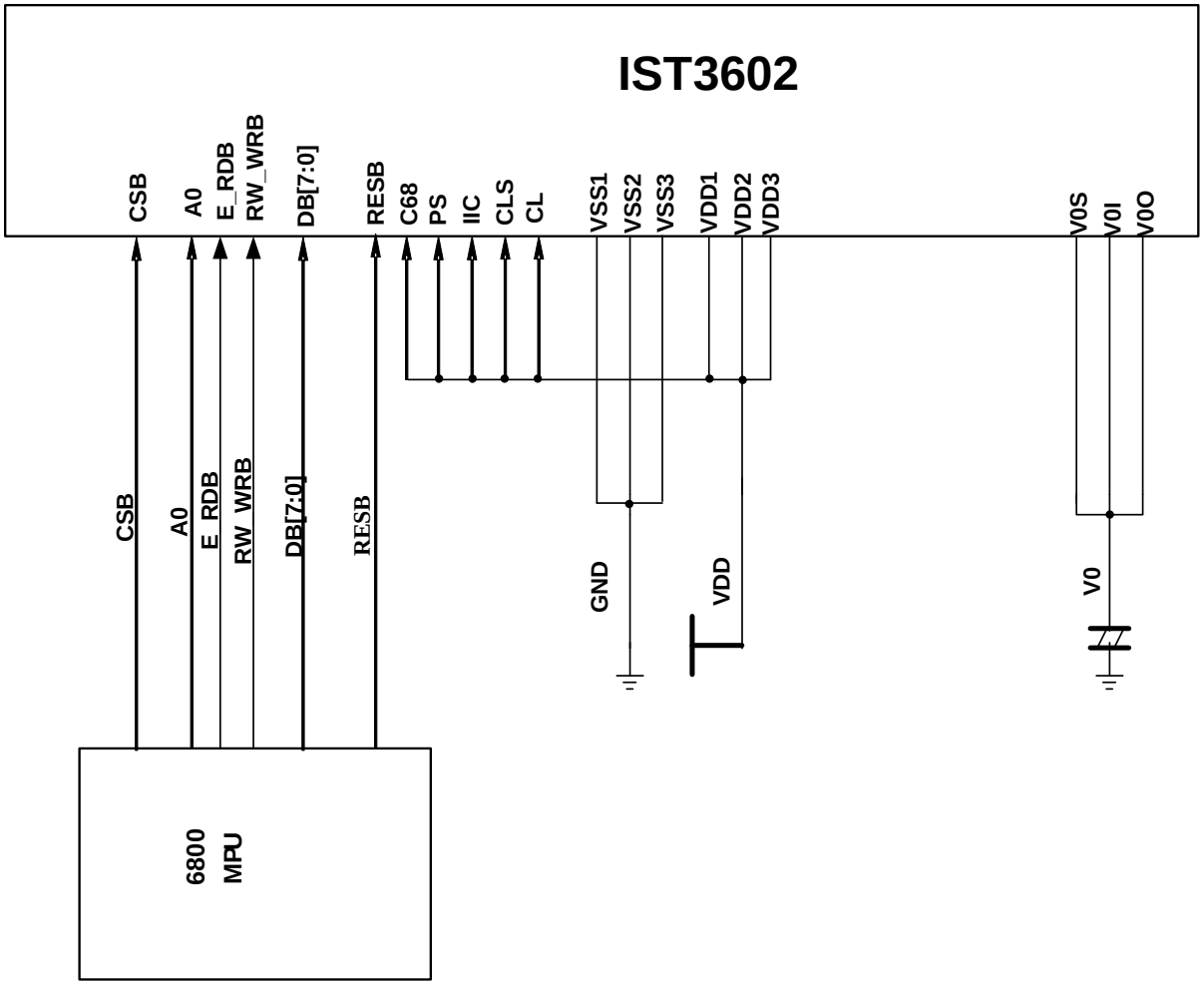
(V**DD1** = 1.8V ~ 3.6V, Ta = -30~80℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RESB	t**RW**	50	-	-	us	
Reset time	-	t**R**	50	-		us	
Reset after VDD stable	RESB	t1	0	-	-	us	
CSB to RESB pull High	CSB	t2	0			us	
CSB hold	CSB	tcsh	50			us	

REFERENCE APPLICATIONS

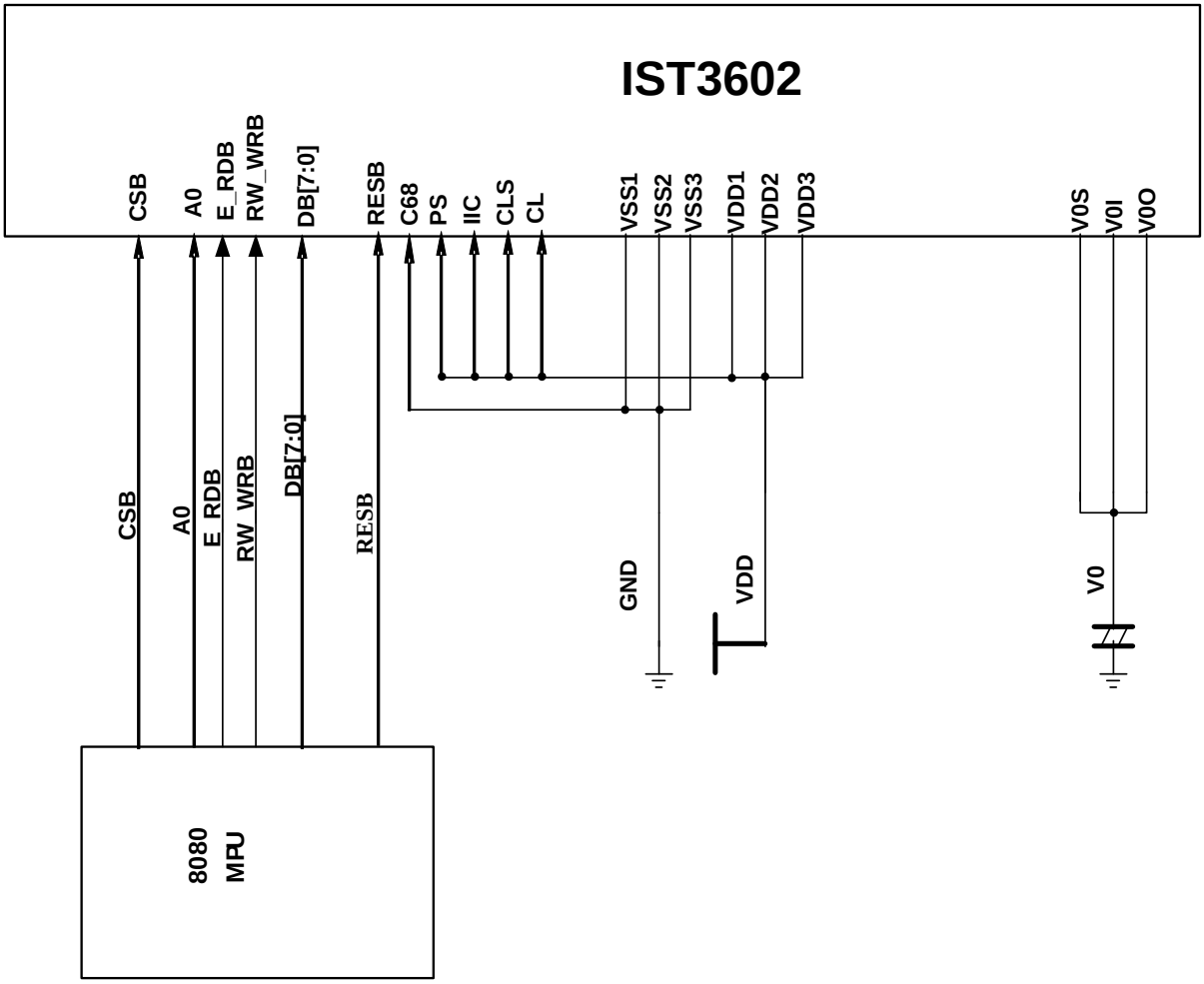
MPU Interface

In Case of Interfacing with 6800-series (PS = “H”, C68 = “H”, IIC=“H”)



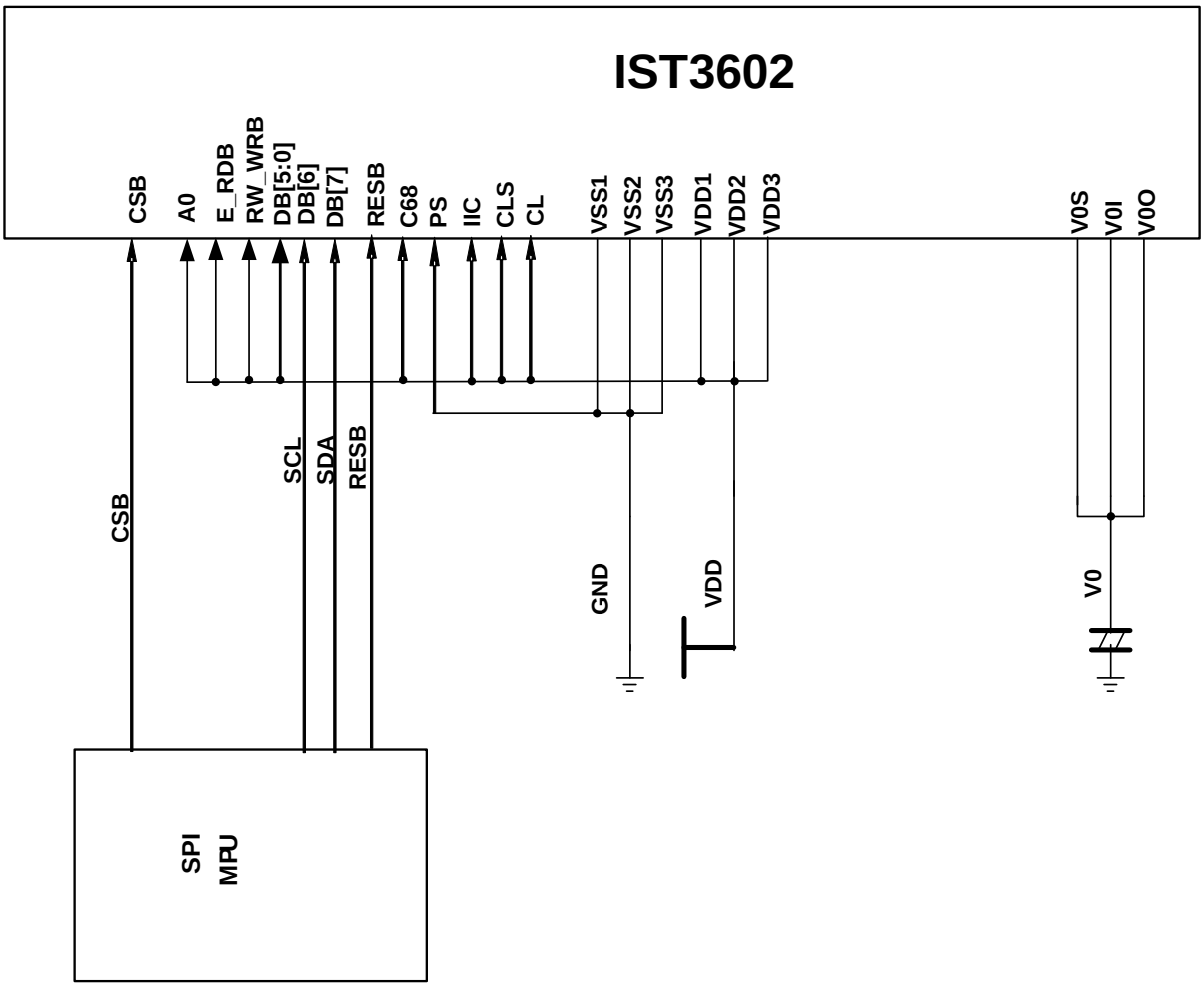
*: No use pin must fix to VSS1 or VDD1.

In Case of Interfacing with 8080-series (PS = "H", C68 = "L", IIC="H")



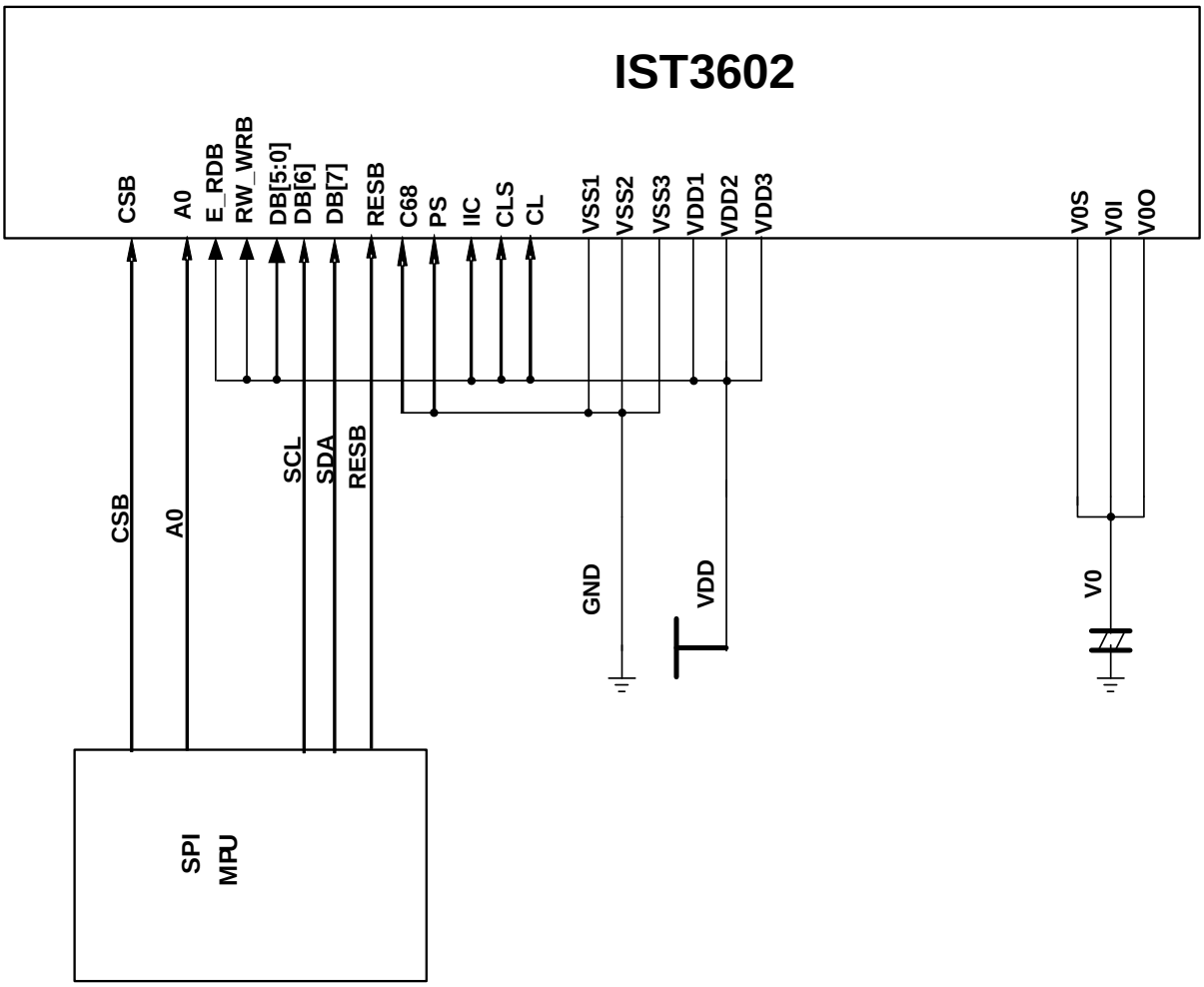
*: No use pin must fix to VSS1 or VDD1.

In Case of Serial Interface 3 (PS = "L", C68="H", IIC="H")



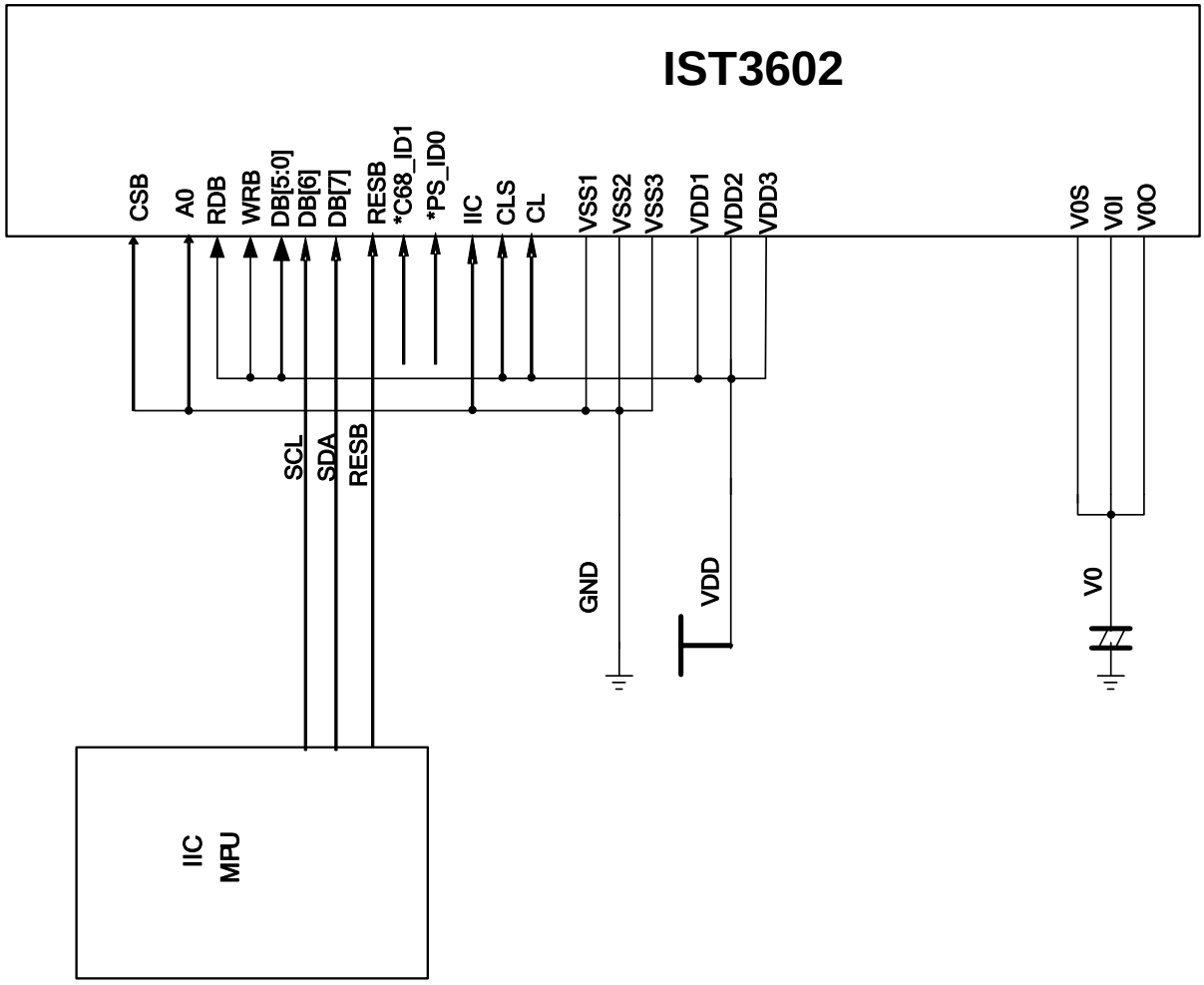
*: No use pin must fix to VSS1 or VDD1.

In Case of Serial Interface 4 (PS = "L", C68="L", IIC="H")



*: No use pin must fix to VSS1 or VDD1.

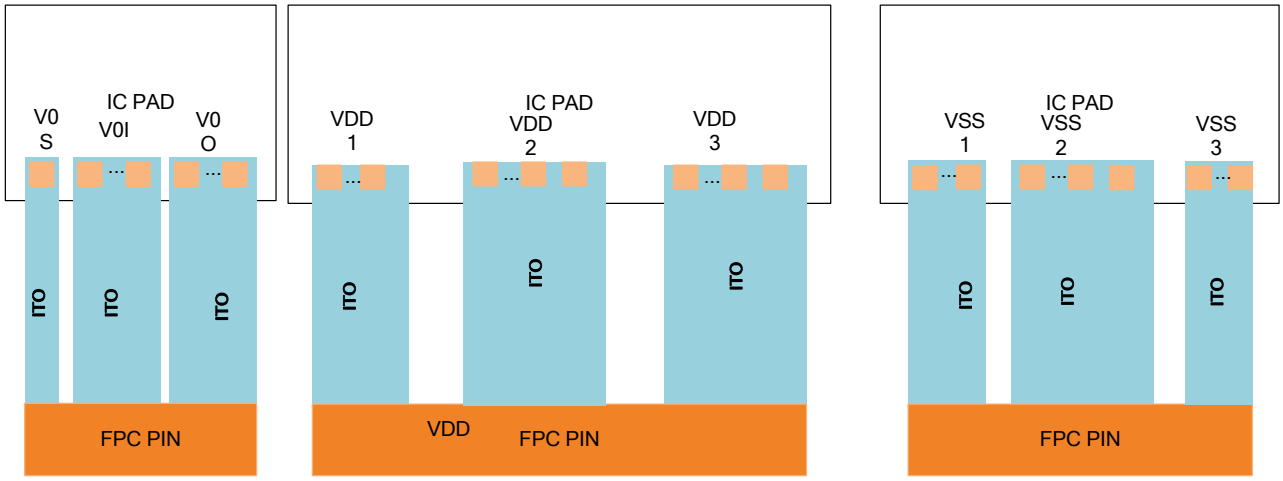
In Case of IIC Interface (IIC = “L”)



*: No use pin must fix to VSS1 or VDD1.

C68_ID1,PS_ID0: define the IIC interface address.

ITO CONNECTION



APPENDIX – ROM CODE AND ROM TABLE

The available character fonts in CGROM are shown below:

ROM Code	Character generator ROM Size	Character Type
1A	256	**English/European/Japanese**

IST3602-1A

CAUTIONS:

1. This Specification will be subjected to modify without notice.

2. Precautions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

2.1Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation .

2.2Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3The IC must be shielded from light in the front, back and side faces.

3. ESD control and prevention:

3.1Humidity Control: 30~70% relative humidity is recommended.

3.2To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed. (Example: Station ionizers).

3.3Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4. Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months