No. : LT-RD-01-LI03-A1

LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT6911C

HDMI1.4/DP++ to Dual-port MIPI DSI/CSI/LVDS with Audio

Datasheet

1. Features

- **HDMI1.4 Receiver**
  - Compliant with the HDMI 1.4 specification with TMDS data rates up to 3.4Gbps per channel
  - Support HDCP 1.4
  - Adaptive receiver equalization for PCB, cable and connector losses
- **Dual-mode DispalyPort Receiver**
  - Compliant with DisplayPort Dual-mode spec 1.1(DP++)with 4K30Hz HDMI support
  - Adaptive receiver equalization to compensate PCB and/or connector losses
  - Integrated 50Ω termination resistors for AC coupled differential inputs
  - Low Intra-pair and Inter-pair skews
  - Support DisplayPort all 4 levels of output
- **Single/Dual-Port MIPI® DSI/CSI Transmitter**
  - Compliant with DCS1.02, D-PHY1.2& DSI1.02 &CSI-2 1.0
  - 1 Clock Lane, and 1~4 Configurable Data Lanes per port
  - 1/2 configurable port
  - 80Mbps~1.5Gbps per data lane
  - Maximum 64pixels overlap for each half
  - Both non-burst and burst video mode supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2,20-bit YCbCr4:2:2,24-bit YCbCr 4:2:2 Video Format
  - Video stream copy mode for each port
  - Side-by-side 3D support
- **Single/Dual-Port LVDS Transmitter**
  - Compatible with VESA and JEIDA standard
  - 1/2 Configurable Port
  - 1 clock lane and 4 configurable data lanes per port
  - Support Maximum Data Rate 1.2Gbps/lane
  - Output Color Depth supports 6-bit and 8-bit
  - Video stream copy mode for each port
  - Side-by-side 3D support
- **Miscellaneous**
  - 3.3V/1.2V Supply Power
  - Internal CSC support conversions between YCbCr 4:4:4 and RGB, and between YCbCr 4:2:2 and YCbCr 4:4:4
  - Support SPDIF and 2-channel IIS audio output
  - Support 100KHz I2C slave
  - Integrated Microprocessor
  - Temperature Range: -40°C ~ +85°C
  - ESD ±2kV HBM

2. General Description

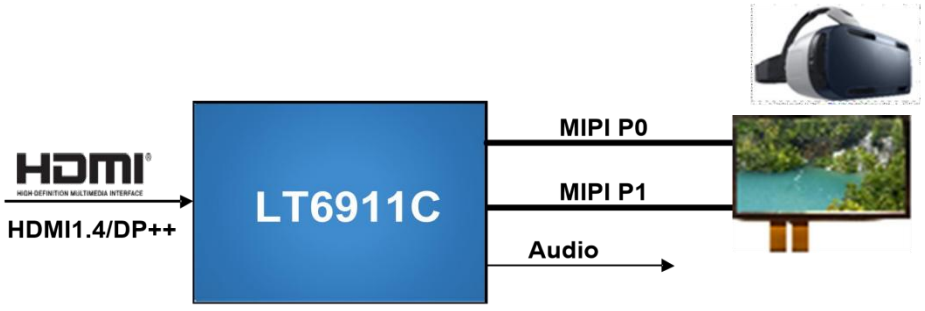
The LT6911C is a high performance HDMI1.4/DP++ to MIPI®DSI/CSI/LVDS chip for VR/Smart phone/Display application.

For MIPI®DSI/CSI output, LT6911C features configurable single-port or dual-port MIPI®DSI/CSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 1.5Gbps/lane, which can support a total bandwidth of up to 12Gbps. LT6911C supports burst mode DSI video data transferring, also supports flexible video data mapping path. For LVDS output, LT6911C can be configured as single-port or dual-port.

For 2D video stream, the same video stream can be mapped to two separated panels, for 3D video format, left side data can be sent to one panel, and right side data can be sent to another panel.

3. Applications

- Mobile system
- Display
- VR



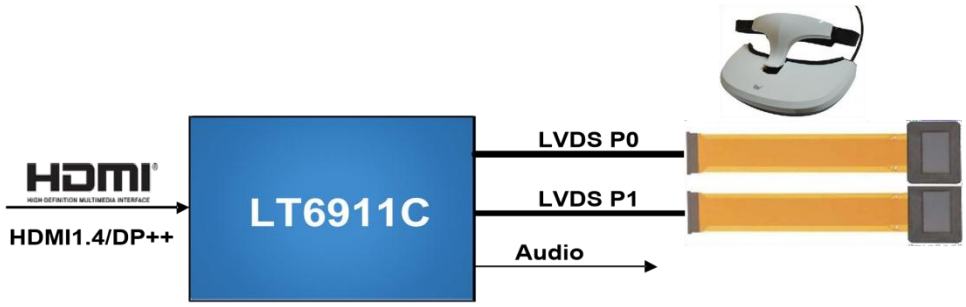


Figure 3.1 Application Diagrams

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method	MPQ
LT6911C	-40℃ to+85℃	QFN64 (7.5*7.5)	Tray	2600pcs

Table of Contents

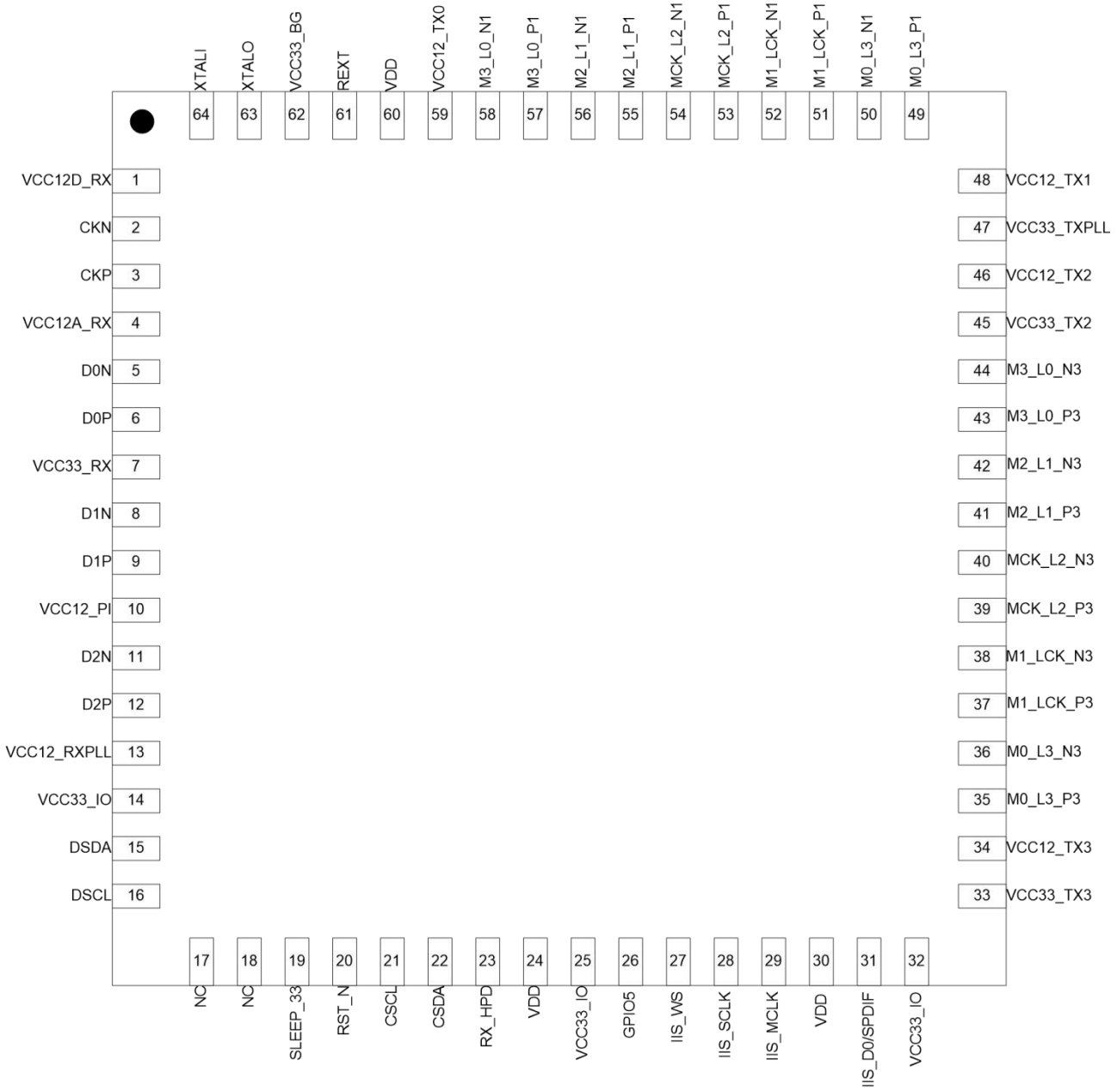
5. Revision History

Version	Owner	Content	Date
R1.0	XF CH	Initial datasheet creation	03/09/2017
R1.1	Terry	Update pin and package information	05/22/2017
R1.2	Terry	Update pin and package information	06/22/2017
R1.3	Terry	Update about feature information	04/27/2018
R1.4	Terry	Update about feature information	05/29/2018
	N W	Update package information	11/14/2018
R1.5	PP J	Update Figure 6.1.1	07/18/2019
R1.6	Terry	Update about power consumption information	11/01/2019
R1.7	Terry	Update about power consumption information	07/07/2020
R1.8	Terry	Add the function of LT6211C and merge into one document	03/30/2021
R1.9	Terry	Add the DC/AC characteristics of LVDS	05/18/2021
R2.0	Terry	Add the DP++ feature information and update Figure 7.1.1	10/12/2022
R2.1	Terry	Update package dimensions	11/11/2022

6. Pinning Information

6.1 Pin Configuration

Figure 6.1.1 LT6911C (QFN64) Pin Assignment (Top View)



6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
65	VSS	PG	N/A	**Ground(EPAD)**
14,25,32	VCC33_IO	PG	N/A	**3.3V IO Power**
62	VCC33_BG	PG	N/A	**3.3V Power for BG**
7	VCC33_RX	PG	N/A	**3.3V Power for RX**
45	VCC33_TX2	PG	N/A	**3.3V Power for MIPI/LVDS TX Port2**
33	VCC33_TX3	PG	N/A	**3.3V Power for MIPI/LVDS TX Port3**
47	VCC33_TXPLL	PG	N/A	**3.3V Power for TXPLL**
24,30,60	VDD	PG	N/A	**1.2V Core Power**
10	VCC12_PI	PG	N/A	**1.2V Power for PI**
13	VCC12_RXPLL	PG	N/A	**1.2V Power for RXPLL**
4	VCC12A_RX	PG	N/A	**1.2V Power for RX Analog Part**
1	VCC12D_RX	PG	N/A	**1.2V Power for RX Digital Part**
59	VCC12_TX0	PG	N/A	**1.2V Power for MIPI/LVDS TX Port0**
48	VCC12_TX1	PG	N/A	**1.2V Power for MIPI/LVDS TX Port1**
46	VCC12_TX2	PG	N/A	**1.2V Power for MIPI/LVDS TX Port2**
34	VCC12_TX3	PG	N/A	**1.2V Power for MIPI/LVDS TX Port3**
11	D2N	Analog	I	**RX Data Channel Lane-2 Negative Input** Maximum data rate is 3.4Gbps.
12	D2P	Analog	I	**RX Data Channel Lane-2 Positive Input** Maximum data rate is 3.4Gbps.
8	D1N	Analog	I	**RX Data Channel Lane-1 Negative Input** Maximum data rate is 3.4Gbps.
9	D1P	Analog	I	**RX Data Channel Lane-1 Positive Input** Maximum data rate is 3.4Gbps.
5	D0N	Analog	I	**RX Data Channel Lane-0 Negative Input** Maximum data rate is 3.4Gbps.
6	D0P	Analog	I	**RX Data Channel Lane-0 Positive Input** Maximum data rate is 3.4Gbps.
2	CKN	Analog	I	**RX Clock Channel Negative Input** Maximum clock rate is 340MHz.
3	CKP	Analog	I	**RX Clock Channel Positive Input** Maximum clock rate is 340MHz.
17	NC	N/A	N/A	**Reserved pin (left floating)**
18	NC	N/A	N/A	**Reserved pin (left floating)**
64	XTALI	LVTTL	I	**XTAI for Debug(27MHz，100ppm)**
63	XTALO	LVTTL	O	**XTAO for Debug**
57	M3_L0_P1	Analog	O	**MIPI TX Port1/Lane3 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Lane0 Channel Positive Output** Maximum data rate is 1.2Gbps.
58	M3_L0_N1	Analog	O	**MIPI TX Port1/Lane3 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Lane0 Channel Negative Output** Maximum data rate is 1.2Gbps.
55	M2_L1_P1	Analog	O	**MIPI TX Port1/Lane2 Channel Positive Output**

Pin#	Pin Name	I/O Type	I/O Dir	Description
				Maximum data rate is 1.5Gbps. **LVDS TX Port1/Lane1 Channel Positive Output** Maximum data rate is 1.2Gbps.
56	M2_L1_N1	Analog	O	**MIPI TX Port1/Lane2 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Lane1 Channel Negative Output** Maximum data rate is 1.2Gbps.
53	MCK_L2_P1	Analog	O	**MIPI TX Port1/Clock Channel Positive Output** Maximum Frequency is 750MHz. **LVDS TX Port1/Lane2 Channel Positive Output** Maximum data rate is 1.2Gbps.
54	MCK_L2_N1	Analog	O	**MIPI TX Port1/Clock Channel Negative Output** Maximum Frequency is 750MHz. **LVDS TX Port1/Lane2 Channel Negative Output** Maximum data rate is 1.2Gbps.
51	M1_LCK_P1	Analog	O	**MIPI TX Port1/Lane1 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Clock Channel Positive Output** Maximum Frequency is 171MHz.
52	M1_LCK_N1	Analog	O	**MIPI TX Port1/Lane1 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Clock Channel Negative Output** Maximum Frequency is 171MHz.
49	M0_L3_P1	Analog	O	**MIPI TX Port1/Lane0 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Lane3 Channel Positive Output** Maximum data rate is 1.2Gbps.
50	M0_L3_N1	Analog	O	**MIPI TX Port1/Lane0 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port1/Lane3 Channel Negative Output** Maximum data rate is 1.2Gbps.
43	M3_L0_P3	Analog	O	**MIPI TX Port3/Lane3 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Lane0 Channel Positive Output** Maximum data rate is 1.2Gbps.
44	M3_L0_N3	Analog	O	**MIPI TX Port3/Lane3 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Lane0 Channel Negative Output** Maximum data rate is 1.2Gbps.
41	M2_L1_P3	Analog	O	**MIPI TX Port3/Lane2 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Lane1 Channel Positive Output** Maximum data rate is 1.2Gbps.
42	M2_L1_N3	Analog	O	**MIPI TX Port3/Lane2 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Lane1 Channel Negative Output** Maximum data rate is 1.2Gbps.
39	MCK_L2_P3	Analog	O	**MIPI TX Port3/Clock Channel Positive Output** Maximum Frequency is 750MHz. **LVDS TX Port3/Lane2 Channel Positive Output** Maximum data rate is 1.2Gbps.
40	MCK_L2_N3	Analog	O	**MIPI TX Port3/Clock Channel Negative Output** Maximum Frequency is 750MHz. **LVDS TX Port3/Lane2 Channel Negative Output** Maximum data rate is 1.2Gbps.

37	M1_LCK_P3	Analog	O	**MIPI TX Port3/Lane1 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Clock Channel Positive Output** Maximum Frequency is 171MHz.

Pin#	Pin Name	I/O Type	I/O Dir	Description
38	M1_LCK_N3	Analog	O	**MIPI TX Port3/Lane1 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Clock Channel Negative Output** Maximum Frequency is 171MHz.
35	M0_L3_P3	Analog	O	**MIPI TX Port3/Lane0 Channel Positive Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Lane3 Channel Positive Output** Maximum data rate is 1.2Gbps.
36	M0_L3_N3	Analog	O	**MIPI TX Port3/Lane0 Channel Negative Output** Maximum data rate is 1.5Gbps. **LVDS TX Port3/Lane3 Channel Negative Output** Maximum data rate is 1.2Gbps.
15	DSDA	LVTTL, OD	I/O	**Slave I2C SDA Signal For EDID**
16	DSCL	LVTTL	I	**Slave I2C SCL Signal For EDID**
23	RX_HPD	OD	O	**HPD Signal of RX**
28	IIS_SCLK	LVTTL	I/O	**SCLK of IIS(GPI)**
31	IIS_D0/SPDIF	LVTTL	I/O	**D0/SPDIF of IIS(GPI)**
26	GPIO5	LVTTL	I/O	**GPIO**
27	IIS_WS	LVTTL	I/O	**WS of IIS(GPI)**
20	RST_N	LVTTL	I	**External Reset Signal (active low)**
29	IIS_MCLK	LVTTL	I/O	**MCLK of IIS(GPI)**
19	SLEEP_33	LVTTL	I	**External Sleep Mode Control Signal**
22	CSDA	LVTTL, OD	I/O	**Slave I2C SDA Signal For Program Register**
21	CSCL	LVTTL	I	**Slave I2C SCL Signal For Program Register**
61	REXT	Analog	O	**External 7.68Kohm Resistor For BG**

7. Function Description

7.1 Function Block Diagram

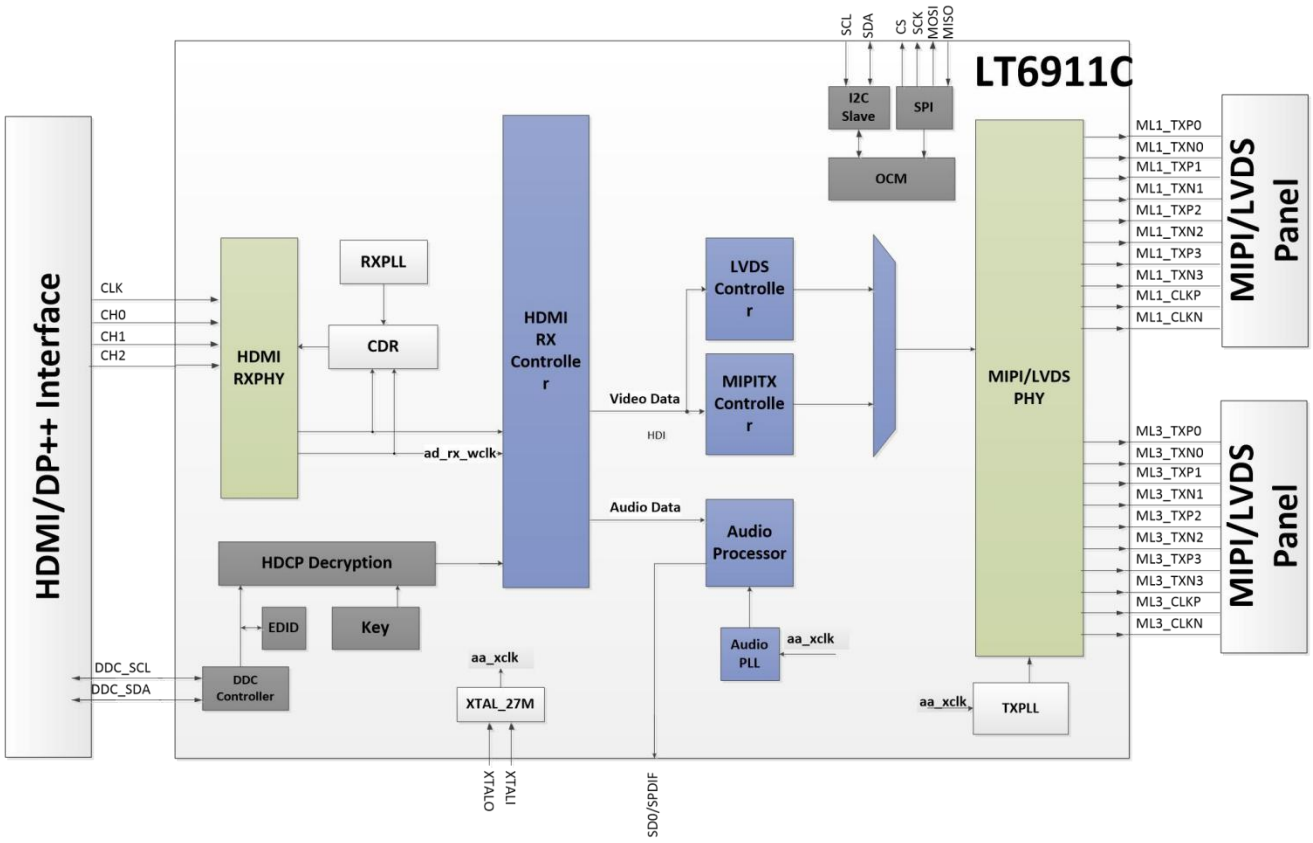


Figure 7.1.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX2,VCC33_TX3,VCC33_BG, VCC33_TXPLL VCC33_RX	3.3V Power Supply Voltage	-0.3		4	V
VDD,VCC12_TX0,VCC12_TX1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VCC12_PI,VCC12_RXPLL	1.2V Power Supply Voltage	-0.3		1.7	V
V_I / V_O	LVTTL Input/Ouput Voltage Range	-0.3		VCC33+ 0.3	V
$V_{I(5V)}$ / $V_{O(5V)}$	5V Tolerant Input/Ouput Voltage Range	-0.3		6	V
T_S	Storage Temperature	-65		150	℃
ESD	HBM Electrostatic Discharge Level	±2000			V
	CDM Electrostatic Discharge Level	±500			V
Note: Permanent device damage may occur if absolute maximum conditions are exceeded.					

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX2,VCC33_TX3,VCC33_BG, VCC33_TXPLL, VCC33_RX	3.3V Power Supply Voltage	3.0	3.3	3.6	V
VDD,VCC12_TX0,VCC12_TX1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VCC12_PI,VCC12_RXPLL	1.2V Power Supply Voltage	1.08		1.32	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃
θ_{JC}	Junction to Case Thermal Resistance		8.8		℃/W

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

TMDS RX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{IDIFF}	Differential input voltage level	150		1200	mV

V_{ICM}	Input common mode voltage	VCC33_RX-700		VCC33_RX-37.5	mV
R_{TERM}	Single-ended termination resistance	45	50	55	Ω
MIPI HS Line TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{CM}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS transmit output high voltage			360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
MIPI LP Line TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Output low-level SE voltage	-50	0	50	mV
V_{OH}	Output high-level SE voltage	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	110			Ω
LVDS Transmitter DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
Voh	Output voltage high			1475	mV
Vol	Output voltage low	925			mV
Vod	Output differential voltage	250		400	mV
Vos	Output offset voltage	1125		1275	mV

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

TMDS RX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_S	Minimum differential sensitivity(peak to peak) after the reference cable equalizer	150			mV
T_{INTRA_SKEW}	Intra-pair skew at sink connector			$0.15T_{bit}+112$	ps
T_{INTER_SKEW}	Inter-pair skew at sink connector			$0.2T_{character}+1.78$	ns
T_{JITTER}	TMDS clock jitter			$0.3T_{bit}$	ps
MIPI HS Line TX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$\Delta V_{CMTX(HF)}$	Common mode Voltage variation above 450MHz			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode Voltage variation between 50-450MHz			25	mV_{PEAK}
t_R and t_F (rise/fall time, 20%-80%)	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps

MIPI LP Line TX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
T_{RLP}/T_{FLP}	Single ended output rise/fall time,15% to 85%, C_L< 70pF			25	ns
T_{REOT}	Single ended output rise/fall time,30% to 85%, C_L< 70pF			35	ns
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	20			ns
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0			500	mV/ns
	Slew rate @ C_{LOAD} = 5pF			350	mV/ns
	Slew rate @ C_{LOAD} = 20pF			250	mV/ns
	Slew rate @ C_{LOAD} = 70pF			150	mV/ns
	Slew rate @ C_{LOAD} = 0 to 70pF(falling edge only)	30			mV/ns
	Slew rate @ C_{LOAD} = 0 to 70pF(rising edge only)	30			mV/ns
	Slew rate @ C_{LOAD} = 0 to 70pF(rising edge only)	30–0.075*($V_{O,INST}$-700)			mV/ns
LVDS Transmitter AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
D-Clock	Clock duty cycle	45		55	%
T_intra_skew	Intra-pair skew			50	ps
T_inter_skew	Inter-pair skew			100	ps
Trise	Vod rise time, 20% to 80%	300		500	ps
Tfall	Vod fall time, 20% to 80%	300		500	ps

8.5 Power Consumption

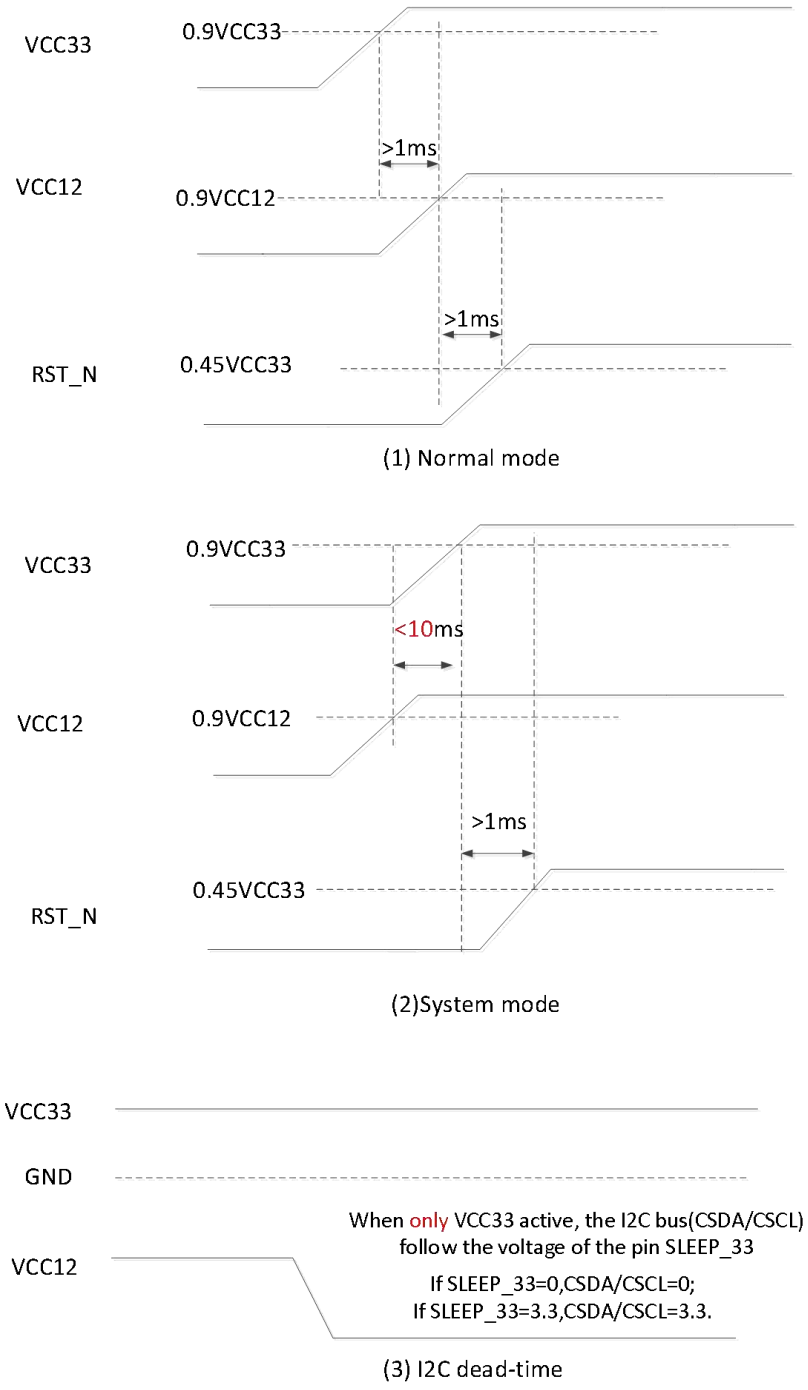
Table 8.5.1 Power Consumption （MIPI Output, Typical）

Condition	Supply Current(3.3V)	Supply Current(1.2V)	Unit
4Kx2K@30Hz	94	460	mA
1080p@60Hz’	56	306	mA
720p@60Hz’	54	223	mA
480p@60Hz’	49	170	mA

Table 8.5.2 Power Consumption （LVDS Output, Typical）

Condition	Supply Current(3.3V)	Supply Current(1.2V)	Unit
4Kx2K@30Hz	149	414	mA
1080p@60Hz’	108	273	mA
720p@60Hz’	81	206	mA

8.6 Power-up and Reset Sequence



Note: In order to avoid the I2C error (3), you can select the second reset sequence(2).

Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

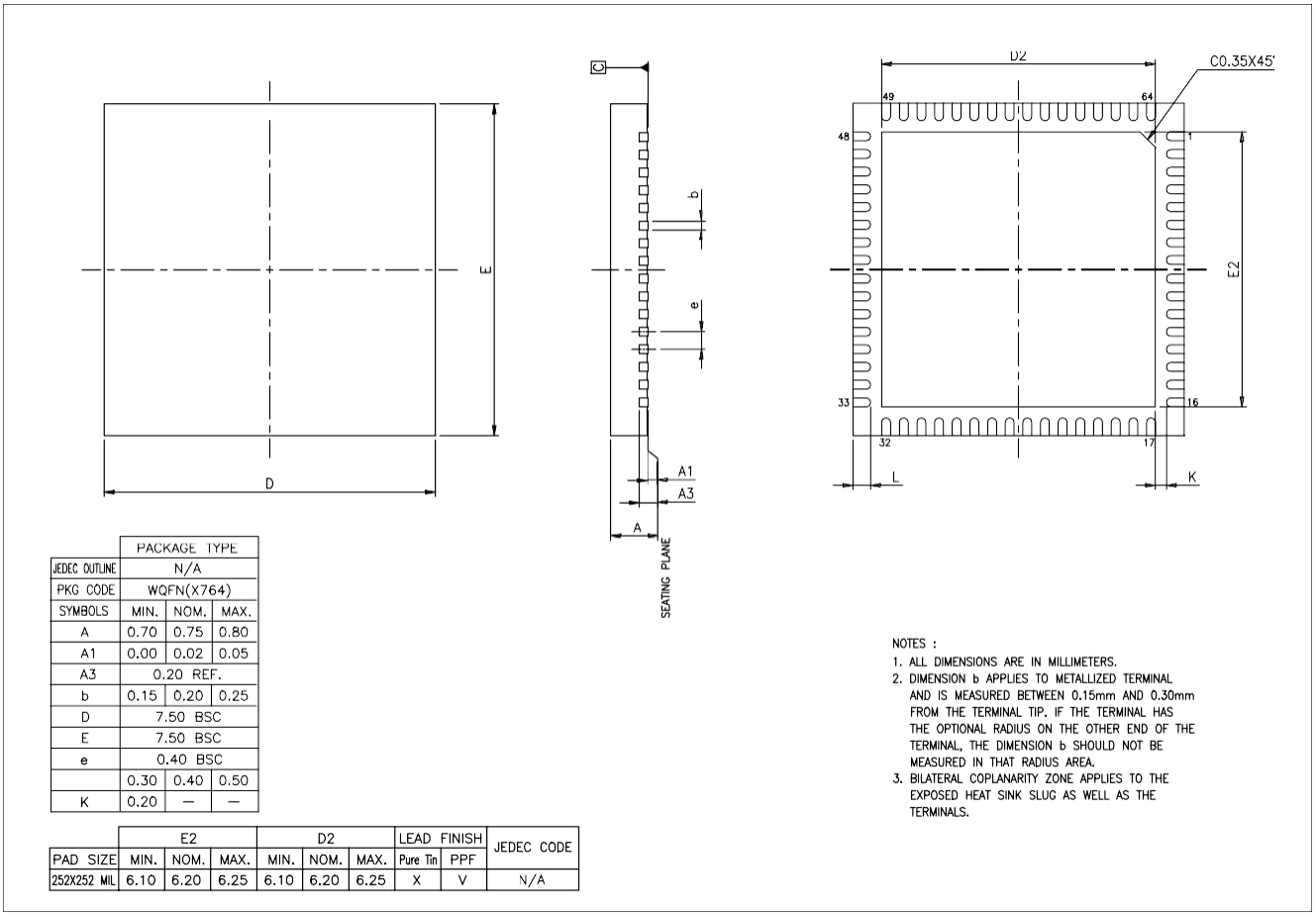
The LT6911C is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.1 Package Dimensions

Figure 9.1.1 is the package dimensions for the date code beginning with GT.
Figure 9.1.2 is the package dimensions for the date code beginning with JC.

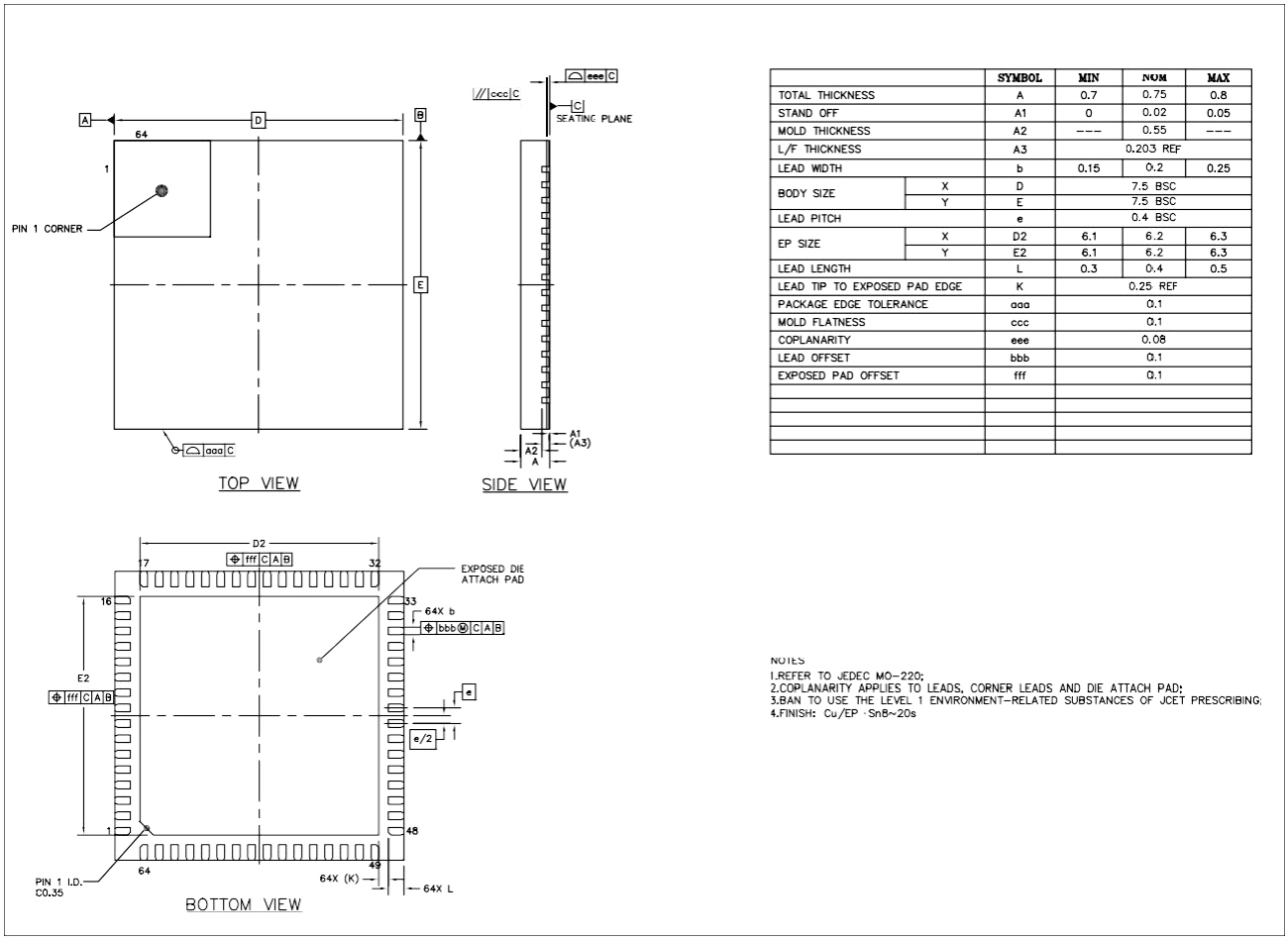


	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
	0.30	0.40	0.50
K	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X252 MIL	6.10	6.20	6.25	6.10	6.20	6.25	X	V	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 9.1.1 Package Dimensions (GT)

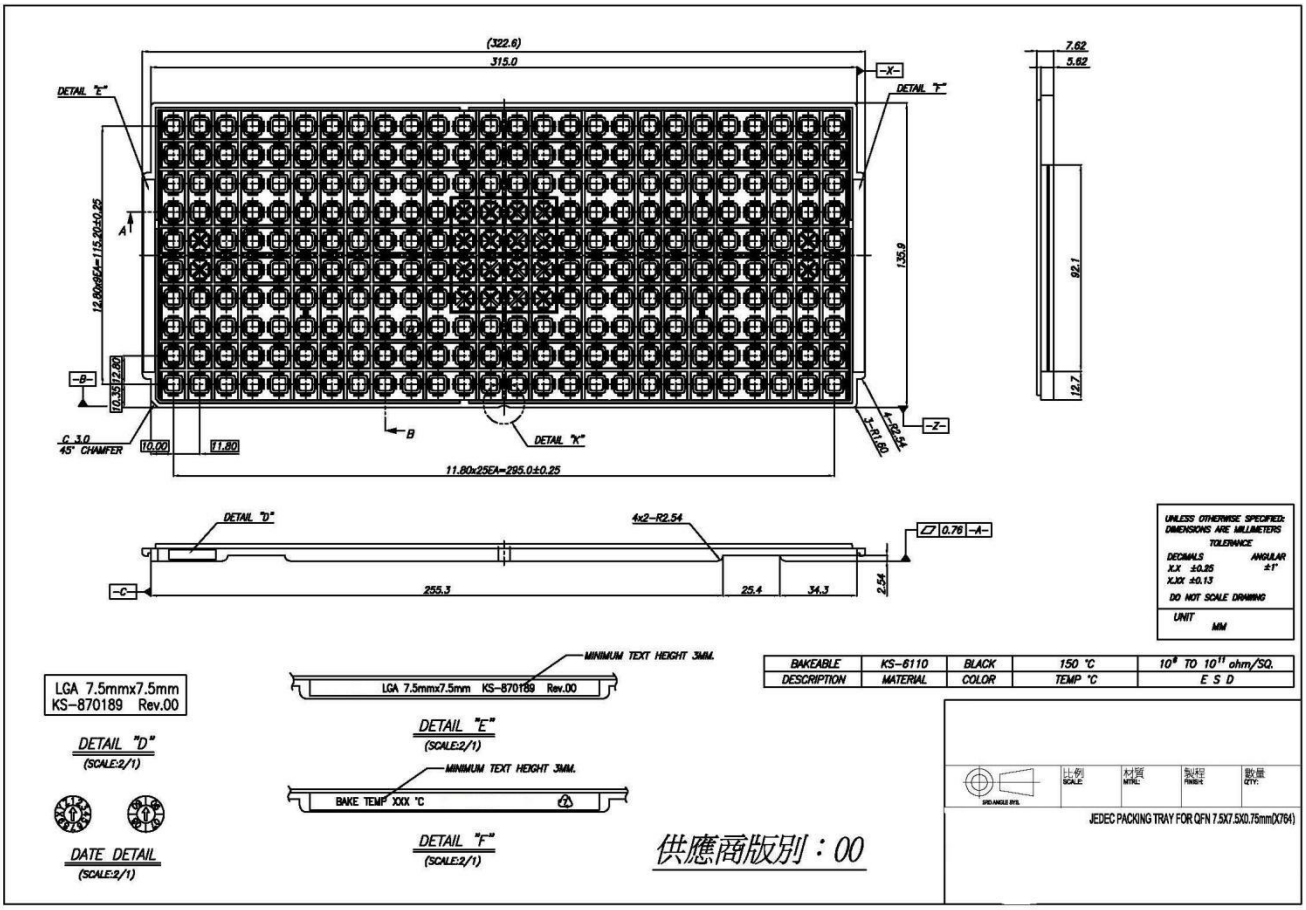


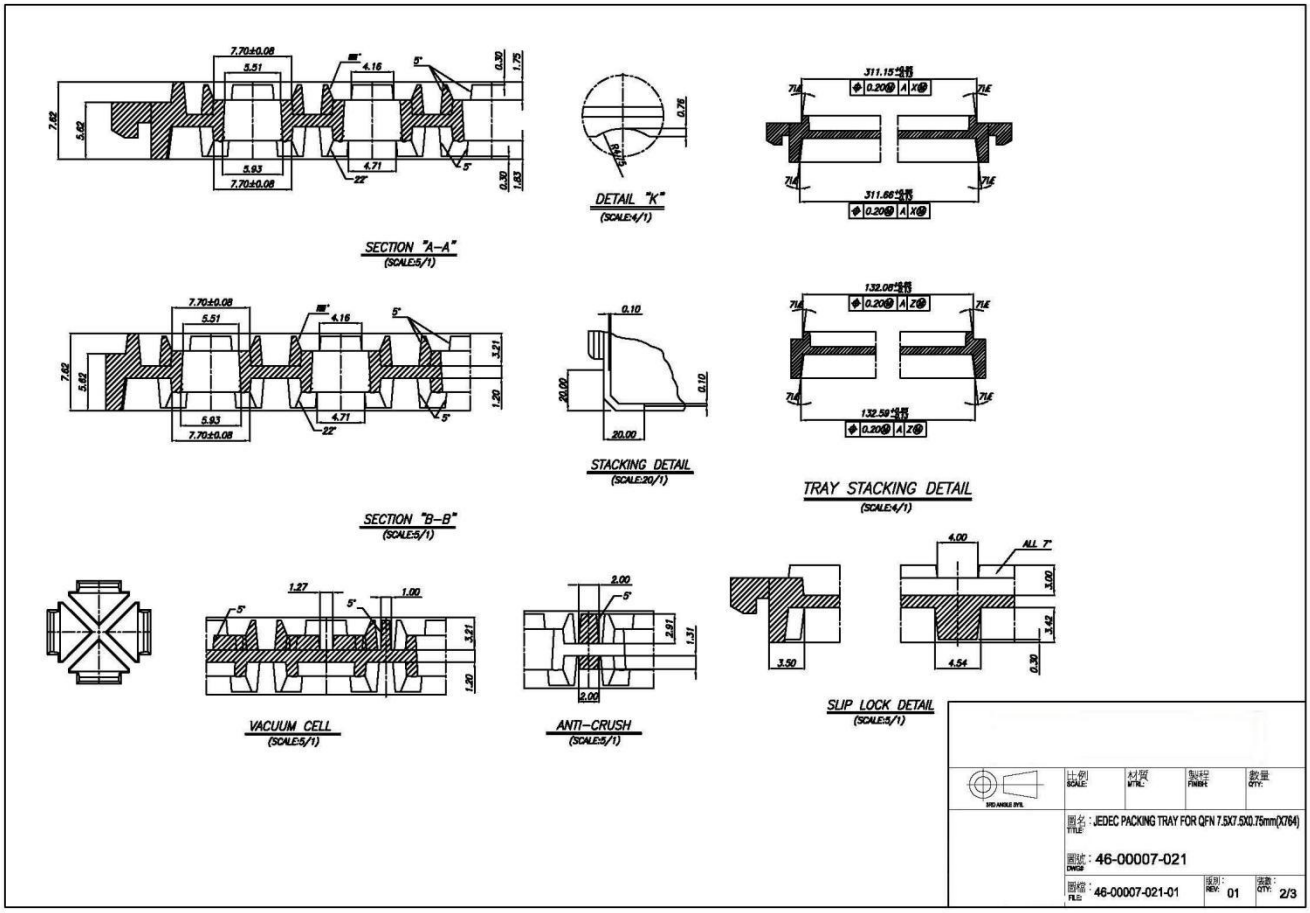
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		7.5 BSC	
	Y	E		7.5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	6.1	6.2	6.3
	Y	E2	6.1	6.2	6.3
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;
4.FINISH: Cu/EP :Sn8~20u

Figure 9.1.2 Package Dimensions (JC)

9.2 Packing Dimensions




SECTION "A–A"
(SCALE:5/1)
DETAIL "K"
(SCALE:4/1)
SECTION "B–B"
(SCALE:5/1)
STACKING DETAIL
(SCALE:20/1)
TRAY STACKING DETAIL
(SCALE:4/1)
VACUUM CELL
(SCALE:5/1)
ANTI–CRUSH
(SCALE:5/1)
SLIP LOCK DETAIL
(SCALE:5/1)
圖名：JEDEC PACKING TRAY FOR QFN 7.5X7.5X0.75mm(X764)
圖號：46-00007-021
46-00007-021-01
01
2/3

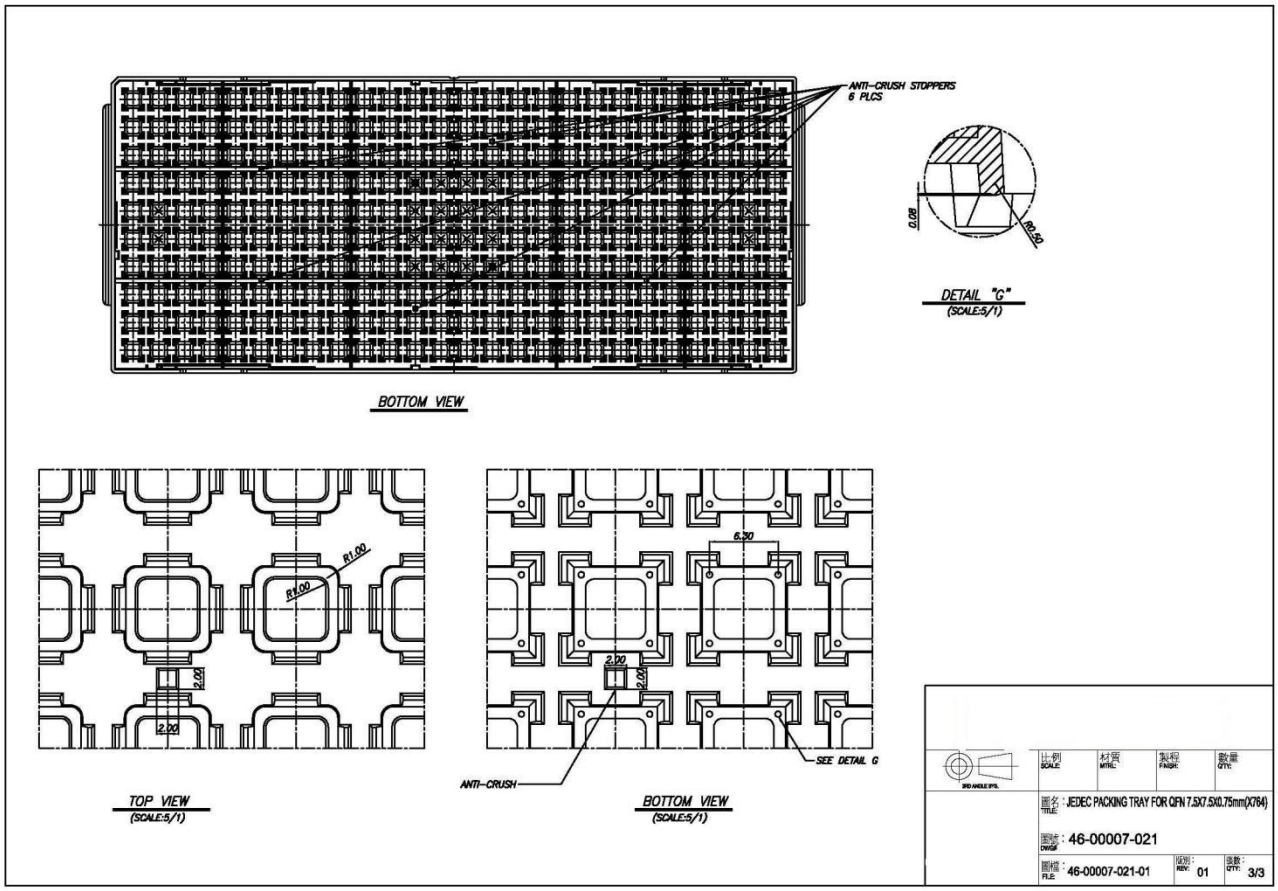


Figure 9.2.1 Packing Dimensions

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