DATA SHEET

NV3051F-L

2400-channel 8-bit Source Driver and GOA/GIP Gate Driver with System-on chip for Color Amorphous TFT-LCDs

Version 0.7
Apr. 2024

Contents

1.Introduction

The NV3051F-L, a 16,777,216-color System-on-Chip (SoC) RAMless driver LSI designed for small and medium size TFT LCD display, is capable of supporting up to 800xRGBx2048 pixels in resolution. The 2400-channel source driver can provide true 8-bit resolution and generate 256 Gamma-corrected values with an internal D/A converter.

The NV3051F-L is able to operate with low IO interface power supply. Incorporating with several charge pumps, the NV3051F-L can generate various voltage levels by an on-chip power management system for gate and source driver.

The built-in timing controller in the NV3051F-L can support several functions to meet a wide variety of requirements about portable display applications. It provides several system interfaces, including MIPI/SPI/LVDS, which can be used to configure the system. Furthermore, it can also achieve high speed display data transmission by using the MIPI video mode.

The NV3051F-L also provides standby mode for power control considerations. For further power control requirements, the dynamic backlight control function, which is based on the image content, is also supported.

2. Features

◎ **One-chip solution for color amorphous TFT-LCD and IGZO-LCD**

◎ **Display Resolution**

- 800 x RGB x (1280, others), (Source output from S1 to S1200, S1201 to S2400)
- 768 x RGB x (1280, others), (Source output from S1 to S1152, S1249 to S2400)
- 750 x RGB x (1334, others), (Source output from S55 to S1152, S1249 to S2400)
- 750 x RGB x (1334, others), (Source output from S1 to S1152, S1249 to S2346)
- 750 x RGB x (1334, others), (Source output from S1 to S1125, S1276 to S2400)
- 720 x RGB x (1280, others), (Source output from S1 to S1080, S1321 to S2400)
- 640 x RGB x (1280, others), (Source output from S1 to S960, S1441 to S2400)
- 600 x RGB x (1280,1024, others), (Source output from S1 to S900, S1501 to S2400)
- 540 x RGB x (1280,960, others), (Source output from S1 to S810, S1591 to S2400)
- 480 x RGB x (1280,960, others), (Source output from S1 to S720, S1681 to S2400)
- 480 x RGB x (1280,960, others), (Source output from S961 to S1200, S1201 to S2400)
- 480 x RGB x (1280,960, others), (Source output from S1 to S900, S1501 to S2040)
- 400 x RGB x (1280,960, others), (Source output from S1201 to S2400)
- 400 x RGB x (1280,960, others), (Source output from S1 to S600, S1801 to S2400)
- 320 x RGB x (1280,960, others), (Source output from S1441 to S2400)

◎ **Display Data Memory: None (RAMless)**

◎ **System Interfaces**

- MIPI DSI (2/3/4 data lane): MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01).
- SPI interface
- LVDS interface

◎ **Display Features**

- Outputs 256γ-corrected values and using an internal true 8-bit resolution D/A converter to achieve 16,777,216 colors

◎ **Display Modes**

- Power saving mode (standby)
- Low power consumption structure for source driver

◎ **On Chip Function**

- Support DC-VCOM driving scheme
- RAMless driver with MIPI video mode
- RAMless driver with LVDS video mode
- Built-in internal oscillator and hardware reset

- On-chip OTP program voltage generator
- Built–in OTP (3 Times) to store ID1~ID3
- Built–in OTP (2 Times) to store gamma curve
- Built–in OTP (1 Time) to store VGMP, VGMN, VCOM calibration
- Built-in 3 power structure modes for application
- Source output voltage level VGMP-AGND: 2.64 ~ 5.846V , VGMN-AGND: -2.509 ~ -5.702V

◎ **Power Supply Range**

- External power IC:

- I/O pads supply voltage (IOVCC): 1.65 ~ 3.6V
- Power supply for MIPI regulator circuit (VDDAM): 1.75 ~ 3.6V
- Analog power supply voltage (VCI): 2.5 ~ 3.6V

- Three-Power Mode:

- I/O pads supply voltage (IOVCC): 1.65 ~ 3.6V
- Power supply for MIPI regulator circuit (VDDAM): 1.75 ~ 6V
- Analog power supply (VSP)：4.5V to 6V
- Analog power supply (VSN)：-4.5V to -6V

Note: 3V≤IOVCC≤3.6V for using LVDS.

3. Block Diagram

3.1 Block Function:

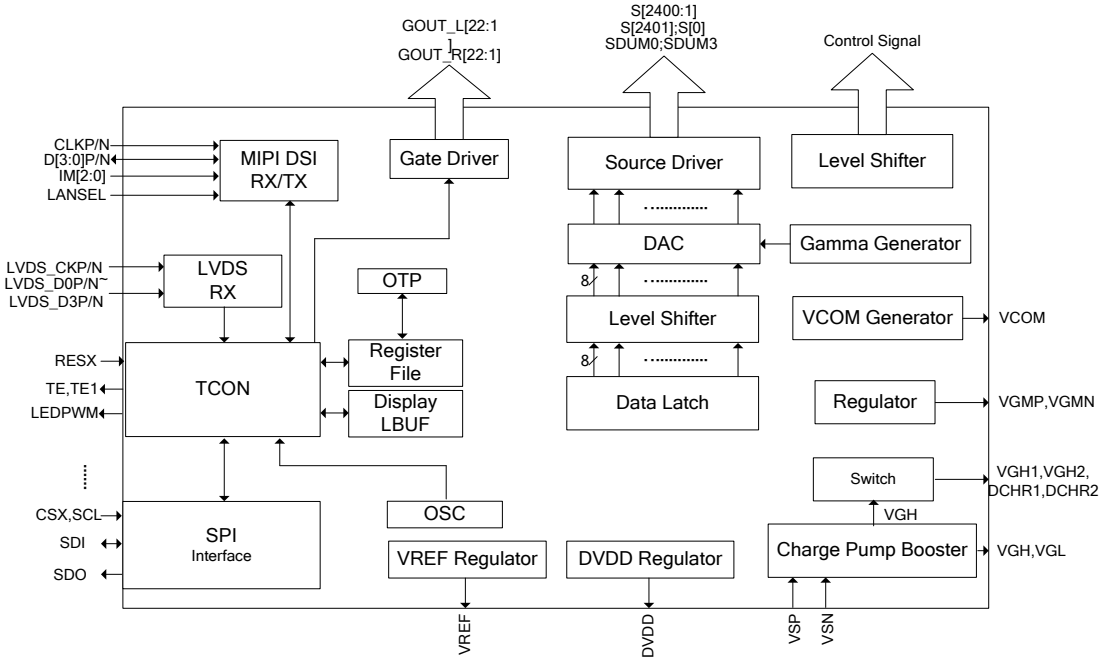


Figure 3.1

3.1.1 System interface

The NV3051F-L supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor Interface) and LVDS.

3.1.5 Source driver circuit

NV3051F-L consists of a 2400-output source driver circuit (S1 to S1200,S1201 to S2400) and several source dummy outputs (SDUM3;SDUM0;S[2401];S[0]).Data transmitted through MIPI video mode are latched when a single line data has been accumulated. And then the latched data controls the source driver and generates a drive waveform.

3.1.2 Grayscale voltage generating circuit

NV3051F-L has true 8-bit resolution D/A converter, which generates 256 Gamma-corrected values and cooperates with OP-AMP structure to enhance display quality.The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

3.1.3 Timing controller

NV3051F-L has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, image data accessing timing, etc.

3.1.4 Oscillator (OSC)

The NV3051F-L also features an internal oscillator. In standby mode, the oscillator is halted to reduce power consumption.

3.1.6 Gate driver circuit

NV3051F-L consists of output gate driver control circuit. The gate driver circuit outputs gate driver signals at either VGH or VGL level.

3.1.7 LCD driving power supply circuit

The LCD driving power supply circuit generates the voltage levels VGH,VGL and VCOM for driving an LCD. All this voltages can be adjusted by register setting.

4. PIN DESCRIPTIONS

4.1 Pin Definition

Signal	I/O	PAD Type (Voltage Level)	Function
Global Control Signal			
RS[1]	I	Digital Input (IOVCC-VSSI)	When rising edge,turn on the chip and enter the display on mode.If no used,let it open.
RESX	I	Digital Input (IOVCC-VSSI)	Global Reset Signal. Active Low.
TE	O	Digital Output (IOVCC-VSSI)	Tearing effect output pin is used to synchronize MCU frame writing, activated by S/W command. When this pin is not activated (TE function OFF), this pin is VSSI level.
TE1	O	Digital Output (IOVCC-VSSI)	Output pin for scan line signal, activated by S/W command. When this pin is not activated, this pin is VSSI level.
LEDPWM	O	Digital Output (IOVCC-VSSI)	LCD backlight control PWM output pin.
PWM_VSN	O	Digital Output (VSSI-VSN)	LCD backlight control PWM output pin.
LED_K1～ LED_K5	O	-	LCD backlight control on chip switch drain output.(3V backlight)

<table>
<tr><th colspan="4">MIPI Interface</th></tr>
<tr><td>IM[2:0]</td><td>I</td><td>Digital Input
(IOVCC-VSSI)</td><td>Interface mode select pins.IM [2]: Internal pull low.
Notes:
(1) IM[2:0] pins are used to configure lane sequence and polarity.
(2) The bottom table is an example for MIPI 4 lane setting.
<table>
<tr><th colspan="3">External Pad Set</th><th colspan="5">Configuration of MIPI Lane</th></tr>
<tr><td>IM[2]</td><td>IM[1]</td><td>IM[0]</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>D3P/N</td><td>D2P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>D3N/P</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>D3P/N</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D2P/N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>D3N/P</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D2N/P</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr>
</table></td></tr>
<tr><td>LANSEL</td><td>I</td><td>Digital Input
(IOVCC-VSSI)</td><td>MIPI DSI Lane number selection pin.
LANSEL=”1”, MIPI DSI is 2 Lane mode.
LANSEL=”0”, MIPI DSI is 3 or 4 Lane mode.</td></tr>
<tr><td>CLKP</td><td>I</td><td>MIPI Input
(MV1P2-MGND)</td><td>MIPI-DSI clock Lane positive-end input pin.</td></tr>
<tr><td>CLKN</td><td>I</td><td>MIPI Input
(MV1P2-MGND)</td><td>MIPI-DSI clock Lane negative-end input pin.</td></tr>
<tr><td>D0P</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 0 positive-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D0N</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 0 negative-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D1P</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 1 positive-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D1N</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 1 negative-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D2P</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 2 positive-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D2N</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 2 negative-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D3P</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 3 positive-end input/output pin.
Please connected to MGND if not used.</td></tr>
<tr><td>D3N</td><td>I/O</td><td>MIPI I/O
(MV1P2-MGND)</td><td>MIPI-DSI data Lane 3 negative-end input/output pin.
Please connected to MGND if not used.</td></tr>
</table>

<table>
<tr><td colspan="4">LVDS Interface</td></tr>
<tr><td>LVDS_CKP/N</td><td>I</td><td>LVDS input
(IOVCC-VSSI)</td><td>LVDS clock Input.</td></tr>
<tr><td>LVDS_D0P/N~LVDS_D3P/N</td><td>I</td><td>LVDS input
(IOVCC-VSSI)</td><td>LVDS data Input.</td></tr>
<tr><td colspan="4">SPI Interface</td></tr>
<tr><td>CSX</td><td>I</td><td>Digital Input
(IOVCC-VSSI)</td><td>Chip select signal for SPI interface operation.
”0” : the NV3051F-L is accessible.
”1” : the NV3051F-L is not accessible.
If not used, please fix to the IOVCC or VSSI.</td></tr>
<tr><td>SCL</td><td>I</td><td>Digital Input
(IOVCC-VSSI)</td><td>SCL: Serial interface Clock Input.
If not used, please fix to the IOVCC or VSSI.</td></tr>
<tr><td>SDI</td><td>I/O</td><td>Digital I/O
(IOVCC-VSSI)</td><td>SDI: Serial interface DATA Input/Output.
If not used, please fix to the IOVCC or VSSI.</td></tr>
<tr><td>SDO</td><td>O</td><td>Digital Output
(IOVCC-VSSI)</td><td>Serial interface DATA output. If not used, please let it open.</td></tr>
<tr><td colspan="4">Source Control Signals</td></tr>
<tr><td>S[2400:1]</td><td>O</td><td>Analog Output
(VSP-VSN)</td><td>Output source driver signals. The D/A converted 256-gray-scale analog voltage is output. Source output mapping with different resolution.
<table>
<tr><th>Resolution</th><th>Source channel</th></tr>
<tr><td>800RGB</td><td>S[2400:1201],S[1200:1]</td></tr>
<tr><td>768RGB</td><td>S[2400:1249],S[1152:1]</td></tr>
<tr><td rowspan="3">750RGB</td><td>S[2400:1249],S[1152:55]</td></tr>
<tr><td>S[2346:1249],S[1152:1]</td></tr>
<tr><td>S[2400:1276],S[1125:1]</td></tr>
<tr><td>720RGB</td><td>S[2400:1321],S[1080:1]</td></tr>
<tr><td>640RGB</td><td>S[2400:1441],S[960:1]</td></tr>
<tr><td>600RGB</td><td>S[2400:1501],S[900:1]</td></tr>
<tr><td>540RGB</td><td>S[2400:1591],S[810:1]</td></tr>
<tr><td rowspan="2">480RGB</td><td>S[2400:1681];S[720:1]</td></tr>
<tr><td>S[2400:1201];S[1200:961]</td></tr>
<tr><td rowspan="2">400RGB</td><td>S[2400:1201]</td></tr>
<tr><td>S[2400:1801];S[600:1]</td></tr>
<tr><td>320RGB</td><td>S[2400:1441]</td></tr>
</table></td></tr>
<tr><td>SDUM[3]
S[2401]</td><td>O</td><td>Analog Output
(VSP-VSN)</td><td>Source dummy output.</td></tr>
</table>

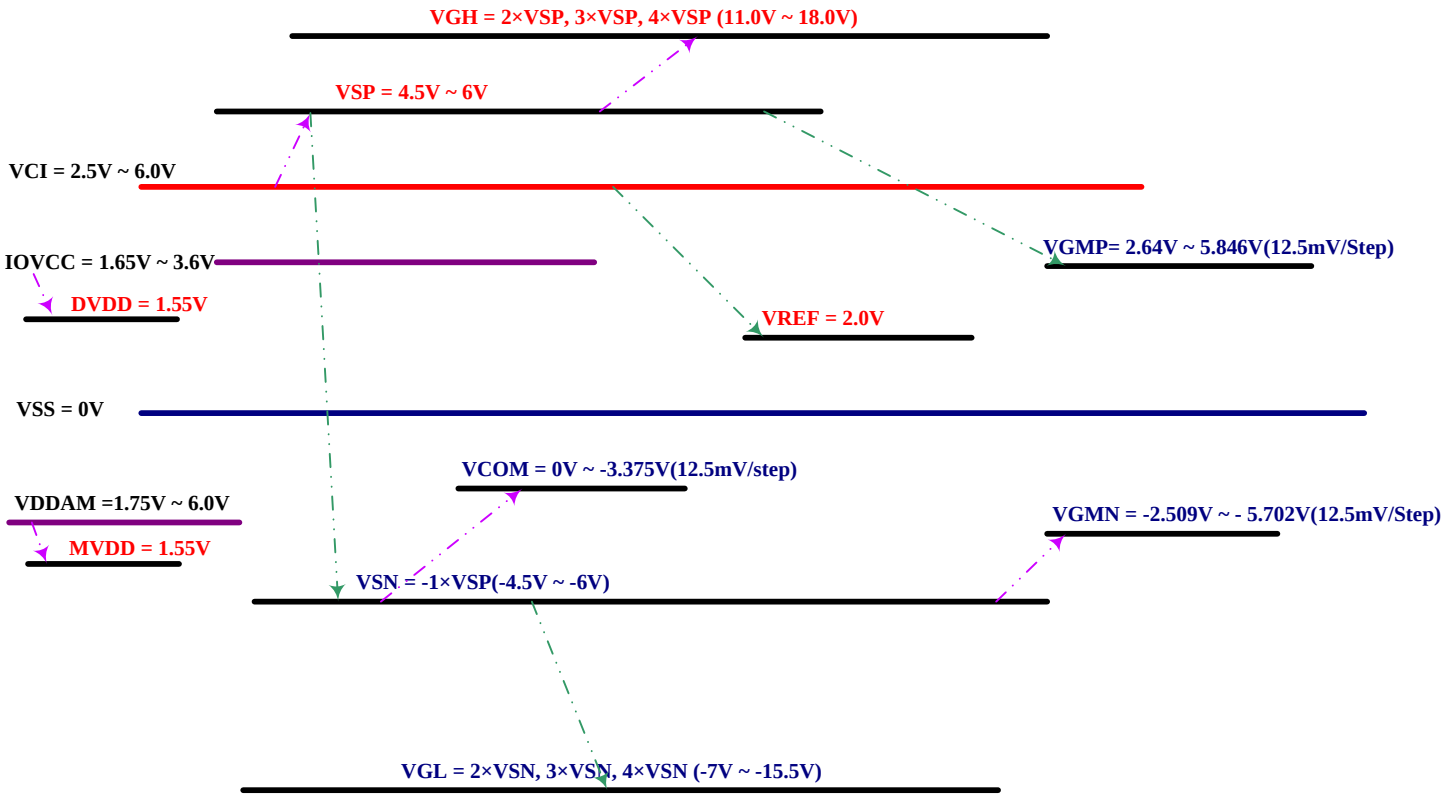
S[0] SDUM[0]	O	Analog Output (VSP-VSN)	Source dummy output.

Panel Control and VCOM Pins			
GOUTL [22:1]	O	Analog Output	Gate control signals for panel in left side of IC.
GOUTR [22:1]	O	Analog Output	Gate control signals for panel in right side of IC.
VCOM_L	O	DUMMY Pin	VCOM DUMMY Pin.
VCOM_R	O	Analog Output	VCOM signal output.
VCOM_DUM	O	DUMMY Pin	VCOM DUMMY Pin.
Charge Pump / Boost			
VSP	I	Analog Input	Input voltage from the set-up circuit (4.5V to 6V).
VSN	I	Analog Input	Input voltage from the set-up circuit (-4.5V to -6V).
VGH	O	Analog Output	Positive Power Supply for Gate Driver. VGH=2xVSP, 3xVSP, 4xVSP
VGL	O	Analog Output	Negative Power Supply for Gate Driver. VGL=2xVSN, 3xVSN, 4xVSN
VGH1	O	Analog Output	This pin is used to discharge function. Connect to a capacitor between VGH1 and system ground. If not used, please let this pin short to VGH.
VGH2	O	Analog Output	This pin is used to discharge function. Connect to a capacitor between VGH2 and system ground. If not used, please let this pin short to VGH.
DCHR1	O	Resister	External discharge for VGH1 voltage. Connect to a resister between DCHR1 and system ground.
DCHR2	O	Resister	External discharge for VGH2 voltage. Connect to a resister between DCHR2 and system ground.
EXTP	O	Analog Output	Booster/charge pump power IC output to generate VSP.
EXTN	O	Analog Output	Booster/charge pump power IC output to generate VSN.
Regulator Relative Pins			
VGMP	O	Analog Output	Output voltage generated from VSP. It's used for positive gray scale voltage.
VGMN	O	Analog Output	Output voltage generated from VSN. It's used for negative gray scale voltage.
VREF	O	Analog Output	Reference Voltage for internal voltage generating circuits.

Power Supply and Regulator pins			
VCI	I	Power Supply	Power supply for analog circuits. (VCI=2.5V to 6V)
VDDAM	I	Power Supply	Power Supply for MIPI regulator circuits.(VDDAM=1.75V to 6V)
IOVCC	I	Power Supply	External Power Supply for IO pads and other logic circuits. (IOVCC=1.65 to 3.6V)
VPP	I	Power Supply	Input power for NV memory programming. Input power range: 8.0V ~ 8.5V (Typical=8.25V). When not under programming, VPP pin can be float or tied to ground.
AGND	I	Ground	Analog Ground for analog circuits.
VSSI	I	Ground	I/O Ground for I/O logic circuits.
VSSI_LVDS	I	Ground	I/O Ground for LVDS logic circuits.
DGND	I	Ground	Digital Ground for digital circuits.
DGND_LVDS	I	Ground	Digital Ground for LVDS circuits.
MGND	I	Ground	MIPI Ground for MIPI circuits.
RGND	I	Ground	Analog Ground for regulators.
CGND1	I	Ground	Analog Ground for PUMP’s.
DVDD	O	Analog Output	Internal Power Supply for Digital Logic Circuits.
DVDD_LVDS	O	Analog Output	Internal Power Supply for LVDS Logic Circuits.
MVDD	O	Analog Output	Internal Power Supply for MIPI.

Test/Dummy Signal			
TEST_EN	I	Digital Input (IOVCC-VSSI)	Internal pull low, digital test enable, active high. If not used, please let it open or connect to VSSI.
BIST_EN	I	Digital Input (IOVCC-VSSI)	Internal pull low, CP test enable, active high. If not used, please let it open or connect to VSSI.
CLK_SEL	I	Digital Input (IOVCC-VSSI)	Test pin, internal pull low. If not used, please let it open or connect to VSSI.
EXT_CLK	I	Digital Input (IOVCC-VSSI)	Test pin, If not used, please let it open or connect to VSSI.
TEST[3:0]	I	Digital Input (IOVCC-VSSI)	Test pins. Please let them float or connect to VSSI.
TOUT[3:0]	O	Digital Output (IOVCC-VSSI)	Test output pins. Please let them float.
DUMMYR1;DUMMYR2	-	-	Dummy pins. For bonding resistance measurement. There are two pads here, propose to connect them separately.
DUMMY	-	-	Bottom of the chip. Dummy pins. They are not used, left it open.
DUMMY3-DUMMY30/DUMMY151-DUMMY174/ DUMMY295- DUMMY322	-	-	Top of the chip. Dummy pins. They are not used, left it open.
NC	-	-	Not connect.

4.2. Power Block Diagram



4.3. Power Supply Configuration

Two power structures for different applications controlled by BOOSTM[1:0](register control),like the following table.

BOOSTM1	BOOSTM0	Mode
0	1	Mode-8, External VSP and VSN
1	0	Mode-3, Power IC

These pins must connect to VSSI or IOVCC level.

4.3.1. Mode 3: Power IC mode (Mode-3 BOOSTM=2'b10)

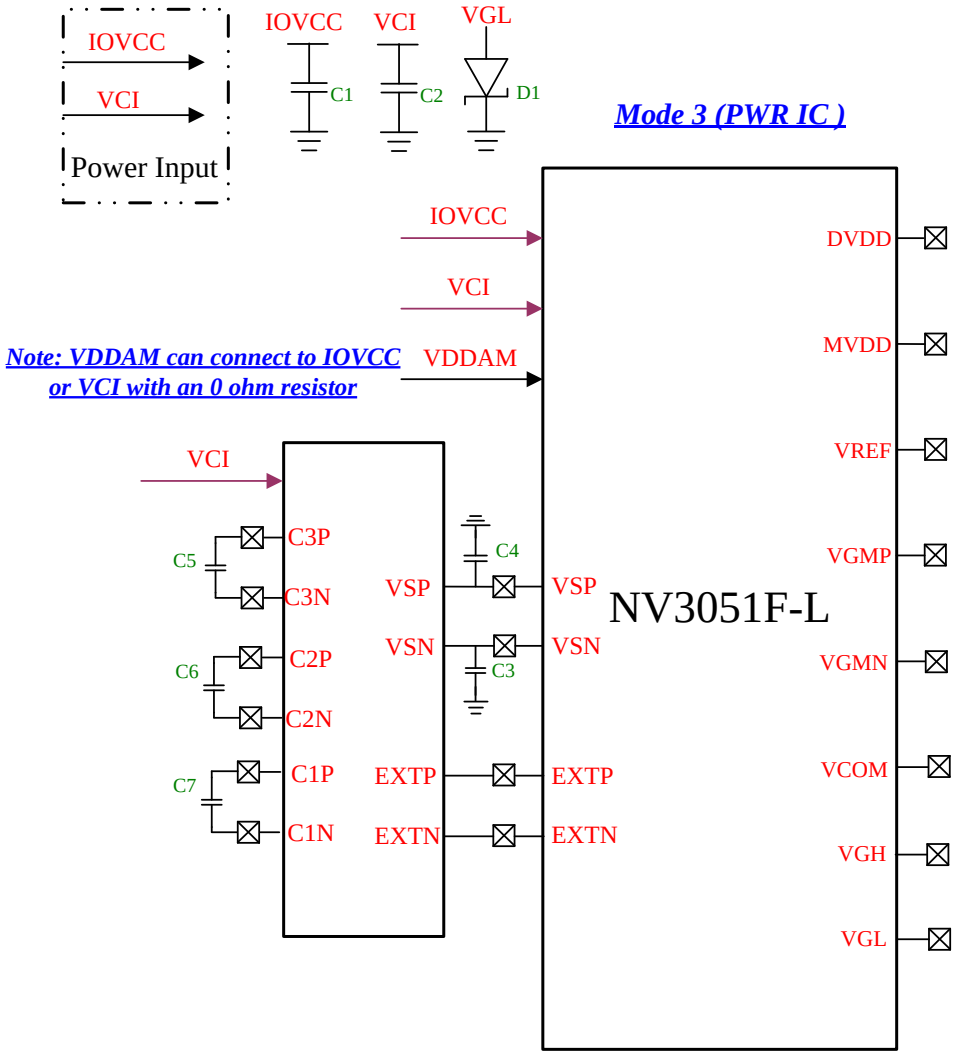


Fig 4.1

4.3.2. Mode 8: External VSP and VSN (Mode-8 BOOSTM=2'b01)

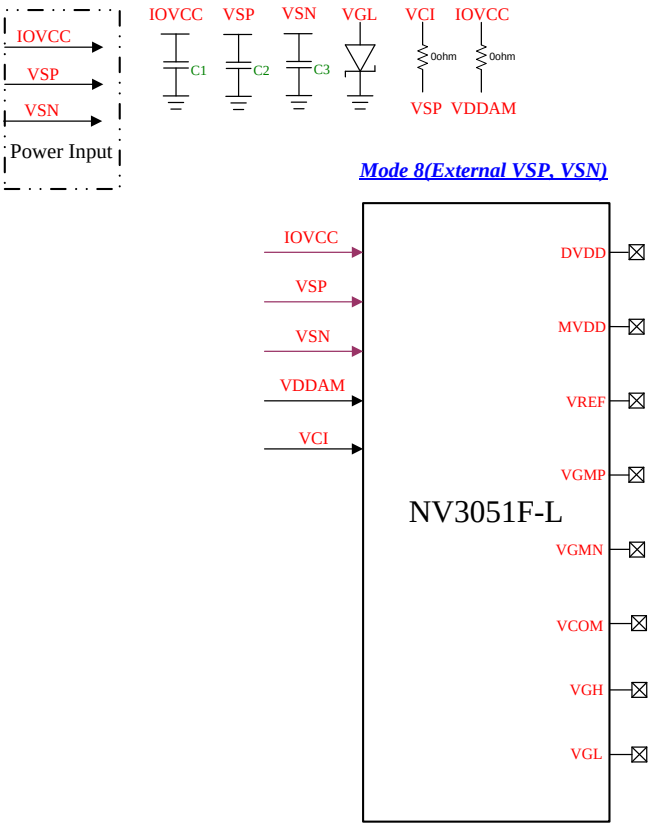


Fig 4.2

4.4 BOM List

4.4.1. Mode-3: Power IC mode

NV3051F-L BOM Lists for WXGA				
No.	**Signal name**	**Values**	**Max ability**	**Note**
1	IOVCC(C1)	1.0uF	4V	I/O and Digital Power
2	VCI(C2)	2.2uF	6.3V	Analog Power
3	C5(C3P/C3N)	1.0uF	6.3V	NV7052 related
4	C6(C2P/C2N)	1.0uF	6.3V	
5	C7(C1P/C1N)	1.0uF	6.3V	
6	VSN(C3)	2.2uF	6.3V	
7	VSP(C4)	2.2uF	6.3V	
8	VGL(D1)	schottky diode		GND-VGL diode

Note: Larger VSP/VSN component values are proposed to get better power efficiency and stability.

4.4.2. Mode-8: External VSP and VSN

NV3051F-L BOM Lists for WXGA (External VSP and VSN)				
No.	**Signal name**	**Values**	**Max ability**	**Note**
1	IOVCC(C1)	1.0uF	4V	I/O and Digital Power
2	VSP(C2)	2.2uF	6.3V	Analog Power
3	VSN(C3)	2.2uF	6.3V	Analog Power
4	VGL(D1)	schottky diode		GND-VGL diode

Note: Larger VSP/VSN component values are proposed to get better power efficiency and stability.

5.INSTRUCTIONS

5.1. Outline

The NV3051F-L supports high speed serial interface, MIPI to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00. Updating command instructions can also be accomplished by using all supporting system interfaces .

The NV3051F-L has the following major categories of

instructions:

(1). System function instructions (User Command Set).

(2). Customer Command List and Description (Manufacturer Command Set / Command 2).

Since updating these instructions are asynchronous to the internal clock of the NV3051F-L, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents of this chapter will describe the supported instructions in detail.

System function commands

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state (Please refer to “RESET TABLE” section). The commands 10h, 11h, 20h, 21h, 22h, 23h, 28h, 29h, 36h will be updated only during V-sync periods while module is in the “Sleep Out” mode to avoid abnormal visual effects, and will be updated immediately in the “Sleep In” mode. The Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh),Read Display Signal Mode (0Eh), and Read Display Self Diagnostic Result (0Fh) will be updated immediately in both “Sleep In” and “Sleep Out” mode.

System function command accessing flow is described as the following example.

Example 1: Sleep Out
CMDWR 0x11

Example 2: Display On
CMDWR 0x29

Example 3: TE ON
CMDWR 0x35
DATWR 0x00

System Function Command List

Page 0 Command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	0	0	0	0	0	0	0	0	00h	No operation
	1	1	↑	rd_00[7:0]								ffh	-
	1	1	↑	rd_01[7:0]								ffh	-
SWRESET	0	↑	1	0	0	0	0	0	0	0	1	01h	Software reset
	1	1	↑	rd_01[7:0]								ffh	-
RDDIDIF	0	↑	1	0	0	0	0	0	1	0	0	04h	Read display ID
	1	1	↑	ID1								30h	ID1 read
	1	1	↑	ID2								52h	ID2 read
	1	1	↑	ID3								01h	ID3 read
RDDPM	0	↑	1	0	0	0	0	1	0	1	0	0Ah	read display power mode
	1	1	↑	boost	idle_mode_on	0	sleep_out	normal	disp_on	0	0	08h	-
RDD MADCTL	0	↑	1	0	0	0	0	1	0	1	1	0Bh	read display MADCTL
	1	1	↑	0	0	0	0	bgr	0	ss	gs	00h	-
RDDCOLMOD	0	↑	1	0	0	0	0	1	1	0	0	0Ch	read display pixel format
	1	1	↑	0	dpi[2:0]			0	0	0	0	70h	-
RDDIM	0	↑	1	0	0	0	0	1	1	0	1	0Dh	Read display image
	1	1	↑	0	0	inver_on	pixel_on	pixel_off	gcs[2:0]			00h	-
RDDSM	0	↑	1	0	0	0	0	1	1	1	0	0Eh	Read display signal mode
	1	1	↑	tear_on	tear_mode	0	0	0	0	0	0	00h	-
RDDSDR	0	↑	1	0	0	0	0	1	1	1	1	0Fh	Read display self-diagnostic result
	1	1	↑	regld	fundt	0	0	0	0	0	esd_chk	00h	-
SLPIN	0	↑	1	0	0	0	1	0	0	0	0	10h	Sleep in
SLPOUT	0	↑	1	0	0	0	1	0	0	0	1	11h	Sleep out
NORON	0	↑	1	0	0	0	1	0	0	1	1	13h	normal mode on and partial mode off
INVOFF	0	↑	1	0	0	1	0	0	0	0	0	20h	Display inversion off
INVON	0	↑	1	0	0	1	0	0	0	0	1	21h	Display inversion on
ALLPOFF	0	↑	1	0	0	1	0	0	0	1	0	22h	All Pixel off
ALLPON	0	↑	1	0	0	1	0	0	0	1	1	23h	All Pixel on
DISPOFF	0	↑	1	0	0	1	0	1	0	0	0	28h	Display off

Page 0 Command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
DISPON	0	↑	1	0	0	1	0	1	0	0	1	29h	Display on
TEOFF	0	↑	1	0	0	1	1	0	1	0	0	34h	Tearing Effect Line off
TEON	0	↑	1	0	0	1	1	0	1	0	1	35h	Tearing Effect Line on
	1	↑	1	0	0	0	0	0	0	0	tear_ mode	00h	-
MADCTL	0	↑	1	0	0	1	1	0	1	1	0	36h	Memory data access control
	1	↑	1	0	0	0	0	bgr	0	ss	gs	00h	-
IDMODEOFF	0	↑	1	0	0	1	1	1	0	0	0	38h	Idle mode off
IDMODEON	0	↑	1	0	0	1	1	1	0	0	1	39h	Idle mode on and other mode off
WRTESCN	0	↑	1	0	1	0	0	0	1	0	0	44h	Write tear scanline
	1	↑	1	te_on_lines[7:0]								00h	-
RDSCNL	0	↑	1	0	1	0	0	0	1	0	1	45h	Read scanline
	1	1	↑	te_on_lines[7:0]								00h	-
WRTEWIDTH	0	↑	1	0	1	0	0	0	1	1	0	46h	Write Tear Scan Line Width
	1	↑	1	te_width[7:0]								00h	-
RDTEWIDTH	0	↑	1	0	1	0	0	0	1	1	1	47h	Read Tear Scan Line Width
	1	1	↑	te_width[7:0]								00h	-
WRDISBV	0	↑	1	0	1	0	1	0	0	0	1	51h	Write Display Brightness
	1	↑	1	dbv__reg[15:8]								00h	-
	1	↑	1	dbv__reg[7:0]								00h	-
RDDISBV	0	↑	1	0	1	0	1	0	0	1	0	52h	Read Display Brightness
	1	1	↑	dbv[7:0]								00h	-
WRCTRLD	0	↑	1	0	1	0	1	0	0	1	1	53h	Write CTRL Display
	1	↑	1	sam_out door3	0	bctrl	0	disp_di m	backlight _on	0	0	00h	-
RDCTRLD	0	↑	1	0	1	0	1	0	1	0	0	54h	Read CTRL Display Value
	1	1	↑	0	0	bctrl	0	disp_di m	backlight _on	0	0	00h	-

Page 0 Command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
RDID1	0	↑	1	1	1	0	1	1	0	1	0	DAh	read display id 1
	1	1	↑	id1								30h	-
RDID2	0	↑	1	1	1	0	1	1	0	1	1	DBh	read display id 2
	1	1	↑	id2								52h	-
RDID3	0	↑	1	1	1	0	1	1	1	0	0	DCh	read display id 3
	1	1	↑	id3								01h	-
ENEXTC	0	↑	1	1	1	1	1	1	1	1	1	FFh	EXTC Command Set Enable Register
	1	↑	1	0	0	0	0	0	0	page[1:0]		00h	-

5.2. SYSTEM COMMAND DESCRIPTION

5.2.1. NOP (00h)

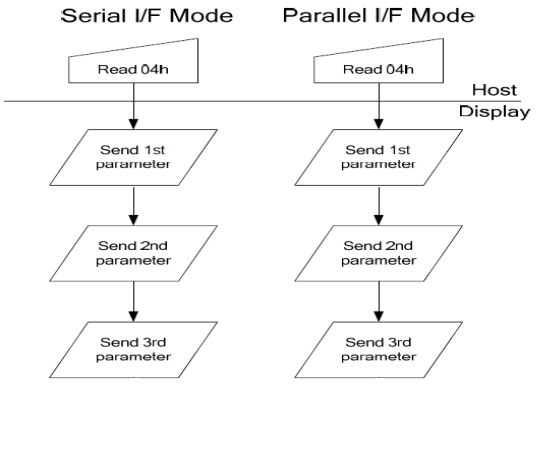
<table>
<tr><th colspan="2">00H</th><th colspan="9">NOP (No Operation)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00H</td></tr>
<tr><td>1st Parameter</td><td>Read</td><td colspan="8">rd_00[7:0]</td><td>ffh</td></tr>
<tr><td>2nd Parameter</td><td>Read</td><td colspan="8">rd_01[7:0]</td><td>ffh</td></tr>
<tr><td>Description</td><td colspan="10">rd_00[7:0]:Support MOTO E4 ID1 read function.
rd_01[7:0]:Usually apply to software reset order.After finish to send “FF 98 81 01”,it can be used as MOTE E4 ID2 read address.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><td>rd_00[7:0]</td><td>rd_00[7:0]</td></tr><tr><td>Power On Sequence</td><td>ffh</td><td>ffh</td></tr><tr><td>S/W Reset</td><td>ffh</td><td>ffh</td></tr><tr><td>H/W Reset</td><td>ffh</td><td>ffh</td></tr></table></td></tr>
</table>

5.2.2. Software Reset(01h)

<table>
<tr><td colspan="2">01H</td><td colspan="9">SWRESET (Software Reset)</td></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01H</td></tr>
<tr><td>Parameter</td><td>Write/Read</td><td colspan="8">rd_01[7:0]</td><td>ffh</td></tr>
<tr><td>Description</td><td colspan="10">rd_01[7:0]:Usually apply to software reset order.After finish to send “FF 98 81 01”,it can be used as MOTE E4 ID2 read address.</td></tr>
<tr><td>Restriction</td><td colspan="10">It is necessary to wait 5msec before sending a new command following software reset.The display module loads all display suppliers’ factory default values to the registers during 5msec.If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command.The Software Reset command cannot be sent during Sleep Out sequence.
As MOTE E4 ID2 Read restriction, It can be to read after send“FF 98 81 01”.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>ffh</td></tr><tr><td>S/W Reset</td><td>ffh</td></tr><tr><td>H/W Reset</td><td>ffh</td></tr></table></td></tr>
</table>

5.2.3 Read Display ID(04h)

<table>
<tr><th colspan="2">04H</th><th colspan="9">RDDIDIF (Read Display ID)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04H</td></tr>
<tr><td>1st parameter</td><td>Read</td><td colspan="8">ID1</td><td>30h</td></tr>
<tr><td>2nd parameter</td><td>Read</td><td colspan="8">ID2</td><td>52h</td></tr>
<tr><td>3rd parameter</td><td>Read</td><td colspan="8">ID3</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="10">The 1st parameter (ID1): LCD module’s manufacturer ID.
The 2nd parameter (ID2): LCD module/driver version ID.
The 3rd parameter (ID3): LCD module/driver ID.
Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 1,2,3 of the command 04h,respectively.</td></tr>
<tr><td>Restriction</td><td colspan="10"></td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>ID1</th><th>ID2</th><th>ID3</th></tr><tr><td>Power On Sequence</td><td>30h</td><td>52h</td><td>01h</td></tr><tr><td>S/W Reset</td><td>30h</td><td>52h</td><td>01h</td></tr><tr><td>H/W Reset</td><td>30h</td><td>52h</td><td>01h</td></tr></table></td></tr>
</table>

Flow Chart	 Serial I/F Mode Parallel I/F Mode Read 04h Read 04h Host Display Send 1st parameter Send 1st parameter Send 2nd parameter Send 2nd parameter Send 3rd parameter Send 3rd parameter Legend Command Parameter Display Action Mode Sequential transter

5.2.4. Read Display Power Mode(0Ah)

<table>
<tr><th colspan="2">0AH</th><th colspan="9">RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>parameter</td><td>Read</td><td>boost</td><td>idle_mode_on</td><td>0</td><td>sleep_out</td><td>normal</td><td>disp_on</td><td>0</td><td>0</td><td>08h</td></tr>
<tr><td>Description</td><td colspan="10">boost=0, charge pump booster off mode.
boost=1, charge pump booster on mode.
sleep_out=0,Sleep In Mode.
sleep_out=1,Sleep Out Mode.
normal =0,Display Normal Mode Off.
normal =1,Display Normal Mode On.
disp_on=0,Display is Off.
disp_on =1, Display is On.
idle_mode_on=0: idel mode off.
idle_mode_on=1: idel mode on.
This read byte can programmed by OTP Function.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h08</td></tr><tr><td>S/W Reset</td><td>8’h08</td></tr><tr><td>H/W Reset</td><td>8’h08</td></tr></table></td></tr>
</table>

5.2.5. Read Display MADCTL(0BH)

<table>
<tr><th colspan="2">0BH</th><th colspan="9">RDDMADCTL(Read Display MADCTL)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0BH</td></tr>
<tr><td>Parameter</td><td>Read</td><td>0</td><td>0</td><td>0</td><td>0</td><td>bgr</td><td>0</td><td>ss</td><td>gs</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display:
bgr=0,RGB format.
bgr=1,BGR format.
ss=0,Source output Left to Right.
ss=1,Source output Right to Left.
gs=0,Gate output from top to bottom.
gs=1,Gate output from bottom to top.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

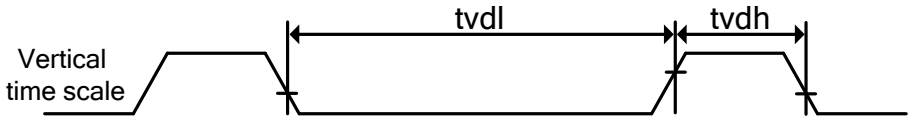
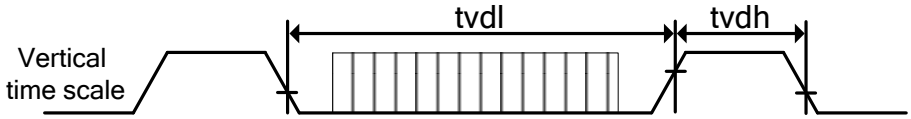
5.2.6. Read Display Pixel Format(0CH)

<table>
<tr><th colspan="2">0CH</th><th colspan="9">RDDCOLMOD (Read Display COLMOD)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0CH</td></tr>
<tr><td>Parameter</td><td>Read</td><td>0</td><td colspan="3">dpi[2:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70H</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display as described in the table below:
<table>
<tr><th colspan="3">dpi[2:0]</th><th>Interface Format</th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16-bit/pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18-bit/pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>24-bit/pixel</td></tr>
<tr><td colspan="3">Others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h70</td></tr>
<tr><td>S/W Reset</td><td>8’h70</td></tr>
<tr><td>H/W Reset</td><td>8’h70</td></tr>
</table></td></tr>
</table>

5.2.7. Read Display Image Mode(0DH)

<table>
<tr><th colspan="2">0DH</th><th colspan="9">RDDIM (Read Display Image Mode)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0DH</td></tr>
<tr><td>parameter</td><td>Read</td><td>0</td><td>0</td><td>inver_on</td><td>pixel_on</td><td>pixel_off</td><td colspan="3">gcs[2:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">inver_on =0,Inversion is Off.
inver_on =1,Inversion is On.
pixel_on =0,Normal Display.
pixel_on =1,White Display.
pixel_off =0,Normal Display.
pixel_off =1,Black Display.
GCS=3’b000,GC0 is selected,others are not defined.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.8. Read Display Signal Mode(0EH)

<table>
<tr><th colspan="2">0EH</th><th colspan="9">RDDSM (Read Display Signal Mode)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>Parameter</td><td>Read</td><td>tear_on</td><td>tear_mode</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command indicates the current status of the display.
TEON=0,Tearing Effect Line Off.
TEON=1, Tearing Effect Line On.
TEAR_MODE=0,The Tearing Effect Output line consists of V-Blanking information only.
 
EAR_MODE=1,The Tearing Effect Output line consists of both V-Blanking and H-Blanking informatic
  </td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.9. Read Display Self-Diagnostic Result(0FH)

<table>
<tr><th colspan="2">0FH</th><th colspan="9">RDDSDR（Read Display Self-Diagnostic Result）</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0FH</td></tr>
<tr><td>Parameter</td><td>Read</td><td>regld</td><td>fundt</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>esd_chk</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">regld =1,when the OTP and register values are the same.
fundt =1,when the chip met User’s functionality requirements.
esd_chk: ESD check result.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.10. Sleep In(10h)

<table>
<tr><th colspan="2">10H</th><th colspan="9">SLPIN (Sleep In)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command cause the NV3051F-L to enter the minimum power consumption mode.
In this mode the NV3051F-L control signals,Internal oscillator and panel scanning are stopped.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be left by the Sleep Out command. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to stabilize. It is necessary to wait 120msec after sending Sleep Out command(when in Sleep In Mode)before the Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table></td></tr>
</table>

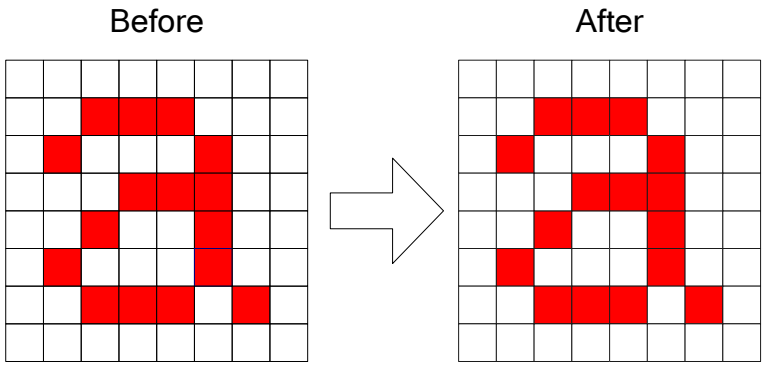
5.2.11. Sleep Out(11H)

<table>
<tr><th colspan="2">11H</th><th colspan="9">SLPOUT (Sleep Out)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command turns off sleep mode.
In this mode ,the NV3051F-L control signals,Internal oscillator and panel scanning are started.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Sleep Out mode. Sleep Out mode can be left by the Sleep In command(10h),S/W reset command (01h) or H/W reset. It is necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
The NV3051F-L loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the NV3051F-L is already Sleep Out mode.During this 5msec, NV3051F-L is running self-diagnostic functions. It is necessary to wait 120msec after sending the Sleep In command (when in Sleep Out mode) before the Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In Mode</td></tr><tr><td>S/W Reset</td><td>Sleep In Mode</td></tr><tr><td>H/W Reset</td><td>Sleep In Mode</td></tr></table></td></tr>
</table>

5.2.12. Normal Display Mode On(13H)

<table>
<tr><th colspan="2">13H</th><th colspan="9">NORON (Normal Display Mode On)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command returns the display to Normal Display Mode.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when Normal Display Mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode On.</td></tr><tr><td>S/W Reset</td><td>Normal Display Mode On.</td></tr><tr><td>H/W Reset</td><td>Normal Display Mode On.</td></tr></table></td></tr>
</table>

5.2.13. Display Inversion Off(20H)

20H	INVOFF (Display Inversion Off)									
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	0	1	0	0	0	0	0	20H
Parameter	-	No Parameter								-
Description	This command is used to recover from display inversion on mode. This command does not change any other status. 									
Restriction	This command has no effect when module is already in Display Inversion Off mode.									

Register Availability

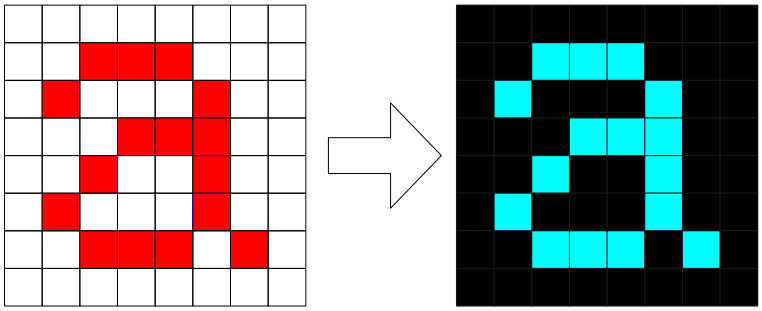
Status	Availability
Normal Mode On,Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

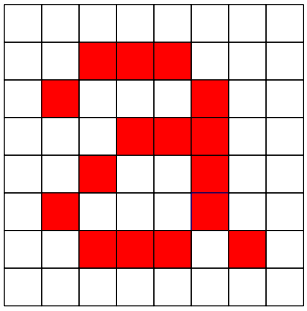
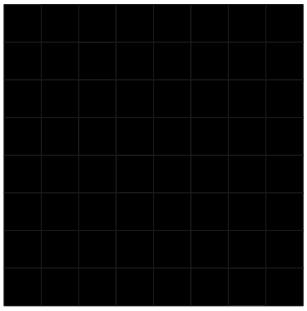
5.2.14. Display Inversion On(21H)

<table>
<tr><th>21H</th><th colspan="9">INVON (Display Inversion On)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into Display Inversion On mode.
This command does not change any other status.
To exit Display Inversion On mode, the Display Inversion Off command(20h)should be written.

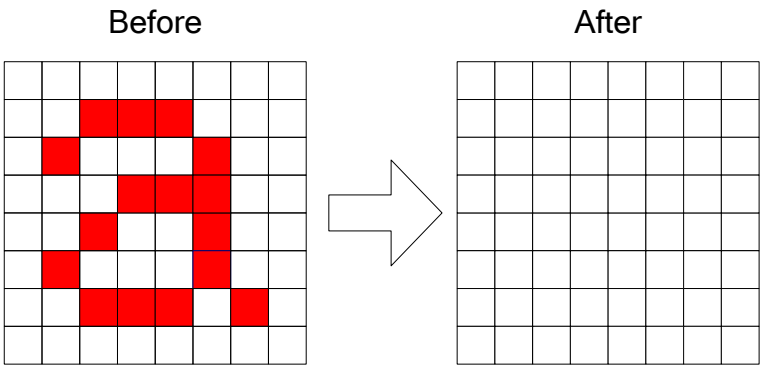
Before
 
After</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the NV3051F-L is already in Inversion On mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
</table>

5.2.15. All Pixel Off(22H)

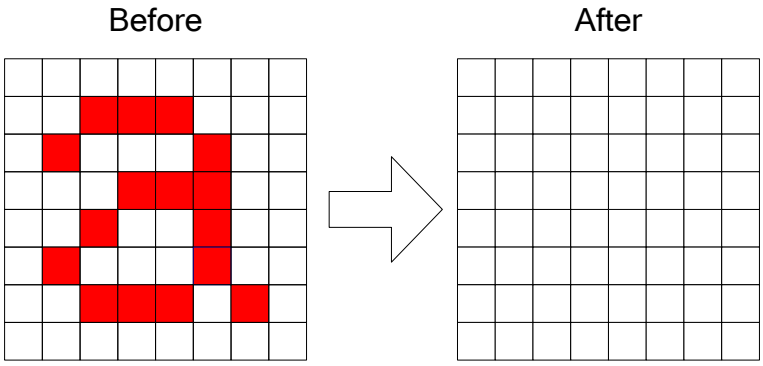
<table>
<tr><th colspan="2">22H</th><th colspan="9">ALLPOFF (All Pixels Off)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>22H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command turns the display panel black in ‘Sleep Out’ mode and a status of the ‘Display On/Off’ register can be ‘on’ or ‘off’.
This command does not change any other status.

Before
 
After
 
‘All Pixels On’,‘Normal Display Mode On’commands are used to leave this mode.
0:normal display
1:NB screen:nom_black = 0,black display;nom_black = 1,white display
NW screen:nom_black = 0,white display;nom_black = 1,black display</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the NV3051F-L is already in All Pixels Off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table></td></tr>
</table>

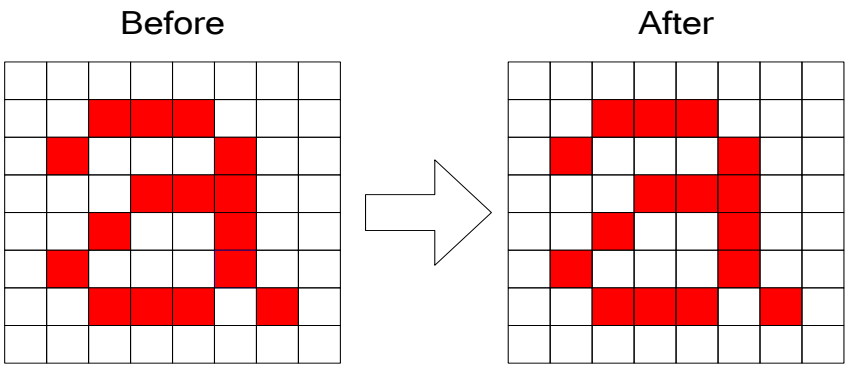
5.2.16. All Pixels On(23H)

<table>
<tr><th colspan="2">23H</th><th colspan="9">ALLPON (All Pixels On)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>23H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command turns the display panel white in ‘Sleep out ’ mode and a status of the ‘Display On/Off’ register can be ‘on’ or ‘off’.This command does not change any other status.
 
‘All Pixels Off’, ‘Normal Display Mode On’commands are used to leave this mode.
0:normal display.
1:NB screen:nom_black = 0,white display;nom_black = 1,black display.
NW screen:nom_black = 0,black display;nom_black = 1,white display.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the NV3051F-L is already in All Pixels On mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Off</td></tr><tr><td>S/W Reset</td><td>Off</td></tr><tr><td>H/W Reset</td><td>Off</td></tr></table></td></tr>
</table>

5.2.17. Display Off(28H)

<table>
<tr><th colspan="2">28H</th><th colspan="9">DISOFF (Display Off)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into Display Off mode. In this mode, the output data is disabled and blank page is inserted.
This command makes no change any other status.
There will be no abnormal visible effect on the display.
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in Display Off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
</table>

5.2.18. Display On(29H)

<table>
<tr><th colspan="2">29H</th><th colspan="9">DISON (Display On)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to recover from Display Off mode. Output data is enabled.
This command does not change any other status.
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the NV3051F-L is already in Display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display off</td></tr><tr><td>S/W Reset</td><td>Display off</td></tr><tr><td>H/W Reset</td><td>Display off</td></tr></table></td></tr>
</table>

5.2.19. Tearing Effect Line OFF(34H)

<table>
<tr><th colspan="2">34H</th><th colspan="9">TEOFF (Tearing Effect Line OFF)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn off the Display module’s Tearing Effect output signal(Active Low) from the TE signal line.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the Tearing Effect output is already off.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Tearing Effect Line Off</td></tr><tr><td>S/W Reset</td><td>Tearing Effect Line Off</td></tr><tr><td>H/W Reset</td><td>Tearing Effect Line Off</td></tr></table></td></tr>
</table>

5.2.20. Tearing Effect Line ON(35H)

<table>
<tr><th colspan="2">35H</th><th colspan="9">TEON (Tearing Effect Line On)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="7">No Parameter</td><td>tear_mode</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to turn on the Tearing Effect output signal from the TE signal line.
tear_mode:describes the mode of the Tearing Effect Output Line.
Tearing Effect Line mode.
0:The Tearing Effect Output line consists of V-Blanking information only.
1:The Tearing Effect Output line consists of both V-Blanking and H-Blanking information.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the Tearing Effect output is already on.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Tearing Effect Line Off</td></tr><tr><td>S/W Reset</td><td>Tearing Effect Line Off</td></tr><tr><td>H/W Reset</td><td>Tearing Effect Line Off</td></tr></table></td></tr>
</table>

5.2.21. Display Access Control(36H)

<table>
<tr><th colspan="2">36H</th><th colspan="9">MADCTL (Display Access Control)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36H</td></tr>
<tr><td>Parameter</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>bgr</td><td>0</td><td>ss</td><td>gs</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This command defines the panel operation mode.
<table>
<tr><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>bgr</td><td>Pannel RGB-BGR Order.</td><td>Color selector switch control.
(0’ =RGB color filter panel, ‘1’ =BGR color filter panel)</td></tr>
<tr><td>ss</td><td>Panel Flip Horizontal.</td><td>Select the source driver scan direction on the panel module.（SS=“1” Source Scan sequence from right to left, ‘0’ = Source Scan sequence from left to right）</td></tr>
<tr><td>gs</td><td>Panel Flip Vertical.</td><td>Select the gate driver scan direction on panel module.（GS=“1” Gate Scan sequence from bottom to top, ‘0’ = Gate Scan sequence from top to bottom）</td></tr>
</table>
Note:gs scan direction depend on panel’s design. Top-Left(0,0) means the physical panel location.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="10">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>S/W Reset</td><td>8’h00</td></tr>
<tr><td>H/W Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
</table>

5.2.22. Idle Mode Off(38H)

<table>
<tr><th colspan="2">38H</th><th colspan="9">IDMODEOFF (Idle Mode Off)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command causes the Display module to exit the Idle mode.
In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the module is already in the Idle Mode Off.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Idle Mode Off,Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On,Idle Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></table></td></tr>
</table>

5.2.23. Idle mode on and other mode off (39H)

<table>
<tr><th colspan="2">39H</th><th colspan="9">IDMODEON (Idle mode on and other mode off)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39H</td></tr>
<tr><td>Parameter</td><td>-</td><td colspan="8">No Parameter</td><td>-</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into the Idle Mode On. In the Idle Mode On, color expression is reduced.</td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when the module is already in the Idle Mode On.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle Mode Off</td></tr><tr><td>S/W Reset</td><td>Idle Mode Off</td></tr><tr><td>H/W Reset</td><td>Idle Mode Off</td></tr></table></td></tr>
</table>

5.2.24. Write Tear Scan Line(44H)

<table>
<tr><th colspan="2">44H</th><th colspan="9">WRTESCN (Write Tear Scan Line)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44H</td></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">te_on_lines[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command turns on the display module’s TE signal when the display module reaches line te_on_lines[7:0].</td></tr>
<tr><td>Restriction</td><td colspan="10">The command takes affect with the end of one frame.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.25. Read Scan Line(45H)

<table>
<tr><th colspan="2">45H</th><th colspan="9">RDSCNL(Read Scan Line)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>45H</td></tr>
<tr><td>Parameter</td><td>Read</td><td colspan="8">te_on_lines[7:0]</td><td>00h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte returns the current scan line.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.26. Write Tear Scan Line Width(46H)

<table>
<tr><th colspan="2">46H</th><th colspan="9">WRTEWIDTH(Write Tear Scan Line Width)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>46H</td></tr>
<tr><td>Parameter</td><td>Write</td><td colspan="8">te_width[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">Set the width of TE scan line.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.27. Read Tear Scan Line Width(47H)

<table>
<tr><th colspan="2">47H</th><th colspan="9">RDTEWIDTH(Read Tear Scan Line Width)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>47H</td></tr>
<tr><td>Parameter</td><td>Read</td><td colspan="8">te_width[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">Read the width of TE scan line.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.28. Write Display Brightness Value(51H)

<table>
<tr><th colspan="2">51H</th><th colspan="9">WRDISBV(Write Display Brightness Value)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51H</td></tr>
<tr><td>1st Parameter</td><td>Write</td><td colspan="8">dbv_reg[15:8]</td><td>00H</td></tr>
<tr><td>2nd Parameter</td><td>Write</td><td colspan="8">dbv_reg[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to adjust the brightness value of the display.
dbv_reg[15:0]:16-bit,for display brightness of manual brightness setting in the NV3051F-L.PWM output signal sends to LEDPWM pin to control the LED driver IC in order to control display brightness.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>dbv_reg[15:8]</th><th>dbv_reg[7:0]</th></tr><tr><td>Power On Sequence</td><td>8’h00</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.29. Read Display Brightness Value(52h)

<table>
<tr><th colspan="2">52H</th><th colspan="9">RDDISBV(Read Display Brightness Value)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>52H</td></tr>
<tr><td>Parameter</td><td>Read</td><td colspan="8">dbv[7:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to return the brightness value of the display.
dbv[7:0] is reset when display is in Sleep in mode.
dbv[7:0] is ‘0’when bit bctrl of “Write CTRL Display(53h)”command is “0”.
dbv[7:0] is manual set brightness specified with “Write CTRL Display(53h)”command when bctrl bit is ‘1’.
When bit bctrl of “Write CTRL Display(53h)”command is ‘1’or write SLPIN(10h) command, dbv[7:0] output is the brightness value specified with “Write Display Brightness(51h)”command.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

5.2.30. Write CTRL Display Value(53H)

<table>
<tr><th colspan="2">53H</th><th colspan="9">WRCTRLD(Write CTRL Display)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53H</td></tr>
<tr><td>Parameter</td><td>Write</td><td>sam_outdoor3</td><td>0</td><td>bctrl</td><td>0</td><td>disp_dim</td><td>backlight_on</td><td>0</td><td>0</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="9">
This command is used to control display brightness.
sam_outdoor3:SAMSUNG outdoor mode enable switch.“1”=open. “0”=close.
bctrl:Brightness Control Black On/Off. This bit is always used to switch brightness for display.
<table>
<tr><th>bctrl</th><th>Description</th></tr>
<tr><td>0</td><td>Brightness Control Black Off(dbv[7:0]=00h)</td></tr>
<tr><td>1</td><td>Brightness Control Black On(dbv[7:0] is active)</td></tr>
</table>
disp_dim:Display Dimming Control. This function is only for manual brightness setting.
<table>
<tr><th>disp_dim</th><th>Description</th></tr>
<tr><td>0</td><td>Display Dimming Off.</td></tr>
<tr><td>1</td><td>Display Dimming On.</td></tr>
</table>
backlight_on:Backlight Control On/Off.
<table>
<tr><th>backlight_on</th><th>Description</th></tr>
<tr><td>0</td><td>Backlight Control Off.</td></tr>
<tr><td>1</td><td>Backlight Control On.</td></tr>
</table>
Dimming function is adapted to the brightness registers for display when bit bctrl is changed at disp_dim =1,e.g.bctrl:0→1 or 1 → 0.
When backlight_on bit change from “On” to “Off”,backlight is turned off without gradual dimming,even if Display Dimming On(disp_dim=1) are selected.
</td></tr>
<tr><td>Restriction</td><td colspan="9">-</td></tr>
<tr><td>Register Availability</td><td colspan="9">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default	

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

5.2.31. Read CTRL Display Value(54H)

54H		RDCTRLD(Read CTRL Display Value)								
	Write/Read	D7	D6	D5	D4	D3	D2	D1	D0	Default
Command	Write	0	1	0	1	0	1	0	0	54H
Parameter	Read	0	0	bctrl	0	disp_dim	backlight_on	0	0	00H
Description	This command is used to read the control status of display brightness. bctrl: display brightness control. backlight_on: backlight control. disp_dim: display dimming control.									
Restriction	-									
Register Availability										
Default										

Status	Availability
Normal Mode On,Sleep Out	Yes
Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	8'h00
S/W Reset	8'h00
H/W Reset	8'h00

5.2.32. Read Display ID1(DAH)

<table>
<tr><th>DAH</th><th colspan="10">RDID1(Read Display ID1)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DAH</td></tr>
<tr><td>Parameter</td><td>Read</td><td colspan="8">id1</td><td>30h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The parameter is LCD module’s manufacturer ID.
The id1 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value
(Before OTP program)</th><th>Default Value
(Before OTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h30</td><td>OTP value</td></tr><tr><td>H/W Reset</td><td>8’h30</td><td>OTP value</td></tr></table></td></tr>
</table>

5.2.33. Read Display ID2(DBH)

<table>
<tr><th colspan="2">DBH</th><th colspan="9">RDID2(Read Display ID2)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DBH</td></tr>
<tr><td>Parameter</td><td>Read</td><td colspan="8">id2</td><td>52h</td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The parameter is LCD module/driver version ID.
The id2 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value
(Before OTP program)</th><th>Default Value
(Before OTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h52</td><td>OTP value</td></tr><tr><td>H/W Reset</td><td>8’h52</td><td>OTP value</td></tr></table></td></tr>
</table>

5.2.34. Read Display ID3(DCH)

<table>
<tr><th colspan="2">DCH</th><th colspan="9">RDID3(Read ID3)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCH</td></tr>
<tr><td>Parameter</td><td>Read</td><td colspan="8">id3</td><td>01H</td></tr>
<tr><td>Description</td><td colspan="10">This read byte is used to track the LCD module/driver version. It is defined by the display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The parameter is LCD module/driver version ID.
The id3 is programmed by OTP function.</td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value
(Before OTP program)</th><th>Default Value
(Before OTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h01</td><td>OTP value</td></tr><tr><td>H/W Reset</td><td>8’h01</td><td>OTP value</td></tr></table></td></tr>
</table>

5.2.35. EXTC Command Set enable register (FFH)

<table>
<tr><th colspan="2">FFh</th><th colspan="9">ENEXTC (EXTC Command Set Enable Register)</th></tr>
<tr><td></td><td>Write/Read</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>Write</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FFH</td></tr>
<tr><td>Parameter</td><td>Write</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">page[1:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="10">Config page.
Write three times. The first time write 30h, the second time write 52h, the last time write page[1:0].
<table><tr><th>page</th><th>Descriptions</th></tr><tr><td>00</td><td>select page0</td></tr><tr><td>01</td><td>select page1</td></tr><tr><td>10</td><td>select page2</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="10">-</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On,Sleep Out</td><td>Yes</td></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>S/W Reset</td><td>8’h00</td></tr><tr><td>H/W Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

Customer Command List

Page 1 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
IFCTRL2	0	↑	1	0	0	1	0	0	0	0	1	21h	interface_ctrl
	1	↑	1	0	0	0	0	pad_sel	1	0	0	04h	-
IFCTRL3	0	↑	1	0	0	1	0	0	0	0	1	23h	interface_ctrl
	1	↑	1	rgb_enable	0	sync_mode[1:0]		vspl	hspl	dpl	epl	02h	-
VCOM_ADJ1	0	↑	1	0	0	1	1	0	1	1	1	37h	vcom_adj
	1	↑	1	vap_adj								dch	-
VCOM_ADJ2	0	↑	1	0	0	1	1	1	0	0	0	38h	vcom_adj
	1	↑	1	van_adj								57h	-
VCOM_ADJ3	1	↑	1	0	0	1	1	1	0	0	1	39h	vcom_adj
	1	↑	1	vcom_adj								41h	
VCOM_ADJ4	0	↑	1	0	0	1	1	1	0	1	0	3Ah	vcom_adj
	1	↑	1	vcom2_adj								20h	-
PADCTRL1	0	↑	1	0	1	0	0	1	0	0	0	48h	pad_ctrl
	1	↑	1	0	0	vcom_hiz	0	sdo_oe	ledpwm_oe	te_oe	te1_oe	0fh	-
BOOST_CTRL1	0	↑	1	1	0	0	0	0	0	0	0	80h	pump_ctrl
	1	↑	1	0	0	boostm[1:0]		0	0	0	0	10h	-
BOOST_CTRL2	0	↑	1	1	0	0	0	0	0	0	1	81h	pump_ctrl
	1	↑	1	0	0	drvn[1:0]		0	0	drvp[1:0]		11h	-
EXTPW_CTRL1	0	↑	1	1	0	0	1	0	0	0	0	90h	pump_ctrl
	1	↑	1	1	1	1	0	ext_dm_nor[1:0]		ext_dm_pwr[1:0]		E5h	-
EXTPW_CTRL2	0	↑	1	1	0	0	1	0	0	0	1	91h	pump_ctrl
	1	↑	1	0	ext_clkp_nor_width[2:0]			0	ext_clkp_pwr_width[2:0]			44h	-
EXTPW_CTRL3	0	↑	1	1	0	0	1	0	0	1	0	92h	pump_ctrl
	1	↑	1	0	ext_clkn_nor_width[2:0]			0	ext_clkn_pwr_width[2:0]			44h	-
PUMP_CTRL1	0	↑	1	1	0	0	1	1	0	0	0	98h	pump_ctrl
	1	↑	1	vgh_cmp_en	vgh_amp_en	vgh_sync	0	pump_ss_width[1:0]		vgh_sel[1:0]		4ah	-
PUMP_CTRL2	0	↑	1	1	0	0	1	1	0	0	1	99h	pump_ctrl
	1	↑	1	vgh_clk_sel[3:0]				vgh_clamp[3:0]				54h	-
PUMP_CTRL3	0	↑	1	1	0	0	1	1	0	1	0	9Ah	pump_ctrl

Page 1 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	↑	1	vgl_cmp_en	vgl_amp_en	vgl_sync	0	0	0	vgl_sel[1:0]		41h	-
PUMP_CTRL4	0	↑	1	1	0	0	1	1	0	1	1	9Bh	pump_ctrl
	1	↑	1	vgl_clk_sel[3:0]				vgl_clamp[3:0]				56h	-
LVDS_CTRL1	0	↑	1	1	1	1	0	0	0	0	0	D0h	lvds_ctrl
	1	↑	1	0	0	0	0	0	lvfmt	lvbit	lvds_en	06h	-
LVDS_CTRL8	0	↑	1	1	1	1	0	0	1	1	1	D7h	lvds_ctrl
	1	↑	1	0	pol_swap	0	0	lane_swap[3:0]				00h	-
ENEXTC	0	↑	1	1	1	1	1	1	1	1	1	FFh	EXTC Command Set Enable Register
	1	↑	1	0	0	0	0	0	0	page[1:0]		00h	-

5.3. Customer Command List and Description

5.3.1. IFCTRL2: 21H

Address	IFCTRL2								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
21H	0	0	0	0	pad_sel	1	0	0	04H
pad_sel: 0:SPI send “1129” to make the chip enter display on mode,1:pad(RS1) rising edge to make the chip enter display on mode.									

5.3.2. IFCTRL3: 23H

Address	IFCTRL3								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
23H	0	0	sync_mode[1:0]		vspl	hspl	dpl	epl	02H

sync_mode[1:0]: It is used to configure Mode

sync_mode[1:0]		Mode
0	0	Sync+DE
0	1	Sync
1	0	DE
1	1	Sync+DE

vspl: It is used to select the polarity of vs signal for LVDS interface

0: active-low

1: active-high

hspl: It is used to select the polarity of hs signal for LVDS interface

0: active-low

1: active-high

dpl: It is used to select the polarity of pclk signal for LVDS interface

0: rising edge

1: falling edge

epl: It is used to select the polarity of de signal for LVDS interface

0: high enable

1: low enable

5.3.3. vcom_adj:37H～3AH

Address	vcom_adj								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
37h	vap_adj								dcH
38h	van_adj								57H
39h	vcom_adj								41H
3Ah	vcom2_adj								20H

Description

vap_adj: Set the output voltage for VGMP.

vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)
10H	2.842	20H	3.043	30H	3.244	40H	3.445
11H	2.854	21H	3.055	31H	3.257	41H	3.458
12H	2.867	22H	3.068	32H	3.269	42H	3.47
13H	2.879	23H	3.08	33H	3.282	43H	3.483
14H	2.892	24H	3.093	34H	3.294	44H	3.495
15H	2.904	25H	3.106	35H	3.307	45H	3.508
16H	2.917	26H	3.118	36H	3.319	46H	3.521
17H	2.93	27H	3.131	37H	3.332	47H	3.533
18H	2.942	28H	3.143	38H	3.345	48H	3.546
19H	2.955	29H	3.156	39H	3.357	49H	3.558
1AH	2.967	2AH	3.168	3AH	3.37	4AH	3.571
1BH	2.98	2BH	3.181	3BH	3.382	4BH	3.584
1CH	2.992	2CH	3.194	3CH	3.395	4CH	3.596
1DH	3.005	2DH	3.206	3DH	3.407	4DH	3.609
1EH	3.018	2EH	3.219	3EH	3.42	4EH	3.621
1FH	3.03	2FH	3.231	3FH	3.433	4FH	3.634

vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)
50H	3.646	60H	3.848	70H	4.049	80H	4.251
51H	3.659	61H	3.86	71H	4.062	81H	4.264
52H	3.672	62H	3.873	72H	4.075	82H	4.277
53H	3.684	63H	3.886	73H	4.087	83H	4.289
54H	3.697	64H	3.898	74H	4.1	84H	4.302
55H	3.709	65H	3.911	75H	4.112	85H	4.314
56H	3.722	66H	3.923	76H	4.125	86H	4.327
57H	3.735	67H	3.936	77H	4.138	87H	4.34
58H	3.747	68H	3.949	78H	4.15	88H	4.352
59H	3.76	69H	3.961	79H	4.163	89H	4.365
5AH	3.772	6AH	3.974	7AH	4.176	8AH	4.378
5BH	3.785	6BH	3.986	7BH	4.188	8BH	4.39
5CH	3.797	6CH	3.999	7CH	4.201	8CH	4.403

5DH	3.81	6DH	4.012	7DH	4.213	8DH	4.416
5EH	3.823	6EH	4.024	7EH	4.226	8EH	4.428
5FH	3.835	6FH	4.037	7FH	4.239	8FH	4.441

vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)
90H	4.454	A0H	4.655	B0H	4.856	C0H	5.057
91H	4.466	A1H	4.668	B1H	4.868	C1H	5.069
92H	4.479	A2H	4.68	B2H	4.881	C2H	5.082
93H	4.492	A3H	4.693	B3H	4.894	C3H	5.094
94H	4.504	A4H	4.705	B4H	4.906	C4H	5.107
95H	4.517	A5H	4.718	B5H	4.919	C5H	5.119
96H	4.529	A6H	4.73	B6H	4.931	C6H	5.132
97H	4.542	A7H	4.743	B7H	4.944	C7H	5.144
98H	4.555	A8H	4.756	B8H	4.956	C8H	5.157
99H	4.567	A9H	4.768	B9H	4.969	C9H	5.169
9AH	4.58	AAH	4.781	BAH	4.981	CAH	5.182
9BH	4.592	ABH	4.793	BBH	4.994	CBH	5.195
9CH	4.605	ACH	4.806	BCH	5.006	CCH	5.207
9DH	4.618	ADH	4.818	BDH	5.019	CDH	5.22
9EH	4.63	AEH	4.831	BEH	5.031	CEH	5.232
9FH	4.643	AFH	4.843	BFH	5.044	CFH	5.245

vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)	vap_adj[7:0] (Hex)	VGMP (V)
D0H	5.257	E0H	5.458	F0H	5.659
D1H	5.27	E1H	5.471		
D2H	5.282	E2H	5.483		
D3H	5.295	E3H	5.496		
D4H	5.307	E4H	5.508		
D5H	5.32	E5H	5.521		
D6H	5.333	E6H	5.533		
D7H	5.345	E7H	5.546		
D8H	5.358	E8H	5.558		
D9H	5.37	E9H	5.571		
DAH	5.383	EAH	5.583		
DBH	5.395	EBH	5.596		
DCH	5.408	ECH	5.609		
DDH	5.42	EDH	5.621		
DEH	5.433	EEH	5.634		
DFH	5.445	EFH	5.646		

van_adj: Set the output voltage for VGMN.

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
10H	-2.709	20H	-2.91	30H	-3.11	40H	-3.31
11H	-2.722	21H	-2.922	31H	-3.122	41H	-3.323
12H	-2.734	22H	-2.935	32H	-3.135	42H	-3.335
13H	-2.747	23H	-2.947	33H	-3.147	43H	-3.348

14H	-2.759	24H	-2.96	34H	-3.16	44H	-3.36
15H	-2.772	25H	-2.972	35H	-3.173	45H	-3.373
16H	-2.784	26H	-2.985	36H	-3.185	46H	-3.385
17H	-2.797	27H	-2.997	37H	-3.198	47H	-3.398
18H	-2.81	28H	-3.01	38H	-3.21	48H	-3.41
19H	-2.822	29H	-3.022	39H	-3.223	49H	-3.423
1AH	-2.835	2AH	-3.035	3AH	-3.235	4AH	-3.435
1BH	-2.847	2BH	-3.047	3BH	-3.248	4BH	-3.448
1CH	-2.86	2CH	-3.06	3CH	-3.26	4CH	-3.461
1DH	-2.872	2DH	-3.072	3DH	-3.273	4DH	-3.473
1EH	-2.885	2EH	-3.085	3EH	-3.285	4EH	-3.486
1FH	-2.897	2FH	-3.097	3FH	-3.298	4FH	-3.498

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
50H	-3.511	60H	-3.711	70H	-3.911	80H	-4.112
51H	-3.523	61H	-3.724	71H	-3.924	81H	-4.124
52H	-3.536	62H	-3.736	72H	-3.936	82H	-4.137
53H	-3.548	63H	-3.749	73H	-3.949	83H	-4.149
54H	-3.561	64H	-3.761	74H	-3.962	84H	-4.162
55H	-3.573	65H	-3.774	75H	-3.974	85H	-4.174
56H	-3.586	66H	-3.786	76H	-3.987	86H	-4.187
57H	-3.598	67H	-3.799	77H	-3.999	87H	-4.2
58H	-3.611	68H	-3.811	78H	-4.012	88H	-4.212
59H	-3.623	69H	-3.824	79H	-4.024	89H	-4.225
5AH	-3.636	6AH	-3.836	7AH	-4.037	8AH	-4.237
5BH	-3.648	6BH	-3.849	7BH	-4.049	8BH	-4.25
5CH	-3.661	6CH	-3.861	7CH	-4.062	8CH	-4.262
5DH	-3.673	6DH	-3.874	7DH	-4.074	8DH	-4.275
5EH	-3.686	6EH	-3.886	7EH	-4.087	8EH	-4.287
5FH	-3.698	6FH	-3.899	7FH	-4.099	8FH	-4.3

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
90H	-4.312	A0H	-4.513	B0H	-4.713	C0H	-4.913
91H	-4.325	A1H	-4.525	B1H	-4.726	C1H	-4.926
92H	-4.337	A2H	-4.538	B2H	-4.738	C2H	-4.939
93H	-4.35	A3H	-4.55	B3H	-4.751	C3H	-4.951
94H	-4.362	A4H	-4.563	B4H	-4.763	C4H	-4.964
95H	-4.375	A5H	-4.575	B5H	-4.776	C5H	-4.976
96H	-4.387	A6H	-4.588	B6H	-4.788	C6H	-4.989
97H	-4.4	A7H	-4.6	B7H	-4.801	C7H	-5.001
98H	-4.412	A8H	-4.613	B8H	-4.813	C8H	-5.014
99H	-4.425	A9H	-4.625	B9H	-4.826	C9H	-5.026
9AH	-4.438	AAH	-4.638	BAH	-4.838	CAH	-5.039
9BH	-4.45	ABH	-4.65	BBH	-4.851	CBH	-5.051

9CH	-4.463	ACH	-4.663	BCH	-4.863	CCH	-5.064
9DH	-4.475	ADH	-4.676	BDH	-4.876	CDH	-5.076
9EH	-4.488	AEH	-4.688	BEH	-4.888	CEH	-5.089
9FH	-4.5	AFH	-4.701	BFH	-4.901	CFH	-5.101

van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)	van_adj[7:0] (Hex)	VGMN (V)
D0H	-5.114	E0H	-5.314	F0H	-5.515
D1H	-5.126	E1H	-5.327		
D2H	-5.139	E2H	-5.339		
D3H	-5.151	E3H	-5.352		
D4H	-5.164	E4H	-5.364		
D5H	-5.177	E5H	-5.377		
D6H	-5.189	E6H	-5.389		
D7H	-5.202	E7H	-5.402		
D8H	-5.214	E8H	-5.414		
D9H	-5.227	E9H	-5.427		
DAH	-5.239	EAH	-5.44		
DBH	-5.252	EBH	-5.452		
DCH	-5.264	ECH	-5.465		
DDH	-5.277	EDH	-5.477		
DEH	-5.289	EEH	-5.49		
DFH	-5.302	EFH	-5.502		

vcom_adj: Set the output voltage for VCOM.

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
10H	-0.3875	20H	-0.5875	30H	-0.7875	40H	-0.9875
11H	-0.4000	21H	-0.6000	31H	-0.8000	41H	-1.0000
12H	-0.4125	22H	-0.6125	32H	-0.8125	42H	-1.0125
13H	-0.4250	23H	-0.6250	33H	-0.8250	43H	-1.0250
14H	-0.4375	24H	-0.6375	34H	-0.8375	44H	-1.0375
15H	-0.4500	25H	-0.6500	35H	-0.8500	45H	-1.0500
16H	-0.4625	26H	-0.6625	36H	-0.8625	46H	-1.0625
17H	-0.4750	27H	-0.6750	37H	-0.8750	47H	-1.0750
18H	-0.4875	28H	-0.6875	38H	-0.8875	48H	-1.0875
19H	-0.5000	29H	-0.7000	39H	-0.9000	49H	-1.1000
1AH	-0.5125	2AH	-0.7125	3AH	-0.9125	4AH	-1.1125
1BH	-0.5250	2BH	-0.7250	3BH	-0.9250	4BH	-1.1250
1CH	-0.5375	2CH	-0.7375	3CH	-0.9375	4CH	-1.1375
1DH	-0.5500	2DH	-0.7500	3DH	-0.9500	4DH	-1.1500
1EH	-0.5625	2EH	-0.7625	3EH	-0.9625	4EH	-1.1625
1FH	-0.5750	2FH	-0.7750	3FH	-0.9750	4FH	-1.1750

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)

50H	-1.1875	60H	-1.3875	70H	-1.5875	80H	-1.7875
51H	-1.2000	61H	-1.4000	71H	-1.6000	81H	-1.8000
52H	-1.2125	62H	-1.4125	72H	-1.6125	82H	-1.8125
53H	-1.2250	63H	-1.4250	73H	-1.6250	83H	-1.8250
54H	-1.2375	64H	-1.4375	74H	-1.6375	84H	-1.8375
55H	-1.2500	65H	-1.4500	75H	-1.6500	85H	-1.8500
56H	-1.2625	66H	-1.4625	76H	-1.6625	86H	-1.8625
57H	-1.2750	67H	-1.4750	77H	-1.6750	87H	-1.8750
58H	-1.2875	68H	-1.4875	78H	-1.6875	88H	-1.8875
59H	-1.3000	69H	-1.5000	79H	-1.7000	89H	-1.9000
5AH	-1.3125	6AH	-1.5125	7AH	-1.7125	8AH	-1.9125
5BH	-1.3250	6BH	-1.5250	7BH	-1.7250	8BH	-1.9250
5CH	-1.3375	6CH	-1.5375	7CH	-1.7375	8CH	-1.9375
5DH	-1.3500	6DH	-1.5500	7DH	-1.7500	8DH	-1.9500
5EH	-1.3625	6EH	-1.5625	7EH	-1.7625	8EH	-1.9625
5FH	-1.3750	6FH	-1.5750	7FH	-1.7750	8FH	-1.9750

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
90H	-1.9875	A0H	-2.1875	B0H	-2.3875	C0H	-2.5875
91H	-2.0000	A1H	-2.2000	B1H	-2.4000	C1H	-2.6000
92H	-2.0125	A2H	-2.2125	B2H	-2.4125	C2H	-2.6125
93H	-2.0250	A3H	-2.2250	B3H	-2.4250	C3H	-2.6250
94H	-2.0375	A4H	-2.2375	B4H	-2.4375	C4H	-2.6375
95H	-2.0500	A5H	-2.2500	B5H	-2.4500	C5H	-2.6500
96H	-2.0625	A6H	-2.2625	B6H	-2.4625	C6H	-2.6625
97H	-2.0750	A7H	-2.2750	B7H	-2.4750	C7H	-2.6750
98H	-2.0875	A8H	-2.2875	B8H	-2.4875	C8H	-2.6875
99H	-2.1000	A9H	-2.3000	B9H	-2.5000	C9H	-2.7000
9AH	-2.1125	AAH	-2.3125	BAH	-2.5125	CAH	-2.7125
9BH	-2.1250	ABH	-2.3250	BBH	-2.5250	CBH	-2.7250
9CH	-2.1375	ACH	-2.3375	BCH	-2.5375	CCH	-2.7375
9DH	-2.1500	ADH	-2.3500	BDH	-2.5500	CDH	-2.7500
9EH	-2.1625	AEH	-2.3625	BEH	-2.5625	CEH	-2.7625
9FH	-2.1750	AFH	-2.3750	BFH	-2.5750	CFH	-2.7750

vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)	vcom_adj[7:0] (Hex)	VCOM (V)
D0H	-2.7875	E0H	-2.9875	F0H	-3.1875
D1H	-2.8000	E1H	-3.0000		
D2H	-2.8125	E2H	-3.0125		
D3H	-2.8250	E3H	-3.0250		
D4H	-2.8375	E4H	-3.0375		
D5H	-2.8500	E5H	-3.0500		
D6H	-2.8625	E6H	-3.0625		
D7H	-2.8750	E7H	-3.0750		
D8H	-2.8875	E8H	-3.0875		
D9H	-2.9000	E9H	-3.1000		

DAH	-2.9125	EAH	-3.1125		
DBH	-2.9250	EBH	-3.1250		
DCH	-2.9375	ECH	-3.1375		
DDH	-2.9500	EDH	-3.1500		
DEH	-2.9625	EEH	-3.1625		
DFH	-2.9750	EFH	-3.1750		

vcom2_adj: Set the output voltage for VCOM when power down.

Note: 00h~0Fh and F1h~FFh of vap[7:0]、van[7:0] and vcom_adj[7:0] are not allowed to be configured

5.3.4. PADCTRL1: 48H

Address	PADCTRL1								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
48H	0	0	vcom_hiz	0	sdo_oe	ledpwm_oe	te_oe	te1_oe	0fH

vcom_hiz：Set VCOM Hi-Z state when disable.H: enable;L: disable.

sdo_oe：sdo output enable.0: Hi-Z;1:output.

te1_oe：te1 pad outout enable.0: Hi-Z;1: output.

te_oe：te pad outout enable.0:Hi-Z;1: output.

ledpwm_oe：ledpwm pad outout enable.0: Hi-Z;1:output.

5.3.5. BOOST_CTRL1~2：80h~81h

Address	BOOST_CTRL1~2								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
80h	0	0	boostm[1:0]		0	0	0	0	10H
81h	0	0	drvn[1:0]		0	0	drvp[1:0]		11H

Description

boostm[1:0]: It is used to select power mode.

BOOSTM[1]	BOOSTM[0]	Mode
0	1	Mode-8, External VSP and VSN
1	0	Mode-3, Power IC

drvn[1:0] : Driving capacity of DC2DCN driver.

DRVN[1:0]	Driving Capability of DC2DCN Driver
00	Level 1 (weak)
01	Level 2 (default)
10	Level 3
11	Level 4 (strong)

drvp[1:0]: Driving capacity of D2DCP driver.

DRVP[1:0]	Driving Capability of DC2DCP Driver
00	Level 1 (weak)
01	Level 2 (default)
10	Level 3
11	Level 4 (strong)

5.3.6. EXTPW_CTRL1~3:90H~92H

Address	EXTPW_CTRL1~3								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
90H	1	1	1	0	ext_dm_nor[1:0]		ext_dm_pwr[1:0]		e5H
91H	0	ext_clkp_nor_width[2:0]			0	ext_clkp_pwr_width[2:0]			44H
92H	0	ext_clkn_nor_width[2:0]			0	ext_clkn_pwr_width[2:0]			44H

Description

ext_dm_nor[1:0]: External power IC mode Pump ratio setting at normal display.

ext_dm_nor[1:0]	VSP pump ratio
00	1.5xVCI
01	2.0xVCI
10	3.0 xVCI
11	3.0 xVCI

ext_dm_pwr[1:0]: External power IC mode Pump ratio setting at power on region.

ext_dm_pwr[1:0]	VSP pump ratio
00	1.5xVCI
01	2.0xVCI
10	3.0 xVCI

11	3.0 xVCI

ext_clkp_nor_width[2:0]: External Power IC clkp ratio setting when normal display.

ext_clkp_nor_width[2:0]	CLK Frequency	ext_clkp_nor_width[2:0]	CLK Frequency
000	1/16 times	100	1 times
001	1/8 times	101	2 times
010	1/4 times	110	4 times
011	1/2 times	111	8 times

ext_clkp_pwr_width[2:0]: External Power IC clkp ratio setting when power on region.

ext_clkp_pwr_width[2:0]	CLK Frequency	ext_clkp_pwr_width[2:0]	CLK Frequency
000	1/16 times	100	1 times
001	1/8 times	101	2 times
010	1/4 times	110	4 times
011	1/2 times	111	8 times

ext_clkn_nor_width[2:0]: External Power IC clkn ratio setting when normal display.

ext_clkn_nor_width[2:0]	CLK Frequency	ext_clkn_nor_width[2:0]	CLK Frequency
000	1/16 times	100	1 times
001	1/8 times	101	2 times
010	1/4 times	110	4 times
011	1/2 times	111	8 times

ext_clkn_pwr_width[2:0]: External Power IC clkn ratio setting when power on region.

ext_clkn_pwr_width[2:0]	CLK Frequency	ext_clkn_pwr_width[2:0]	CLK Frequency
000	1/16 times	100	1 times
001	1/8 times	101	2 times
010	1/4 times	110	4 times
011	1/2 times	111	8 times

5.3.7. PUMP_CTRL1~4:98H~9BH

<table>
<tr><th>Address</th><th colspan="9">PUMP_CTRL1~4</th></tr>
<tr><td>Parameter Address</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>98H</td><td>vgh_cmp_en</td><td>vgh_amp_en</td><td>vgh_sync</td><td>0</td><td colspan="2">pump_ss_width[1:0]</td><td colspan="2">vgh_sel[1:0]</td><td>4aH</td></tr>
<tr><td>99H</td><td colspan="4">vgh_clk_sel[3:0]</td><td colspan="4">vgh_clamp[3:0]</td><td>54H</td></tr>
<tr><td>9AH</td><td>vgl_cmp_en</td><td>vgl_amp_en</td><td>vgl_sync</td><td>0</td><td>0</td><td>0</td><td colspan="2">vgl_sel[1:0]</td><td>41H</td></tr>
<tr><td>9BH</td><td colspan="4">vgl_clk_sel[3:0]</td><td colspan="4">vgl_clamp[3:0]</td><td>56H</td></tr>
<tr><td>Description</td><td colspan="9">
vgh_cmp_en: VGH pump output clamp using digital mode.
<table>
<tr><th>vgh_cmp_en</th><th>VGH clamp digital mode</th></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table>
vgh_amp_en:VGH pump output clamp using linear mode.
<table>
<tr><th>vgh_amp_en</th><th>VGH clamp linear mode</th></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table>
Note: when vgh_amp_en and vgh_cmp_en are both 1, the VGH pump output clamp will use linear mode as the ouput clamp working mode.

vgh_sync: VGH pump output clamp synchronizes with clock when using digital mode.
<table>
<tr><th>vgh_sync</th><th>VGH clamp synchronize function</th></tr>
<tr><td>0</td><td>Disable</td></tr>
<tr><td>1</td><td>Enable</td></tr>
</table>
pump_ss_width[1:0]: Set the soft start time for HV pumps. The longer soft start time, the smaller peak current when pumps pump up, but the longer time to pump to the work voltage. Adjust the soft start time take into account the trade-off between the peak current when pump and pump time.
<table>
<tr><th>pump_ss_width[1:0]</th><th>Multiple of soft start time to refresh one line time</th></tr>
<tr><td>00</td><td>128 lines</td></tr>
<tr><td>01</td><td>256 lines</td></tr>
<tr><td>10</td><td>512 lines</td></tr>
<tr><td>11</td><td>1024 lines</td></tr>
</table>
vgh_sel[1:0]: set the factor used in the set-up circuits for VGH.
Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.
</td></tr>
</table>

vgh_sel[1:0]	VGH OUTPUT
00	2xVSP
01	3xVSP
10	4xVSP
11	reserved

Note: When vpp_src_selr=1, then the factor will change as follows.

vgh_sel[1:0]	VGH OUTPUT
00	2xVSP
01	3xVSP
10	2xVSP
11	3xVSP

vgh_clk_sel[3:0]: Set the VGH pump's working frequency which is the ratio of the main clock.

vgh_clk_sel[3:0]				VGH pump frequency
0	0	0	0	1/2 times
0	0	0	1	1/4 times
0	0	1	0	1/6 times
0	0	1	1	1/8 times
0	1	0	0	1/10 times
0	1	0	1	1/12 times
0	1	1	0	1/14 times
0	1	1	1	1/16 times
1	0	0	0	1/18 times
1	0	0	1	1/20 times
1	0	1	0	1/22 times
1	0	1	1	1/24 times
1	1	0	0	1/26 times
1	1	0	1	1/28 times
1	1	1	0	1/30 times
1	1	1	1	1/32 times

vgh_clamp[3:0]: Set the VGH pump's clamp level.

vgh_clamp[3:0]				VGH clamp level(V)
0	0	0	0	11.0
0	0	0	1	12.0
0	0	1	0	13.0
0	0	1	1	14.0
0	1	0	0	15.0
0	1	0	1	15.5
0	1	1	0	16.0
0	1	1	1	16.5
1	0	0	0	17.0
1	0	0	1	17.5
1	0	1	0	18.0
1	0	1	1	reserved
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	reserved
1	1	1	1	reserved

Note: When vpp_src_selr=1, then the factor will change as follows.

vgh_clamp_sel[3:0]				VGH clamp level(V)
x	0	0	0	7.5
x	0	0	1	8.0
x	0	1	0	8.5
x	0	1	1	9.0
x	1	0	0	9.5
x	1	0	1	10.0
x	1	1	0	10.5
x	1	1	1	11.0

vgl_cmp_en: VGL pump output clamp using digital mode.

vgl_cmp_en	VGL clamp digital mode
0	Disable
1	Enable

vgl_amp_en: VGL pump output clamp using linear mode.

vgl_amp_en	VGL clamp linear mode
0	Disable
1	Enable

Note: when vgl_amp_en and vgl_cmp_en are both 1, the VGL pump output clamp will use linear mode as the ouput clamp working mode.

vgl_sync: VGL pump output clamp synchronizes with clock when using digital mode.

vgl_sync	VGL clamp synchronize function
0	Disable
1	Enable

vgl_sel[1:0]: set the factor used in the set-up circuits for VGL.

Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

vgl_sel[1:0]	VGL OUTPUT
00	2xVSN
01	3xVSN
10	4xVSN
11	4xVSN

vgl_clk_sel[3:0]: Set the VGL pump's working frequency which is the ratio of main clock.

vgl_clk_sel[3:0]				VGL pump frequency
0	0	0	0	1/2 times
0	0	0	1	1/4 times
0	0	1	0	1/6 times
0	0	1	1	1/8 times
0	1	0	0	1/10 times
0	1	0	1	1/12 times
0	1	1	0	1/14 times
0	1	1	1	1/16 times
1	0	0	0	1/18 times

1	0	0	1	1/20 times
1	0	1	0	1/22 times
1	0	1	1	1/24 times
1	1	0	0	1/26 times
1	1	0	1	1/28 times
1	1	1	0	1/30 times
1	1	1	1	1/32 times

vgl_clamp[3:0]: Set the VGL pump's clamp level.

vgl_clamp[3:0]				VGL clamp level(V)
0	0	0	0	-7.0
0	0	0	1	-7.5
0	0	1	0	-8.0
0	0	1	1	-8.5
0	1	0	0	-9.0
0	1	0	1	-9.5
0	1	1	0	-10.0
0	1	1	1	-11.0
1	0	0	0	-11.5
1	0	0	1	-12.0
1	0	1	0	-12.5
1	0	1	1	-13.0
1	1	0	0	-14.0
1	1	0	1	-14.5
1	1	1	0	-15.0
1	1	1	1	-15.5

5.3.8.LVDS_CTRL0,LVDS_CTRL8:D0H,D7H

Address	LVDS_CTRL0,LVDS_CTRL8								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
D0H	0	0	0	0	0	lvfmt	lvbit	lvds_en	06H
D7H	0	pol_ swap	0	0	lane_swap[3:0]				00H

Description

lvfmt: L:JDEA format H:VESA format.

Lvbit: L:6bit,H:8bit.

lvds_en: L:lvds interface disable,H:lvds interface enable.

pol_swap:polarity selection.(default:1)

pol_swap	LVDS Lane Mapping				
	LVDS_ D0P/N	LVDS_ D1P/N	LVDS_ CLKP/N	LVDS_ D2P/N	LVDS_ D3P/N
0	LVDS_ D0N/P	LVDS_ D1N/P	LVDS_ CLKN/P	LVDS_ D2N/P	LVDS_ D3N/P
1	LVDS_ D0P/N	LVDS_ D1P/N	LVDS_ CLKP/N	LVDS_ D2P/N	LVDS_ D3P/N

lane_swap[3:0]:lane swap selection.(default:0010)

lane_swap[3:0]				LVDS_D0	LVDS_D1	LVDS_CLK	LVDS_D2	LVDS_D3
0	0	0	0	D3	D2	CLK	D1	D0
0	0	0	1	D3	CLK	D2	D1	D0
0	0	1	0	D0	D1	CLK	D2	D3
0	0	1	1	D0	D1	D2	CLK	D3
0	1	0	0	CLK	D0	D1	D2	D3
0	1	0	1	CLK	D3	D2	D1	D0
0	1	1	0	D3	D2	D1	D0	CLK
0	1	1	1	D0	D1	D2	D3	CLK
1	0	0	0	D3	D0	CLK	D1	D2
1	0	0	1	D2	D1	CLK	D0	D3

5.3.9. ENEXTC:FFH

<table>
<tr><th>FFh</th><th colspan="8">ENEXTC</th></tr>
<tr><td>Parameter Address</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FFH</td></tr>
<tr><td>Parameter</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">page[1:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="9">Config page.
Write three times. The first time write 30h, the second time write 52h, the last time write page[1:0]

<table><tr><th>page</th><th>Descriptions</th></tr><tr><td>00</td><td>select page0</td></tr><tr><td>01</td><td>select page1</td></tr><tr><td>10</td><td>select page2</td></tr></table></td></tr>
</table>

Page2 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PGAMVR0	0	↑	1	1	0	1	1	0	0	0	0	B0h	gam_config
	1	↑	1	0	0	vrp0[5:0]						02h	-
PGAMVR1	0	↑	1	1	0	1	1	0	0	0	1	B1h	gam_config
	1	↑	1	0	0	vrp1[5:0]						02h	-
PGAMVR2	0	↑	1	1	0	1	1	0	0	1	0	B2h	gam_config
	1	↑	1	0	0	vrp2[5:0]						02h	-
PGAMVR3	0	↑	1	1	0	1	1	0	0	1	1	B3h	gam_config
	1	↑	1	0	0	vrp3[5:0]						11h	-
PGAMVR4	0	↑	1	1	0	1	1	0	1	0	0	B4h	gam_config
	1	↑	1	0	0	vrp4[5:0]						16h	-
PGAMVR5	0	↑	1	1	0	1	1	0	1	0	1	B5h	gam_config
	1	↑	1	0	0	vrp5[5:0]						34h	-
PGAMPR0	0	↑	1	1	0	1	1	0	1	1	0	B6h	gam_config
	1	↑	1	0	prp0[6:0]							15h	-
PGAMPR1	0	↑	1	1	0	1	1	0	1	1	1	B7h	gam_config
	1	↑	1	0	prp1[6:0]							32h	-
PGAMPK0	0	↑	1	1	0	1	1	1	0	0	0	B8h	gam_config
	1	↑	1	0	0	0	pkp0[4:0]					11h	-
PGAMPK1	0	↑	1	1	0	1	1	1	0	0	1	B9h	gam_config
	1	↑	1	0	0	0	pkp1[4:0]					05h	-
PGAMPK2	0	↑	1	1	0	1	1	1	0	1	0	BAh	gam_config
	1	↑	1	0	0	0	pkp2[4:0]					18h	-
PGAMPK3	0	↑	1	1	0	1	1	1	0	1	1	BBh	gam_config
	1	↑	1	0	0	0	pkp3[4:0]					18h	-
PGAMPK4	0	↑	1	1	0	1	1	1	1	0	0	BCh	gam_config
	1	↑	1	0	0	0	pkp4[4:0]					18h	-
PGAMPK5	0	↑	1	1	0	1	1	1	1	0	1	BDh	gam_config
	1	↑	1	0	0	0	pkp5[4:0]					18h	-
PGAMPK6	0	↑	1	1	0	1	1	1	1	1	0	BEh	gam_config
	1	↑	1	0	0	0	pkp6[4:0]					1ah	-
PGAMPK7	0	↑	1	1	0	1	1	1	1	1	1	BFh	gam_config
	1	↑	1	0	0	0	pkp7[4:0]					0fh	-
PGAMPK8	0	↑	1	1	1	0	0	0	0	0	0	C0h	gam_config

	1	↑	1	0	0	0	pkp8[4:0]					18h	-
Page2 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PGAMPK9	0	↑	1	1	1	0	0	0	0	0	1	C1h	gam_config
	1	↑	1	0	0	0	pkp9[4:0]					09h	-
GAMP0	0	↑	1	1	1	0	0	0	0	1	0	C2h	gam_config
	1	↑	1	0	0	0	gamp0[4:0]					00h	-
NGAMVR0	0	↑	1	1	1	0	1	0	0	0	0	D0h	gam_config
	1	↑	1	0	0	vrn0[5:0]						02h	-
NGAMVR1	0	↑	1	1	1	0	1	0	0	0	1	D1h	gam_config
	1	↑	1	0	0	vrn1[5:0]						02h	-
NGAMVR2	0	↑	1	1	1	0	1	0	0	1	0	D2h	gam_config
	1	↑	1	0	0	vrn2[5:0]						02h	-
NGAMVR3	0	↑	1	1	1	0	1	0	0	1	1	D3h	gam_config
	1	↑	1	0	0	vrn3[5:0]						11h	-
NGAMVR4	0	↑	1	1	1	0	1	0	1	0	0	D4h	gam_config
	1	↑	1	0	0	vrn4[5:0]						16h	-
NGAMVR5	0	↑	1	1	1	0	1	0	1	0	1	D5h	gam_config
	1	↑	1	0	0	vrn5[5:0]						34h	-
NGAMPR0	0	↑	1	1	1	0	1	0	1	1	0	D6h	gam_config
	1	↑	1	0	prn0[6:0]							15h	-
NGAMPR1	0	↑	1	1	1	0	1	0	1	1	1	D7h	gam_config
	1	↑	1	0	prn1[6:0]							32h	-
NGAMPK0	0	↑	1	1	1	0	1	1	0	0	0	D8h	gam_config
	1	↑	1	0	0	0	pkn0[4:0]					11h	-
NGAMPK1	0	↑	1	1	1	0	1	1	0	0	1	D9h	gam_config
	1	↑	1	0	0	0	pkn1[4:0]					05h	-
NGAMPK2	0	↑	1	1	1	0	1	1	0	1	0	DAh	gam_config
	1	↑	1	0	0	0	pkn2[4:0]					18h	-
NGAMPK3	0	↑	1	1	1	0	1	1	0	1	1	DBh	gam_config
	1	↑	1	0	0	0	pkn3[4:0]					18h	-
NGAMPK4	0	↑	1	1	1	0	1	1	1	0	0	DCh	gam_config
	1	↑	1	0	0	0	pkn4[4:0]					18h	-
NGAMPK5	0	↑	1	1	1	0	1	1	1	0	1	DDh	gam_config
	1	↑	1	0	0	0	pkn5[4:0]					18h	-

Page2 command													
Instruction	DCX	WRX	RDX	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NGAMPK6	0	↑	1	1	1	0	1	1	1	1	0	DEh	gam_config
	1	↑	1	0	0	0	pkn6[4:0]					1ah	-
NGAMPK7	0	↑	1	1	1	0	1	1	1	1	1	DFh	gam_config
	1	↑	1	0	0	0	pkn7[4:0]					0fh	-
NGAMPK8	0	↑	1	1	1	1	0	0	0	0	0	E0h	gam_config
	1	↑	1	0	0	0	pkn8[4:0]					18h	-
NGAMPK9	0	↑	1	1	1	1	0	0	0	0	1	E1h	gam_config
	1	↑	1	0	0	0	pkn9[4:0]					09h	-
GAMN0	0	↑	1	1	1	1	0	0	0	1	0	E2h	gam_config
	1	↑	1	0	0	0	gamn0[4:0]					00h	-
ENEXTC	0	↑	1	1	1	1	1	1	1	1	1	FFh	page_ctrl
	1	↑	1	0	0	0	0	0	0	page[1:0]		00h	-

5.3.10. PGAMVR0~5;PGAMPR0~1;PGAMPK0~9;GAMP0:B0H~C2H

Address	PGAMVR0~5;PGAMPR0~1;PGAMPK0~9;GAMP0								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
B0H	0	0	vrp0[5:0]						02H
B1H	0	0	vrp1[5:0]						02H
B2H	0	0	vrp2[5:0]						02H
B3H	0	0	vrp3[5:0]						11H
B4H	0	0	vrp4[5:0]						16H
B5H	0	0	vrp5[5:0]						34H
B6H	0	prp0[6:0]							15H
B7H	0	prp1[6:0]							32H
B8H	0	0	0	pkp0[4:0]					11H
B9H	0	0	0	pkp1[4:0]					05H
BAH	0	0	0	pkp2[4:0]					18H
BBH	0	0	0	pkp3[4:0]					18H
BCH	0	0	0	pkp4[4:0]					18H
BDH	0	0	0	pkp5[4:0]					18H
BEH	0	0	0	pkp6[4:0]					1aH
BFH	0	0	0	pkp7[4:0]					0fH
C0H	0	0	0	pkp8[4:0]					18H
C1H	0	0	0	pkp9[4:0]					09H
C2H	0	0	0	gamp0[4:0]					00H
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.								

5.3.11. NGAMVR0~5;NGAMPR0~1;NGAMPK0~9;GAMN0:D0H~E2H

Address	NGAMVR0~5;NGAMPR0~1;NGAMPK0~9;GAMN0								
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
D0H	0	0	vrn0[5:0]						02H
D1H	0	0	vrn1[5:0]						02H
D2H	0	0	vrn2[5:0]						02H
D3H	0	0	vrn3[5:0]						11H
D4H	0	0	vrn4[5:0]						16H
D5H	0	0	vrn5[5:0]						34H
D6H	0	prn0[6:0]							15H
D7H	0	prn1[6:0]							32H
D8H	0	0	0	pkn0[4:0]					11H
D9H	0	0	0	pkn1[4:0]					05H
DAH	0	0	0	pkn2[4:0]					18H
DBH	0	0	0	pkn3[4:0]					18H
DCH	0	0	0	pkn4[4:0]					18H
DDH	0	0	0	pkn5[4:0]					18H
DEH	0	0	0	pkn6[4:0]					1aH
DFH	0	0	0	pkn7[4:0]					0fH
E0H	0	0	0	pkn8[4:0]					18H
E1H	0	0	0	pkn9[4:0]					09H
E2H	0	0	0	gamn0[4:0]					00H
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.								

5.3.12. ENEXTC:FFH

<table>
<tr><th>FFh</th><th colspan="9">ENEXTC</th></tr>
<tr><td></td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Default</td></tr>
<tr><td>Command</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FFH</td></tr>
<tr><td>Parameter</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">page[1:0]</td><td>00H</td></tr>
<tr><td>Description</td><td colspan="9">Config page.
Write three times. The first time write 30h, the second time write 52h, the last time write page[1:0].
Write three times.The frist time write 30h, the second time write 52h, the last time write the
<table><tr><th>page</th><th>Descriptions</th></tr><tr><td>00</td><td>select page0</td></tr><tr><td>01</td><td>select page1</td></tr><tr><td>10</td><td>select page2</td></tr></table></td></tr>
</table>

6. FUNCTIONS

6.1. Interface Type Selection

NV3051F-L support MIPI 1/2/3/4 Lane, which can be set by the IM[2:0] pins and LANSEL.

Table 6-1, depicts the interface corresponding to IM[2:0] and LANSEL pins.

External Pad Set			Configuration of MIPI Lane				
IM[2]	IM[1]	IM[0]	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P

Table 6-1

6.2. MIPI-DSI Interface

6.2.1. General description

The communication can be separated 2 different levels between the MCU and the display module:

– Interface Level : Low level communication

– Packet level : High level communication

6.2.2. Interface level communication

6.2.2.1. General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven Low Power (LP) or High Speed (HS) mode. Data lane1/2/3 can be driven High Speed mode only.

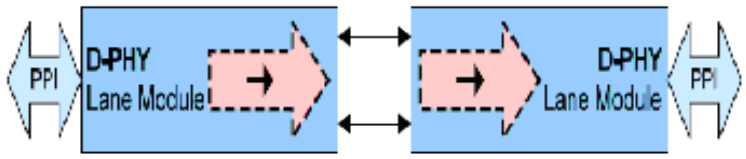
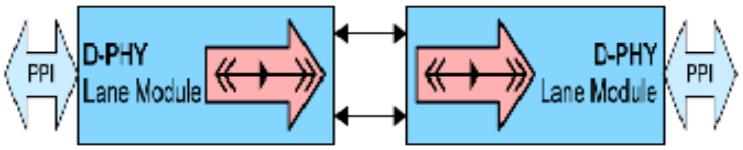
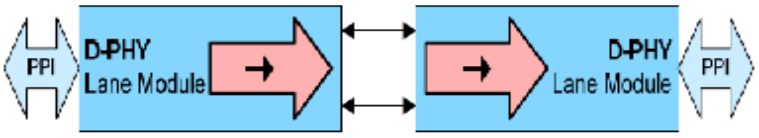
-	Lane support mode	MPU(Host) NV3051F-L(Slave)
Clock Lane	Unidirectional lane • High-Speed Clock only • Simplified Escape Mode (ULPS Only)	
Data Lane0	Bi-directional lane • Forward high-speed only • Bi-directional Escape Mode • Bi-direction LPDT	
Data Lane1/2/3	Unidirectional lane • Forward high-speed only • Simplified Escape Mode (ULPS Only)	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disable (A termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enable) are not used in the single end mode.

There are used different modes and protocols in each mode when there are wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

6.2.2.2. DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.
The principal flow chart of the different clock lanes power modes is illustrated below.

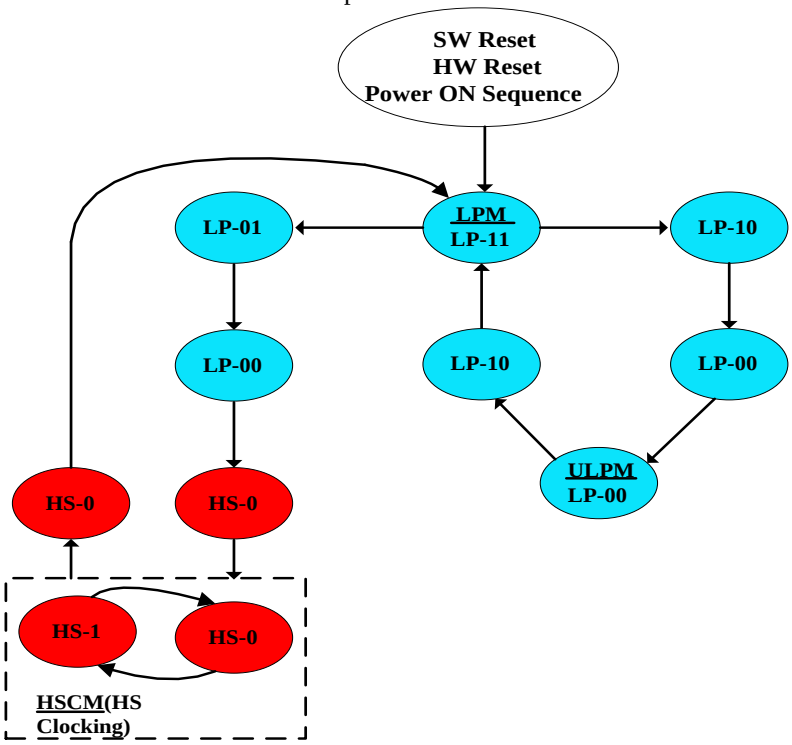


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

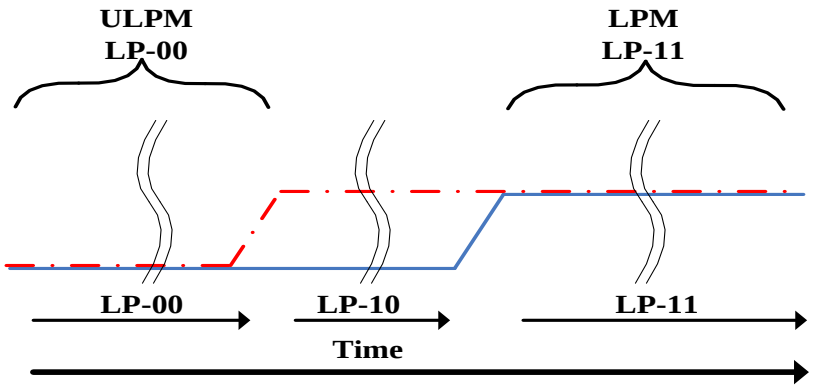


Figure: From ULPM to LPM

3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

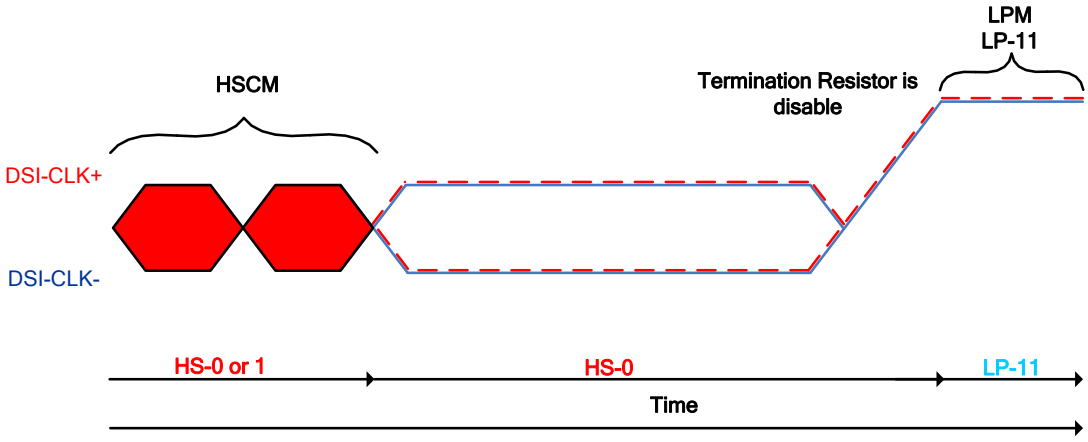


Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

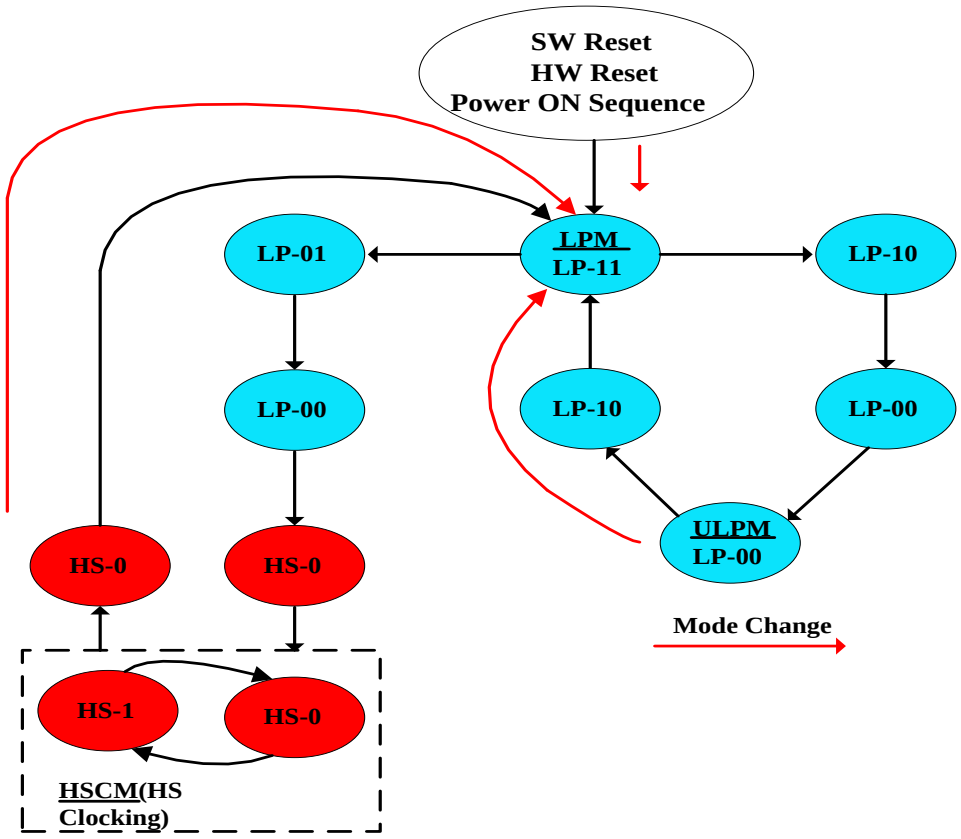


Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

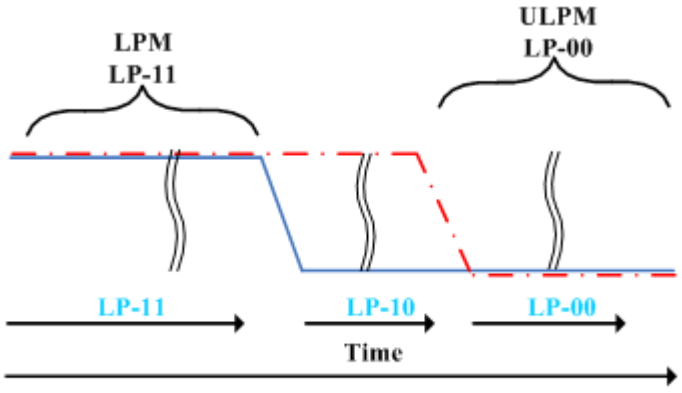


Figure: From LPM to ULPM

The mode change is also illustrated below:

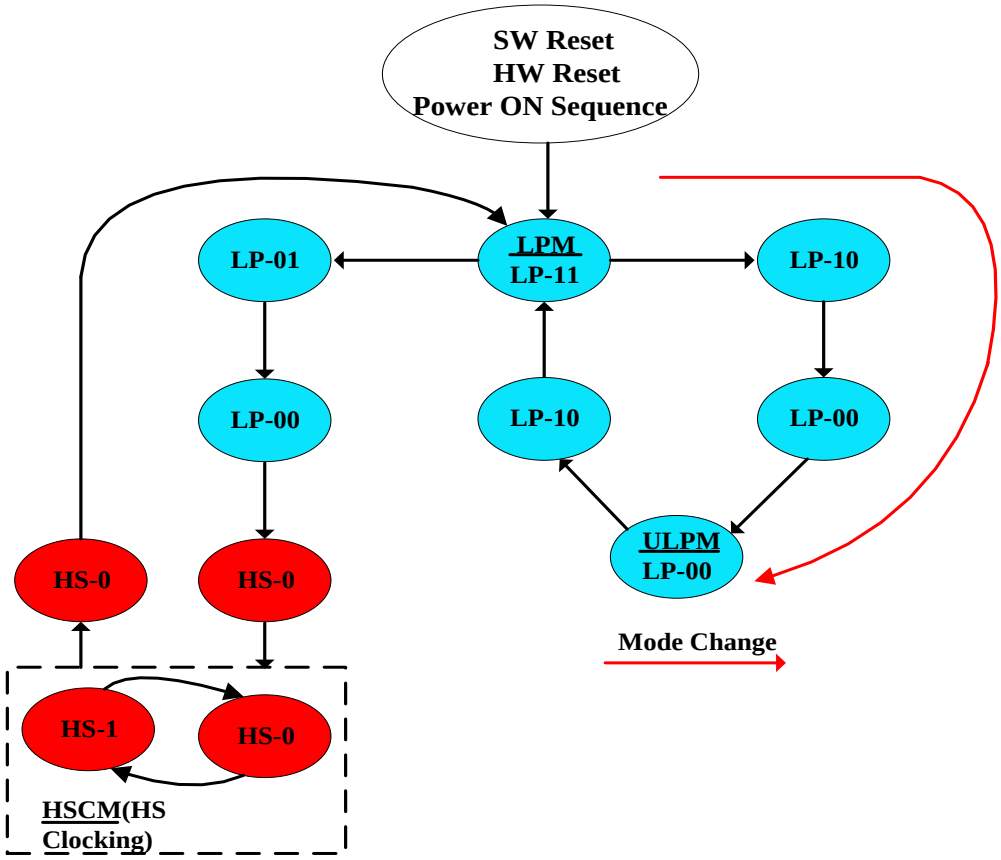


Figure: The mode change from LPM to ULPM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

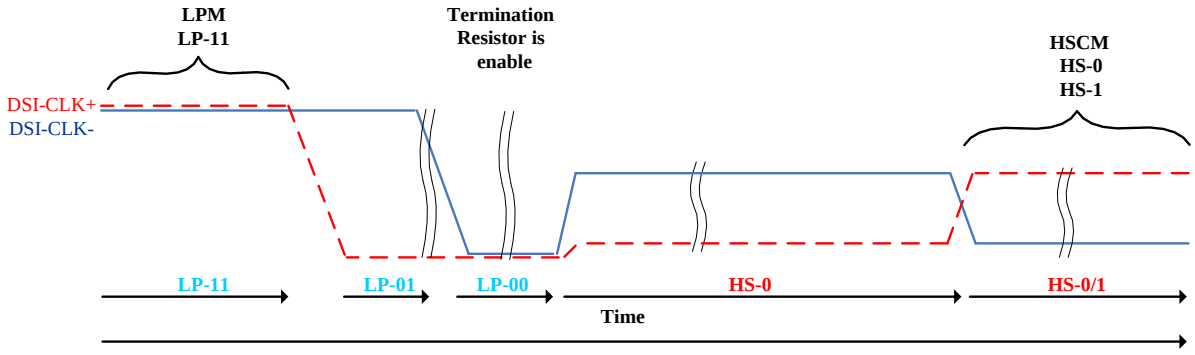


Figure: From LPM to HSCM

The mode change is also illustrated below:

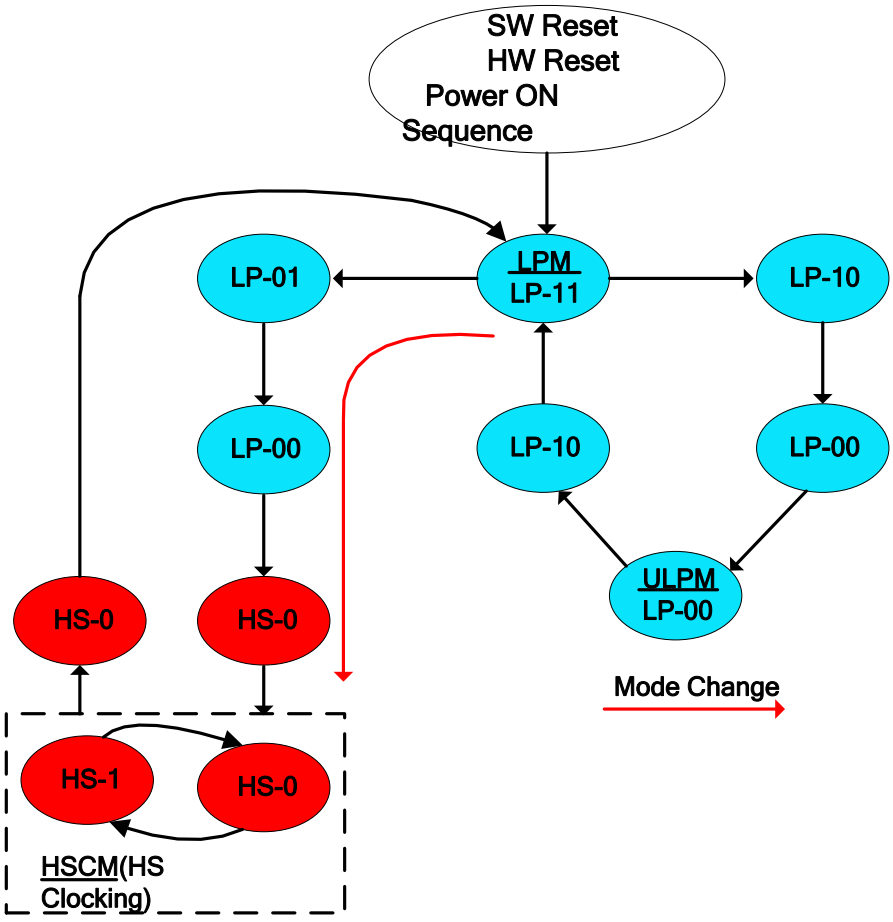


Figure: Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes.

The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

– Even number of transitions
– Start state is HS-0
– End state is HS-0

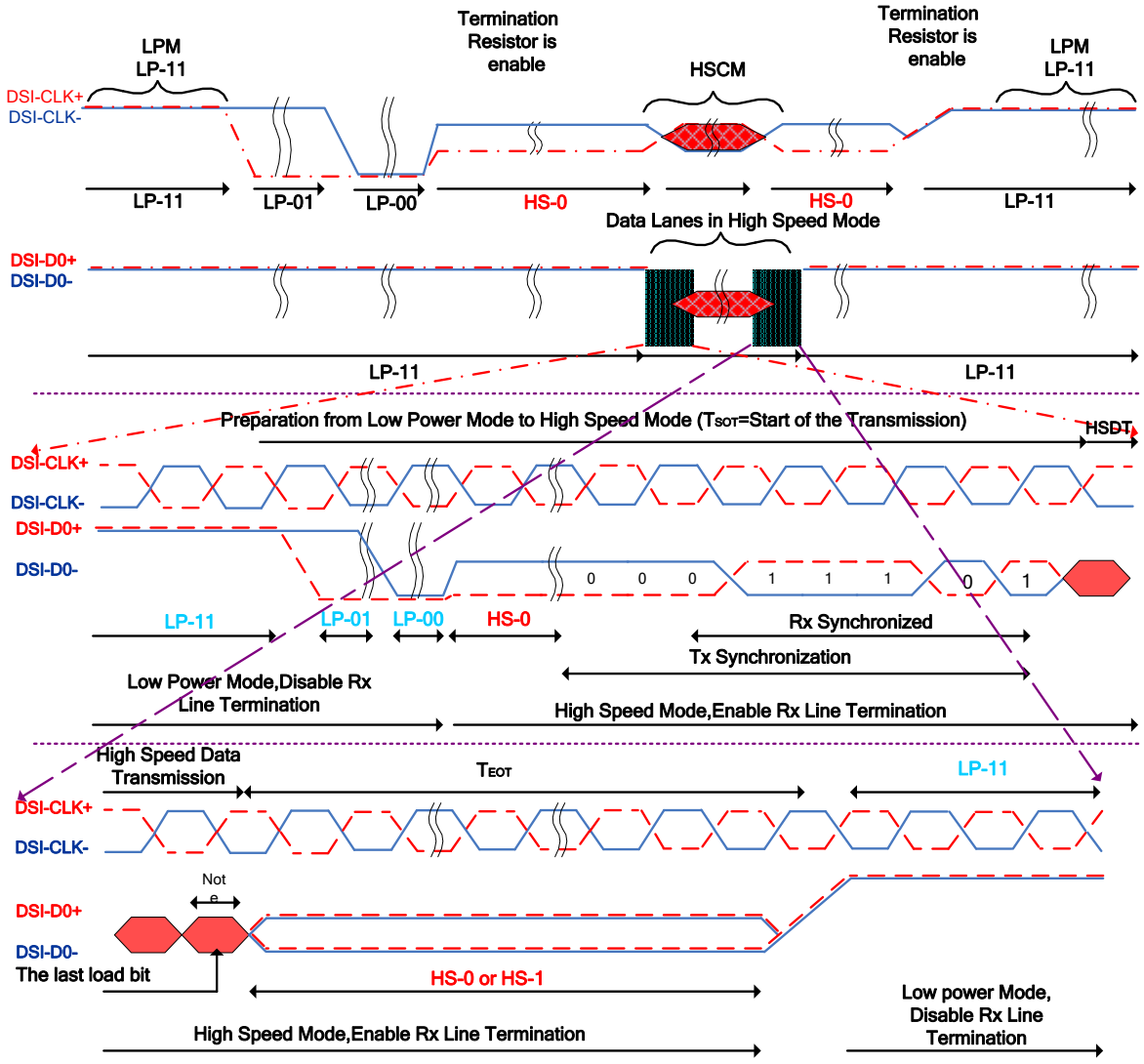


Figure: High speed clock burst

Note:

If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

6.2.3. DSI data lanes

6.2.3.1. General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

6.2.3.2. Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follow

• Start: LP-11

• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit.

• A payload stream if it is needed

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11

• End: LP-11

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action.

All currently available Escape mode commands and actions are list below.

• Send or receive “Low-Power Data Transmission” (LPDT)

• Drive data lanes to “Ultra-Low Power State” (ULPS)

• Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function)
• Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the MCU,

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding.

Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

For Data Lane1 and 2, only support ULPS Escape mode commands.

• Drive data lanes to "Ultra-Low Power State" (ULPS)

The basic construction is illustrated below:

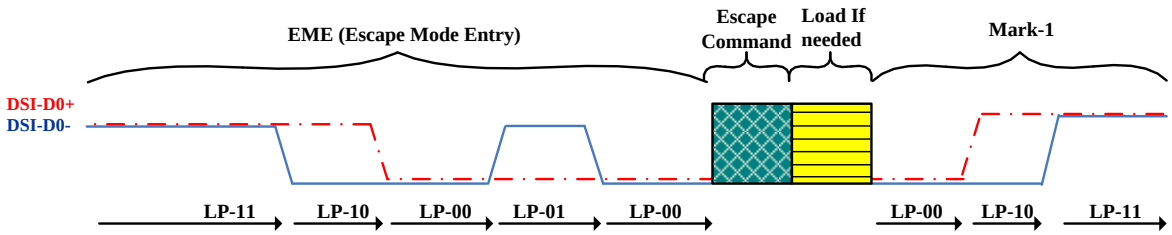


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided 2 different groups: Mode or Trigger. Escape command groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001 bin
Ultra-Low Power Mode	Mode	0001 1110 bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g.

The MCU can inform to the display module that it can put data lanes in the low power mode.

The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module reaches a new V-synch, the display module sent to the MCU a TE trigger (TEE), if the MCU has been requested it.

Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Payload (Data):

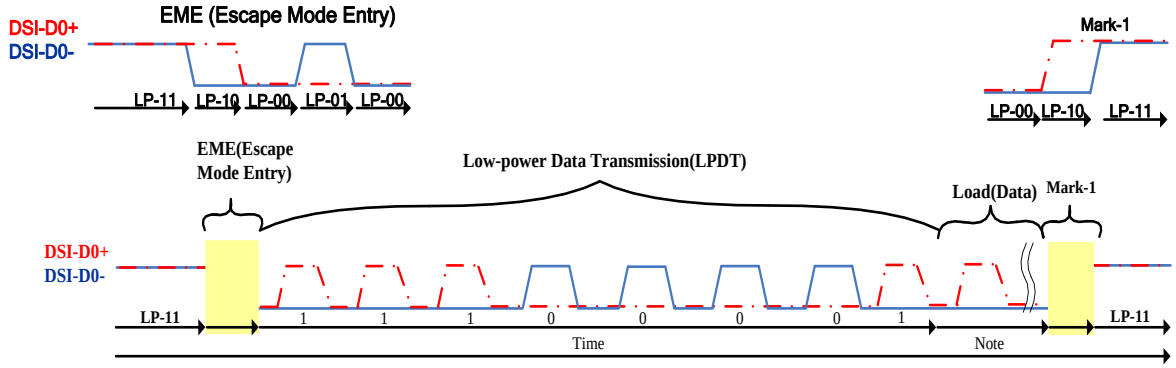
- One or more bytes

- Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:



Note:Load(Data)is presenting that the first bit is logical“1”in this example.

Figure: Low-power data transmission

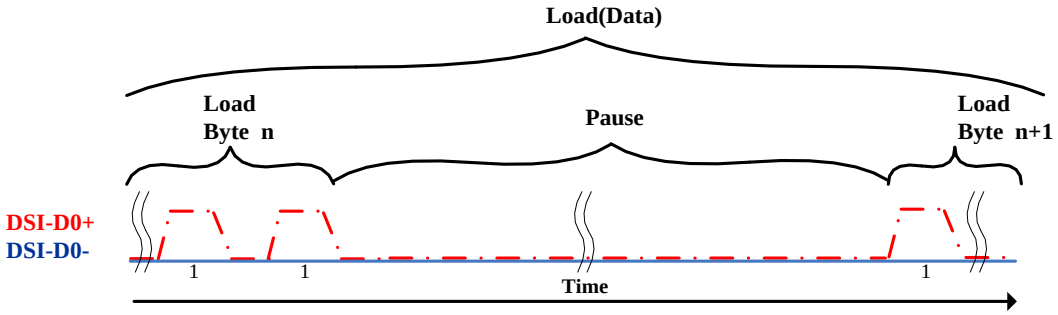


Figure: Pause (example)

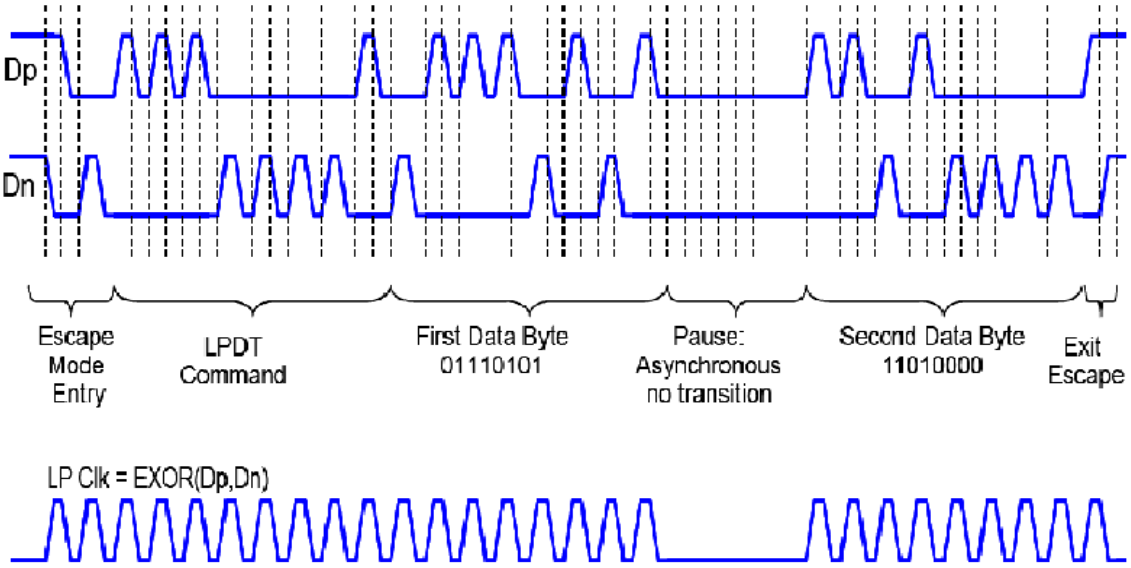


Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

• Start: LP-11

• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)

• Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

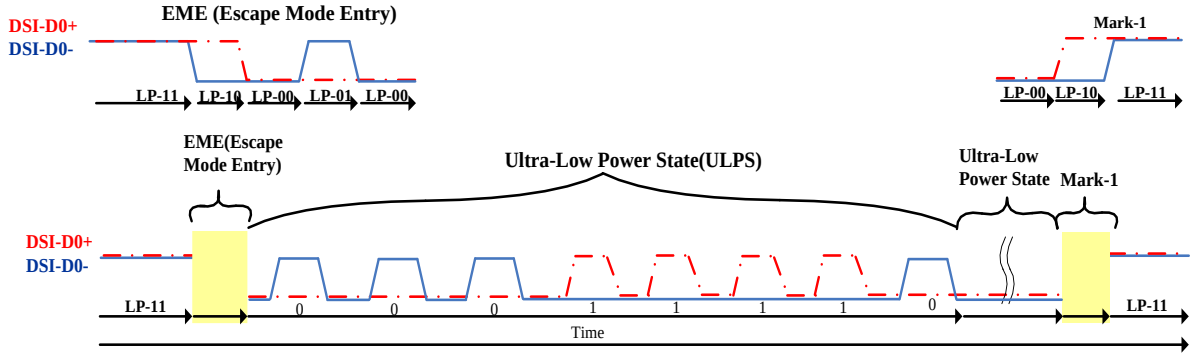


Figure: Ultra-low power state(ULPS)

Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset is using a following sequence:

• Start: LP-11

• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

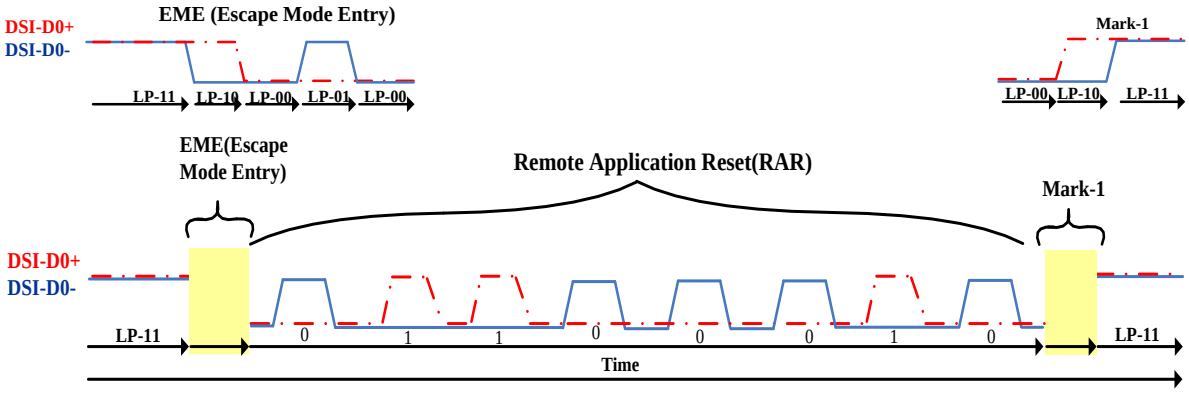


Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform to the MCU when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

• Start: LP-11

• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

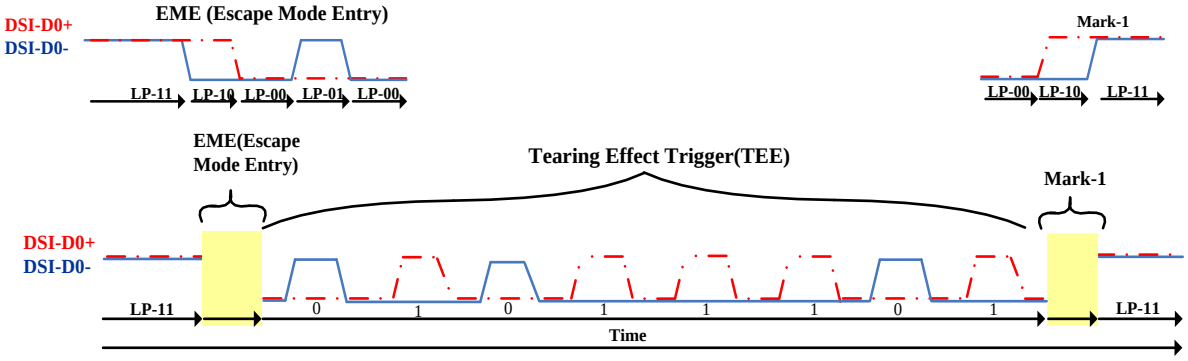


Figure: Tearing effect (TEE)

Acknowledgement (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK). The Acknowledge (ACK) is using a following sequence:

• Start: LP-11

• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

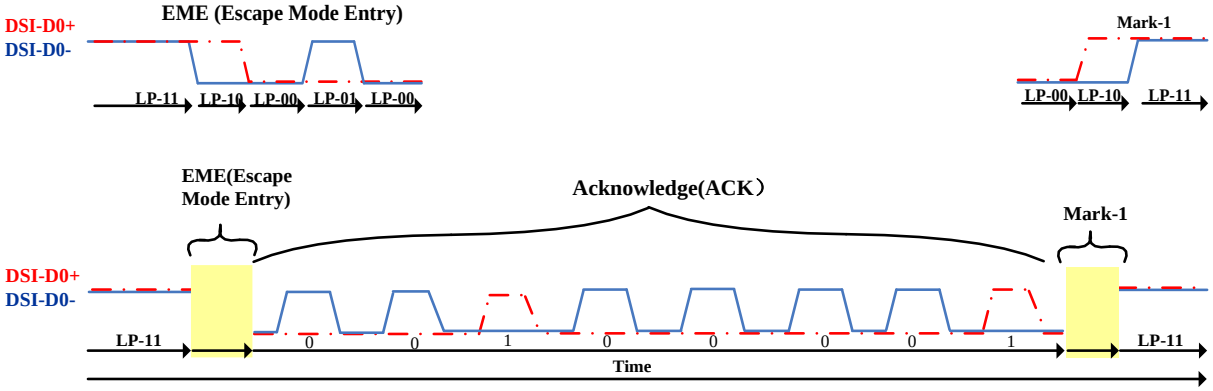


Figure: Acknowledgement (ACK)

6.2.3.3. High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (Tsot of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follows

• Start: LP-11

• HS-Request: LP-01

• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)

• Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)

• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

Preparation from Low Power Mode to High Speed Mode(TSOT=Start of the Transmission)

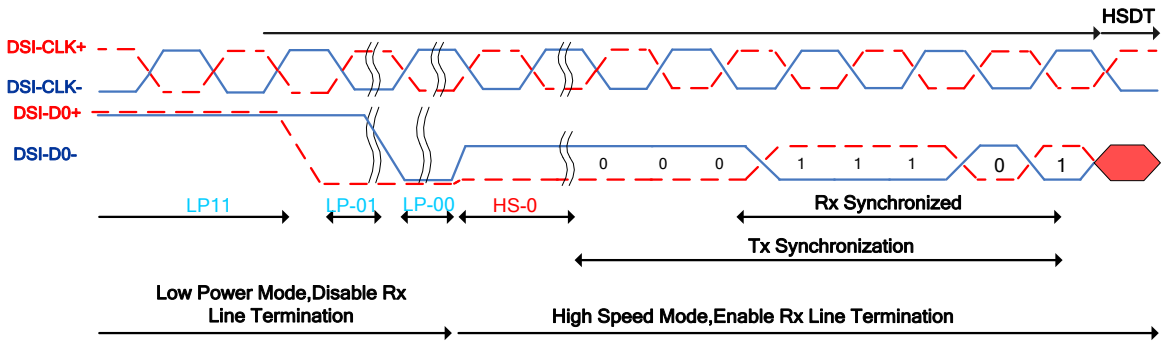


Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes

DSI-D0+/- are in LP-11 mode. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follows

• Start: High-Speed Data Transmission (HSDT)

• Stops High-Speed Data Transmission

-MCU changes to HS-1, if the last load bit is HS-0

-MCU changes to HS-0, if the last load bit is HS-1

• End: LP-11 (Rx: Lane Termination Disable)

This same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

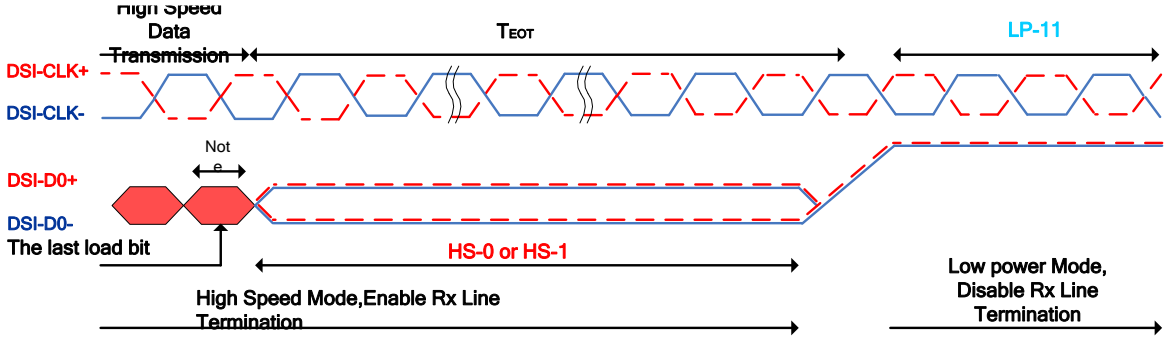


Figure: TEOT of HSDT

Note:

If the last load bit is HS-0,the transmitter changes from HS-0 to HS-1.

If the last load bit is HS-1,the transmitter changes from HS-1 to HS-0.

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (Lpa) or Short (Spa) packets. These packets are defined on chapter “Short Packet (Spa) and Long Packet (Lpa) Structures”.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

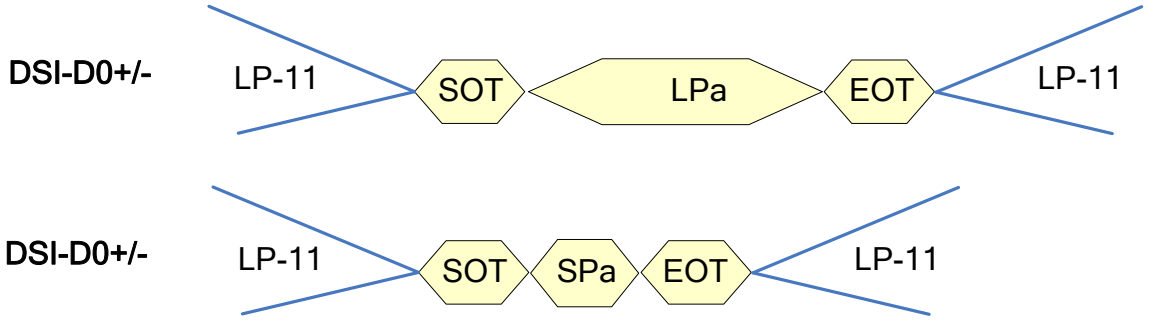


Figure: Single packet in HSDT

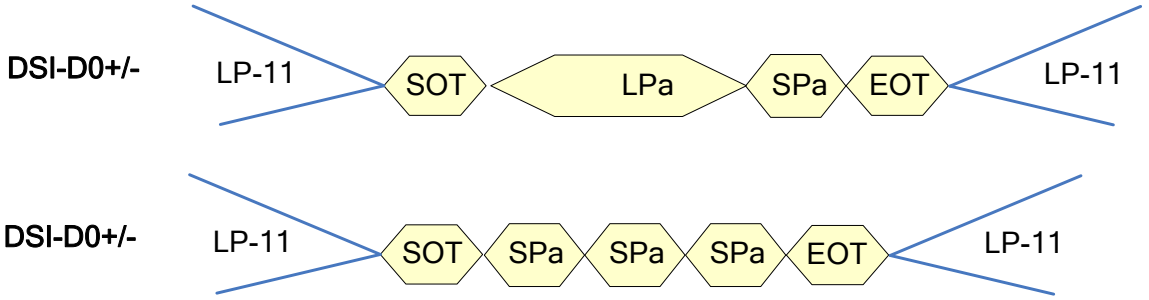


Figure: Multiple packets in HSDT

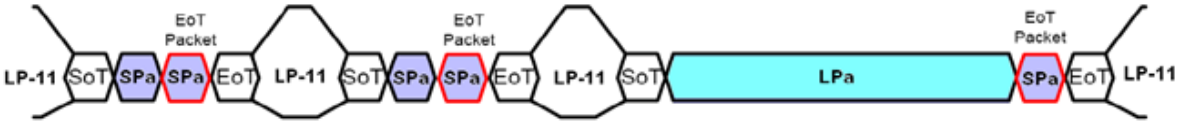


Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SOT	Start of the Transmission
Lpa	Long Packet
Spa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

6.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU and display module are using the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follows.

• Start (MCU): LP-11

• Turnaround Request (MCU): LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00

• The MCU waits until the display module is starting to control DSI-D0+/- data lanes and the MCU stops to control DSI-D0+/- data lanes (= High-Z)

• The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.

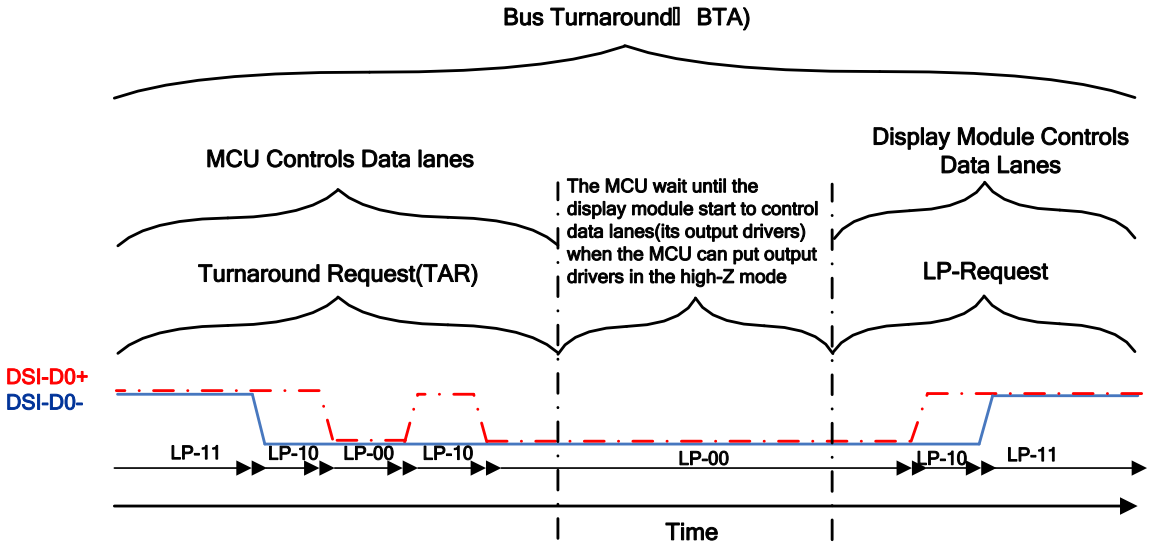


Figure: Bus turnaround procedure

6.2.3.5. Two Data-lane High Speed Transmission

Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of lanes, one lane may run out of data before the other. Therefore, the lane management layer, as it buffers up the final set of less-than-2 bytes, de-asserts its “valid data” signal into all lanes for which there’s no further data.

Although all lanes start simultaneously with parallel SoTs, each lane operates independently and may complete the HS transmission before the other lane, sending an EoT one cycle (byte) earlier.

The two PHYs on the receiving end of the link collect bytes in parallel and feed them into the lane management layer. The lane management layer reconstructs the original sequence of bytes in the transmission.

Below Figure shows the way a HS transmission can terminate for two data-lane HS transmission.

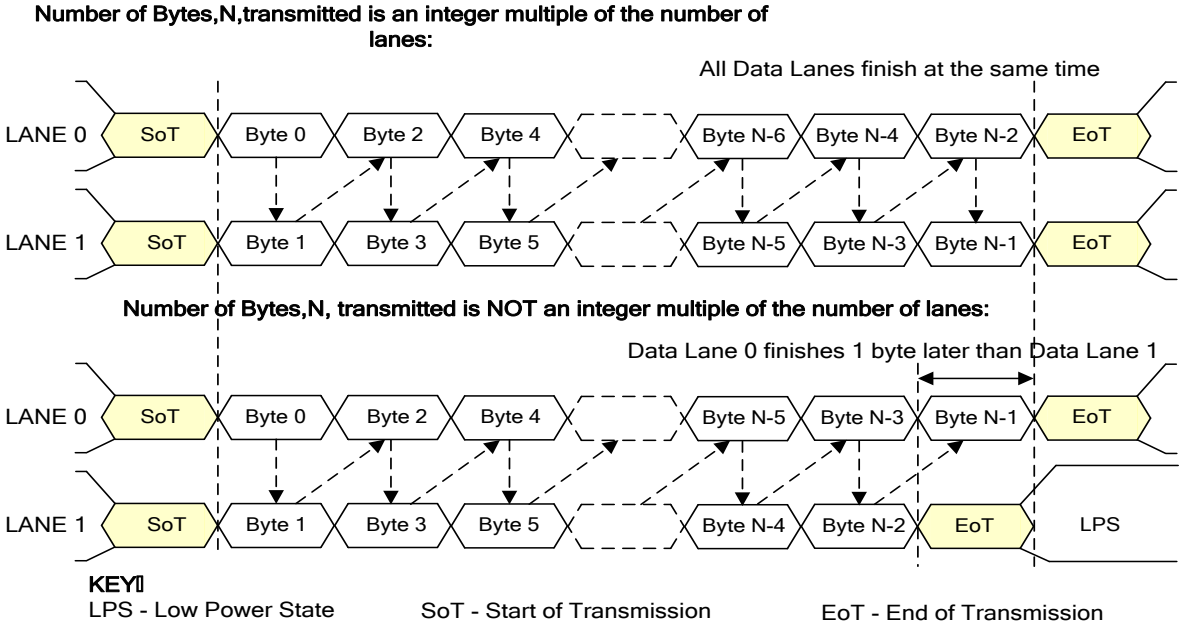


Figure: Two data-lane HS transmission example

6.2.3.6. Three data-lane high speed transmission

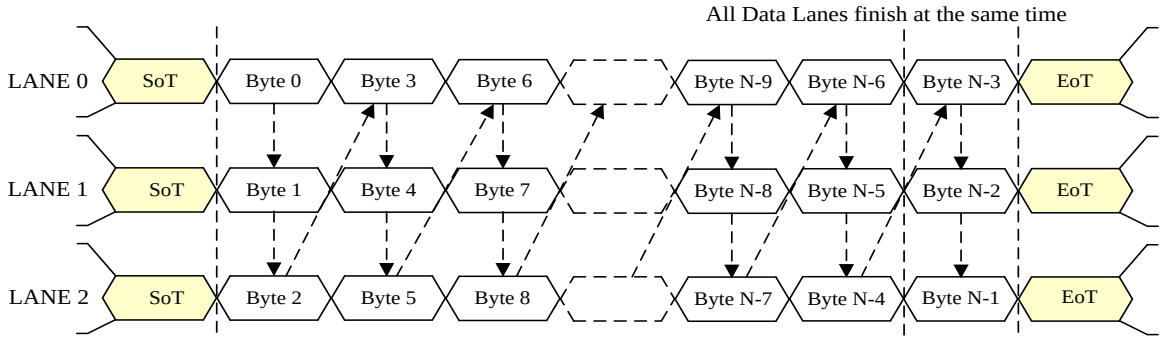
Since a HS transmission is composed of an arbitrary number of bytes that may not be an integer multiple of the number of Lanes, some Lanes may run out of data before others. Therefore, the Lane Management layer, as it buffers up the final set of less-than-N bytes, de-asserts its “valid data” signal into all Lanes for which there is no further data.

Although all Lanes start simultaneously with parallel SoTs, each Lane operates independently and may complete the HS transmission before the other Lanes, sending an EoT one cycle (byte) earlier.

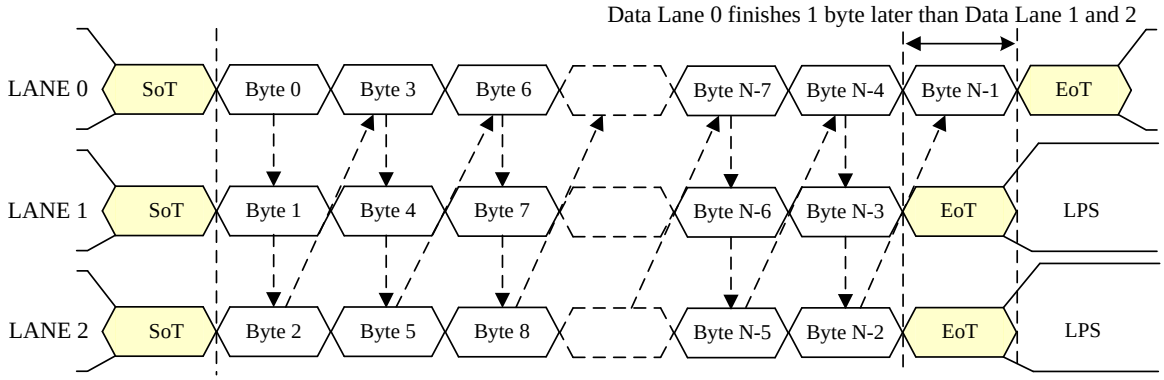
The N PHYs on the receiving end of the Link collect bytes in parallel and feed them into the Lane Management layer. The Lane Management layer reconstructs the original sequence of bytes in the transmission.

Below Figure illustrate a variety of ways a HS transmission can terminate for different number of Lanes and packet lengths.

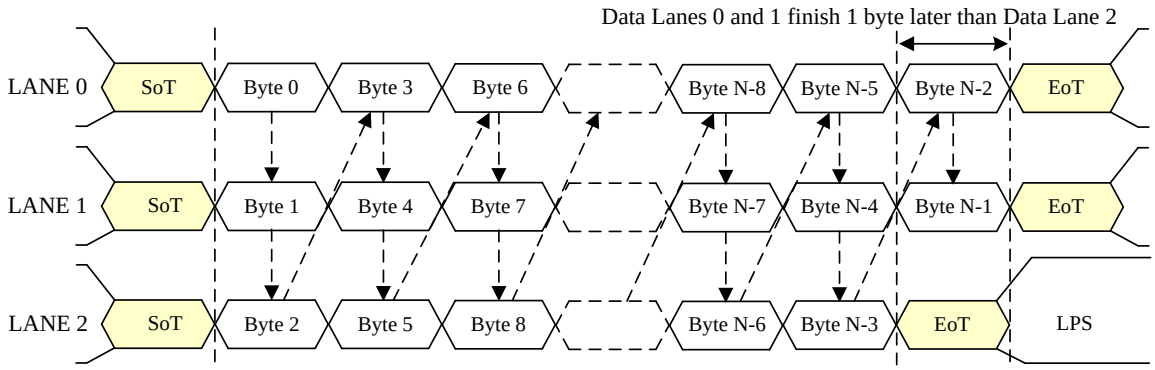
Number of Bytes,N,transmitted is an integer multiple of the number of lanes:



Number of Bytes,N,transmitted is NOT an integer multiple of the number of lanes（Example 1):



Number of Bytes,N,transmitted is NOT an integer multiple of the number of lanes(Example 2):



6.2.4. Packet level communication

6.2.4.1. Short Packet (Spa) and Long Packet (Lpa) structures

Short Packet (Spa) and Long Packet (Lpa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are

- Short Packet (Spa): 4 bytes
- Long Packet (Lpa): From 6 to 65,541 bytes

The type (Spa or Lpa) of the packet can be recognized from their package headers (PH).

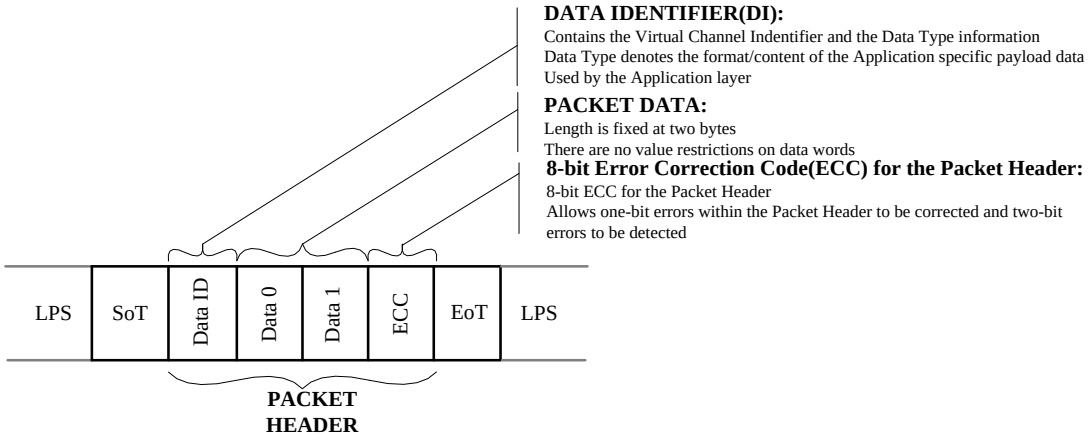


Figure: Short packet structure

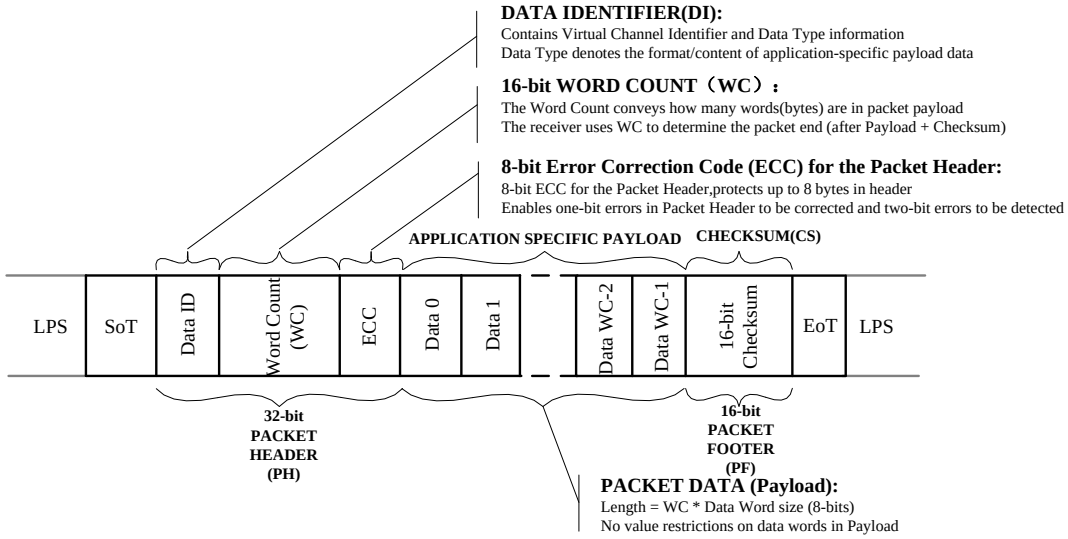


Figure: Long packet structure

Note: “Short Packet (Spa) Structure” and “Long Packet (Lpa) Structure” are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

• LP-11 =>SoT =>Spa =>Lpa =>Spa =>Spa =>EoT =>LP-11

• LP-11 =>SoT =>Spa =>Spa =>Spa =>EoT =>LP-11

• LP-11 =>SoT =>Lpa =>Lpa =>Lpa =>EoT =>LP-11

Bit Order of the Byte on Packets

All packet data traverses the interface as bytes. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified.

Below Figure shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation,i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

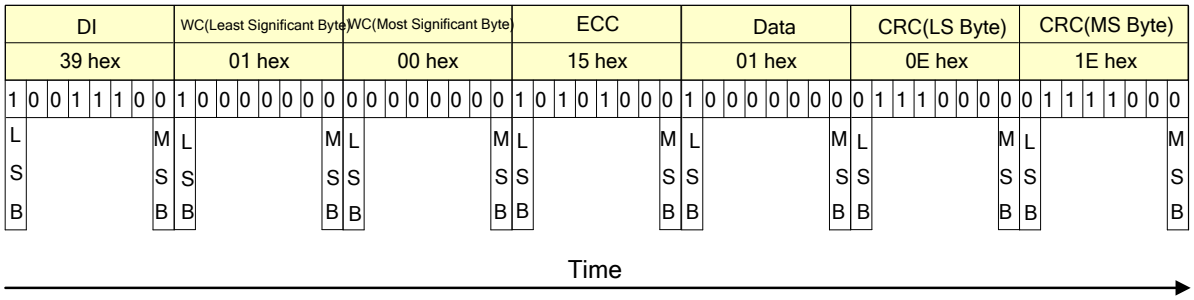


Figure: Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. E.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last. This same order is illustrated for reference purposes below.

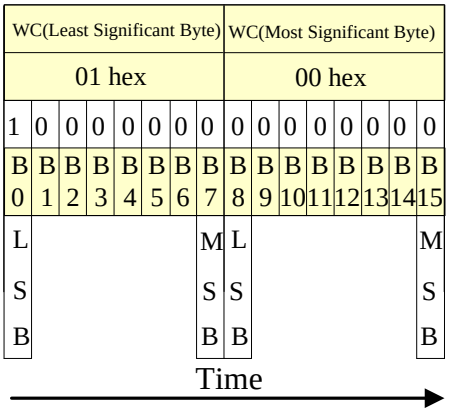


Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (Spa) or Long Packet (Lpa).

Short Packet (Spa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (Spa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

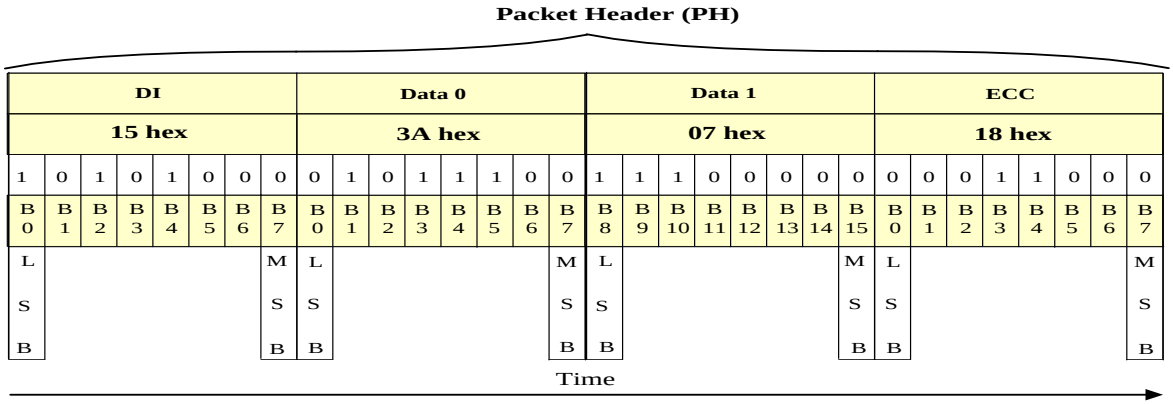


Figure: Packet head on short packet

Long Packet (Lpa):

• 1st byte: Data Identification (DI) => Identification that this is Long Packet (Lpa)

• 2nd and 3rd bytes: Word Count (WC)

• 4th byte: Error Correction Code (ECC)

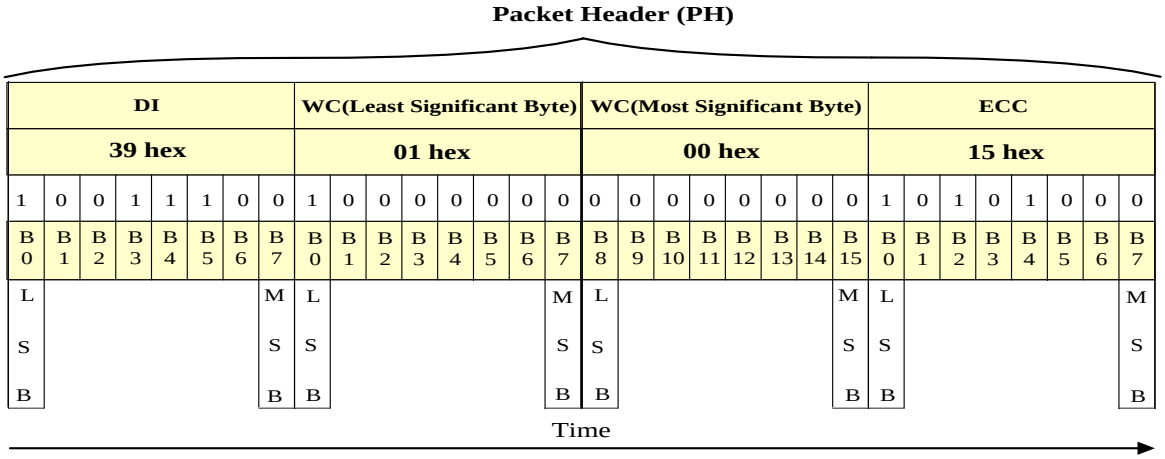


Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

• Virtual Channel (VC), 2 bits, DI[7...6]

• Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

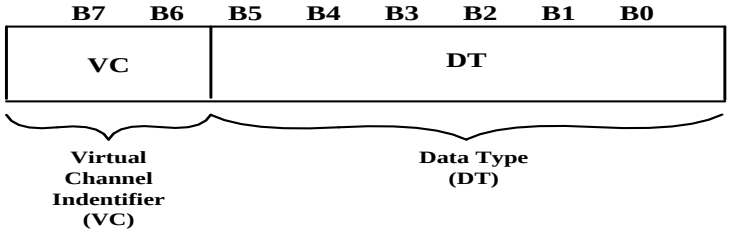


Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

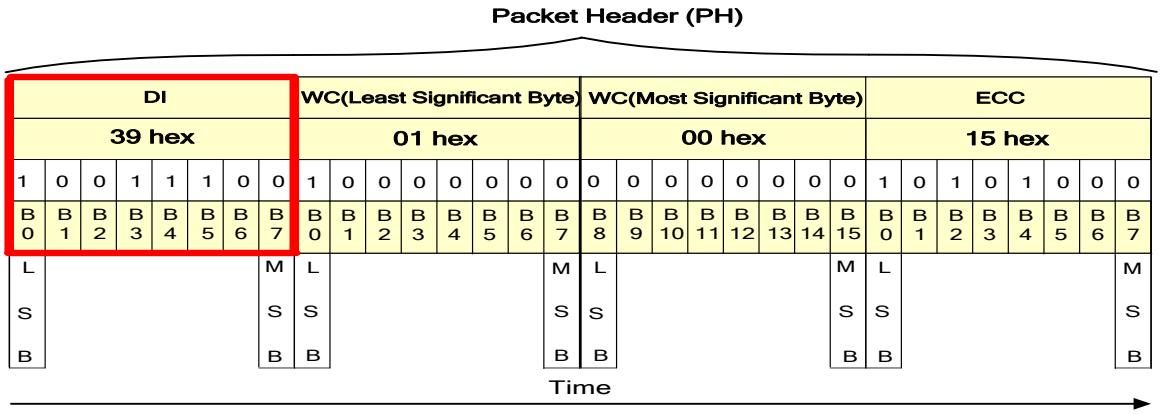


Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

NV3051F-L only support VC code=00, package with other VC code(01/10/11) will be filter out.

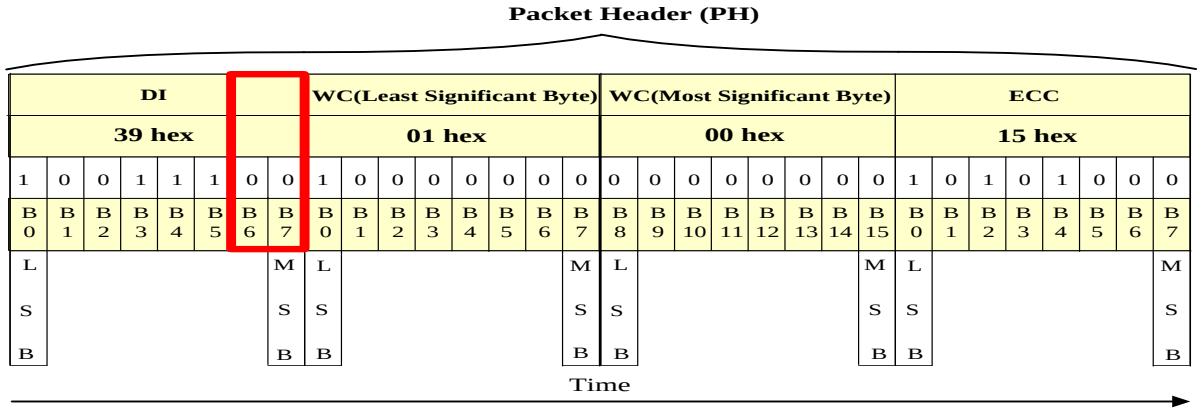


Figure: Virtual channel on the packet head

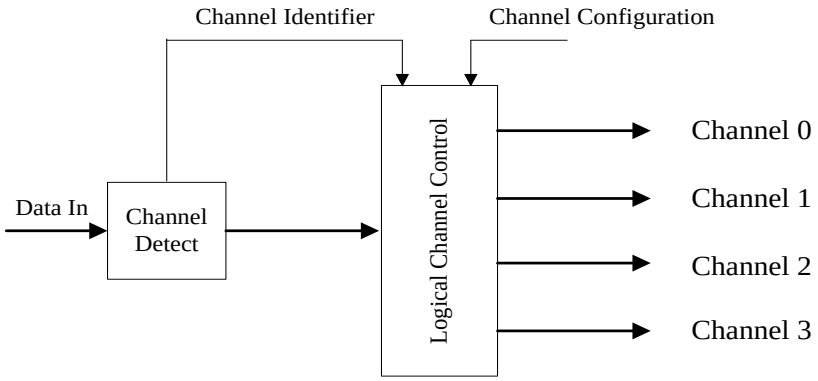


Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

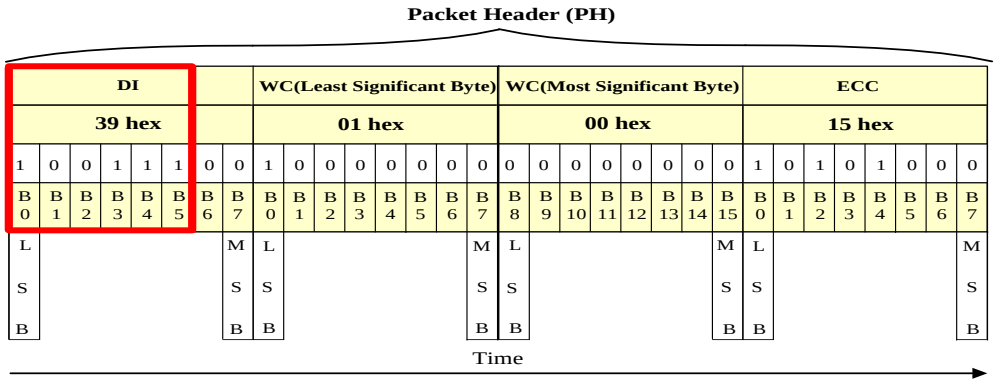


Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (Spa) or Long Packet (Lpa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

From the MCU to the Display module		
Data Type(HEX)	Data Type(Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT) packet
02h	00 0010	Color Mode (CM) Off Command
12h	01 0010	Color Mode (CM) On Command
22h	10 0010	Shut Down Peripheral Command
32h	11 0010	Turn On Peripheral Command
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data

19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
0Eh	00 1110	Packet Pixel Stream, 16-bit RGB, 5-6-5 Format
2Eh	10 1110	Loosely Packet Pixel Stream, 18-bit RGB, 6-6-6 Format
3Eh	11 1110	Packet Pixel Stream, 24-bit RGB, 8-8-8 Format

Table: Data type from the MCU to the display module

From the Display Module to the MCU		
Data Type(HEX)	Data Type(Binary)	Description
02h	00 0010	Acknowledge & Error Report
11h	01 0001	Generic Short READ Response, 1 byte returned
21h	10 0001	DCS Short READ Response, 1 byte returned

Table: Data type from the display module to the MCU

The receiver is ignored other Data Type (DT) if they are not defined on tables above. Host send “Generic Read” data type, NV3051F-L will return DCS Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (Spa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (Spa) is wanted to send.

Packet Data (PD) of the Short Packet (Spa) consists of 2 data bytes: Data 0 and Data 1.

Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to 00h, if the information length is 1 byte.

Packet Data (PD) of the Short Packet (Spa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

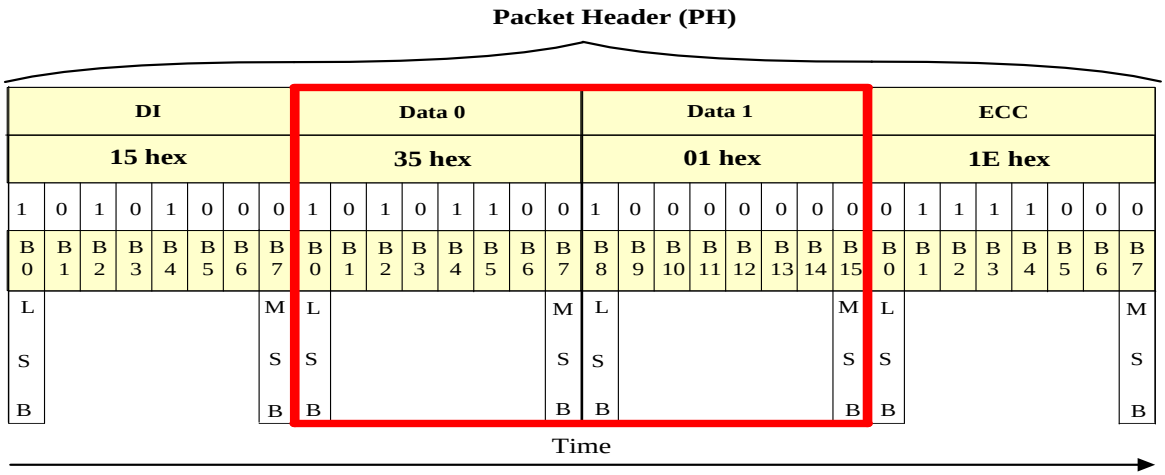


Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

• Data 0: 10hex

• Data 1: 00hex (Null)

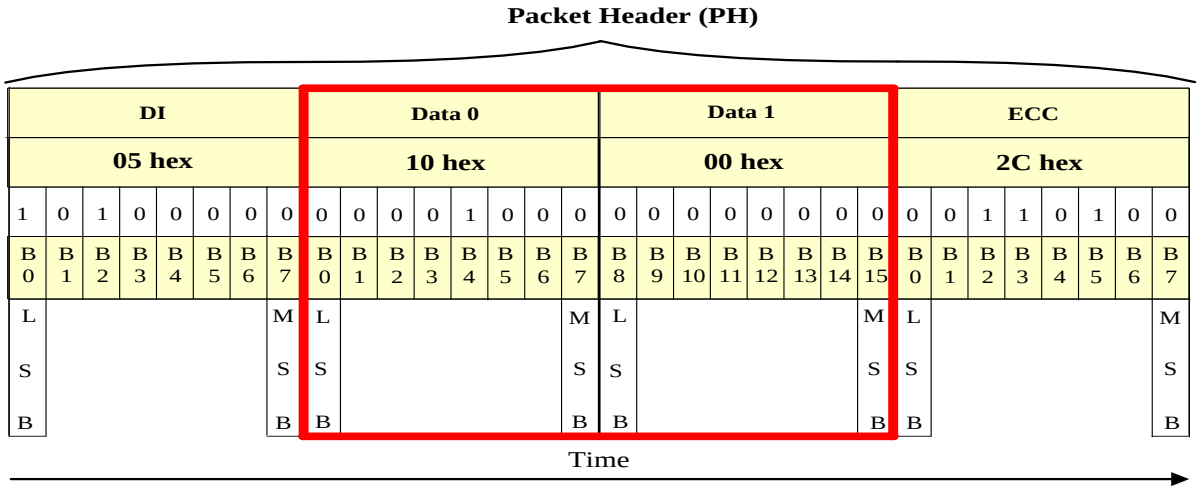


Figure: Packet data on the short packet, 1 bytes information

Word count on the long packet

Word Count (WC) of the Long Packet (Lpa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (Lpa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (Spa) is placed in the Packet Header (PH).

Word Count (WC) of the Long Packet (Lpa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (Lpa) is illustrated for reference purposes below.

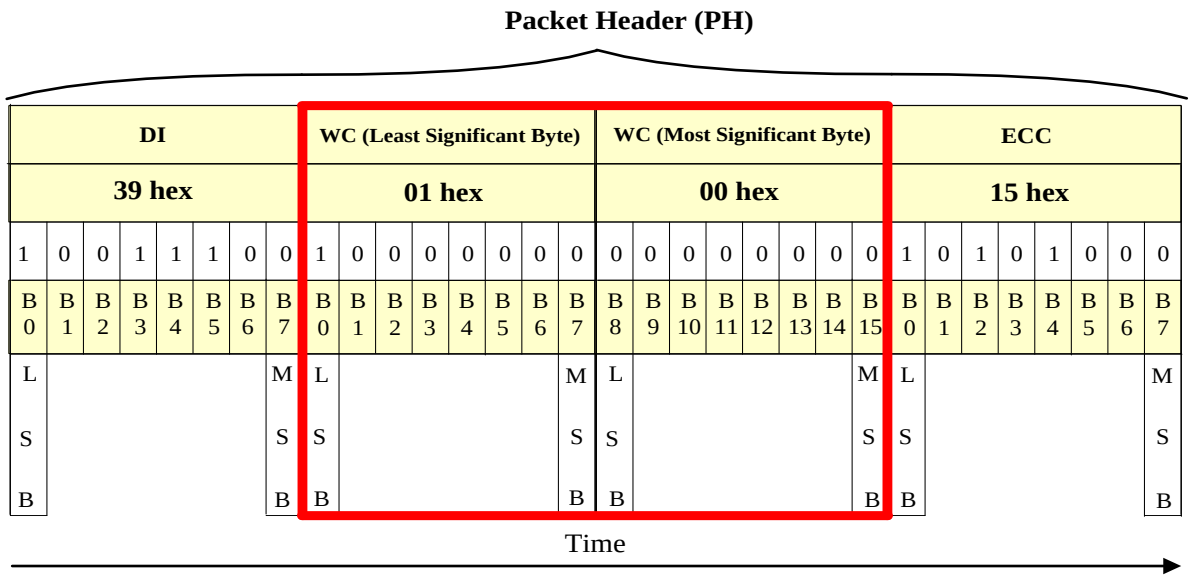


Figure: Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

• Short Packet (Spa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])

• Long Packet (Lpa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.

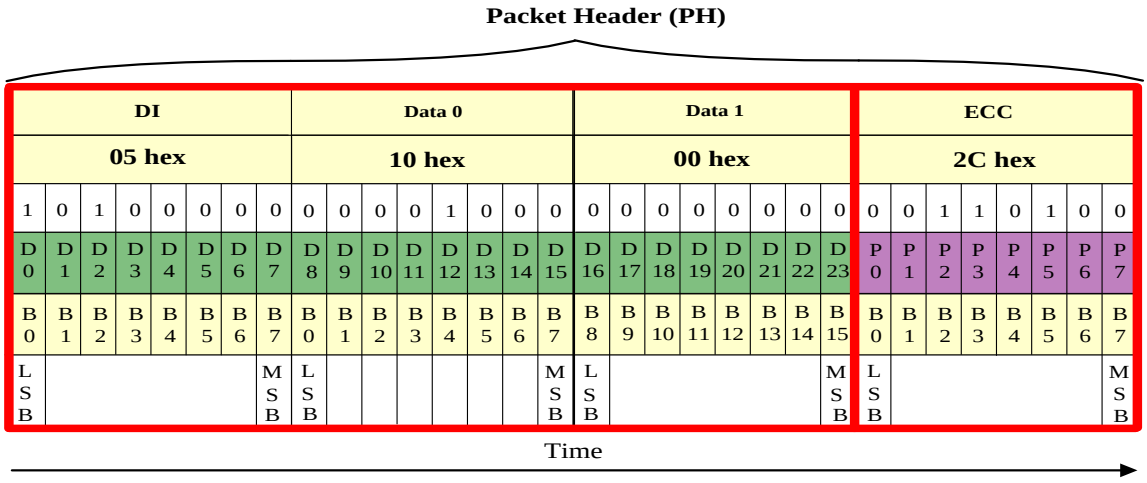


Figure: D[23:0] and P[7:0] on the short packet

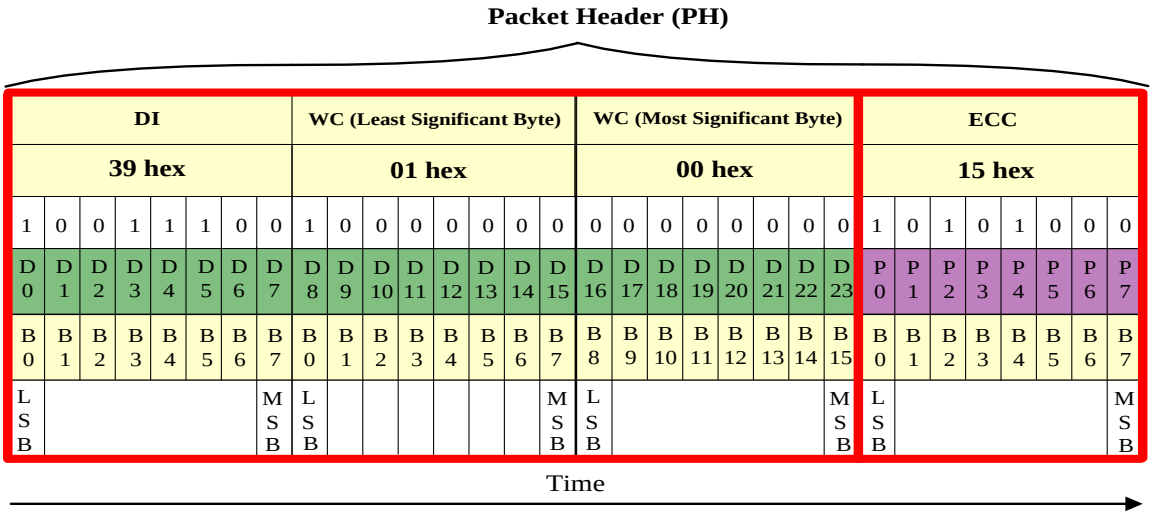


Figure: D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

• P7 = 0

• P6 = 0

• P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

• P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

• P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

• P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

• P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

• P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

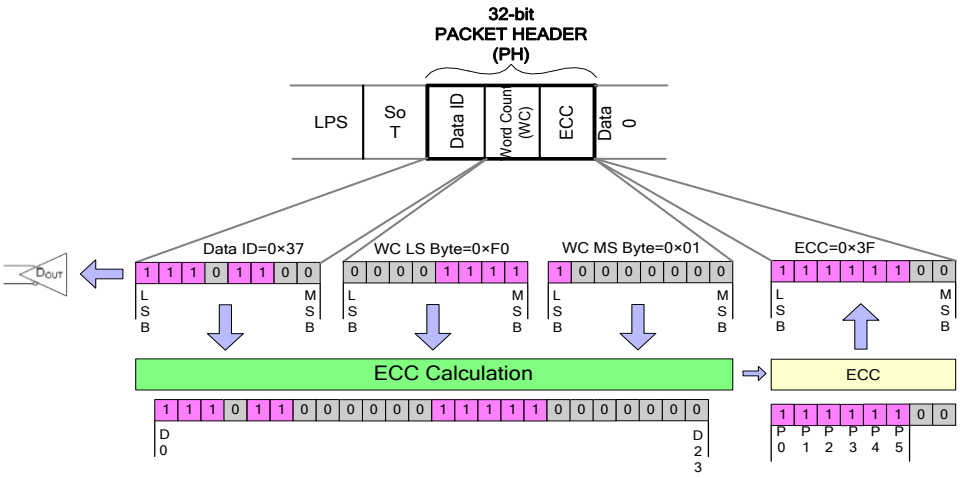


Figure: 24-bit ECC generation on TX side (Example)

Packet footer on the long packet

Packet Footer (PF) of the Long Packet (Lpa) is defined after the Packet Data (PD) of the Long Packet (Lpa).

The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (Lpa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

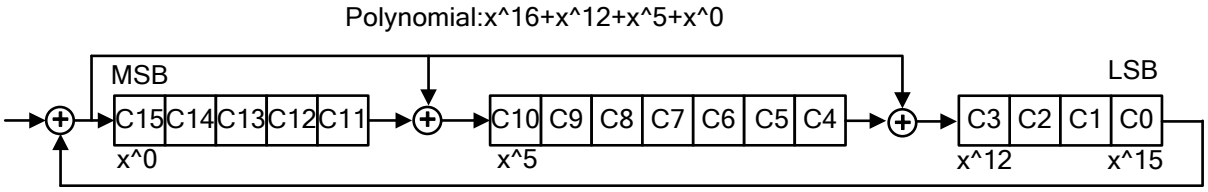


Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations.

The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer(PF) are not equal.

6.2.4.2. Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module.

This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (Spa) and Long packet (Lpa) as these are illustrated below.

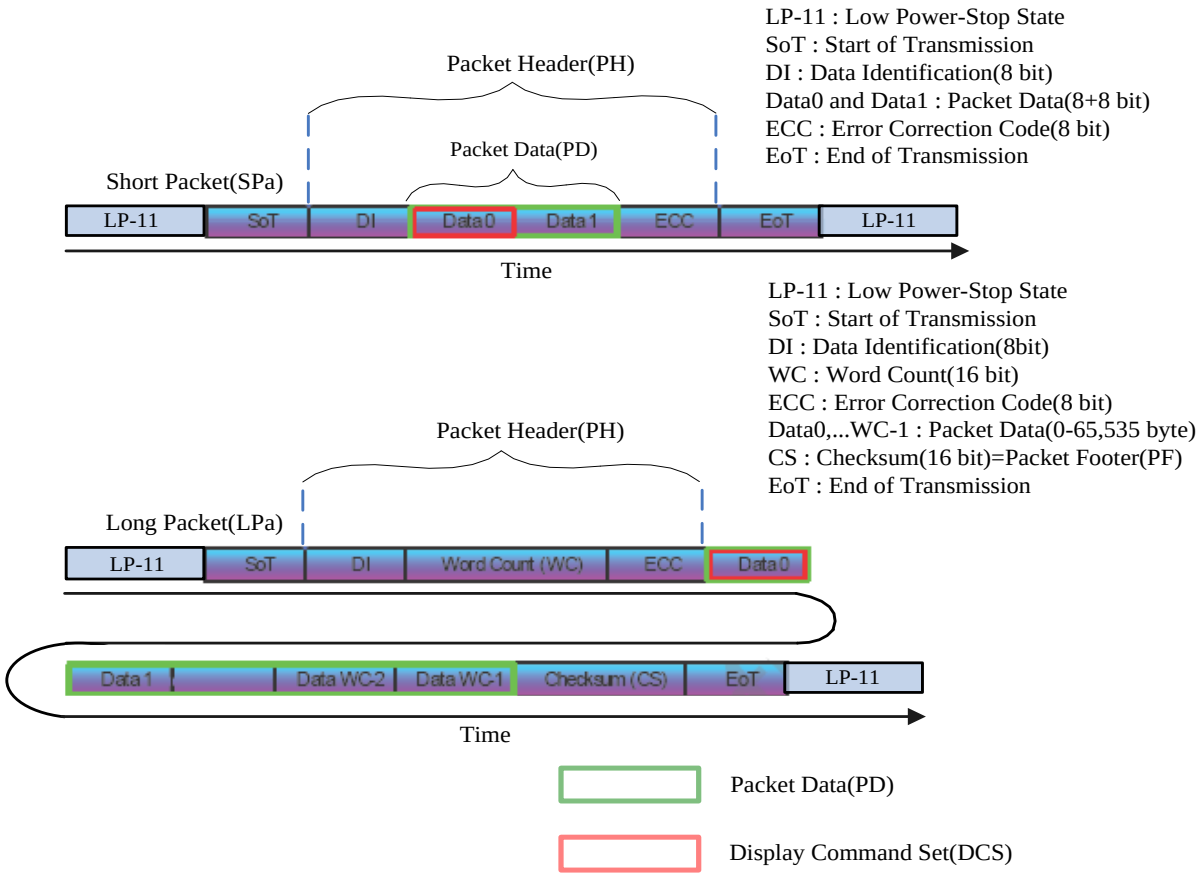


Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (Spa) or Long Packet (Lpa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type(DT).

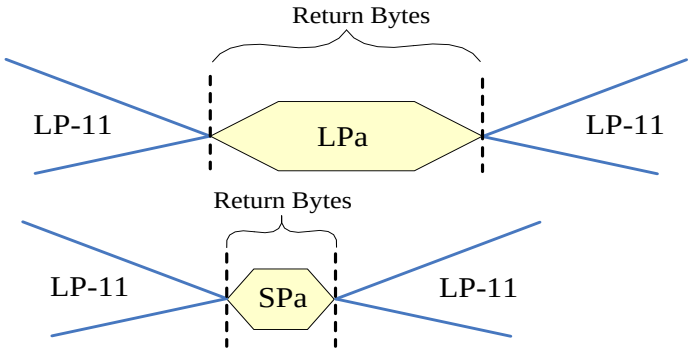


Figure: Return bytes on single packet

Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (Spa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to 1 , as they are defined on the following table.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error,signal-bit(detected and corrected)
9	ECC Error,multi-bit(detected,not corrected)
10	Checksum(CRC)Error(only for Long Packet(LP))
11	DSI Data Type(DT)Not Recognized
12	DSI Virtual Channel(VC)ID Invalid
13	Invalid Transmission Length
14	Reserved,set to 0 internally
15	DSI Protocol violation

Table: Acknowledge with error report for long packet response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error,signal-bit(detected and corrected)
9	ECC Error,multi-bit(detected,not corrected)
10	set to 0 internally
11	DSI Data Type(DT)Not Recognized
12	DSI Virtual Channel(VC)ID Invalid
13	Invalid Transmission Length
14	Reserved,set to 0 internally
15	DSI Protocol violation

Table: Acknowledge with error report for short packet response

These errors are only included on the last packet, which has been received from the MCU to the display module, before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (Spa) is defined e.g.

• Data Identification (DI)

-Virtual Channel (VC, DI[7…6]): 00b

-Data Type (DT, DI[5…0]): 00 0010b

• Packet Data (PD)

-Bit 8: ECC Error, single-bit (detected and corrected)

-AwER: 0100h

• Error Correction Code (ECC)

This is defined on the Short Packet (Spa) as follows.

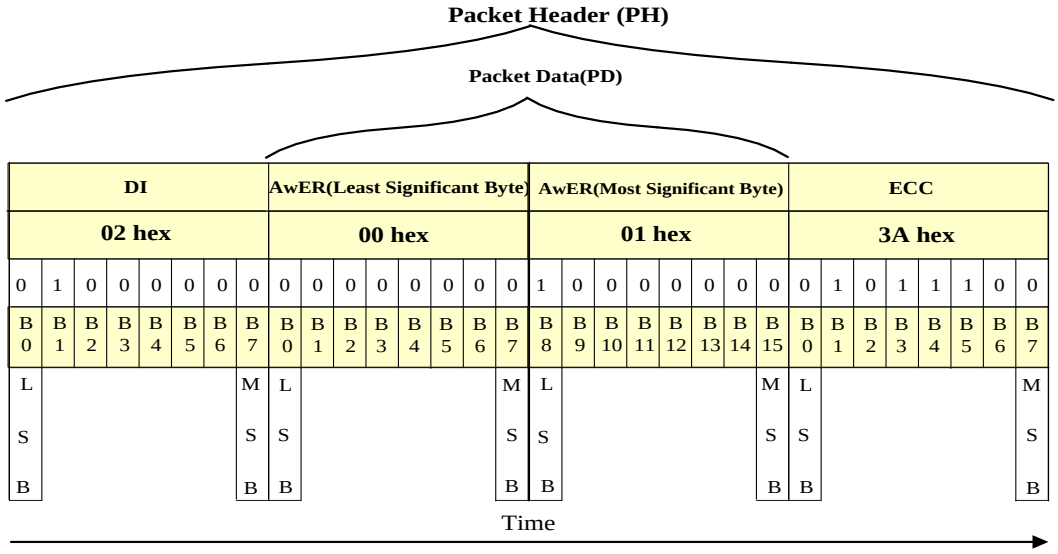


Figure: Acknowledge with error report – example

6.2.5. Customer-defined generic read data type format

NV3051F-L supports three types of generic read, generic read with no parameter,1 parameter and 2 parameters. If NV3051F-L receives generic read with no parameter packet, it will return ack report. If NV3051F-L receives generic read with 1 parameter or 2 parameters packet, it will return generic short packet with 1 byte response.

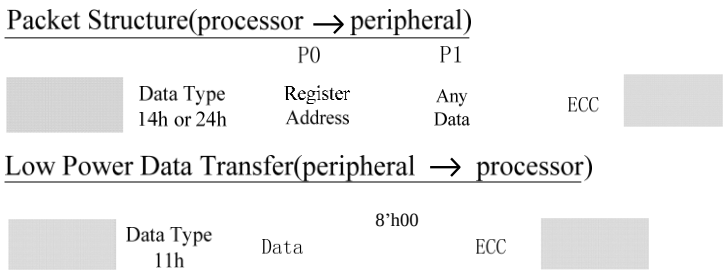


Figure: Generic read data type format

6.2.6. MIPI video parameter

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data.

Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

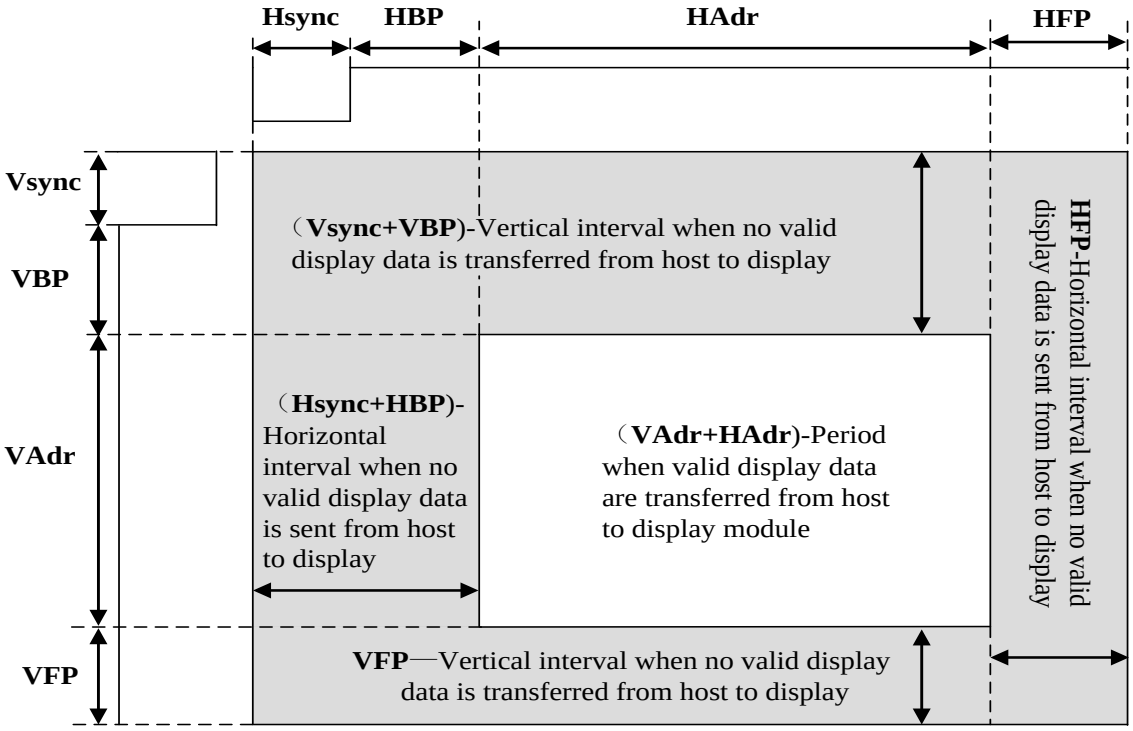


Figure define timing parameter for MIPI video operation

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle and PCLK Frequency (Resolution for 800 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	425	-	Mbps
PCLK Frequency	FPCLK	TBD	70.22	-	MHz
Horizontal Synchronization	Hsync	TBD	2	-	PCLK
Horizontal Back Porch	HBP	TBD	44	-	PCLK
Horizontal Front Porch	HFP	TBD	46	-	PCLK
Hsync+ HBP+ HFP	-	TBD	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	800	-	PCLK
Horizontal cycle	-	TBD	892	-	PCLK
Vertical Synchronization	Vsync	TBD	2	-	Line
Vertical Back Porch	VBP	TBD	14	-	Line
Vertical Front Porch	VFP	TBD	16	-	Line
Vsync+ VBP+ VFP	-	TBD	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate			60		Hz

“-”means no limit.

Note1 : If using Image Process Algorithm, Typ value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle and PCLK Frequency (Resolution for 720 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	384	-	Mbps
PCLK Frequency	FPCLK	TBD	63.92	-	MHz
Horizontal Synchronization	Hsync	TBD	2	-	PCLK
Horizontal Back Porch	HBP	TBD	44	-	PCLK
Horizontal Front Porch	HFP	TBD	46	-	PCLK
Hsync+ HBP+ HFP	-	TBD	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	720	-	PCLK
Horizontal cycle	-	TBD	812	-	PCLK
Vertical Synchronization	Vsync	TBD	2	-	Line
Vertical Back Porch	VBP	TBD	14	-	Line
Vertical Front Porch	VFP	TBD	16	-	Line
Vsync+ VBP+ VFP	-	TBD	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate			60		Hz

“-”means no limit.

Note1 : If using Image Process Algorithm, Typ value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle and PCLK Frequency (Resolution for 640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	347	-	Mbps
PCLK Frequency	FPCLK	TBD	57.62	-	MHz
Horizontal Synchronization	Hsync	TBD	2	-	PCLK
Horizontal Back Porch	HBP	TBD	44	-	PCLK
Horizontal Front Porch	HFP	TBD	46	-	PCLK
Hsync+ HBP+ HFP	-	TBD	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	640	-	PCLK
Horizontal cycle	-	TBD	732	-	PCLK
Vertical Synchronization	Vsync	TBD	2	-	Line
Vertical Back Porch	VBP	TBD	14	-	Line
Vertical Front Porch	VFP	TBD	16	-	Line
Vsync+ VBP+ VFP	-	TBD	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate			60		Hz

“-”means no limit.

Note1 : If using Image Process Algorithm, Typ value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle
(Resolution for 800 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	425	-	Mbps
PCLK Frequency	FPCLK	-	70.22	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	800	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle
(Resolution for 720 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	384	-	Mbps
PCLK Frequency	FPCLK	-	63.92	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle and Horizontal cycle
(Resolution for 640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	347	-	Mbps
PCLK Frequency	FPCLK	-	57.62	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	640	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	1312	-	Line
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle

(Resolution for 800 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	425	-	Mbps
PCLK Frequency	FPCLK	-	70.22	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	800	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	16.66	-	ms
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle
(Resolution for 720 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	384	-	Mbps
PCLK Frequency	FPCLK	-	63.92	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	720	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	16.66	-	ms
Frame-Rate	-	-	60	-	Hz

"-" means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

Below Table provide the timing parameter by external Vertical-cycle

(Resolution for 640 horizontal x 1280 vertical display with Frame-Rate of 60Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
MIPI Vedio data-rate (4 lane)	-	-	347	-	Mbps
PCLK Frequency	FPCLK	-	57.62	-	MHz
Horizontal Synchronization	Hsync	-	2	-	PCLK
Horizontal Back Porch	HBP	-	44	-	PCLK
Horizontal Front Porch	HFP	-	46	-	PCLK
Hsync+ HBP+ HFP	-	-	92	-	PCLK
Horizontal Address (Display area)	Hadr	-	640	-	PCLK
Horizontal cycle	-	-	12.703	-	us
Vertical Synchronization	Vsync	-	2	-	Line
Vertical Back Porch	VBP	-	14	-	Line
Vertical Front Porch	VFP	-	16	-	Line
Vsync+ VBP+ VFP	-	-	32	-	Line
Vertical Address (Display area)	Vadr	-	1280	-	Line
Vertical cycle	-	-	16.66	-	ms
Frame-Rate	-	-	60	-	Hz

“-” means no limit.

Note : 1. If using Image Process Algorithm, Type value for H-blanking is minimum requirement.

6.3. Serial Interface (SPI)

The serial interface is used to communication between the micro controller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

6.3.1. SPI write mode

The write mode of the interface means the micro controller writes commands and data to the NV3051F-L. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. When CSX is high, SCL clock is ignored. During the high time of CSX the serial interface is initialized. At the falling CSX edge, SCL can be high or low. SDI/SDO is sampled at the rising edge of SCL. R/W indicates, whether the byte is read command(R/W = '1') or write command (R/W = '0'). It is sampled when first rising SCL edge. If CSX stays low after the last bit of command/data byte, the serial interface expects the R/W bit of the next byte at the next rising edge of SCL.

Register Write: Singal Parameter

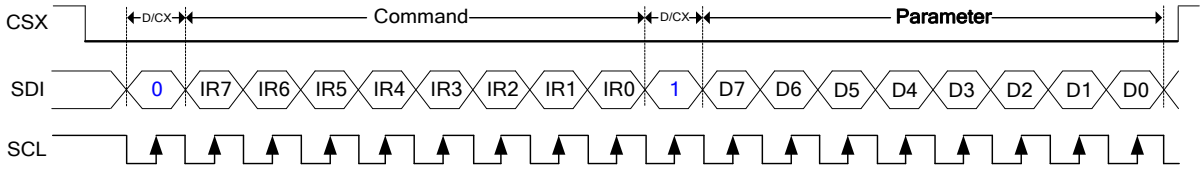


Figure: SPI Protocol for write

6.3.2. SPI read mode

The read mode of the interface means that the micro controller reads register value from the NV3051F-L. To do so the micro controller first has to send a command and then the following byte is transmitted in the opposite direction. After that CSX is required to go high before a new command is send. The NV3051F-L samples the SDI (input data) at the rising edges, but shifts SDO (output data) at the falling SCL edges.

Thus the micro controller is supported to read data at the rising SCL edges. After the read status command has been sent, the SDI line must be set to tri-state no later than at the falling SCL edge of the last bit. For the memory data read, a dummy clock cycle is needed (8 SCL clocks) to wait the memory data send out in SPI interface. But it doesn't need any dummy clock when execute the command data read.

Register Read: Without dummy clock

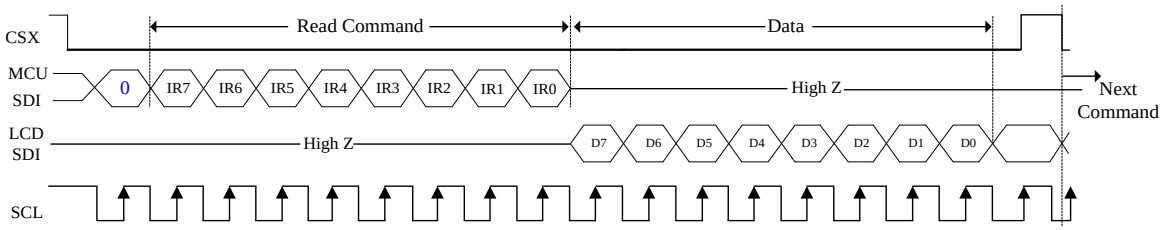
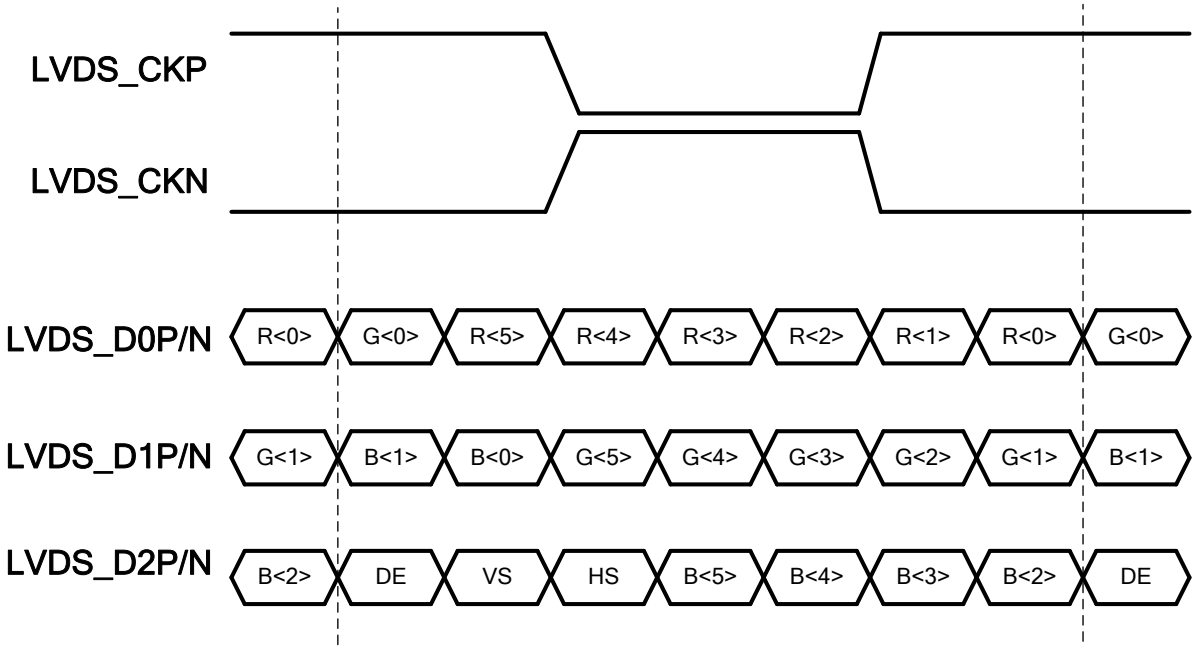


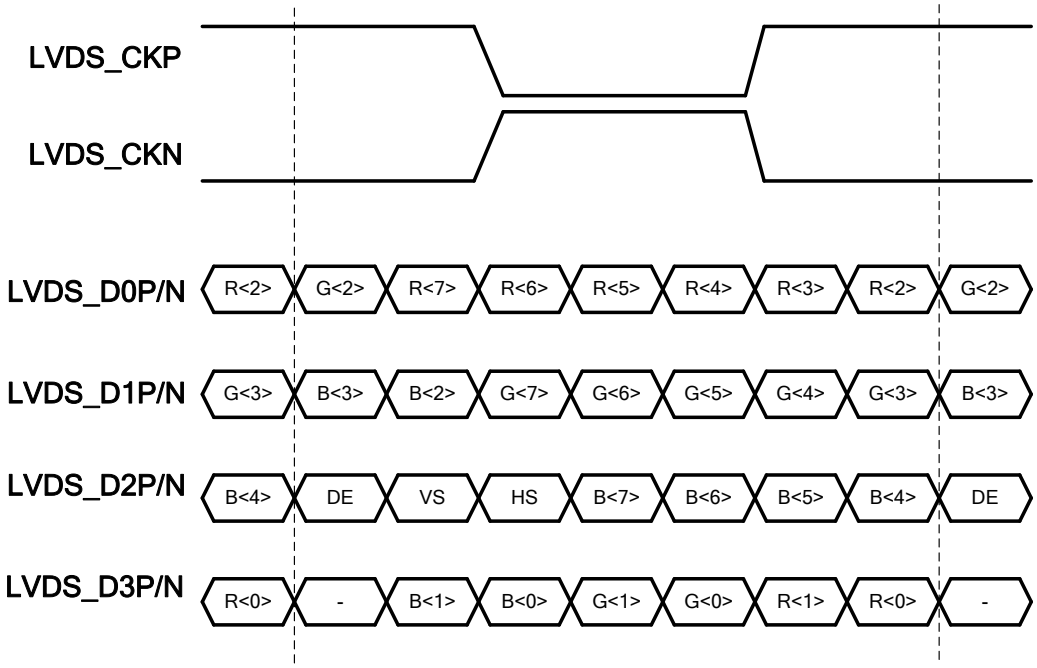
Figure: SPI Protocol for register read mode

6.4. LVDS interface

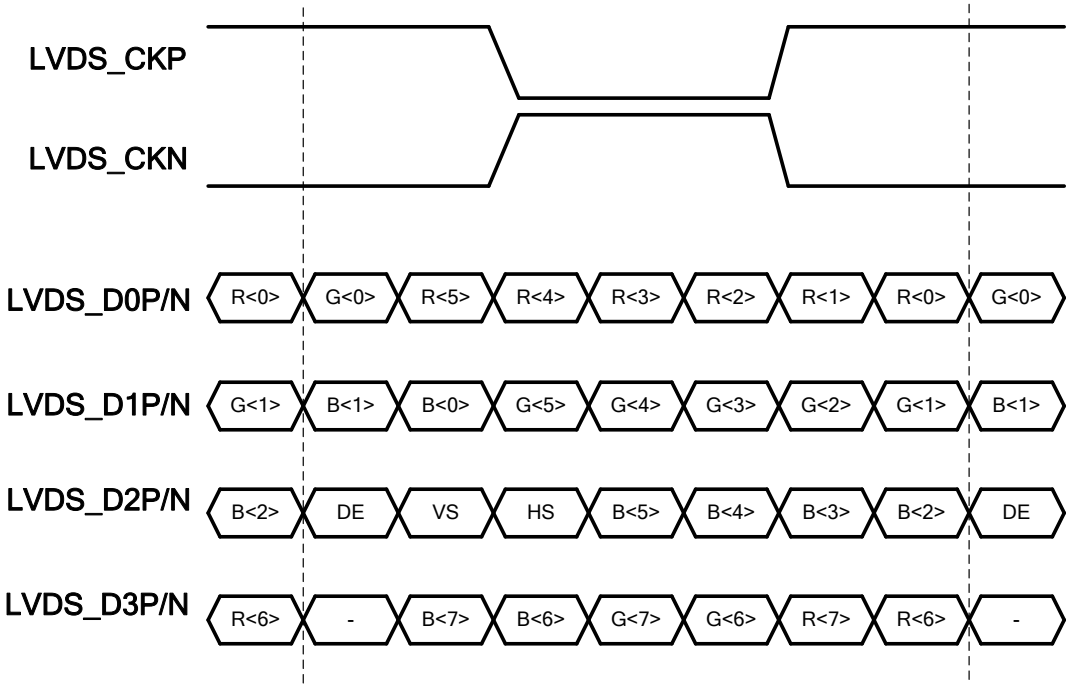
6.4.1 Data input format for LVDS



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input (LVBIT=H, LVFMT=H)

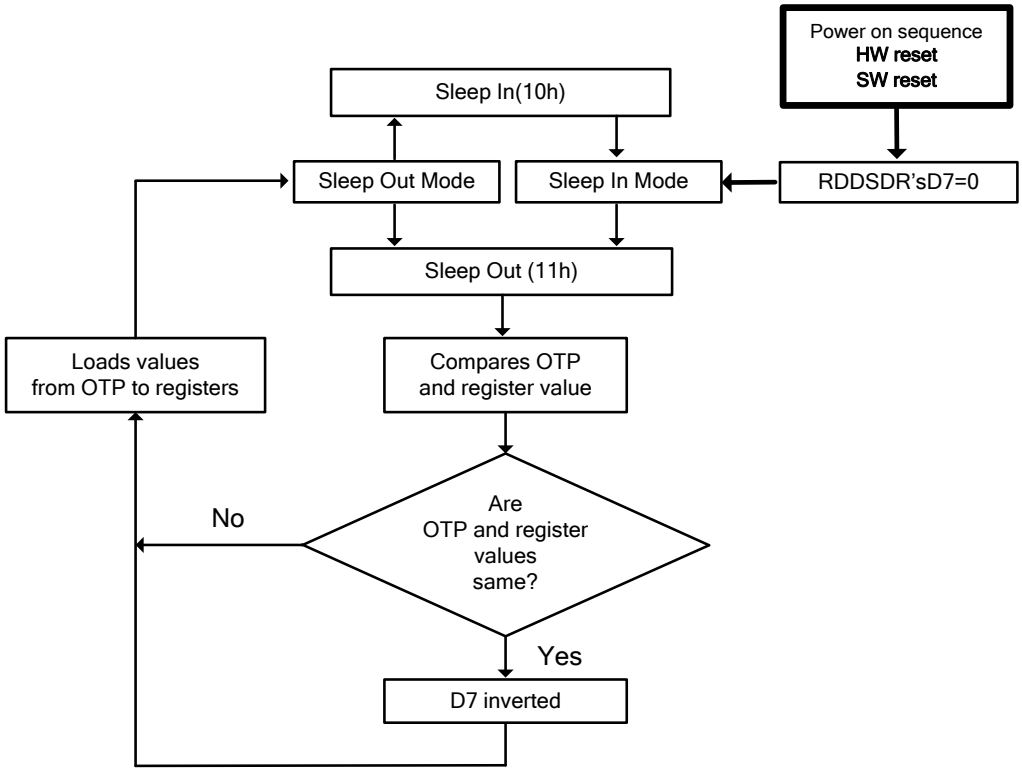
6.5. Sleep Out-Command And Self-Diagnostic Functions Of The Display Module

6.5.1. Register loading detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (one-time programming memory) to registers of the display controller is working properly.

There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit in “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (= increased by 1).

The flow chart for this internal function is following:

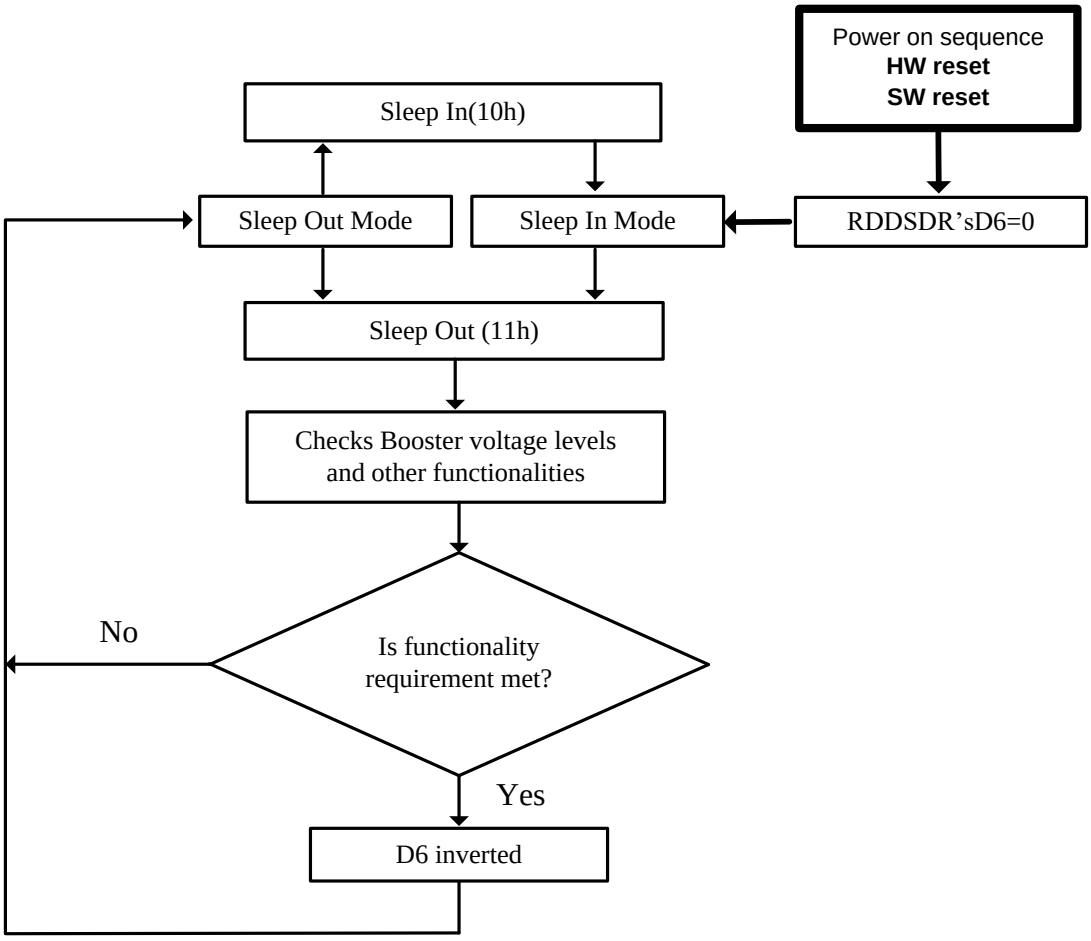


6.5.2. Functionality detection

Sleep Out-command is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted (= increased by 1) a bit in "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1).

The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out –command, when there is changing from Sleep In –mode to Sleep Out –mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out –mode.

6.6. Power On/Off Sequence

IOVCC and VCI can be applied in any order. IOVCC and VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

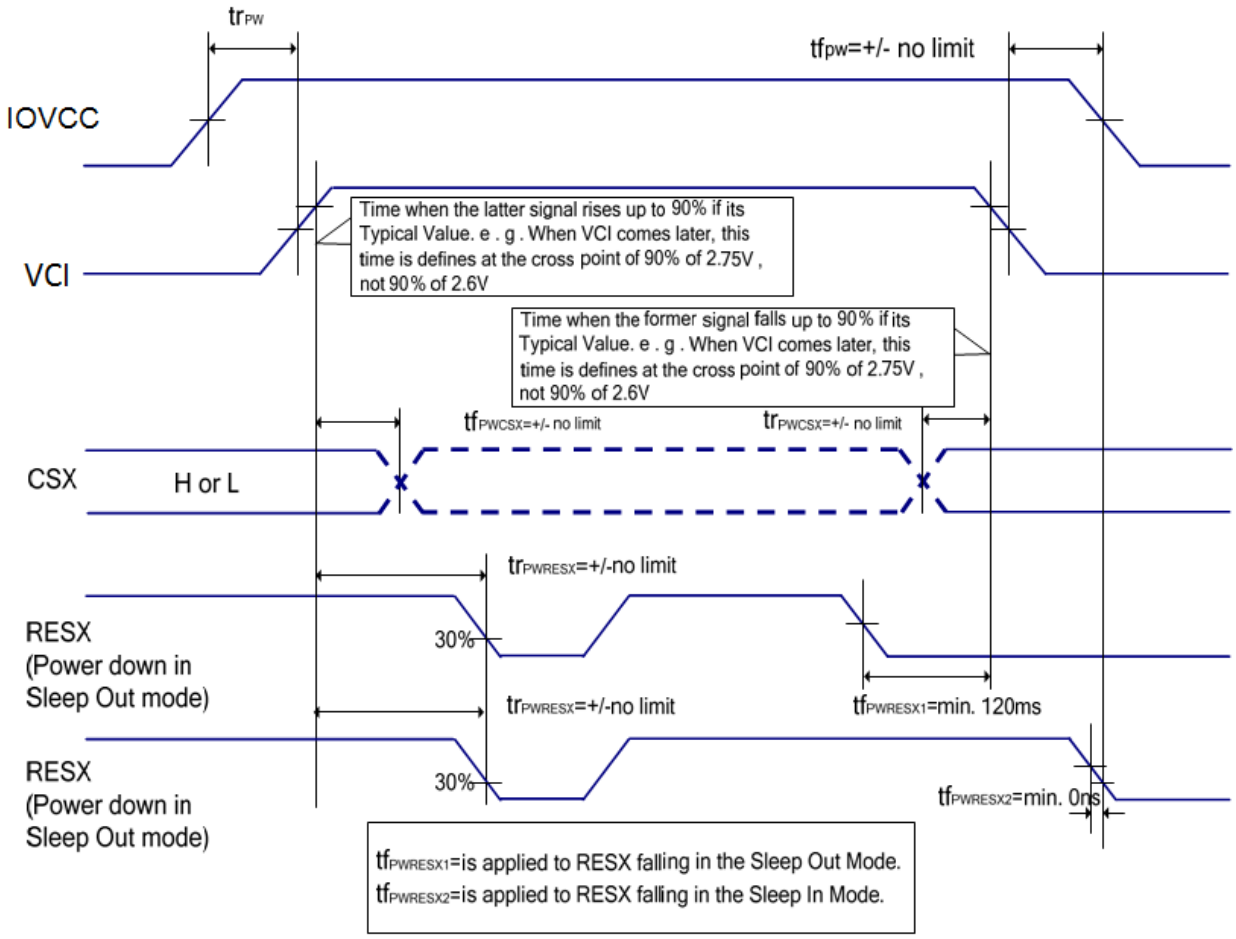
Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below:

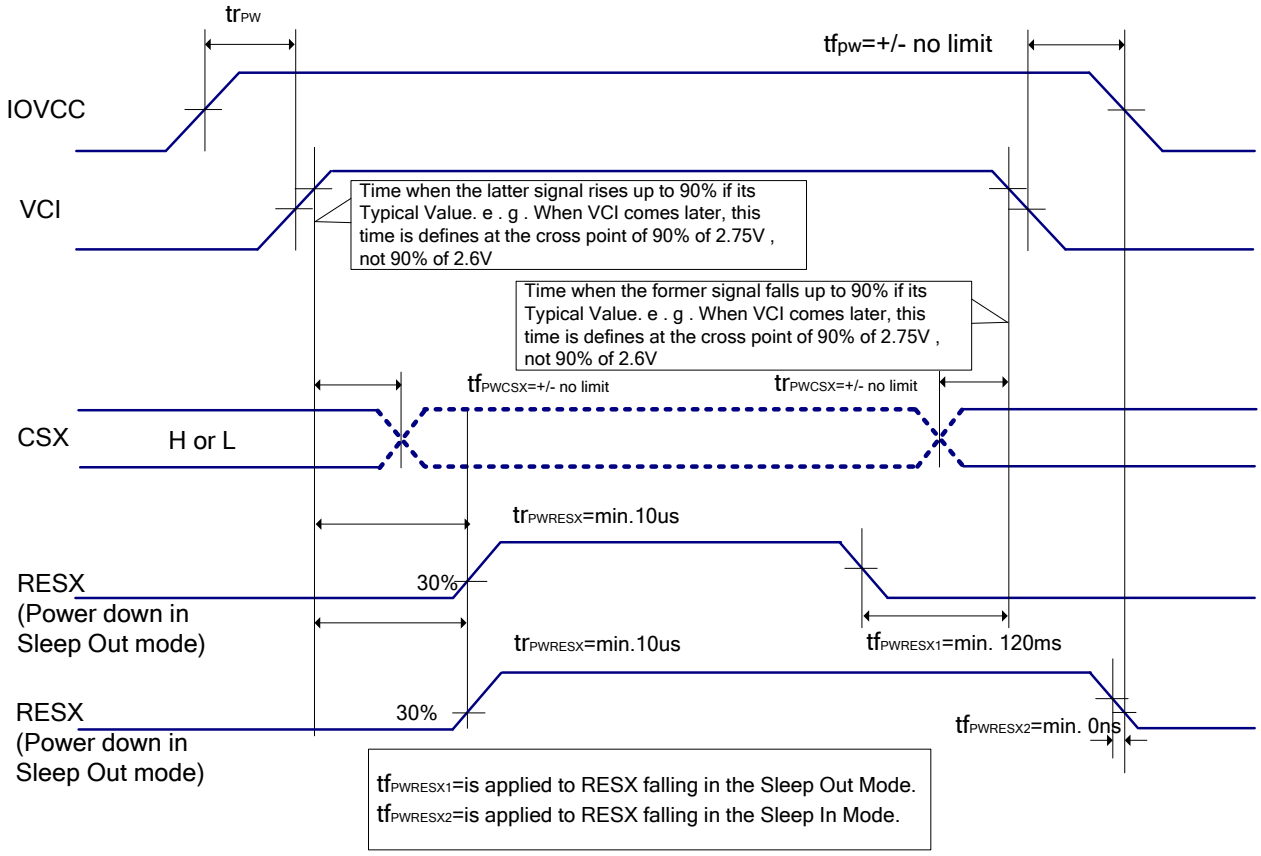
6.6.1. Case 1 – RESX line is held high or unstable by host at power on

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



6.6.2. Case 2 – RESX line is held low or unstable by host at power on

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10sec after both VCI and IOVCC have been applied.



6.6.3. Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface.

At an uncontrolled power off the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7. ELECTRICAL SPECIFICATION

7.1. Absolute Maximum Ratings

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30℃ ~ 85℃)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	IOVCC-VSS	-0.3 ~ +4.5	V	
Power Supply Voltage 2	VDDAM-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 3	VCI-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 4	VPP-VSS	-0.3 ~ +7.8	V	
Power Supply Voltage 5	DVDD-VSS	-0.3 ~ +1.8	V	
Power Supply Voltage 6	VSP-VSS	-0.3 ~ +6.6	V	
Power Supply Voltage 7	VSS-VSN	-0.3 ~ +6.6	V	
Power Supply Voltage 8	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ IOVCC +0.3	V	
Operating Temperature	Topr	-30 ~ +85	℃	
Storage Temperature	Tstg	-40 ~ +125	℃	

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2. DC characteristic

7.2.1. Basic DC characteristic

(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30℃ ~ 85℃)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.5	2.8	6.0	V	
Logic Operating voltage	IOVCC	I/O supply voltage	1.65	1.8	3.6	V	
MIPI interface operating voltage	VDDAM	MIPI supply voltage	1.75	-	6.0	V	Note1
Input/Output							
Logic High level input voltage	VIH	-	0.7*IOVCC	-	IOVCC	V	
Logic Low level input voltage	VIL	-	VSS	-	0.3*IOVCC	V	
Logic High level output voltage	VOH	IOH = -0.1mA	0.8*IOVCC	-	IOVCC	V	
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2*IOVCC	V	
Logic Input leakage current	IIL	Vin=IOVCC or VSSI	-0.1	-	+0.1	uA	
VCOM Operation							
VCOM voltage	VCOM	-	-3.375	-1.0	0	V	
Source Driver							
Source output range	Vsout	-	VGMN+0.1	-	VGMP-0.1	V	
Gamma positive reference voltage	VGMP	-	2.64	-	5.846	V	
Gamma negative reference voltage	VGMN	-	-5.702	-	-2.509	V	
Source output settling time	Tr	Below with 99% precision	-	TBD	-	us	
Output deviation voltage (Source positive output channel)	V,dev	Sout >=+4.2V, Sout<=+0.8V	-	-	TBD	mV	
		+4.2V>Sout>+0.8V	-	-	TBD	mV	
Output deviation voltage (Source negative output channel)	V,dev	Sout <=-4.2V, Sout>=-0.8V	-	-	TBD	mV	
		-4.2V<Sout<-0.8V	-	-	TBD	mV	

Output offset voltage	VOFFSET	-	-	-	TBD	mV	
Reference Voltage							
Internal reference voltage	VREF		1.876	2.00	2.125	V	
Booster operation							
1st booster output voltage	VSP		4.5		6	V	
	VSN		-6		-4.5	V	
2nd booster output voltage	VGH		11.0		18.0	V	
	VGL		-15.5		-7.0	V	
Current Consumption							
Sleep-IN mode	IIOVCC	RESX=High		TBD	TBD	uA	Note2
	IVCI			TBD	TBD	uA	
Deep standby mode	IIOVCC	RESX=High		TBD	TBD	uA	
	IVCI			TBD	TBD	uA	

Note1. VDDAM are used as the power of MVDD LDO, the voltage level can't be lower than 1.75V

Note2. The power/temperature conditions for Current consumption (Sleep-IN) part is (VCI, VDDAM) =3.0V, IOVCC=1.8V@25℃

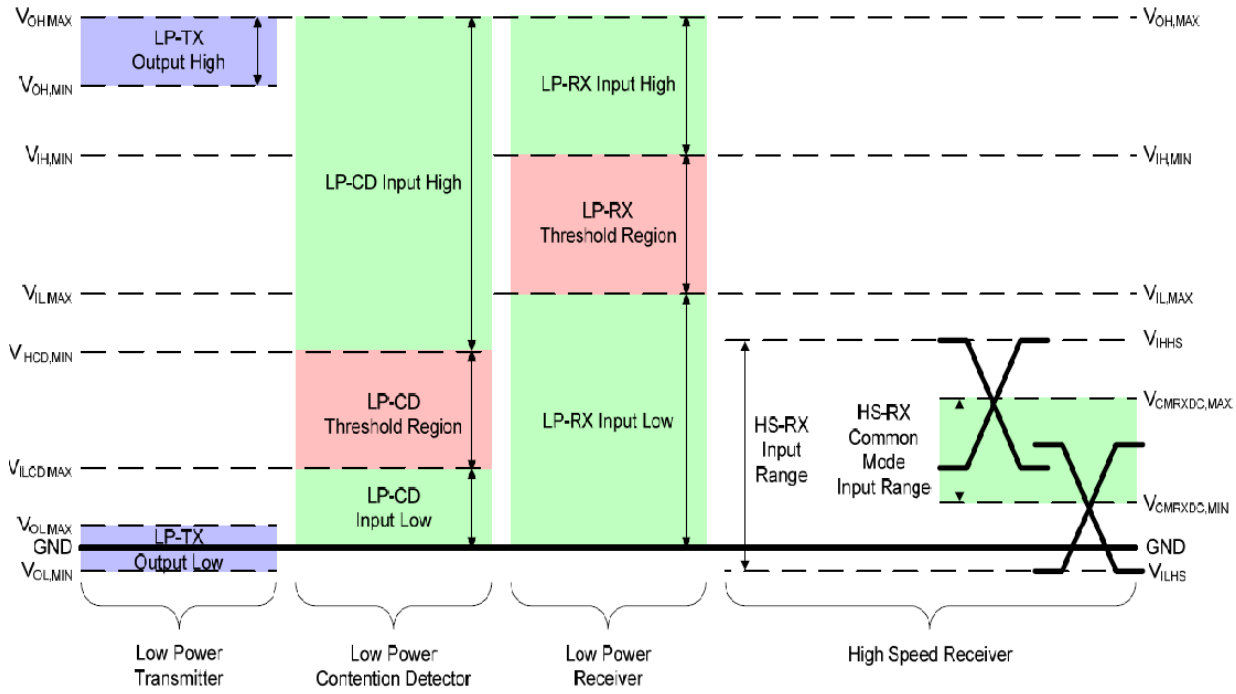
(These values might be updated after further evaluation.)

7.2.2. MIPI DC character

DC characteristics for MIPI-DSI

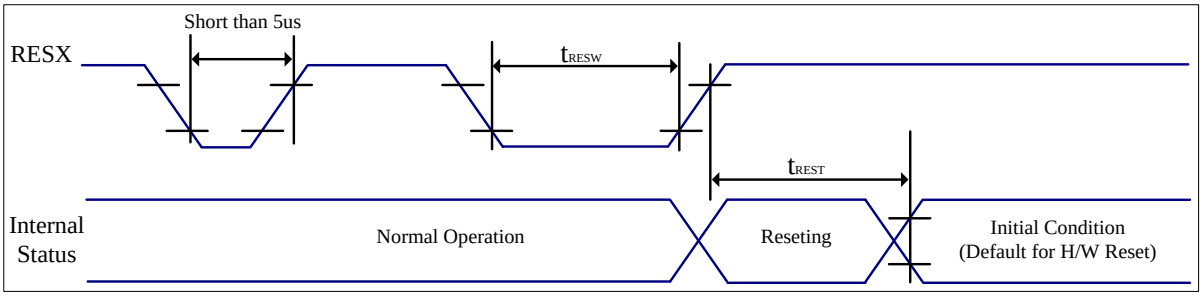
(VCI=2.5V~6.0V, IOVCC = 1.65V~3.6V, Ta = -30℃~ 85℃)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDAM	-	1.75	1.8	6.0	V
	MV1P2	-	1.125	1.2	1.3	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGNDSH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	MV1P2	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	MV1P2	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedence	ZID	-	80	100	125	ohm


VOH,MAX
LP-TX
Output High
VOH,MIN
VIH,MIN
VIL,MAX
VHCD,MIN
VILCD,MAX
VOL,MAX
GND
LP-TX
Output Low
VOL,MIN
LP-CD Input High
LP-CD
Threshold Region
LP-CD
Input Low
LP-RX Input High
LP-RX
Threshold Region
LP-RX Input Low
HS-RX
Input
Range
HS-RX
Common
Mode
Input Range
VIHHS
VCMRXDC,MAX
VCMRXDC,MIN
GND
VILHS
Low Power
Transmitter
Low Power
Contention Detector
Low Power
Receiver
High Speed Receiver

7.3. AC characteristic

7.3.1. Reset timing characteristics



VSS=0V, IOVCC=1.65V to 3.6V, VCI=2.5V to 6.0V,Ta = -30℃ to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Table: Reset input timing

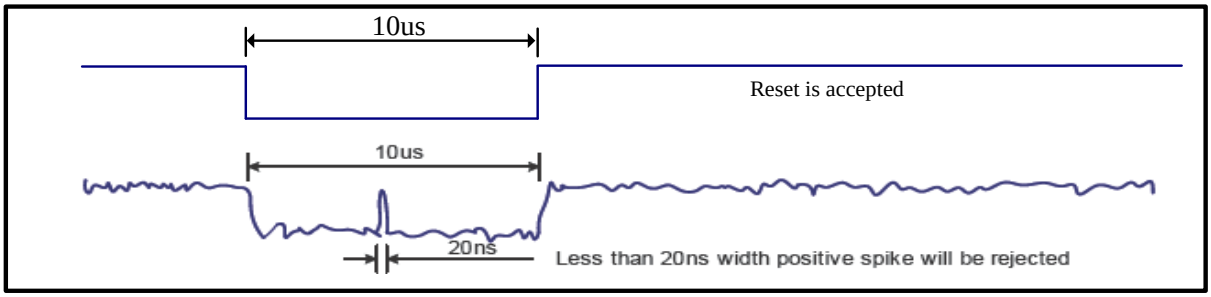
Note 1: Due to an electrostatic discharge on RESX line,spike does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition.)

Note 2: During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode) , then return to default condition for H/W reset.

Note 3: During Reset Complete Time, ID1/ID2/ID3 and VCOM value in OTP will be latched to internal register. After a rising edge of RESX, there is a H/W reset complete time (Trest) which lasted 5ms.The loading operation will be done every time during this reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 msec.

7.3.2. Serial interface characteristics (SPI)

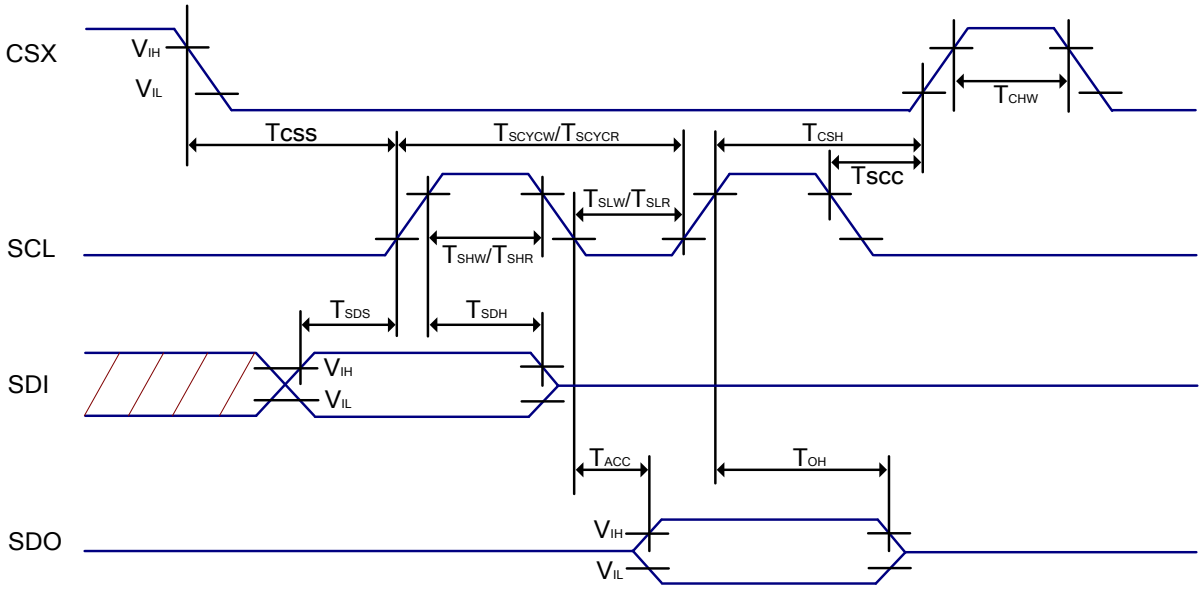


Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time	15	-	ns	-
	T_{CSH}	Chip select hold time	15	-	ns	
	T_{SCC}	Chip select setup time	20	-	ns	
	T_{CHW}	Chip “H” pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	66	-	ns	-
	T_{SHW}	SCL “H” pulse width (Write)	10	-	ns	
	T_{SLW}	SCL “L” pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	-
	T_{SHR}	SCL“H” pulse width (Read)	60	-	ns	
	T_{SLR}	SCL“L” pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	T_{SDH}	Data hold time	10	-	ns	
	T_{ACC}	Access time	10	50	ns	For maximum C_L=30pf For minimum C_L=8pf
	T_{OH}	Output disable time	15	50	ns	

Note 1: IOVCC=1.65 to 3.6V, VCI=2.5 to 6V, VSSI=VSS=0V, Ta=-30 to 85℃

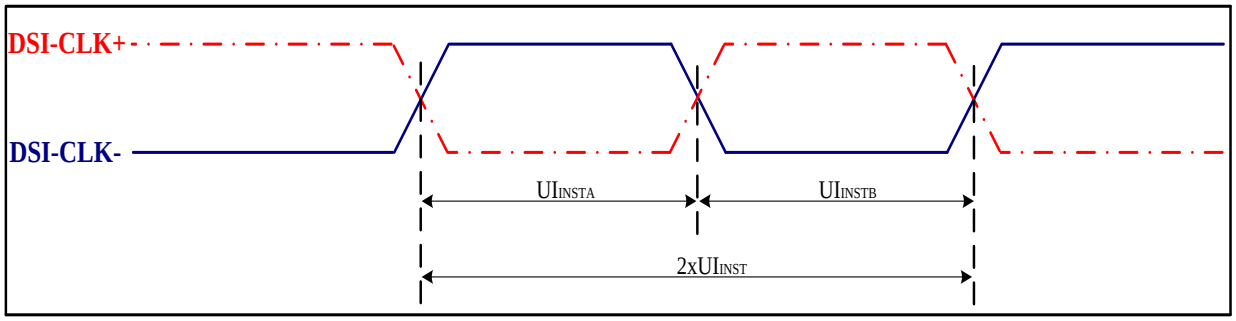
Note 2: The rise time and fall time (tr, tf) of input signal is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

7.3.3. MIPI-DSI characteristics

7.3.3.1. High speed mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2Xui_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T_{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T_{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T_{drtclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{drtdata}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T_{dftclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{dftdata}$	Differential fall time for data	150	-	0.3UI	ps



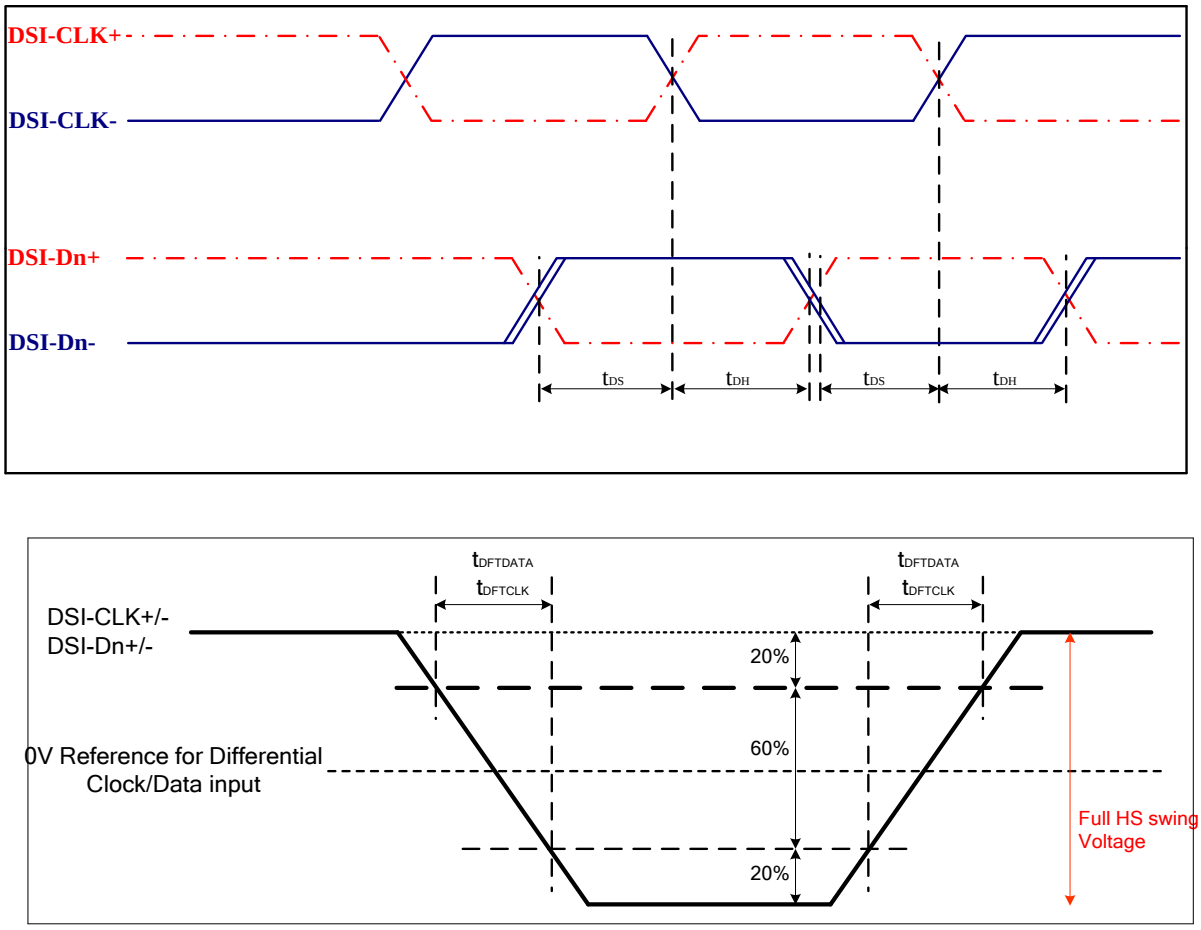


Figure: AC characteristics for MIPI-DSI High speed mode

7.3.3.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

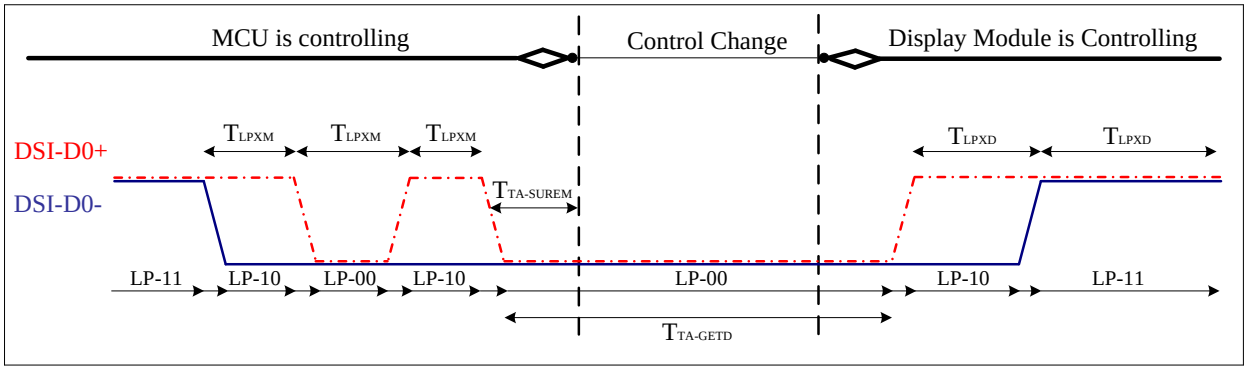


Figure: BTA from the MCU to the Display Module

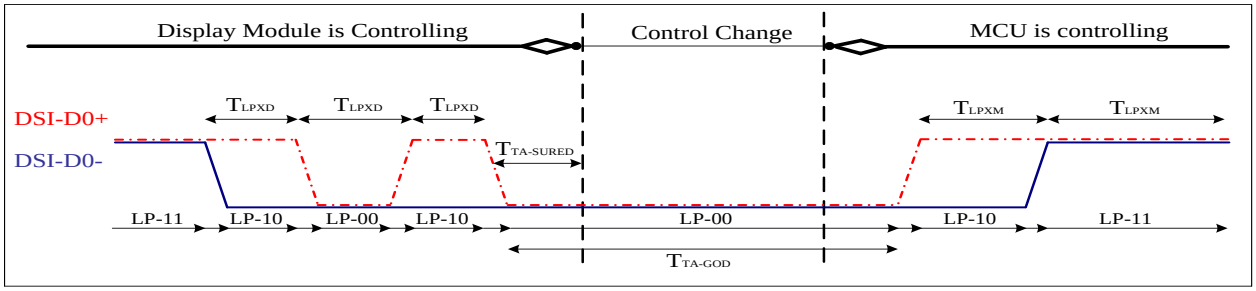


Figure: BTA from the Display Module to the MCU

7.3.3.3. Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS- PREPARE+THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

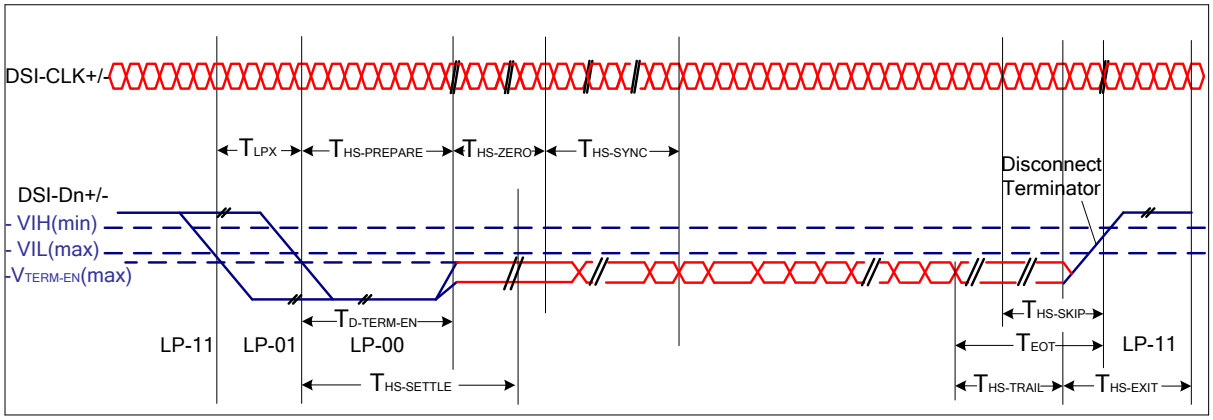


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

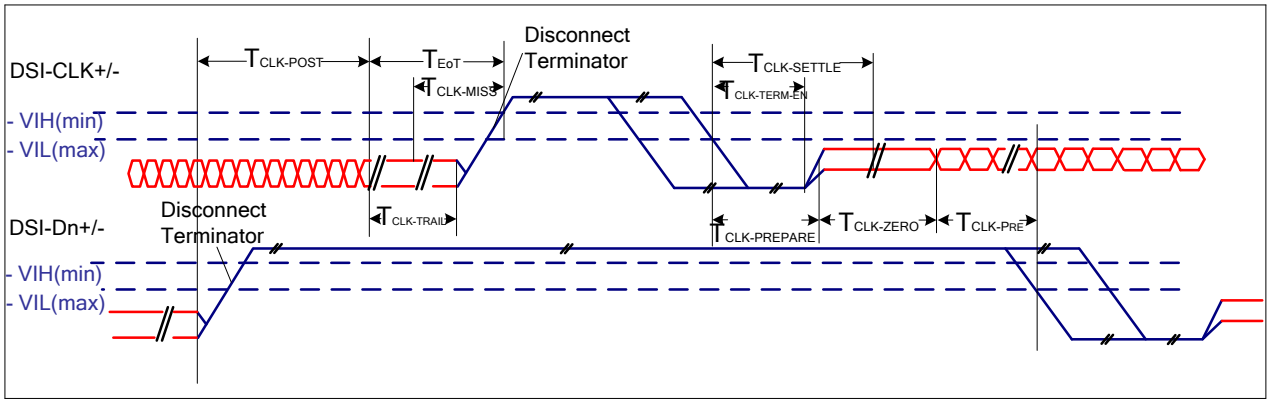


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

7.3.4 LVDS DC characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential input high threshold voltage	$V_{Rx,TH}$	V_{RxVCM}=1.2V	-	-	0.1[Note]	V
Differential input low threshold voltage	$V_{Rx,TL}$		-0.1[Note]	-	-	V
Input voltage range(single-end)	V_{RxIN}		0	-	1.8	V
Differential input common mode voltage	V_{RxVCM}		|VID|/2	1.2	1.8 - |VID|/2	V
Differential input voltage	|VID|		0.2	-	0.6	V
Differential input leakage current	I_{LCLVDS}		-10	-	10	uA
Differential input impedance	ZID		80	100	140	Ω

Note : VCI=3.3V

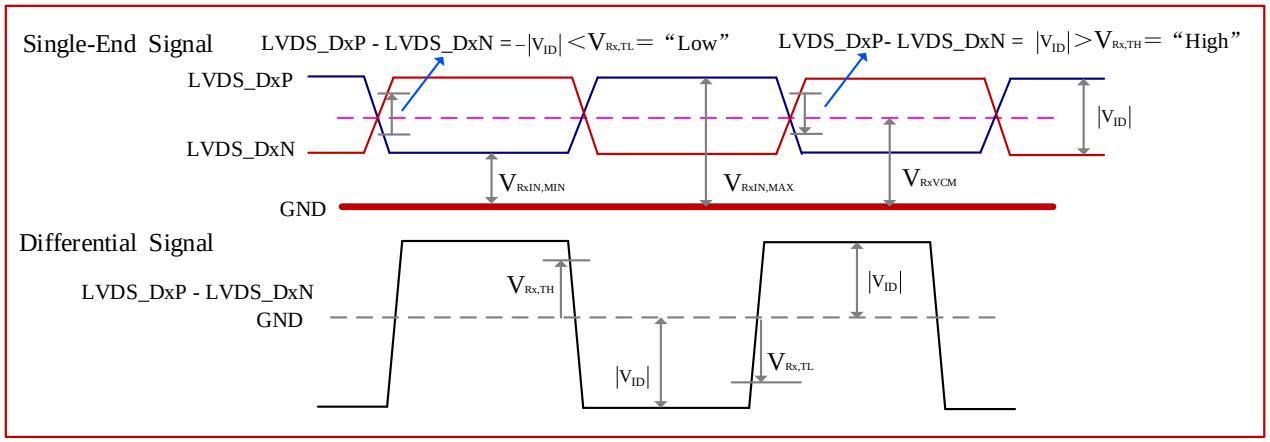


Figure: LVDS Receiver Differential Definition

7.3.5 LVDS AC characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	RxFCLK	-	30	-	71	MHz
Input data skew margin	TRSKM	|VID|=200mV RxVCM=1.2V RxFCLK=71MHz	500	-	-	ps
Clock High Time	TLVCH	-	-	4/(7*RxFCLK)	-	ns
Clock Low Time	TLVCL	-	-	3/(7*RxFCLK)	-	ns
PLL wake-up-time	TenPLL	-	-	-	150	us

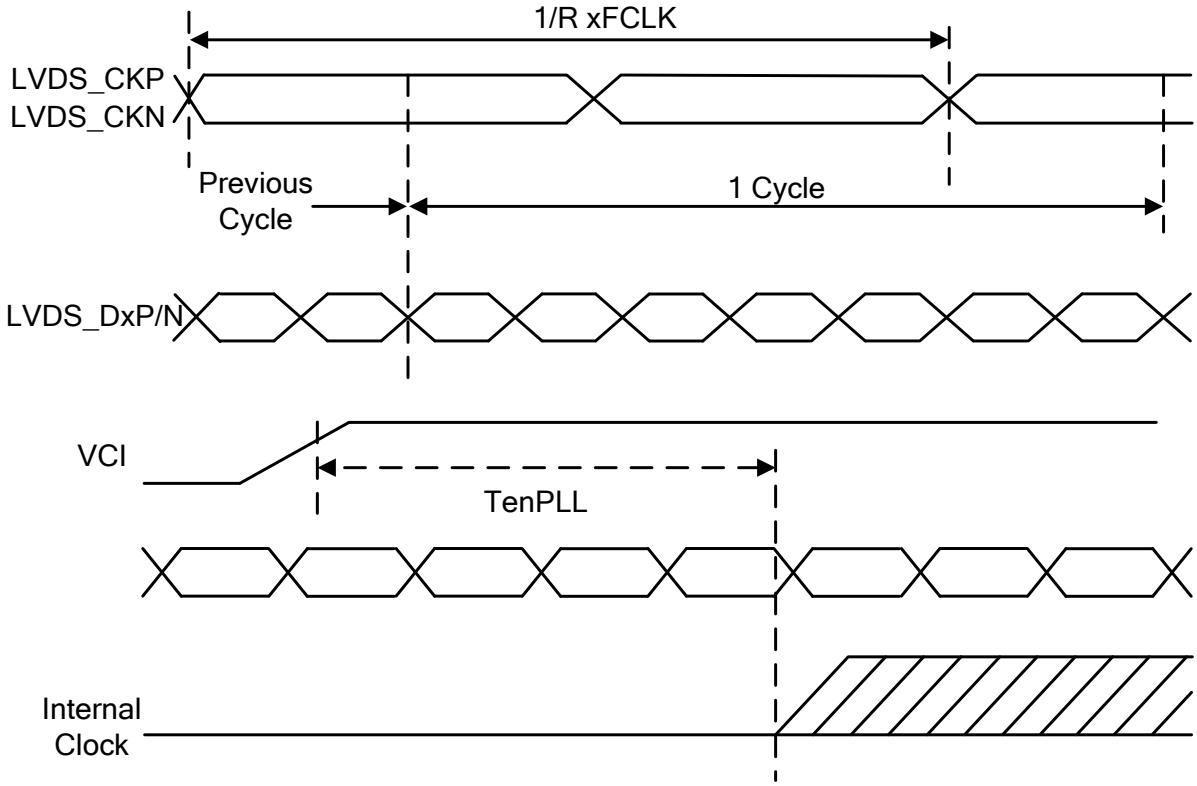
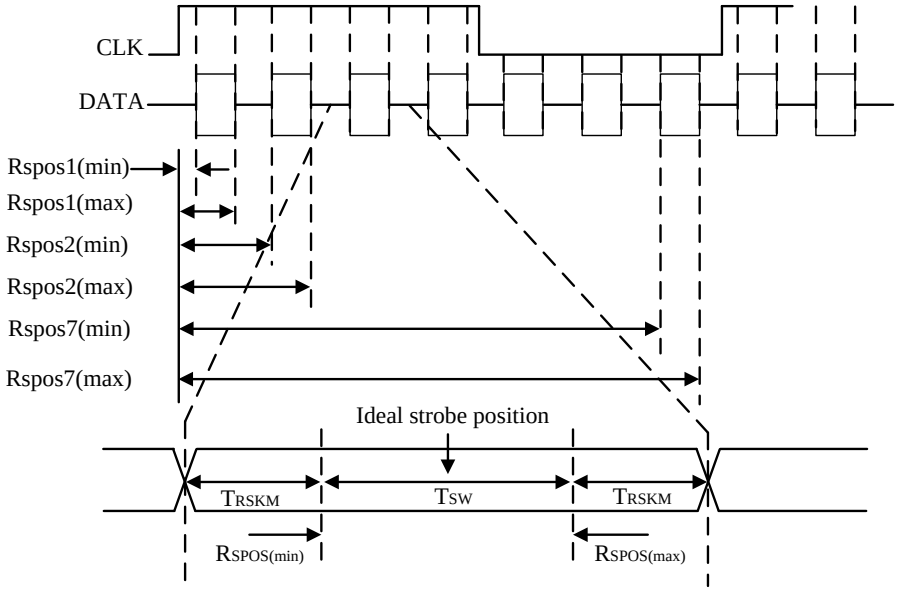


Figure LVDS figure

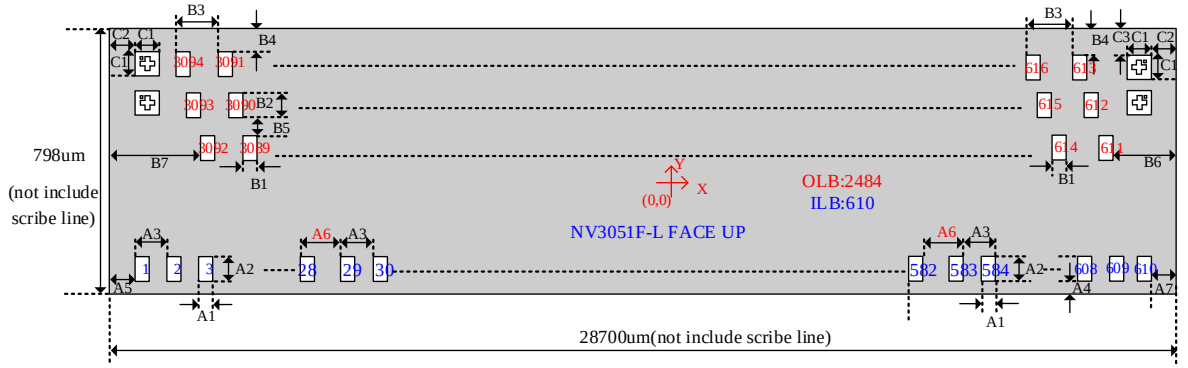
Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Modulation Frequency	SSC_{MF}	23	-	93	KHz	
Modulation Rate	SSC_{MR}	-	-	+3	%	



TSW:Strobe width (Internal data sampling window)
RSPOS:Receiver strobe position
TRSKM:Receiver strobe margin

8. CHIP INFORMATION

8.1. PAD Assignment



Symbol	Size	Symbol	Size	Symbol	Size
A1	30	A7	672.5	B6	735.5
A2	48	B1	16	B7	657.5
A3	45	B2	65	C1	60
A4	13	B3	33	C2	664
A5	572.5	B4	13	C3	10.1
A6	55	B5	25	Unit: um	

Note: There is temperature compensation design.

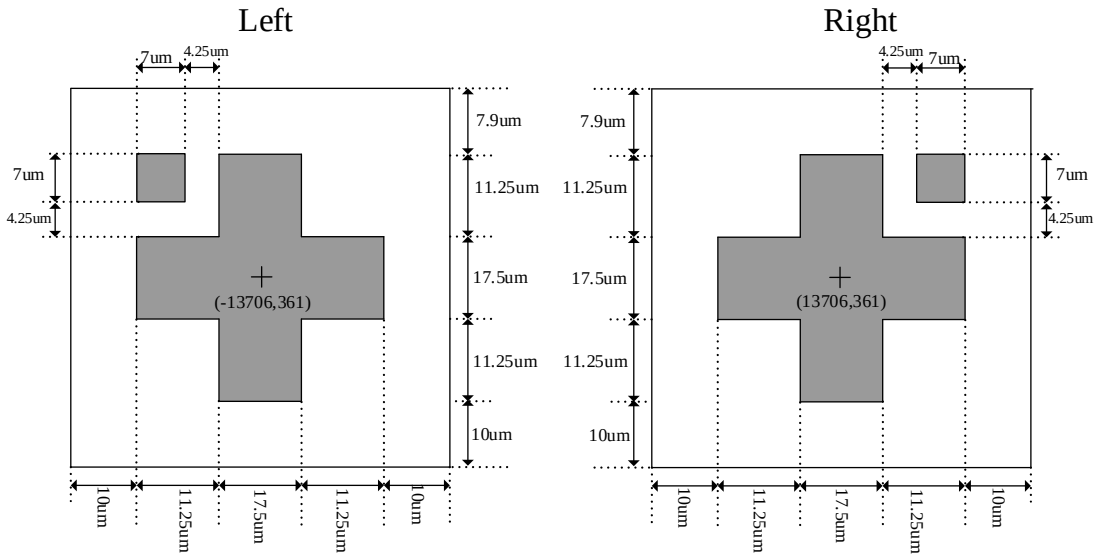
Maximum layout resistance:

Name	Type	Maximum layout resistance	Unit
IOVCC	Power supply	10	Ω
VDDAM	Power supply	10	Ω
VCI	Power supply	10	Ω
VSP,VSN	Power supply	10	Ω
DGND	Power supply	10	Ω
DGND_LVDS	Power supply	10	Ω
AGND	Power supply	10	Ω
VSSI	Power supply	10	Ω
VSSI_LVDS	Power supply	10	Ω
MGND	Power supply	10	Ω
CGND1	Power supply	10	Ω
RGND	Power supply	10	Ω
VPP	Power supply	10	Ω
IM[2:0],LANSEL	Input	100	Ω
EXTP,EXTN	Output	30	Ω
SCL,CSX,RESX	Input	100	Ω
SDI	Input/Output	100	Ω
SDO	Output	100	Ω
TE, TE1	Output	100	Ω
LEDPWM	Output	100	Ω
PWM_VSN	Output	100	Ω
CLKP;CLKN	Input	8	Ω
D0P/N~D3P/N	Input/Output	8	Ω
LVDS_CKP;LVDS_CKN	Input	5	Ω
LVDS_D0P/N~LVDS_D3P/N	Input	5	Ω
DVDD	Output	10	Ω
DVDD_LVDS	Output	10	Ω
VGMP, VGMN	Output	10	Ω
VREF	Output	10	Ω
VGH	Output	10	Ω
VGL	Output	10	Ω
MVDD	Output	10	Ω
GOUT_L[22:1]	Output	30	Ω
GOUT_R[22:1]	Output	30	Ω
VCOM_L,VCOM_R,VCOM_DUM	Output	10	Ω
TEST_EN,BIST_EN,CLK_SEL	Input	100	Ω
EXT_CLK,TEST[3:0]	Input	30	Ω
TOUT[3:0]	Output	30	Ω
LED_K1; LED_K2; LED_k3; LED_k4; LED_k5	Input/Output	5	Ω
RS1	Input	100	Ω
VGH1,VGH2	Output/Capacitor Connection	10	Ω
DCHR1, DCHR2	Output/Resistor Connection	50	Ω

8.2. Alignment Mark

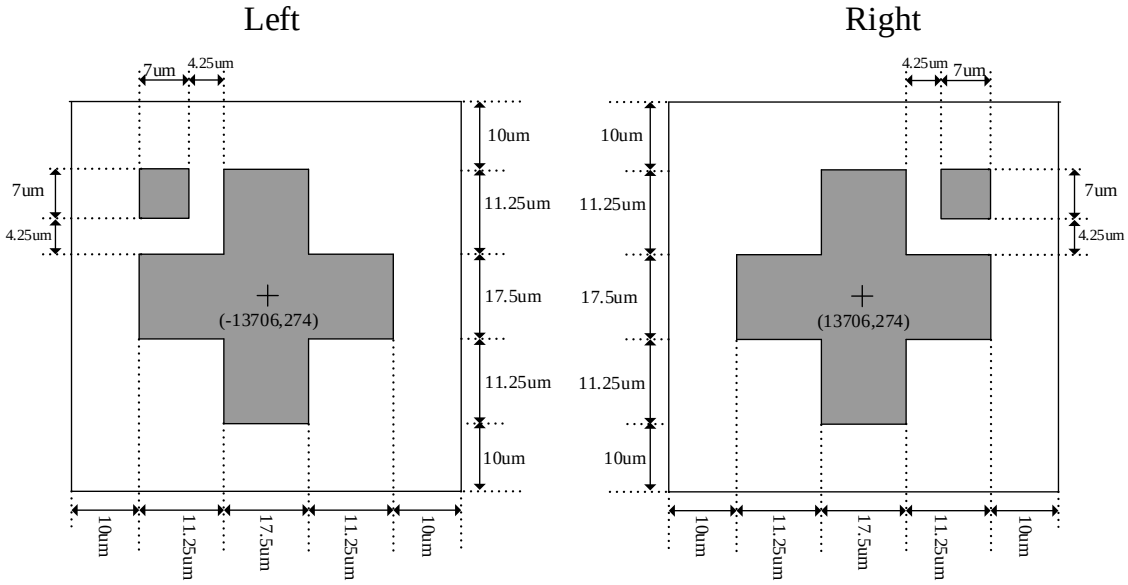
--Alignment Mark coordinate

Left1 (-13706,361),Right1 (13706,361)



Left2 (-13706, 274),Right2 (13706, 274)

--Alignment Mark size



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Revision history

Version No.	Date	Page	Introduction
0.1	2022-3-10	All	New build.
0.2	2022-11-07	All	Update “Chapter 6.2.6 MIPI video parameter”
0.3	2023-5-5	151、153	Update “Chapter 8 CHIP INFORMATION”
0.4	2023-9-13	63	Add the register of 23h in chapter 5.3
0.5	2023-10-8	64	Update the description of 37H~39H register in “Chapter 5.3.3”
0.6	2024-3-11	149、150	Update the voltage of $V_{Rx,TH}$ and $V_{Rx,TL}$ in chapter 7.3.4 Update the LVDS clock frequency in chapter 7.3.5
0.7	2024-4-10	148	Delete the typical value of differential input voltage and update the waveform in chapter 7.3.4