ST75160

4 Level Gray Scale Dot Matrix LCD Controller/Driver

Datasheet

Version 1.6

Sitronix Technology Corporation

LIST OF CONTENT

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

ST75160 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 160-segment and 160-common with 1-icon-common driver circuits. This chip can be connected directly to a microprocessor which accepts 8-bit parallel interface (8080-series or 6800-series type), 4-Line serial, 3-Line serial or I^2C interface. Display data is stored into an on-chip Display Data RAM (DDRAM). It performs the Display Data RAM read/write operation without external operating clock, and the power consumption can be minimized. In addition, since all necessary power supply circuits for LCD system are built-in, ST75160 constructs a LCD display system with the fewest components.

2 FEATURES

Single-chip LCD controller/driver

Driver Output Circuits

- 160-segment / 160-common + 1-icon-common

On-chip Display Data RAM

- Capacity: 160x 161 x 2 = 51,520bits (Max)

Various Partial Display Features

- Applicable partial duty
- Partial window moving & data scrolling

Microprocessor Interface

- 8-bit parallel bi-directional interface supports 6800-series or 8080-series MPU
- 4-line serial interface support write-operation and read-status
- 9 bit 3-line serial interface support write-operation and read-status
- I^2C interface

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage booster with built-in boost-capacitors
- Extremely few external components: 3 capacitors
- Built-in voltage regulator with programmable contrast
- Built-in voltage follower supports LCD bias voltage Available bias: 1/9 ~ 1/14

Operating Voltage Range

- Digital Power (VDD1): 1.8V ~ 3.3V (TYP.)
- Analog Power (VDD2~VDD4): 2.8V ~ 3.3V (TYP.)
- LCD operation voltage (Vop = V0-XV0): 18V(Max.)

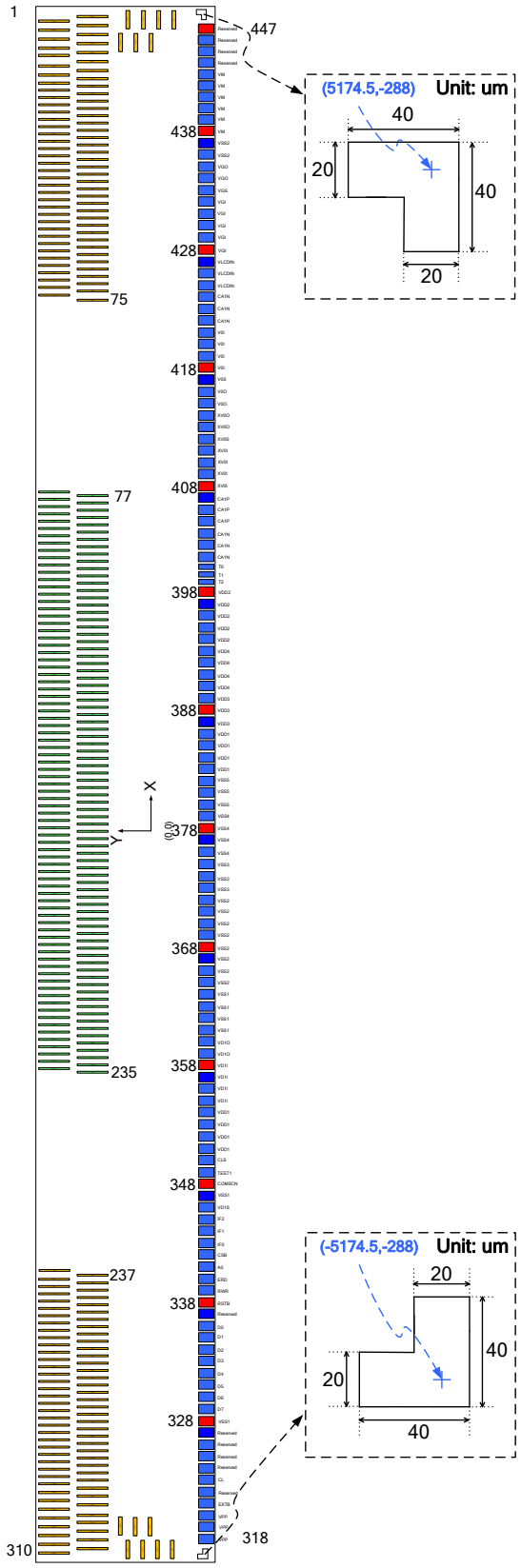
Built-in OTP−ROM for LCD Vop Optimization

Design for Consumer and Industrial Applications; Automotive Related Products are Excluded

Package Type: COG

ST75160	**6800 , 8080 , 4-Line, 3-Line Interface (without I^2C Interface)**	
ST75160i	**I^2C Interface**	

3 PAD ARRANGEMENT



ST75160-G2			
Chip Size		10455x682	
Chip Thickness	480	**Bump Height**	15
PAD No.		**Bump Size**	
1~317, 448~454		14x111	
318~320, 351~398, 402~447		62x63	
321~338, 343~350		60x63	
339~342		72x63	
399~401		22x63	
PAD No.		**Bump Pitch**	
1~317, 448~454		25	
318~320, 351~398, 402~447		80	
321~338, 343~350		78	
342~343, 338~339		84	
350~351, 317~318		79	
399~401		40	
401~402, 398~399		60	
339~342		90	
* Refer to “PAD CENTER COORDINATES” for ITO layout			

Unit: um

Figure 1 Chip Outline

4 PAD CENTER COORDINATES

PAD	NAME	X	Y
1	COM146	5157.5	118.5
2	COM144	5132.5	249.5
3	COM142	5107.5	118.5
4	COM140	5082.5	249.5
5	COM138	5057.5	118.5
6	COM136	5032.5	249.5
7	COM134	5007.5	118.5
8	COM132	4982.5	249.5
9	COM130	4957.5	118.5
10	COM128	4932.5	249.5
11	COM126	4907.5	118.5
12	COM124	4882.5	249.5
13	COM122	4857.5	118.5
14	COM120	4832.5	249.5
15	COM118	4807.5	118.5
16	COM116	4782.5	249.5
17	COM114	4757.5	118.5
18	COM112	4732.5	249.5
19	COM110	4707.5	118.5
20	COM108	4682.5	249.5
21	COM106	4657.5	118.5
22	COM104	4632.5	249.5
23	COM102	4607.5	118.5
24	COM100	4582.5	249.5
25	COM98	4557.5	118.5
26	COM96	4532.5	249.5
27	COM94	4507.5	118.5
28	COM92	4482.5	249.5
29	COM90	4457.5	118.5
30	COM88	4432.5	249.5
31	COM86	4407.5	118.5
32	COM84	4382.5	249.5
33	COM82	4357.5	118.5

PAD	NAME	X	Y
34	COM80	4332.5	249.5
35	COM78	4307.5	118.5
36	COM76	4282.5	249.5
37	COM74	4257.5	118.5
38	COM72	4232.5	249.5
39	COM70	4207.5	118.5
40	COM68	4182.5	249.5
41	COM66	4157.5	118.5
42	COM64	4132.5	249.5
43	COM62	4107.5	118.5
44	COM60	4082.5	249.5
45	COM58	4057.5	118.5
46	COM56	4032.5	249.5
47	COM54	4007.5	118.5
48	COM52	3982.5	249.5
49	COM50	3957.5	118.5
50	COM48	3932.5	249.5
51	COM46	3907.5	118.5
52	COM44	3882.5	249.5
53	COM42	3857.5	118.5
54	COM40	3832.5	249.5
55	COM38	3807.5	118.5
56	COM36	3782.5	249.5
57	COM34	3757.5	118.5
58	COM32	3732.5	249.5
59	COM30	3707.5	118.5
60	COM28	3682.5	249.5
61	COM26	3657.5	118.5
62	COM24	3632.5	249.5
63	COM22	3607.5	118.5
64	COM20	3582.5	249.5
65	COM18	3557.5	118.5
66	COM16	3532.5	249.5

PAD	NAME	X	Y
67	COM14	3507.5	118.5
68	COM12	3482.5	249.5
69	COM10	3457.5	118.5
70	COM8	3432.5	249.5
71	COM6	3407.5	118.5
72	COM4	3382.5	249.5
73	COM2	3357.5	118.5
74	COM0	3332.5	249.5
75	COMS	3307.5	118.5
76	SEG0	1987.5	249.5
77	SEG1	1962.5	118.5
78	SEG2	1937.5	249.5
79	SEG3	1912.5	118.5
80	SEG4	1887.5	249.5
81	SEG5	1862.5	118.5
82	SEG6	1837.5	249.5
83	SEG7	1812.5	118.5
84	SEG8	1787.5	249.5
85	SEG9	1762.5	118.5
86	SEG10	1737.5	249.5
87	SEG11	1712.5	118.5
88	SEG12	1687.5	249.5
89	SEG13	1662.5	118.5
90	SEG14	1637.5	249.5
91	SEG15	1612.5	118.5
92	SEG16	1587.5	249.5
93	SEG17	1562.5	118.5
94	SEG18	1537.5	249.5
95	SEG19	1512.5	118.5
96	SEG20	1487.5	249.5
97	SEG21	1462.5	118.5
98	SEG22	1437.5	249.5
99	SEG23	1412.5	118.5
100	SEG24	1387.5	249.5
101	SEG25	1362.5	118.5

PAD	NAME	X	Y
102	SEG26	1337.5	249.5
103	SEG27	1312.5	118.5
104	SEG28	1287.5	249.5
105	SEG29	1262.5	118.5
106	SEG30	1237.5	249.5
107	SEG31	1212.5	118.5
108	SEG32	1187.5	249.5
109	SEG33	1162.5	118.5
110	SEG34	1137.5	249.5
111	SEG35	1112.5	118.5
112	SEG36	1087.5	249.5
13	SEG37	1062.5	118.5
114	SEG38	1037.5	249.5
115	SEG39	1012.5	118.5
116	SEG40	987.5	249.5
117	SEG41	962.5	118.5
118	SEG42	937.5	249.5
119	SEG43	912.5	118.5
120	SEG44	887.5	249.5
121	SEG45	862.5	118.5
122	SEG46	837.5	249.5
123	SEG47	812.5	118.5
124	SEG48	787.5	249.5
125	SEG49	762.5	118.5
126	SEG50	737.5	249.5
127	SEG51	712.5	118.5
128	SEG52	687.5	249.5
129	SEG53	662.5	118.5
130	SEG54	637.5	249.5
131	SEG55	612.5	118.5
132	SEG56	587.5	249.5
133	SEG57	562.5	118.5
134	SEG58	537.5	249.5
135	SEG59	512.5	118.5
136	SEG60	487.5	249.5

PAD	NAME	X	Y
137	SEG61	462.5	118.5
138	SEG62	437.5	249.5
139	SEG63	412.5	118.5
140	SEG64	387.5	249.5
141	SEG65	362.5	118.5
142	SEG66	337.5	249.5
143	SEG67	312.5	118.5
144	SEG68	287.5	249.5
145	SEG69	262.5	118.5
146	SEG70	237.5	249.5
147	SEG71	212.5	118.5
148	SEG72	187.5	249.5
149	SEG73	162.5	118.5
150	SEG74	137.5	249.5
151	SEG75	112.5	118.5
152	SEG76	87.5	249.5
153	SEG77	62.5	118.5
154	SEG78	37.5	249.5
155	SEG79	12.5	118.5
156	SEG80	-12.5	249.5
157	SEG81	-37.5	118.5
158	SEG82	-62.5	249.5
159	SEG83	-87.5	118.5
160	SEG84	-112.5	249.5
161	SEG85	-137.5	118.5
162	SEG86	-162.5	249.5
163	SEG87	-187.5	118.5
164	SEG88	-212.5	249.5
165	SEG89	-237.5	118.5
166	SEG90	-262.5	249.5
167	SEG91	-287.5	118.5
168	SEG92	-312.5	249.5
169	SEG93	-337.5	118.5
170	SEG94	-362.5	249.5
171	SEG95	-387.5	118.5

PAD	NAME	X	Y
172	SEG96	-412.5	249.5
173	SEG97	-437.5	118.5
174	SEG98	-462.5	249.5
175	SEG99	-487.5	118.5
176	SEG100	-512.5	249.5
177	SEG101	-537.5	118.5
178	SEG102	-562.5	249.5
179	SEG103	-587.5	118.5
180	SEG104	-612.5	249.5
181	SEG105	-637.5	118.5
182	SEG106	-662.5	249.5
183	SEG107	-687.5	118.5
184	SEG108	-712.5	249.5
185	SEG109	-737.5	118.5
186	SEG110	-762.5	249.5
187	SEG111	-787.5	118.5
188	SEG112	-812.5	249.5
189	SEG113	-837.5	118.5
190	SEG114	-862.5	249.5
191	SEG115	-887.5	118.5
192	SEG116	-912.5	249.5
193	SEG117	-937.5	118.5
194	SEG118	-962.5	249.5
195	SEG119	-987.5	118.5
196	SEG120	-1012.5	249.5
197	SEG121	-1037.5	118.5
198	SEG122	-1062.5	249.5
199	SEG123	-1087.5	118.5
200	SEG124	-1112.5	249.5
201	SEG125	-1137.5	118.5
202	SEG126	-1162.5	249.5
203	SEG127	-1187.5	118.5
204	SEG128	-1212.5	249.5
205	SEG129	-1237.5	118.5
206	SEG130	-1262.5	249.5

PAD	NAME	X	Y
207	SEG131	-1287.5	118.5
208	SEG132	-1312.5	249.5
209	SEG133	-1337.5	118.5
210	SEG134	-1362.5	249.5
211	SEG135	-1387.5	118.5
212	SEG136	-1412.5	249.5
213	SEG137	-1437.5	118.5
214	SEG138	-1462.5	249.5
215	SEG139	-1487.5	118.5
216	SEG140	-1512.5	249.5
217	SEG141	-1537.5	118.5
218	SEG142	-1562.5	249.5
219	SEG143	-1587.5	118.5
220	SEG144	-1612.5	249.5
221	SEG145	-1637.5	118.5
222	SEG146	-1662.5	249.5
223	SEG147	-1687.5	118.5
224	SEG148	-1712.5	249.5
225	SEG149	-1737.5	118.5
226	SEG150	-1762.5	249.5
227	SEG151	-1787.5	118.5
228	SEG152	-1812.5	249.5
229	SEG153	-1837.5	118.5
230	SEG154	-1862.5	249.5
231	SEG155	-1887.5	118.5
232	SEG156	-1912.5	249.5
233	SEG157	-1937.5	118.5
234	SEG158	-1962.5	249.5
235	SEG159	-1987.5	118.5
236	COMS	-3307.5	249.5
237	COM1	-3332.5	118.5
238	COM3	-3357.5	249.5
239	COM5	-3382.5	118.5
240	COM7	-3407.5	249.5
241	COM9	-3432.5	118.5

PAD	NAME	X	Y
242	COM11	-3457.5	249.5
243	COM13	-3482.5	118.5
244	COM15	-3507.5	249.5
245	COM17	-3532.5	118.5
246	COM19	-3557.5	249.5
247	COM21	-3582.5	118.5
248	COM23	-3607.5	249.5
249	COM25	-3632.5	118.5
250	COM27	-3657.5	249.5
251	COM29	-3682.5	118.5
252	COM31	-3707.5	249.5
253	COM33	-3732.5	118.5
254	COM35	-3757.5	249.5
255	COM37	-3782.5	118.5
256	COM39	-3807.5	249.5
257	COM41	-3832.5	118.5
258	COM43	-3857.5	249.5
259	COM45	-3882.5	118.5
260	COM47	-3907.5	249.5
261	COM49	-3932.5	118.5
262	COM51	-3957.5	249.5
263	COM53	-3982.5	118.5
264	COM55	-4007.5	249.5
265	COM57	-4032.5	118.5
266	COM59	-4057.5	249.5
267	COM61	-4082.5	118.5
268	COM63	-4107.5	249.5
269	COM65	-4132.5	118.5
270	COM67	-4157.5	249.5
271	COM69	-4182.5	118.5
272	COM71	-4207.5	249.5
273	COM73	-4232.5	118.5
274	COM75	-4257.5	249.5
275	COM77	-4282.5	118.5
276	COM79	-4307.5	249.5

PAD	NAME	X	Y
277	COM81	-4332.5	118.5
278	COM83	-4357.5	249.5
279	COM85	-4382.5	118.5
280	COM87	-4407.5	249.5
281	COM89	-4432.5	118.5
282	COM91	-4457.5	249.5
283	COM93	-4482.5	118.5
284	COM95	-4507.5	249.5
285	COM97	-4532.5	118.5
286	COM99	-4557.5	249.5
287	COM101	-4582.5	118.5
288	COM103	-4607.5	249.5
289	COM105	-4632.5	118.5
290	COM107	-4657.5	249.5
291	COM109	-4682.5	118.5
292	COM111	-4707.5	249.5
293	COM113	-4732.5	118.5
294	COM115	-4757.5	249.5
295	COM117	-4782.5	118.5
296	COM119	-4807.5	249.5
297	COM121	-4832.5	118.5
298	COM123	-4857.5	249.5
299	COM125	-4882.5	118.5
300	COM127	-4907.5	249.5
301	COM129	-4932.5	118.5
302	COM131	-4957.5	249.5
303	COM133	-4982.5	118.5
304	COM135	-5007.5	249.5
305	COM137	-5032.5	118.5
306	COM139	-5057.5	249.5
307	COM141	-5082.5	118.5
308	COM143	-5107.5	249.5
309	COM145	-5132.5	118.5
310	COM147	-5157.5	249.5
311	COM149	-5005	-11
312	COM151	-5136	-36
313	COM153	-5005	-61
314	COM155	-5136	-86
315	COM157	-5005	-111
316	COM159	-5136	-136
317	COMS	-5136	-186
318	VPP	-5094	-273.5
319	VPP	-5014	-273.5
320	VPP	-4934	-273.5
321	EXTB	-4855	-273.5
322	Reserved	-4777	-273.5
323	CL	-4699	-273.5
324	Reserved	-4621	-273.5
325	Reserved	-4543	-273.5
326	Reserved	-4465	-273.5
327	Reserved	-4387	-273.5
328	VSS1	-4309	-273.5
329	D7	-4231	-273.5
330	D6	-4153	-273.5
331	D5	-4075	-273.5
332	D4	-3997	-273.5
333	D3	-3919	-273.5
334	D2	-3841	-273.5
335	D1	-3763	-273.5
336	D0	-3685	-273.5
337	Reserved	-3607	-273.5
338	RSTB	-3529	-273.5
339	RWR	-3445	-273.5
340	ERD	-3355	-273.5
341	A0	-3265	-273.5
342	CSB	-3175	-273.5
343	IF0	-3091	-273.5
344	IF1	-3013	-273.5
345	IF2	-2935	-273.5
346	VD1S	-2857	-273.5

PAD	NAME	X	Y
347	VSS1	-2779	-273.5
348	COMSCN	-2701	-273.5
349	TEST1	-2623	-273.5
350	CLS	-2545	-273.5
351	VDD1	-2466	-273.5
352	VDD1	-2386	-273.5
353	VDD1	-2306	-273.5
354	VDD1	-2226	-273.5
355	VD1I	-2146	-273.5
356	VD1I	-2066	-273.5
357	VD1I	-1986	-273.5
358	VD1I	-1906	-273.5
359	VD1O	-1826	-273.5
360	VD1O	-1746	-273.5
361	VSS1	-1666	-273.5
362	VSS1	-1586	-273.5
363	VSS1	-1506	-273.5
364	VSS1	-1426	-273.5
365	VSS2	-1346	-273.5
366	VSS2	-1266	-273.5
367	VSS2	-1186	-273.5
368	VSS2	-1106	-273.5
369	VSS2	-1026	-273.5
370	VSS2	-946	-273.5
371	VSS2	-866	-273.5
372	VSS2	-786	-273.5
373	VSS3	-706	-273.5
374	VSS3	-626	-273.5
375	VSS3	-546	-273.5
376	VSS4	-466	-273.5
377	VSS4	-386	-273.5
378	VSS4	-306	-273.5
379	VSS4	-226	-273.5
380	VSS5	-146	-273.5
381	VSS5	-66	-273.5
382	VSS5	14	-273.5
383	VDD1	94	-273.5
384	VDD1	174	-273.5
385	VDD1	254	-273.5
386	VDD1	334	-273.5
387	VDD3	414	-273.5
388	VDD3	494	-273.5
389	VDD3	574	-273.5
390	VDD4	654	-273.5
391	VDD4	734	-273.5
392	VDD4	814	-273.5
393	VDD4	894	-273.5
394	VDD2	974	-273.5
395	VDD2	1054	-273.5
396	VDD2	1134	-273.5
397	VDD2	1214	-273.5
398	VDD2	1294	-273.5
399	T2	1354	-273.5
400	T1	1394	-273.5
401	T0	1434	-273.5
402	CA1N	1494	-273.5
403	CA1N	1574	-273.5
404	CA1N	1654	-273.5
405	CA1P	1734	-273.5
406	CA1P	1814	-273.5
407	CA1P	1894	-273.5
408	XV0I	1974	-273.5
409	XV0I	2054	-273.5
410	XV0I	2134	-273.5
411	XV0I	2214	-273.5
412	XV0S	2294	-273.5
413	XV0O	2374	-273.5
414	XV0O	2454	-273.5
415	V0O	2534	-273.5
416	V0O	2614	-273.5

PAD	NAME	X	Y
417	V0S	2694	-273.5
418	V0I	2774	-273.5
419	V0I	2854	-273.5
420	V0I	2934	-273.5
421	V0I	3014	-273.5
422	CA1N	3094	-273.5
423	CA1N	3174	-273.5
424	CA1N	3254	-273.5
425	VLCDIN	3334	-273.5
426	VLCDIN	3414	-273.5
427	VLCDIN	3494	-273.5
428	VGI	3574	-273.5
429	VGI	3654	-273.5
430	VGI	3734	-273.5
431	VGI	3814	-273.5
432	VGI	3894	-273.5
433	VGS	3974	-273.5
434	VGO	4054	-273.5
435	VGO	4134	-273.5
436	VSS2	4214	-273.5
437	VSS2	4294	-273.5
438	VM	4374	-273.5
439	VM	4454	-273.5
440	VM	4534	-273.5
441	VM	4614	-273.5
442	VM	4694	-273.5
443	VM	4774	-273.5
444	Reserved	4854	-273.5
445	Reserved	4934	-273.5
446	Reserved	5014	-273.5
447	Reserved	5094	-273.5
448	COMS	5136	-186
449	COM158	5136	-136
450	COM156	5005	-111
451	COM154	5136	-86
452	COM152	5005	-61
453	COM150	5136	-36
454	COM148	5005	-11

Unit :um

5 BLOCK DIAGRAM

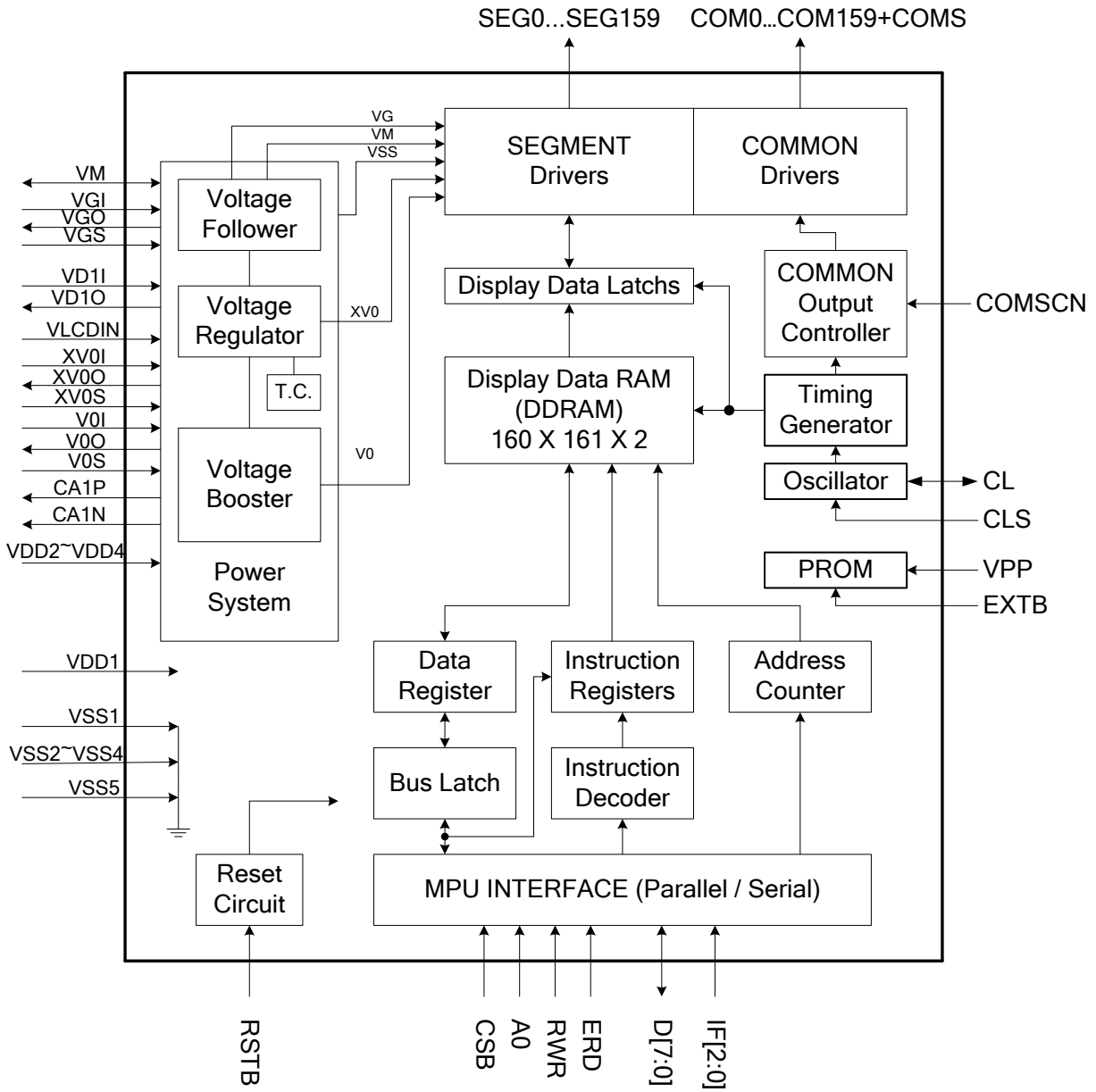


Figure 2 Block Diagram

6 PIN DESCRIPTION

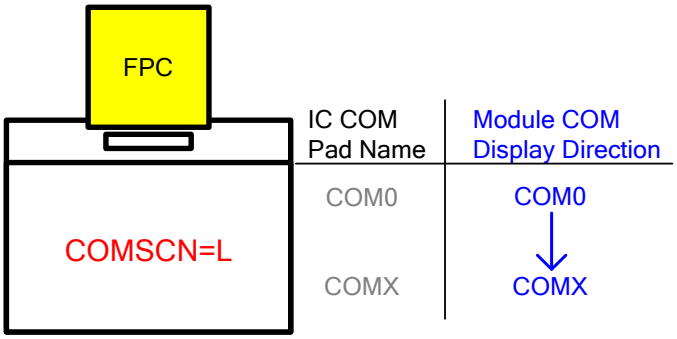
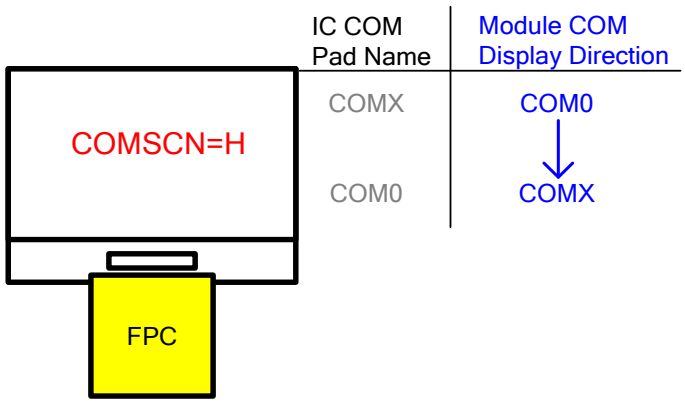
6.1 Power Supply Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>VDD1</td><td>Power</td><td>Digital power. If VDD1=VDD2, connect to VDD2 externally.</td></tr>
<tr><td>VDD2</td><td>Power</td><td>Analog power for internal booster. If VDD1=VDD2, connect to VDD1 externally.</td></tr>
<tr><td>VDD3</td><td>Power</td><td>Analog power for temperature compensation circuit.</td></tr>
<tr><td>VDD4</td><td>Power</td><td>Analog power for follower circuit.</td></tr>
<tr><td>VSS1</td><td>Power</td><td>Digital ground. Ground system should be connected together.</td></tr>
<tr><td>VSS2
VSS3
VSS4</td><td>Power</td><td>Analog ground. Ground system should be connected together.</td></tr>
<tr><td>VSS5</td><td>Power</td><td>Analog ground for external power supply and should be connected with VSS1~VSS4.</td></tr>
<tr><td>VD1S</td><td>I</td><td>Digital power source selection.
VD1S = “L”: the power source of digital circuit is VDD1.
VD1S = “H”: the power source of digital circuit is internal regulator.
<table>
<tr><th>VDD1 (TYP.)</th><th>Level of VD1S</th></tr>
<tr><td>1.8V</td><td>VSS1</td></tr>
<tr><td>2.8V</td><td>VDD1</td></tr>
<tr><td>3.0V</td><td>VDD1</td></tr>
<tr><td>3.3V</td><td>VDD1</td></tr>
</table></td></tr>
<tr><td>VD1I
VD1O</td><td>Power</td><td>VD1I is the power source of digital circuits.
VD1O is the VD1 output. VD1I and VD1O should be connected together.</td></tr>
<tr><td>CA1P
CA1N</td><td>O</td><td>DC/DC voltage converter. Connect a capacitor between CA1P and CA1N.</td></tr>
<tr><td>VLCDIN</td><td>Power</td><td>External voltage supply for power system.
If the internal voltage generator is used, VLCDIN has to be left open.</td></tr>
<tr><td>V0O
V0I
V0S</td><td>Power</td><td>Positive operating voltage of COM-drivers.
V0O is the output of the positive Vop generator.
V0I is the positive Vop supply of LCD drivers.
V0S is the sensor of the positive Vop generator.
V0O, V0I & V0S should be connected together by ITO.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>XV0O
XV0I
XV0S</td><td>Power</td><td>Negative operating voltage of COM-drivers.
XV0O is the output of the negative Vop generator.
XV0I is the negative Vop supply of LCD drivers.
XV0S is the sensor of the negative Vop generator.
XV0O, XV0I & XV0S should be connected together by ITO.</td></tr>
<tr><td>VGO
VGI
VGS
VM</td><td>Power</td><td>VG is the power of SEG-drivers. VM is the non-select voltage level of COM-drivers.
VGO is the output of the VG regulator.
VGI is the supply of SEG-drivers.
VGS is the sensor of the VG regulator.
VGO, VGI & VGS should be connected together by ITO.
VM is the I/O pin of LCD bias supply voltage.
Be sure the relationships (as shown below) among the LCD driving voltages:
V0 ≥ VG ≥ VM ≥ VSS ≥ XV0;
VG ≥ VM ≥ 0.9V;
VDD2 ≥ VG ≥ 1.8V
When this IC is operating, VG and VM are generated according to the bias setting shown below:
<table>
<tr><th>LCD Bias</th><th>VG</th><th>VM</th></tr>
<tr><td>1/N Bias</td><td>(2/N) x V0</td><td>(1/N) x V0</td></tr>
</table>
Note: N = 9~14</td></tr>
</table>

6.2 Driver Output Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG159</td><td>O</td><td>LCD SEG-driver outputs.
The display data and the polar-signal (M) control the output voltage of SEG-driver.
<table>
<tr><th rowspan="2">Display Data</th><th rowspan="2">M</th><th colspan="2">Segment Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Reverse Display</th></tr>
<tr><td>H</td><td>H</td><td>VG</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>H</td><td>VSS</td><td>VG</td></tr>
<tr><td>L</td><td>L</td><td>VG</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Sleep-In mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM159</td><td>O</td><td>LCD COM-driver outputs.
The internal scanning data and the polar-signal (M) control the output voltage of COM-driver.
<table>
<tr><th>Scan data</th><th>M</th><th>Common Driver Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>XV0</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>VM</td></tr>
<tr><td>L</td><td>L</td><td>VM</td></tr>
<tr><td colspan="2">Display OFF, Sleep-In mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>LCD common driver outputs for icons. There are four pins to choose if using icon. When icon is not used, left these pins open.</td></tr>
</table>

Name	Type	Description
COMSCN	I	Set scan direction of COM. 1. COMSCN="L"; COM0→COMX; IC is placed above the module.  2. COMSCN="H"; COMX→COM0; IC is placed below the module.  Note: COMX is determined by the DUTY setting.

6.3 Clock System Input

Name	Type	Description
CLS	I	Clock source selection pin. CLS="H": enable internal clock. CLS="L": disable internal clock and use external clock.
CL	I/O	For external clock. If CLS="H": this pin is the output of oscillator. If CLS="L": this pin is the input of oscillator.

6.4 Interface Logic Pins

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>RSTB</td><td>I</td><td>Reset input pin. When RSTB is “L”, internal initialization procedure is executed.</td></tr>
<tr><td>IF[2:0]</td><td>I</td><td>These pins select interface operation mode.
<table>
<tr><th>IF2</th><th>IF1</th><th>IF0</th><th>MPU interface type</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>4-line serial interface</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>I^2C serial interface</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>8-bit 6800 parallel interface</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>8-bit 8080 parallel interface</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>9-bit 3-line serial interface</td></tr>
</table>
Note: Refer to ““Parallel / Serial Interface” for detailed information.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select input pin.
CSB=“L”: This chip is selected and the MPU interface is active.
CSB=“H”: This chip is not selected and the MPU interface is disabled (D[7:0] are high impedance).
<u>There is no CSB pin in I^2C interface and it should be fixed to “L” by VSS1.</u></td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0 = "H": Indicates that D[7:0] are display data;
A0 = "L": Indicates that D[7:0] are control data.
There is no A0 pin in 3-Line SPI and I^2C interface. A0 should be fixed to “H” by VDD1.</td></tr>
<tr><td>RWR</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>6800-series</td><td>R/W</td><td>Read / Write control input pin
R/W = “H” : read
R/W = “L” : write</td></tr>
<tr><td>8080-series</td><td>/WR</td><td>Write enable input pin.
The data are latched at the rising edge of the /WR signal.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to VDD1.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>ERD</td><td>I</td><td>Read / Write execution control pin. (This pin is only used in parallel interface)
<table>
<tr><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>6800-series</td><td>E</td><td>Read / Write control input pin.
R/W = “H”: When E is “H”, data bus is in output status.
R/W = “L”: The data are latched at the falling edge of the E signal.</td></tr>
<tr><td>8080-series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, data bus is in output status.</td></tr>
</table>
This pin is not used in serial interfaces and should be connected to VDD1.</td></tr>
<tr><td rowspan="3">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: 8080 or 6800 mode
8 bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CSB is “H” , D[7:0] are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface : 4-line SPI or 3-line SPI mode
D[7:4] : fix to “H” by VDD1.
D[3:1] : serial input/output data (SDA).
D[0] : serial input clock (SCL).
<u>D1 to D3 must be connected together (SDA)</u>
When CSB is “H” , D[7:0] are high impedance.</td></tr>
<tr><td>I/O</td><td>When using serial interface : I^{2}C interface
D[7] : SA[1], I^{2}C slave address bit. Must be connected to VDD1 or VSS1.
D[6] : SA[0], I^{2}C slave address bit. Must be connected to VDD1 or VSS1.
D[5:4] : fix to “H” by VDD1.
D[3:2] : SDA_OUT, serial data and acknowledge output for the I^{2}C interface.
D[1] : SDA_IN, serial input data
D[0] : SCL, serial input clock .
<u>D1 to D3 must be connected together (SDA)</u>
<u>CSB must be fixed to “L” by VSS1.</u></td></tr>
</table>

Note:

1. After VDD1 is turned ON, all MPU interface pins should not be left OPEN.
2. By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully I^2C interface compatible. Separating acknowledge-output from serial data input is advantageous for chip-on-glass (COG) applications. In COG applications, the ITO resistance and the pull-up resistor will form a voltage divider, which affects acknowledge-signal level. Larger ITO resistance will raise the acknowledged-signal level and system cannot recognize this level as a valid logic “0” level. By separating SDA_IN from SDA_OUT, the IC can be used in a mode that ignores the acknowledge-bit. For applications which check acknowledge-bit, it is necessary to minimize the ITO resistance of the SDA_OUT trace to guarantee a valid low level

6.5 OTP Pins

Name	Type	Description
VPP	Power	The programming power supply of the built-in OTP. Apply external power 6.5V here when programming (> 8mA for successful programming).
EXTB	I	EXTB=“L”: Enable the extension operation mode. When programming OTP, connect EXTB to VSS1 externally. This pin has an internal pull-high resistor. Please leave this pin OPEN after special operation.

6.6 Test Pins

Name	Type	Description
T0-T2	Test	Reserved for test only. T0 can be floating or connected to VSS1. T1-T2 must be floating.
TEST1	Test	Reserved for testing only. Recommend setting to VDD1.
Reserved	Test	Reserved for test only, recommend setting to floating.

6.7 ITO Resistance Limitation

Pin Name	ITO Resister
V0I, V0O, V0S, XV0I, XV0O, XV0S, VGI, VGO, VGS,VM,CA1P,CA1N , V_{LCDIN} , (I2C.SDA) (I2C.SCL)	<100Ω
VPP, VDD1~VDD4, VSS1~VSS5	<50Ω
A0, ERD, RWR, CSB, D[7:0], (SPI.SDA), (SPI.SCL)	<700Ω
RSTB	1~3KΩ
COMSCN, IF[2:0], CLS, EXTB, TEST1, T0, VD1S	<1KΩ
CL, T[2:1], Reserved	Floating

Note:

1. Make sure that the ITO resistance of COM0 ~ COM159 is equal, and so is it of SEG0 ~ SEG159.
2. These limitations include the bottleneck of ITO layout.
3. Refer to the application note for “ITO Layout Guide”.

6.8 ITO Layout Guide

For V0, XV0, VG, VDD and VSS- The ITO layout suggestion is shown as below:

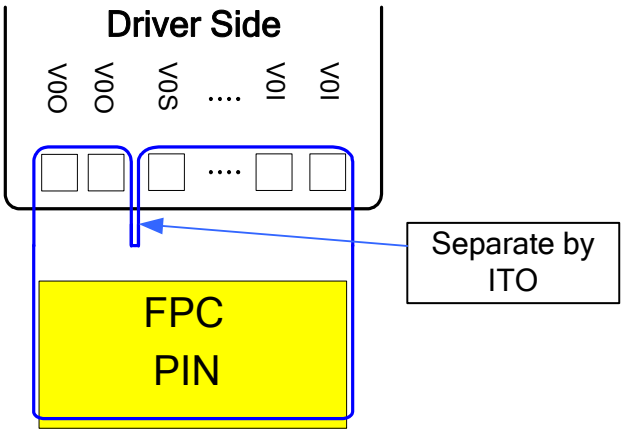


Figure 3 V0 ITO Layout

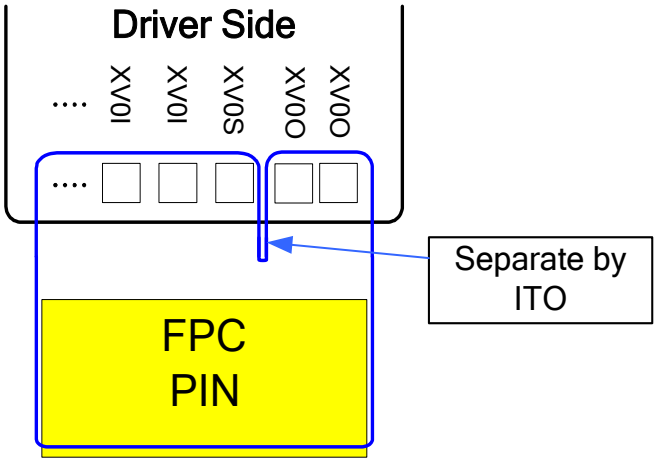


Figure 4 XV0 ITO Layout

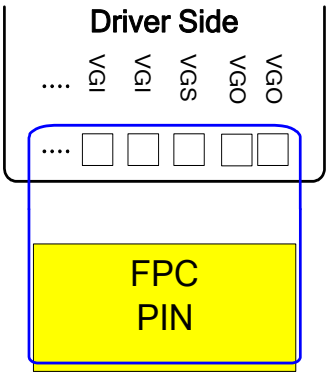


Figure 5 VG ITO Layout

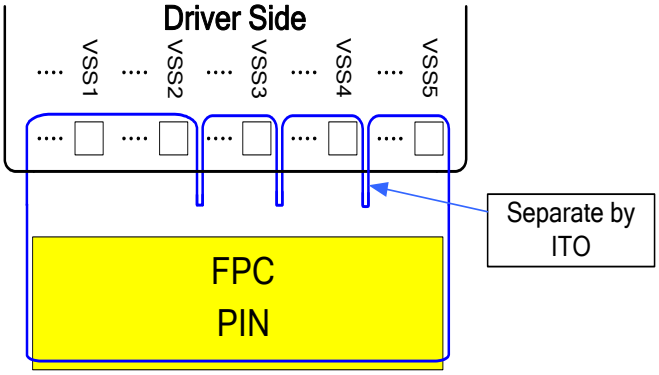
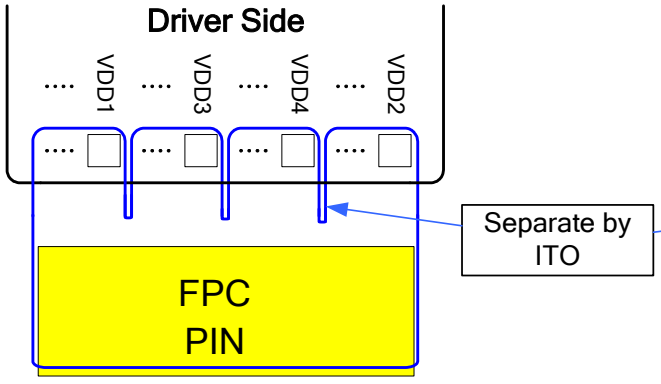
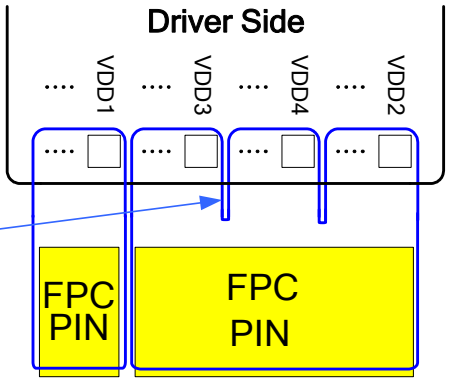


Figure 6 VSS ITO Layout



Single VDD: VDDI and VDDA together



Dual VDD: VDDI and VDDA separately

Figure 7 VDD ITO Layout

6.9 For VPP

This is the power source for programming the internal OTP. If the ITO resistance is too high, the operation current will cause the voltage drop while programming OTP. Please try to keep the ITO resistance as low as possible.

6.10 Enhance ESD performance for COG application

1. Increase RSTB resistance:

Figure 8 RSTB ITO Layout

2. Add ESD protection ring:

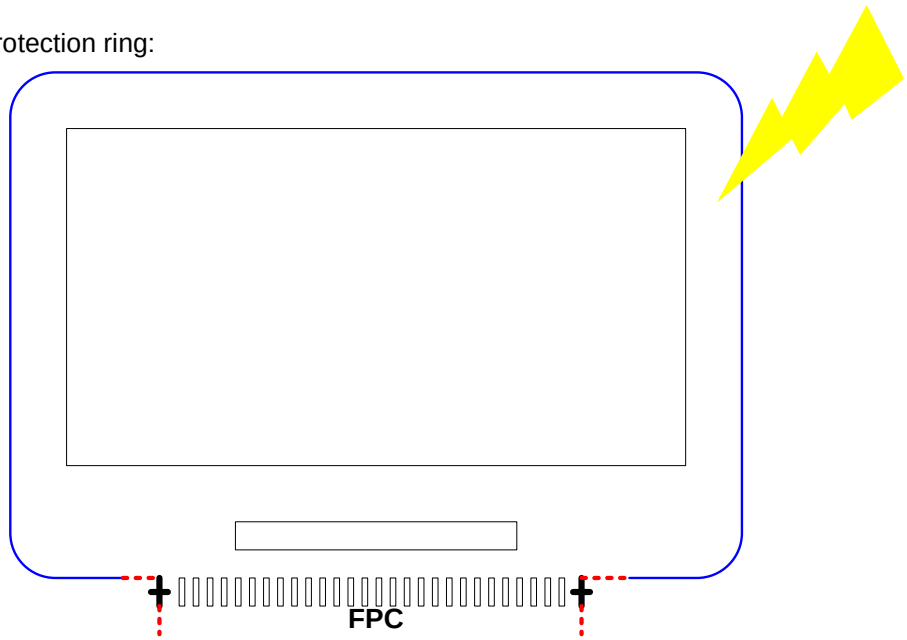
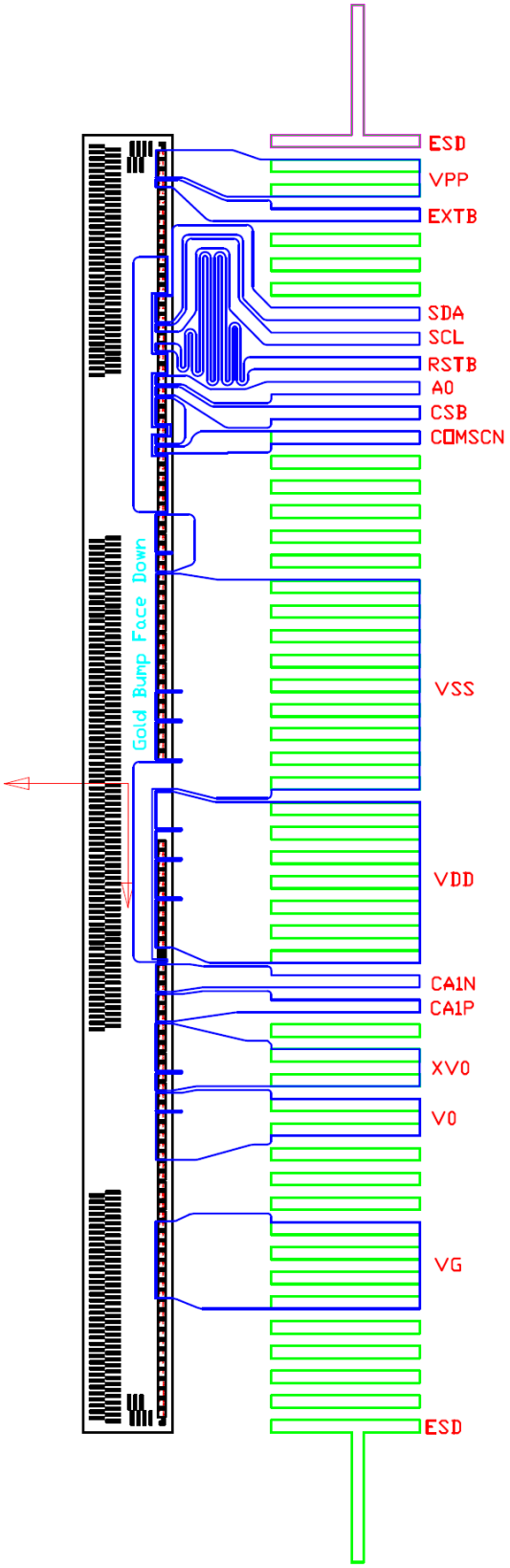


Figure 9 Air ESD Protection Ring

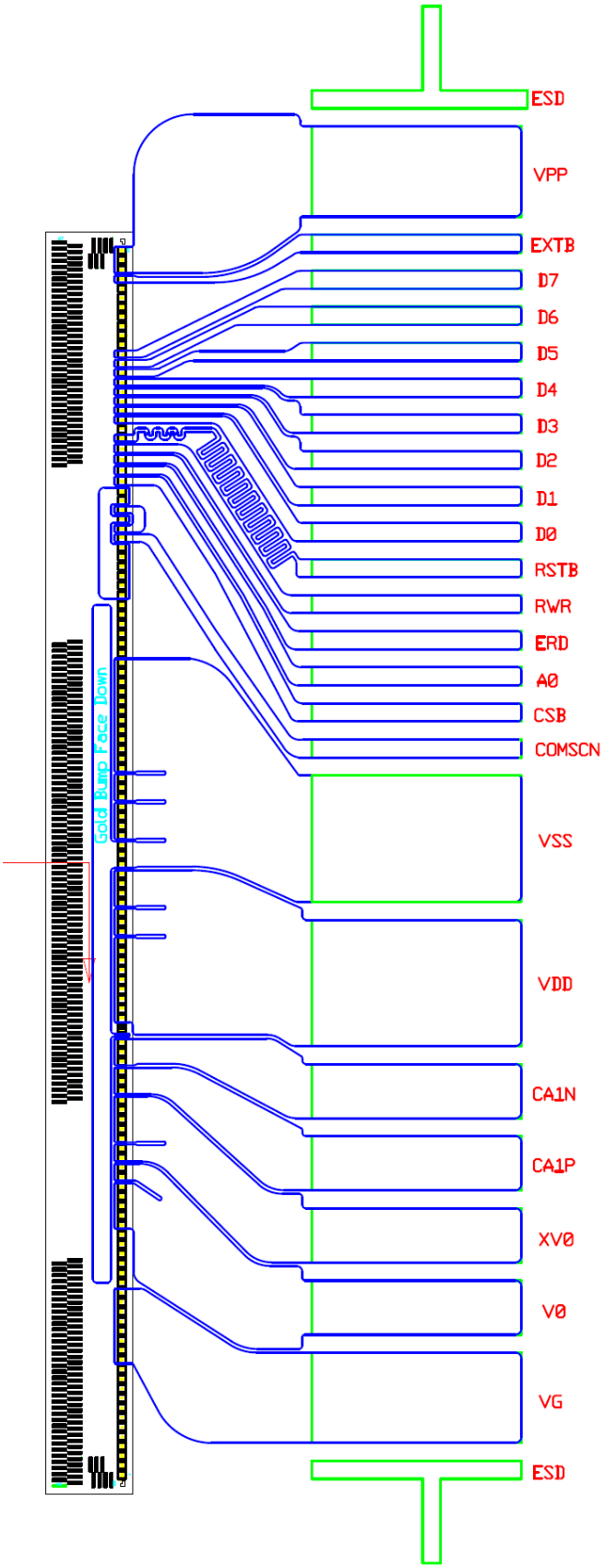
Note: Please short the ESD protection ring to VSS of external device.

6.11 ITO Layout Reference

The reference ITO layout is shown below: Example (4-Line SPI)



The reference ITO layout is shown below: Example (8080 series)



7 FUNCTION DESCRIPTION

7.1 Microprocessor Interface

7.1.1 Chip Select Input

CSB pin is used for chip selection. ST75160 can interface with an MPU when CSB is "L". If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial, 3-Line serial and I^2C interface, the internal shift register and serial counter are reset when CSB is “H”.

7.1.2 Parallel / Serial Interface

ST75160 has four types of interface for kinds of MPU. The MPU interface is selected by IF[2:0] pins as shown in **Table 1**.

Table 1 Parallel/Serial Interface Mode

Type	IF2	IF1	IF0	Interface mode
Serial	L	L	L	4-line serial interface
	L	L	H	I^2C serial interface
	H	L	L	9 bit 3-line serial interface
Parallel	L	H	L	8bit 6800-series MPU mode
	L	H	H	8bit 8080-series MPU mode

7.1.3 Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by IF[2:0] as shown in **Table 2**. The data transfer type is determined by signals of A0, ERD and RWR as shown in **Table 3**.

Table 2 Microprocessor Selection for Parallel Interface

IF2	IF1	IF0	CSB	A0	ERD	RWR	D[7:0]	MPU Interface
L	H	L	CSB	A0	E	R/W	D[7:0]	6800-series
L	H	H			/RD	/WR		8080-series

Table 3 Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

7.1.4 Setting Serial Interface

Interface	CSB	A0	ERD	RWR	D[7:0]
4-Line SPI	CSB	A0	---	---	D[0]= SCL, D[1:3]=SDA, D[4:7]= ---
3-Line SPI	CSB	---	---	---	D[0]= SCL, D[1:3]=SDA, D[4:7]= ---
I^2C interface	L	---	---	---	D[0]=SCL, D1=SDA_IN, D[3:2]=SDA_OUT, D[5:4]= ---, D[7:6]=SA[1:0]. Refer to I^2C interface.

* The un-used pins are marked as "---" and should be fixed to "H" by VDD1.

Note:

1. The option setting to be "H" should connect to VDD1.
2. The option setting to be "L" should connect to VSS1.

7.1.5 4-Line Serial Interface

ST75160 is active when CSB is "L", serial data (SDA) and serial clock (SCL) inputs are enabled. When CSB is "H", ST75160 is not active, the internal 8-bit shift register and 3-bit counter are reset. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCL). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.

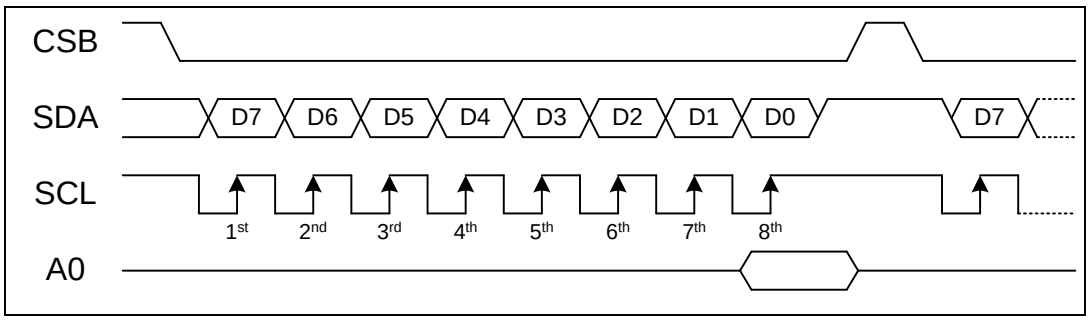


Figure 10 Write Operation of 4-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

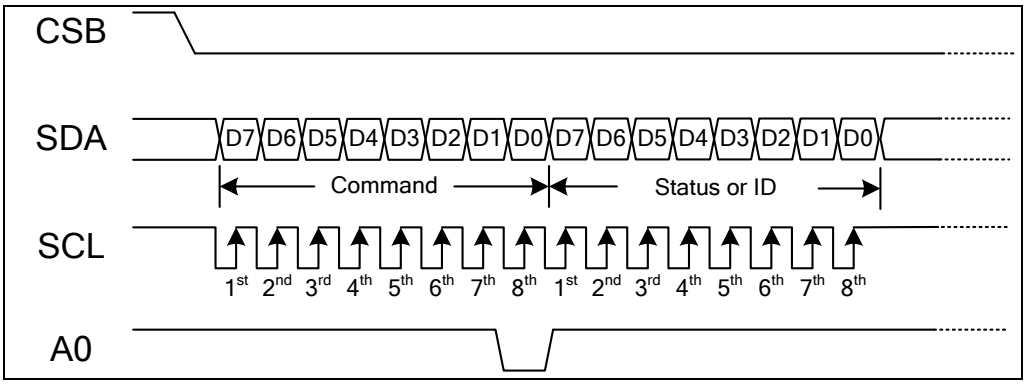


Figure 11 Read Operation of 4-Line SPI

7.1.6 3-Line Serial Interface

In 3-Line interface, A0 pin is not available. The 1st output bit defines command byte or parameter byte.

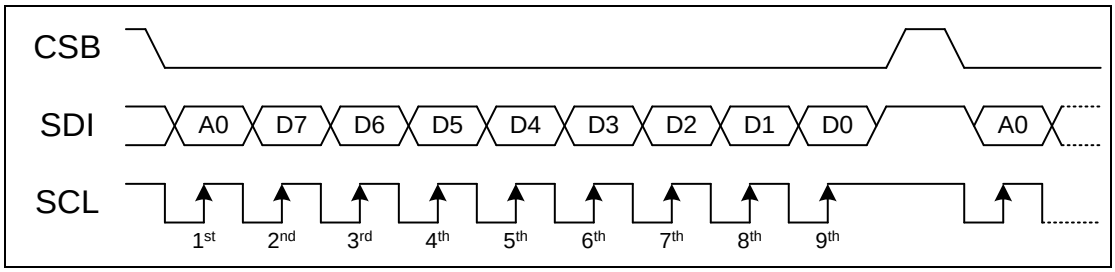


Figure 12 Write Operation of 3-Line SPI

After entering the “Read Status” instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

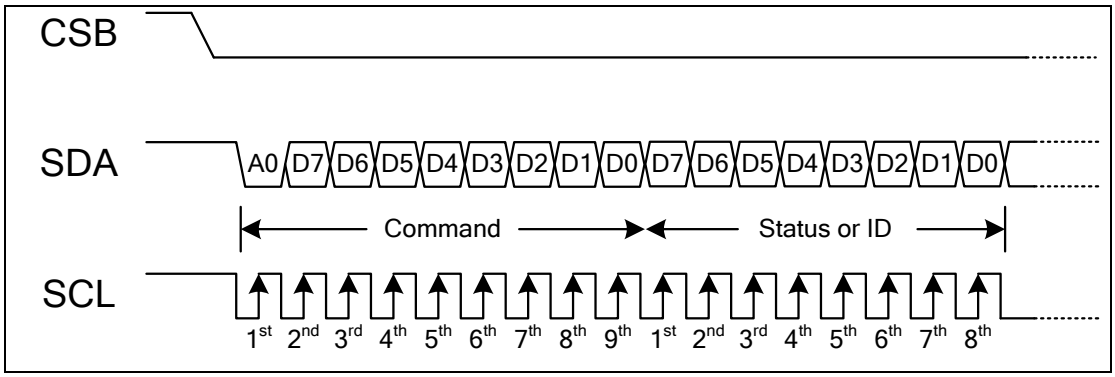


Figure 13 Read Operation of 3-Line SPI

7.1.7 I²C Interface

The I²C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in **Figure 14**.

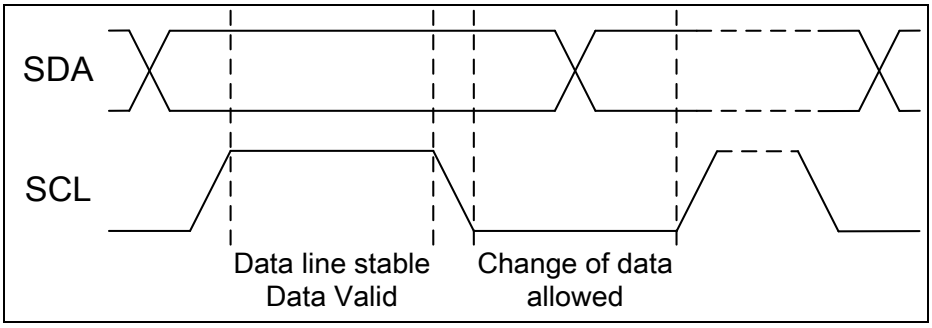


Figure 14 Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA, while SCL is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in **Figure 15**.

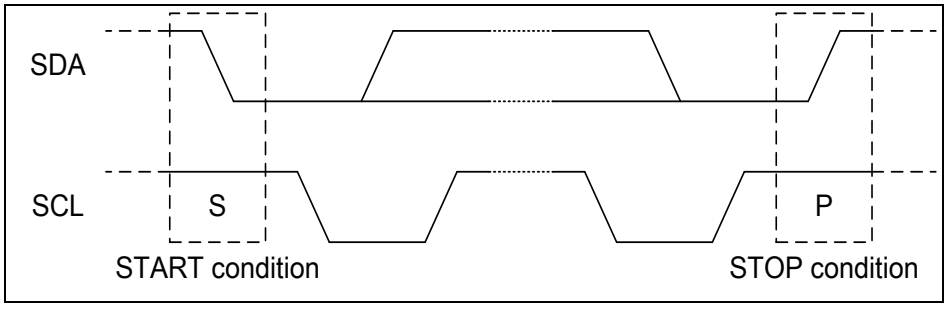


Figure 15 Definition of START and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in **Figure 16** and some word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.
- Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
- Arbitration: the procedure to ensure that, if more than one master tries to control the bus simultaneously, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.

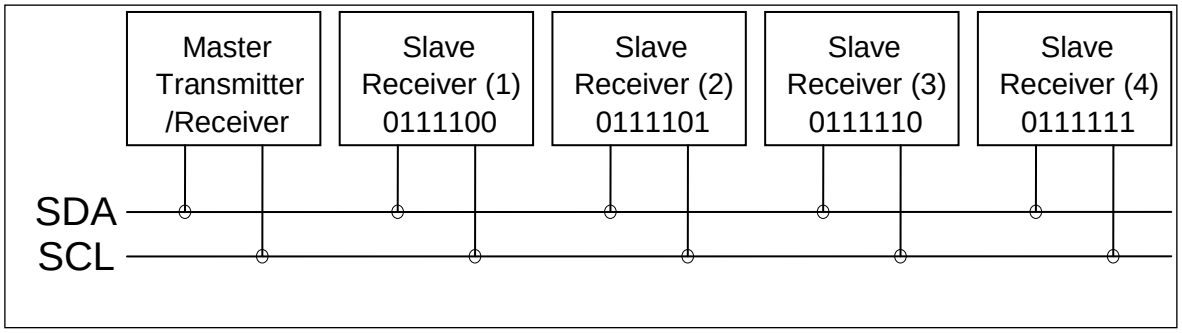


Figure 16 System Configuration

ACKNOWLEDGEMENT

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter during the time when the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge-bit after the reception of each byte. A master receiver must also generate an acknowledge-bit after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge-bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I^2C Interface is illustrated in **Figure 17**.

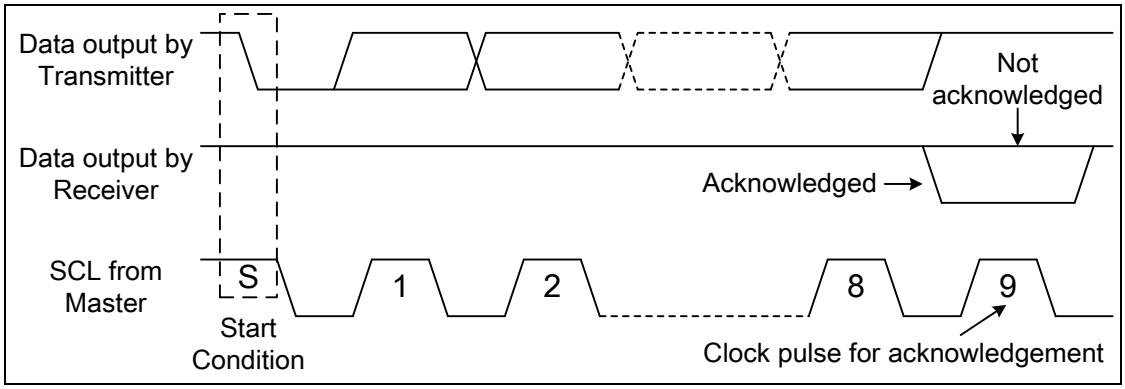


Figure 17 Acknowledgement of I²C Interface

I²C INTERFACE PROTOCOL

ST75160 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**00**, 0111**01**, 0111**10** and 0111**11**) are reserved for ST75160. The least significant 2 bits of the slave address is set by connecting SA0 and SA1 to either logic 0 (VSS1) or logic 1 (VDD1).The I²C Interface protocol is illustrated in **Figure 18**.

The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address and A0. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command or data words are followed and define the status of the addressed slaves.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST75160 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST75160 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

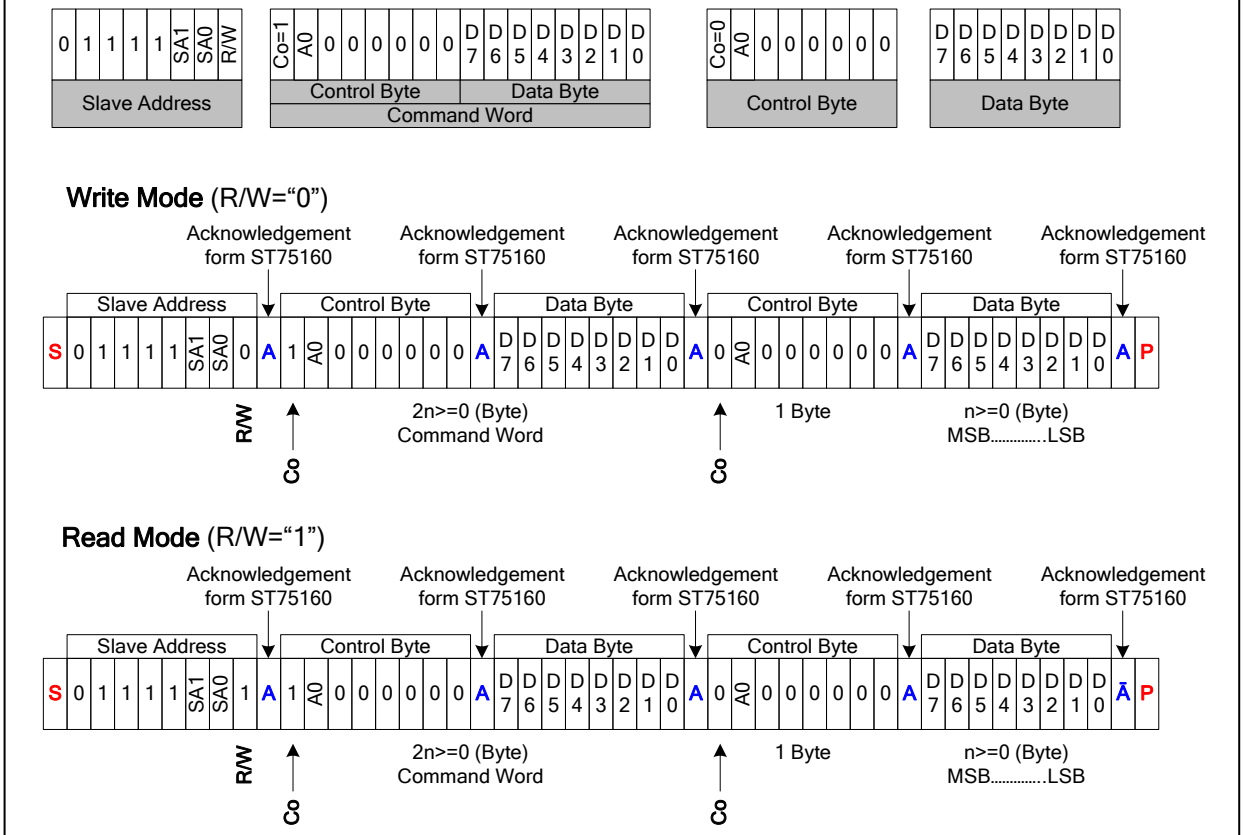


Figure 18 I²C Interface Protocol

Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

7.2 Data Transfer

ST75160 uses bus holder and internal data bus for data transfer with MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in **Figure 19**. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in **Figure 20**. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

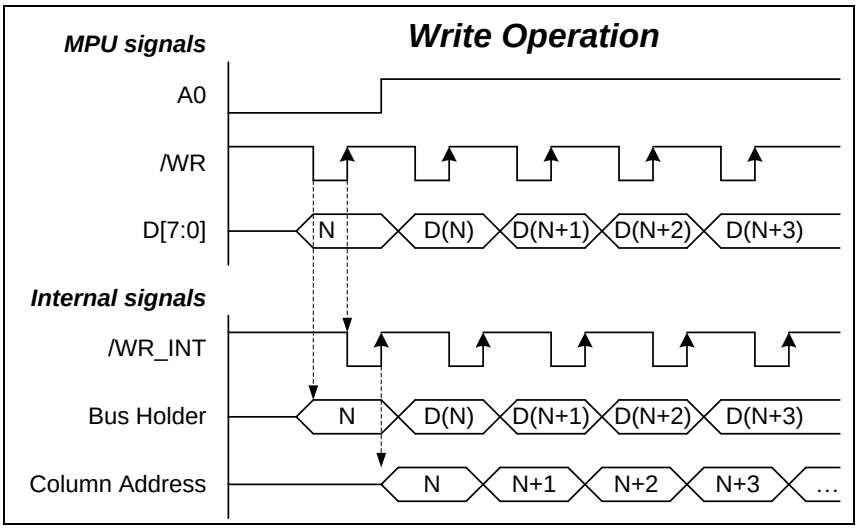


Figure 19 Data Transfer: Write

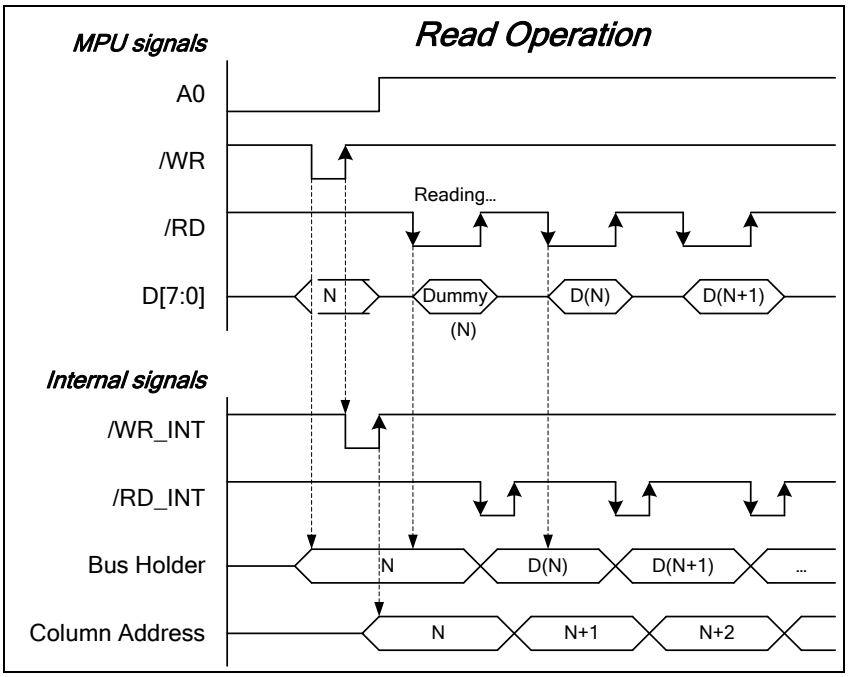
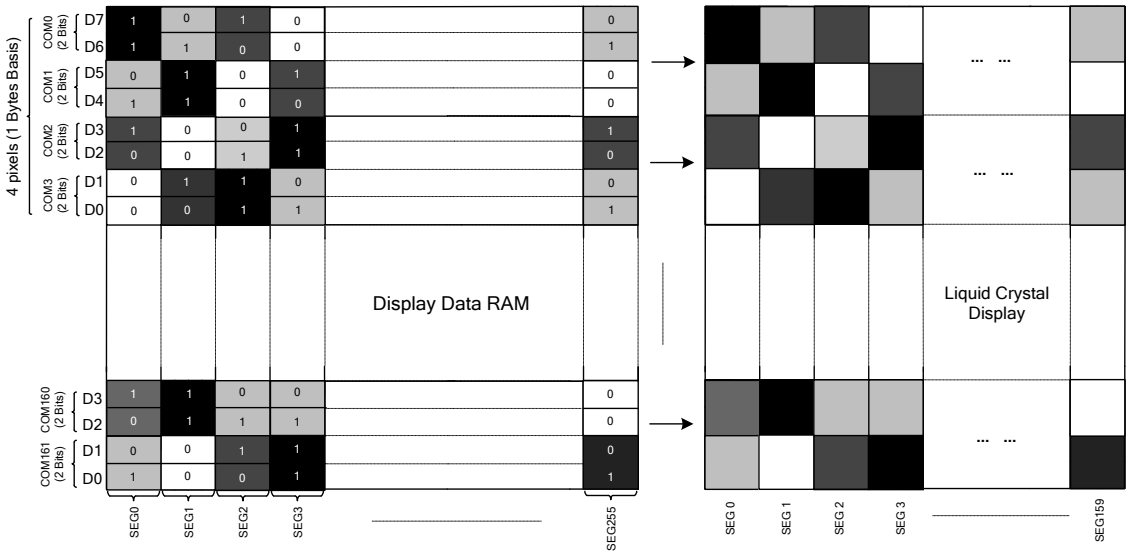


Figure 20 Data Transfer: Read

7.3 Display Data RAM (DDRAM)

ST75160 containing a 160x161x2 bit static RAM stores the display data. The display data RAM (DDRAM) stores the pixel data of the LCD. The built-in DDRAM is an addressable memory array with 160 columns by 161 rows. ST75160 provides 2 kinds of display modes (4-Gray/Monochrome scale mode) and a fast-addressing mode for fast updating display data. Each page address represents different sub-COMs in different display mode. For example, in 4-Gray/Monochrome scale mode setting the page address to “00h” means that upcoming 8 bits data is addressing to COM0~COM3/COM0~COM7 (refer to **Figure 21**, **Figure 22**). The column address is directly related to the SEG output number. The LCD controller reads the pixel data in DDRAM, and then it outputs to COM/SEG pad. While the LCD controller operates independently, display data can be written into DDRAM at the same time and data is also being displayed on LCD panel without causing the abnormal display.



2 Bits Data N=0~3		DDRAM		LCD
D2N+1	D2N			
1	1	1	1	
0	0	0	0	
1	0	1	0	
0	1	0	1	

Figure 21 DDRAM Mapping (4-Level Gray Scale Mode)

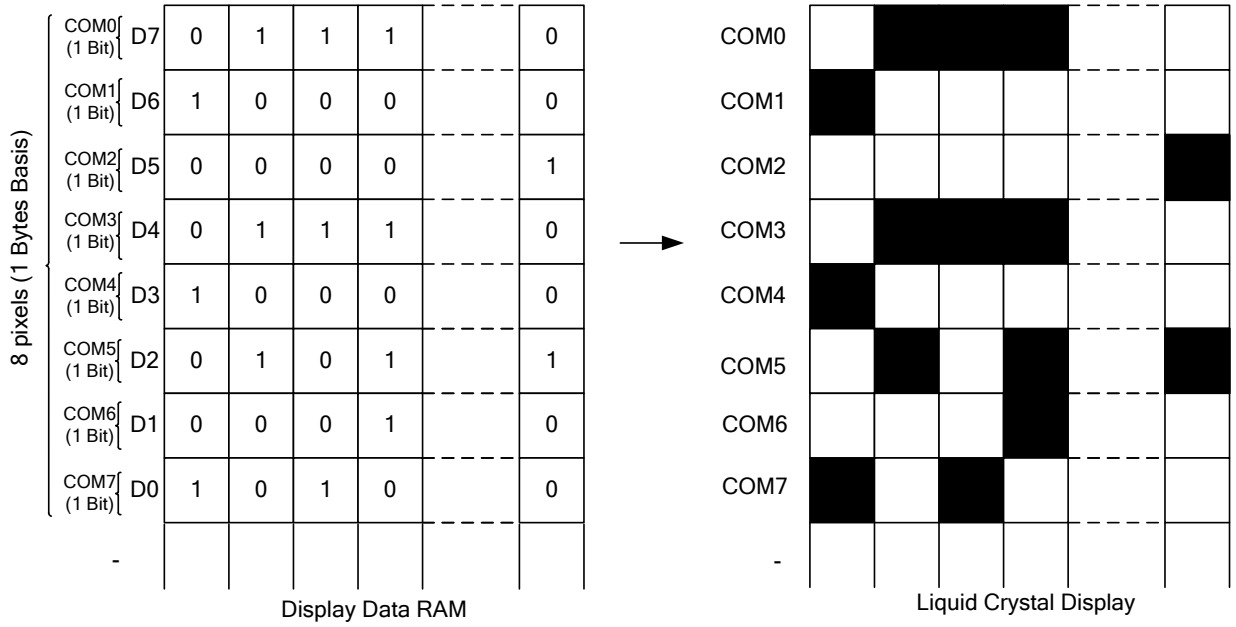


Figure 22 DDRAM Mapping (Monochrome Mode)

7.3.1 Page Address Circuit

Use the set page address command and set column address command to specify DDRAM address to be accessed as shown in **Figure 27**. This circuit controls the address in the page direction when MPU accesses the DDRAM or read the DDRAM to display image on the LCD. When the page-direction scan is specified with "Data Scan Direction"command and the address are increased from the start up to the end page, the column address is increased by 1 and the page address returns to the start page.

In the READ operation, as the end page is reached, the column address is automatically increased by 1 and the page address returns to the start page.

User may inverse the correspondence between the DDRAM address and common output via the address normal/inverse parameter of "Data Scan Direction" command.

7.3.2 Column Address Circuit

This circuit is to control the address in the column direction when MPU accesses the DDRAM. When the column-direction scan is specified with "Data Scan Direction" command and the address are increased from the start up to the end column, the page address is increased by 1 and the column address returns to the start column.

In the READ operation, the column address is also automatically increased by 1 and returns to the start page as the end column is reached.

Just like the page address control circuit, users may inverse the correspondence between the DDRAM column address and segment output via the column address normal/inverse parameter of "Data Scan Direction" command. This arrangement makes the chip layout on the LCD module flexible.

7.3.3 I/O Buffer Circuit

It is the bi-directional buffer when MPU reads or writes the DDRAM. Since the READ or WRITE operation of MPU to DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

7.3.4 Display Data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since display normal/inverse and display on/off commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

7.3.5 Data Orientation

By setting control flag “DO” (Refer to Data Format Select Command),, the input Data written into DDRAM can have the LSB on top (DO=0, **Figure 23** & **Figure 25**) or at bottom (DO=1, **Figure 24** & **Figure 26**)

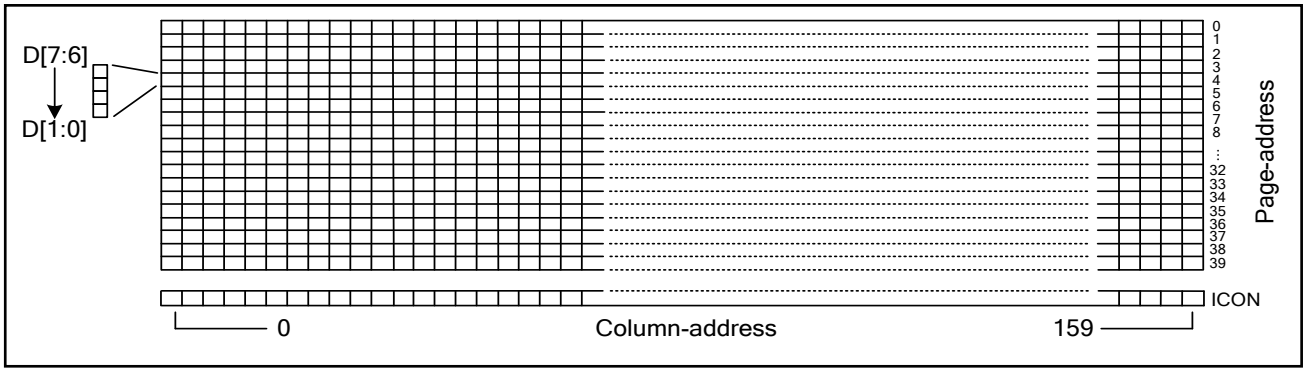


Figure 23 RAM Format and Addressing, if DO=0 (4-Level Gray Scale Mode)

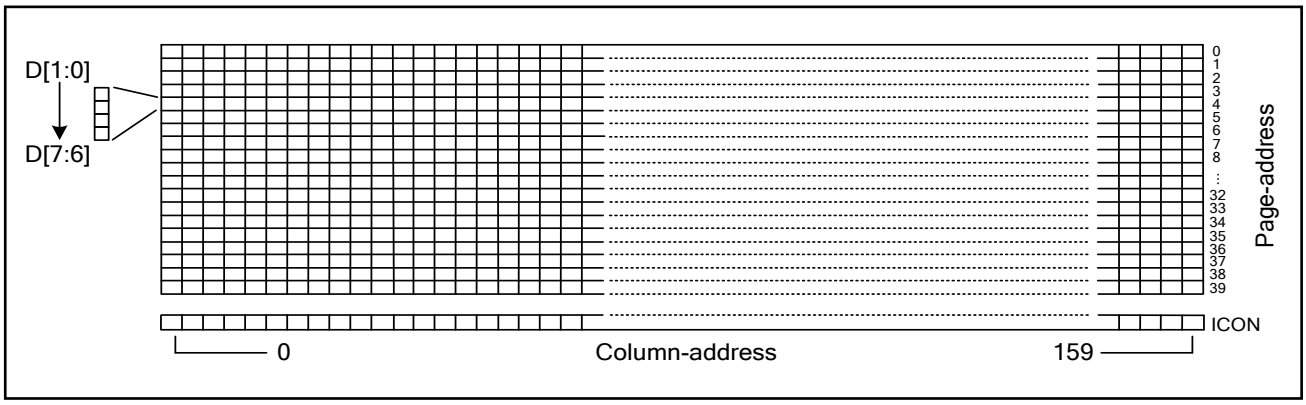


Figure 24 RAM Format and Addressing, if DO=1 (4-Level Gray Scale Mode)

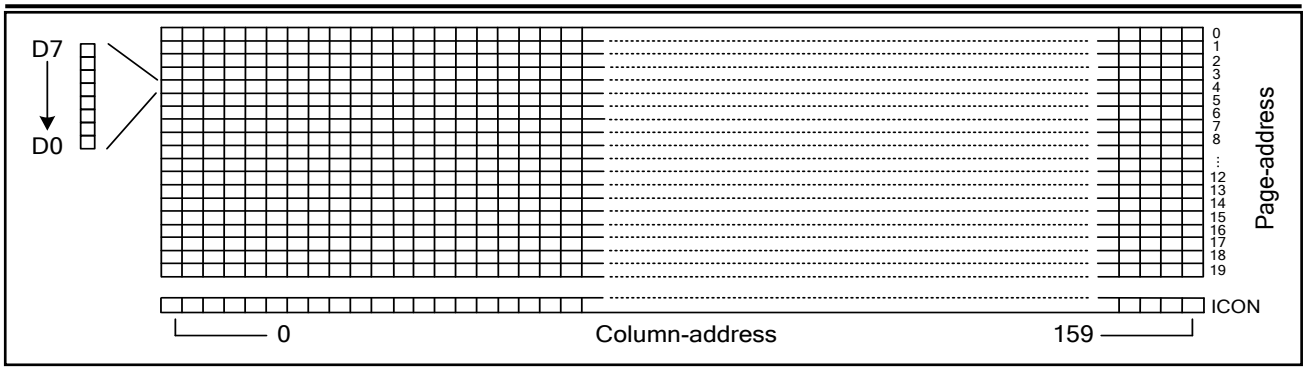


Figure 25 RAM Format and Addressing, if DO=0 (Monochrome Mode)

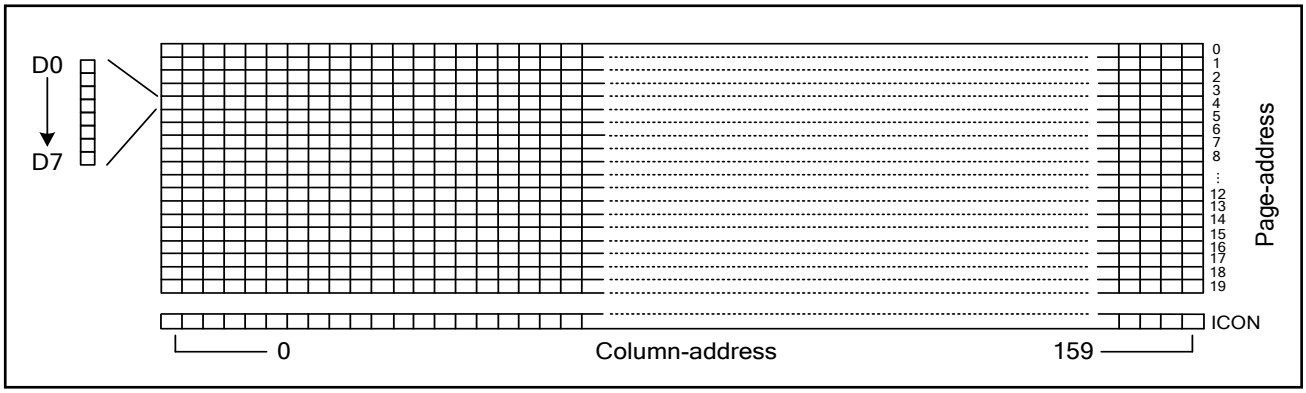


Figure 26 RAM Format and Addressing, if DO=1 (Monochrome Mode)

7.3.6 DDRAM Map to LCD Driver Output

The internal relation between DDRAM and LCD driver circuit (SEG/COM output path) with different MX or COMSCN setting is illustrated below.

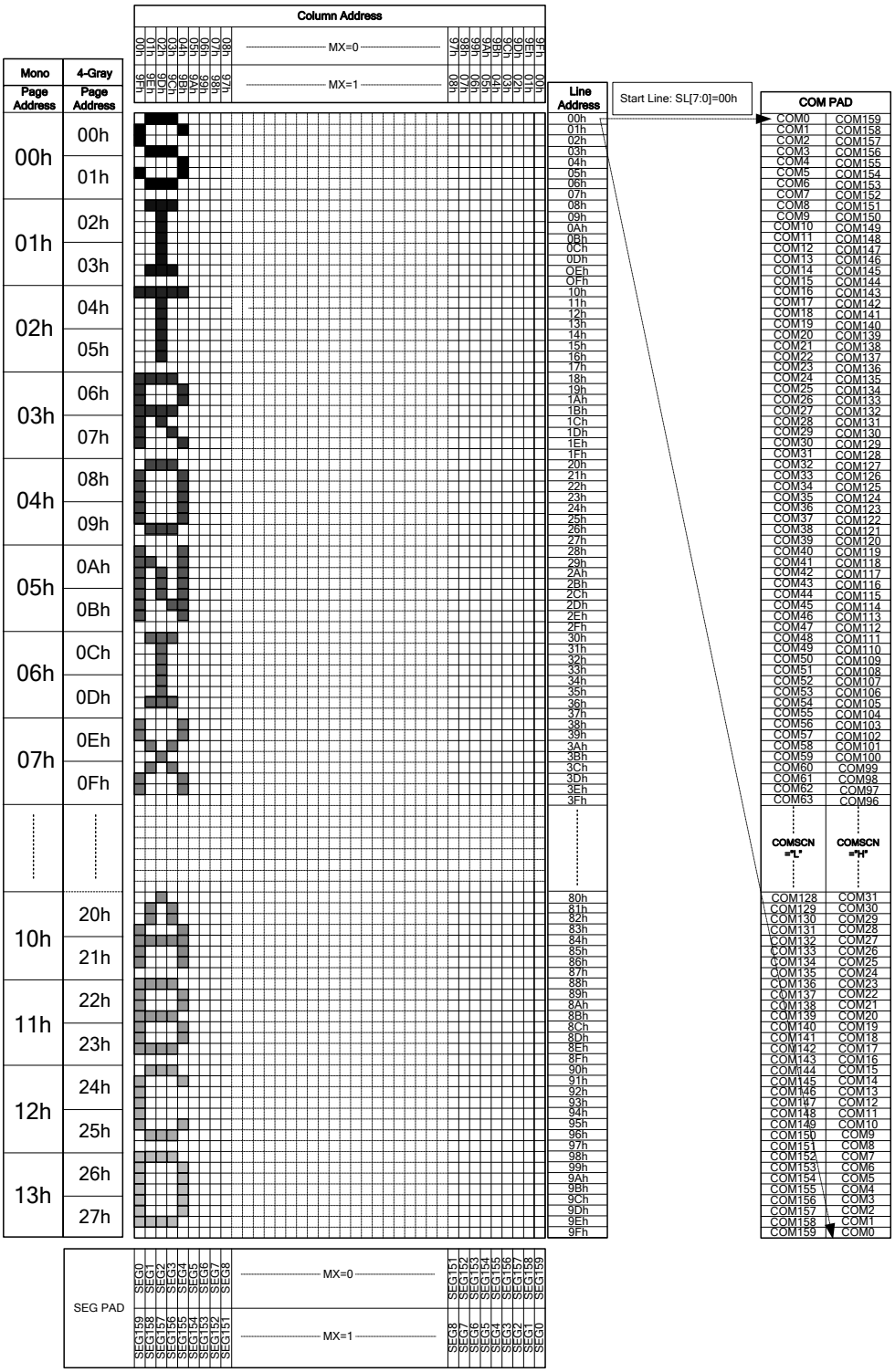


Figure 27 DDRAM Display Direction

7.3.7 Set ICON

The internal relation between ICON DDRAM and LCD driver circuit (SEG/ICON output path) with different MX setting is illustrated below. Please ensure to write B/W data to ICON DDRAM in 4 gray scale mode.

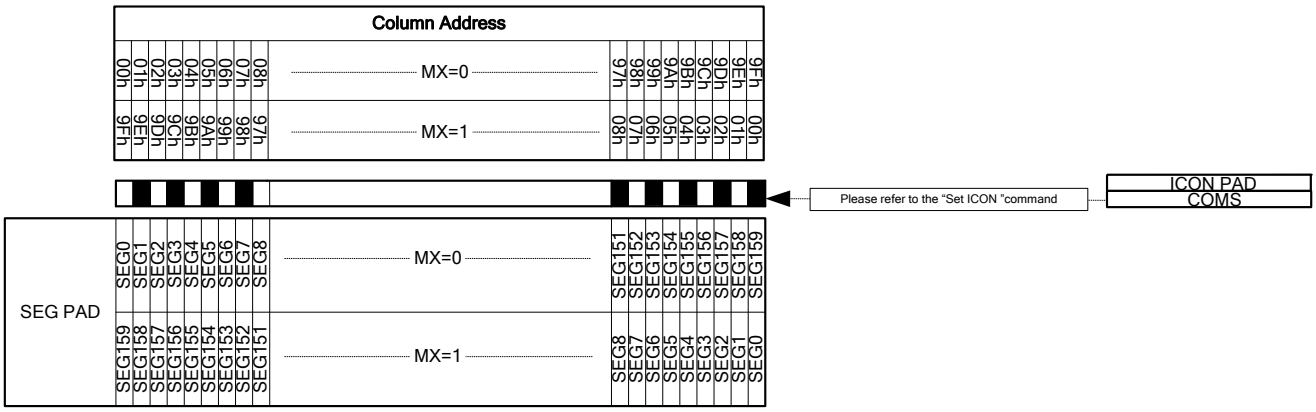


Figure 28 ICON DDRAM Display Direction

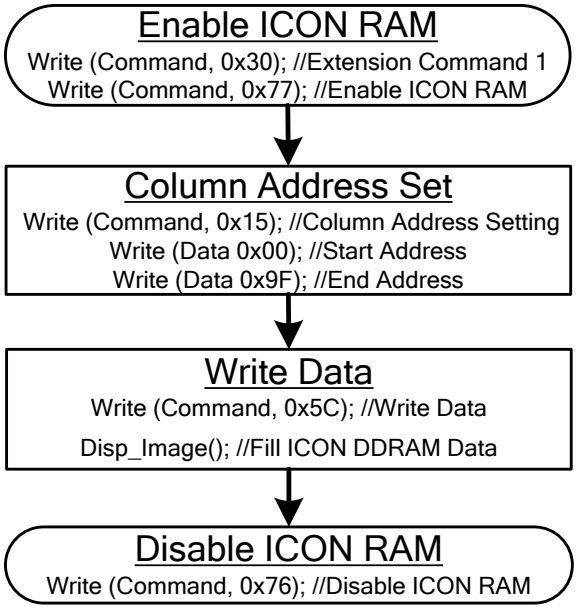


Figure 29 Command Sequence for Set ICON

7.3.8 Partial Display

This function is defining the visible display area as illustrated in Figure 30. The different partial display area setting will be changing frame rate or Vop to avoid abnormal display. This mode consumes less current than the whole screen display and is suitable for the equipment in the standby state. If the partial display region is out of the maximum display range, it will be no operation.

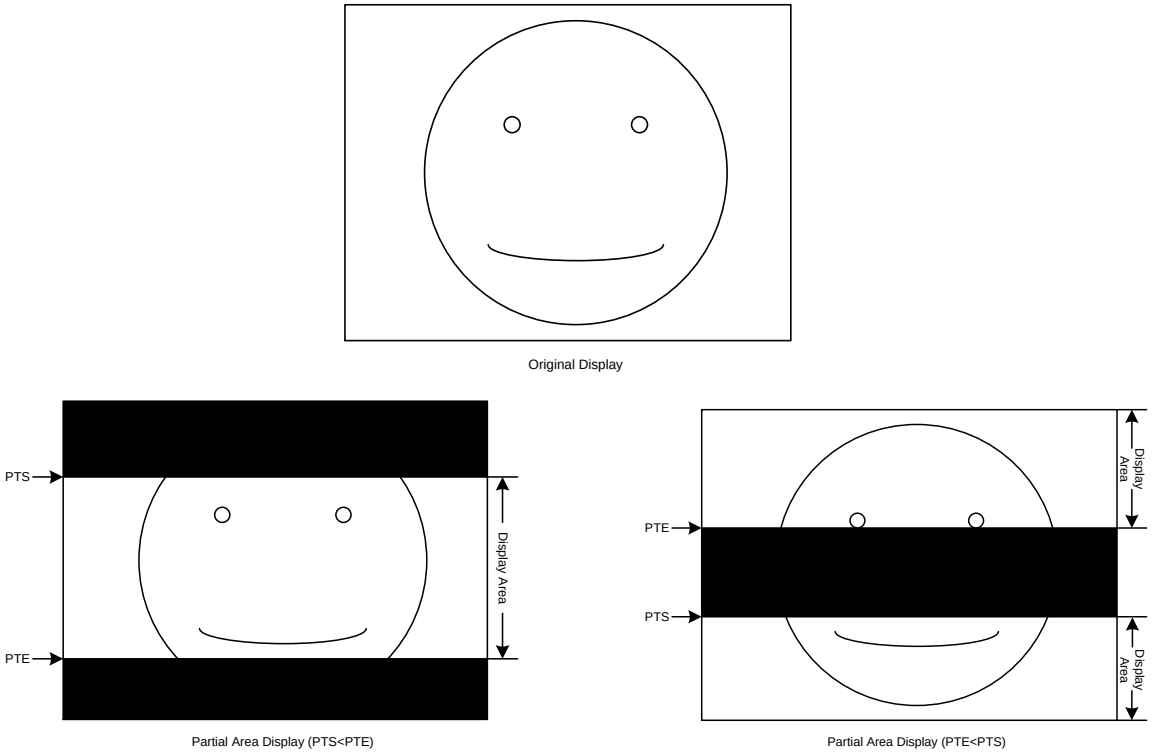


Figure 30 Partial Display Definition

7.3.9 Area Scroll Display

The user may scroll the display screen partially in any one of the following four scroll pattern via partial mode

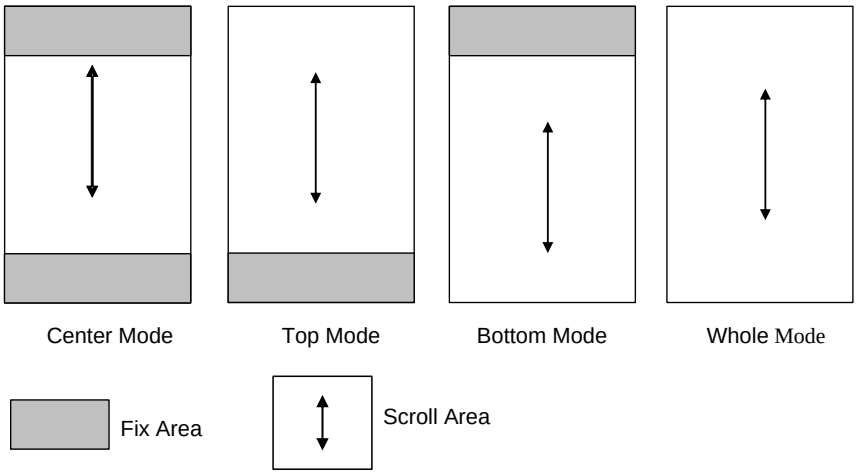


Figure 31 Scroll Definition

7.3.10 Partial Display Application with COMSCN

The relation between display output and different COMSCN setting is shown below. **The partial duty layout must be pulled from COM0 to COMx(partial duty)**. The following illustration for partial duty equal to 64 duties and the related setting on COMSCN please refer to Section 6.2 Driver Output Pins.

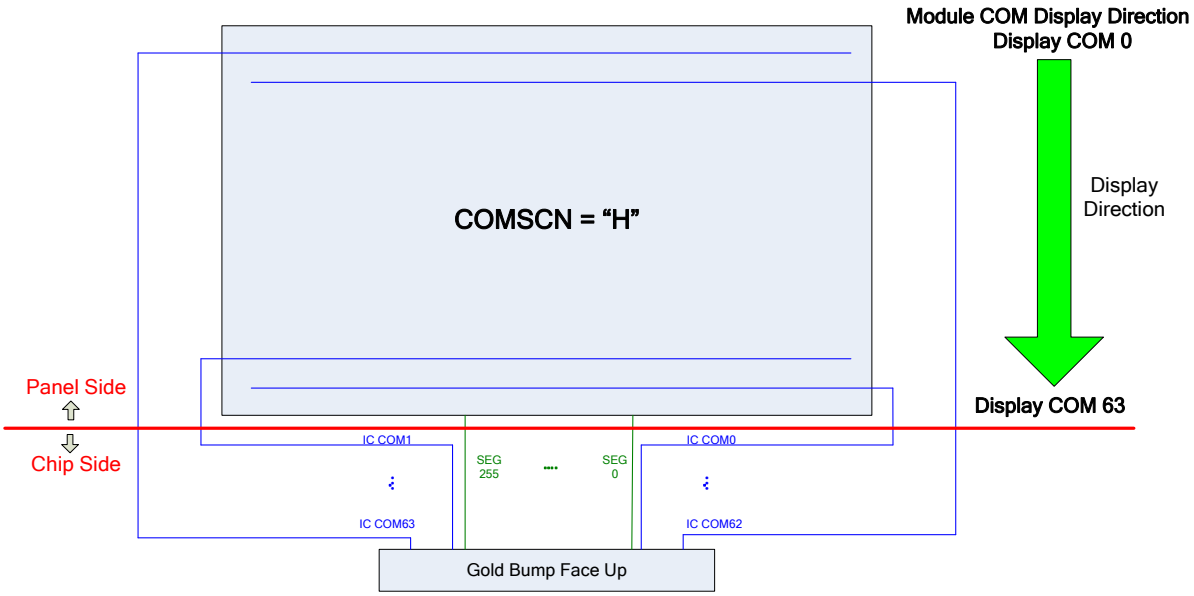


Figure 32 64 duty and COMSCN = H

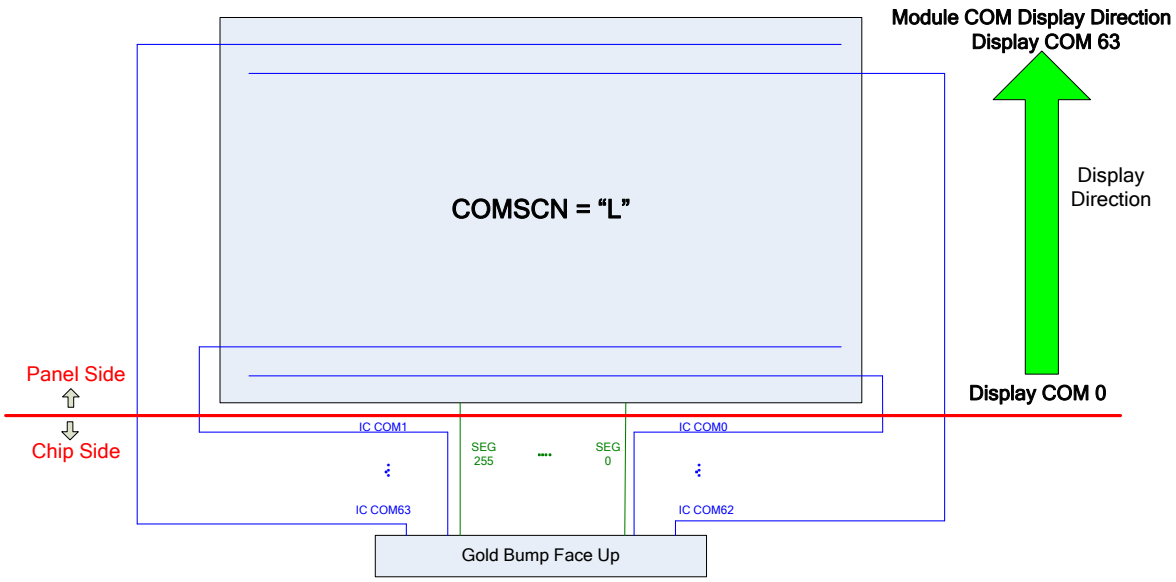


Figure 33 64 duty and COMSCN = L

7.4 Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. It consumes low power with the fewest external component. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. Before power ST75160 is OFF, a Power OFF procedure is needed. Please refer to the OPERATION FLOW selection.

7.4.1 External Component of Power Circuit

The recommended external power components need only three capacitors. The detailed values of these three capacitors are determined by panel size and loading.

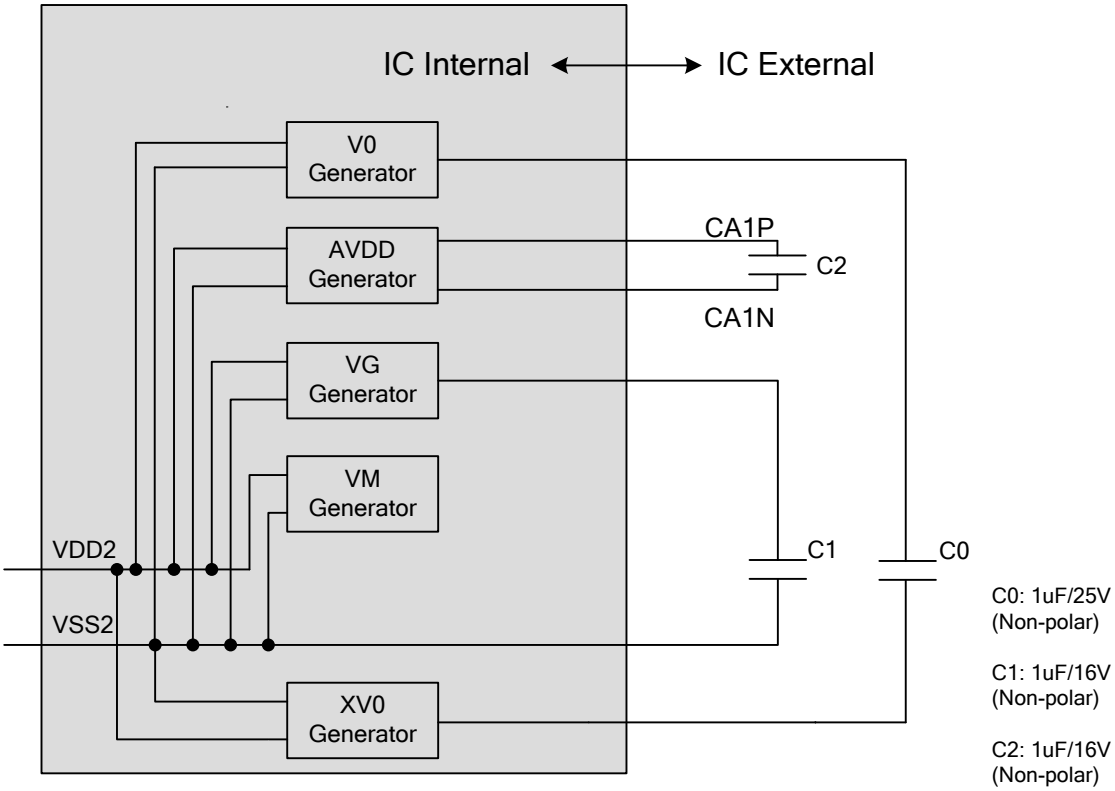


Figure 34 Internal Power Supply Circuit

Note:

1. C0: 1uF/25V~2.2uF/25V (Default 1uF/25V)
2. C1: 1uF/16V~2.2uF/16V (Default 1uF/16V)
3. C2: 1uF/16V~2.2uF/16V (Default 1uF/16V)

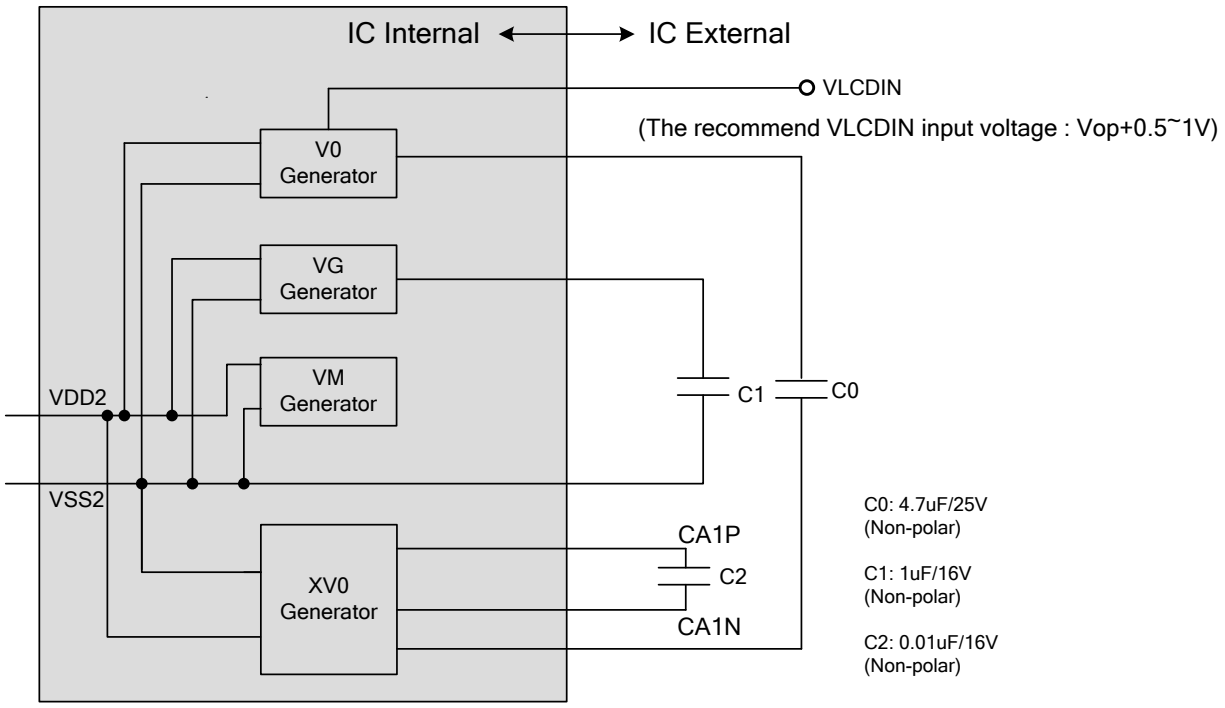


Figure 35 External Power Supply Circuit

Note:

1. C0: 2.2uF/25V~4.7uF/25V (Default 4.7uF/25V)
2. C1: 1uF/16V~2.2uF/16V (Default 1uF/16V)
3. C2: 0.01uF/16V~0.022uF/16V (Default 0.01uF/16V)

7.4.2 Voltage Regulator Circuits

The set Vop function is to program the optimum LCD supply voltage V0.

- **SET Vop (Temperature = 24°C)**

The V0 value is programmed via the Vop[8:0] register.

V0 = a + Vop[8:0] x b

Ex: Vop[5:0]=000001, Vop[8:6]=100

→ Vop[8:0]=100000001

→ 3.6+257x0.04=13.88

where **a** is a fixed constant value 3.6, **b** is a fixed constant value 0.04, Vop[8:0] is the programmed **V0** value with programming range from 85 to 360 (55_{HEX} to 168_{HEX}), and Vop[5:0] is the set contrast value which can be set via the interface and is in two's complement format.(See command Vop Control)

The Vop[8:0] value must be in the V0 programming range as given in **Figure 36**

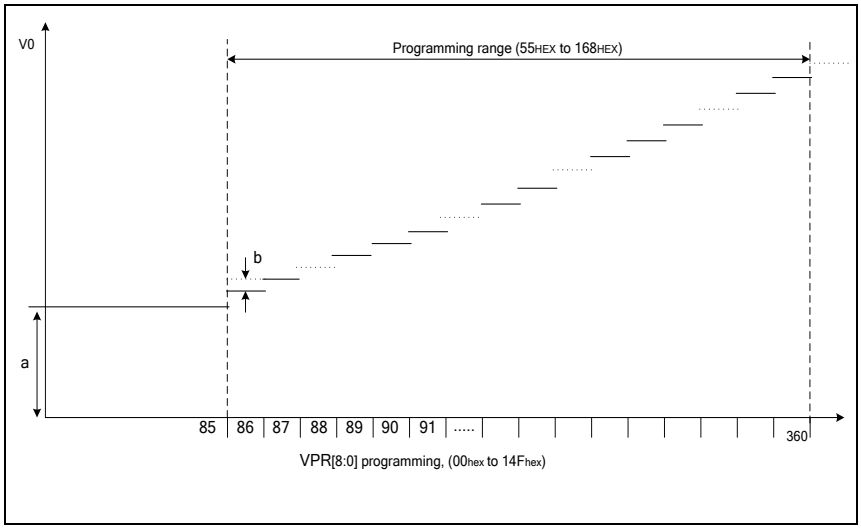


Figure 36 V0 Programming Range

Although the programming range for the internally generated V0 allows values above the maximum allowed V0, the customer has to ensure setting the Vop[8:0] register and selecting the temperature compensation under all condition and including all tolerances that the maximum allowed V0 (18V) will never be exceeded.

- **V0 Restriction**

Because VG should larger than 1.8V, V0 value should be higher than 1.8 x Bias / 2 (V) and lower than 18V. V0 value outside the available range is undefined. User has to ensure while selecting the temperature compensation that under all conditions and including all tolerances that V0 voltage remains in the range.

7.5 Temperature Gradient Selection Circuit

7.5.1 SET V0 with temperature compensation (Temperature ≠ 24°C)

There are 16-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C. Please see **Figure 37** as below.

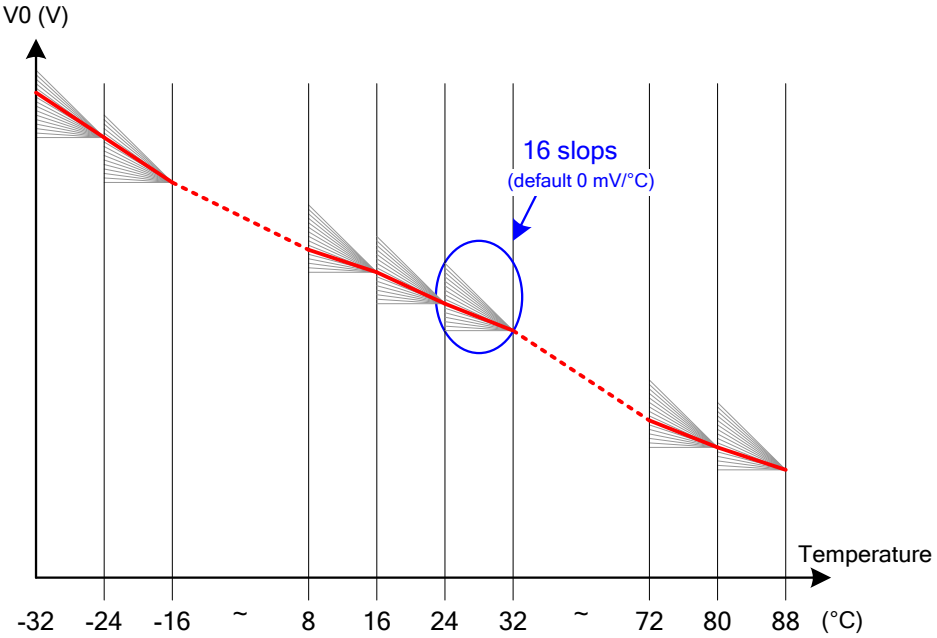


Figure 37 Temperature Compensation Coefficient Selection

In instruction Temperature Gradient Compensation each parameter MTx, where x=0, 1, 2,…, E, F has a setting value between 0 and 15. MTx=0 results in Mx=0V increment on V0, MTx=1 results in Mx=5mV increment,…, MTx=15 results in Mx=15x5mV=75mV increment. Note that each MTx individually corresponds to a temperature interval; the Mx means temperature gradient slope coefficient. The relations between Mx and V0 quantity due to temperature V0(T) are described in the equation shown in **Table 4**.

Temperature Range	Equation V0(T) at temperature=T°C
-32°C ≦ T < -24°C	V0(T) = V0(T24) + (-24 - T) x M1 + (M2 + M3 + M4 + M5 + M6 + M7) x 8
-24°C ≦ T < -16°C	V0(T) = V0(T24) + (-16 - T) x M2 + (M3 + M4 + M5 + M6 + M7) x 8
-16°C ≦ T < -8°C	V0(T) = V0(T24) + (-8 - T) x M3 + (M4 + M5 + M6 + M7) x 8
-8°C ≦ T < 0°C	V0(T) = V0(T24) + (0 - T) x M4 + (M5 + M6 + M7) x 8
0°C ≦ T < 8°C	V0(T) = V0(T24) + (8 - T) x M5 + (M6 + M7) x 8
8°C ≦ T < 16°C	V0(T) = V0(T24) + (16 - T) x M6 + M7 x 8
16°C ≦ T < 24°C	V0(T) = V0(T24) + (24 - T) x M7
24°C ≦ T < 32°C	V0(T) = V0(T24) - (T - 24) x M8
32°C ≦ T < 40°C	V0(T) = V0(T24) - (T - 32) x M9 – M8 x 8
40°C ≦ T < 48°C	V0(T) = V0(T24) - (T - 40) x M10 – (M9 + M8) x 8
48°C ≦ T < 56°C	V0(T) = V0(T24) - (T - 48) x M11 – (M10 + M9 + M8) x 8
56°C ≦ T < 64°C	V0(T) = V0(T24) - (T - 56) x M12 – (M11 + M10 + M9 + M8) x 8
64°C ≦ T < 72°C	V0(T) = V0(T24) - (T - 64) x M13 – (M12 + M11 + M10 + M9 + M8) x 8
72°C ≦ T < 80°C	V0(T) = V0(T24) - (T - 72) x M14 – (M13 + M12 + M11 + M10 + M9 + M8) x 8
80°C ≦ T < 88°C	V0(T) = V0(T24) - (T - 80) x M15 – (M14 + M13 + M12 + M11 + M10 + M9 + M8) x 8

Table 4 Equation V0(T) at Different Temperature

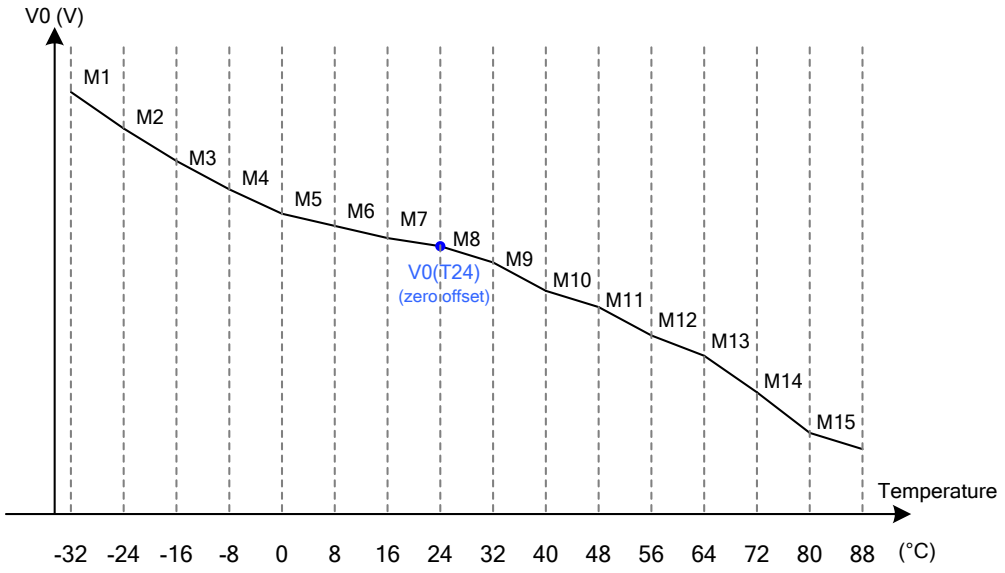


Figure 38 Temperature Gradient Compensation

Note:

- Please make sure to avoid any kind of heating source near ST75160 such as back light, to prevent Vop is not anticipative because of temperature compensation circuit is working.

7.6 Frequency Temperature Gradient Compensation Coefficient

7.6.1 Register Loading Detection

ST75160 will auto-switch frame rate in different temperature such as Figure 39. TA, TB and TC are frame rate switching temperature which can be defined by customer with instruction Temperature Range. FRA, FRB, FRC and FRD are switched frame rate which also can be defined by customer with instruction Frame Rate. The frame rate range is from 5Hz to153Hz.

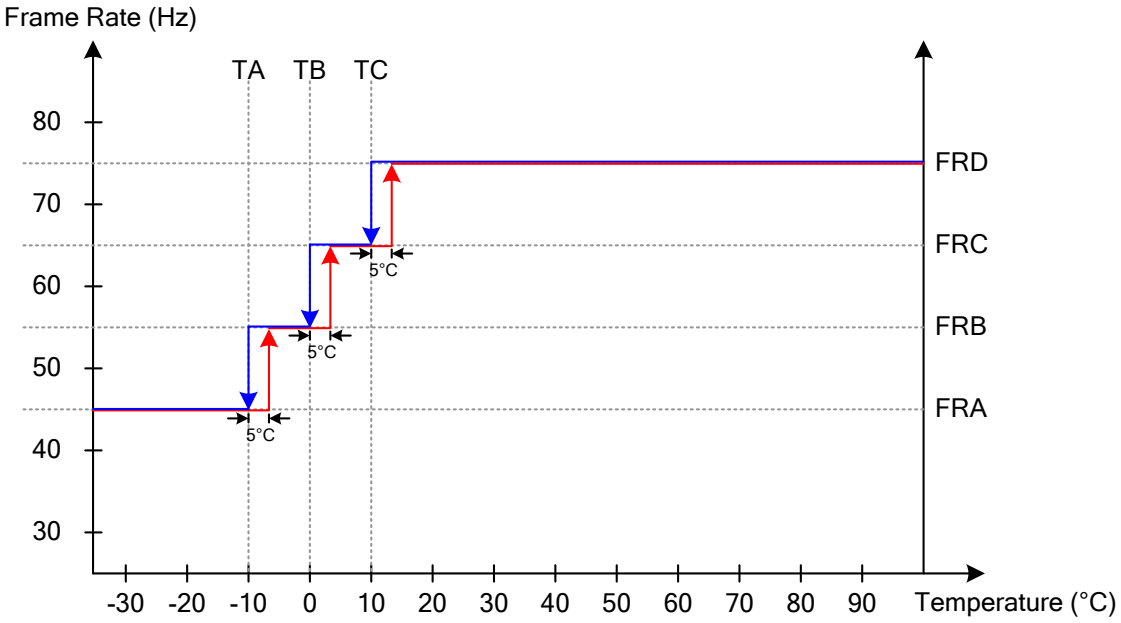


Figure 39 Frame Rate

8 RESET CIRCUIT

Setting RSTB pin to “L” can initialize internal function. While RSTB is “L”, no instruction can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating.

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON.

The default values of registers are listed below:

Procedure		Hardware Reset
DDRAM Content		No Change
Extension Command		EXT[1:0]=[0, 0]
Display ON/OFF		Display OFF
Normal/Inverse Display		Normal
ALL Pixel ON/OFF		ALL Pixel OFF
Setting CL Dividing Ratio		Not Divide
Duty Setting		DT[7:0]=00h
N-Line Inversion		Frame Inversion
N-Line Inversion Mode		FI=0h
Power Save Mode		Sleep in Mode
Page Address	Start Address	00h
	End Address	00h
Column Address	Start Address	00h
	End Address	00h
Address Scan Direction		Column Direction
Normal/Reverse Direction of the Line Address		Normal
Normal/Reverse Direction of the Column Address		Normal
Partial In	Start Address	00h
	End Address	00h
Read Modify Write		Disable
Scroll Area	Top Line Address	00h
	Bottom Line Address	9Fh
	Number of Specified Lines	9Fh
Scroll Area Mode		Whole Screen Scroll
Start Line		00h
OSC ON/OFF		OSC OFF
Power Control		VB=0, VR=0, VF=0

Procedure	Hardware Reset
Set Vop	Vop[8:0]=000h
Vop Control	VOL=0
Read Register Mode	REG=0
Data Format Select	DO=0; LSB on Bottom
Display Mode	Mono
Set ICON	Disable
Set Gray Level	GL[4:0]=0Ch, GD[4:0]=12h
Booster Efficiency Set	BE[1:0]=01h
BIAS	1/12
Booster Level	X10
Driving Select	Internal
Auto Read Control	XARD=0
OTP WR/RD Control	WR/RD=0
OTP Selection Control	Ctrl=0
Frame Rate	FRA[4:0]=00h, FRB[4:0]=03h, FRC[4:0]=0Dh, FRD[4:0]=1Bh
Temperature Range	TA[6:0]=0Fh, TB[6:0]=28h, TC[6:0]=5Ah
Temperature Gradient Compensation	MT1[3:0]=07h, MT2[3:0]=02h, MT3[3:0]=02h, MT4[3:0]=01h, MT5[3:0]=01h, MT6[3:0]=02h, MT7[3:0]=00h, MT8[3:0]=00h, MT9[3:0]=00h, MTA[3:0]=02h, MTB[3:0]=03h, MTC[3:0]=02h, MTD[3:0]=08h, MTE[3:0]=06h, MTF[3:0]=0Bh
Enable OTP	Disable

Table 5 The Default Values of Registers

9 COMMAND

9.1 INSTRUCTION TABLE

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
1.Extension Command	0	0	0	0	1	1	EXT1	0	0	EXT0	Set extension instruction
Ext[1:0]=0,0 (Extension Command 1)											
2.Display ON/OFF	0	0	1	0	1	0	1	1	1	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
3.Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display INV=0: Normal display INV=1: Inverse display
4.All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode AP=0: All pixel off mode AP=1: All pixel on mode
5.Display Control	0	0	1	1	0	0	1	0	1	0	Set display control CLD :Set CL dividing ratio DT[7:0] : Set the number of duty LF[4:0] : Set N-line inversion counter FI : Set the inversion type of frame at the end of common scan cycle
	1	0	0	0	0	0	0	CLD	0	0	
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
	1	0	0	0	LF4	FI	LF3	LF2	LF1	LF0	
6.Power Save	0	0	1	0	0	1	0	1	0	SLP	Set power save mode SLP=0: Sleep out mode SLP=1: Sleep in mode
7.Set Page Address	0	0	0	1	1	1	0	1	0	1	Set page address Starting page address: 00h≦YS≦27h Ending page address: YS≦YE≦27h
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
8.Set Column Address	0	0	0	0	0	1	0	1	0	1	Set column address Starting column address: 00h≦XS≦9Fh Ending column address: XS≦XE≦9Fh
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
9.Data Scan Direction	0	0	1	0	1	1	1	1	0	0	Set normal/ inverse display of address and address scan direction
	1	0	0	0	0	0	0	MV	MX	0	
10.Write Data	0	0	0	1	0	1	1	1	0	0	Write data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
11.Read Data	0	0	0	1	0	1	1	1	0	1	Read data from DDRAM (Only for parallel interface and I^2C)
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
12.Partial In	0	0	1	0	1	0	1	0	0	0	Set partial area Starting partial display address: 00h≦PTS≦9Fh Ending partial display address: 00h≦PTE≦9Fh
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
	1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
13.Partial Out	0	0	1	0	1	0	1	0	0	1	Exit the partial mode
14.Read/Modify/Write In	0	0	1	1	1	0	0	0	0	0	Enable read modify write
15.Read/Modify/Write Out	0	0	1	1	1	0	1	1	1	0	Disable read modify write
16.Scroll Area	0	0	1	0	1	0	1	0	1	0	Set scroll area TL[7:0] : Set top line address BL[7:0] : Set bottom line address NSL[7:0] : Number of specified line SCM[1:0] : Area scroll mode
	1	0	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	
	1	0	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	
	1	0	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	
	1	0	0	0	0	0	0	0	SCM1	SCM0	
17.Set Start Line	0	0	1	0	1	0	1	0	1	1	Set scroll start address 00h≦SL≦9Fh
	1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	
18.OSC ON	0	0	1	1	0	1	0	0	0	1	Turn on the internal oscillator
19.OSC OFF	0	0	1	1	0	1	0	0	1	0	Turn off the internal oscillator
20.Power Control	0	0	0	0	1	0	0	0	0	0	Power circuit operation VB=0: OFF, VB=1: ON VF=0: OFF, VF=1: ON VR=0: OFF, VR=1: ON
	1	0	0	0	0	0	VB	0	VF	VR	
21.Set Vop	0	0	1	0	0	0	0	0	0	1	Set Vop
	1	0	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	1	0	0	0	0	0	0	Vop8	Vop7	Vop6	
22.Vop Control	0	0	1	1	0	1	0	1	1	VOL	Control Vop VOL=0: Vop increase one step VOL=1: Vop decrease one step
23.Read Register Mode	0	0	0	1	1	1	1	1	0	REG	Set read register mode REG=0: read the register value of Vop[5:0] REG=1: read the register value of Vop[8:6]
24.Nop	0	0	0	0	1	0	0	1	0	1	No operation
25.Read Status (Parallel and I^2C)	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read status byte (Parallel and I^2C)
26.Read Status (4-Line and 3-Line SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte (4-Line and 3-Line SPI)
	0	1	D7	D6	D5	D4	D3	D2	D1	D0	
27.Data Format Select	0	0	0	0	0	0	1	DO	0	0	DO=0; LSB on bottom (Default) DO=1; LSB on top
28. Display Mode	0	0	1	1	1	1	0	0	0	0	Set display mode DM=0 :Mono(Default) DM=1 :4Gray Scale Mode
	1	0	0	0	0	1	0	0	0	DM	

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
29.Set ICON	0	0	0	1	1	1	0	1	1	ICON	Enable/Disable ICON RAM ICON=1 ; Enable ICON RAM ICON=0 ; Disable ICON RAM
Ext[1:0]=0,1 (Extension Command 2)											
30. Set Gray Level	0	0	0	0	1	0	0	0	0	0	Set gray scale level GL[4:0]: Set Light Gray Level GD[4:0]: Set Dark Gray Level
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	
31.Analog Circuit Set	0	0	0	0	1	1	0	0	1	0	Set analog circuit BE[1:0]: Booster efficiency set BS[2:0]: Set bias ratio
	1	0	0	0	0	0	0	0	0	0	
	1	0	0	0	0	0	0	0	BE1	BE0	
	1	0	0	0	0	0	0	BS2	BS1	BS0	
32.Booster Level	0	0	0	1	0	1	0	0	0	1	Set booster level BST=0 : X8 BST=1 : X10
	1	0	1	1	1	1	1	0	1	BST	
33. Driving Select	0	0	0	1	0	0	0	0	0	DS	Power type DS=0: Internal (Default) DS=1 :External
34.Auto Read Control	0	0	1	1	0	1	0	1	1	1	Set auto-read instruction XARD=0: Enable auto read XARD=1: Disable auto read
	1	0	1	0	0	XARD	1	1	1	1	
35.OTP WR/RD Control	0	0	1	1	1	0	0	0	0	0	OTP WR/RD control WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
	1	0	0	0	WR/ RD	0	0	0	0	0	
36.OTP Control Out	0	0	1	1	1	0	0	0	0	1	OTP control out
37.OTP Write	0	0	1	1	1	0	0	0	1	0	OTP write
38.OTP Read	0	0	1	1	1	0	0	0	1	1	OTP read

INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
39.OTP Selection Control	0	0	1	1	1	0	0	1	0	0	OTP selection control Ctrl=1: Disable OTP Selection Ctrl=0: Enable OTP Selection
	1	0	1	Ctrl	0	1	1	0	0	1	
40.OTP Programming Setting	0	0	1	1	1	0	0	1	0	1	OTP programming setting
	1	0	0	0	0	0	1	1	1	1	
41.Frame Rate	0	0	1	1	1	1	0	0	0	0	Frame rate setting in different temperature range
	1	0	0	0	0	FRA4	FRA3	FRA2	FRA1	FRA0	
	1	0	0	0	0	FRB4	FRB3	FRB2	FRB1	FRB0	
	1	0	0	0	0	FRC4	FRC3	FRC2	FRC1	FRC0	
	1	0	0	0	0	FRD4	FRD3	FRD2	FRD1	FRD0	
42.Temperature Range	0	0	1	1	1	1	0	0	1	0	Temperature range setting
	1	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
	1	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
	1	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	
43.Temperature Gradient Compensation	0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
	1	0	MT13	MT12	MT11	MT10	1	1	1	1	
	1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
	1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
	1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
	1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
	1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
	1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
	1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	
Ext[1:0]=1,1(Extension Command 4)											
44.Enable OTP	0	0	1	1	0	1	0	1	1	0	Enable OTP EOTP =0 ; Disable (Default) EOTP =1 ; Enable
	1	0	0	0	0	EOTP	0	0	0	0	

9.2 INSTRUCTION DESCRIPTION

9.2.1 Extension Command

This instruction sets the extension instruction mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	1	EXT1	0	0	EXT0

Flag	Description
EXT[1:0]	Extension command mode. EXT [1:0]=[0,0]: Extension command 1. EXT [1:0]=[0,1]: Extension command 2. EXT [1:0]=[1,0]: Extension command 3. EXT [1:0]=[1,1]: Extension command 4.

“Extension Command 1”

9.2.2 Display ON/OFF

This instruction turns the display ON or OFF. When ST75160 enters display off, the display output is blank regardless of the content of DDRAM. When ST75160 enters display on (exit display off), the display output is according to content of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	1	1	DSP	DSP=0: Display off mode DSP=1: Display on mode

9.2.3 Inverse Display

This instruction would inverse the scanned data without recover the content of DDRAM. As the result, the ON and OFF status of all pixels are interchanged.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	0	1	1	INV	INV=0: Normal display INV=1: Inverse display

9.2.4 All Pixel ON/OFF

When ST75160 enters all pixels on or off mode, all display pixels are turned on or off regardless of the content of DDRAM. The content of DDRAM is not changed by setting All Pixel ON/OFF. After execute the instruction of Partial Mode, the display mode will exit all pixel on/off mode then enter normal mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	1	AP	AP=0: All pixel off mode AP=1: All pixel on mode

Note: This function is only used in mono mode, does not support grayscale mode.

9.2.5 Display Control

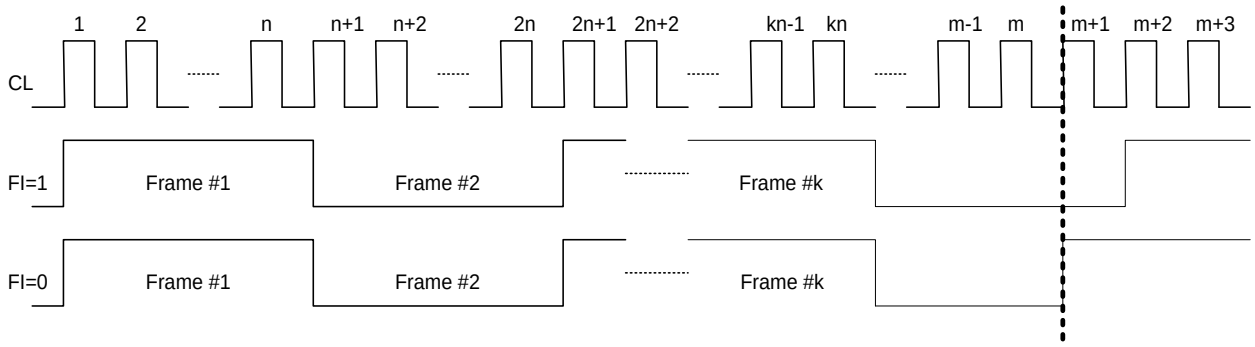
A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	0	1	0	1	0	CLD: CL Dividing ratio
1	0	0	0	0	0	0	CLD	0	0	DT: Duty of the module
1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	LF: Line cycles in a frame
1	0	0	0	LF4	FI	LF3	LF2	LF1	LF0	FI: Inversion type of frame

CLD: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.
CLD=0: not divide, CLD=1: 2 divisions.

DT [7:0] is used to set duty of the module.

DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	Duty
0	0	0	1	1	1	1	1	32
0	0	1	1	1	1	1	1	64
0	1	0	0	1	1	1	1	80
0	1	1	1	1	1	1	1	128
1	0	0	1	1	1	1	1	160

LF[4:0] specifies number of line cycles (range from 2 to 32) in a frame.
Number of line cycles-1 = LF4 x 2^4 + LF3 x 2^3 + LF2 x 2^2 + LF1 x 2^1 + LF0 x 2^0
For example, 11 line cycles in a frame → 11-1=10 → (LF4, LF3, LF2, LF1, LF0) = (0, 1, 0, 1, 0)
In the default, frame inversion (LF4, LF3, LF2, LF1, LF0) = (0, 0, 0, 0, 0) is selected.
FI decides the inversion type of frame at the end of common scan cycle while the number of duty is not divisible by the number of line cycles per frame. For example, in the application of 1/m duty and n line cycles in a frame set, the difference of the choice in FI is shown as the following figure.
m = n x k + r, where m, n, k, and r are all whole numbers, and r is the remainder of m divided by n (r < n).



9.2.6 Power Save

When ST75160 enters the sleep in mode, the mode causes the LCD module entering the minimum power consumption mode. All of operations (e.g. the DC/DC converter, internal oscillator and panel scanning) are stopped. When ST75160 enters sleep out mode (exit sleep in mode), the DC/DC converter and internal oscillator are started.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	1	0	1	0	SLP	SLP=0: Sleep out mode SLP=1: Sleep in mode

9.2.7 Set Page Address

This instruction is used to define area of DDRAM where MCU can access. The page address is automatically increased by one (+1) after column address counter is over XE[7:0]. The page address will return to starting page address YS[7:0] immediately when the page address increases one over the ending page address YE[7:0]. The YS[7:0] setting must be equal to or less than YE[7:0]. When YS[7:0] or YE[7:0] is great than 27h, out of DDRAM range will be ignored.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	0	1	0	1	YS: Starting page address YE: Ending page address
1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	

Note: The range of address is 00h~27h.

9.2.8 Set Column Address

This instruction is used to define area of DDRAM where MCU can access. The column address is automatically increased by one (+1) after each DDRAM access. After the ending column address XE[7:0], column address returns to starting column address XS[7:0]. The XS[7:0] setting that must be equal to or less than XE[7:0]. When XS[7:0] or XE[7:0] is great than 9Fh, out of DDRAM range will be ignored.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	1	0	1	0	1	XS: Starting column address XE: Ending column address
1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	

Note: The range of address is 00h~9Fh.

9.2.9 Data Scan Direction

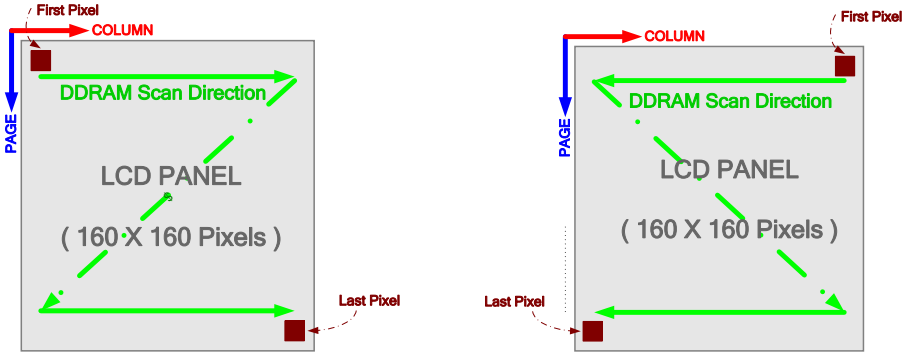
This instruction defines the write/read scanning direction of DDRAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	1	1	1	0	0	Specify COM scan direction
1	0	0	0	0	0	0	MV	MX	0	

MV: Address-scan direction. MV =0: In the column direction, MV =1: In the page direction

MX: Normal/reverse direction of the column address. MX =0: Normal, MX =1: Reverse

"MV=0"



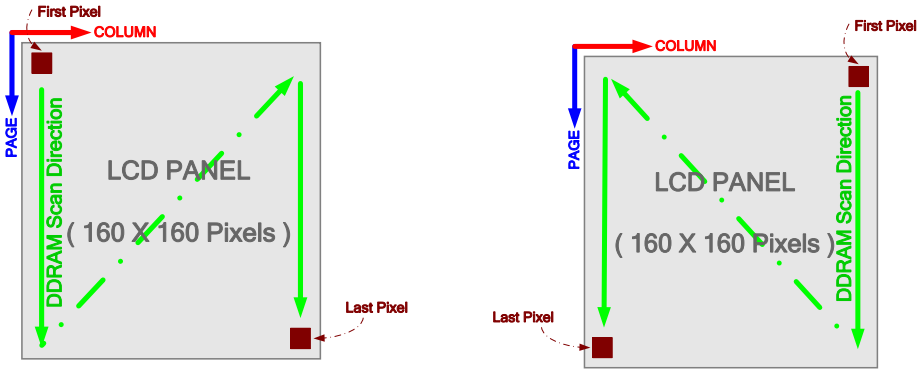
(a) COMMAND 0xBCh, DATA 0x00h **(b) COMMAND 0xBCh, DATA 0x02h**

Figure 40 Different RAM accessing setup under COMMAND 0xBCh

(a) DATA 0x00h (MV=0, MX=0)

(b) DATA 0x02h (MV=0, MX=1)

"MV=1"



(a) COMMAND 0xBCh, DATA 0x04h **(b) COMMAND 0xBCh, DATA 0x06h**

Figure 41 Different RAM accessing setup under COMMAND 0xBCh

(a) DATA 0x04h (MV=1, MX=0)

(b) DATA 0x06h (MV=1, MX=1)

9.2.10 Write Data

This instruction is used to transfer data from MCU to DDRAM without changing status of ST75160. The column address and page address will be reset to starting column address (XS) and starting page address (YS) when this instruction is accepted. The pre-instruction is defined to enter write DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. Write Display Data would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	0	0	Write display data to DDRAM
1	0	D7	D6	D5	D4	D3	D2	D1	D0	

9.2.11 Read Data

The instruction is used to transfer data from DDRAM to MCU without changing status of ST75160. The column address and page address will be reset to staring column address (XS) and starting page address (YS) when this instruction is accepted. The pre-instruction is defined to enter read DDRAM mode. The following continuously data means content of DDRAM without pre-instruction. Read Display Data would be stopped when any other instruction is accepted.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	0	1	Read data from DDRAM (Only for parallel interface and I^2C)
1	1	D7	D6	D5	D4	D3	D2	D1	D0	

9.2.12 Partial In

This instruction is to specify the partial display area. It will turn on partial display of the screen (dividing screen by lines) to save power.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	0	PTS: Start line address PTE: End line address
1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	
1	0	PTE7	PTE6	PTE5	PTE4	PTE3	PTE2	PTE1	PTE0	

Only the address of the display line can be specified for the partial display. Do not specify an address not to be displayed when scrolled

9.2.13 Partial Out

This instruction is used to exit the PARTIAL DISPLAY MODE.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	0	1	Exit the partial display mode

9.2.14 Read /Modify/Write In

This command is used paired with the “Read/Modify/Write Out” command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	Enable read/modify/write

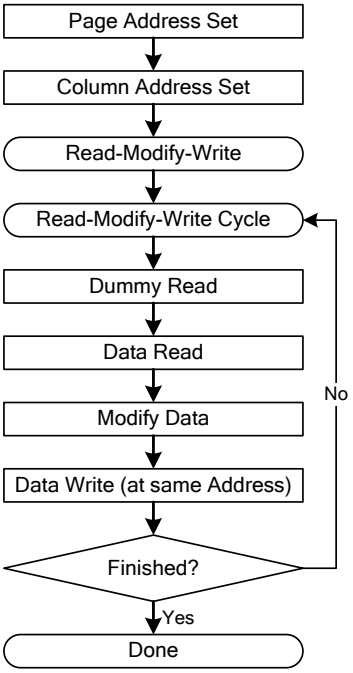


Figure 42 Command Sequence for Read/Modify/Write

9.2.15 Read /Modify/Write Out

When the Read/Modify/Write Out command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	1	1	1	0	Disable read/modify/write

9.2.16 Scroll Area

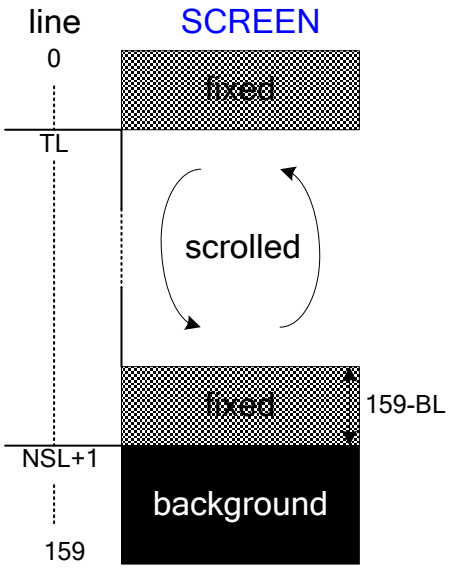
This command specifies the scrolling type of area, fixed area and scrolled area.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	0	TL: Top line address
1	0	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	BL: Bottom line address
1	0	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0	NSL: Number of specified
1	0	NSL7	NSL6	NSL5	NSL4	NSL3	NSL2	NSL1	NSL0	lines
1	0	0	0	0	0	0	0	SCM1	SCM0	SCM: Area scroll mode

SCM[1:0]: It is used to specify the scrolling mode.

SCM1	SCM0	Scrolling Mode	Settings		
			Top line address (TL)	Bottom line address (BL)	Number of specified lines (NSL)
0	0	Center mode	Top(fixed area) height = Top address	Bottom(fixed area) height = 159-Bottom address	Bottom start address = Specified number
0	1	Top mode	0	Bottom(fixed area) height = 159-Bottom address	Bottom start address = Specified number
1	0	Bottom mode	Top(fixed area) height = Top address	159	159
1	1	Whole mode	0	159	159

DDRAM address of the top fixed area is set in the line address increasing direction starting with the 0th line. DDRAM address of the bottom fixed area is set in the line address decreasing direction starting with 159st line. The DDRAM addresses of other line fixed areas are assigned to the scrolled + background areas.



TL[7:0] is to specify the top line address of the scrolled + background areas. Specify the 0th line for the top screen scroll or whole screen scroll.

BL[7:0] specifies the bottom line address of the scroll + background areas. Specify the 159th line for the bottom or whole screen scroll. The relation that top line address < bottom line address must be maintained.

NSL[7:0] specifies a specific number of lines {Numbers of (Top fixed area +Scroll area) line-1}. In the case of the bottom scroll or whole screen scroll, the value is identical with BL[7:0].

The user can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start address set command.

9.2.17 Scroll Start Address Set

This command is to specify which line address of DDRAM to be the start line content shown on screen. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start line address.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	1	0	1	0	1	1	SL: Start line address
1	0	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	

Note : Don’t repeat “Scroll Area (AAH)” instruction when “Scroll Start Address” is executed.

9.2.18 OSC ON

This command is used to turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit CLS = HIGH

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	0	1	Turn on the internal OSC

9.2.19 OSC OFF

It turns off the internal oscillation circuit.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	0	1	0	Turn off the internal OSC

9.2.20 Power Control

This command is used to turn on or off the Booster circuit, voltage regulator circuit, and reference voltage.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	0	0	Power circuit control
1	0	0	0	0	0	VB	0	VF	VR	

Flag	Description
VB	VB=0: Internal booster is turned OFF VB=1: Internal booster is turned ON
VR	VR=0: Internal regulator is turned OFF VR=1: Internal regulator is turned ON
VF	VF=0: Internal follower is turned OFF VF=1: Internal follower is turned ON

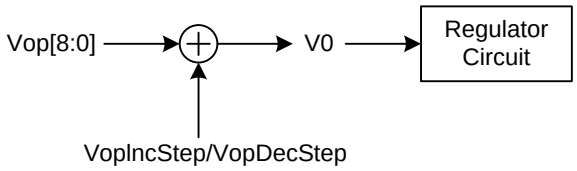
9.2.21 Set Vop

This instruction is used to adjust the optimum LCD supply voltage Vop.

The calculation of Vop is as shown blow: V0=3.6+(Vop[8:0]+VopIncStep-VopDecStep)x0.04

VopIncStep = Total Vop Increase Steps

VopDecStep = Total Vop Decrease Steps



A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	0	0	0	0	0	0	1	Set Vop
1	0	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
1	0	0	0	0	0	0	Vop8	Vop7	Vop6	

The suggestion of usable V0 voltage is shown below (assume VopIncStep/ VopDecStep=0):

Vop8	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	V0 (V)
0	0	1	0	1	0	1	0	1	7.00
0	0	1	0	1	0	1	1	0	7.04
0	0	1	0	1	0	1	1	1	7.08
:	:	:	:	:	:	:	:	:	:
1	0	1	1	0	0	1	1	0	17.92
1	0	1	1	0	0	1	1	1	17.96
1	0	1	1	0	1	0	0	0	18.00

9.2.22 Vop Control

This command is used to increase/decrease Vop step by one. Each step is 0.04V.

VOL=0; Vop increase one step

VOL=1; Vop decrease one step

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	VOL	Adjust Vop step by one

9.2.23 Read Register Mode

Execute the Read Register Mode and Read Status commands in succession to read the value of specified register.

REG=0 ; read the Vop[5:0] value of Vop set

REG=1 ; read the Vop[8:6] value of Vop set

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	1	1	0	REG	Set read register mode

Execute the “Read Status” command (parallel or serial) immediately after this command and execute the “NOP” command after the “Read Status” command.

9.2.24 NOP

This command does not affect the operation but has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and so on.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	1	0	1	No operation

9.2.25 Read Status (Parallel and I^2C)

The command is to read the internal condition of the IC. One status can be displayed depending on the setting status after reset or after NOP operation

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	D7	D6	D5	D4	D3	D2	D1	D0	Read status byte

Data Bus	Flag	Description
D7	Scroll Area Mode	Refer to SCM1
D6	Scroll Area Mode	Refer to SCM0
D5	RMW ON/OFF	0 : Out ; 1: In
D4	Data Scan Direction	0 : Column ; 1: Page
D3	Display ON/OFF	0 : OFF; 1: ON
D2	OTP Access	0 : OutAccess; 1: InAccess
D1	Inverse Display	0 : Inverse; 1: Normal
D0	Partial Display	0 : OFF; 1: ON

9.2.26 Read Status (4-Line and 3-Line SPI)

The command is to read the internal condition of the IC. One status can be displayed depending on the setting status after reset or after NOP operation

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	1	1	1	1	1	1	0	Read status byte
0	1	D7	D6	D5	D4	D3	D2	D1	D0	

Data Bus	Flag	Description
D7	Scroll Area Mode	Refer to SCM1
D6	Scroll Area Mode	Refer to SCM0
D5	RMW ON/OFF	0 : Out ; 1: In
D4	Data Scan Direction	0 : Column ; 1: Page
D3	Display ON/OFF	0 : OFF; 1: ON
D2	OTP Access	0 : OutAccess; 1: InAccess
D1	Inverse Display	0 : Inverse; 1: Normal
D0	Partial Display	0 : OFF; 1: ON

9.2.27 Data Format Select

Top/bottom mode sets data order.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	1	DO	0	0	Select LSB position

Flag	Description
DO	DO=0: LSB is on bottom ; D7→D0 (Default) DO=1: LSB is on top; D0→D7

9.2.28 Display Mode

This instruction defines the display mode is gray scale mode or monochrome mode.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	0	0	Set display mode DM=0 :Mono(Default) DM=1 :4Gray Scale Mode
1	0	0	0	0	1	0	0	0	DM	

9.2.29 Set ICON

This instruction is used to enable/disable ICON RAM.

ICON=0 ; Disable ICON RAM.

ICON=1 ; Enable ICON RAM.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	1	1	0	1	1	ICON	Enable/Disable ICON RAM

Ensure to write B/W data to ICON DDRAM in 4 gray scale mode.

"Extension Command 2"

9.2.30 Set Gray Level

This instruction is used to set gray scale level.

GL[4:0] : Set light gray level ; GD[4:0]: Set dark gray level.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	0	0	Set Gray Scale Level GL[4:0]: Set Light Gray Level GD[4:0]:Set Dark Gray Level
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
1	0	0	0	0	GL4	GL3	GL2	GL1	GL0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
1	0	0	0	0	GD4	GD3	GD2	GD1	GD0	
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	0	0	

Note:

1. The range of gray level is 0x00h~0x1Fh. 0x00h is the lightest gray scale level. 0x1Fh is the darkest gray scale level.
2. Parameter 4~6 should be set to the same value for light gray level.
3. Parameter 9,12~14 should be set to the same value for dark gray level

9.2.31 Analog Circuit Set

This instruction is used to set booster efficiency and bias ratio.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	1	0	0	1	0	Analog setting
1	0	0	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	0	BE1	BE0	
1	0	0	0	0	0	0	BS2	BS1	BS0	

Booster Efficiency set

BE1	BE0	Frequency on booster capacitors (Hz)
0	0	Level 0
0	1	Level 1 (Default)
1	0	Level 2
1	1	Level 3

Select LCD bias ratio of the voltage required for driving the LCD

BS2	BS1	BS0	LCD bias
0	0	0	1/14
0	0	1	1/13
0	1	0	1/12 (Default)
0	1	1	1/11
1	0	0	1/10
1	0	1	1/9

9.2.32 Booster Level

This instruction is used to control the built-in booster circuit to provide the power source of the built-in regulator.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	0	1	Analog setting
1	0	1	1	1	1	1	0	1	BST	

BST	Booster Level
0	X8
1	X10 (Default)

9.2.33 Driving Select

This instruction is used to decide power source mode.

DS=0 ; Internal (default)

DS=1 ; External

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	0	DS	Power source select

9.2.34 Auto Read Control

This instruction is used to set status of OTP auto read to enable or disable.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	1	XARD=0: Enable auto read
1	0	1	0	0	XARD	1	1	1	1	XARD=1: Disable auto read

9.2.35 OTP WR/RD Control

This instruction is used to set status of OTP that write to OTP or read from OTP.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	0	WR/RD=0: Enable OTP read WR/RD=1: Enable OTP write
1	0	0	0	WR /RD	0	0	0	0	0	

9.2.36 OTP Control Out

This instruction is used to cancel the OTP control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	0	1	OTP control out

9.2.37 OTP Write

This instruction is used to trigger OTP programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	0	OTP programming procedure

9.2.38 OTP Read

This instruction is used to trigger OTP programming procedure.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	0	1	1	OTP programming procedure

9.2.39 OTP Selection Control

This instruction is used to define OTP selection control.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	0	Ctrl=1: Disable OTP Selection
1	0	1	Ctrl	0	1	1	0	0	1	Ctrl=0: Enable OTP Selection

9.2.40 OTP Programming Setting

This instruction is used to set OTP write timing.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	0	0	1	0	1	OTP programming setting
1	0	0	0	0	0	1	1	1	1	

9.2.41 Frame Rate

The instruction is used to define frequency of frame rate in different temperature range as shown in **Figure 39**

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	0	0	FRA: FR in temp. -30°C to TA FRB: FR in temp TA to TB FRC: FR in temp. TB to TC FRD: FR in temp TC to 90°C
1	0	0	0	0	FRA4	FRA3	FRA2	FRA1	FRA0	
1	0	0	0	0	FRB4	FRB3	FRB2	FRB1	FRB0	
1	0	0	0	0	FRC4	FRC3	FRC2	FRC1	FRC0	
1	0	0	0	0	FRD4	FRD3	FRD2	FRD1	FRD0	

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
0	0	0	0	0	5.0
0	0	0	0	1	10.0
0	0	0	1	0	20.0
0	0	0	1	1	34.5
0	0	1	0	0	41.5
0	0	1	0	1	46.0
0	0	1	1	0	46.0
0	0	1	1	1	49.0
0	1	0	0	0	51.0
0	1	0	0	1	53.0
0	1	0	1	0	55.0
0	1	0	1	1	55.0
0	1	1	0	0	69.0
0	1	1	0	1	73.0

FRx4	FRx3	FRx2	FRx1	FRx0	Frame Rate (Hz)
0	1	1	1	0	76.5
0	1	1	1	1	76.5
1	0	1	0	0	83.0
1	0	1	0	1	92.0
1	0	1	1	0	92.0
1	0	1	1	1	98.0
1	1	0	0	0	102.0
1	1	0	0	1	106.0
1	1	0	1	0	110.0
1	1	0	1	1	110.0
1	1	1	0	0	138.0
1	1	1	0	1	146.0
1	1	1	1	0	153.0
1	1	1	1	1	153.0

The frame rate table is used for 32/64/80/128/160 duty. If the number of duty is changed, the frame rate will be different also.

9.2.42 Temperature Range

This instruction is used to define the temperature range for automatic frame rate adjustment according to current temperature as shown in **Figure 38**.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	0	1	0	TA[6:0]=TA Temp.(°C)+40 TB[6:0]=TB Temp.(°C)+40 TC[6:0]=TC Temp.(°C)+40
1	0	0	TA6	TA5	TA4	TA3	TA2	TA1	TA0	
1	0	0	TB6	TB5	TB4	TB3	TB2	TB1	TB0	
1	0	0	TC6	TC5	TC4	TC3	TC2	TC1	TC0	

Temp. Range Value	Temp. Rising State (°C)	Temp. Falling State (°C)
Freq. changing point A	(TA[6:0]-40)+5	TA[6:0]-40
Freq. changing point B	(TB[6:0]-40)+5	TB[6:0]-40
Freq. changing point C	(TC[6:0]-40)+5	TC[6:0]-40

9.2.43 Temperature Gradient Compensation

This instruction is used to define the temperature gradient compensation coefficient. The temperature gradient compensation coefficient setting is shown as below table.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	1	1	0	1	0	0	Set temperature gradient compensation coefficient
1	0	MT13	MT12	MT11	MT10	1	1	1	1	
1	0	MT33	MT32	MT31	MT30	MT23	MT22	MT21	MT20	
1	0	MT53	MT52	MT51	MT50	MT43	MT42	MT41	MT40	
1	0	MT73	MT72	MT71	MT70	MT63	MT62	MT61	MT60	
1	0	MT93	MT92	MT91	MT90	MT83	MT82	MT81	MT80	
1	0	MTB3	MTB2	MTB1	MTB0	MTA3	MTA2	MTA1	MTA0	
1	0	MTD3	MTD2	MTD1	MTD0	MTC3	MTC2	MTC1	MTC0	
1	0	MTF3	MTF2	MTF1	MTF0	MTE3	MTE2	MTE1	MTE0	

MTx3	MTx2	MTx1	MTx0	Mx (mV/°C)
0	0	0	0	0
0	0	0	1	-5
0	0	1	0	-10
:	:	:	:	:
1	1	0	1	-65
1	1	1	0	-70
1	1	1	1	-75

"Extension Command 4"

9.2.44 Enable OTP

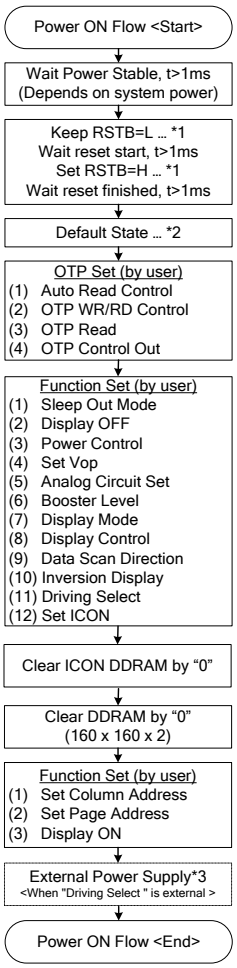
This instruction is used to disable/enable OTP programming.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	1	1	0	1	0	1	1	0	Enable OTP EOTP=0 ; Disable (Default) EOTP =1 ; Enable
1	0	0	0	0	EOTP	0	0	0	0	

10 OPERATION FLOW

10.1 Power ON

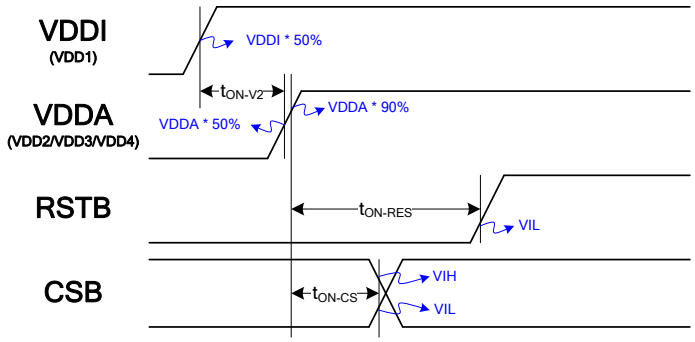
Referential Operation Flow	Operation Sequence



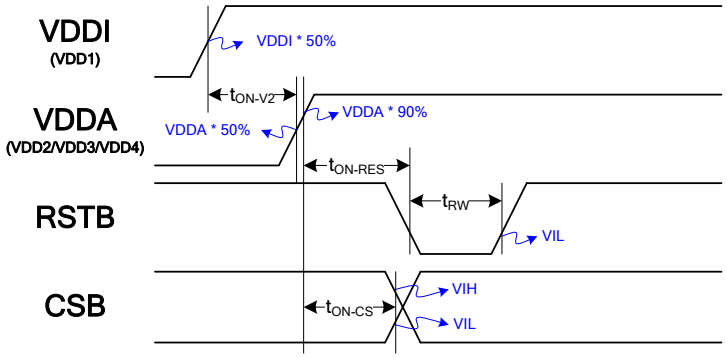
Note

1. Please refer to the specification of tRW and tR.
2. Refer to the section of Reset circuit.
3. The detail instruction functionality is described in section of INSTRUCTION DESCRIPTION.
4. The power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.
5. VDDA include VDD2, VDD3, VDD4

Case-1: RSTB=L while Power ON



Case-2: RSTB=H while Power ON



Item	Symbol	Requirement	Description
VDDA power ON delay	t_{ON-V2}	No Limitation	● VDDI and VDDA can be applied in any order. IC will NOT be damaged when one of VDDI and VDDA is ON but another is OFF. ● Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage. ● Recommend Setting: 0ms ≤ t_{ON-V2} ≤ No Limitation.
RSTB input time	t_{ON-RES}	Case-1 $t_{RW} \leq t_{ON-RES}$ Case-2 No Limitation	● RSTB =L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RSTB. ● RSTB has priority over CSB. ● Recommend Setting: 0 ≤ t_{ON-RES} ≤ 50 ms.
CSB input time	t_{ON-CS}	No Limitation	● CSB can be input at any time after power is stable.

Note: If RSTB is held high or unstable during power ON, a successful hardware reset by RSTB is required after VDDI and VDDA are both stable (as illustrated in Case-2). Otherwise, correct functionality can NOT be guaranteed.

10.2 Power OFF

Referential Operation Flow	Operation Sequence

Power OFF Flow <Start>
(Sleep Out Mode)

↓

External Power Stop
<When "Driving Select " is external >

↓

Function Set (by user)
(1) Display OFF
(2) Sleep In Mode

↓

Wait 120ms

↓

Keep RSTB=L

↓

Wait 200ms

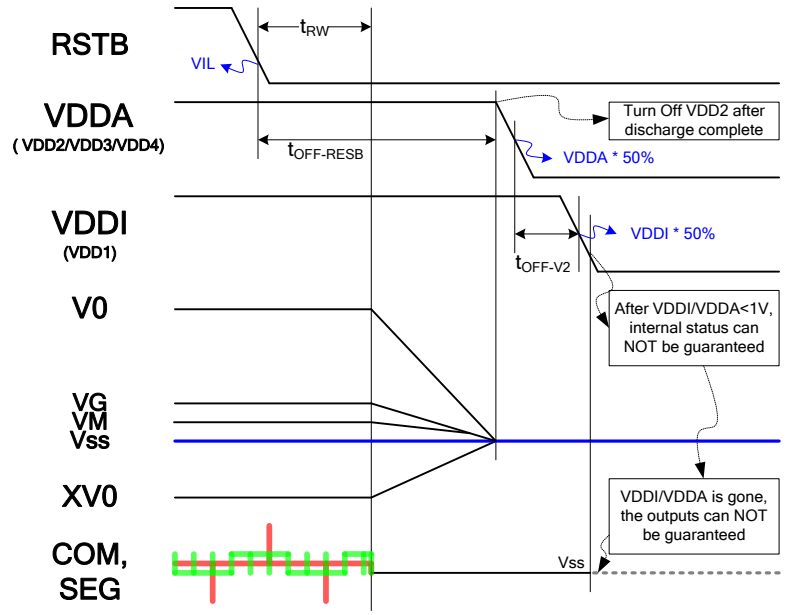
↓

Power OFF

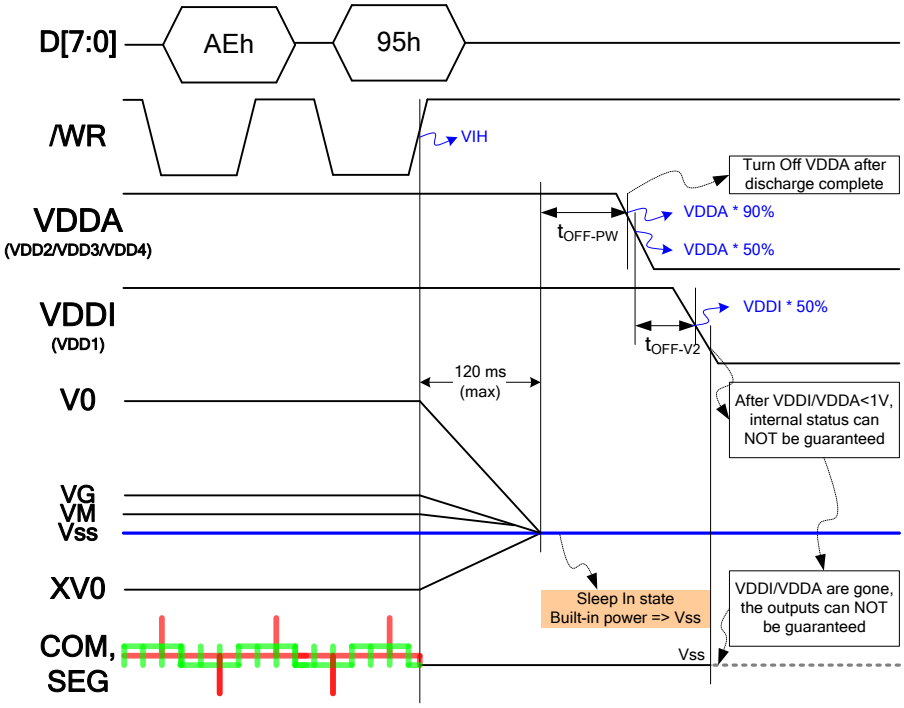
↓

Power OFF Flow <End>
(Sleep In Mode)

Case-1: Use RSTB



Case-2: Power OFF at Sleep State

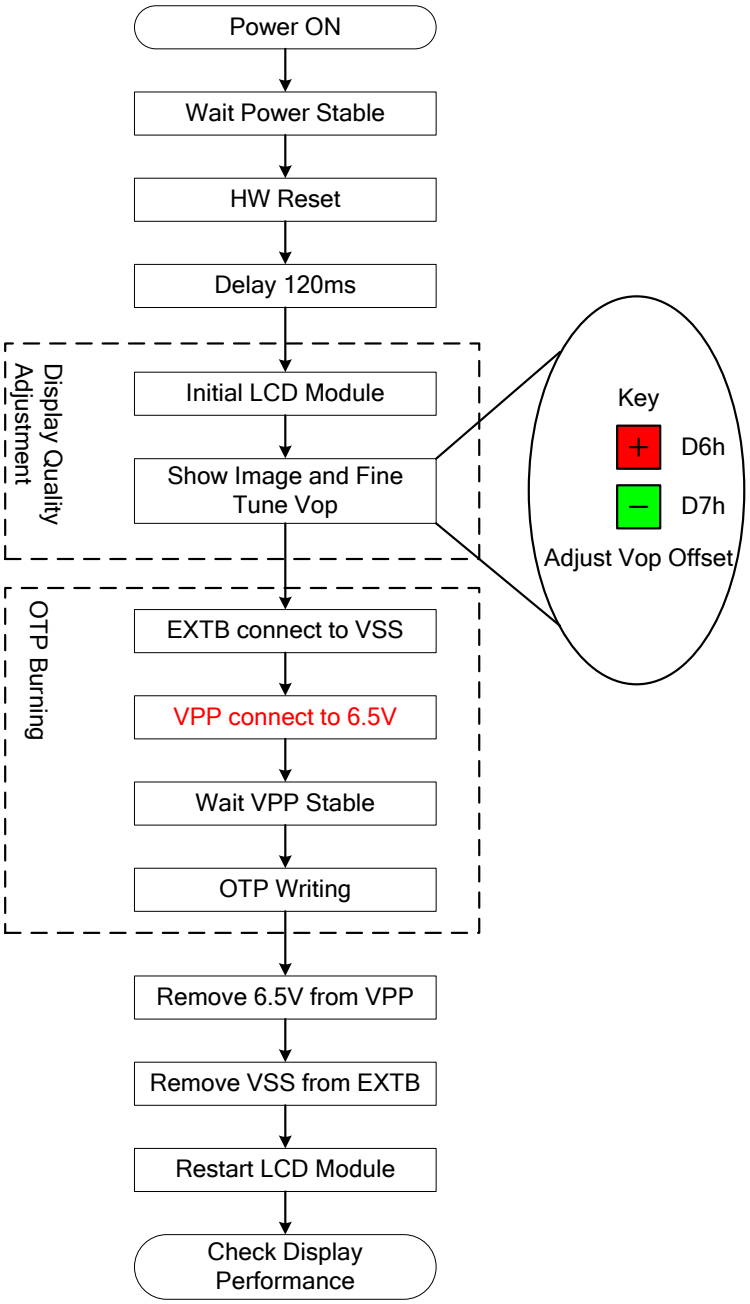


Item		Symbol	Requirement	Description
Power OFF Time	Case-1	$t_{OFF-RESB}$	200ms ≤$t_{OFF-RESB}$	● Power can be turned OFF after built-in power becomes VSS.
	Case-2	t_{OFF-PW}	0 ≤ t_{OFF-PW}	
VDDA power ON delay		t_{OFF-V2}	No Limitation	● VDDI and VDDA can be powered down in any order. IC will NOT be damaged when one of VDDI and VDDA is ON but another is OFF. ● Recommend Setting: 0ms ≤ t_{OFF-V2} ≤ No Limitation.

Note: In Case-2, RSTB can fall to VSS at the same time as VDDI.

10.3 OTP Operation

10.3.1 Referential OTP Burning Flow



Note:

- In this section “+” and “-” key button, please execute command D6h to increase one step at Vop and execute command D7h to decrease one step at Vop.

10.3.2 Referential OTP Operation Code

```
void Initialization_ST75160(void)
{
        Reset_ms(10);
        Write(Command, 0x31);                  // Extension Command 2
        Write(Command, 0xD7);                  // Disable Auto Read
        Write(Data, 0x9F);
        Write(Command, 0xE0);                  // Enable OTP Read
        Write(Data, 0x00);
        Delay_ms(10);
        Write(Command, 0xE3);                  // OTP Up-Load
        Delay_ms(20);
        Write(Command, 0xE1);                  // OTP Control Out
        Write(Command, 0x30);                  // Extension Command 1
        Write(Command, 0x94);                  // Sleep Out
        Write(Command, 0xAE);                  // Display OFF
        Delay_ms(50);
        Write(Command, 0x20);                  //Power Control
        Write(Data, 0x0B);                     // VB, VR,VF All ON
        Delay_ms(100);
        Write(Command, 0x81);                  // Set Vop = 16V
        Write(Data, 0x36);
        Write(Data, 0x04);
        Write(Command, 0x31);                  // Extension Command 2
        Write(Command, 0x20);                  // Set Gray Scale Level
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x17);                     //Light Gray Level Setting
        Write(Data, 0x17);                     //Light Gray Level Setting
        Write(Data, 0x17);                     //Light Gray Level Setting
        Write(Data, 0x00);
        Write(Data, 0x00);
        Write(Data, 0x1D);                     //Dark Gray Level Setting
        Write(Data, 0x00);
        Write(Data, 0x00);
```

```
Write(Data, 0x1D);          //Dark Gray Level Setting
Write(Data, 0x1D);          //Dark Gray Level Setting
Write(Data, 0x1D);          //Dark Gray Level Setting
Write(Data, 0x00);
Write(Data, 0x00);
Write(Command, 0x32);       // Analog Circuit Set
Write(Data, 0x00);
Write(Data, 0x01);          // Booster Efficiency =Level1
Write(Data, 0x02);          //Bias=1/12
Write(Command, 0x51);       // Booster Level x10
Write(Data, 0xFB);
Write(Command, 0x30);       // Extension Command 1
Write(Command, 0xF0);       //Display Mode
Write(Data, 0x11);          //4Gray Mode
Write(Command, 0xCA);       //Display Control
Write(Data, 0x00);          // CL Dividing Ratio → Not Divide
Write(Data, 0x9F);          //Duty Set→160 Duty
Write(Data, 0x00);          //Frame Inversion
Write(Command, 0xBC);       // Data Scan Direction
Write(Data, 0x00);
Write(Command, 0xA6);       // Normal Display
Write(Command, 0x31);       //Extension Command 2
Write(Command, 0x40);       //Internal Power Supply

Write(Command, 0x30);       // Extension Command 1
Write(Command, 0x77);       // Enable ICON RAM
Write(Command, 0x15);       // Column Address Setting
Write(Data, 0x00);          // SEG0 -> SEG159
Write(Data, 0x9F);
Clear_ICON_DDRAM();         //Clear Whole ICON DDRAM by "0"
Write(Command, 0x76);       // Disable ICON RAM

Write(Command, 0x30);       //Extension Command 1
Write(Command, 0x75);       // Row Address Setting
Write(Data, 0x00);          // COM0 -> COM159
Write(Data, 0x27);
Clear_DDRAM();              // Clear whole DDRAM by "0"
```

```
        Write(Command, 0x30);                   //Extension Command 1
        Write(Command, 0x15);                   // Column Address Setting
        Write(Data, 0x00);                      // SEG0 -> SEG159
        Write(Data, 0x9F);
        Write(Command, 0x75);                   // Row Address Setting
        Write(Data, 0x00);                      // COM0 -> COM159
        Write(Data, 0x27);

        Disp_Image();                           // Fill the DDRAM Data by Panel
                                                Resolution
        Write(Command, 0xAF);                   // Display ON
}

void Vop_Fine_Tune(void)
{
        Disp_Image();                           // Display the image
        Write(Command, 0x30);                   //Extension Command 1
        Write(Command, 0xAF);                   // Display ON
        Write(Command, 0xD6);                   // Fine tuning Vop to adjust display
        or                                      quality
        Write(Command, 0xD7);
}
```

```
void OTP_Write(void)
{
        Write(Command, 0x30);                   //Extension Command 1
        Write(Command, 0xAE);                   // Display OFF
        Delay_ms(50);                           // Delay 50ms

        Write(Command, 0x39);                   //Enable OTP
        Write(Command, 0XD6);
        Write(Data, 0x10);

        Write(Command, 0x31);                   //Extension Command 2
        Write(Command, 0xF0);                   // Frame Rate = 73Hz
        Write(Data, 0x0D);
        Write(Data, 0x0D);
        Write(Data, 0x0D);
        Write(Data, 0x0D);

        Write(Command, 0xE4);                   // OTP Selection Control
        Write(Data, 0x99);
        Write(Command, 0xE5);                   // OTP Programming Setting
        Write(Data, 0x0F);
        Write(Command, 0xE0);                   // OTP WR/RD Control
        Write(Data, 0x20);
        Delay_ms(100);                          // Delay 100ms
        Write(Command, 0xE2);                   // OTP Write
        Delay_ms(100);                          // Delay 100ms
        Write(Command, 0xE1);                   // OTP Control Out
        Write(Command, 0x30);                   //Extension Command 1
}
```

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices

12 ABSOLUTE MAXIMUM RATINGS

VSS=0V

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDDI (VDD1)	–0.3 ~ 4.0	V
Analog Power supply voltage	VDDA (VDD2~VDD4)	–0.3 ~ 4.0	V
LCD Power supply voltage	VLCDIN	–0.3 ~ 20	V
LCD Power supply voltage	V0-XV0	–0.3 ~ 19	V
LCD Power supply voltage	VG	–0.3 ~ VDDA+0.3	V
LCD Power supply voltage	VM	–0.3 ~ VDDA+0.3	V
MPU Interface Input Voltage	Vin	–0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	–30 to +85	°C
Storage temperature	TSTR	–55 to +125	°C

Note:

1. All voltages are respect to VSS unless otherwise noted (VSS1=VSS2=VSS3=VSS4=VSS5).
2. Insure the voltage levels of VLCDIN, V0, VG, VM, VSS and XV0 always match the correct relation while operating: VLCDIN > V0 ≥ VG > VM > VSS ≥ XV0
3. Stresses exceed the ranges listed above may cause permanent damage to IC. These values are stresses only. IC should be operated under DC/AC Characteristics condition for normal operation. If this condition is not met, IC operation may be error and the reliability may be deteriorated.
4. Parameters are valid in operating temperature range unless otherwise specified.
5. Interface input voltage range cannot exceed the maximum limitation of digital power supply voltage. Vin≦ 3.6V.

13 DC CHARACTERISTICS

VSS1=VSS2=VSS3=VSS4=VSS5=0V and Ta = –30 ~ 85 °C, unless otherwise specified.

Item	Symbol	Condition		Related Pin	Rating			Unit
					Min.	Typ.	Max.	
Digital Operating Voltage	VDDI			VDD1	1.7	–	3.6	V
Analog Operating Voltage	VDDA			VDD2~5	2.6	–	3.6	V
Input High-level Voltage	V_{IH}			MPU Interface	0.7*VDD1	–	VDD1	V
Input Low-level Voltage	V_{IL}			MPU Interface	VSS1	–	0.3*VDD1	V
Output High-level Voltage	V_{OH}			D[7:0]	0.8*VDD1	–	VDD1	V
Output Low-level Voltage	V_{OL}			D[7:0]	VSS1	–	0.2*VDD1	V
Input Leakage Current	I_{IL}	Vin = VDD1 or VSS1		MPU Interface	–1.0	–	1.0	μA
ON Resistance of LCD Drivers	R_{ON}	Ta=25°C Bias=1/14	Vop=16V ΔV=10%	COM Drivers	–	1	–	KΩ
			VG=3V, ΔV=10%	SEG Drivers	–	1	–	KΩ
Frame Frequency	f_{FR}	VDDI=VDDA=3.3V, N-Line OFF, FR= 0x0D Duty=1/160, Ta = 25°C		–	66	73	80	Hz
VLCDIN Voltage Input	VLCDIN			VLCDIN	7	–	19	V
Vop Voltage Output	Vop			V0-XV0[*1,2]	7	–	18	V
VG Voltage Output	VG			VG[*1,2]	1.8	–	VDD2	V
VM Voltage Output	VM			VM[*2]	0.9	VG/2	VDD2	V

Note:

1. V0, XV0 and VG include: V0I, V0O, V0S, XV0I, XV0O, XV0S, VGI, VGO & VGS.
2. V0, XV0, VG and VM do NOT support external power supply.

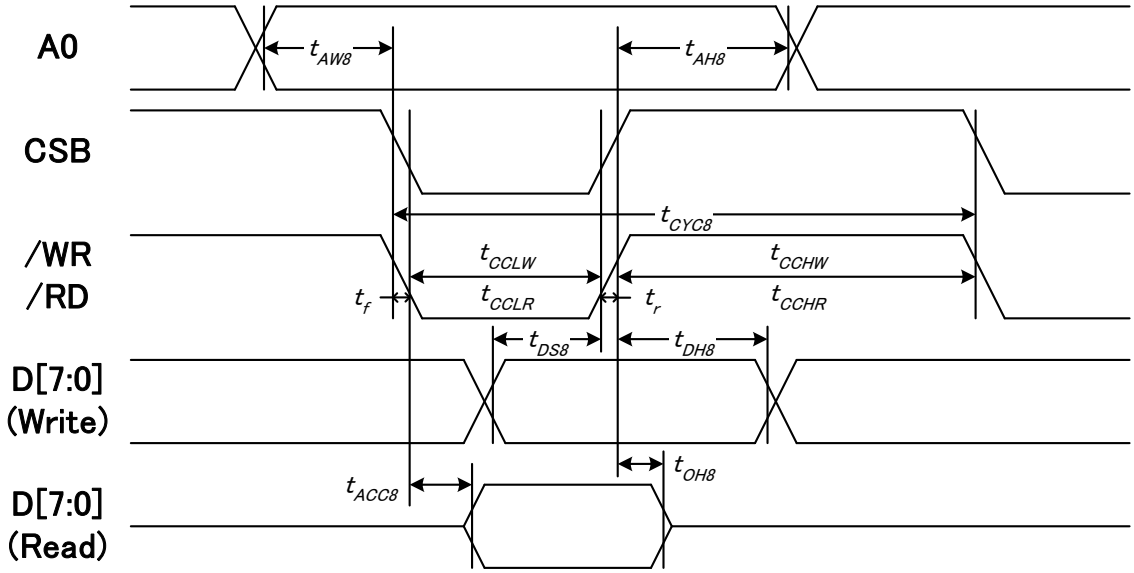
The current consumed by whole IC (bare die) with internal power system:

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display ON Pattern: SNOW (Static)	ISS	VDDI=VDDA=3.3V, 10x Booster, Vop = 14.0V, Bias=1/14 N-Line OFF, f_{FR}=73Hz, Ta=25°C	–	800	1000	μA
Sleep In	ISS	VDDI=VDDA=3.3V, Ta=25°C	–	10	20	μA

Note: The current is DC characteristic of a “Bare Chip”

14 AC CHARATERISTIC

14.1 System Bus Timing for 8080 MCU Interface



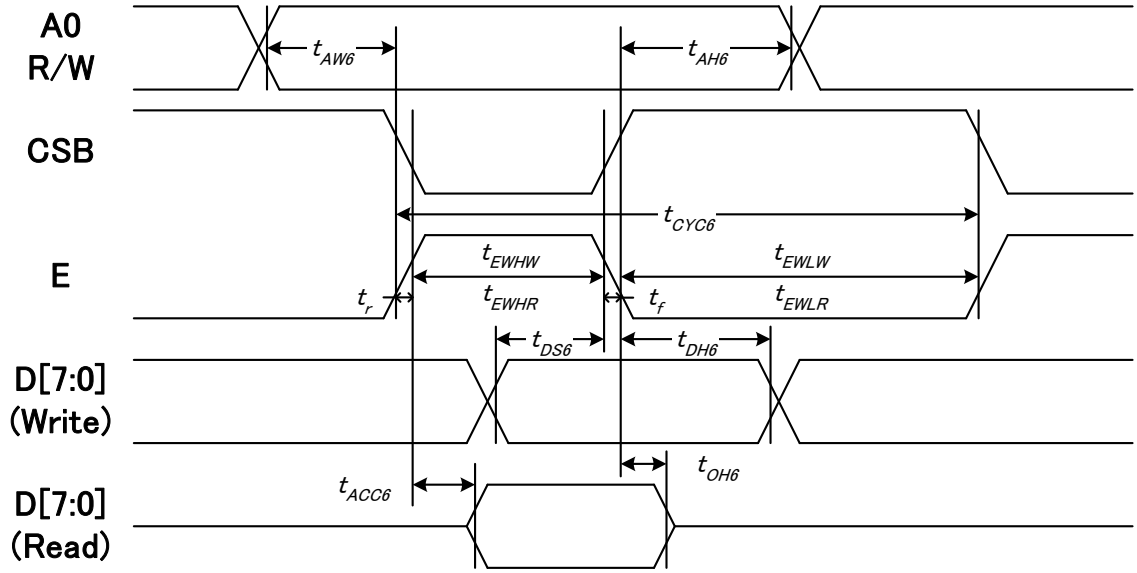
VDD1 = 1.8~3.3V, Ta = –30~85°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		20	—	ns
Address hold time		tAH8		0	—	
System cycle time (WRITE)	/WR	tCYC8		160	—	
/WR L pulse width (WRITE)		tCCLW		70	—	
/WR H pulse width (WRITE)		tCCHW		70	—	
System cycle time (READ)	RD	tCYC8		400	—	
/RD L pulse width (READ)		tCCLR		180		
/RD H pulse width (READ)		tCCHR		180		
WRITE Data setup time	D[7:0]	tDS8		15	—	
WRITE Data hold time		tDH8		15	—	
READ access time		tACC8	CL = 30 pF	—	100	
READ Output disable time		tOH8	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.

14.2 System Bus Timing for 6800 MCU Interface



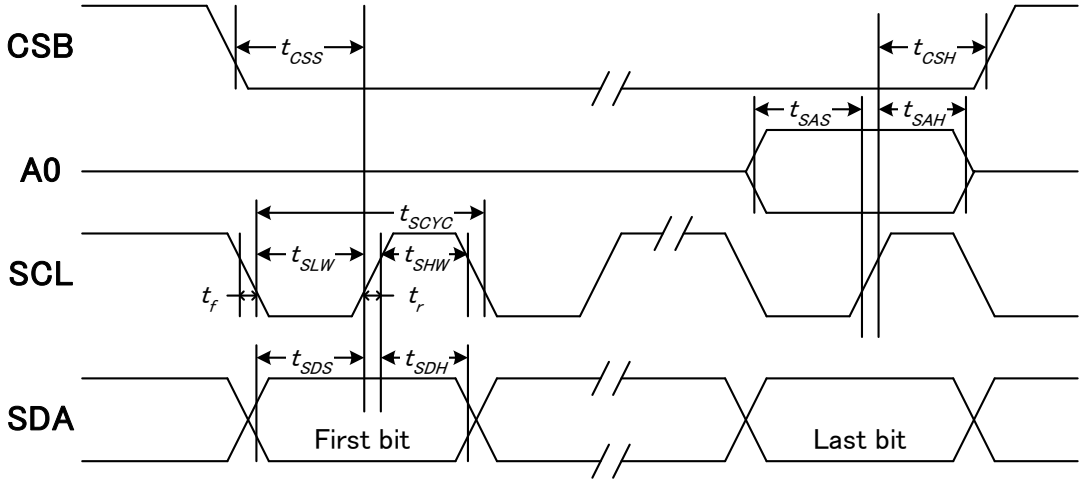
VDD1 = 1.8~3.3V, Ta = –30~85°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		20	—	ns
Address hold time		tAH6		0	—	
System cycle time (WRITE)	E	tCYC6		160	—	
Enable L pulse width (WRITE)		tEWLW		70	—	
Enable H pulse width (WRITE)		tEWHW		70	—	
System cycle time (READ)		tCYC6		400		
Enable L pulse width (READ)		tEWLR		180	—	
Enable H pulse width (READ)		tEWHR		180		
Write data setup time	D[7:0]	tDS6		15	—	
Write data hold time		tDH6		15	—	
Read data access time		tACC6	CL = 30 pF	—	100	
Read data output disable time		tOH6	CL = 30 pF	10	110	

Note:

1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.
2. All timing is specified using 20% and 80% of VDD1 as the reference.

14.3 System Bus Timing for 4-Line SPI MCU Interface



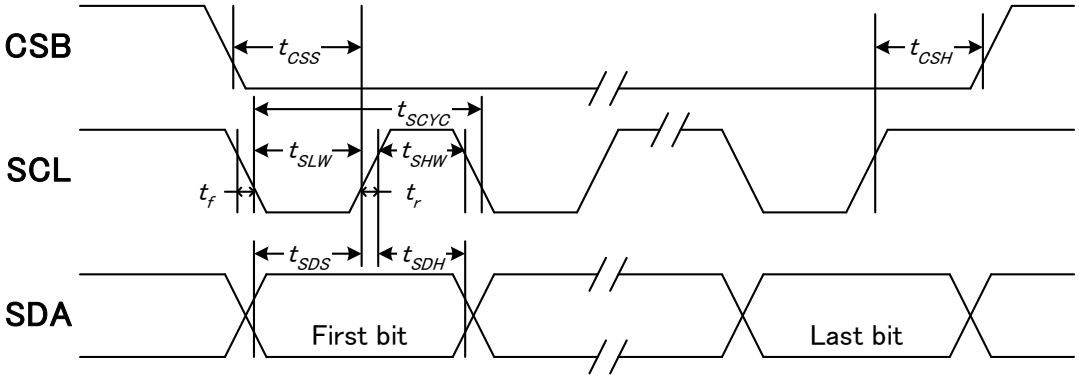
VDD1 = 1.8~3.3V, Ta = –30~85°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		80	—	ns
SCLK “H” pulse width		tSHW		30	—	
SCLK “L” pulse width		tSLW		30	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CSB-SCLK time	CSB	tCSS		20	—	
CSB-SCLK time		tCSH		20	—	
CS “H” pulse width		tCHW		0	-	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

14.4 System Bus Timing for 3-Line SPI MCU Interface



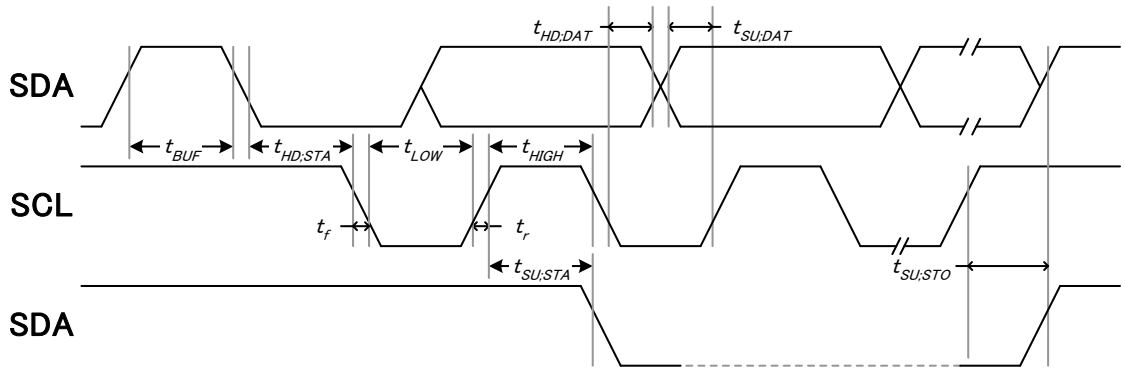
VDD1 = 1.8~3.3V, Ta = –30~85°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		80	—	ns
SCL “H” pulse width		tSHW		30	—	
SCL “L” pulse width		tSLW		30	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		20	—	
CSB-SCL time	CSB	tCSS		20	—	
CSB-SCL time		tCSH		20	—	

Note:

1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDD1 as the standard.

14.5 SERIAL INTERFACE (I²C Interface)



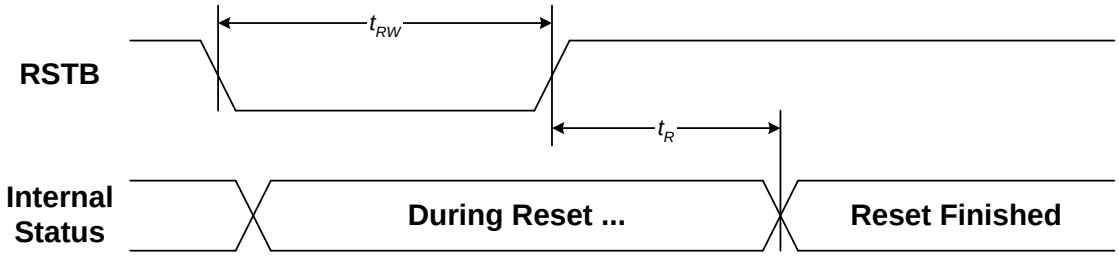
VDD1 = 1.8~3.3V, Ta = –30~85°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
SCL clock frequency	SCL	fSCL		-	400	KHZ
SCL clock low period		tLOW		1.3	-	us
SCL clock high period		tHIGH		0.6	-	
Data set-up time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Bus free time between a STOP and START		tBUF		0.1	-	
Signal rise time	SCL SDA	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns

Note:

1. All timing is specified using 20% and 80% of VDD1 as the standard.

14.6 Reset Timing



VDD1 = 1.8~3.3V, Ta = –30~85°C

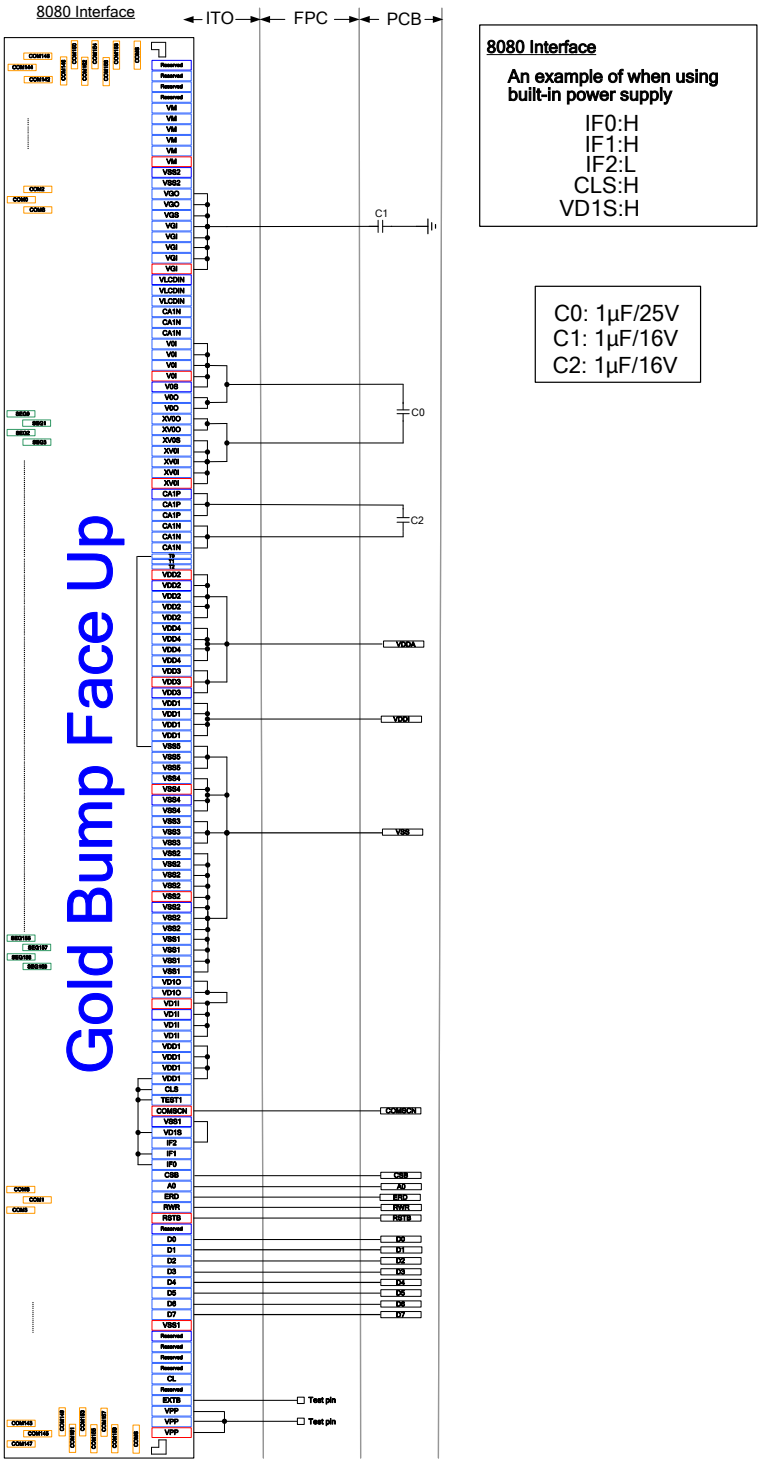
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1	ms
Reset “L” pulse width	tRW		1	—	ms

15 APPLICATION NOTE

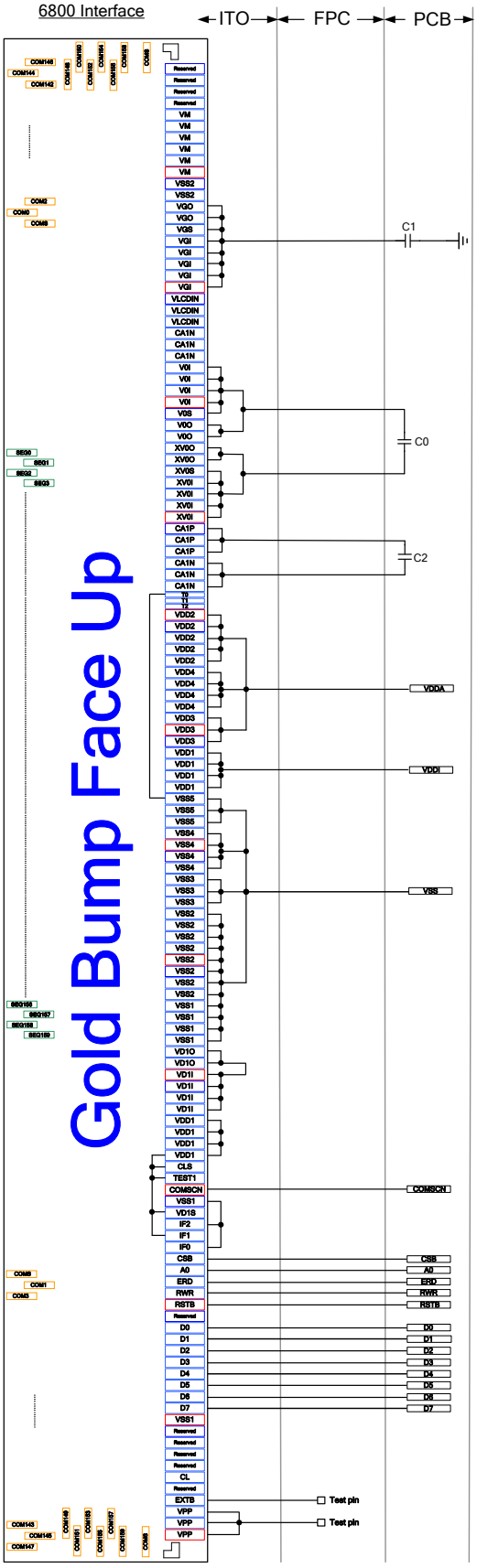
15.1 Application Circuit

The application circuits are examples of using built-in power supply. When using external power supply, please refer to the section 7.4.1 External Component of Power Circuit.

15.1.1 Parallel 8080 Interface



15.1.2 Parallel 6800 Interface



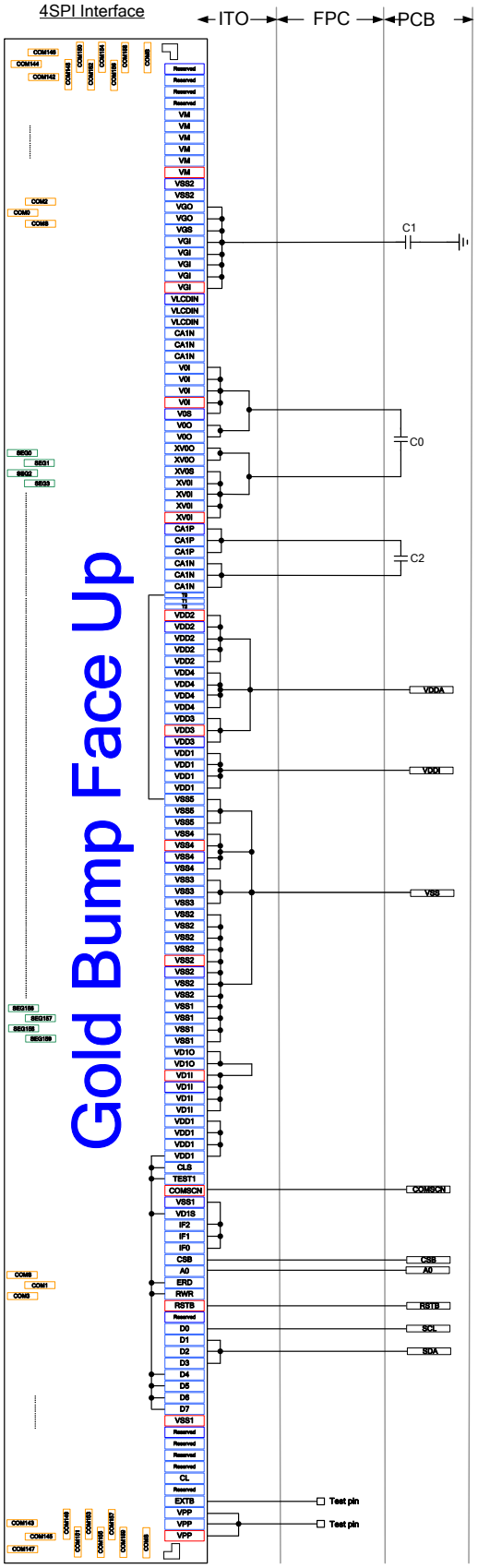
6800 Interface

An example of when using built-in power supply

IF0:L
IF1:H
IF2:L
CLS:H
VD1S:H

C0: 1µF/25V
C1: 1µF/16V
C2: 1µF/16V

15.1.3 4-Line SPI Interface



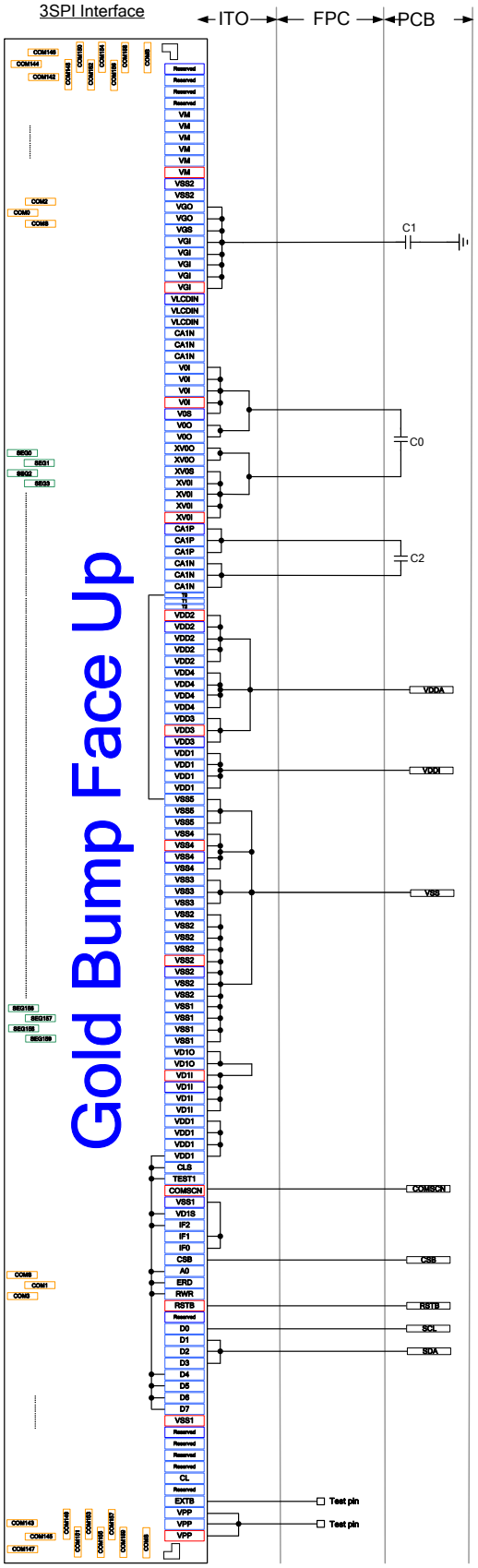
4-Line SPI Interface

An example of when using built-in power supply

IF0:L
IF1:L
IF2:L
CLS:H
VD1S:H

C0: 1µF/25V
C1: 1µF/16V
C2: 1µF/16V

15.1.4 3-Line SPI Interface



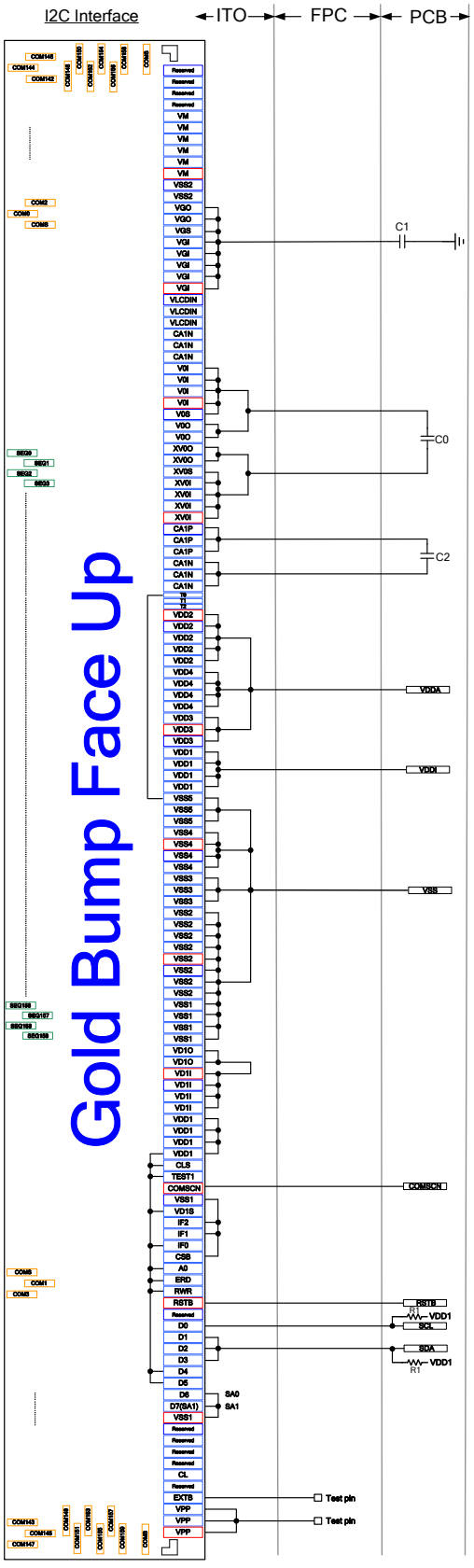
3-Line SPI Interface

An example of when using built-in power supply

IF0:L
IF1:L
IF2:H
CLS:H
VD1S:H

C0: 1µF/25V
C1: 1µF/16V
C2: 1µF/16V

15.1.5 I²C Interface



I2C Interface

An example of when using built-in power supply

IF0:H
IF1:L
IF2:L
CLS:H
VD1S:H

C0: 1µF/25V
C1: 1µF/16V
C2: 1µF/16V
R1: 3~5 KΩ

16 REVISION HISTORY

Version	Date	Description
V1.0	2013/09/05	● Preliminary
V1.1	2013/11/15	● Modify MAXIMUM RATINGS ● Add ITO Layout Reference
V1.1a	2013/11/25	● Modify Gold Bump
V1.2	2014/04/25	● Add Set ICON Flow ● Modify frame rate default value ● Modify Application Circuit
V1.2a	2014/05/02	● Replace Cover ● Modify temperature range and add for industrial application ● Add Gray Level Setting
V1.3	2014/07/01	● Modify capacitance value of external power supply. ● Remove high power mode. ● Add 3-Line SPI and serial read status.
V1.4	2014/12/08	● Modify Application Circuit for COMSCN ● Remove ID Function ● Modify All Pixel On/Off Instruction Description ● Modify Operation Temperature (-30°C ~85°C)
V1.5	2015/02/17	● Add Partial Duty with COMSCN Description
V1.6	2016/04/29	● Modify COMSCN Pin Description ● Modify Partial Display Application with COMSCN ● Modify ABSOLUTE MAXIMUM RATINGS & DC CHARACTERISTICS