DATA SHEET

FT5426G Preliminary

True Multi-Touch
Capacitive Touch Panel Controller

May. 21, 2021

Version: 0.1

Table of Contents

PAGE

TABLE OF CONTENTS 3
INTRODUCTION 4
FEATURES 4
1. OVERVIEW 5
1.1. TYPICAL APPLICATIONS 5
2. FUNCTIONAL BLOCK DESCRIPTION 6
2.1. ARCHITECTURE OVERVIEW 6
2.2. MCU 7
2.3. OPERATION MODES 7
2.4. INTERFACE 8
2.5. SERIAL INTERFACE 8
3. ELECTRICAL SPECIFICATIONS 10
3.1. ABSOLUTE MAXIMUM RATINGS 10
3.2. DC CHARACTERISTICS 11
3.3. AC CHARACTERISTICS 11
3.4. I/O PORTS CIRCUITS 12
3.5. POWER ON/ RESET SEQUENCE 12
4. PIN CONFIGURATIONS 15
5. PACKAGE INFORMATION 17
5.1. PACKAGE INFORMATION OF BGA-5X5-81 PACKAGE 17
5.2. ORDER INFORMATION 18
6. POWER CONSUNMPTION REFERENCE 18
7. DISCLAIMER 19
8. REVISION HISTORY 20

INTRODUCTION

The FT5426G is single-chip capacitive touch panel controllers with built-in enhanced 16bit Micro-controller unit (MCU).It provides the benefits of full screen common mode scan technology, fast response time and high level of accuracy. It can drive capacitive type touch panel with up to 16 driving and 30 sensing lines.

FEATURES

- Mutual Capacitive Sensing Techniques
- Full Screen Common Mode Scan Techniques
- True Multi-touch up to 10Points of absolute X and Y Coordinates
- High immunity to RF and power Interferences
- Supports up to 16TX + 30RX
- Supports up to 10 fingers
- High immunity to inductive power noise
- Automatic mode switching (Active, Monitor, Sleep)
- Support up to 2 fingers 240Hz touch sampling rate
- Auto-calibration
- 11-Bit ADC Accuracy
- Serial interfaces :
  - I2C, up to 400Kbps
- Power
  - 2.7 V to 3.6V Operating Voltage
  - IOVCC supports 1.7V~3.6V
- Built-in 128KB Flash
- 3 Operating Modes
  - Active
  - Monitor
  - Sleep
- Operating Temperature Range: -30°C to +85°C
- Package:
  - QFN56 6x6x0.6mm, 0.35mm/pitch
- ESD:HBM ±2000V; MM ±200V

1. OVERVIEW

1.1. TYPICAL APPLICATIONS

FT5426G accommodates a wide range of applications with a set of buttons up to a 2D touch sensing device; It's powerful design for below applications.

- Tablets
- Mobiles
- Navigation systems, GPS
- Game consoles
- POS (Point of Sales) devices
- Digital cameras

FT5426G support Touch Panel, the spec is listed in the following table,

Part Number	Package	TX	RX	Total Channels	Recommended for TP Size
FT5426G	QFN 56L 6x6x0.6mm Pitch =0.35mm	16	30	46	≦ 7.0”

2. FUNCTIONAL BLOCK DESCRIPTION

2.1. Architecture Overview

Figure2-1 shows the overall architecture for the FT5426G.

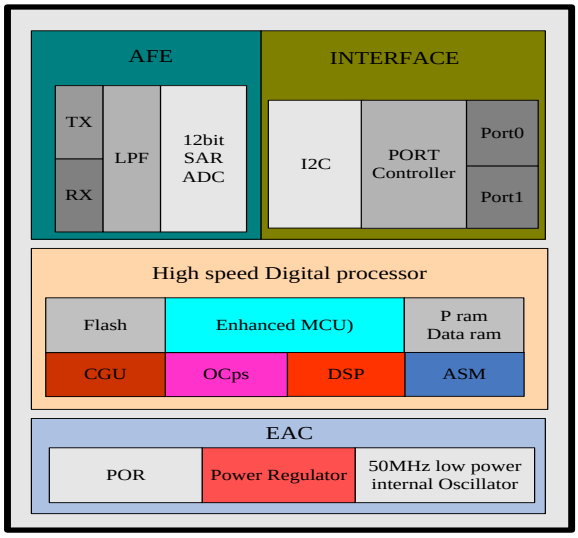


Figure 2-1 System Architecture Diagram

The FT5426G is comprised of five main functional parts listed below,

- **Touch Panel Interface Circuits**

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. It includes both Transmit (TX) and Receive (RX) functions. Key parameters to configure this circuit can be sent via serial interfaces.

- **Enhanced MCU with DSP accelerator**

For the Enhanced MCU, larger program and data memories are supported. Furthermore, a Flash memory is implemented to store programs and some key parameters.

Complex signal processing algorithms are implemented by MCU and DSP accelerator to detect the touches reliably and efficiently. Communication protocol software is also implemented in this MCU to exchange data and control information with the host processor.

- **External Interface**
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip. The port is also use to wake up the FT5426G from the Sleep mode.
- **A watch dog timer is implemented to ensure the robustness of the chip.**
- **A voltage regulator to generate 1.8V for digital circuits from the input VDD3 supply**
- **Power-On Reset (POR) is active until VDDD is higher than some level and hold decades of μs.**

2.2. MCU

This section describes some critical features and operations supported by the enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the enhanced MCU core, we have added the following circuits,

- A DSP accelerator cooperates with MCU to process the complex algorithms
- Timer: A number of timers are available to generate different clocks
- Clock Manager: To control various clocks under different operation conditions of the system

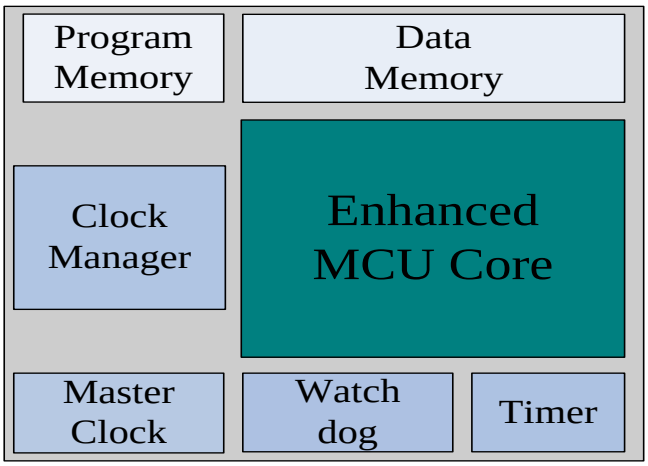


Figure 2-2 MCU Block Diagram

2.3. Operation Modes

FT5426G offers following three modes:

- **Active Mode**

When in this mode, FT5426G actively scans the panel. The default scan rate is 100 frames per second. The host processor can configure it to speed up or to slow down.

- **Monitor Mode**

In this mode, FT5426G scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. In this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT5426G shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor.

- **Sleep Mode**

In this mode, the chip is set in a power down mode. It shall only respond to the “RESET” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

2.4. Interface

Figure 2-3 shows the interface between a host processor and FT5426G. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT5426G to the Host
- Reset Signal from the Host to FT5426G

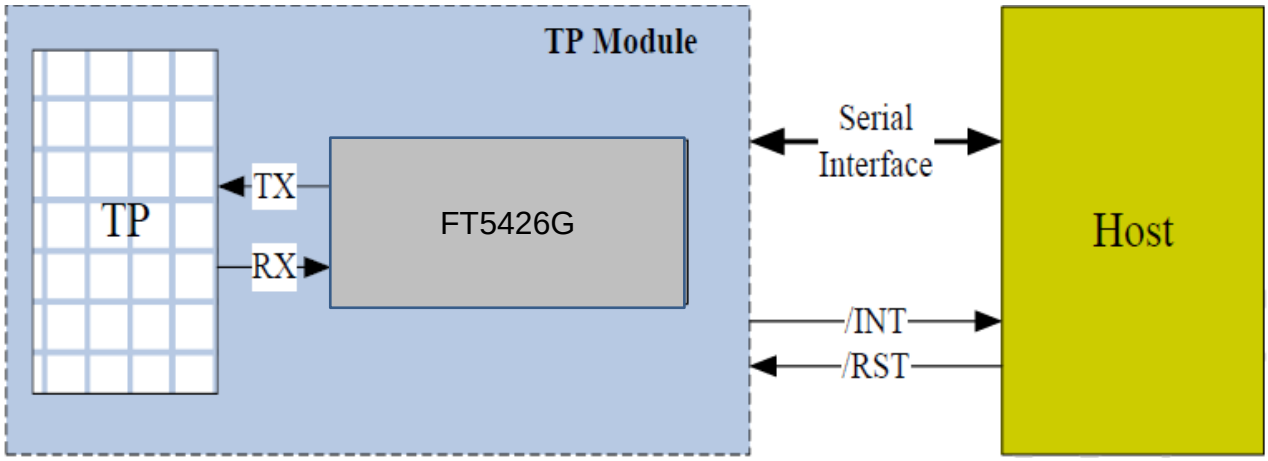


Figure 2-3 Host Interface Diagram

The serial interface of FT5426G is I2C. The detail of the interface is described in detail in Section 2.5. The interrupt signal (/INT) is used for FT5426G to inform the host that data are ready for the host to receive. The /RST signal is used for the host to wake up FT5426G from the Hibernate mode. After resetting, FT5426G shall enter the Active mode.

2.5. Serial Interface

- **I2C Interface**

FT5426G supports the I2C interfaces, which can be used by a host processor or other devices.

The default I2C address is 0x70 and can be changed to the other assigned address by setting.

The I2C is always configured in the Slave mode. The data transfer format is shown in **Figure 2-4**.

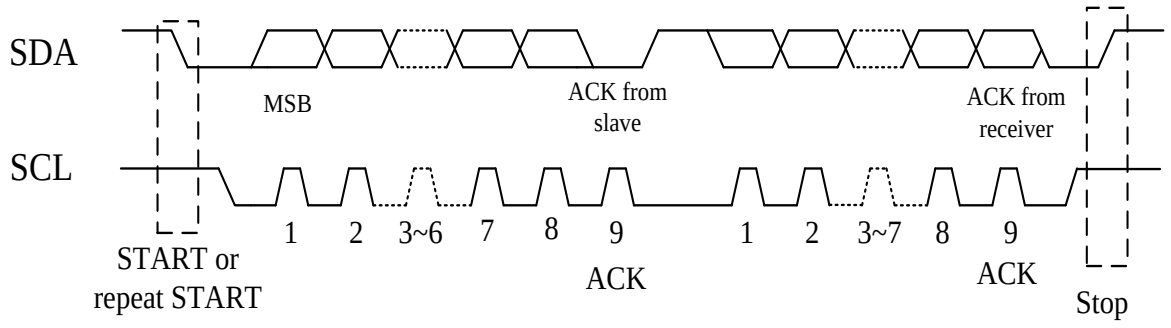


Figure 2-4 I2C Serial Data Transfer Format

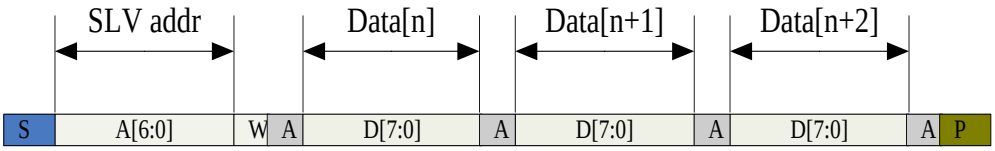


Figure 2-5I2C master write, slave read

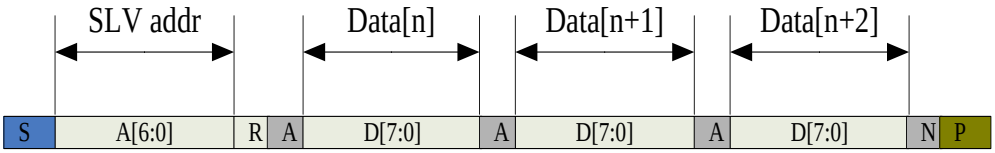


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/ W	READ/WRITE bit, ‘1’ for read, ‘0’for write
A(N)	ACK(NACK) bit
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	0	400	KHz
Bus free time between a STOP and START condition	1.3		us
Hold time (repeated) START condition	0.6		us
Data setup time	100		ns
Setup time for a repeated START condition	0.6		us
Setup Time for STOP condition	0.6		us

3. ELECTRICAL SPECIFICATIONS

3.1. Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDD3 – VSS	2.7 ~ +3.6	V	1, 2
I/O Digital Voltage	IOVCC	1.7~ +3.6	V	1
Operating Temperature	Topr	-30 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1
ESD “Human Body Mode”	HBM	8000	V	3
ESD “Charged Device Mode”	CDM	≧1000	V	4
Latch up	I latch-up	+/-200@1.5Vmax	mA	5

Notes

1. If used beyond the absolute maximum ratings, FT5426G may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDD (high) ≥VSS (low)
3. ESD HBM refers to ANSI/ESDA/JEDEC JS-001-2014.
4. ESD CDM is based on JESD22-C101-E.
5. Latch up refers to JESD78

3.2. DC Characteristics

Table 3-2 DC Characteristics

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high-level voltage	VIH	V		0.7 x IOVCC	--	IOVCC+0.3	
Input low -level voltage	VIL	V		-0.3	--	0.3 x IOVCC	
Output high -level voltage	VOH	V		0.7 x IOVCC	--	--	
Output low -level voltage	VOL	V		--	--	0.3 x IOVCC	
I/O leakage current	ILI	uA		-1	--	1	
Step-up output voltage	VDD5	V	VDD3=2.8V		5V		
Power Supply voltage	VDD3	V		2.7	--	3.6	

Notes:

This sample data is intended for design guidance only. Values shown are typical for a 16Tx × 28Rx sensor configured at 103 Hz report rate. Actual current will depend on the particular sensor design and firmware options. The DC characteristics are tested under the temperature 25℃.

3.3. AC Characteristics

AC Characteristics of Oscillators

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
OSC clock 1	fosc1	MHz	VDD3=2.8V; Ta=25℃	63.3	64	64.7	

Table 3-3 AC Characteristics of TX

Item	Symbol	Test Condition	Min	Typ	Max	Unit	Note
TX acceptable clock	ftx		50	150	400	KHz	

3.4. I/O PORTS CIRCUITS

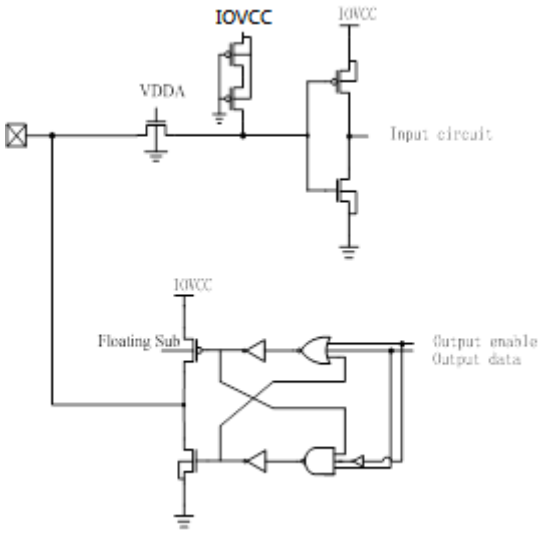


*Figure 3-1*General Purpose *In/Out Port Circuit*.

The input/output property can be configured via firmware setting. The firmware can also control its output behavior as push-pull or as open-drain that SDA of I2C interface is required.

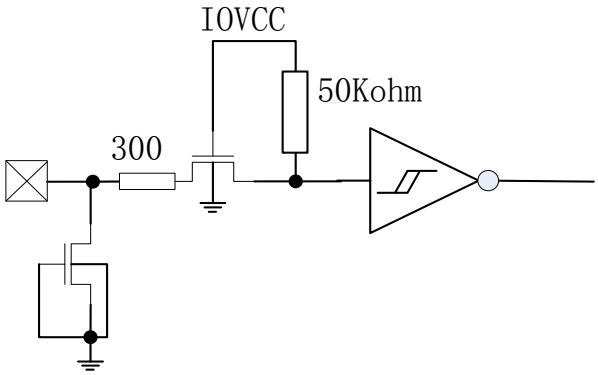


Figure 3-2 Reset Input Port Circuits

3.5. Power ON/ Reset Sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

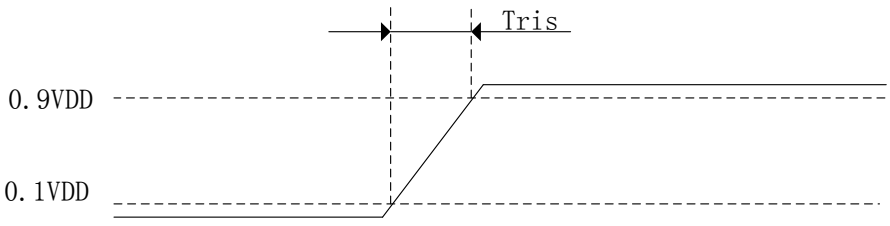


Figure 3-3 Power on time

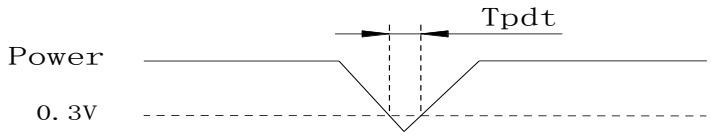


Figure 3-4 Power Cycle requirement

There are two power supply configurations, in one mode, VDD supplies whole chip exclude the communication I/O and GPIO, IOVCC supplies this part power, as figure 3-5-1. And the other mode, VDD supplies whole chip power, as figure 3-5-2;

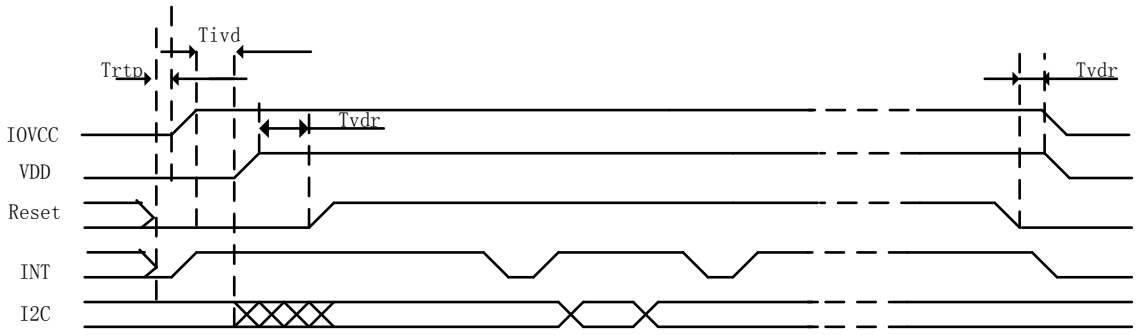


Figure 3-5-1 Power on Sequence for 2 power sources

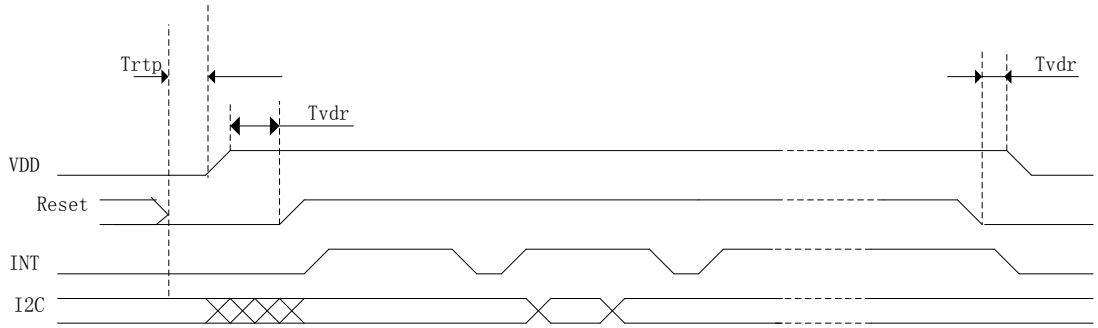


Figure 3-5-2 Power on Sequence for 1 power source

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

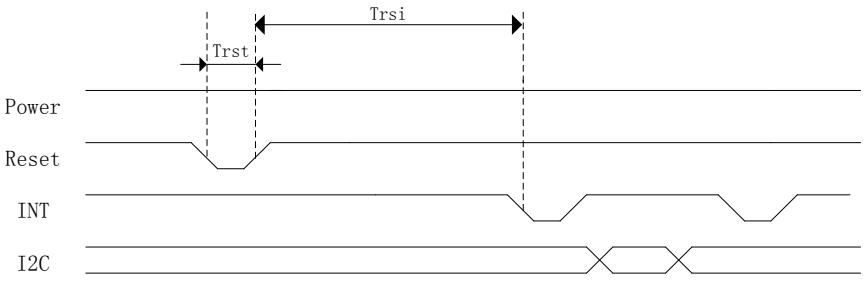


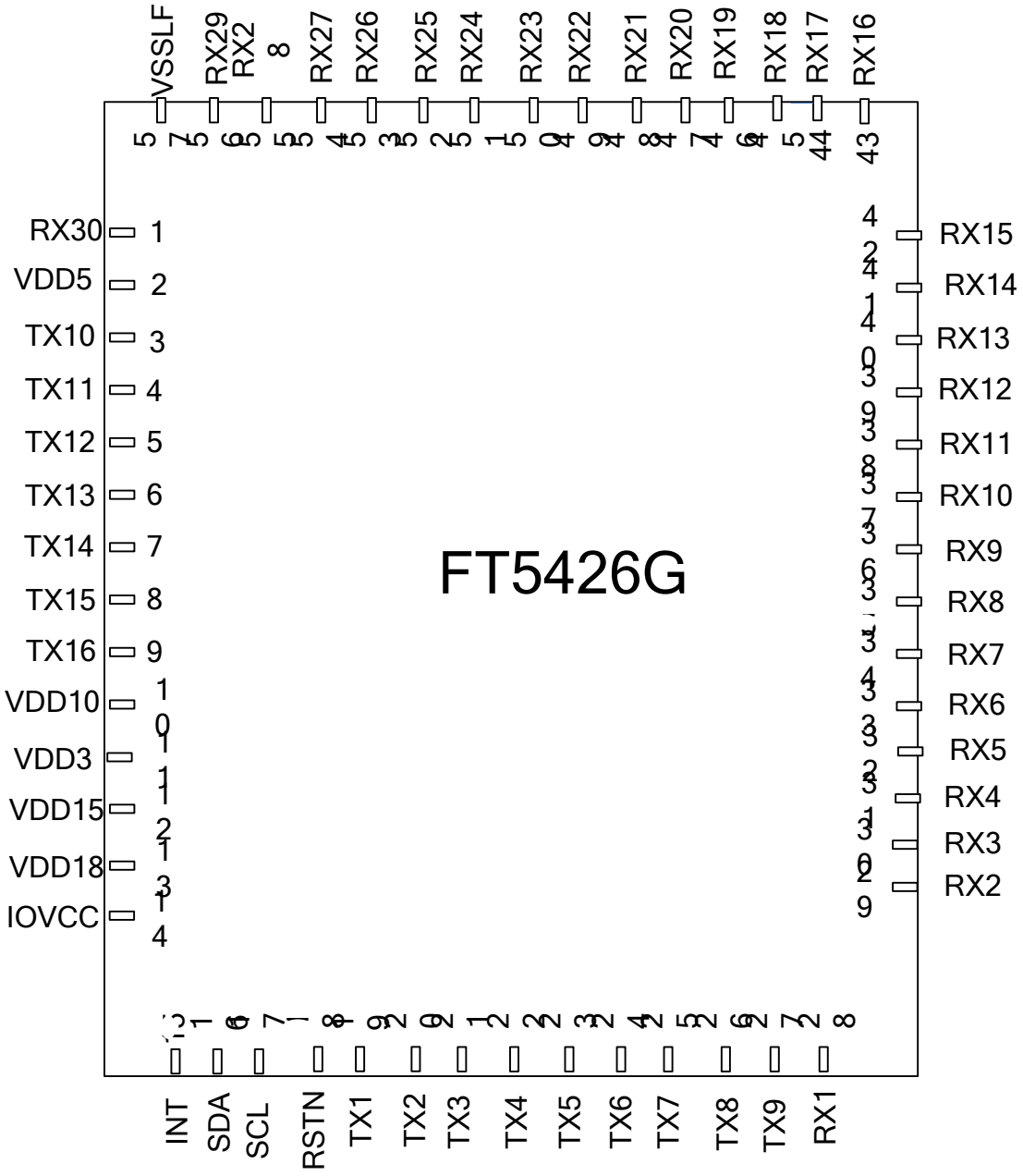
Figure 3-6 Reset Sequence

Table 3-5 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC	10		μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	1	--	ms

4. Pin Configurations

Pin List of FT5426G



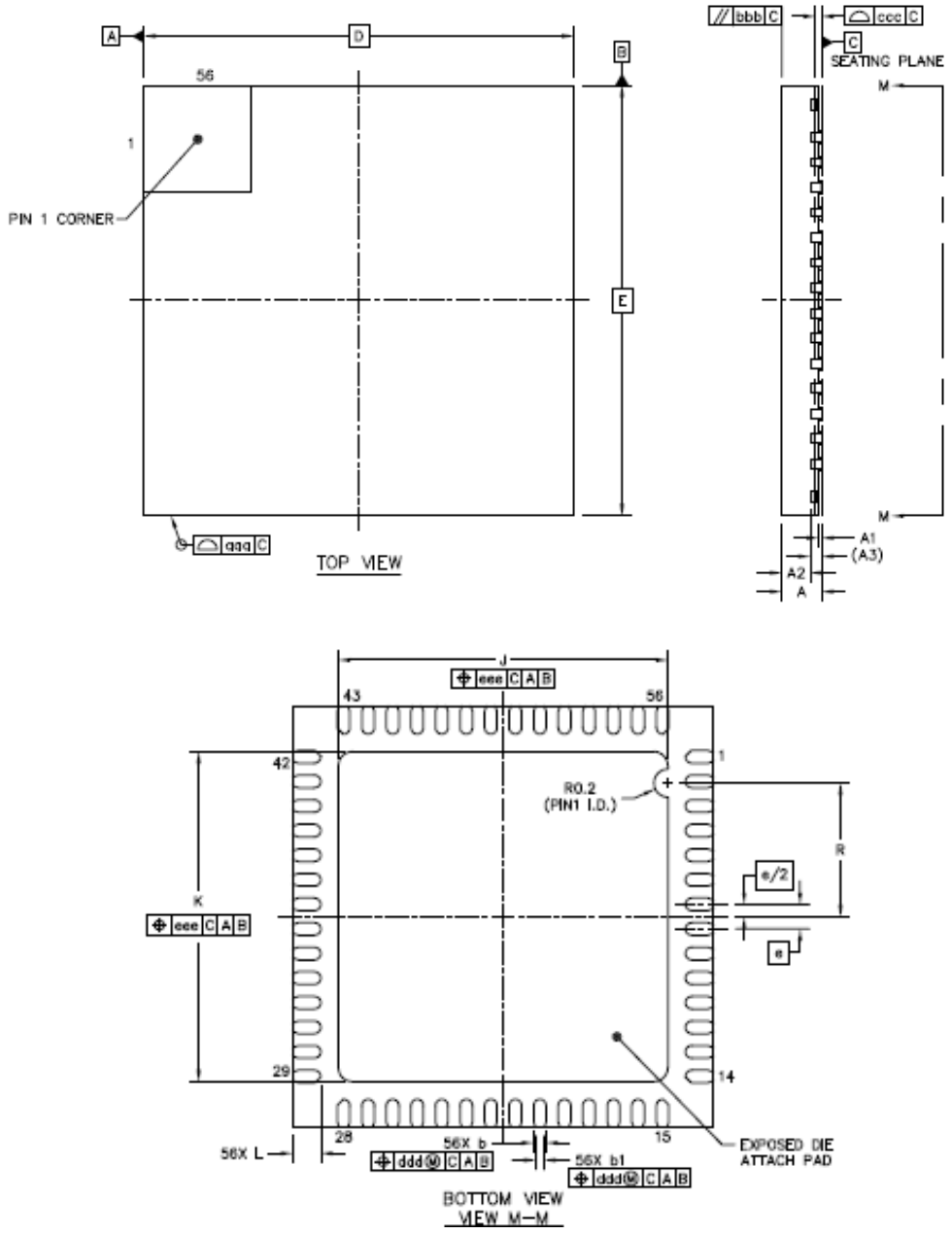
FT5426G Package Diagram

Table 5-1 Pin Definition

Signal	I/O	PAD Type	Function Description
Power Supply Pad			
VDD3	I	Analog Power	VDD3 is IC's Power supply Connect a capacitor for stabilization (2.7V~3.6V)
IOVCC	I	IO Digital Power	IOVCC is GPIO Power supply Connect a capacitor for stabilization (1.7V~3.6V)
GND	I	Ground	Ground for whole chip
Regulator & Pump Pad			
VDD15	O	Digital Power	Internal voltage regulator power output for digital circuit（1.35V~1.65V), Connect a capacitor for stabilization
VDD18	O	Digital Power	Internal voltage regulator power output for IO digital circuit（1.7V~1.9V), Connect a capacitor for stabilization
VDD5_OUT	O	Charge Pump	Charge Pump output voltage, external connect to VDD5_IN (4.5V~6.5V), Connect a capacitor for stabilization
VDD5_IN	I	Charge Pump	Charge Pump voltage, external connect to VDD5_OUT (4.5V~6.5V)
VDD10	O	Charge Pump	Charge Pump output voltage for TX driving (7V~11.5V) Connect a capacitor for stabilization
IO Interface PAD			
SCL	I/O	Digital IO	When interface is configured as I2C, GPIO0 is SCL
SDA	I/O	Digital IO	When interface is configured as I2C, GPIO1 is SDA
INT	I/O	Digital IO	INT signal.
RSTN	I	Digital IO	Hardware Reset Pin, Low：Reset
TX & RX Pad			
TX1~ TX16	I/O	TX	Scan Drive channel
RX1~ RX30	I/O	RX	Receive channel

5. PACKAGE INFORMATION

5.1. Package Information of QFN-6x6-56L Package



Item		Symbol	Millimeter		
			Min	Type	Max
Total Thickness		A	0.5	0.55	0.6
Stand Off		A1	0	0.035	0.05
Mold Thickness		A2	----	0.4	----
L/F Thickness		A3	0.152 REF		
Lead Width		b	0.13	0.18	0.23
		b1	0.07	0.12	0.17
Body Size	X	D	6 BSC		
	Y	E	6 BSC		
Lead Pitch		e	0.35 BSC		
EP Size	X	J	3.9	4	4.1
	Y	K	3.9	4	4.1
Lead Length		L	0.35	0.4	0.45
		R	1.45	1.55	1.65
Package Edge Tolerance		aaa	0.1		
Mold Flatness		bbb	0.1		
Co Planarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

5.2. Order Information

Product Name	Package Type	# TX Pins	# RX Pins
FT5426G	**QFN56 6*6*0.6 Pitch0.35mm**	**16**	**30**

6. POWER CONSUNMPTION REFERENCE

Test conditions: VDD3=3.3V, VDD18=1.8V. Temperature 25℃

Mode	Typ	Unit	Test Condition: Single power supply	Note
Active, 120Hz	TBD	mW	VDD3=3.3V	One finger
Active, 180Hz	TBD	mW	VDD3=3.3V	One finger
Active, 240Hz	TBD	mW	VDD3=3.3V	One finger
Idle, 100Hz	TBD	mW	VDD3=3.3V	
Sleep	0.21	mW	VDD3=3.3V	

Notes: This sample data is intended for the design guidance only. The typical value are for a 16TX*30RX sensor panel. The actual current will depend on the sensor design and firmware configuration.

7. DISCLAIMER

The information appearing in this publication is believed to be accurate.

Integrated circuits sold by FocalTech Systems are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. FocalTech Systems makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, FocalTech Systems MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. FocalTech Systems reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by FocalTech Systems for such applications. Please note that application circuits illustrated in this document are for reference purposes only.

8. REVISION HISTORY

Date	Revision #	Description	Page	Auditor
May. 21, 2021	0.1	1st Preliminary	All	MKT