APPENDIX SUMMARY

Reference	Item
APPENDIX I	SSD1333Z
APPENDIX II	SSD1333 Bump Die Pad Coordinates
APPENDIX III	SSD1333 Command Table
APPENDIX IV	SSD1333 Command Description
APPENDIX VI	SSD1333 Master Contrast Curent Control

Appendix I: SSD1333Z

Table 1-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1333Z	176RGB	176	COG	○ Min SEG pad pitch : 27um ○ Min COM pad pitch : 27um ○ Min I/O pad pitch : 55um ○ Die thickness: 250um ○ Bump height: nominal 12um

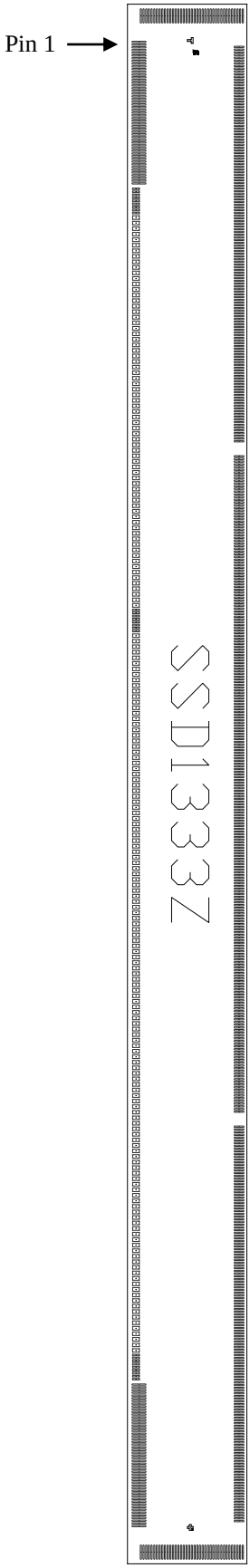


Figure 1-2: – SSD1333Z Die drawing

Die size	15.48 mm +/- 0.05mm x 1.20 mm+/- 0.05mm
Die thickness	250 +/- 15um
Min I/O pad pitch	55um
Min SEG pad pitch	27um
Min COM pad pitch	27um
Bump height	Nominal 12 um

Bump size		
Pad#	X[um]	Y[um]
1~53, 281~333	12	140
54~62, 134~141, 272~280	15	67
63~133, 142~271	35	67
334~372, 907~945	140	12
373~906	12	100

Alignment mark	Position	Size
+ shape	(7379.5, 31.5)	56.25um x 56.25um
T shape	(-7379.5, 31.5)	56.25um x 56.25um

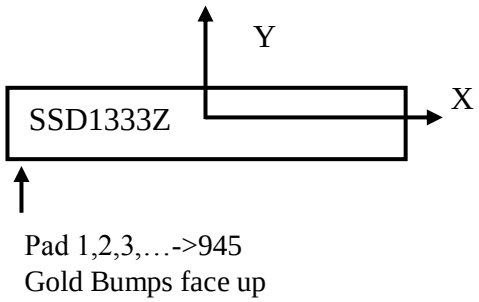
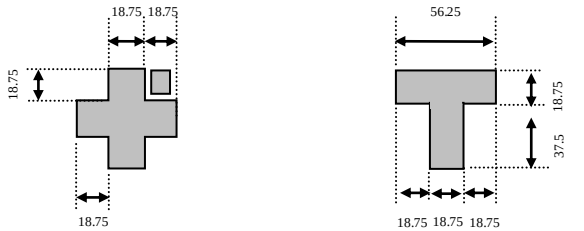


Figure 1-3: SSD1333Z alignment mark dimension



Center: (7379.5, 31.5)
Size: 56.25 x 56.25 μm²

Center: (-7379.5, 31.5)
Size: 56.25 x 56.25 μm²

Appendix II: SSD1333 Bump Die Pad Coordinates

Table 1 : SSD1333 Bump Die Pad Coordinates

Pin no.	Pin name	x	y	Pin no.	Pin name	x	y	Pin no.	Pin name	x	y
1	VLSS	-7365.5	-484	81	VLSS	-4632.5	-514.5	161	BS1	-427.5	-514.5
2	COM125	-7338.5	-484	82	VLSS	-4577.5	-514.5	162	VLH	-372.5	-514.5
3	COM126	-7311.5	-484	83	VLSS	-4522.5	-514.5	163	BS0	-317.5	-514.5
4	COM127	-7284.5	-484	84	VLSS	-4467.5	-514.5	164	VLL	-262.5	-514.5
5	COM128	-7257.5	-484	85	VLSS	-4412.5	-514.5	165	R/W#(WR#)	-207.5	-514.5
6	COM129	-7230.5	-484	86	NC	-4357.5	-514.5	166	E(RD#)	-152.5	-514.5
7	COM130	-7203.5	-484	87	VDD	-4302.5	-514.5	167	VLH	-97.5	-514.5
8	COM131	-7176.5	-484	88	VDD	-4247.5	-514.5	168	D_SEL	-42.5	-514.5
9	COM132	-7149.5	-484	89	VSS	-4192.5	-514.5	169	VLL	12.5	-514.5
10	COM133	-7122.5	-484	90	VSS	-4137.5	-514.5	170	VDD	67.5	-514.5
11	COM134	-7095.5	-484	91	NC	-4082.5	-514.5	171	VDD	122.5	-514.5
12	COM135	-7068.5	-484	92	VSL	-4027.5	-514.5	172	D0	177.5	-514.5
13	COM136	-7041.5	-484	93	VSL	-3972.5	-514.5	173	D1	232.5	-514.5
14	COM137	-7014.5	-484	94	VSL	-3917.5	-514.5	174	D2	287.5	-514.5
15	COM138	-6987.5	-484	95	VSL	-3862.5	-514.5	175	D3	342.5	-514.5
16	COM139	-6960.5	-484	96	VCOMH	-3807.5	-514.5	176	D4	397.5	-514.5
17	COM140	-6933.5	-484	97	VCOMH	-3752.5	-514.5	177	D5	452.5	-514.5
18	COM141	-6906.5	-484	98	VCOMH	-3697.5	-514.5	178	D6	507.5	-514.5
19	COM142	-6879.5	-484	99	VCOMH	-3642.5	-514.5	179	D7	562.5	-514.5
20	COM143	-6852.5	-484	100	VCOMH	-3587.5	-514.5	180	D8	617.5	-514.5
21	COM144	-6825.5	-484	101	VP	-3532.5	-514.5	181	D9	672.5	-514.5
22	COM145	-6798.5	-484	102	VP	-3477.5	-514.5	182	D10	727.5	-514.5
23	COM146	-6771.5	-484	103	VP	-3422.5	-514.5	183	D11	782.5	-514.5
24	COM147	-6744.5	-484	104	VP	-3367.5	-514.5	184	D12	837.5	-514.5
25	COM148	-6717.5	-484	105	VCC	-3312.5	-514.5	185	D13	892.5	-514.5
26	COM149	-6690.5	-484	106	VCC	-3257.5	-514.5	186	D14	947.5	-514.5
27	COM150	-6663.5	-484	107	VCC	-3202.5	-514.5	187	D15	1002.5	-514.5
28	COM151	-6636.5	-484	108	VCC	-3147.5	-514.5	188	VSS	1057.5	-514.5
29	COM152	-6609.5	-484	109	VCC	-3092.5	-514.5	189	VSS	1112.5	-514.5
30	COM153	-6582.5	-484	110	VCC	-3037.5	-514.5	190	VSS	1167.5	-514.5
31	COM154	-6555.5	-484	111	VCC	-2982.5	-514.5	191	VSS	1222.5	-514.5
32	COM155	-6528.5	-484	112	IREF	-2927.5	-514.5	192	VSS	1277.5	-514.5
33	COM156	-6501.5	-484	113	VSS	-2872.5	-514.5	193	VSS	1332.5	-514.5
34	COM157	-6474.5	-484	114	VSS	-2817.5	-514.5	194	VSS	1387.5	-514.5
35	COM158	-6447.5	-484	115	VSS	-2762.5	-514.5	195	VSS	1442.5	-514.5
36	COM159	-6420.5	-484	116	VSS	-2707.5	-514.5	196	VSS	1497.5	-514.5
37	COM160	-6393.5	-484	117	VSS	-2652.5	-514.5	197	VSS	1552.5	-514.5
38	COM161	-6366.5	-484	118	VSS	-2597.5	-514.5	198	VSS	1607.5	-514.5
39	COM162	-6339.5	-484	119	VSS	-2542.5	-514.5	199	VSS	1662.5	-514.5
40	COM163	-6312.5	-484	120	VSS	-2487.5	-514.5	200	VSS	1717.5	-514.5
41	COM164	-6285.5	-484	121	VSS	-2432.5	-514.5	201	VSS	1772.5	-514.5
42	COM165	-6258.5	-484	122	VSS	-2377.5	-514.5	202	VSS	1827.5	-514.5
43	COM166	-6231.5	-484	123	VSS	-2322.5	-514.5	203	VSS	1882.5	-514.5
44	COM167	-6204.5	-484	124	VSS	-2267.5	-514.5	204	VSS	1937.5	-514.5
45	COM168	-6177.5	-484	125	VSS	-2212.5	-514.5	205	VSS	1992.5	-514.5
46	COM169	-6150.5	-484	126	VSS	-2157.5	-514.5	206	VSS	2047.5	-514.5
47	COM170	-6123.5	-484	127	VSS	-2102.5	-514.5	207	VSS	2102.5	-514.5
48	COM171	-6096.5	-484	128	VSS	-2047.5	-514.5	208	VSS	2157.5	-514.5
49	COM172	-6069.5	-484	129	VSS	-1992.5	-514.5	209	VSS	2212.5	-514.5
50	COM173	-6042.5	-484	130	VSS	-1937.5	-514.5	210	VSS	2267.5	-514.5
51	COM174	-6015.5	-484	131	VSS	-1882.5	-514.5	211	VSS	2322.5	-514.5
52	COM175	-5988.5	-484	132	VSS	-1827.5	-514.5	212	VSS	2377.5	-514.5
53	VLSS	-5961.5	-484	133	VSS	-1772.5	-514.5	213	VSS	2432.5	-514.5
54	PT0	-5907.5	-514.5	134	VSS	-1727.5	-514.5	214	VSS	2487.5	-514.5
55	PT0	-5877.5	-514.5	135	TP5	-1697.5	-514.5	215	VSS	2542.5	-514.5
56	VSS	-5847.5	-514.5	136	TP6	-1667.5	-514.5	216	VSS	2597.5	-514.5
57	TP0	-5817.5	-514.5	137	TP7	-1637.5	-514.5	217	VSS	2652.5	-514.5
58	TP1	-5787.5	-514.5	138	TP8	-1607.5	-514.5	218	NC	2707.5	-514.5
59	TP2	-5757.5	-514.5	139	TP9	-1577.5	-514.5	219	VDD	2762.5	-514.5
60	TP3	-5727.5	-514.5	140	TP10	-1547.5	-514.5	220	VDD	2817.5	-514.5
61	TP4	-5697.5	-514.5	141	VSS	-1517.5	-514.5	221	VSS	2872.5	-514.5
62	VSS	-5667.5	-514.5	142	BGGND	-1472.5	-514.5	222	VSS	2927.5	-514.5
63	VLSS	-5622.5	-514.5	143	VBREF	-1417.5	-514.5	223	VCC	2982.5	-514.5
64	VLSS	-5567.5	-514.5	144	VDD	-1362.5	-514.5	224	VCC	3037.5	-514.5
65	VLSS	-5512.5	-514.5	145	VDD	-1307.5	-514.5	225	VCC	3092.5	-514.5
66	VLSS	-5457.5	-514.5	146	FR	-1252.5	-514.5	226	VCC	3147.5	-514.5
67	VLSS	-5402.5	-514.5	147	CL	-1197.5	-514.5	227	VCC	3202.5	-514.5
68	VLSS	-5347.5	-514.5	148	VLL	-1142.5	-514.5	228	VCC	3257.5	-514.5
69	VLSS	-5292.5	-514.5	149	RES#	-1087.5	-514.5	229	VCC	3312.5	-514.5
70	VLSS	-5237.5	-514.5	150	D/C	-1032.5	-514.5	230	VP	3367.5	-514.5
71	VLSS	-5182.5	-514.5	151	CS#	-977.5	-514.5	231	VP	3422.5	-514.5
72	VLSS	-5127.5	-514.5	152	VLL	-922.5	-514.5	232	VP	3477.5	-514.5
73	VLSS	-5072.5	-514.5	153	CLS	-867.5	-514.5	233	VP	3532.5	-514.5
74	VLSS	-5017.5	-514.5	154	VLH	-812.5	-514.5	234	VCOMH	3587.5	-514.5
75	VLSS	-4962.5	-514.5	155	T1	-757.5	-514.5	235	VCOMH	3642.5	-514.5
76	VLSS	-4907.5	-514.5	156	VLL	-702.5	-514.5	236	VCOMH	3697.5	-514.5
77	VLSS	-4852.5	-514.5	157	T0	-647.5	-514.5	237	VCOMH	3752.5	-514.5
78	VLSS	-4797.5	-514.5	158	VLH	-592.5	-514.5	238	VCOMH	3807.5	-514.5
79	VLSS	-4742.5	-514.5	159	BS2	-537.5	-514.5	239	VSL	3862.5	-514.5
80	VLSS	-4687.5	-514.5	160	VLL	-482.5	-514.5	240	VSL	3917.5	-514.5

Pin no.	Pin name	x	y
241	VSL	3972.5	-514.5
242	VSL	4027.5	-514.5
243	NC	4082.5	-514.5
244	VDD	4137.5	-514.5
245	VDD	4192.5	-514.5
246	VSS	4247.5	-514.5
247	VSS	4302.5	-514.5
248	NC	4357.5	-514.5
249	VLSS	4412.5	-514.5
250	VLSS	4467.5	-514.5
251	VLSS	4522.5	-514.5
252	VLSS	4577.5	-514.5
253	VLSS	4632.5	-514.5
254	VLSS	4687.5	-514.5
255	VLSS	4742.5	-514.5
256	VLSS	4797.5	-514.5
257	VLSS	4852.5	-514.5
258	VLSS	4907.5	-514.5
259	VLSS	4962.5	-514.5
260	VLSS	5017.5	-514.5
261	VLSS	5072.5	-514.5
262	VLSS	5127.5	-514.5
263	VLSS	5182.5	-514.5
264	VLSS	5237.5	-514.5
265	VLSS	5292.5	-514.5
266	VLSS	5347.5	-514.5
267	VLSS	5402.5	-514.5
268	VLSS	5457.5	-514.5
269	VLSS	5512.5	-514.5
270	VLSS	5567.5	-514.5
271	VLSS	5622.5	-514.5
272	VSS	5667.5	-514.5
273	TP11	5697.5	-514.5
274	TP12	5727.5	-514.5
275	TP13	5757.5	-514.5
276	TP14	5787.5	-514.5
277	TP15	5817.5	-514.5
278	VSS	5847.5	-514.5
279	PT1	5877.5	-514.5
280	PT1	5907.5	-514.5
281	VLSS	5961.5	-484
282	COM87	5988.5	-484
283	COM86	6015.5	-484
284	COM85	6042.5	-484
285	COM84	6069.5	-484
286	COM83	6096.5	-484
287	COM82	6123.5	-484
288	COM81	6150.5	-484
289	COM80	6177.5	-484
290	COM79	6204.5	-484
291	COM78	6231.5	-484
292	COM77	6258.5	-484
293	COM76	6285.5	-484
294	COM75	6312.5	-484
295	COM74	6339.5	-484
296	COM73	6366.5	-484
297	COM72	6393.5	-484
298	COM71	6420.5	-484
299	COM70	6447.5	-484
300	COM69	6474.5	-484
301	COM68	6501.5	-484
302	COM67	6528.5	-484
303	COM66	6555.5	-484
304	COM65	6582.5	-484
305	COM64	6609.5	-484
306	COM63	6636.5	-484
307	COM62	6663.5	-484
308	COM61	6690.5	-484
309	COM60	6717.5	-484
310	COM59	6744.5	-484
311	COM58	6771.5	-484
312	COM57	6798.5	-484
313	COM56	6825.5	-484
314	COM55	6852.5	-484
315	COM54	6879.5	-484
316	COM53	6906.5	-484
317	COM52	6933.5	-484
318	COM51	6960.5	-484
319	COM50	6987.5	-484
320	COM49	7014.5	-484
321	COM48	7041.5	-484
322	COM47	7068.5	-484
323	COM46	7095.5	-484
324	COM45	7122.5	-484
325	COM44	7149.5	-484
326	COM43	7176.5	-484
327	COM42	7203.5	-484
328	COM41	7230.5	-484
329	COM40	7257.5	-484
330	COM39	7284.5	-484
331	COM38	7311.5	-484
332	COM37	7338.5	-484
333	VLSS	7365.5	-484
334	NC	7624	-465.5
335	COM36	7624	-438.5
336	COM35	7624	-411.5
337	COM34	7624	-384.5
338	COM33	7624	-357.5
339	COM32	7624	-330.5
340	COM31	7624	-303.5
341	COM30	7624	-276.5
342	COM29	7624	-249.5
343	COM28	7624	-222.5
344	COM27	7624	-195.5
345	COM26	7624	-168.5
346	COM25	7624	-141.5
347	COM24	7624	-114.5
348	COM23	7624	-87.5
349	COM22	7624	-60.5
350	COM21	7624	-33.5
351	COM20	7624	-6.5
352	COM19	7624	20.5
353	COM18	7624	47.5
354	COM17	7624	74.5
355	COM16	7624	101.5
356	COM15	7624	128.5
357	COM14	7624	155.5
358	COM13	7624	182.5
359	COM12	7624	209.5
360	COM11	7624	236.5
361	COM10	7624	263.5
362	COM9	7624	290.5
363	COM8	7624	317.5
364	COM7	7624	344.5
365	COM6	7624	371.5
366	COM5	7624	398.5
367	COM4	7624	425.5
368	COM3	7624	452.5
369	COM2	7624	479.5
370	COM1	7624	506.5
371	COM0	7624	533.5
372	V33	7624	560.5
373	V33	7316.5	522
374	SEGA0	7289.5	522
375	SEGB0	7262.5	522
376	SEGC0	7235.5	522
377	SEGA1	7208.5	522
378	SEGB1	7181.5	522
379	SEGC1	7154.5	522
380	SEGA2	7127.5	522
381	SEGB2	7100.5	522
382	SEGC2	7073.5	522
383	SEGA3	7046.5	522
384	SEGB3	7019.5	522
385	SEGC3	6992.5	522
386	SEGA4	6965.5	522
387	SEGB4	6938.5	522
388	SEGC4	6911.5	522
389	SEGA5	6884.5	522
390	SEGB5	6857.5	522
391	SEGC5	6830.5	522
392	SEGA6	6803.5	522
393	SEGB6	6776.5	522
394	SEGC6	6749.5	522
395	SEGA7	6722.5	522
396	SEGB7	6695.5	522
397	SEGC7	6668.5	522
398	SEGA8	6641.5	522
399	SEGB8	6614.5	522
400	SEGC8	6587.5	522
401	SEGA9	6560.5	522
402	SEGB9	6533.5	522
403	SEGC9	6506.5	522
404	SEGA10	6479.5	522
405	SEGB10	6452.5	522
406	SEGC10	6425.5	522
407	SEGA11	6398.5	522
408	SEGB11	6371.5	522
409	SEGC11	6344.5	522
410	SEGA12	6317.5	522
411	SEGB12	6290.5	522
412	SEGC12	6263.5	522
413	SEGA13	6236.5	522
414	SEGB13	6209.5	522
415	SEGC13	6182.5	522
416	SEGA14	6155.5	522
417	SEGB14	6128.5	522
418	SEGC14	6101.5	522
419	SEGA15	6074.5	522
420	SEGB15	6047.5	522
421	SEGC15	6020.5	522
422	SEGA16	5993.5	522
423	SEGB16	5966.5	522
424	SEGC16	5939.5	522
425	SEGA17	5912.5	522
426	SEGB17	5885.5	522
427	SEGC17	5858.5	522
428	SEGA18	5831.5	522
429	SEGB18	5804.5	522
430	SEGC18	5777.5	522
431	SEGA19	5750.5	522
432	SEGB19	5723.5	522
433	SEGC19	5696.5	522
434	SEGA20	5669.5	522
435	SEGB20	5642.5	522
436	SEGC20	5615.5	522
437	SEGA21	5588.5	522
438	SEGB21	5561.5	522
439	SEGC21	5534.5	522
440	SEGA22	5507.5	522
441	SEGB22	5480.5	522
442	SEGC22	5453.5	522
443	SEGA23	5426.5	522
444	SEGB23	5399.5	522
445	SEGC23	5372.5	522
446	SEGA24	5345.5	522
447	SEGB24	5318.5	522
448	SEGC24	5291.5	522
449	SEGA25	5264.5	522
450	SEGB25	5237.5	522
451	SEGC25	5210.5	522
452	SEGA26	5183.5	522
453	SEGB26	5156.5	522
454	SEGC26	5129.5	522
455	SEGA27	5102.5	522
456	SEGB27	5075.5	522
457	SEGC27	5048.5	522
458	SEGA28	5021.5	522
459	SEGB28	4994.5	522
460	SEGC28	4967.5	522
461	SEGA29	4940.5	522
462	SEGB29	4913.5	522
463	SEGC29	4886.5	522
464	SEGA30	4859.5	522
465	SEGB30	4832.5	522
466	SEGC30	4805.5	522
467	SEGA31	4778.5	522
468	SEGB31	4751.5	522
469	SEGC31	4724.5	522
470	SEGA32	4697.5	522
471	SEGB32	4670.5	522
472	SEGC32	4643.5	522
473	SEGA33	4616.5	522
474	SEGB33	4589.5	522
475	SEGC33	4562.5	522
476	SEGA34	4535.5	522
477	SEGB34	4508.5	522
478	SEGC34	4481.5	522
479	SEGA35	4454.5	522
480	SEGB35	4427.5	522

Pin no.	Pin name	x	y
481	SEGC35	4400.5	522
482	SEGA36	4373.5	522
483	SEGB36	4346.5	522
484	SEGC36	4319.5	522
485	SEGA37	4292.5	522
486	SEGB37	4265.5	522
487	SEGC37	4238.5	522
488	SEGA38	4211.5	522
489	SEGB38	4184.5	522
490	SEGC38	4157.5	522
491	SEGA39	4130.5	522
492	SEGB39	4103.5	522
493	SEGC39	4076.5	522
494	SEGA40	4049.5	522
495	SEGB40	4022.5	522
496	SEGC40	3995.5	522
497	SEGA41	3968.5	522
498	SEGB41	3941.5	522
499	SEGC41	3914.5	522
500	SEGA42	3887.5	522
501	SEGB42	3860.5	522
502	SEGC42	3833.5	522
503	SEGA43	3806.5	522
504	SEGB43	3779.5	522
505	SEGC43	3752.5	522
506	SEGA44	3725.5	522
507	SEGB44	3698.5	522
508	SEGC44	3671.5	522
509	SEGA45	3644.5	522
510	SEGB45	3617.5	522
511	SEGC45	3590.5	522
512	SEGA46	3563.5	522
513	SEGB46	3536.5	522
514	SEGC46	3509.5	522
515	SEGA47	3482.5	522
516	SEGB47	3455.5	522
517	SEGC47	3428.5	522
518	NC	3401.5	522
519	NC	3253.5	522
520	SEGA48	3226.5	522
521	SEGB48	3199.5	522
522	SEGC48	3172.5	522
523	SEGA49	3145.5	522
524	SEGB49	3118.5	522
525	SEGC49	3091.5	522
526	SEGA50	3064.5	522
527	SEGB50	3037.5	522
528	SEGC50	3010.5	522
529	SEGA51	2983.5	522
530	SEGB51	2956.5	522
531	SEGC51	2929.5	522
532	SEGA52	2902.5	522
533	SEGB52	2875.5	522
534	SEGC52	2848.5	522
535	SEGA53	2821.5	522
536	SEGB53	2794.5	522
537	SEGC53	2767.5	522
538	SEGA54	2740.5	522
539	SEGB54	2713.5	522
540	SEGC54	2686.5	522
541	SEGA55	2659.5	522
542	SEGB55	2632.5	522
543	SEGC55	2605.5	522
544	SEGA56	2578.5	522
545	SEGB56	2551.5	522
546	SEGC56	2524.5	522
547	SEGA57	2497.5	522
548	SEGB57	2470.5	522
549	SEGC57	2443.5	522
550	SEGA58	2416.5	522
551	SEGB58	2389.5	522
552	SEGC58	2362.5	522
553	SEGA59	2335.5	522
554	SEGB59	2308.5	522
555	SEGC59	2281.5	522
556	SEGA60	2254.5	522
557	SEGB60	2227.5	522
558	SEGC60	2200.5	522
559	SEGA61	2173.5	522
560	SEGB61	2146.5	522

Pin no.	Pin name	x	y
561	SEGC61	2119.5	522
562	SEGA62	2092.5	522
563	SEGB62	2065.5	522
564	SEGC62	2038.5	522
565	SEGA63	2011.5	522
566	SEGB63	1984.5	522
567	SEGC63	1957.5	522
568	SEGA64	1930.5	522
569	SEGB64	1903.5	522
570	SEGC64	1876.5	522
571	SEGA65	1849.5	522
572	SEGB65	1822.5	522
573	SEGC65	1795.5	522
574	SEGA66	1768.5	522
575	SEGB66	1741.5	522
576	SEGC66	1714.5	522
577	SEGA67	1687.5	522
578	SEGB67	1660.5	522
579	SEGC67	1633.5	522
580	SEGA68	1606.5	522
581	SEGB68	1579.5	522
582	SEGC68	1552.5	522
583	SEGA69	1525.5	522
584	SEGB69	1498.5	522
585	SEGC69	1471.5	522
586	SEGA70	1444.5	522
587	SEGB70	1417.5	522
588	SEGC70	1390.5	522
589	SEGA71	1363.5	522
590	SEGB71	1336.5	522
591	SEGC71	1309.5	522
592	SEGA72	1282.5	522
593	SEGB72	1255.5	522
594	SEGC72	1228.5	522
595	SEGA73	1201.5	522
596	SEGB73	1174.5	522
597	SEGC73	1147.5	522
598	SEGA74	1120.5	522
599	SEGB74	1093.5	522
600	SEGC74	1066.5	522
601	SEGA75	1039.5	522
602	SEGB75	1012.5	522
603	SEGC75	985.5	522
604	SEGA76	958.5	522
605	SEGB76	931.5	522
606	SEGC76	904.5	522
607	SEGA77	877.5	522
608	SEGB77	850.5	522
609	SEGC77	823.5	522
610	SEGA78	796.5	522
611	SEGB78	769.5	522
612	SEGC78	742.5	522
613	SEGA79	715.5	522
614	SEGB79	688.5	522
615	SEGC79	661.5	522
616	SEGA80	634.5	522
617	SEGB80	607.5	522
618	SEGC80	580.5	522
619	SEGA81	553.5	522
620	SEGB81	526.5	522
621	SEGC81	499.5	522
622	SEGA82	472.5	522
623	SEGB82	445.5	522
624	SEGC82	418.5	522
625	SEGA83	391.5	522
626	SEGB83	364.5	522
627	SEGC83	337.5	522
628	SEGA84	310.5	522
629	SEGB84	283.5	522
630	SEGC84	256.5	522
631	SEGA85	229.5	522
632	SEGB85	202.5	522
633	SEGC85	175.5	522
634	SEGA86	148.5	522
635	SEGB86	121.5	522
636	SEGC86	94.5	522
637	SEGA87	67.5	522
638	SEGB87	40.5	522
639	SEGC87	13.5	522
640	SEGA88	-13.5	522

Pin no.	Pin name	x	y
641	SEGB88	-40.5	522
642	SEGC88	-67.5	522
643	SEGA89	-94.5	522
644	SEGB89	-121.5	522
645	SEGC89	-148.5	522
646	SEGA90	-175.5	522
647	SEGB90	-202.5	522
648	SEGC90	-229.5	522
649	SEGA91	-256.5	522
650	SEGB91	-283.5	522
651	SEGC91	-310.5	522
652	SEGA92	-337.5	522
653	SEGB92	-364.5	522
654	SEGC92	-391.5	522
655	SEGA93	-418.5	522
656	SEGB93	-445.5	522
657	SEGC93	-472.5	522
658	SEGA94	-499.5	522
659	SEGB94	-526.5	522
660	SEGC94	-553.5	522
661	SEGA95	-580.5	522
662	SEGB95	-607.5	522
663	SEGC95	-634.5	522
664	SEGA96	-661.5	522
665	SEGB96	-688.5	522
666	SEGC96	-715.5	522
667	SEGA97	-742.5	522
668	SEGB97	-769.5	522
669	SEGC97	-796.5	522
670	SEGA98	-823.5	522
671	SEGB98	-850.5	522
672	SEGC98	-877.5	522
673	SEGA99	-904.5	522
674	SEGB99	-931.5	522
675	SEGC99	-958.5	522
676	SEGA100	-985.5	522
677	SEGB100	-1012.5	522
678	SEGC100	-1039.5	522
679	SEGA101	-1066.5	522
680	SEGB101	-1093.5	522
681	SEGC101	-1120.5	522
682	SEGA102	-1147.5	522
683	SEGB102	-1174.5	522
684	SEGC102	-1201.5	522
685	SEGA103	-1228.5	522
686	SEGB103	-1255.5	522
687	SEGC103	-1282.5	522
688	SEGA104	-1309.5	522
689	SEGB104	-1336.5	522
690	SEGC104	-1363.5	522
691	SEGA105	-1390.5	522
692	SEGB105	-1417.5	522
693	SEGC105	-1444.5	522
694	SEGA106	-1471.5	522
695	SEGB106	-1498.5	522
696	SEGC106	-1525.5	522
697	SEGA107	-1552.5	522
698	SEGB107	-1579.5	522
699	SEGC107	-1606.5	522
700	SEGA108	-1633.5	522
701	SEGB108	-1660.5	522
702	SEGC108	-1687.5	522
703	SEGA109	-1714.5	522
704	SEGB109	-1741.5	522
705	SEGC109	-1768.5	522
706	SEGA110	-1795.5	522
707	SEGB110	-1822.5	522
708	SEGC110	-1849.5	522
709	SEGA111	-1876.5	522
710	SEGB111	-1903.5	522
711	SEGC111	-1930.5	522
712	SEGA112	-1957.5	522
713	SEGB112	-1984.5	522
714	SEGC112	-2011.5	522
715	SEGA113	-2038.5	522
716	SEGB113	-2065.5	522
717	SEGC113	-2092.5	522
718	SEGA114	-2119.5	522
719	SEGB114	-2146.5	522
720	SEGC114	-2173.5	522

Pin no.	Pin name	x	y
721	SEGA115	-2200.5	522
722	SEGB115	-2227.5	522
723	SEGC115	-2254.5	522
724	SEGA116	-2281.5	522
725	SEGB116	-2308.5	522
726	SEGC116	-2335.5	522
727	SEGA117	-2362.5	522
728	SEGB117	-2389.5	522
729	SEGC117	-2416.5	522
730	SEGA118	-2443.5	522
731	SEGB118	-2470.5	522
732	SEGC118	-2497.5	522
733	SEGA119	-2524.5	522
734	SEGB119	-2551.5	522
735	SEGC119	-2578.5	522
736	SEGA120	-2605.5	522
737	SEGB120	-2632.5	522
738	SEGC120	-2659.5	522
739	SEGA121	-2686.5	522
740	SEGB121	-2713.5	522
741	SEGC121	-2740.5	522
742	SEGA122	-2767.5	522
743	SEGB122	-2794.5	522
744	SEGC122	-2821.5	522
745	SEGA123	-2848.5	522
746	SEGB123	-2875.5	522
747	SEGC123	-2902.5	522
748	SEGA124	-2929.5	522
749	SEGB124	-2956.5	522
750	SEGC124	-2983.5	522
751	SEGA125	-3010.5	522
752	SEGB125	-3037.5	522
753	SEGC125	-3064.5	522
754	SEGA126	-3091.5	522
755	SEGB126	-3118.5	522
756	SEGC126	-3145.5	522
757	SEGA127	-3172.5	522
758	SEGB127	-3199.5	522
759	SEGC127	-3226.5	522
760	NC	-3253.5	522
761	NC	-3401.5	522
762	SEGA128	-3428.5	522
763	SEGB128	-3455.5	522
764	SEGC128	-3482.5	522
765	SEGA129	-3509.5	522
766	SEGB129	-3536.5	522
767	SEGC129	-3563.5	522
768	SEGA130	-3590.5	522
769	SEGB130	-3617.5	522
770	SEGC130	-3644.5	522
771	SEGA131	-3671.5	522
772	SEGB131	-3698.5	522
773	SEGC131	-3725.5	522
774	SEGA132	-3752.5	522
775	SEGB132	-3779.5	522
776	SEGC132	-3806.5	522
777	SEGA133	-3833.5	522
778	SEGB133	-3860.5	522
779	SEGC133	-3887.5	522
780	SEGA134	-3914.5	522
781	SEGB134	-3941.5	522
782	SEGC134	-3968.5	522
783	SEGA135	-3995.5	522
784	SEGB135	-4022.5	522
785	SEGC135	-4049.5	522
786	SEGA136	-4076.5	522
787	SEGB136	-4103.5	522
788	SEGC136	-4130.5	522
789	SEGA137	-4157.5	522
790	SEGB137	-4184.5	522
791	SEGC137	-4211.5	522
792	SEGA138	-4238.5	522
793	SEGB138	-4265.5	522
794	SEGC138	-4292.5	522
795	SEGA139	-4319.5	522
796	SEGB139	-4346.5	522
797	SEGC139	-4373.5	522
798	SEGA140	-4400.5	522
799	SEGB140	-4427.5	522
800	SEGC140	-4454.5	522

Pin no.	Pin name	x	y
801	SEGA141	-4481.5	522
802	SEGB141	-4508.5	522
803	SEGC141	-4535.5	522
804	SEGA142	-4562.5	522
805	SEGB142	-4589.5	522
806	SEGC142	-4616.5	522
807	SEGA143	-4643.5	522
808	SEGB143	-4670.5	522
809	SEGC143	-4697.5	522
810	SEGA144	-4724.5	522
811	SEGB144	-4751.5	522
812	SEGC144	-4778.5	522
813	SEGA145	-4805.5	522
814	SEGB145	-4832.5	522
815	SEGC145	-4859.5	522
816	SEGA146	-4886.5	522
817	SEGB146	-4913.5	522
818	SEGC146	-4940.5	522
819	SEGA147	-4967.5	522
820	SEGB147	-4994.5	522
821	SEGC147	-5021.5	522
822	SEGA148	-5048.5	522
823	SEGB148	-5075.5	522
824	SEGC148	-5102.5	522
825	SEGA149	-5129.5	522
826	SEGB149	-5156.5	522
827	SEGC149	-5183.5	522
828	SEGA150	-5210.5	522
829	SEGB150	-5237.5	522
830	SEGC150	-5264.5	522
831	SEGA151	-5291.5	522
832	SEGB151	-5318.5	522
833	SEGC151	-5345.5	522
834	SEGA152	-5372.5	522
835	SEGB152	-5399.5	522
836	SEGC152	-5426.5	522
837	SEGA153	-5453.5	522
838	SEGB153	-5480.5	522
839	SEGC153	-5507.5	522
840	SEGA154	-5534.5	522
841	SEGB154	-5561.5	522
842	SEGC154	-5588.5	522
843	SEGA155	-5615.5	522
844	SEGB155	-5642.5	522
845	SEGC155	-5669.5	522
846	SEGA156	-5696.5	522
847	SEGB156	-5723.5	522
848	SEGC156	-5750.5	522
849	SEGA157	-5777.5	522
850	SEGB157	-5804.5	522
851	SEGC157	-5831.5	522
852	SEGA158	-5858.5	522
853	SEGB158	-5885.5	522
854	SEGC158	-5912.5	522
855	SEGA159	-5939.5	522
856	SEGB159	-5966.5	522
857	SEGC159	-5993.5	522
858	SEGA160	-6020.5	522
859	SEGB160	-6047.5	522
860	SEGC160	-6074.5	522
861	SEGA161	-6101.5	522
862	SEGB161	-6128.5	522
863	SEGC161	-6155.5	522
864	SEGA162	-6182.5	522
865	SEGB162	-6209.5	522
866	SEGC162	-6236.5	522
867	SEGA163	-6263.5	522
868	SEGB163	-6290.5	522
869	SEGC163	-6317.5	522
870	SEGA164	-6344.5	522
871	SEGB164	-6371.5	522
872	SEGC164	-6398.5	522
873	SEGA165	-6425.5	522
874	SEGB165	-6452.5	522
875	SEGC165	-6479.5	522
876	SEGA166	-6506.5	522
877	SEGB166	-6533.5	522
878	SEGC166	-6560.5	522
879	SEGA167	-6587.5	522
880	SEGB167	-6614.5	522

Pin no.	Pin name	x	y
881	SEGC167	-6641.5	522
882	SEGA168	-6668.5	522
883	SEGB168	-6695.5	522
884	SEGC168	-6722.5	522
885	SEGA169	-6749.5	522
886	SEGB169	-6776.5	522
887	SEGC169	-6803.5	522
888	SEGA170	-6830.5	522
889	SEGB170	-6857.5	522
890	SEGC170	-6884.5	522
891	SEGA171	-6911.5	522
892	SEGB171	-6938.5	522
893	SEGC171	-6965.5	522
894	SEGA172	-6992.5	522
895	SEGB172	-7019.5	522
896	SEGC172	-7046.5	522
897	SEGA173	-7073.5	522
898	SEGB173	-7100.5	522
899	SEGC173	-7127.5	522
900	SEGA174	-7154.5	522
901	SEGB174	-7181.5	522
902	SEGC174	-7208.5	522
903	SEGA175	-7235.5	522
904	SEGB175	-7262.5	522
905	SEGC175	-7289.5	522
906	V33	-7316.5	522
907	V33	-7624	560.5
908	COM88	-7624	533.5
909	COM89	-7624	506.5
910	COM90	-7624	479.5
911	COM91	-7624	452.5
912	COM92	-7624	425.5
913	COM93	-7624	398.5
914	COM94	-7624	371.5
915	COM95	-7624	344.5
916	COM96	-7624	317.5
917	COM97	-7624	290.5
918	COM98	-7624	263.5
919	COM99	-7624	236.5
920	COM100	-7624	209.5
921	COM101	-7624	182.5
922	COM102	-7624	155.5
923	COM103	-7624	128.5
924	COM104	-7624	101.5
925	COM105	-7624	74.5
926	COM106	-7624	47.5
927	COM107	-7624	20.5
928	COM108	-7624	-6.5
929	COM109	-7624	-33.5
930	COM110	-7624	-60.5
931	COM111	-7624	-87.5
932	COM112	-7624	-114.5
933	COM113	-7624	-141.5
934	COM114	-7624	-168.5
935	COM115	-7624	-195.5
936	COM116	-7624	-222.5
937	COM117	-7624	-249.5
938	COM118	-7624	-276.5
939	COM119	-7624	-303.5
940	COM120	-7624	-330.5
941	COM121	-7624	-357.5
942	COM122	-7624	-384.5
943	COM123	-7624	-411.5
944	COM124	-7624	-438.5
945	NC	-7624	-465.5

Appendix III: SSD1333 Command Table

1 COMMAND TABLE

Table 1-1: SSD1333 Command Table

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	15	0	0	0	1	0	1	0	1	Set Column Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=175d] Ranges from 0 to 175
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	75	0	1	1	1	0	1	0	1	Set Row Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=175d] Ranges from 0 to 175
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0	A0	1	0	1	0	0	0	0	0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 175 is mapped to SEG0 A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A A[3]=0b, Reserved [reset] A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] A[7:6] Set Color Depth, 00b: 256color 01b: 65k color [reset] 10b: 262k color 11b Pseudo 262k color, 16-bit format 2 Refer to Product Preview Table 6-7 for details
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~175. [reset=00h]
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-175. [reset=00h]
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 2~30 DCLK(s) clocks [reset=0100b] A[3:0]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 = 30DCLKs A[7:4] Phase 2 period of 2~30 DCLK(s) clocks [reset=1000b] A[7:4]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 =30DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0000b], divide by DIVSET where A[7:4] Oscillator frequency, frequency increases as level increases [reset=1001b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[3:0]	DIVSET
0000	divide by 1
0001	divide by 2
0010	divide by 4
0011	divide by 8
0100	divide by 16
0101	divide by 32
0110	divide by 64
0111	divide by 128
1000	divide by 256
>=1001	invalid

0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS .... 1000 8 DCLKS [reset] .... 1111 15 DCLKS
1	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		
0	B8	1	0	1	1	1	0	0	0	Master Look Up Table for Gray Scale Pulse width (Color A,B,C)	The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d). A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A62[7:0]: Gamma Setting for GS62, A63[7:0]: Gamma Setting for GS63 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS62 < Setting of GS63 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input only, color A, B, C will follow the master LUT. (5) When command BCh is input, it selects individual LUT for color A, GS1~31A; When command BDh is input, it selects individual LUT for color C, GS1~31C (6) To select individual LUT for color B, A and C, command B8h should be input before command BCh and BDh,
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A62[7:0]	$A62_7$	$A62_6$	$A62_5$	$A62_4$	$A62_3$	$A62_2$	$A62_1$	$A62_0$		
1	A63[7:0]	$A63_7$	$A63_6$	$A63_5$	$A63_4$	$A63_3$	$A63_2$	$A63_1$	$A63_0$		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: **Color A**: GS1A = 0 DCLK; GS2A = 4 DCLK; GS3A = 8 DCLK; ... ; GS31A = 120 DCLK **Color B**: GS1B = 0 DCLK; GS2B = 2 DCLK; GS3B = 4 DCLK; ... ; GS62B = 122 DCLK; GS63B = 124 DCLK **Color C**: GS1C = 0 DCLK; GS2C = 4 DCLK; GS3C = 8 DCLK; ... ; GS31C = 120 DCLK
0 1	BB A[4:0]	1 0	0 0	1 0	1 A_4	1 A_3	0 A_2	1 A_1	1 A_0	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 01111b] A[4:0] / Hex code / pre-charge voltage: 00000 / 00h / 0.10 x V_{CC} : / : / : 10111 / 17h / 0.40 x V_{CC} [reset] : / : / : 11111 / 1Fh / 0.5133 x V_{CC} **Note** (1)Pre-charge voltage level must be smaller than COM deselect voltage level
0 1 1 1 1 1 1 1	BC A1[7:0] A2[7:0] . . . A30[7:0] A31[7:0]	1 $A1_7$ $A2_7$ . . . $A30_7$ $A31_7$	0 $A1_6$ $A2_6$ . . . $A30_6$ $A31_6$	1 $A1_5$ $A2_5$ . . . $A30_5$ $A31_5$	1 $A1_4$ $A2_4$ . . . $A30_4$ $A31_4$	1 $A1_3$ $A2_3$ . . . $A30_3$ $A31_3$	1 $A1_2$ $A2_2$ . . . $A30_2$ $A31_2$	0 $A1_1$ $A2_1$ . . . $A30_1$ $A31_1$	0 $A1_0$ $A2_0$ . . . $A30_0$ $A31_0$	Individual Look Up Table for Gray Scale Pulse width (Color A)	The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color A. A1[7:0]: Gamma Setting for GS1A, A2[7:0]: Gamma Setting for GS2A, : A30[7:0]: Gamma Setting for GS30A, A31[7:0]: Gamma Setting for GS31A **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for color A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BD	1	0	1	1	1	1	0	1	Individual Look Up Table for Gray Scale Pulse width (Color C)	The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color C. A1[7:0]: Gamma Setting for GS1C, A2[7:0]: Gamma Setting for GS2C, : A30[7:0]: Gamma Setting for GS30C, A31[7:0]: Gamma Setting for GS31C **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for color A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A30[7:0]	$A30_7$	$A30_6$	$A30_5$	$A30_4$	$A30_3$	$A30_2$	$A30_1$	$A30_0$		
1	A31[7:0]	$A31_7$	$A31_6$	$A31_5$	$A31_4$	$A31_3$	$A31_2$	$A31_1$	$A31_0$		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Set COM deselect voltage level [reset = 05h] **A[2:0] / Hex code / V_{COMH}** 000 / 00h / 0.72 x V_{CC} : / : / : 101 / 05h / 0.82 x V_{CC} [reset] : / : / : 111 / 07h / 0.86 x V_{CC}
1	A[2:0]	0	0	0	0	0	A_2	A_1	A_0		
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=7Fh] B[7:0] Contrast Value Color B [reset=7Fh] C[7:0] Contrast Value Color C [reset=7Fh]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] : 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset]
1	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0] MUX ratio 4MUX ~ 176MUX, [reset=175] (Ranges from 3 to 175)
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1	FD A[7:0]	1 A_7	1 A_6	1 A_5	1 A_4	1 A_3	1 A_2	0 A_1	1 A_0	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12h, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16h, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Note
(1) "*" stands for "Don't care".

Appendix IV: SSD1333 Command Description

1 COMMAND DESCRIPTION

1.1 Set Column Address (15h)

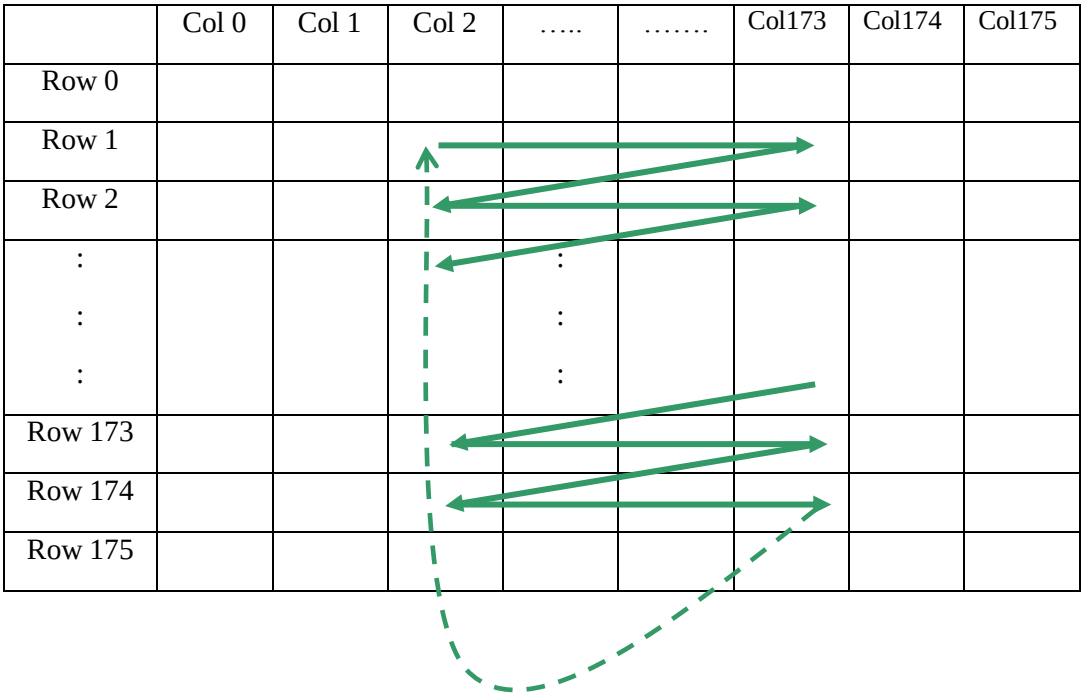
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

For example, column start address is set to 2 and column end address is set to 173, row start address is set to 1 and row end address is set to 174. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 2 to column 173 and from row 1 to row 174 only. In addition, the column address pointer is set to 2 and row address pointer is set to 1. After finishing read/write one pixel of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation(*solid line in Figure 1-1*). Whenever the column address pointer finishes accessing the end column 173, it is reset back to column 2 and row address is automatically increased by 1(*solid line in Figure 1-1*). While the end row 174 and end column 173 RAM location is accessed, the row address is reset back to 1 and the column address is reset back to 2(*dotted line in Figure 1-1*).

Figure 1-1 : Example of Column and Row Address Pointer Movement



1.3 Write RAM Command (5Ch)

After entering this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

1.4 Read RAM Command (5Dh)

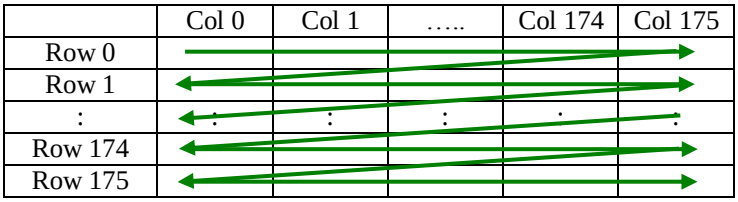
After entering this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

1.5 Set Re-map / Color Depth (A0h)

This command has multiple configurations and each bit setting is described as follows:

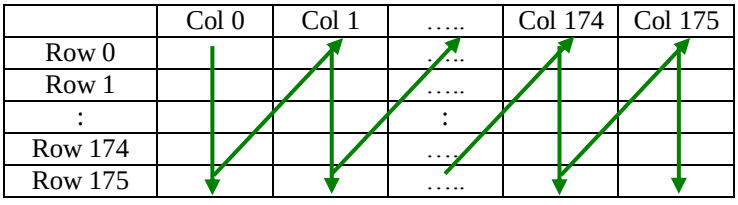
- Address increment mode (A[0])
  When A[0] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 1-2.

Figure 1-2 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 1-3.

Figure 1-3: Address Pointer Movement of Vertical Address Increment Mode



- Column Address Remap (A[1])
  This command bit is made for increasing the layout flexibility of segment signals in OLED module with segment arranged from left to right (when A[1] is set to 0) or vice versa (when A[1] is set to 1), as demonstrated in Figure 1-4.

A[1] = 0 (reset): RAM Column 0 ~ 175 maps to Col0~Col175
A[1] = 1: RAM Column 0 ~ 175 maps to Col175~Col0

- Color Remap (A[2])
  A[2] = 0 (reset): color sequence A → B → C
  A[2] = 1: color sequence C → B → A

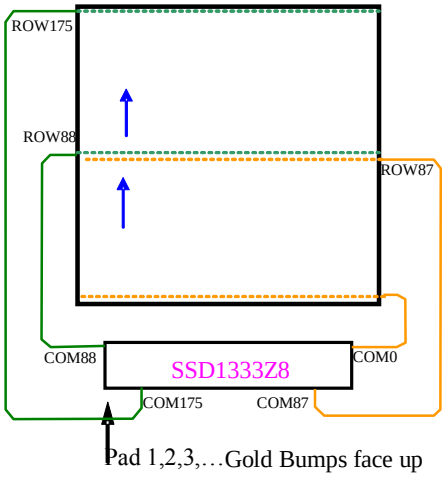
- COM scan direction Remap (A[4])
  This command bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
  A[4] = 0 (reset): COM scan from 0 to 175
  A[4] = 1: COM scan from 175 to 0
  Details of pin arrangement can be found in Figure 1-4.

- Odd even split of COM pins (A[5])
  This command bit can set the odd even arrangement of COM pins.
  A[5] = 0 (reset): Disable COM split odd even, pin assignment of common is in sequential as
  COM175 COM174...COM 89 COM88...SEG527...SEG0...COM0 COM1...COM86 COM87
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM175 COM173...COM3 COM1...SEG527...SEG0...COM0 COM2...COM172 COM174
  Details of pin arrangement can be found in Figure 1-4.

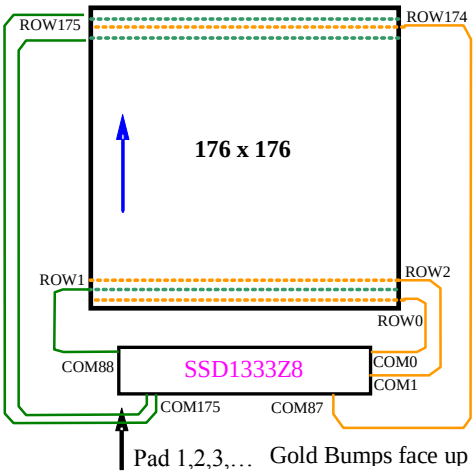
- Display color mode (A[7:6])
  Select either 262k, 65k or 256 color mode.

Figure 1-4 : COM Pins Hardware Configuration (MUX ratio: 176)

A[5] =0	A[3]=0	A[4]=0
Disable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM0 to COM175



A[5] =1	A[3]=0	A[4]=0
Enable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM0 to COM175



1.6 Set Display Start Line (A1h)

This command is used to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 175. Figure 1-5 shows an example of using this command when MUX ratio = 176 and MUX ratio = 148 and Display Start Line = 28. In there, "Row" means the graphic display data RAM row.

Figure 1-5 : Example of Set Display Start Line with no Remap

	176	176	148	148	MUX ratio (CAh)
COM Pin	0	28	0	28	Display start line (A1h)
COM0	Row0	Row28	Row0	Row28	
COM1	Row1	Row29	Row1	Row29	
COM2	Row2	Row30	Row2	Row30	
COM3	Row3	Row31	Row3	Row31	
COM4	Row4	Row32	Row4	Row32	
COM5	Row5	Row33	Row5	Row33	
COM6	Row6	Row34	Row6	Row34	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
:	:	:	:	:	
COM143	Row143	Row171	Row143	Row171	
COM144	Row144	Row172	Row144	Row172	
COM145	Row145	Row173	Row145	Row173	
COM146	Row146	Row174	Row146	Row174	
COM147	Row147	Row175	Row147	Row175	
COM148	Row148	Row0	-	-	
COM149	Row149	Row1	-	-	
COM150	Row150	Row2	-	-	
COM151	Row151	Row3	-	-	
COM152	Row152	Row4	-	-	
COM153	Row153	Row5	-	-	
COM154	Row154	Row6	-	-	
COM155	Row155	Row7	-	-	
COM156	Row156	Row8	-	-	
COM157	Row157	Row9	-	-	
COM158	Row158	Row10	-	-	
COM159	Row159	Row11	-	-	
COM160	Row160	Row12	-	-	
COM161	Row161	Row13	-	-	
COM162	Row162	Row14	-	-	
COM163	Row163	Row15	-	-	
COM164	Row164	Row16	-	-	
COM165	Row165	Row17	-	-	
COM166	Row166	Row18	-	-	
COM167	Row167	Row19	-	-	
COM168	Row168	Row20	-	-	
COM169	Row169	Row21	-	-	
COM170	Row170	Row22	-	-	
COM171	Row171	Row23	-	-	
COM172	Row172	Row24	-	-	
COM173	Row173	Row25	-	-	
COM174	Row174	Row26	-	-	
COM175	Row175	Row27	-	-	
Display example	 (a)	 (b)	 (c)	 (d)	 (GDDARAM)	

1.7 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-175. For example, to move the COM16 towards the COM0 direction for 16 lines, A[7:0] should be given by 00010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 1-6 : Example of Set Display Offset with no Remap

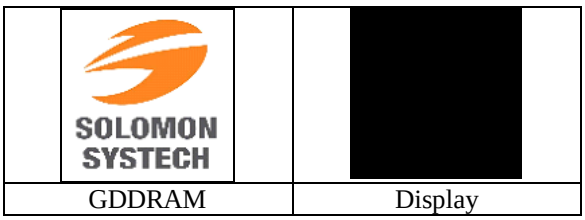
	a	b	c	Case
	176	144	144	MUX ratio (CAh)
	0	0	32	Display offset (A2h A[7:0])
COM0	Row0	Row0	Row32	
COM1	Row1	Row1	Row33	
COM2	Row2	Row2	Row34	
:	:	:	:	
COM109	Row109	Row109	Row141	
COM110	Row110	Row110	Row142	
COM111	Row111	Row111	Row143	
COM112	Row112	Row112	-	
COM113	Row113	Row113	-	
COM114	Row114	Row114	-	
:	:	:	:	
COM141	Row141	Row141	-	
COM142	Row142	Row142	-	
COM143	Row143	Row143	-	
COM144	Row144	-	Row0	
COM145	Row145	-	Row1	
COM146	Row146	-	Row2	
:	:	:	:	
COM173	Row173	-	Row29	
COM174	Row174	-	Row30	
COM175	Row175	-	Row31	
Display example	 (a)	 (c)	 (d)	 (GDDARAM)

1.8 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Entire Display OFF, Entire Display ON, Normal Display and Inverse Display.

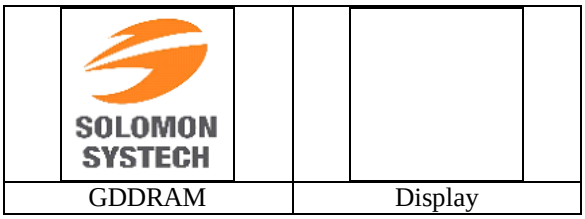
- Set Entire Display OFF (A4h)
  Force the entire display to be at gray scale level "GS0" regardless of the contents of the display data RAM as shown in Figure 1-7.

Figure 1-7 : Example of Entire Display OFF



- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale "GS63" regardless of the contents of the display data RAM as shown in Figure 1-8.

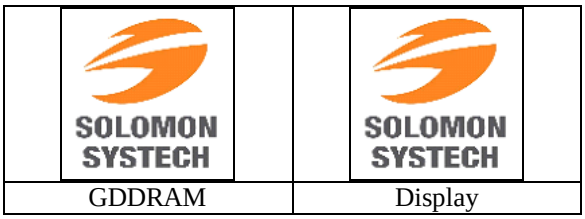
Figure 1-8 : Example of Entire Display ON



- Normal Display (A6h)

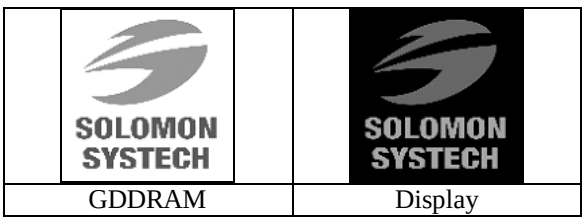
  Reset the above effect and turn the data to ON at the corresponding gray level. Figure 1-9 shows an example of Normal Display.

Figure 1-9 : Example of Normal Display



- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" ↔ "GS63", "GS1" ↔ "GS62", …
  Figure 1-10 shows an example of inverse display.

Figure 1-10 : Example of Inverse Display



1.9 Set Sleep mode ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.
When the display is OFF (command AEh), the segment is in V_{SS} state and common is in high impedance state.

1.10 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 2 to 30 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 2 to 30 in the unit of 2DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P.

1.11 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 256, with reset value =0. Please refer to Product Preview Section 6.3 for the detail relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

1.12 Set Second Pre-charge period (B6h)

This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 1 to 15 DCLK's.

1.13 Look Up Table for Gray Scale Pulse width (B8h, BCh, BDh)

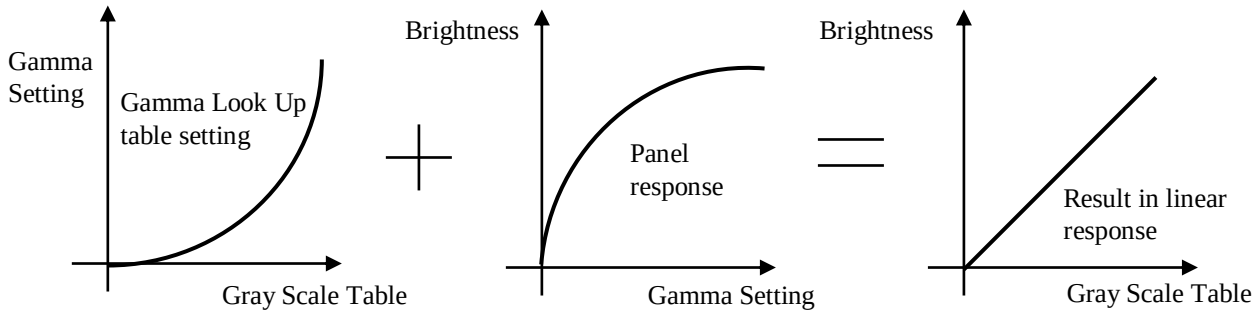
This command is used to set each individual gray scale level of Color A, B and C for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON.

Following the command B8h, the user has to set the gray scale setting for GS1B, GS2B, …, GS62B, GS63B one by one in sequence for LUT of color B. GS1 can be set as gamma setting 0, which means there is only pre-charge phase but no current drive phase. Refer to Product Preview Section 6.8 for details. Command B8h should be input before command BCh and BDh, to select LUT for color B, A and C.

After setting B8h command, BCh and BDh commands are used to set gray scale setting for color A and color C respectively. Following the command BCh, the user has to set the gray scale setting for GS1A, GS2A, …, GS30A, GS31A one by one in sequence for LUT of color A. While following the command BDh, the user has to set the gray scale setting for GS1C, GS2C, …, GS30C, GS31C one by one in sequence for LUT of color C.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 1-11) can compensate this effect.

Figure 1-11: Example of Gamma correction by Gamma Look Up table setting



1.14 Use Built-in Linear LUT (B9h)

This single byte command reloads the preset linear Gray Scale table. For color B, GS0 =Gamma Setting 0, GS1 = Gamma Setting 0, GS2 = Gamma Setting 2, GS3 = Gamma Setting 4,... GS62 = Gamma Setting 122, GS63 = Gamma Setting 124. Refer to Product Preview Section 6.8 for details.

1.15 Set Pre-charge voltage (BBh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC}.

1.16 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}.

1.17 Set Contrast Current for Color A,B,C (C1h)

This command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

1.18 Master Contrast Current Control (C7h)

This double byte command is to control the segment output current by a scaling factor. The chip has 16 master control steps, with the factor ranges from 1 [0000b] to 16 [1111b – default]. The smaller the master current value, the dimmer the OLED panel display is set.
For example, if original segment output current is 320uA at scale factor = 16, setting scale factor to 8 would reduce the current to 160uA.

1.19 Set Multiplex Ratio (CAh)

This double byte command switches default 1:176 multiplex mode to any multiplex mode from 4 to 176. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h. Figure 1-5 and Figure 1-6 show examples of setting the multiplex ratio through command CAh.

1.20 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the "Lock" state. And the driver IC will then respond to the command and memory access.

Appendix VI: SSD1333 Master Contrast Current Control

SSD1333 supports 64 step master current control.

1 COMMAND TABLE

Table 1-1 : Command Table for Master Contrast Current Control

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[7:0]=3Fh [reset]
1	A[7:0]	A_7	*	A_5	A_4	A_3	A_2	A_1	A_0		When A[7] = 0b [reset]: master contrast ranges from 1/16 to 16/16 by toggling A[3:0]: 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset] While A[5:4] = don't care When A[7] = 1b: master contrast ranges from 1/64 to 64/64 by toggling A[5:0]: 000000b reduce output currents for all colors to 1/64 000001b reduce output currents for all colors to 2/64 .... 111110b reduce output currents for all colors to 63/64 111111b no change [reset]

1 COMMAND DESCRIPTION

1.1 Master Contrast Current Control (C7h)

This double byte command is to control the segment output current by a scaling factor.

The chip has 16 master control steps by default when A[7] is set to 0b, with the factor ranges from 1 [0000b] to 16 [1111b – default].

The chip can also support 64 master control steps when A[7] is set to 1b, with the factor ranges from 1 [000000b] to 64 [111111b].

The smaller the master current value, the dimmer the OLED panel display is set.
For example, if original segment output current is 320uA at scale factor = 16 at A[7] = 0b, setting scale factor to 8 would reduce the current to 160uA.
For example, if original segment output current is 320uA at scale factor = 64 at A[7] = 1b, setting scale factor to 8 would reduce the current to 40uA.