



# EK79716B

Rev. 1.6

DATA SHEET

**1200CH TFT LCD**  
**Source Driver with TCON**

*fitipower integrated technology Inc.*

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## 1200CH TFT LCD Source Driver with TCON

### 1. GENERAL DESCRIPTION

EK79716 is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. EK79716 integrated source driver, timing controller and pin control interface.

EK79716 input timing support TTL digital 24bit parallel RGB data format, and source output support 8-bit resolution 256 gray scales with dithering features. Operating parameters can be set via pin control for all control features. Special circuit architecture is designed for lower power dissipation.

EK79716 support two chip cascade operation mode to reduce the FPC amount and save the cost. Configure able Master and Slave configuration increase the flexibility for different panel design. With wide range of supply voltages and small output deviations make this chip more suitable for various applications.

### 2. FEATURES

- Special design for small-sized color TFT LCD source drivers with timing controller
- Integrated 1200 channel source driver
- Support display resolutions : 800(RGB)x600、800(RGB)x480、400(RGB)x480、400(RGB)x240
- 8-bit resolution 256 gray scale with 2-bits dithering ( 6bits DAC + 2bits HFRC)
- Support TTL 24-bit parallel (RGB) input timing
- Support cascade function with bidirectional shift control (CMOS signal)
- Support single or dual-gate operation mode
- Support Stripe color filter configuration
- Support stand-by mode for low power consumption
- Support dot inversion driving scheme (Cascade mode)
- Support 2 dot one inversion driving scheme (Dual Gate mode)
- V1 ~ V4 for adjusting Gamma correction
- Output dynamic range: 0.1V ~ VDDA-0.1V (Dual Gate mode)
- Power for source driver voltage VDDA: 6.5V ~ 13.5V
- Power for digital interface circuit VDD: 1.7 ~ 3.6V (Dual Gate mode)
- Power for digital interface circuit VDD: 1.7 ~ 3.6V (Cascade mode)
- Max. operating frequency: 50 MHz (Dual Gate mode)
- Max. operating frequency: 40MHz (Cascade mode)
- Minimum operating frequency: 20 MHz (800(RGB)x600 and 800(RGB)x480 display resolution)
- Built-in AUTO pattern
- COG package
- Chip Size: 22487um X 803um(not include scribe line), Output Pad Pitch: 17um

### 3. BLOCK DIAGRAM

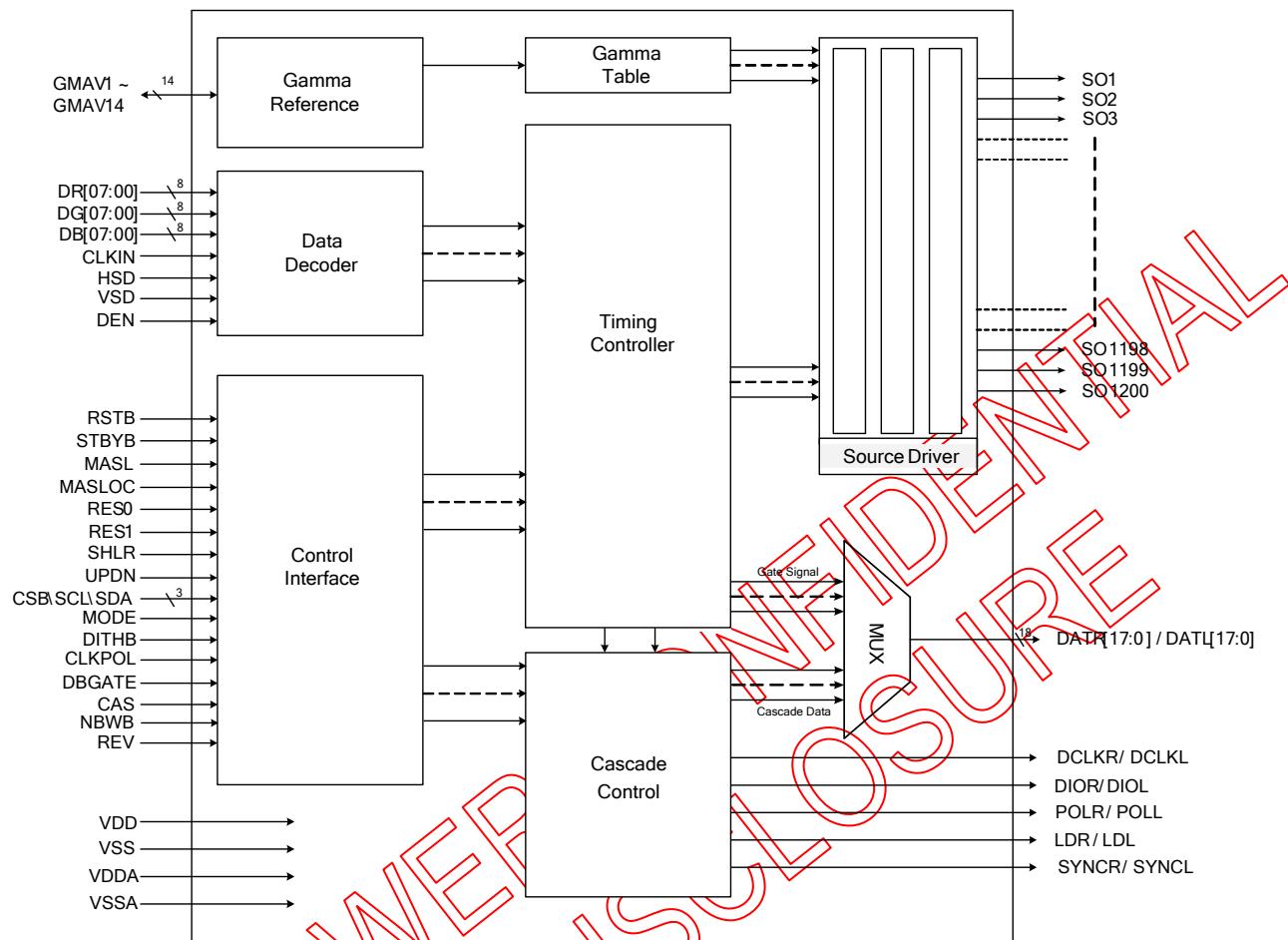
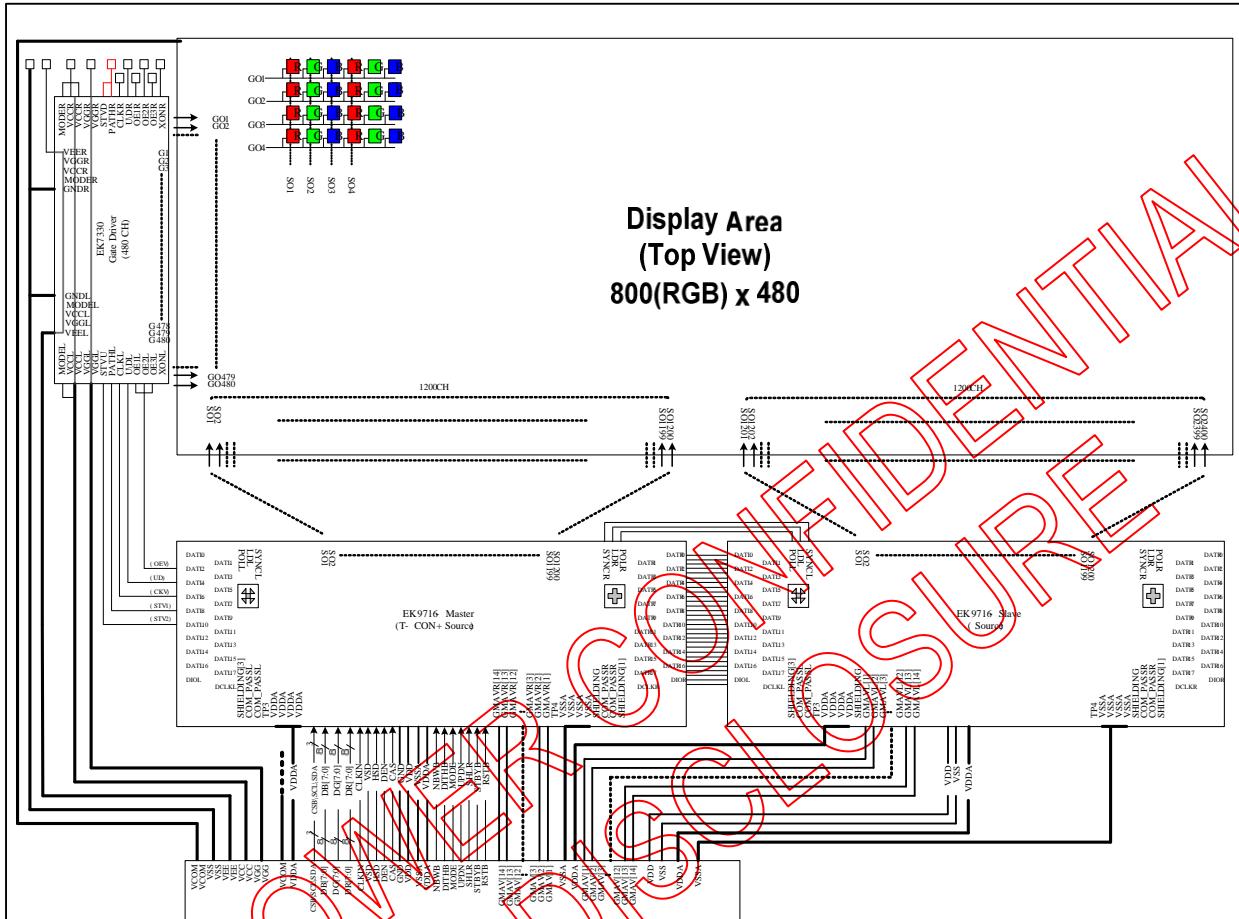
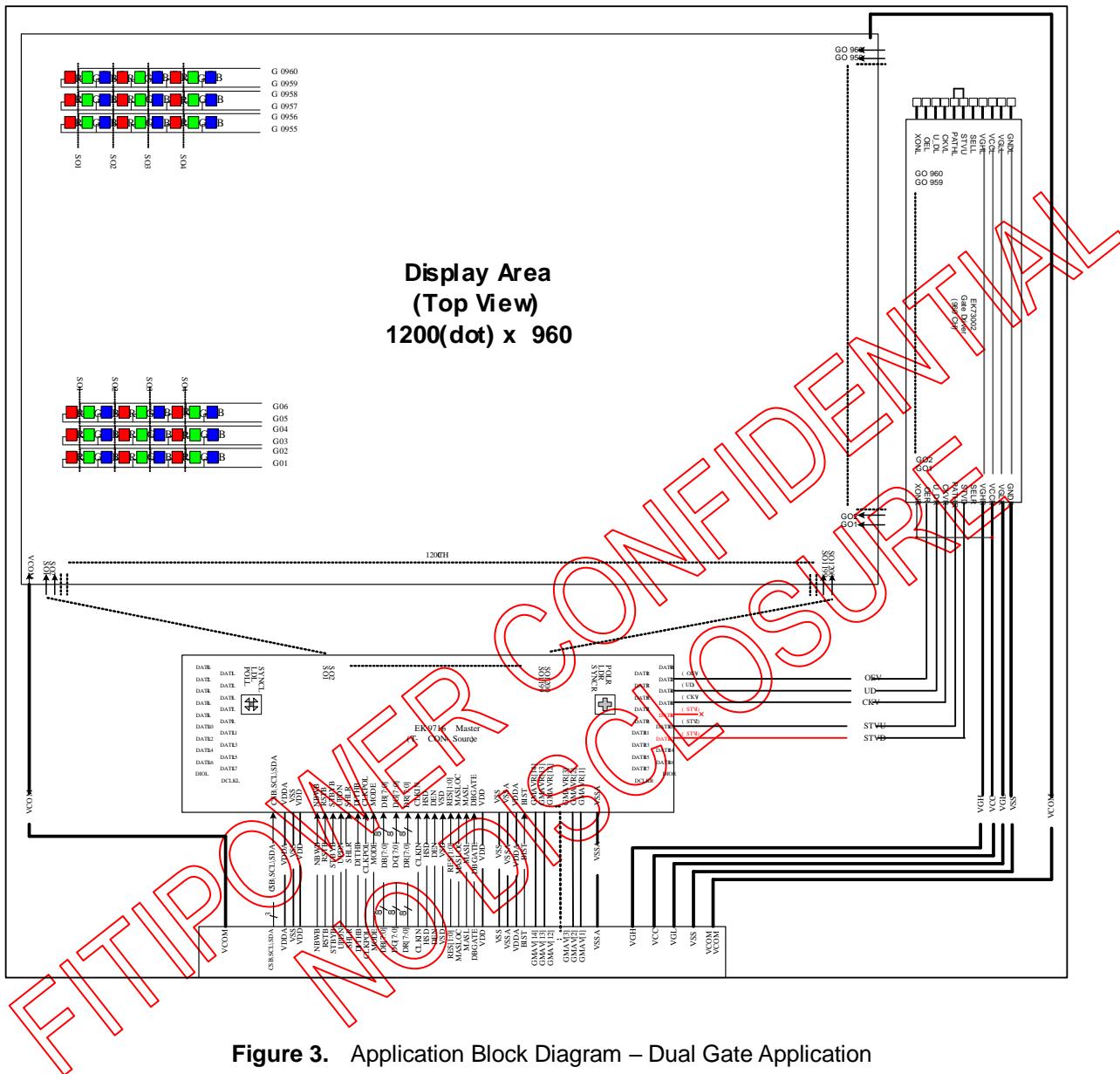


Figure 1. Block Diagram



**Figure 2.** Application Block Diagram – 2 Chip Cascade



**Figure 3.** Application Block Diagram – Dual Gate Application

**FIT**

EK79716

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View



Figure 4. Pad Sequence (Bump Side)

## 4. PIN DESCRIPTION

Table 1. Pin Description

Pin Name	Pin Type	Description
DR[07:00] DG[07:00] DB[07:00]	Input	Parallel data Input. For TTL 24-bit parallel RGB image data input. DR[07:00]=R[7:0] data; DG[07:00]=G[7:0] data; DB[07:00]=B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to VSS.
CLKIN	Input	Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge.
HSD	Input	Horizontal Sync input. Negative polarity.
VSD	Input	Vertical Sync input. Negative polarity.
DEN	Input	Data Input Enable. Active High to enable the data input bus under "DE Mode". Normally pull low.
MODE	Input	DE / SYNC mode select. Normally pull high H: DE mode.(Default) L: HSD/VSD mode.
RES[1:0]	Input	Display resolution selection. RES[1:0] = "00", for 800(RGB)*480 display resolution(Default) RES[1:0] = "01", for 800(RGB)*600 display resolution RES[1:0] = "10", for 400(RGB)*480 display resolution RES[1:0] = "11", for 400(RGB)*240 display resolution
DITHB	Input	Dithering function enable control. Normally pull high DITHB = "1", Disable internal dithering function(Default) DITHB = "0", Enable internal dithering function
CLKPOL	Input	Input clock edge selection. Normally pull low CLKPOL = "1", Latch data at CLKIN rising edge. CLKPOL = "0", Latch data at CLKIN falling edge. (Default)
DBGATE	Input	Dual Gate function enables control. Normally pull low DBGATE = "1", Enable Dual Gate Function. DBGATE = "0", Disable Dual Gate Function (Default) Note: Cascade function will be disabled under "dual gate" mode
GMAV1 ~ GMAV14	Input/Output	Gamma correction reference voltage. These input voltage must be offered by user. VSSA+0.1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< VDDA-0.1 (Dual Gate) VSSA+1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< VDDA-1 (Cascade mode) V2, V6, V9, V13 pads are disabled.
RSTB	Input	Global reset pin. Active Low to enter Reset State. Suggest to connecting with an RC reset circuit for stability. Normally pull high.
STBYB	Input	Standby mode, Normally pull high. STBYB = "1", normal operation(Default) STBYB = "0", timing controller, source driver will turn off, all output are High-Z
MASL	Input	Master and Slave Mode selection. Normally pull high. MASL = "H", for Master mode. (Default Mode) MASL = "L", for Slave mode. Only the Master chip will issue the Gate and Cascade control signal.
MASLOC	Input	Master location definition pin. Normally pull low. MASLOC = "L", Master locate on right side (Panel top view). (Default Mode) MASLOC = "H", Master locate on left side (Panel top view).
CSB	Input	Serial communication chip select. Normally pull high
SDA	Input/Output	Serial communication data input. Normally pull low

Pin Name	Pin Type	Description
SCL	Input	Serial communication clock input. Normally pull low
SHLR	Input	Source Right or Left sequence control. Normally pull high. SHLR = "L", shift left: last data = S1←S2←S3.....←S1200 = first data. SHLR = "H", shift right: first data = S1→S2→S3.....→S1200 = last data.
UPDN	Input	Gate Up or Down scan control. Normally pull low. UPDN = "L", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver.(Default) UPDN = "H", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
BIST	Input	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
CAS	Input	Cascade function select. Normally pull high. CAS = "H", Enable cascade function.(Default) CAS = "L", Disable cascade function.
NBWB	Input	Normally black or normally white setting. NBWB = "0" : Normally black NBWB = "1" : Normally white (Default)
REV	Input	Controls whether the data of D00~D27 are inverted or not, normally pulled low. When "REV"=1 these data will be inverted. EX. "00" → "3F", "07" → "38", "15" → "2A", and so on.
DATR[17:0]	Input/Output	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKR	Input/Output	Master and Slave cascade control signal.
DIOR	Input/Output	Master and Slave cascade control signal..
POLR	Input/Output	Master and Slave cascade control signal.
LDR	Input/Output	Master and Slave cascade control signal.
SYNCR	Input/Output	Master and Slave cascade control signal.
DATL[17:0]	Input/Output	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKL	Input/Output	Master and Slave cascade control signal.
DIOL	Input/Output	Master and Slave cascade control signal.
POLL	Input/Output	Master and Slave cascade control signal.
LDL	Input/Output	Master and Slave cascade control signal.
SYNCL	Input/Output	Master and Slave cascade control signal.
VDDA	Power Input	Power supply for analog circuits
VSSA	Power Input	Ground pins for analog circuits
VDD	Power Input	Power supply for digital circuits
VSS	Power Input	Ground pins for digital circuits
SO1~SO1200	Output	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
ALIGN	Mark	For assembly alignment.
COM_PASSR COM_PASSL	Shorted line	Internal link together between input side and output side.
TP22~0	Testing	Float these pins for normal operation.
SHIELDING	Shielding	IC Shielding pads. Those pins are internally connected to the VSSA. DO NOT connect to any WOA on the panel.

Pin Name	Pin Type	Description
DASHD	Shielding	Data Bus Shielding pad. Those pins are internally connected to the VSS. RECOMMAND to add shielding lines on the FPC to reduce EMI.

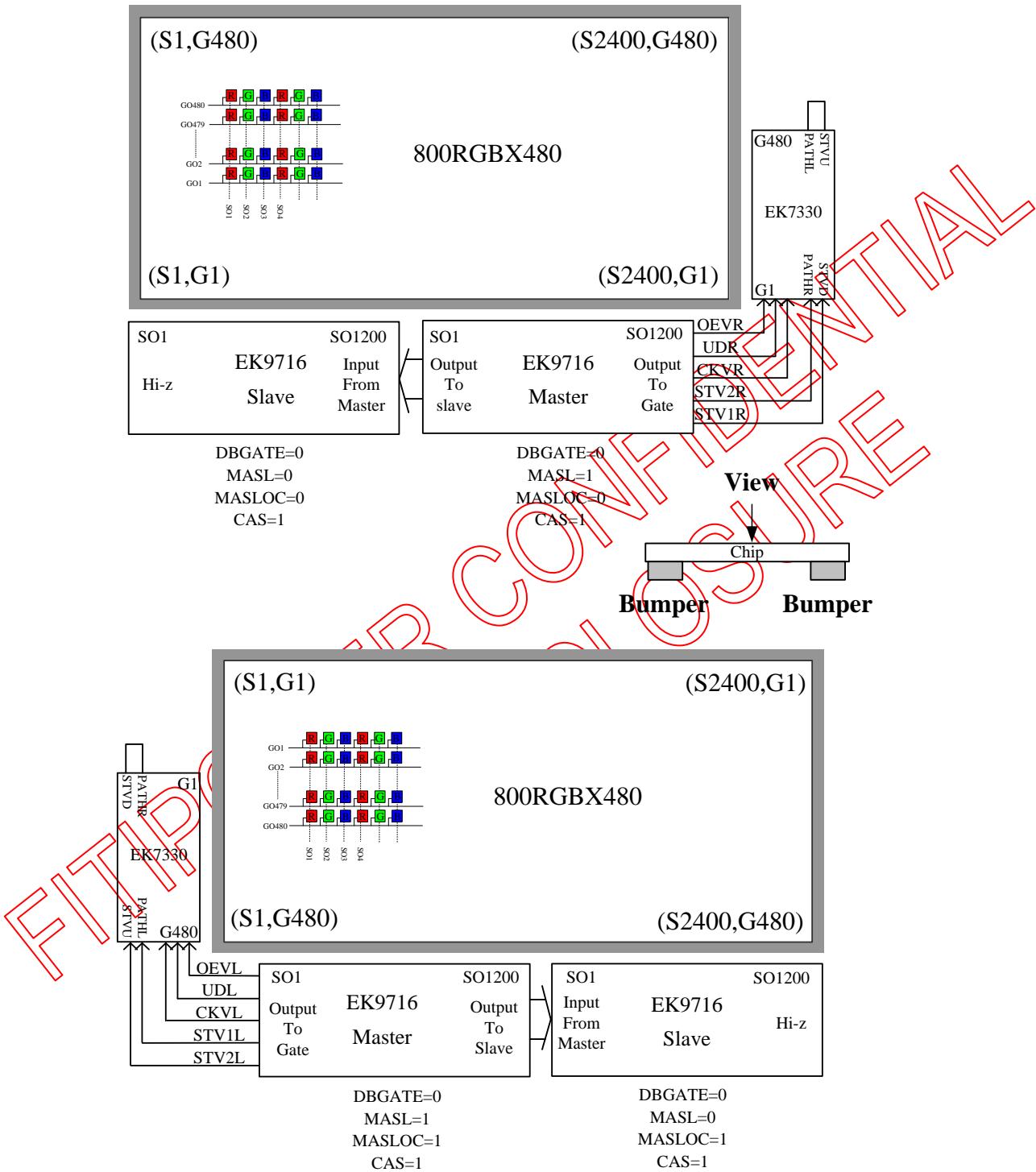
**Table 2.** EK79716 Pass Line Description:

Pass Line No:	Pad Name	
1	COM_PASSR	COM_PASSR
2	COM_PASSL	COM_PASSL

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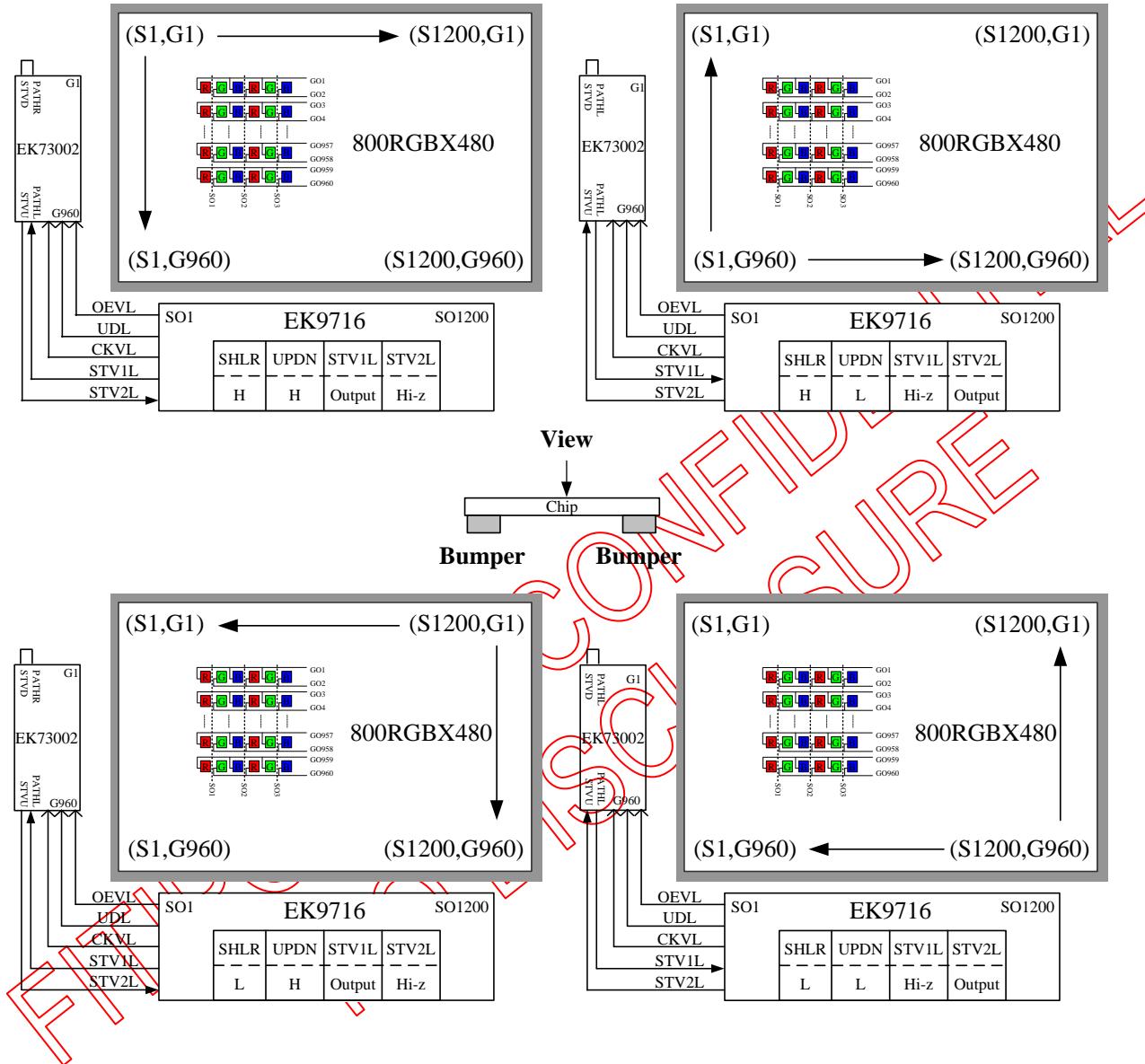
## 4.1. Chip Driver configuration examples of the EK79716

Two pieces of EK79716 driver are cascaded application for 800RGB x480



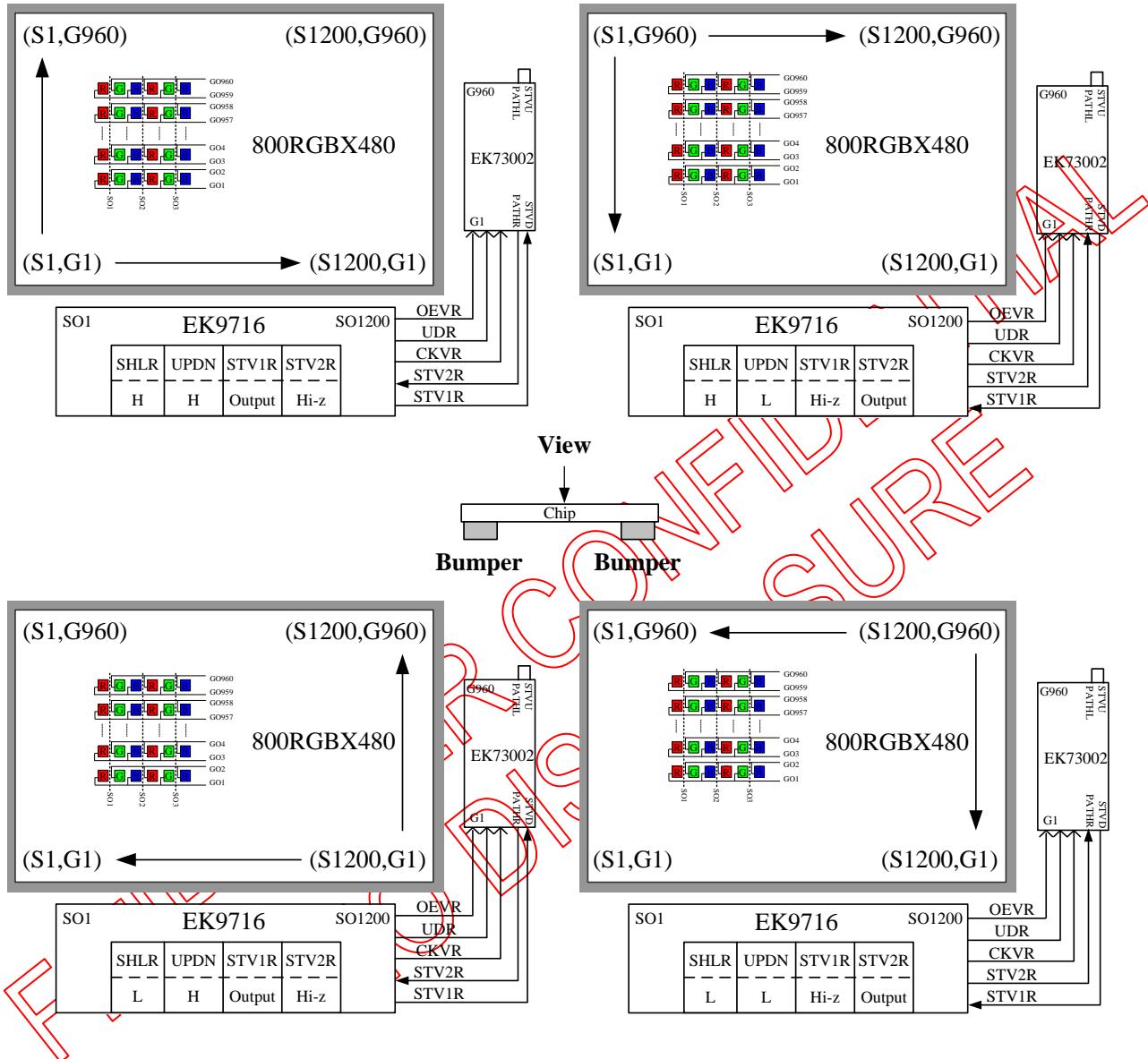
## 4.2. EK79716 put down and EK73002 put left side for 800RGBx480 of dual-gate mode

When DBGATE=1, MASL=1, MASLOC=X and CAS=0, application of the EK79716 will be illustrated as figure.



## 4.3. EK79716 put down and EK73002 put right side for 800RGBx480 of dual-gate mode

When DBGATE=1, MASL=1, MASLOC=X and CAS=0, application of the EK79716 will be illustrated as figure.



**4.4. Value of wiring resistance to each pin**

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

**Table 3.** wiring resistance

Pin Name	Wiring resistance value( $\Omega$ )	Pin Name	Wiring resistance value ( $\Omega$ )
VDD	<25	BIST	<1K
VDDA	<5	CAS	<1K
VSS	<25	CSB/SCL/SDA	<200
VSSA	<5	DATR[17:0]	<200 & 20 pf
GMAV1~GMAV14	<10	DCLKR	<200 & 20 pf
DR[07:00]	<200	DIOR	<200 & 20 pf
DG[07:00]	<200	POLR	<200 & 20 pf
DB[07:00]	<200	LDR	<200 & 20 pf
DEN	<200	SYNCR	<200 & 20 pf
MODE	<1K	DATL[17:0]	<200 & 20 pf
RES[1:0]	<1K	DCLKL	<200 & 20 pf
DITHB	<1K	DIOL	<200 & 20 pf
CLKPOL	<1K	POLL	<200 & 20 pf
DIMO	<1K	LDI	<200 & 20 pf
DBGATE	<1K	CASCADE GMAV1~GMAV14	<30
RSTB	<1K	CLKIN	<50
MASL	<1K	HSD	<200
MASLOC	<1K	VSD	<200
SHLR	>1K		
UPDN	<1K		

Table 4. DATR[17:0] / DATL[17:0] pin mapping Table:

DATR[17:0]	DBGATE = "0" MASL = "1" MASLOC = "0" CAS = "1"	DBGATE = "0" MASL = "1" MASLOC = "1" CAS = "1"	DBGATE = "0" MASL = "0" MASLOC = "0" CAS = "1"	DBGATE = "0" MASL = "0" MASLOC = "1" CAS = "1"	DBGATE = "1" MASL = "1" MASLOC = "X" CAS = "0"	DBGATE = "0" MASL = "1" MASLOC = "X" RES[1:0] = "1X" CAS = "0"
Description	Master for cascade. Master locate on panel right side	Master for cascade. Master locate on panel left side	Slave for cascade. Master locate on panel right side	Slave for cascade. Master locate on panel left side	Dual Gate Mode	Single Source Mode
DATR0	X	DAT0	DAT0	X	X	X
DATR1	X	DAT1	DAT1	X	X	X
DATR2	OEV	DAT2	DAT2	X	OEV	OEV
DATR3	X	DAT3	DAT3	X	X	X
DATR4	UD	DAT4	DAT4	X	UD	UD
DATR5	X	DAT5	DAT5	X	X	X
DATR6	CKV	DAT6	DAT6	X	CKV	CKV
DATR7	X	DAT7	DAT7	X	X	X
DATR8	STV1	DAT8	DAT8	X	STV1	STV1
DATR9	X	DAT9	DAT9	X	X	X
DATR10	STV2	DAT10	DAT10	X	STV2	STV2
DATR11	X	DAT11	DAT11	X	X	X
DATR12	STV1	DAT12	DAT12	X	STV1	STV1
DATR13	X	DAT13	DAT13	X	X	X
DATR14	X	DAT14	DAT14	X	X	X
DATR15	X	DAT15	DAT15	X	X	X
DATR16	STBN	DAT16	DAT16	X	STBN	STBN
DATR17	X	DAT17	DAT17	X	X	X
DCLKR	X	DCLK	DCLK	X	X	X
DIOR	X	DIO	DIO	X	X	X
LDR	X	LD	LD	X	X	X
SYNCR	X	SYNC	SYNC	X	X	X
<hr/>						
DATL0	DAT0	X	X	DAT0	X	X
DATL1	DAT1	X	X	DAT1	X	X
DATL2	DAT2	OEV	X	DAT2	OEV	OEV
DATL3	DAT3	X	X	DAT3	X	X
DATL4	DAT4	UD	X	DAT4	UD	UD
DATL5	DAT5	X	X	DAT5	X	X
DATL6	DAT6	CKV	X	DAT6	CKV	CKV
DATL7	DAT7	X	X	DAT7	X	X
DATL8	DAT8	STV1	X	DAT8	STV1	STV1
DATL9	DAT9	X	X	DAT9	X	X
DATL10	DAT10	STV2	X	DAT10	STV2	STV2
DATL11	DAT11	X	X	DAT11	X	X
DATL12	DAT12	STV1	X	DAT12	STV1	STV1
DATL13	DAT13	X	X	DAT13	X	X
DATL14	DAT14	X	X	DAT14	X	X
DATL15	DAT15	X	X	DAT15	X	X
DATL16	DAT16	STBN	X	DAT16	STBN	STBN
DATL17	DAT17	X	X	DAT17	X	X
DCLKL	DCLK	X	X	DCLK	X	X
DIOL	DIO	X	X	DIO	X	X
LDL	LD	X	X	LD	X	X
SYNCL	SYNC	X	X	SYNC	X	X

## 5. 3-WIRE SERIAL PORT INTERFACE

### 5.1. 3-Wire Command Format

EK79716 use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79716 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing Diagram” for the detail timing.

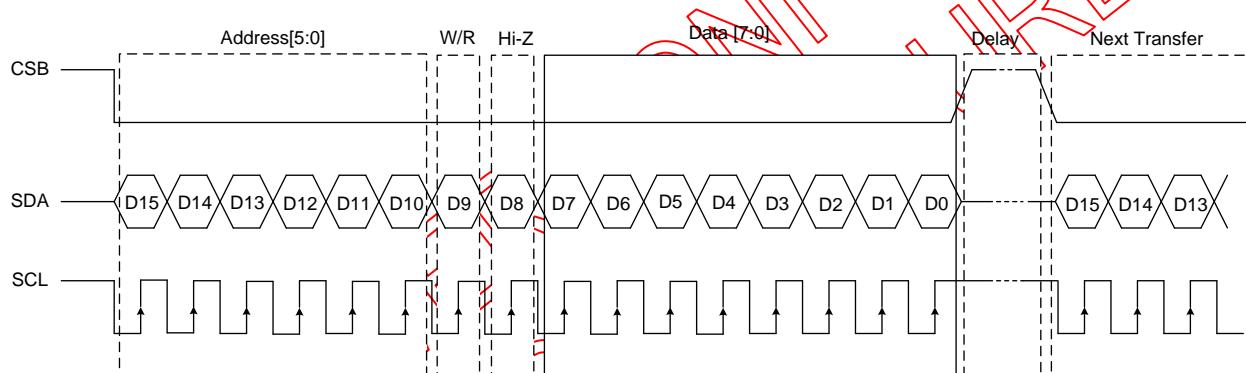


Figure 5. 3-Wire timing chart

Table 5. 3-Wire Command Format

Bit	Description
D15 – D10	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7 – D0	Data for the W/R operation to the address indicated by Address phase

Table 6. 3-Wire Writer Format

MSB	LSB														
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]				0	X	DATA (Issue by external controller)									

Table 7. 3-Wire Read Format

MSB	LSB														
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]				1	Hi-Z	DATA (Issue by 3-Wire engine)									

**5.2. 3-Wire Control Registers**

Following table list all the 3-Wire control registers and bit name definition for EK79716. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

**5.3. 3-Wire Control Register List**

NO.	Address						R/W	D8	MSB	Initial value							LSB
	D15	D14	D13	D12	D11	D10				D7	D6	D5	D4	D3	D2	D1	
R0	0	0	0	0	0	0	R/W(0)	X	RES[1]	RES[0]	SHLR	UPDN	STBYB	GRB	-	MODE	
									0	0	1	0	1	1	1	1	
R1	0	0	0	0	0	1	R/W(0)	X	NBW	-	SCI_ON	-	-	HFR	DITHB	BIST	
									1	-	0	-	-	1	1	0	

Note:

1. The register except upper list was for testing use, to write test register was not allowed.

**Table 8. R0: System Control Register**

Designation	Address	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. MODE="1", DE mode. (Default)
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control and driver are off. All outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data=S1->S2->S3 ... <-S1200=First data. SHLR="1", Shift right: First data=S1->S2->S3 ... ->S1200=Last data. (Default)
RES[1:0]	R0[7:6]	Display resolution selection. RES[1:0] = "00", for 800(RGB)*480 display resolution.(Default) RES[1:0] = "01", for 800(RGB)*600 display resolution. RES[1:0] = "10", for 400(RGB)*480 display resolution. RES[1:0] = "11", for 400(RGB)*240 display resolution.

Table 9. R1: System Control Register

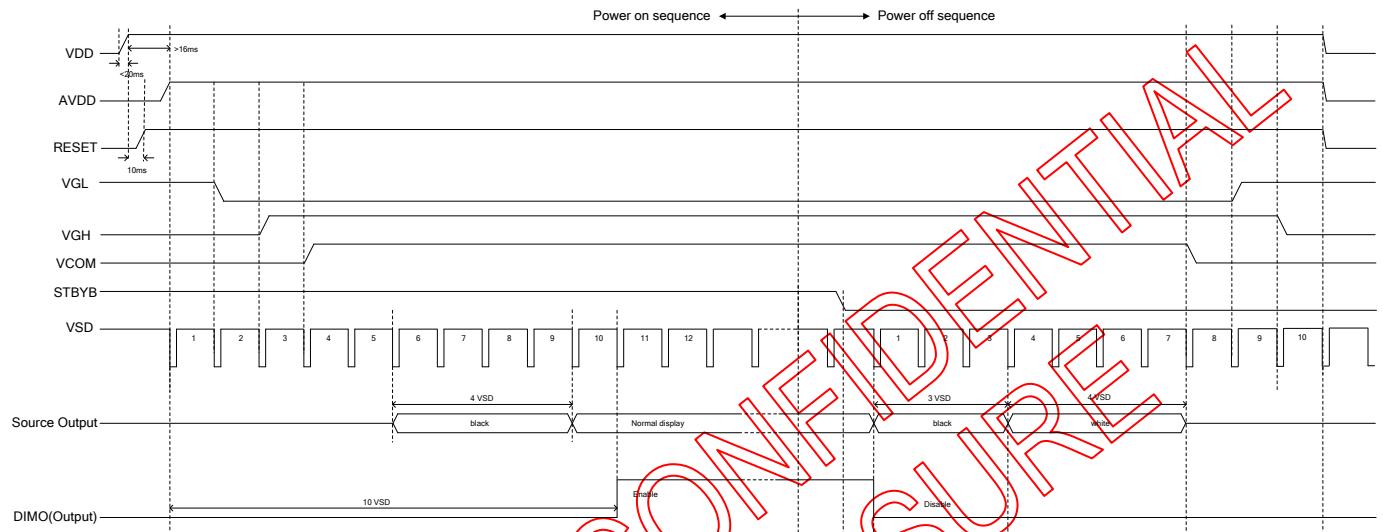
Designation	Address	Description
BIST	R1[0]	Normal Operation/BIST pattern select. BIST = "0" : Normal Operation (Default) BIST = "1" : BIST(DCLK input is not needed)
DITHB	R1[1]	Dithering function enable control. Normally pull high DITHB = "0", Enable internal dithering function. DITHB = "1", Disable internal dithering function.(Default)
HFRC	R1[2]	H-FRC selection. HFRC = "0" : FRC enable. HFRC = "1" : HiFRC enable(Default). If DITHER = "1" , disable dithering function(HiFRC and FRC disable)
SCI_ON	R1[5]	Enable 3-wire control function. Normally pull low SCI_ON = "0" : Base on pin control function. (Default) SCI_ON = "1" : Base on 3-wire register.
NBWB	R1[7]	Normally black or normally white setting. NBWB = "0" : Normally black NBWB = "1" : Normally white (Default)

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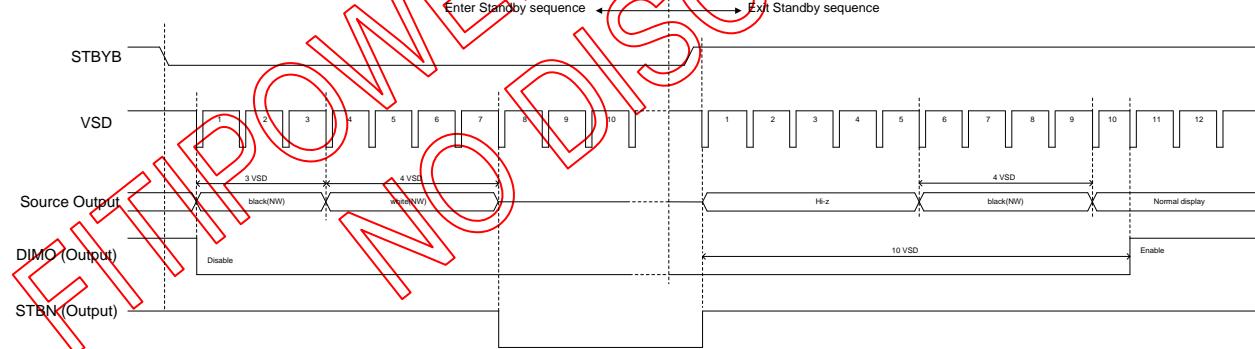
## 6. FUNCTION DESCRIPTION

### 6.1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time ( $T_{POR}$ ) of the digital power supply VDD should be maintained within the given specifications. Refer to "AC Characteristics" for more detail on timing.



**Figure 6. Power-On/Off Timing Sequence**



**Figure 7. Enter and Exit Standby Mode Sequence**

## 6.2. Input Data VS Output Channels

### 6.2.1. DBGATE="0" (Stripe Mode)

**Table 10.** SHLR="1", right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data				→	Last data	
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]

**Table 11.** SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data				←	First data	
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]

### 6.2.2. DBGATE="1" (Stripe Mode)

**Table 12.** SHLR="1", right shift

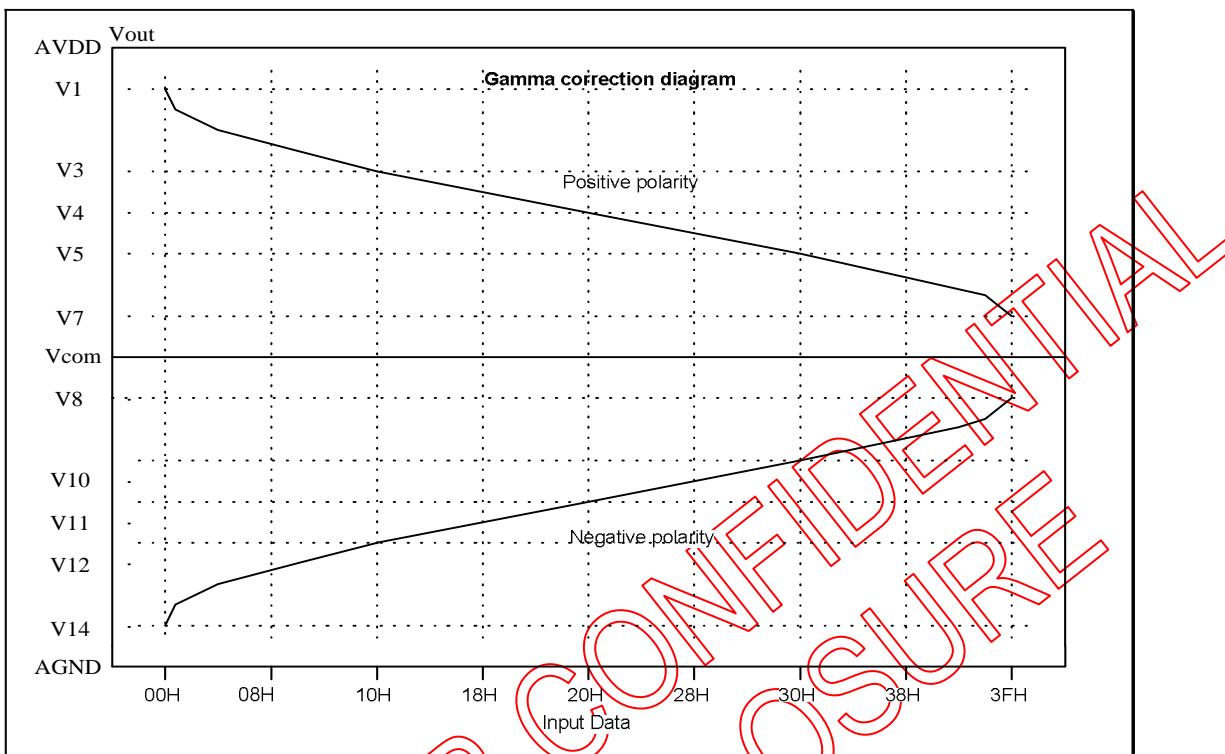
Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data				→	Last data	
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Even Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]

**Table 13.** SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data				←	First data	
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Even Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]

### 6.3. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.

**Remark:**

Dual Gate : VDDA-0.1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > VSSA+0.1V

Cascade : VDDA-1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > VSSA+1V

## 6.4. Input Data and Output Voltage Reference Table

**Table 14.** Gamma correction resistor ratio

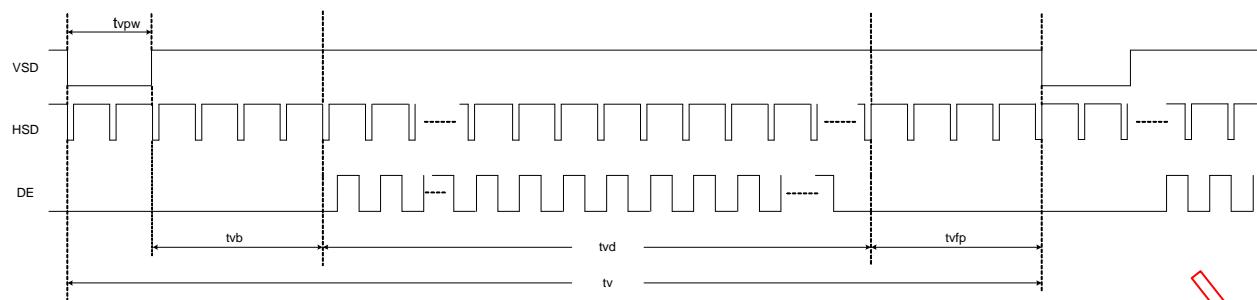
Name	Resistor	Name	Resistor
R0	8.0	R32	0.63
R1	7.11	R33	0.63
R2	6.22	R34	0.63
R3	5.33	R35	0.62
R4	4.45	R36	0.62
R5	3.56	R37	0.62
R6	2.97	R38	0.62
R7	2.48	R39	0.61
R8	2.14	R40	0.61
R9	1.89	R41	0.61
R10	1.69	R42	0.62
R11	1.54	R43	0.63
R12	1.39	R44	0.64
R13	1.28	R45	0.64
R14	1.21	R46	0.65
R15	1.14	R47	0.67
R16	1.05	R48	0.75
R17	1	R49	0.9
R18	0.94	R50	1
R19	0.91	R51	1
R20	0.87	R52	1.2
R21	0.84	R53	1.2
R22	0.81	R54	1.4
R23	0.78	R55	1.5
R24	0.76	R56	1.7
R25	0.73	R57	2
R26	0.71	R58	2.1
R27	0.7	R59	2.3
R28	0.68	R60	3.1
R29	0.67	R61	4.2
R30	0.66	R62	20.1
R31	0.64		

Table 15. Output Voltage VS Input Data

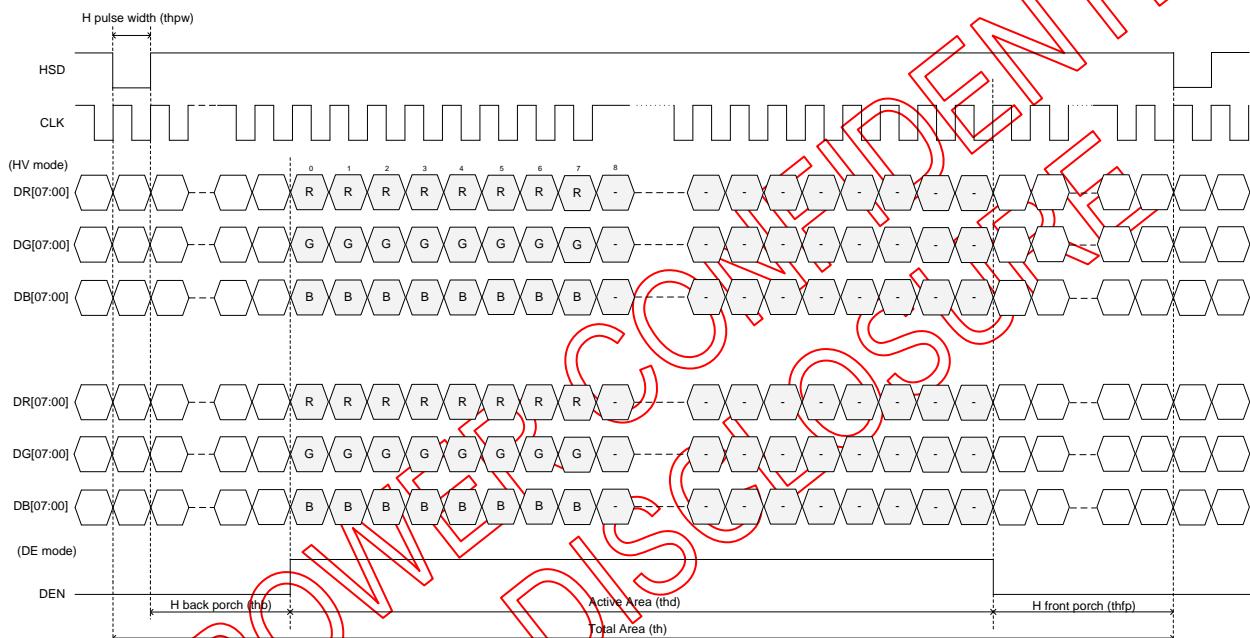
Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	$V3 + (V1 - V3) \times 44.4 / 52.4$	$V14+ (V12 - V14) \times 8 / 52.4$
02H	$V3 + (V1 - V3) \times 37.29 / 52.4$	$V14+ (V12 - V14) \times 15.11 / 52.4$
03H	$V3 + (V1 - V3) \times 31.06 / 52.4$	$V14+ (V12 - V14) \times 21.34 / 52.4$
04H	$V3 + (V1 - V3) \times 25.73 / 52.4$	$V14+ (V12 - V14) \times 26.67 / 52.4$
05H	$V3 + (V1 - V3) \times 21.28 / 52.4$	$V14+ (V12 - V14) \times 31.12 / 52.4$
06H	$V3 + (V1 - V3) \times 17.73 / 52.4$	$V14+ (V12 - V14) \times 34.67 / 52.4$
07H	$V3 + (V1 - V3) \times 14.76 / 52.4$	$V14+ (V12 - V14) \times 37.64 / 52.4$
08H	$V3 + (V1 - V3) \times 12.28 / 52.4$	$V14+ (V12 - V14) \times 40.11 / 52.4$
09H	$V3 + (V1 - V3) \times 10.14 / 52.4$	$V14+ (V12 - V14) \times 42.26 / 52.4$
0AH	$V3 + (V1 - V3) \times 8.25 / 52.4$	$V14+ (V12 - V14) \times 44.15 / 52.4$
0BH	$V3 + (V1 - V3) \times 6.56 / 52.4$	$V14+ (V12 - V14) \times 45.84 / 52.4$
0CH	$V3 + (V1 - V3) \times 5.02 / 52.4$	$V14+ (V12 - V14) \times 47.38 / 52.4$
0DH	$V3 + (V1 - V3) \times 3.64 / 52.4$	$V14+ (V12 - V14) \times 48.76 / 52.4$
0EH	$V3 + (V1 - V3) \times 2.36 / 52.4$	$V14+ (V12 - V14) \times 50.04 / 52.4$
0FH	$V3 + (V1 - V3) \times 1.14 / 52.4$	$V14+ (V12 - V14) \times 51.26 / 52.4$
10H	V3	V12
11H	$V4 + (V3 - V4) \times 11.7 / 12.75$	$V12 + (V11 - V12) \times 1.05 / 12.75$
12H	$V4 + (V3 - V4) \times 10.7 / 12.75$	$V12 + (V11 - V12) \times 2.05 / 12.75$
13H	$V4 + (V3 - V4) \times 9.76 / 12.75$	$V12 + (V11 - V12) \times 2.99 / 12.75$
14H	$V4 + (V3 - V4) \times 8.85 / 12.75$	$V12 + (V11 - V12) \times 3.9 / 12.75$
15H	$V4 + (V3 - V4) \times 7.98 / 12.75$	$V12 + (V11 - V12) \times 4.77 / 12.75$
16H	$V4 + (V3 - V4) \times 7.14 / 12.75$	$V12 + (V11 - V12) \times 5.61 / 12.75$
17H	$V4 + (V3 - V4) \times 6.33 / 12.75$	$V12 + (V11 - V12) \times 6.41 / 12.75$
18H	$V4 + (V3 - V4) \times 5.55 / 12.75$	$V12 + (V11 - V12) \times 7.19 / 12.75$
19H	$V4 + (V3 - V4) \times 4.8 / 12.75$	$V12 + (V11 - V12) \times 7.95 / 12.75$
1AH	$V4 + (V3 - V4) \times 4.06 / 12.75$	$V12 + (V11 - V12) \times 8.68 / 12.75$
1BH	$V4 + (V3 - V4) \times 3.35 / 12.75$	$V12 + (V11 - V12) \times 9.4 / 12.75$
1CH	$V4 + (V3 - V4) \times 2.65 / 12.75$	$V12 + (V11 - V12) \times 10.09 / 12.75$
1DH	$V4 + (V3 - V4) \times 1.97 / 12.75$	$V12 + (V11 - V12) \times 10.78 / 12.75$
1EH	$V4 + (V3 - V4) \times 1.3 / 12.75$	$V12 + (V11 - V12) \times 11.44 / 12.75$
1FH	$V4 + (V3 - V4) \times 0.65 / 12.75$	$V12 + (V11 - V12) \times 12.1 / 12.75$

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	$V5 + (V4 - V5) \times 9.37 / 10$	$V11 + (V10 - V11) \times 0.63 / 10$
22H	$V5 + (V4 - V5) \times 8.74 / 10$	$V11 + (V10 - V11) \times 1.26 / 10$
23H	$V5 + (V4 - V5) \times 8.11 / 10$	$V11 + (V10 - V11) \times 1.89 / 10$
24H	$V5 + (V4 - V5) \times 7.49 / 10$	$V11 + (V10 - V11) \times 2.51 / 10$
25H	$V5 + (V4 - V5) \times 6.87 / 10$	$V11 + (V10 - V11) \times 3.13 / 10$
26H	$V5 + (V4 - V5) \times 6.25 / 10$	$V11 + (V10 - V11) \times 3.75 / 10$
27H	$V5 + (V4 - V5) \times 5.63 / 10$	$V11 + (V10 - V11) \times 4.36 / 10$
28H	$V5 + (V4 - V5) \times 5.02 / 10$	$V11 + (V10 - V11) \times 4.98 / 10$
29H	$V5 + (V4 - V5) \times 4.41 / 10$	$V11 + (V10 - V11) \times 5.59 / 10$
2AH	$V5 + (V4 - V5) \times 3.8 / 10$	$V11 + (V10 - V11) \times 6.2 / 10$
2BH	$V5 + (V4 - V5) \times 3.18 / 10$	$V11 + (V10 - V11) \times 6.82 / 10$
2CH	$V5 + (V4 - V5) \times 2.55 / 10$	$V11 + (V10 - V11) \times 7.45 / 10$
2DH	$V5 + (V4 - V5) \times 1.91 / 10$	$V11 + (V10 - V11) \times 8.08 / 10$
2EH	$V5 + (V4 - V5) \times 1.27 / 10$	$V11 + (V10 - V11) \times 8.72 / 10$
2FH	$V5 + (V4 - V5) \times 0.62 / 10$	$V11 + (V10 - V11) \times 9.38 / 10$
30H	V5	V10
31H	$V7 + (V5 - V7) \times 43.7 / 44.45$	$V10 + (V8 - V10) \times 0.75 / 44.45$
32H	$V7 + (V5 - V7) \times 42.8 / 44.45$	$V10 + (V8 - V10) \times 1.65 / 44.45$
33H	$V7 + (V5 - V7) \times 41.8 / 44.45$	$V10 + (V8 - V10) \times 2.65 / 44.45$
34H	$V7 + (V5 - V7) \times 40.8 / 44.45$	$V10 + (V8 - V10) \times 3.65 / 44.45$
35H	$V7 + (V5 - V7) \times 39.6 / 44.45$	$V10 + (V8 - V10) \times 4.85 / 44.45$
36H	$V7 + (V5 - V7) \times 38.4 / 44.45$	$V10 + (V8 - V10) \times 6.05 / 44.45$
37H	$V7 + (V5 - V7) \times 37 / 44.45$	$V10 + (V8 - V10) \times 7.45 / 44.45$
38H	$V7 + (V5 - V7) \times 35.5 / 44.45$	$V10 + (V8 - V10) \times 8.95 / 44.45$
39H	$V7 + (V5 - V7) \times 33.8 / 44.45$	$V10 + (V8 - V10) \times 10.6 / 44.45$
3AH	$V7 + (V5 - V7) \times 31.8 / 44.45$	$V10 + (V8 - V10) \times 12 / 44.45$
3BH	$V7 + (V5 - V7) \times 29.7 / 44.45$	$V10 + (V8 - V10) \times 14.7 / 44.45$
3CH	$V7 + (V5 - V7) \times 27.4 / 44.45$	$V10 + (V8 - V10) \times 17 / 44.45$
3DH	$V7 + (V5 - V7) \times 24.3 / 44.45$	$V10 + (V8 - V10) \times 20.1 / 44.45$
3EH	$V7 + (V5 - V7) \times 20.1 / 44.45$	$V10 + (V8 - V10) \times 24.3 / 44.45$
3FH	V7	V8

## 6.5. Data Input Format



**Figure 8.** Vertical input timing



**Figure 9.** Horizontal input timing

## 6.6. DE mode and SYNC mode Input Timing (TA = 25°C, VDD = 3.3V)

6.6.1. For 800 × 480 panel (Dual gate mode /Cascade mode)

### I. Dual gate mode

**Table 16.** Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max	MHz	When user use SYNC mode. thb+thpw=88 DCLK is fixed.
		28.2	29.2	46.5		
1 Horizontal Line	th	908	928	1088		
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	40	200		

**Table 17.** Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	480			H	
VSD period time	tv	517	525	712	H	When user use SYNC mode. tvpw+tvb=32H is fixed.
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200	H	

### II. Cascade mode

**Table 18.** Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max	MHz	When user use SYNC mode. thb+thpw=88 DCLK is fixed.
		28.2	29.2	40		
1 Horizontal Line	th	908	928	1088		
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	40	200		

**Table 19.** Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	480			H	
VSD period time	tv	517	525	613	H	When user use SYNC mode. tvpw+tvb=32H is fixed.
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	101	H	

6.6.2. For 800 × 600 panel (Dual gate mode)

**Table 20.** Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max	MHz	
		35.1	39.6	50		
1 Horizontal Line	th	908	1000	1088	DCLK	When user use SYNC mode. thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	112	200		

**Table 21.** Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	600			H	
VSD period time	tv	644	660	766	H	When user use SYNC mode. tvpw+tvb=39H is fixed.
VSD pulse width	tvpw	1	1	3		
VSD Back Porch (Blanking)	tvb	38	38	36	H	
VSD Front Porch	tvfp	5	21	127		

6.6.3. For 400 × 480 panel (Dual gate mode)

**Table 22.** Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max	MHz	
		15.8	16.4	29.4		
1 Horizontal Line	th	508	520	688	DCLK	When user use SYNC mode. thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	32	200		

**Table 23.** Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	480			H	
VSD period time	tv	517	525	712	H	When user use SYNC mode. tvpw+tvb=32H is fixed.
VSD pulse width	tvpw	1	1	3		
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200		

6.6.4. For 400 × 240 panel (Dual gate mode)

**Table 24.** Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		8	8.4	18.9	MHz	
1 Horizontal Line	th	508	520	688	DCLK	When user use SYNC mode. thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	47		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	32	200		

**Table 25.** Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	240			H	
VSD period time	tv	262	270	457	H	
VSD pulse width	tvpw	1	1	3	H	When user use SYNC mode. tvpw+tvb=17H is fixed.
VSD Back Porch (Blanking)	tvb	16	16	14	H	
VSD Front Porch	tvfp	5	13	200	H	

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**7. ELECTRICAL SPECIFICATION****7.1. Absolute Maximum Ratings****Table 26.** VOLTAGE (TA = 25°C, VSS = VSSA = 0V)

	Min.	Max.	Unit
Digital Supply Voltage, VDD	-0.5	+5.0	V
Analog Supply Voltage, VDDA, V1~V14	-0.5	+15.0	V

**Table 27.** TEMPERATURE

	Min.	Max.	Unit
Operating temperature	-20	+85	°C
Storage temperature	-55	+125	°C

**Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

**7.2. Recommended Operating Range****Table 28.** Recommended Operating Range (TA = -20 to 85°C, VSS = VSSA = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage(Dual gate)	VDD	1.7	3.3	3.6	V
Digital supply voltage(Cascade)	VDD	1.7	3.3	3.6	V
Analog supply voltage	VDDA	6.5	-	13.5	V
Digital input voltage	VIN	0	-	VDD	V

## 7.3. DC Characteristics

**Table 29.** DC Characteristics

(TA = -20 to 85°C, VDD = 1.7 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	µA
High level output voltage	Voh	IoH = -400 µA	VDD-0.4	-	-	V
Low level output voltage	Vol	IoL = +400 mA	-	-	VSS+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD=3.3V	200K	250K	300K	ohm
Digital Operation current	Idd	Fclk=50 MHz, FLD=48KHz, VDD=3.3V	-	14	18	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	µA
Analog Operating Current	Idda	No load, Fclk=50MHz, FLD=48KHz @ VDDA=10V, V1=8V, V14=0.4V	-	7	12	mA
Analog Stand-by current	Ist2	No load, Clock and all functions are stopped	-	10	50	µA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input(Cascade Mode)	0.4×VDDA	-	VDDA-1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input(Cascade Mode)	VSSA+1	-	0.6×VDDA	V
Input level of V1 ~ V7	Vref3	Gamma correction voltage input(Dual Gate Mode)	0.4×VDDA	-	VDDA-0.1	V
Input level of V8 ~ V14	Vref4	Gamma correction voltage input(Dual Gate Mode)	VSSA+0.1	-	0.6×VDDA	V
Output Voltage deviation	Vod1	Vo = VSSA+0.1V ~ VSSA+0.5V and Vo = VDDA-0.5V ~ VDDA-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = VSSA+0.5V ~ VDDA-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = VSSA+0.5V ~ VDDA-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ SO1200	0.1	-	VDDA-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ SO1200; Vo=0.1V v.s 1.0V , VDDA=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ SO1200; Vo=13.4V v.s 12.5V , VDDA=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7×Rn	1.0×Rn	1.3×Rn	ohm

## 7.4. AC Characteristics

**Table 30.** AC Characteristics

(TA = -20 to 85°C, VDD = 1.7 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

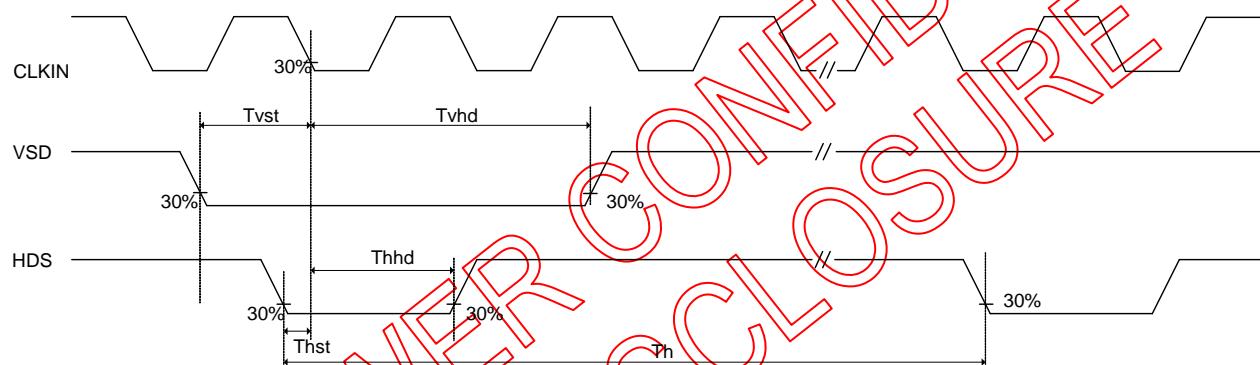
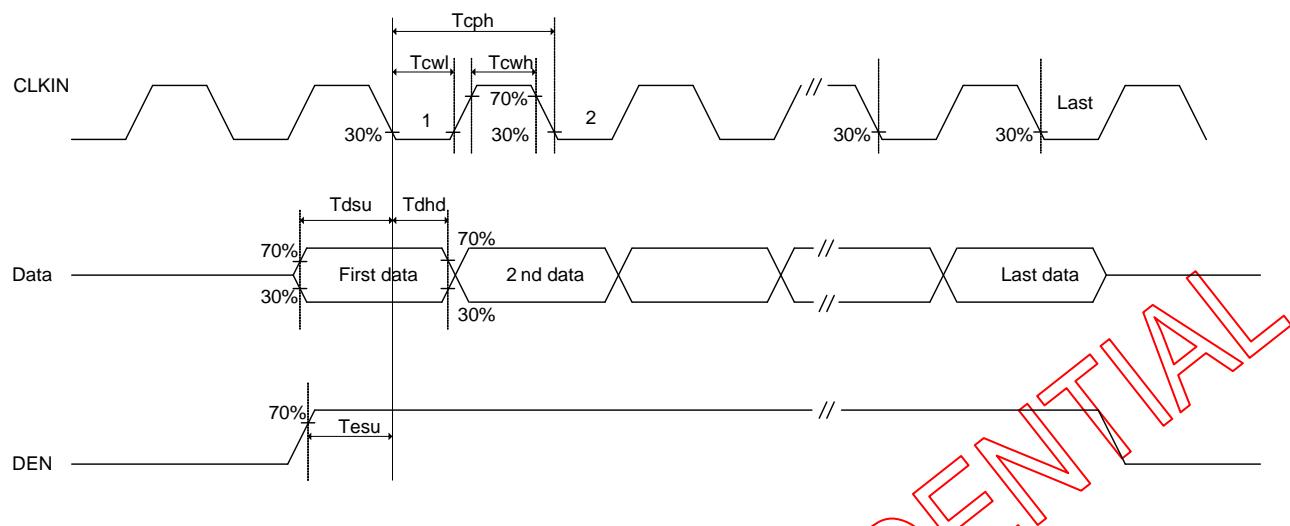
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD Power On Slew rate	T <sub>POR</sub>	From 0V to 90% VDD	-	-	20	ms
RSTB pulse width	T <sub>RST</sub>	CLKIN = 50MHz	50	-	-	us
CLKIN cycle time	T <sub>Cph</sub>	-	20	-	-	ns
CLKIN pulse duty	T <sub>cwh</sub>	-	40	50	60	%
VSD setup time	T <sub>vst</sub>	-	8	-	-	ns
VSD hold time	T <sub>vh</sub>	-	8	-	-	ns
HSD setup time	T <sub>hst</sub>	-	8	-	-	ns
HSD hold time	T <sub>hh</sub>	-	8	-	-	ns
Data set-up time	T <sub>dsu</sub>	DR[7:0], DG[7:0], DB[7:0] to CLKIN	8	-	-	ns
Data hold time	T <sub>dhd</sub>	DR[7:0], DG[7:0], DB[7:0] to CLKIN	8	-	-	ns
DEN setup time	T <sub>esu</sub>	-	8	-	-	ns
DEN hold time	T <sub>ehd</sub>	-	8	-	-	ns
Output stable time	T <sub>sst</sub>	10% to 90% target voltage. CL=120pF, R=10K ohm	-	6	-	us

## 7.5. Timing Table

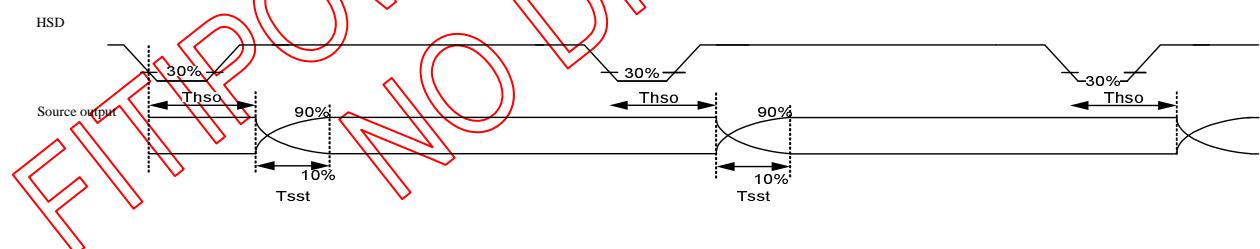
**Table 31.** Parallel 24-bit RGB Mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKIN Frequency(Dual gate)	F <sub>clk</sub>	VDD = 3.3V	-	29.2	46.5	MHz
CLKIN Cycle Time(Dual gate)	T <sub>clk</sub>	-	22	34	-	ns
CLKIN Frequency(cascade)	F <sub>clk</sub>	VDD = 3.3V	-	29.2	40	MHz
CLKIN Cycle Time(cascade)	T <sub>clk</sub>	-	25	34	-	ns
CLKIN Pulse Duty	T <sub>cwh</sub>	T <sub>clk</sub>	40	50	60	%
Time from HSD to Source Output	T <sub>hs</sub>	-	-	46	-	CLKIN
Time from HSD to LD	T <sub>hl</sub>	-	-	46	-	CLKIN
Time from HSD to STV	T <sub>hstv</sub>	-	-	2	-	CLKIN
Time from HSD to CKV	T <sub>hckv</sub>	-	-	20	-	CLKIN
Time from HSD to OEV	T <sub>hoev</sub>	-	-	4	-	CLKIN
LD Pulse Width	T <sub>wld</sub>	-	-	10	-	CLKIN
CKV Pulse Width	T <sub>wckv</sub>	-	-	66	-	CLKIN
OEV Pulse Width	T <sub>woev</sub>	-	-	74	-	CLKIN

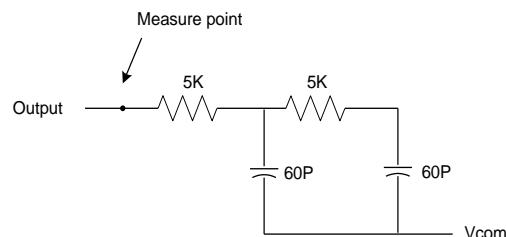
## 7.6. Timing Waveform



**Figure 10.** Input Clock and Data Timing Diagram



**Figure 11.** Source Output Timing Diagram(Cascade)



**Figure 12.** Output load condition

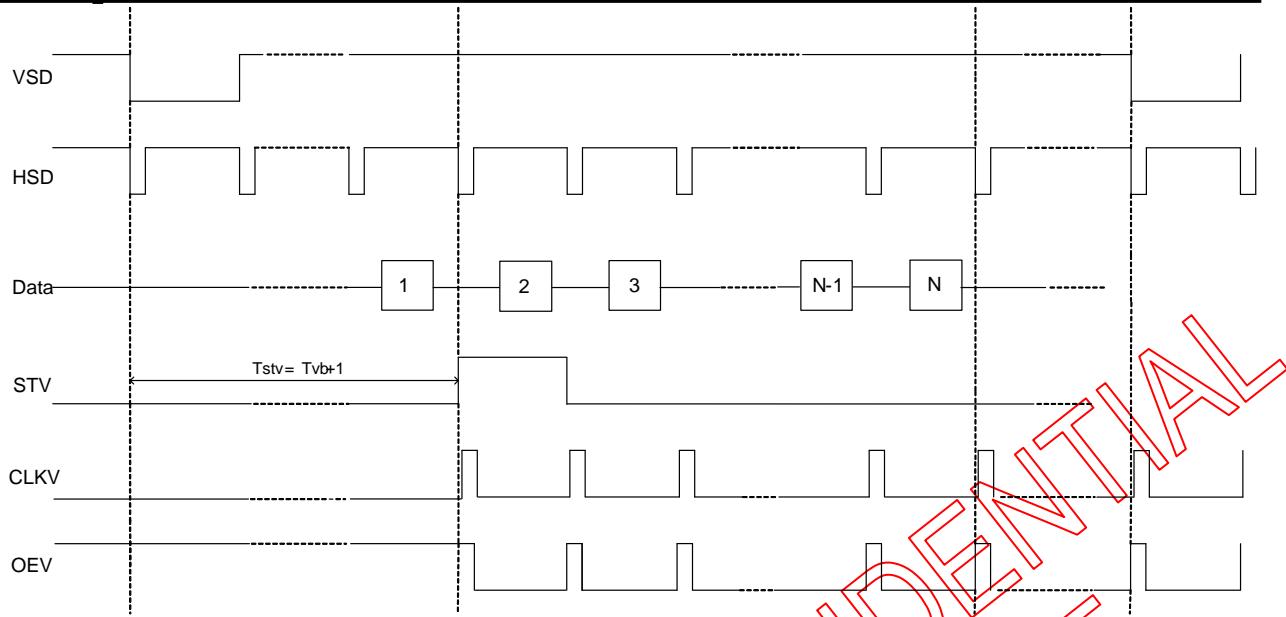


Figure 13. Vertical Timing Diagram HV (Cascade)

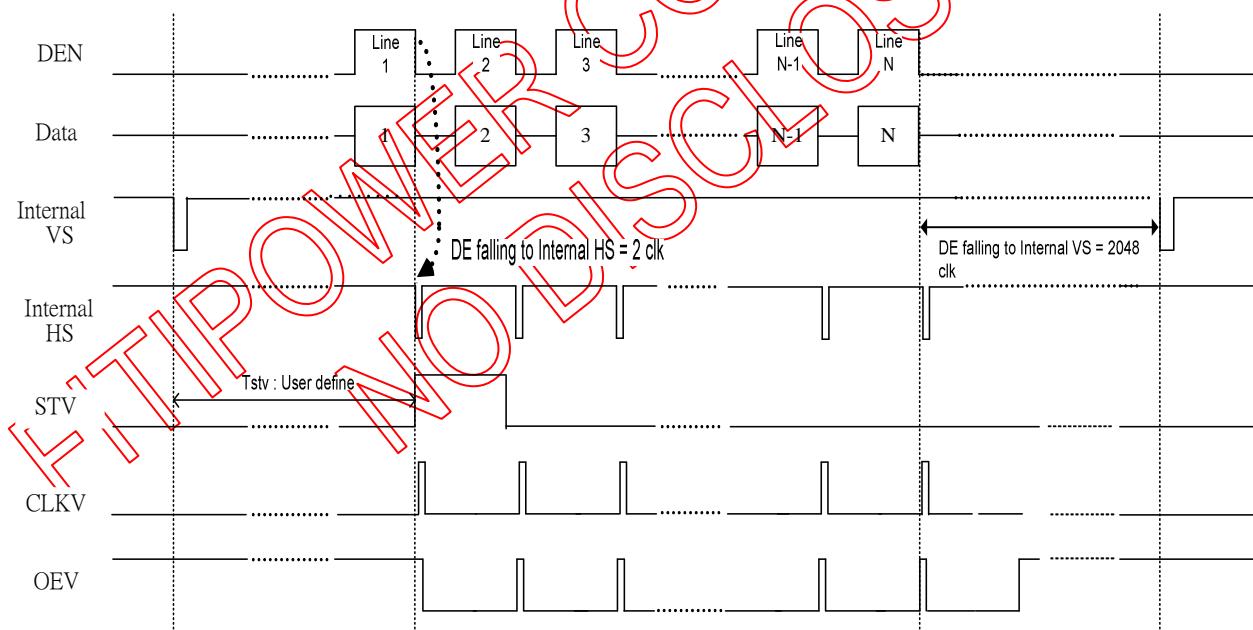
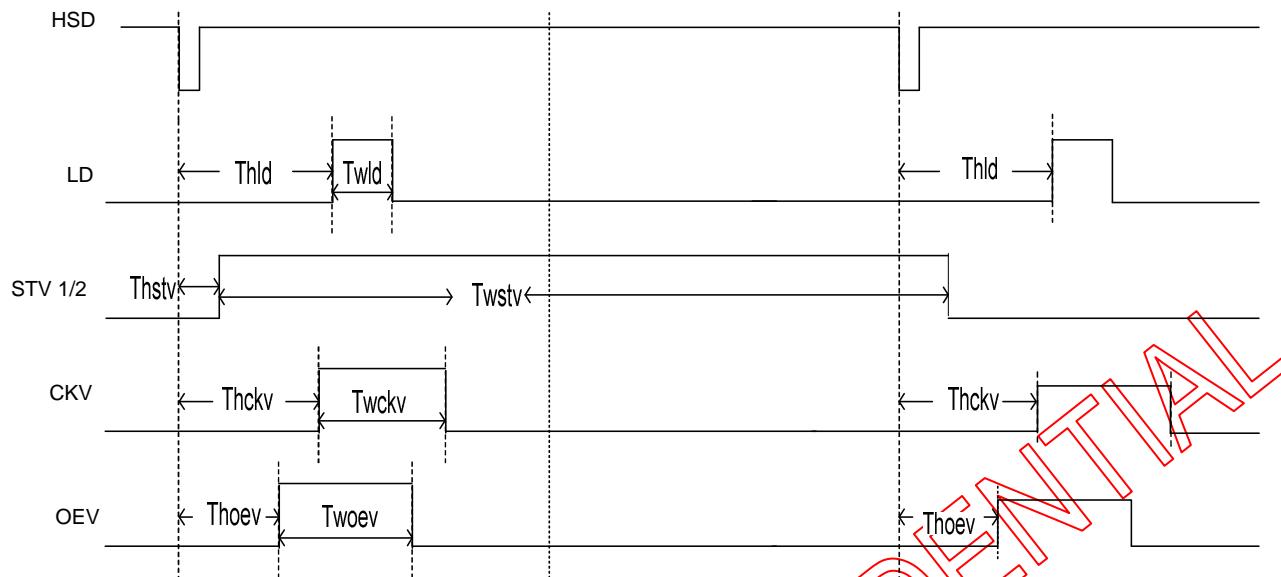
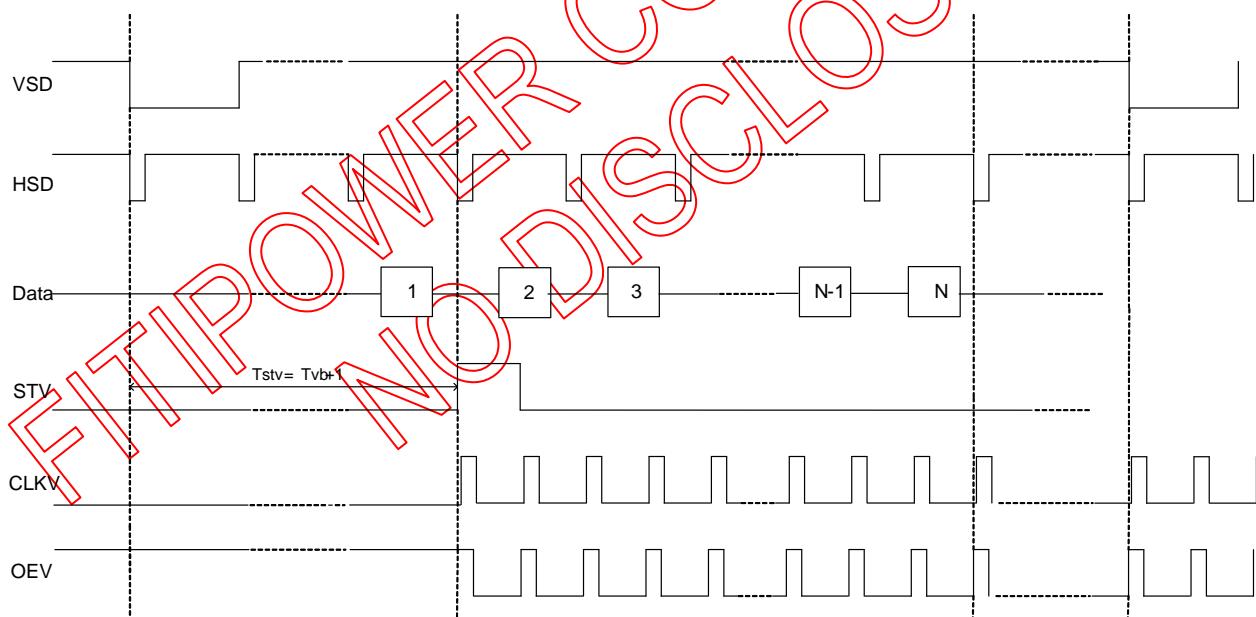


Figure 14. Vertical Timing Diagram DE (Cascade)



**Figure 15.** Gate Output Timing Diagram (Cascade)



**Figure 16.** Vertical Timing Diagram HV (Dual Gate)

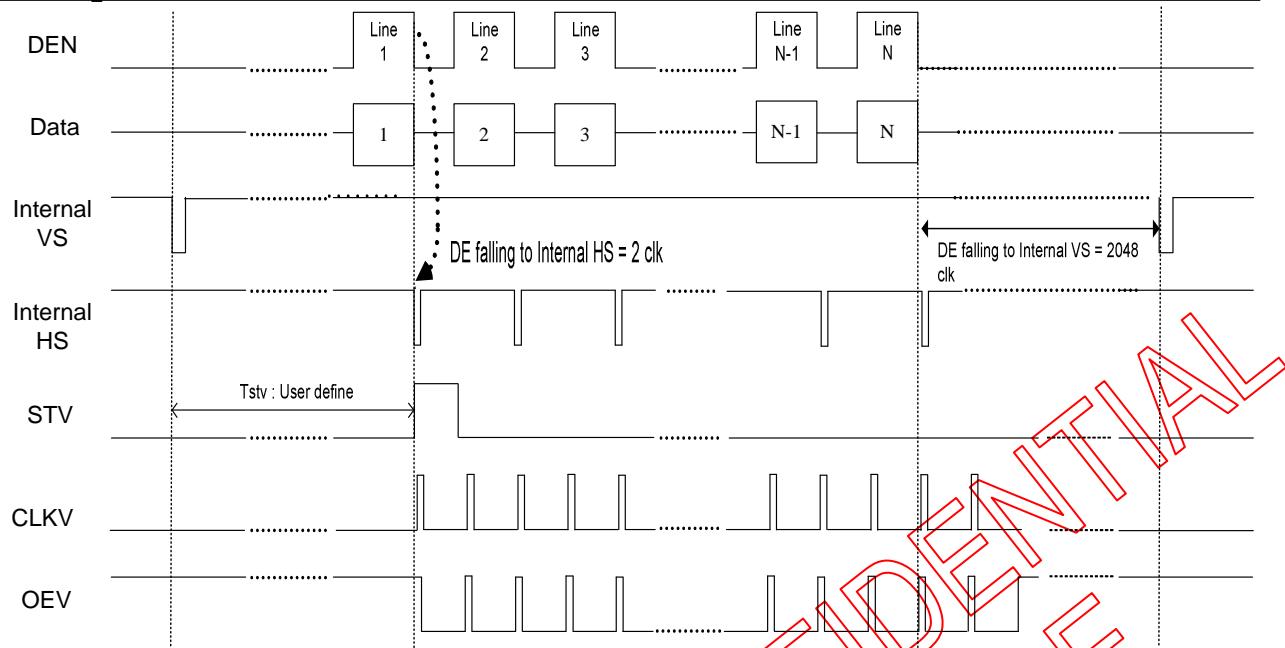


Figure 17. Vertical Timing Diagram DE (Dual Gate)

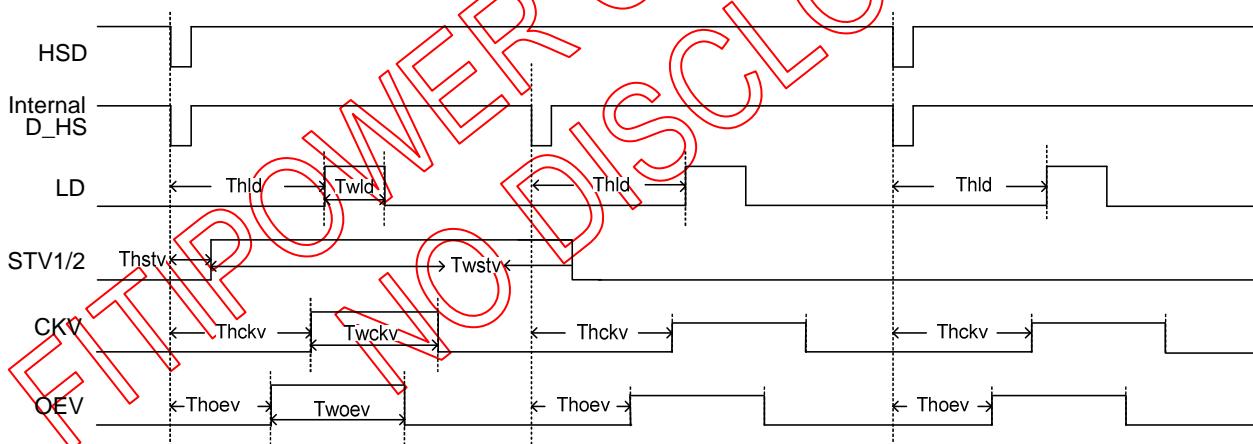
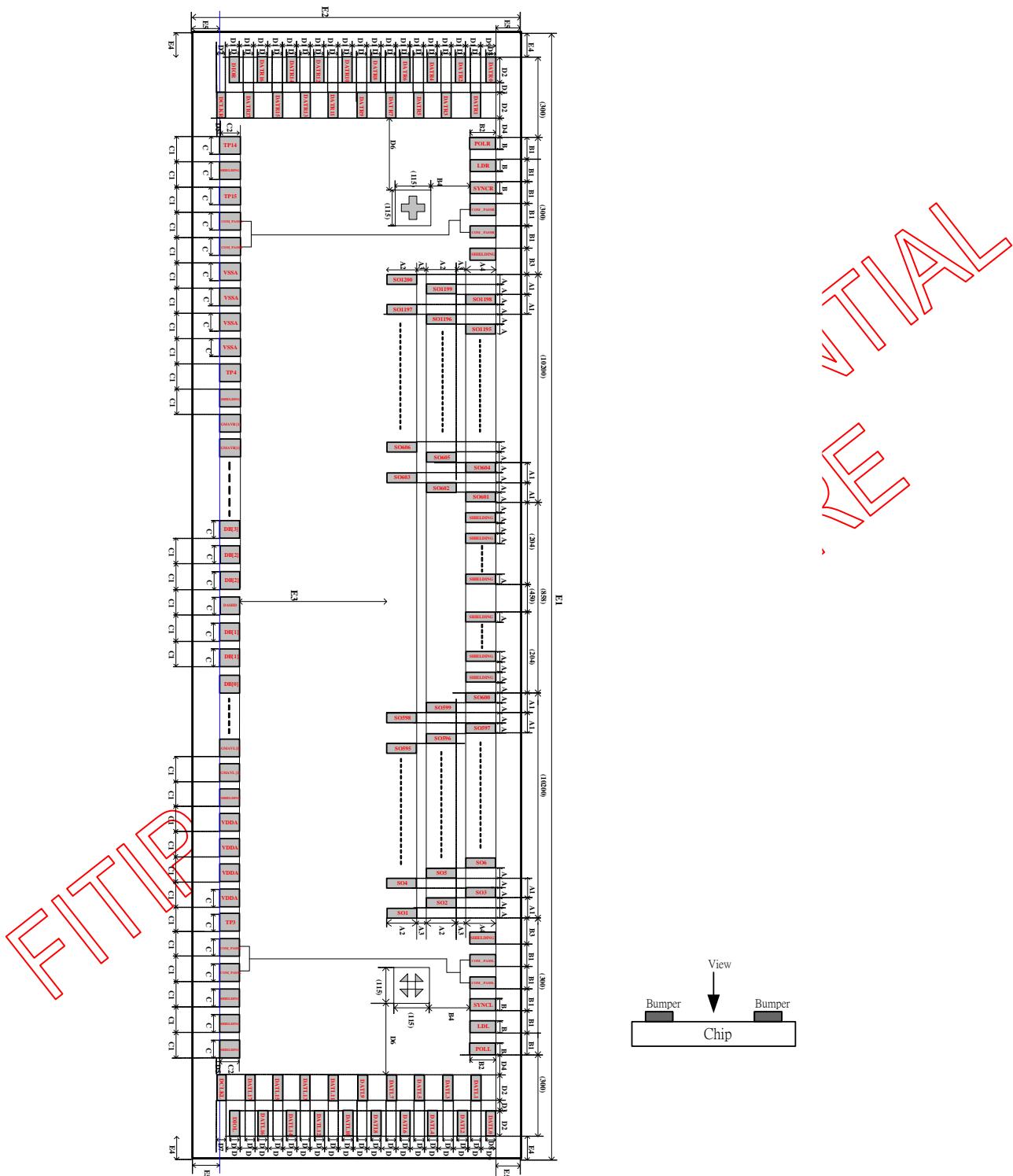
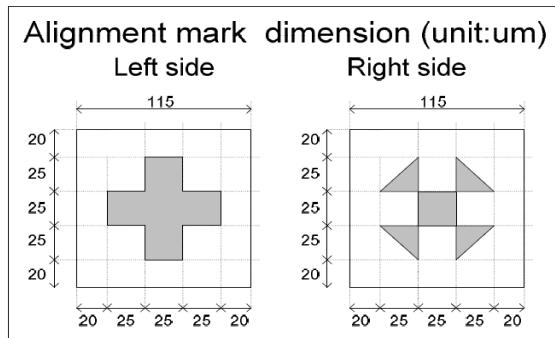


Figure 18. Gate Output Timing Diagram (Dual Gate)

## 8. PAD OUTLINE DIMENSION



**Figure 19.** Pad Outline Dimension (Bump Side)

**8.1. Alignment Mark****Figure 20. Alignment Mark****8.2. Pad Information**

Symbol	Dimension(um)
A	14
A1	34
A2	65
A3	71
A4	65
B	26
B1	50
B2	50
B3	49.5
B4	197.5
C	40
C1	85
C2	60
D	26

Symbol	Dimension(um)
D1	40
D2	50
D3	80
D4	97
D5	6.5
D6	193.5
D7	26
D8	23.5
D9	35.5
E1	22557 (max) *
E2	873 (max) *
E4	74.5(max)
E5	46(max)

\*Note : Chip dimension (not include scribe line)













PAD No.	PAD Name	X-axis	Y-axis	W	H
721	SO[437]	3208.5	202	14	65
722	SO[438]	3191.5	338	14	65
723	SO[439]	3174.5	62	14	65
724	SO[440]	3157.5	202	14	65
725	SO[441]	3140.5	338	14	65
726	SO[442]	3123.5	62	14	65
727	SO[443]	3106.5	202	14	65
728	SO[444]	3089.5	338	14	65
729	SO[445]	3072.5	62	14	65
730	SO[446]	3055.5	202	14	65
731	SO[447]	3038.5	338	14	65
732	SO[448]	3021.5	62	14	65
733	SO[449]	3004.5	202	14	65
734	SO[450]	2987.5	338	14	65
735	SO[451]	2970.5	62	14	65
736	SO[452]	2953.5	202	14	65
737	SO[453]	2936.5	338	14	65
738	SO[454]	2919.5	62	14	65
739	SO[455]	2902.5	202	14	65
740	SO[456]	2885.5	338	14	65
741	SO[457]	2868.5	62	14	65
742	SO[458]	2851.5	202	14	65
743	SO[459]	2834.5	338	14	65
744	SO[460]	2817.5	62	14	65
745	SO[461]	2800.5	202	14	65
746	SO[462]	2783.5	338	14	65
747	SO[463]	2766.5	62	14	65
748	SO[464]	2749.5	202	14	65
749	SO[465]	2732.5	338	14	65
750	SO[466]	2715.5	62	14	65
751	SO[467]	2698.5	202	14	65
752	SO[468]	2681.5	338	14	65
753	SO[469]	2664.5	62	14	65
754	SO[470]	2647.5	202	14	65
755	SO[471]	2630.5	338	14	65
756	SO[472]	2613.5	62	14	65
757	SO[473]	2596.5	202	14	65
758	SO[474]	2579.5	338	14	65
759	SO[475]	2562.5	62	14	65
760	SO[476]	2545.5	202	14	65
761	SO[477]	2528.5	338	14	65
762	SO[478]	2511.5	62	14	65
763	SO[479]	2494.5	202	14	65
764	SO[480]	2477.5	338	14	65
765	SO[481]	2460.5	62	14	65
766	SO[482]	2443.5	202	14	65
767	SO[483]	2426.5	338	14	65
768	SO[484]	2409.5	62	14	65
769	SO[485]	2392.5	202	14	65
770	SO[486]	2375.5	338	14	65
771	SO[487]	2358.5	62	14	65
772	SO[488]	2341.5	202	14	65
773	SO[489]	2324.5	338	14	65
774	SO[490]	2307.5	62	14	65
775	SO[491]	2290.5	202	14	65
776	SO[492]	2273.5	338	14	65
777	SO[493]	2256.5	62	14	65
778	SO[494]	2239.5	202	14	65
779	SO[495]	2222.5	338	14	65
780	SO[496]	2205.5	62	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
781	SO[497]	2188.5	202	14	65
782	SO[498]	2171.5	338	14	65
783	SO[499]	2154.5	62	14	65
784	SO[500]	2137.5	202	14	65
785	SO[501]	2120.5	338	14	65
786	SO[502]	2103.5	62	14	65
787	SO[503]	2086.5	202	14	65
788	SO[504]	2069.5	338	14	65
789	SO[505]	2052.5	62	14	65
790	SO[506]	2035.5	202	14	65
791	SO[507]	2018.5	338	14	65
792	SO[508]	2001.5	62	14	65
793	SO[509]	1984.5	202	14	65
794	SO[510]	1967.5	338	14	65
795	SO[511]	1950.5	62	14	65
796	SO[512]	1933.5	202	14	65
797	SO[513]	1916.5	338	14	65
798	SO[514]	1899.5	62	14	65
799	SO[515]	1882.5	202	14	65
800	SO[516]	1865.5	338	14	65
801	SO[517]	1848.5	62	14	65
802	SO[518]	1831.5	202	14	65
803	SO[519]	1814.5	338	14	65
804	SO[520]	1797.5	62	14	65
805	SO[521]	1780.5	202	14	65
806	SO[522]	1763.5	338	14	65
807	SO[523]	1746.5	62	14	65
808	SO[524]	1729.5	202	14	65
809	SO[525]	1712.5	338	14	65
810	SO[526]	1695.5	62	14	65
811	SO[527]	1678.5	202	14	65
812	SO[528]	1661.5	338	14	65
813	SO[529]	1644.5	62	14	65
814	SO[530]	1627.5	202	14	65
815	SO[531]	1610.5	338	14	65
816	SO[532]	1593.5	62	14	65
817	SO[533]	1576.5	202	14	65
818	SO[534]	1559.5	338	14	65
819	SO[535]	1542.5	62	14	65
820	SO[536]	1525.5	202	14	65
821	SO[537]	1508.5	338	14	65
822	SO[538]	1491.5	62	14	65
823	SO[539]	1474.5	202	14	65
824	SO[540]	1457.5	338	14	65
825	SO[541]	1440.5	62	14	65
826	SO[542]	1423.5	202	14	65
827	SO[543]	1406.5	338	14	65
828	SO[544]	1389.5	62	14	65
829	SO[545]	1372.5	202	14	65
830	SO[546]	1355.5	338	14	65
831	SO[547]	1338.5	62	14	65
832	SO[548]	1321.5	202	14	65
833	SO[549]	1304.5	338	14	65
834	SO[550]	1287.5	62	14	65
835	SO[551]	1270.5	202	14	65
836	SO[552]	1253.5	338	14	65
837	SO[553]	1236.5	62	14	65
838	SO[554]	1219.5	202	14	65
839	SO[555]	1202.5	338	14	65
840	SO[556]	1185.5	62	14	65

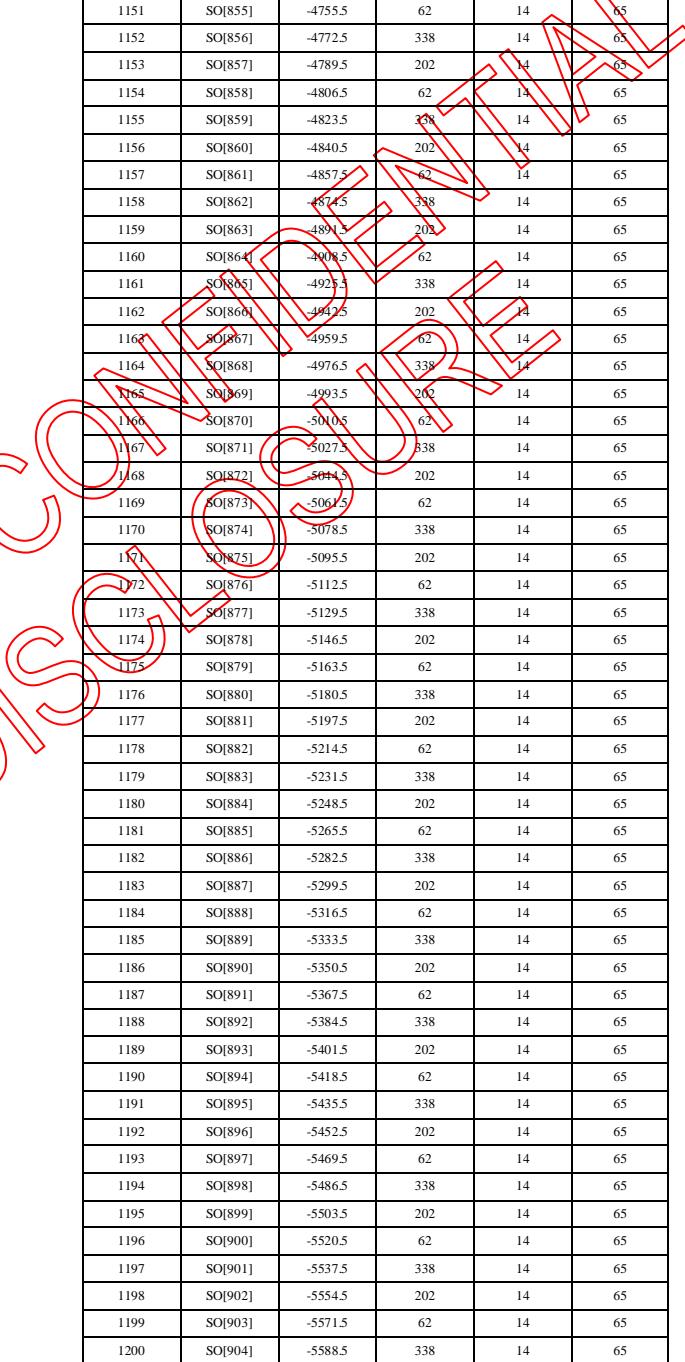
PAD No.	PAD Name	X-axis	Y-axis	W	H
841	SO[557]	1168.5	202	14	65
842	SO[558]	1151.5	338	14	65
843	SO[559]	1134.5	62	14	65
844	SO[560]	1117.5	202	14	65
845	SO[561]	1100.5	338	14	65
846	SO[562]	1083.5	62	14	65
847	SO[563]	1066.5	202	14	65
848	SO[564]	1049.5	338	14	65
849	SO[565]	1032.5	62	14	65
850	SO[566]	1015.5	202	14	65
851	SO[567]	998.5	338	14	65
852	SO[568]	981.5	62	14	65
853	SO[569]	964.5	202	14	65
854	SO[570]	947.5	338	14	65
855	SO[571]	930.5	62	14	65
856	SO[572]	913.5	202	14	65
857	SO[573]	896.5	338	14	65
858	SO[574]	879.5	62	14	65
859	SO[575]	862.5	202	14	65
860	SO[576]	845.5	338	14	65
861	SO[577]	828.5	62	14	65
862	SO[578]	811.5	202	14	65
863	SO[579]	794.5	338	14	65
864	SO[580]	777.5	62	14	65
865	SO[581]	760.5	202	14	65
866	SO[582]	743.5	338	14	65
867	SO[583]	726.5	62	14	65
868	SO[584]	709.5	202	14	65
869	SO[585]	692.5	338	14	65
870	SO[586]	675.5	62	14	65
871	SO[587]	658.5	202	14	65
872	SO[588]	641.5	338	14	65
873	SO[589]	624.5	62	14	65
874	SO[590]	607.5	202	14	65
875	SO[591]	590.5	338	14	65
876	SO[592]	573.5	62	14	65
877	SO[593]	556.5	202	14	65
878	SO[594]	539.5	338	14	65
879	SO[595]	522.5	62	14	65
880	SO[596]	505.5	202	14	65
881	SO[597]	488.5	338	14	65
882	SO[598]	471.5	62	14	65
883	SO[599]	454.5	202	14	65
884	SO[600]	437.5	338	14	65
885	SHIELDING[39]	403.5	338	14	65
886	SHIELDING[40]	369.5	338	14	65
887	SHIELDING[41]	335.5	338	14	65
888	SHIELDING[42]	301.5	338	14	65
889	SHIELDING[43]	267.5	338	14	65
890	SHIELDING[44]	233.5	338	14	65
891	SHIELDING[45]	-233.5	338	14	65
892	SHIELDING[46]	-267.5	338	14	65
893	SHIELDING[47]	-301.5	338	14	65
894	SHIELDING[48]	-335.5	338	14	65
895	SHIELDING[49]	-369.5	338	14	65
896	SHIELDING[50]	-403.5	338	14	65
897	SO[601]	-437.5	338	14	65
898	SO[602]	-454.5	202	14	65
899	SO[603]	-471.5	62	14	65
900	SO[604]	-488.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
901	SO[605]	-505.5	202	14	65
902	SO[606]	-522.5	62	14	65
903	SO[607]	-539.5	338	14	65
904	SO[608]	-556.5	202	14	65
905	SO[609]	-573.5	62	14	65
906	SO[610]	-590.5	338	14	65
907	SO[611]	-607.5	202	14	65
908	SO[612]	-624.5	62	14	65
909	SO[613]	-641.5	338	14	65
910	SO[614]	-658.5	202	14	65
911	SO[615]	-675.5	62	14	65
912	SO[616]	-692.5	338	14	65
913	SO[617]	-709.5	202	14	65
914	SO[618]	-726.5	62	14	65
915	SO[619]	-743.5	338	14	65
916	SO[620]	-760.5	202	14	65
917	SO[621]	-777.5	62	14	65
918	SO[622]	-794.5	338	14	65
919	SO[623]	-811.5	202	14	65
920	SO[624]	-828.5	62	14	65
921	SO[625]	-845.5	338	14	65
922	SO[626]	-862.5	202	14	65
922	SO[627]	-879.5	62	14	65
924	SO[628]	-896.5	338	14	65
925	SO[629]	-913.5	202	14	65
926	SO[630]	-930.5	62	14	65
927	SO[631]	-947.5	338	14	65
928	SO[632]	-964.5	202	14	65
929	SO[633]	-981.5	62	14	65
930	SO[634]	-998.5	338	14	65
931	SO[635]	-1015.5	202	14	65
932	SO[636]	-1032.5	62	14	65
933	SO[637]	-1049.5	338	14	65
934	SO[638]	-1066.5	202	14	65
935	SO[639]	-1083.5	62	14	65
936	SO[640]	-1100.5	338	14	65
937	SO[641]	-1117.5	202	14	65
938	SO[642]	-1134.5	62	14	65
939	SO[643]	-1151.5	338	14	65
940	SO[644]	-1168.5	202	14	65
941	SO[645]	-1185.5	62	14	65
942	SO[646]	-1202.5	338	14	65
943	SO[647]	-1219.5	202	14	65
944	SO[648]	-1236.5	62	14	65
945	SO[649]	-1253.5	338	14	65
946	SO[650]	-1270.5	202	14	65
947	SO[651]	-1287.5	62	14	65
948	SO[652]	-1304.5	338	14	65
949	SO[653]	-1321.5	202	14	65
950	SO[654]	-1338.5	62	14	65
951	SO[655]	-1355.5	338	14	65
952	SO[656]	-1372.5	202	14	65
953	SO[657]	-1389.5	62	14	65
954	SO[658]	-1406.5	338	14	65
955	SO[659]	-1423.5	202	14	65
956	SO[660]	-1440.5	62	14	65
957	SO[661]	-1457.5	338	14	65
958	SO[662]	-1474.5	202	14	65
959	SO[663]	-1491.5	62	14	65
960	SO[664]	-1508.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
961	SO[665]	-1525.5	202	14	65
962	SO[666]	-1542.5	62	14	65
963	SO[667]	-1559.5	338	14	65
964	SO[668]	-1576.5	202	14	65
965	SO[669]	-1593.5	62	14	65
966	SO[670]	-1610.5	338	14	65
967	SO[671]	-1627.5	202	14	65
968	SO[672]	-1644.5	62	14	65
969	SO[673]	-1661.5	338	14	65
970	SO[674]	-1678.5	202	14	65
971	SO[675]	-1695.5	62	14	65
972	SO[676]	-1712.5	338	14	65
973	SO[677]	-1729.5	202	14	65
974	SO[678]	-1746.5	62	14	65
975	SO[679]	-1763.5	338	14	65
976	SO[680]	-1780.5	202	14	65
977	SO[681]	-1797.5	62	14	65
978	SO[682]	-1814.5	338	14	65
979	SO[683]	-1831.5	202	14	65
980	SO[684]	-1848.5	62	14	65
981	SO[685]	-1865.5	338	14	65
982	SO[686]	-1882.5	202	14	65
983	SO[687]	-1899.5	62	14	65
984	SO[688]	-1916.5	338	14	65
985	SO[689]	-1933.5	202	14	65
986	SO[690]	-1950.5	62	14	65
987	SO[691]	-1967.5	338	14	65
988	SO[692]	-1984.5	202	14	65
989	SO[693]	-2001.5	62	14	65
990	SO[694]	-2018.5	338	14	65
991	SO[695]	-2035.5	202	14	65
992	SO[696]	-2052.5	62	14	65
993	SO[697]	-2069.5	338	14	65
994	SO[698]	-2086.5	202	14	65
995	SO[699]	-2103.5	62	14	65
996	SO[700]	-2120.5	338	14	65
997	SO[701]	-2137.5	202	14	65
998	SO[702]	-2154.5	62	14	65
999	SO[703]	-2171.5	338	14	65
1000	SO[704]	-2188.5	202	14	65
1001	SO[705]	-2205.5	62	14	65
1002	SO[706]	-2222.5	338	14	65
1003	SO[707]	-2239.5	202	14	65
1004	SO[708]	-2256.5	62	14	65
1005	SO[709]	-2273.5	338	14	65
1006	SO[710]	-2290.5	202	14	65
1007	SO[711]	-2307.5	62	14	65
1008	SO[712]	-2324.5	338	14	65
1009	SO[713]	-2341.5	202	14	65
1010	SO[714]	-2358.5	62	14	65
1011	SO[715]	-2375.5	338	14	65
1012	SO[716]	-2392.5	202	14	65
1013	SO[717]	-2409.5	62	14	65
1014	SO[718]	-2426.5	338	14	65
1015	SO[719]	-2443.5	202	14	65
1016	SO[720]	-2460.5	62	14	65
1017	SO[721]	-2477.5	338	14	65
1018	SO[722]	-2494.5	202	14	65
1019	SO[723]	-2511.5	62	14	65
1020	SO[724]	-2528.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1021	SO[725]	-2545.5	202	14	65
1022	SO[726]	-2562.5	62	14	65
1023	SO[727]	-2579.5	338	14	65
1024	SO[728]	-2596.5	202	14	65
1025	SO[729]	-2613.5	62	14	65
1026	SO[730]	-2630.5	338	14	65
1027	SO[731]	-2647.5	202	14	65
1028	SO[732]	-2664.5	62	14	65
1029	SO[733]	-2681.5	338	14	65
1030	SO[734]	-2698.5	202	14	65
1031	SO[735]	-2715.5	62	14	65
1032	SO[736]	-2732.5	338	14	65
1033	SO[737]	-2749.5	202	14	65
1034	SO[738]	-2766.5	62	14	65
1035	SO[739]	-2783.5	338	14	65
1036	SO[740]	-2800.5	202	14	65
1037	SO[741]	-2817.5	62	14	65
1038	SO[742]	-2834.5	338	14	65
1039	SO[743]	-2851.5	202	14	65
1040	SO[744]	-2868.5	62	14	65
1041	SO[745]	-2885.5	338	14	65
1042	SO[746]	-2902.5	202	14	65
1043	SO[747]	-2919.5	62	14	65
1044	SO[748]	-2936.5	338	14	65
1045	SO[749]	-2953.5	202	14	65
1046	SO[750]	-2970.5	62	14	65
1047	SO[751]	-2987.5	338	14	65
1048	SO[752]	-3004.5	202	14	65
1049	SO[753]	-3021.5	62	14	65
1050	SO[754]	-3038.5	338	14	65
1051	SO[755]	-3055.5	202	14	65
1052	SO[756]	-3072.5	62	14	65
1053	SO[757]	-3089.5	338	14	65
1054	SO[758]	-3106.5	202	14	65
1055	SO[759]	-3123.5	62	14	65
1056	SO[760]	-3140.5	338	14	65
1057	SO[761]	-3157.5	202	14	65
1058	SO[762]	-3174.5	62	14	65
1059	SO[763]	-3191.5	338	14	65
1060	SO[764]	-3208.5	202	14	65
1061	SO[765]	-3225.5	62	14	65
1062	SO[766]	-3242.5	338	14	65
1063	SO[767]	-3259.5	202	14	65
1064	SO[768]	-3276.5	62	14	65
1065	SO[769]	-3293.5	338	14	65
1066	SO[770]	-3310.5	202	14	65
1067	SO[771]	-3327.5	62	14	65
1068	SO[772]	-3344.5	338	14	65
1069	SO[773]	-3361.5	202	14	65
1070	SO[774]	-3378.5	62	14	65
1071	SO[775]	-3395.5	338	14	65
1072	SO[776]	-3412.5	202	14	65
1073	SO[777]	-3429.5	62	14	65
1074	SO[778]	-3446.5	338	14	65
1075	SO[779]	-3463.5	202	14	65
1076	SO[780]	-3480.5	62	14	65
1077	SO[781]	-3497.5	338	14	65
1078	SO[782]	-3514.5	202	14	65
1079	SO[783]	-3531.5	62	14	65
1080	SO[784]	-3548.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1081	SO[785]	-3565.5	202	14	65
1082	SO[786]	-3582.5	62	14	65
1083	SO[787]	-3599.5	338	14	65
1084	SO[788]	-3616.5	202	14	65
1085	SO[789]	-3633.5	62	14	65
1086	SO[790]	-3650.5	338	14	65
1087	SO[791]	-3667.5	202	14	65
1088	SO[792]	-3684.5	62	14	65
1089	SO[793]	-3701.5	338	14	65
1090	SO[794]	-3718.5	202	14	65
1091	SO[795]	-3735.5	62	14	65
1092	SO[796]	-3752.5	338	14	65
1093	SO[797]	-3769.5	202	14	65
1094	SO[798]	-3786.5	62	14	65
1095	SO[799]	-3803.5	338	14	65
1096	SO[800]	-3820.5	202	14	65
1097	SO[801]	-3837.5	62	14	65
1098	SO[802]	-3854.5	338	14	65
1099	SO[803]	-3871.5	202	14	65
1100	SO[804]	-3888.5	62	14	65
1101	SO[805]	-3905.5	338	14	65
1102	SO[806]	-3922.5	202	14	65
1103	SO[807]	-3939.5	62	14	65
1104	SO[808]	-3956.5	338	14	65
1105	SO[809]	-3973.5	202	14	65
1106	SO[810]	-3990.5	62	14	65
1107	SO[811]	-4007.5	338	14	65
1108	SO[812]	-4024.5	202	14	65
1109	SO[813]	-4041.5	62	14	65
1110	SO[814]	-4058.5	338	14	65
1111	SO[815]	-4075.5	202	14	65
1112	SO[816]	-4092.5	62	14	65
1113	SO[817]	-4109.5	338	14	65
1114	SO[818]	-4126.5	202	14	65
1115	SO[819]	-4143.5	62	14	65
1116	SO[820]	-4160.5	338	14	65
1117	SO[821]	-4177.5	202	14	65
1118	SO[822]	-4194.5	62	14	65
1119	SO[823]	-4211.5	338	14	65
1120	SO[824]	-4228.5	202	14	65
1121	SO[825]	-4245.5	62	14	65
1122	SO[826]	-4262.5	338	14	65
1123	SO[827]	-4279.5	202	14	65
1124	SO[828]	-4296.5	62	14	65
1125	SO[829]	-4313.5	338	14	65
1126	SO[830]	-4330.5	202	14	65
1127	SO[831]	-4347.5	62	14	65
1128	SO[832]	-4364.5	338	14	65
1129	SO[833]	-4381.5	202	14	65
1130	SO[834]	-4398.5	62	14	65
1131	SO[835]	-4415.5	338	14	65
1132	SO[836]	-4432.5	202	14	65
1133	SO[837]	-4449.5	62	14	65
1134	SO[838]	-4466.5	338	14	65
1135	SO[839]	-4483.5	202	14	65
1136	SO[840]	-4500.5	62	14	65
1137	SO[841]	-4517.5	338	14	65
1138	SO[842]	-4534.5	202	14	65
1139	SO[843]	-4551.5	62	14	65
1140	SO[844]	-4568.5	338	14	65



PAD No.	PAD Name	X-axis	Y-axis	W	H
1141	SO[845]	-4585.5	202	14	65
1142	SO[846]	-4602.5	62	14	65
1143	SO[847]	-4619.5	338	14	65
1144	SO[848]	-4636.5	202	14	65
1145	SO[849]	-4653.5	62	14	65
1146	SO[850]	-4670.5	338	14	65
1147	SO[851]	-4687.5	202	14	65
1148	SO[852]	-4704.5	62	14	65
1149	SO[853]	-4721.5	338	14	65
1150	SO[854]	-4738.5	202	14	65
1151	SO[855]	-4755.5	62	14	65
1152	SO[856]	-4772.5	338	14	65
1153	SO[857]	-4789.5	202	14	65
1154	SO[858]	-4806.5	62	14	65
1155	SO[859]	-4823.5	338	14	65
1156	SO[860]	-4840.5	202	14	65
1157	SO[861]	-4857.5	62	14	65
1158	SO[862]	-4874.5	338	14	65
1159	SO[863]	-4891.5	202	14	65
1160	SO[864]	-4908.5	62	14	65
1161	SO[865]	-4925.5	338	14	65
1162	SO[866]	-4942.5	202	14	65
1163	SO[867]	-4959.5	62	14	65
1164	SO[868]	-4976.5	338	14	65
1165	SO[869]	-4993.5	202	14	65
1166	SO[870]	-5010.5	62	14	65
1167	SO[871]	-5027.5	338	14	65
1168	SO[872]	-5044.5	202	14	65
1169	SO[873]	-5061.5	62	14	65
1170	SO[874]	-5078.5	338	14	65
1171	SO[875]	-5095.5	202	14	65
1172	SO[876]	-5112.5	62	14	65
1173	SO[877]	-5129.5	338	14	65
1174	SO[878]	-5146.5	202	14	65
1175	SO[879]	-5163.5	62	14	65
1176	SO[880]	-5180.5	338	14	65
1177	SO[881]	-5197.5	202	14	65
1178	SO[882]	-5214.5	62	14	65
1179	SO[883]	-5231.5	338	14	65
1180	SO[884]	-5248.5	202	14	65
1181	SO[885]	-5265.5	62	14	65
1182	SO[886]	-5282.5	338	14	65
1183	SO[887]	-5299.5	202	14	65
1184	SO[888]	-5316.5	62	14	65
1185	SO[889]	-5333.5	338	14	65
1186	SO[890]	-5350.5	202	14	65
1187	SO[891]	-5367.5	62	14	65
1188	SO[892]	-5384.5	338	14	65
1189	SO[893]	-5401.5	202	14	65
1190	SO[894]	-5418.5	62	14	65
1191	SO[895]	-5435.5	338	14	65
1192	SO[896]	-5452.5	202	14	65
1193	SO[897]	-5469.5	62	14	65
1194	SO[898]	-5486.5	338	14	65
1195	SO[899]	-5503.5	202	14	65
1196	SO[900]	-5520.5	62	14	65
1197	SO[901]	-5537.5	338	14	65
1198	SO[902]	-5554.5	202	14	65
1199	SO[903]	-5571.5	62	14	65
1200	SO[904]	-5588.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1201	SO[905]	-5605.5	202	14	65
1202	SO[906]	-5622.5	62	14	65
1203	SO[907]	-5639.5	338	14	65
1204	SO[908]	-5656.5	202	14	65
1205	SO[909]	-5673.5	62	14	65
1206	SO[910]	-5690.5	338	14	65
1207	SO[911]	-5707.5	202	14	65
1208	SO[912]	-5724.5	62	14	65
1209	SO[913]	-5741.5	338	14	65
1210	SO[914]	-5758.5	202	14	65
1211	SO[915]	-5775.5	62	14	65
1212	SO[916]	-5792.5	338	14	65
1213	SO[917]	-5809.5	202	14	65
1214	SO[918]	-5826.5	62	14	65
1215	SO[919]	-5843.5	338	14	65
1216	SO[920]	-5860.5	202	14	65
1217	SO[921]	-5877.5	62	14	65
1218	SO[922]	-5894.5	338	14	65
1219	SO[923]	-5911.5	202	14	65
1220	SO[924]	-5928.5	62	14	65
1221	SO[925]	-5945.5	338	14	65
1222	SO[926]	-5962.5	202	14	65
1223	SO[927]	-5979.5	62	14	65
1224	SO[928]	-5996.5	338	14	65
1225	SO[929]	-6013.5	202	14	65
1226	SO[930]	-6030.5	62	14	65
1227	SO[931]	-6047.5	338	14	65
1228	SO[932]	-6064.5	202	14	65
1229	SO[933]	-6081.5	62	14	65
1230	SO[934]	-6098.5	338	14	65
1231	SO[935]	-6115.5	202	14	65
1232	SO[936]	-6132.5	62	14	65
1233	SO[937]	-6149.5	338	14	65
1234	SO[938]	-6166.5	202	14	65
1235	SO[939]	-6183.5	62	14	65
1236	SO[940]	-6200.5	338	14	65
1237	SO[941]	-6217.5	202	14	65
1238	SO[942]	-6234.5	62	14	65
1239	SO[943]	-6251.5	338	14	65
1240	SO[944]	-6268.5	202	14	65
1241	SO[945]	-6285.5	62	14	65
1242	SO[946]	-6302.5	338	14	65
1243	SO[947]	-6319.5	202	14	65
1244	SO[948]	-6336.5	62	14	65
1245	SO[949]	-6353.5	338	14	65
1246	SO[950]	-6370.5	202	14	65
1247	SO[951]	-6387.5	62	14	65
1248	SO[952]	-6404.5	338	14	65
1249	SO[953]	-6421.5	202	14	65
1250	SO[954]	-6438.5	62	14	65
1251	SO[955]	-6455.5	338	14	65
1252	SO[956]	-6472.5	202	14	65
1253	SO[957]	-6489.5	62	14	65
1254	SO[958]	-6506.5	338	14	65
1255	SO[959]	-6523.5	202	14	65
1256	SO[960]	-6540.5	62	14	65
1257	SO[961]	-6557.5	338	14	65
1258	SO[962]	-6574.5	202	14	65
1259	SO[963]	-6591.5	62	14	65
1260	SO[964]	-6608.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1261	SO[965]	-6625.5	202	14	65
1262	SO[966]	-6642.5	62	14	65
1263	SO[967]	-6659.5	338	14	65
1264	SO[968]	-6676.5	202	14	65
1265	SO[969]	-6693.5	62	14	65
1266	SO[970]	-6710.5	338	14	65
1267	SO[971]	-6727.5	202	14	65
1268	SO[972]	-6744.5	62	14	65
1269	SO[973]	-6761.5	338	14	65
1270	SO[974]	-6778.5	202	14	65
1271	SO[975]	-6795.5	62	14	65
1272	SO[976]	-6812.5	338	14	65
1273	SO[977]	-6829.5	202	14	65
1274	SO[978]	-6846.5	62	14	65
1275	SO[979]	-6863.5	338	14	65
1276	SO[980]	-6880.5	202	14	65
1277	SO[981]	-6897.5	62	14	65
1278	SO[982]	-6914.5	338	14	65
1279	SO[983]	-6931.5	202	14	65
1280	SO[984]	-6948.5	62	14	65
1281	SO[985]	-6965.5	338	14	65
1282	SO[986]	-6982.5	202	14	65
1283	SO[987]	-6999.5	62	14	65
1284	SO[988]	-7016.5	338	14	65
1285	SO[989]	-7033.5	202	14	65
1286	SO[990]	-7050.5	62	14	65
1287	SO[991]	-7067.5	338	14	65
1288	SO[992]	-7084.5	202	14	65
1289	SO[993]	-7101.5	62	14	65
1290	SO[994]	-7118.5	338	14	65
1291	SO[995]	-7135.5	202	14	65
1292	SO[996]	-7152.5	62	14	65
1293	SO[997]	-7169.5	338	14	65
1294	SO[998]	-7186.5	202	14	65
1295	SO[999]	-7203.5	62	14	65
1296	SO[1000]	-7220.5	338	14	65
1297	SO[1001]	-7237.5	202	14	65
1298	SO[1002]	-7254.5	62	14	65
1299	SO[1003]	-7271.5	338	14	65
1300	SO[1004]	-7288.5	202	14	65
1301	SO[1005]	-7305.5	62	14	65
1302	SO[1006]	-7322.5	338	14	65
1303	SO[1007]	-7339.5	202	14	65
1304	SO[1008]	-7356.5	62	14	65
1305	SO[1009]	-7373.5	338	14	65
1306	SO[1010]	-7390.5	202	14	65
1307	SO[1011]	-7407.5	62	14	65
1308	SO[1012]	-7424.5	338	14	65
1309	SO[1013]	-7441.5	202	14	65
1310	SO[1014]	-7458.5	62	14	65
1311	SO[1015]	-7475.5	338	14	65
1312	SO[1016]	-7492.5	202	14	65
1313	SO[1017]	-7509.5	62	14	65
1314	SO[1018]	-7526.5	338	14	65
1315	SO[1019]	-7543.5	202	14	65
1316	SO[1020]	-7560.5	62	14	65
1317	SO[1021]	-7577.5	338	14	65
1318	SO[1022]	-7594.5	202	14	65
1319	SO[1023]	-7611.5	62	14	65
1320	SO[1024]	-7628.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1321	SO[1025]	-7645.5	202	14	65
1322	SO[1026]	-7662.5	62	14	65
1323	SO[1027]	-7679.5	338	14	65
1324	SO[1028]	-7696.5	202	14	65
1325	SO[1029]	-7713.5	62	14	65
1326	SO[1030]	-7730.5	338	14	65
1327	SO[1031]	-7747.5	202	14	65
1328	SO[1032]	-7764.5	62	14	65
1329	SO[1033]	-7781.5	338	14	65
1330	SO[1034]	-7798.5	202	14	65
1331	SO[1035]	-7815.5	62	14	65
1332	SO[1036]	-7832.5	338	14	65
1333	SO[1037]	-7849.5	202	14	65
1334	SO[1038]	-7866.5	62	14	65
1335	SO[1039]	-7883.5	338	14	65
1336	SO[1040]	-7900.5	202	14	65
1337	SO[1041]	-7917.5	62	14	65
1338	SO[1042]	-7934.5	338	14	65
1339	SO[1043]	-7951.5	202	14	65
1340	SO[1044]	-7968.5	62	14	65
1341	SO[1045]	-7985.5	338	14	65
1342	SO[1046]	-8002.5	202	14	65
1343	SO[1047]	-8019.5	62	14	65
1344	SO[1048]	-8036.5	338	14	65
1345	SO[1049]	-8053.5	202	14	65
1346	SO[1050]	-8070.5	62	14	65
1347	SO[1051]	-8087.5	338	14	65
1348	SO[1052]	-8104.5	202	14	65
1349	SO[1053]	-8121.5	62	14	65
1350	SO[1054]	-8138.5	338	14	65
1351	SO[1055]	-8155.5	202	14	65
1352	SO[1056]	-8172.5	62	14	65
1353	SO[1057]	-8189.5	338	14	65
1354	SO[1058]	-8206.5	202	14	65
1355	SO[1059]	-8223.5	62	14	65
1356	SO[1060]	-8240.5	338	14	65
1357	SO[1061]	-8257.5	202	14	65
1358	SO[1062]	-8274.5	62	14	65
1359	SO[1063]	-8291.5	338	14	65
1360	SO[1064]	-8308.5	202	14	65
1361	SO[1065]	-8325.5	62	14	65
1362	SO[1066]	-8342.5	338	14	65
1363	SO[1067]	-8359.5	202	14	65
1364	SO[1068]	-8376.5	62	14	65
1365	SO[1069]	-8393.5	338	14	65
1366	SO[1070]	-8410.5	202	14	65
1367	SO[1071]	-8427.5	62	14	65
1368	SO[1072]	-8444.5	338	14	65
1369	SO[1073]	-8461.5	202	14	65
1370	SO[1074]	-8478.5	62	14	65
1371	SO[1075]	-8495.5	338	14	65
1372	SO[1076]	-8512.5	202	14	65
1373	SO[1077]	-8529.5	62	14	65
1374	SO[1078]	-8546.5	338	14	65
1375	SO[1079]	-8563.5	202	14	65
1376	SO[1080]	-8580.5	62	14	65
1377	SO[1081]	-8597.5	338	14	65
1378	SO[1082]	-8614.5	202	14	65
1379	SO[1083]	-8631.5	62	14	65
1380	SO[1084]	-8648.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1381	SO[1085]	-8665.5	202	14	65
1382	SO[1086]	-8682.5	62	14	65
1383	SO[1087]	-8699.5	338	14	65
1384	SO[1088]	-8716.5	202	14	65
1385	SO[1089]	-8733.5	62	14	65
1386	SO[1090]	-8750.5	338	14	65
1387	SO[1091]	-8767.5	202	14	65
1388	SO[1092]	-8784.5	62	14	65
1389	SO[1093]	-8801.5	338	14	65
1390	SO[1094]	-8818.5	202	14	65
1391	SO[1095]	-8835.5	62	14	65
1392	SO[1096]	-8852.5	338	14	65
1393	SO[1097]	-8869.5	202	14	65
1394	SO[1098]	-8886.5	62	14	65
1395	SO[1099]	-8903.5	338	14	65
1396	SO[1100]	-8920.5	202	14	65
1397	SO[1101]	-8937.5	62	14	65
1398	SO[1102]	-8954.5	338	14	65
1399	SO[1103]	-8971.5	202	14	65
1400	SO[1104]	-8988.5	62	14	65
1401	SO[1105]	-9005.5	338	14	65
1402	SO[1106]	-9022.5	202	14	65
1403	SO[1107]	-9039.5	62	14	65
1404	SO[1108]	-9056.5	338	14	65
1405	SO[1109]	-9073.5	202	14	65
1406	SO[1110]	-9090.5	62	14	65
1407	SO[1111]	-9107.5	338	14	65
1408	SO[1112]	-9124.5	202	14	65
1409	SO[1113]	-9141.5	62	14	65
1410	SO[1114]	-9158.5	338	14	65
1411	SO[1115]	-9175.5	202	14	65
1412	SO[1116]	-9192.5	62	14	65
1413	SO[1117]	-9209.5	338	14	65
1414	SO[1118]	-9226.5	202	14	65
1415	SO[1119]	-9243.5	62	14	65
1416	SO[1120]	-9260.5	338	14	65
1417	SO[1121]	-9277.5	202	14	65
1418	SO[1122]	-9294.5	62	14	65
1419	SO[1123]	-9311.5	338	14	65
1420	SO[1124]	-9328.5	202	14	65
1421	SO[1125]	-9345.5	62	14	65
1422	SO[1126]	-9362.5	338	14	65
1423	SO[1127]	-9379.5	202	14	65
1424	SO[1128]	-9396.5	62	14	65
1425	SO[1129]	-9413.5	338	14	65
1426	SO[1130]	-9430.5	202	14	65
1427	SO[1131]	-9447.5	62	14	65
1428	SO[1132]	-9464.5	338	14	65
1429	SO[1133]	-9481.5	202	14	65
1430	SO[1134]	-9498.5	62	14	65
1431	SO[1135]	-9515.5	338	14	65
1432	SO[1136]	-9532.5	202	14	65
1433	SO[1137]	-9549.5	62	14	65
1434	SO[1138]	-9566.5	338	14	65
1435	SO[1139]	-9583.5	202	14	65
1436	SO[1140]	-9600.5	62	14	65
1437	SO[1141]	-9617.5	338	14	65
1438	SO[1142]	-9634.5	202	14	65
1439	SO[1143]	-9651.5	62	14	65
1440	SO[1144]	-9668.5	338	14	65

PAD No.	PAD Name	X-axis	Y-axis	W	H
1441	SO[1145]	-9685.5	202	14	65
1442	SO[1146]	-9702.5	62	14	65
1443	SO[1147]	-9719.5	338	14	65
1444	SO[1148]	-9736.5	202	14	65
1445	SO[1149]	-9753.5	62	14	65
1446	SO[1150]	-9770.5	338	14	65
1447	SO[1151]	-9787.5	202	14	65
1448	SO[1152]	-9804.5	62	14	65
1449	SO[1153]	-9821.5	338	14	65
1450	SO[1154]	-9838.5	202	14	65
1451	SO[1155]	-9855.5	62	14	65
1452	SO[1156]	-9872.5	338	14	65
1453	SO[1157]	-9889.5	202	14	65
1454	SO[1158]	-9906.5	62	14	65
1455	SO[1159]	-9923.5	338	14	65
1456	SO[1160]	-9940.5	202	14	65
1457	SO[1161]	-9957.5	62	14	65
1458	SO[1162]	-9974.5	338	14	65
1459	SO[1163]	-9991.5	202	14	65
1460	SO[1164]	-10008.5	62	14	65
1461	SO[1165]	-10025.5	338	14	65
1462	SO[1166]	-10042.5	202	14	65
1463	SO[1167]	-10059.5	62	14	65
1464	SO[1168]	-10076.5	338	14	65
1465	SO[1169]	-10093.5	202	14	65
1466	SO[1170]	-10110.5	62	14	65
1467	SO[1171]	-10127.5	338	14	65
1468	SO[1172]	-10144.5	202	14	65
1469	SO[1173]	-10161.5	62	14	65
1470	SO[1174]	-10178.5	338	14	65
1471	SO[1175]	-10195.5	202	14	65
1472	SO[1176]	-10212.5	62	14	65
1473	SO[1177]	-10229.5	338	14	65
1474	SO[1178]	-10246.5	202	14	65
1475	SO[1179]	-10263.5	62	14	65
1476	SO[1180]	-10280.5	338	14	65
1477	SO[1181]	-10297.5	202	14	65
1478	SO[1182]	-10314.5	62	14	65
1479	SO[1183]	-10331.5	338	14	65
1480	SO[1184]	-10348.5	202	14	65
1481	SO[1185]	-10365.5	62	14	65
1482	SO[1186]	-10382.5	338	14	65
1483	SO[1187]	-10399.5	202	14	65
1484	SO[1188]	-10416.5	62	14	65
1485	SO[1189]	-10433.5	338	14	65
1486	SO[1190]	-10450.5	202	14	65
1487	SO[1191]	-10467.5	62	14	65
1488	SO[1192]	-10484.5	338	14	65
1489	SO[1193]	-10501.5	202	14	65
1490	SO[1194]	-10518.5	62	14	65
1491	SO[1195]	-10535.5	338	14	65
1492	SO[1196]	-10552.5	202	14	65
1493	SO[1197]	-10569.5	62	14	65
1494	SO[1198]	-10586.5	338	14	65
1495	SO[1199]	-10603.5	202	14	65
1496	SO[1200]	-10620.5	62	14	65
1497	SHIELDING[51]	-10664	358	26	50
1498	COM_PASSR	-10714	358	26	50
1499	COM_PASSR	-10764	358	26	50
1500	SYNCR	-10814	358	26	50

PAD No.	PAD Name	X-axis	Y-axis	W	H
1501	LDR	-10864	358	26	50
1502	POLR	-10914	358	26	50
1503	DATR[0]	-11179	378.75	50	23.5
1504	DATR[1]	-11049	342	50	26
1505	DATR[2]	-11179	302	50	26
1506	DATR[3]	-11049	262	50	26
1507	DATR[4]	-11179	222	50	26
1508	DATR[5]	-11049	182	50	26
1509	DATR[6]	-11179	142	50	26
1510	DATR[7]	-11049	102	50	26
1511	DATR[8]	-11179	62	50	26
1512	DATR[9]	-11049	22	50	26
1513	DATR[10]	-11179	-18	50	26
1514	DATR[11]	-11049	-58	50	26
1515	DATR[12]	-11179	-128	50	26
1516	DATR[13]	-11049	-138	50	26
1517	DATR[14]	-11179	-178	50	26
1518	DATR[15]	-11049	-318	50	26
1519	DATR[16]	-11179	-258	50	26
1520	DATR[17]	-11049	-298	50	26
1521	NDVR	-11179	-338	50	26
1522	DCLRR	-11049	-376.5	50	26

PAD Name	X-axis	Y-axis
ALWIN_L	10773	78
ALWIN_R	10773	78

**9. DEFINITIONS****9.1. Data Sheet Status**

Data Sheet	This data sheet contains final product specifications.
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Contents in the document are subject to change without notice.

**9.2. Life Support Application**

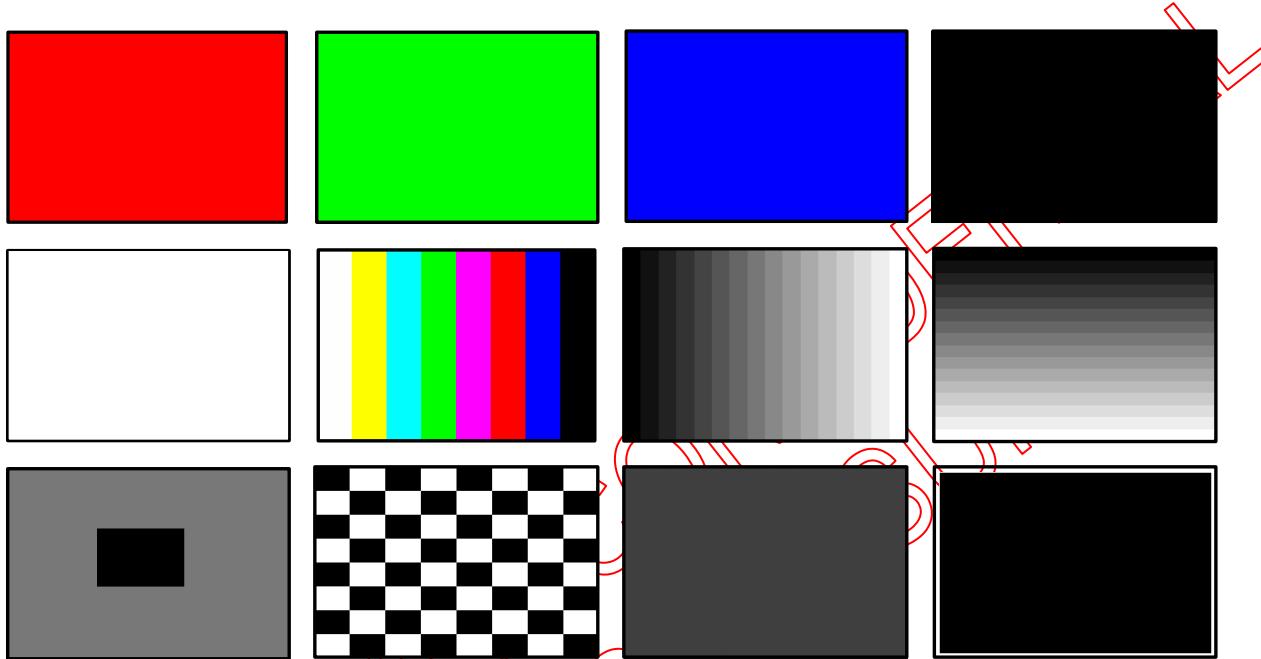
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**10. REVISION HISTORY**

Revision	Content	Page	Date
1.0	New spec.	--	2018/01/25
1.1	1. Timing characteristic dclk frequency value modify 2. Timing table clkin frequency modify	25~27 30	2018/03/27
1.2	Update Pad Coordinates	36~49	2018/06/08
1.3	Update Pad Coordinates	36~49	2018/09/21
1.4	Add VGH, VGL, VCOM in power on/off sequence	18	2019/0719
1.5	Modify VDD 1.7V ~ 3.6V	2 , 28	2019/08/13
1.6	Modify DE mode and SYNC mode application limit.	25~27	2020/05/19

### **APPENDIX A : BIST PATTERN**

R→G→B→Black→White→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame



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